Fully-Digital Rail-to-Rail OTA with Sub-1,000 m2 Area, 250-mV Minimum Supply and nW Power at 150-pF Load in 180nm

Fully-Digital Rail-to-Rail OTA with Sub-1,000 µm^2 Area, 250-mV Minimum Supply and nW Power at 150-pF Load in 180nm

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***Abstract*— A fully-digital operational transconductance amplifier (DIGOTA) architecture for tightly energy-constrained low-cost systems is presented. A 180nm DIGOTA testchip exhibits an area below the 1,000-µm^2 wall, and 2.4-nW power under 150pF load, and a minimum supply voltage V_{min} of 0.25 V. In the 0.3-0.5 V supply range, DIGOTA improves the area-normalized small (large) signal energy FoM by at least 836X (267X) over prior sub-500mV OTAs, while reducing area by 27-85X. The low-V_{min} and nW-power features are shown to enable direct harvesting at the mm scale.**

***Index Terms*—Operational Transconductance Amplifier (OTA), fully-digital, ultra-low power, ultra-low voltage, energy harvesting**

I. Introduction

Operational transconductance amplifiers (OTAs) are essential building blocks in integrated systems with sensing and/or power management capabilities. Their design is particularly challenging in tightly energy- and cost-constrained integrated systems such as sensor nodes for the Internet of Things, implantables, and other energy-harvested systems. In such cases, miniaturization mandates power down to nWs, small area, low design effort and technology/design portability, low minimum supply voltage $V_{\min}$ to withstand large harvested power fluctuations or enable direct harvesting to suppress the power of intermediate DC-DC conversion [1].

Most OTAs in prior art (see, e.g., [2]-[4]) operate above 1-V supply, and their power consumption is limited by their bias current. Such limitation is exacerbated at heavier capacitive loads, especially in multi-stage OTAs requiring complex frequency compensation schemes for stable closed-loop operation [2]-[3]. In prior art, sub-500mV operation comes at the cost of degraded energy efficiency, larger area and design complexity [5]-[7]. To mitigate the design effort of analog design techniques, digital OTAs were proposed [8]-[9] for seamless integration with logic and harvesters, digital-like area scaling versus technology and automated design, and easy porting across technology nodes. However, prior digital OTAs are not competitive in terms of performance and energy efficiency, require large on-chip passives and calibration, and no silicon demonstration has been presented so far [8]-[9].

In this work, a fully-digital OTA is introduced to enable operation at the nW-range power even at capacitive loads in the 100-pF range, and at low $V_{\min}$, while breaking the 1,000-µm^2 area wall for the first time. The ability to operate at low voltage and power is shown to enable direct powering from a light harvester, without requiring any intermediate DC-DC converter. The paper has the following structure. In Section II, the proposed DIGOTA architecture is introduced and its operation is described. Measurement results of the 180-nm testchip are discussed and compared with the state of the art in in Section III. Conclusions are drawn in Section IV.

II. Proposed Digital Operational Transconductance Amplifier (DIGOTA)

The schematic of the proposed digital OTA (DIGOTA) is presented in Fig. 1. As opposed to prior digital OTAs, DIGOTA does not need any passive component at the input stage, which is based on Muller C-element logic gates. The latter dynamically handle and compensate the effect of the common-mode without any calibration, as discussed in the following. Since all transistors operate in a digital fashion (either on or off), DIGOTA exhibits zero DC bias current and hence removes the traditional power floor imposed by bias currents and the necessity of current references, improving power efficiency.

In detail, the input differential stage is implemented by two Muller C-elements driven by the input voltages v_{IN+} and v_{IN-}. Their outputs v_{MUL+} and v_{MUL-} drive the INV+ and INV- inverter gates, whose digital outputs $\overline{MUL+}$ and $\overline{MUL-}$ govern the evolution of the circuit throughout the states A, B, C and D as detailed in Fig. 2a, so that to properly drive the output stage and the MCswap tri-state buffers. The latter alternately activates the Muller C-element pull-up or pull-down paths, resulting in a self-oscillating dynamic compensation of the common-mode input voltage, as illustrated in what follows.

Under DIGOTA open-loop operation with $v_D = v_{IN+} - v_{IN-} = 0$ and v_{MUL+}=v_{MUL-}=0V at t=0, the output of INV+ and INV- is $\overline{MUL+}$=$\overline{MUL-}$=1, which sets the DIGOTA state A (Fig. 2a). In this state, the output stage is disabled and the MCswap output *PD* in Fig. 1 is forced low as in Fig.2b, thus enabling only the pull-up network of the Muller C-elements. As shown in Fig. 3, the output parasitic capacitances $C_{\rm MUL}$, assumed to be equal, are charged by equal currents $I_{MC,A}$ as in Fig. 2b (black line in Fig. 3, right after t=0) and v_{MUL+} and v_{MUL-} increase at the same rate $I_{MC,A}/C_{\rm MUL}$ and cross the INV+ and INV- trip point $V_{\rm trip}$ at the same time, making $\overline{MUL+}$=$\overline{MUL-}$=0 and

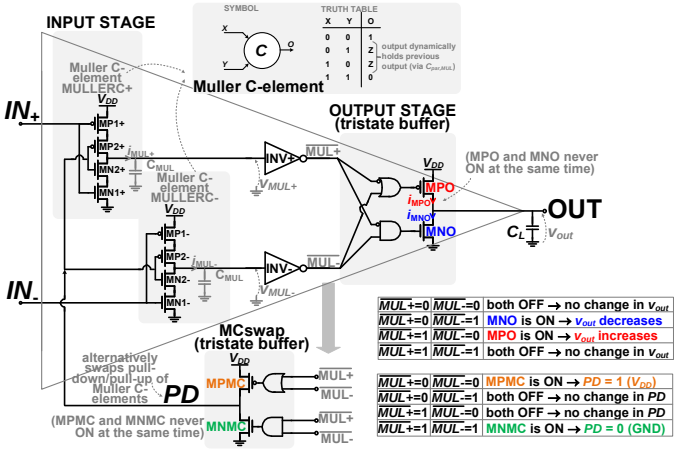

Fig. 1. Schematic of the proposed DIGOTA circuit.

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setting the state *C* from Fig. 2a. After the propagation delay t_D of the logic in the MCswap control loop, the pull-down network of the Muller C-elements is enabled as in Fig. 2b, and v_{MUL+} and v_{MUL-} decrease at the same rate $I_{MC,C}/C_{\mathrm{MUL}}$ until they cross V_{trip}. Being ΔV_{MUL} the swing of the v_{MUL+}=v_{MUL-} signals, the circuit oscillates between states A and C with period

$$T_0 = \frac{1}{f_0} = \frac{\Delta V_{MUL} C_{\mathrm{MUL}}}{2\, I_{MC,A}} + \frac{\Delta V_{MUL} C_{\mathrm{MUL}}}{2\, I_{MC,C}} + 2t_D. \quad (1)$$

Since $I_{MC,A}$ and $I_{MC,C}$ have opposite dependence on common-mode input, the self-oscillation frequency in (1) is nearly independent of it.

When a positive differential input voltage v_D is applied at time $t = t_0$ in Fig. 3, two opposite small-signal components $\pm g_m v_D/2$ are added to the current $I_{MC,A}$ drawn by MP1+ and MP1- in state A, and the waveforms of v_{MUL+} and v_{MUL-} become different (blue and red in Fig. 3) by an amount $\delta v_{MUL} = v_{MUL+} - v_{MUL-}$ proportional to the differential current $g_m v_D$ integrated in C_{MUL}, and cross V_{trip} at different points of time t_1 and t_2 in Fig. 3. Their difference in (2)

$$\Delta t_{12} = \frac{(\Delta V_{MUL}+\delta v_{MUL})\, C_{\mathrm{MUL}}}{2\, I_{MC,A}} - \frac{(\Delta V_{MUL}-\delta v_{MUL})\, C_{\mathrm{MUL}}}{2 I_{MC,A}} \simeq \frac{\delta v_{MUL} C_{\mathrm{MUL}}}{I_{MC,A}} \quad (2)$$

is therefore proportional to δv_{MUL} and hence to the integrated input differential voltage v_D. In other words, the Muller C-element performs voltage-to-time conversion, thus enabling efficient time-domain processing at low voltages. During Δt_{12}, $\overline{MUL+}$ and $\overline{MUL-}$ are at different logic levels, moving the state from A to B in Fig. 3, thus enabling the output stage, which charges (discharges) the load capacitance C_L at the on-current I_{ON} of transistor MPO (MNO). In turn, the output voltage v_{OUT} increases/decreases by an amount Δv_{OUT} proportional to Δt_{12} and hence to v_D. In other words, the output stage inherently performs the time-to-voltage conversion. After t_2 in Fig. 3, both v_{MUL+} and v_{MUL-} cross the inverter trip point and lead to state C, in which the output stage is disabled and the pull-down network of the Muller C-elements is enabled after t_D, the input

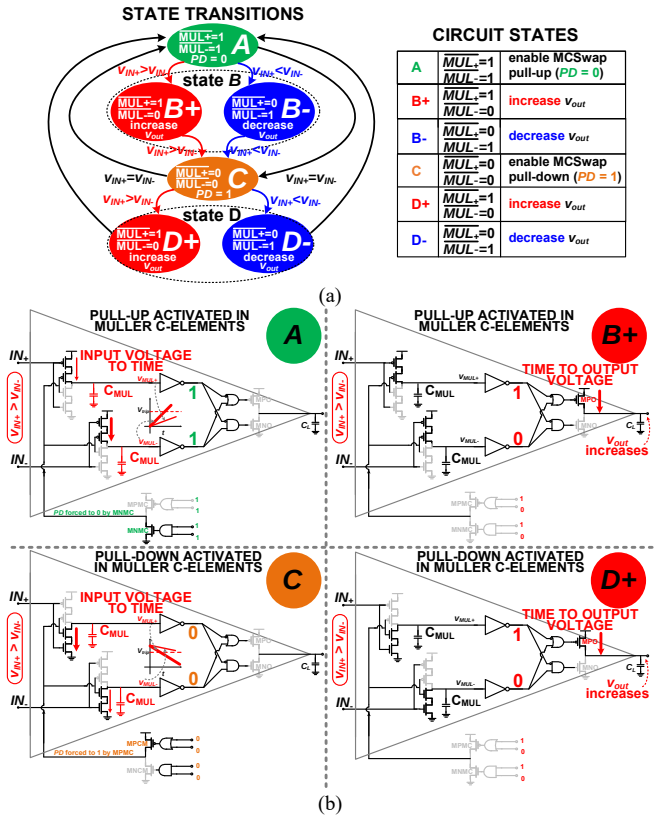

Fig. 2. DIGOTA operation throughout its digital states: a) state transition diagram, b) transistor-level detail for each state, assuming v_D>0.

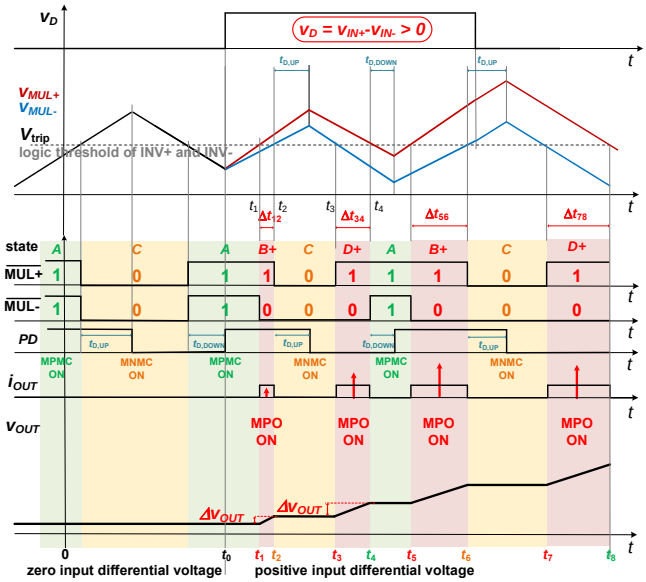

Fig. 3. DIGOTA states: a) state transition graph and b) transistor level detail for each state, assuming v_D>0.

differential voltage keeps being integrated in δv_{MUL} and v_{MUL+} and v_{MUL-} cross the inverter trip point at different time t_4 (t_3). As a result, the state moves from C to D in Fig. 3, in which it remains for a time $\Delta t_{34} = t_3 - t_4$ proportional to δv_{MUL}, during which the output stage is operated in a similar fashion as in state B. Then, DIGOTA returns in state A and the same sequence is repeated.

Below the self-oscillating frequency f_0, the DIGOTA operation can be described by a small-signal frequency response with a dominant pole at the output node $s_{p1} = -\overline{g_{out}}/C_L$ ($\overline{g_{out}}$ is the time-averaged DIGOTA output conductance, very low since the output stage is in high impedance most of the time). The DIGOTA gain-bandwidth product (GBW) is upper-limited by the self-oscillation frequency f_0 in (1) and the pole $s_{p2} = -g_o/C_{MUL}$ at the Muller C-element output. The output slew rate is limited to I_{ON}/C_L.

The DC gain is given by the product of three terms: a) the gain from v_D to δv_{MUL} (i.e., g_m/g_o, which is limited by the finite output conductance g_o of the Muller C-element), b) the voltage-to-time conversion gain $C_{\mathrm{MUL}}/I_{MC,A/C}$ in INV+/INV- given in (2); c) the time-to-voltage conversion gain $I_{ON}/(T_0\, \overline{g_{out}})$ at the output stage. The common-mode dependence of the MP1+/- current $I_{MC,A}$ in state A is compensated by an opposite dependence of the current of MN1+/- in state C. Hence, the DC gain is nearly independent of the common mode. The DIGOTA performance in terms of noise and offset and their drift over process and temperature are determined by the input devices MP1+/- and MN1+/-, as in traditional OTAs. The adoption of more advanced technologies expectedly increases the self-oscillation frequency from (1), decreases the DC gain due to the reduction in the intrinsic transistor gain and the capacitance C_{MUL}, while increasing the ON current of the output stage I_{ON} and the DIBL-related output conductance $\overline{g_{out}}$ of the devices in the output stage.

III. DIGOTA Testchip and Measurement Reults

A 180 nm testchip was designed with logic standard cells (Fig. 4), targeting ultra-low power, low area and able to drive large capacitive loads at ultra-low voltage as primary design requirements. The fabricated DIGOTA testchip occupies a total area of 982 μm^2. Measurements of the DIGOTA circuit in the voltage follower configuration under 0.3-V supply are reported in Fig. 5, which shows the expected OTA operation under sinewave and square wave inputs.

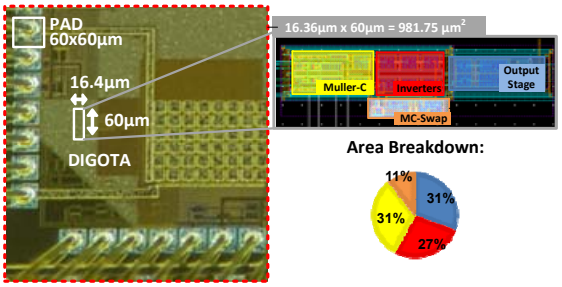

Fig. 4. Micrograph of the DIGOTA 180 nm testchip and area breakdown.

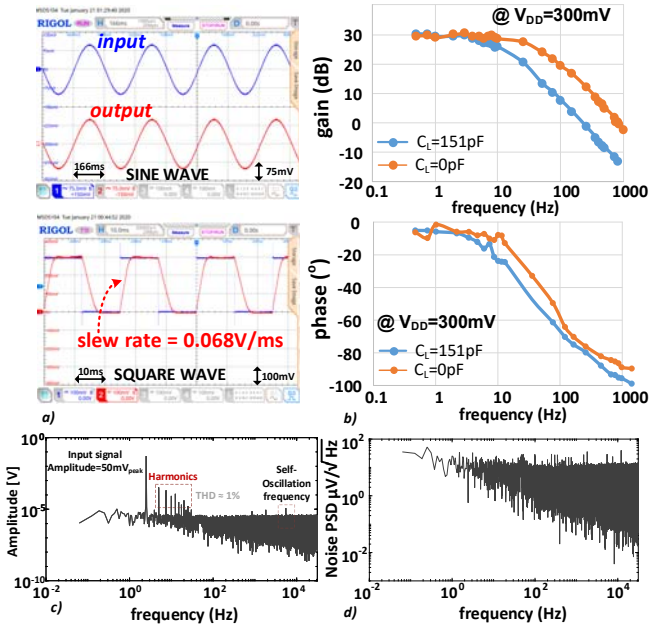

Fig. 5. a) sine/square wave response (3-Hz frequency, 75-mV ampl.), b) open-loop frequency response (V_{DD}=0.3 V), c) wideband output spectrum (sine input, 2.5-Hz, 75-mV ampl.), d) input noise spectrum.

The OTA exhibits 30-dB DC gain, 250-Hz (1-kHz) gain-bandwidth product GBW, 90° (85°) phase margin under 150 pF (0 pF) off-chip load. Under a square wave input and 150-pF load, the rising/falling slew rate (SR) are 0.068/0.101 V/ms, respectively. The wideband output spectrum for a 2.5-Hz input at 150-pF load is reported in Fig. 5c, revealing harmonics and the out-of-band self-oscillation frequency tone at 8kHz. The noise spectrum is reported in Fig. 5d.

The measured total harmonic distortion THD in Fig. 6 is less than 2% at more than 90% of the rail-to-rail swing. THD is nearly independent of the signal amplitude, due to the nonlinearity of the input devices MP1+,MP1-,MN1+,MN1- (increasing with amplitude) and from the "dead-zone" nonlinearity of the output stage, which generates distortion at low input signal amplitude. The measured

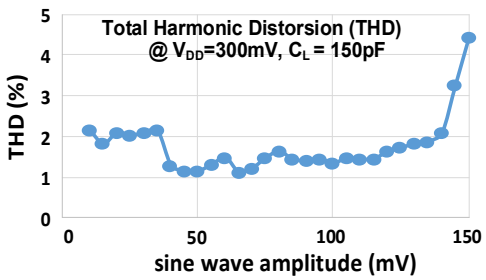

Fig. 6. THD vs input amplitude for a 3-Hz sinewave input signal.

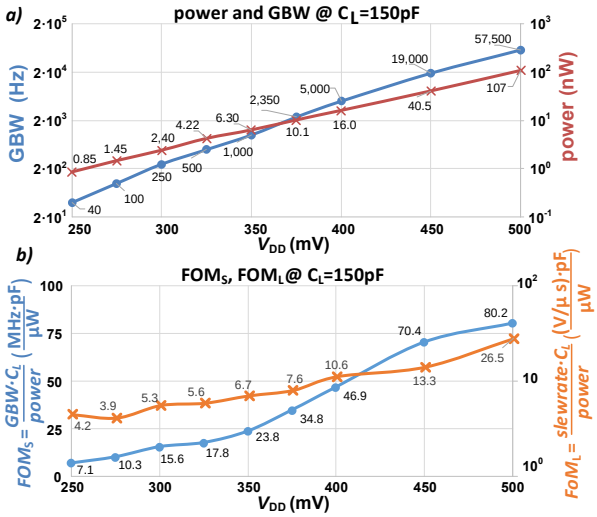

Fig. 7. DIGOTA characterization vs V_{DD}: a) power (3Hz, 50-mV sine wave input) and GBW, b) small (large) signal energy efficiency FoMs (FoML) [3].

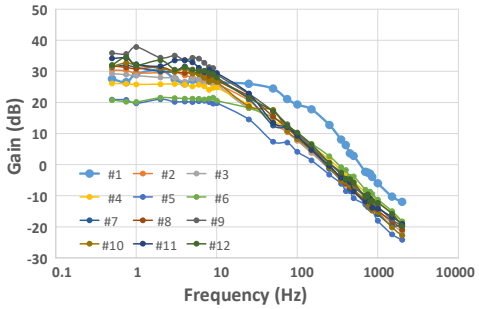

Fig. 8. Open-loop frequency response across 12 dice.

CMRR and the PSRR are 41 dB and 30 dB, respectively. The open-loop output resistance is 21 MΩ. The input-referred noise is 21µV_{RMS}, whereas the mean (standard deviation) measured offset for 12 measured samples is 1.3mV (4.9mV).

From Fig. 7a, the DIGOTA power consumption and GBW at 27°C under a 250-500 mV power supply and 150-pF capacitive load range from 850 pW to 107 nW and from 40 Hz to 57.5 kHz. Based on simulations, DIGOTA power and GBW increase with temperature by 10%/°C and 3%/°C, as expected from the sub-threshold nature of the transistor currents. To evaluate the corresponding energy efficiency, the small- and large-signal figures of merit are evaluated as [2]-[7]:

$$FOM_S = \frac{GBW \cdot C_L}{power} \quad (3a) \qquad FOM_L = \frac{SR \cdot C_L}{power} \quad (3b)$$

$$FOM_{S,A} = \frac{GBW \cdot C_L}{power \cdot area} \quad (3c) \qquad FOM_{L,A} = \frac{SR \cdot C_L}{power \cdot area} \quad (3d)$$

of which (3c) and (3d) also include the area efficiency. The first two figures of merit are plotted in Fig. 7b and are in the 7.1-80.2 MHz·pF/µW and in the 4.2-26.5 V/µs·pF/µW range, respectively. The other two are omitted as they are simply a scaled version of them. Fig. 8 shows the measured open-loop frequency response across 12 dice.

The comparison with the state of the art of ultra-low voltage ultra-low power OTAs is presented in Table I. At 0.3-V supply the proposed OTA achieves an energy efficiency FOMs=15.63MHz·pF/µW, which improves prior art on sub-500 mV OTAs by 1.5-34X [5]-[7], as shown in Fig. 9. Over the latter, the proposed OTA consumes the lowest power (7.5X-45,800X less than others), and drives the largest output capacitance (7.5X-75X compared to others). From an area efficiency viewpoint, the proposed OTA occupies the smallest area (27-85X

TABLE I. OTA PERFORMANCE COMPARISON (BEST PERFORMANCE IN BOLD)

	$V_{DD} \leq 500$mV				$V_{DD} > 500$mV			
	[5]	[6]	[7]	This work	[2]	[3]	[4]	This work
supply voltage used for comparison (minimum voltage V_{min}) [V]	0.5 (0.45)	0.3 (0.3)	0.25 (0.25)	0.3 (0.25)	1.1 (1.1)	1.2 (1.2)	2 (2)	0.5 (0.25)
design	custom	custom	custom	**std cell**	custom	custom	custom	**std cell**
OTA architecture	bulk-driven	gate-driven	bulk-driven	digital	PSS amplifiers	Miller	folded Cascode	digital
Ext. current reference needed (Y/N)	Y	N	Y	N	Y	Y	Y	N
technology [nm]	180	130	130	180	180	180	500	180
area (μm^2)	26,000	-	83,000	**982**	2,100	13,000	30,000	**982**
normalized area ($10^3 \cdot F^{-2}$)	802.47	-	4,911	**30.3**	64.81	401.23	120	**30.3**
cap load C_L [pF]	20	2	15	**150**	100	**18,000**	70	150
power [µW]	110[a]	1.8	0.018[a]	**0.0024**[b]	7.4[a]	69.6[a]	100[a]	**0.1075**[b]
DC gain [dB]	52	49.8	**60**	30	100	100	76.8	73
GBW [kHz]	2,500	**9,100**	1.88	0.250	1,660	1,180	3,400	57.5
average slew rate SR [V/µs]	2.89	**3.8**	0.0007	0.000085	8.67	0.22	19.25	0.019
in-band input noise [µV]	442.7	105.6	143	**21**	-	-	**42.41**	122
CMRR [dB]	78	-	-	41	-	-	112	65
PSRR [dB]	76	-	-	30	-	-	92	50
THD [%]	1.0	-	1.0	2.0	-	-	-	1.0
FOM_S [MHz · pF/µW]	0.45	10	1.6	**15.6**	22.4	**305.2**	2.4	80.2
FOM_L [(V/µs) · pF/µW]	0.52	4.2	0.58	**5.3**	**117.2**	56.9	13.5	26.5
area-normalized $FOM_{S,A}$ $\left[\frac{MHz \cdot pF}{\mu W \cdot mm^2}\right]$	17.3	-	19	**15,885**	10,666	23,477	80	**81,724**
area-normalized $FOM_{L,A}$ $\left[\frac{V/\mu s \cdot pF}{\mu W \cdot mm^2}\right]$	20.2	-	7	**5,397**	**55,792**	4,377	450	27,000

[a] The consumption of the current reference is not accounted for

[b] Evaluated at 3-Hz, 50-mV input

lower than others), and the resulting figures of merit in (1c)-(1d) are improved by 836X and 267X, respectively. This is achieved at the cost of reduced DC gain (30 dB lower than the highest), PSRR/CMRR (37/46dB lower than [5]), reduced bandwidth (7.5X-36,000X less) and slew rate (8.2X-44,700X lower), and increased (+1%) harmonic distortion.

At 0.5 V, the DIGOTA performance improves to 73-dB DC gain, GBW=57.5 kHz and 19 V/ms slew rate. Even compared to OTAs with higher supply (1.1-2V [2]-[4]), DIGOTA exhibits the lowest power, the second best FOMs and $FOM_{L,A}$, and the best $FOM_{S,A}$, confirming the ability of DIGOTA to efficiently drive heavy capacitive loads.

The low power and high energy and area efficiency of DIGOTA make it well suited for low-cost systems operating directly off of the energy harvester voltage, as experimentally demonstrated by proper operation when powered by a 7 mm^2 solar cell at very dim light (<100lux, dark overcast day), or equivalently at 1-2 mm^2 at indoor light (500 lux).

IV. CONCLUSION

A compact and energy-efficient digital OTA has been proposed and demonstrated in 180 nm. The proposed OTA exhibits the lowest area (982 μm^2) and power (2.4 nW) reported to date, and operates down to 250 mV, at lower DC gain, PSRR, CMRR and bandwidth compared to other ultra-low voltage OTAs. At 300 mV, the best FOMs, FOM_L, $FOM_{S,A}$ and $FOM_{L,A}$ are achieved among sub-500mV OTAs, with a 836X and 267X improvement on the latter two, thanks to the improved energy and area efficiency. At 500-mV supply, the energy efficiency is still competitive with previously proposed OTAs operating at above-1 V supplies.

The ability to operate at ultra-low voltage and power has been demonstrated in the context of energy-autonomous sensor nodes, as directly powered by a small energy harvester (7-mm^2 solar cell) at dim light <100 lux (dark overcast day).

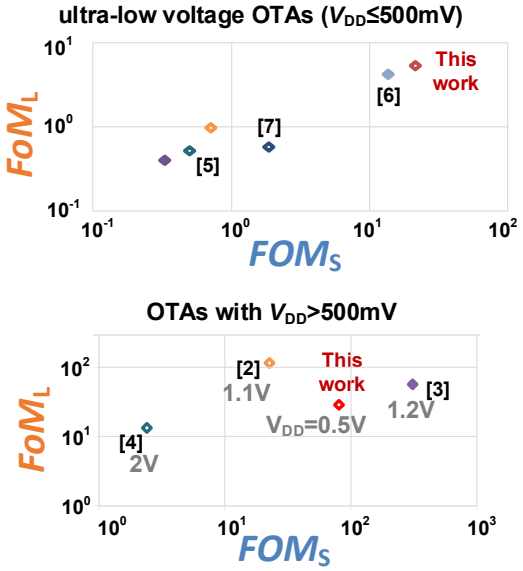

Fig. 9. FOMs and FOM_L energy efficiency: comparison with OTAs with V_{DD}≤500mV and V_{DD}>500mV.

REFERENCES

[1] L. Lin, S. Jain, M. Alioto, "Multi-Sensor Platform with Five-Order-of-Magnitude System Power Adaptation down to 3.1nW and Sustained Operation under Moonlight Harvesting," in *VLSI Symposium 2020*.

[2] S. Hong *et al.*, "7.4µW Ultra-high slew-rate pseudo single-stage amplifier driving 0.1-to-15nF capacitive load with >69° phase margin," in *VLSI Symposium 2015*, pp. 296-297.

[3] W. Qu *et al.*, "Design-Oriented Analysis for Miller Compensation and Its Application to Multistage Amplifier Design," *IEEE J. of Solid-State Circuits*, vol. 52, no. 2, pp. 517-527, Feb. 2017.

[4] M. P. Garde *et al.*, "Super Class-AB Recycling Folded Cascode OTA," in *IEEE J. of Solid-State Circuits*, vol. 53, no. 9, pp. 2614-2623, Sept. 2018.

[5] S. Chatterjee *et al.*, "0.5-V analog circuit techniques and their application in OTA and filter design," *IEEE J. of Solid-State Circuits*, vol. 40, no. 12, pp. 2373-2387, Dec. 2005

[6] L. Lv, X. *et al.*, "Inverter-Based Subthreshold Amplifier Techniques and Their Application in 0.3-V ΔΣ-Modulators," *IEEE J. of Solid-State Circuits*, vol. 54, no. 5, pp. 1436-1445, May 2019.

[7] L. H. C. Ferreira *et al.*, "A 60-dB Gain OTA Operating at 0.25-V Power Supply in 130-nm Digital CMOS Process," *IEEE Trans. on Circuits and Systems – part I*, vol. 61, no. 6, pp. 1609-1617, June 2014.

[8] P. Toledo, *et al.*, "A 300mV-Supply, 2nW-Power, 80pF-Load CMOS Digital-Based OTA for IoT Interfaces," in Proc. of *IEEE ICECS*, Genoa, Italy, 2019, pp. 170-173.

[9] P. S. Crovetti, "A Digital-Based Analog Differential Circuit," *IEEE Trans. on Circ. and Syst.– I*, vol. 60, no. 12, pp. 3107-3116, Dec. 2013.