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Error sources in electronic fully-digital impedance bridges

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***Abstract*—We present here a comprehensive analysis of the error sources in electronic fully-digital impedance bridges, for both sourcing and digitizing bridges. This work can be used as a basis to optimize the design and the operating parameters of digital bridges, and in the evaluation of the uncertainty.**

***Index Terms*—Impedance measurement, bridge circuits, measurement errors, measurement uncertainty, calibration**

I. Introduction

In recent years, electronic fully-digital impedance bridges based on polyphase digital signal sources have emerged as devices suitable for primary impedance metrology [1], [2]. With typical accuracies in the 10^{-6}–10^{-5} range, these kinds of bridges are not as accurate as traditional transformer-ratio bridges, but can measure impedances across the whole complex plane and are characterized by affordable cost, short measuring time and ease of operation. These features make them of interest for calibration laboratories.

We present here a comprehensive analysis of the error sources in electronic fully-digital bridges for two standard architectures: *sourcing* (*DAC-based*) bridges, where an impedance ratio is compared to a reference ratio determined from the settings of a digital signal source; and *digitizing* (*sampling* or *ADC-based*) bridges, where an impedance ratio is compared to a ratio determined from digitized samples.

II. Sourcing bridges

For the purpose of analyzing error sources, common four-terminal-pair fully-digital impedance bridges can be reduced to the basic schematic of Fig. 1 on the next page, where the network of a sourcing bridge is represented by black and red lines. Relevant quantities and symbols are defined therein.

For the balanced bridge, the impedance ratio is given by

$$W = \frac{Z_1}{Z_2} = -\frac{E_1}{E_2}. \tag{1}$$

In a sourcing bridge, the readings E_1^{read} and E_2^{read} of the voltage phasors E_1 and E_2 are computed from the samples used to synthesize the two waveforms. Due to the source non-idealities, the actual voltage phasors differ from the readings, $E_k = [1 + g_k(E_k^{\mathrm{read}})]E_k^{\mathrm{read}}$, $k = 1, 2$, with $g_k(E_k^{\mathrm{read}})$ representing a possibly voltage-dependent complex gain error that accounts for nonlinear magnitude and phase errors. This error can be partially compensated by performing two measurements (*channel swapping*), one with E_1 and E_2 connected as in Fig. 1 (F configuration) and one with the two channels exchanged (R configuration), and by computing the reading $W^{\mathrm{read}} = \sqrt{E_{1\mathrm{F}}^{\mathrm{read}} E_{2\mathrm{R}}^{\mathrm{read}} / (E_{2\mathrm{F}}^{\mathrm{read}} E_{1\mathrm{R}}^{\mathrm{read}})}$.

The impedance ratio W differs from W^{read} by the error $\Delta W = W^{\mathrm{read}} - W$. The main components of this error are: i) the *source nonlinearity*, that is, the dependence of the gain errors g_k from the generated voltages, $g_k = g_k(E_k^{\mathrm{read}})$; ii) the *source crosstalk*, that is, the interference of one source channel onto another, $E_j = E_j^{\mathrm{read}} + \sum_{k \neq j} a_{jk} E_k^{\mathrm{read}}$; iii) the *bridge unbalance*, that is, the deviations of V_{L1}, V_{L2}, V_{H1} and V_{H2} from zero; and iv) the *source loading*, that is, the fact that E_1 and E_2 have to energize the stray admittances Y_{H1} and Y_{H2} through the source output impedance z. Tab. I reports, for each error component, the error equation $\Delta W / W^{\mathrm{read}}$ which results from the analysis of the circuit of Fig. 1, by considering channel swapping. In four-terminal-pair sourcing bridges, the source loading effect is typically negligible, for the mismatch $Y_{\mathrm{H1}} - Y_{\mathrm{H2}}$ is usually small compared to z^{-1}.

III. Digitizing bridges

The network of a digitizing bridge is represented in Fig. 1 by black and blue lines. The impedance ratio is given by (1). In a digitizing bridge, the readings E_1^{read} and E_2^{read} of the voltage phasors E_1 and E_2 are computed from the digitized samples. The digitizer is based on an analog-to-digital converter (ADC) which reads the voltages at the high- and low-potential ports of the impedances Z_1 and Z_2 (the detector D and the digitizer V can be then the same device).

Equations similar to those reported in Tab. I can be derived also for the error sources of a digitizing bridge, just by

TABLE I

BRIDGE ERROR COMPONENTS AND MODELS. FOR THE LOW UNBALANCE TERM, $V_{\mathrm{L}} = (V_{\mathrm{L1}} + V_{\mathrm{L2}})/2$ AND $\Delta V_{\mathrm{L}} = V_{\mathrm{L1}} - V_{\mathrm{L2}}$. FOR THE CROSSTALK TERM, FOR BREVITY, ONLY THE TWO MAIN CHANNELS ARE CONSIDERED.

Error source	Error model	$\Delta W/W^{\mathrm{read}}$
Source nonlinearity	$g_j = g_j(E_k^{\mathrm{read}})$	$-\frac{1}{2}[g_1(E_{\mathrm{1F}}^{\mathrm{read}}) - g_1(E_{\mathrm{1R}}^{\mathrm{read}}) - g_2(E_{\mathrm{2F}}^{\mathrm{read}}) + g_2(E_{\mathrm{2R}}^{\mathrm{read}})]$
Source crosstalk	$E_j = E_j^{\mathrm{read}} + \sum_{k\neq j} a_{jk} E_k^{\mathrm{read}}$	$-\frac{1}{2}\left[a_{12}\left(\frac{E_{\mathrm{2F}}^{\mathrm{read}}}{E_{\mathrm{1F}}^{\mathrm{read}}} - \frac{E_{\mathrm{2R}}^{\mathrm{read}}}{E_{\mathrm{1R}}^{\mathrm{read}}}\right) - a_{21}\left(\frac{E_{\mathrm{1F}}^{\mathrm{read}}}{E_{\mathrm{2F}}^{\mathrm{read}}} - \frac{E_{\mathrm{1R}}^{\mathrm{read}}}{E_{\mathrm{2R}}^{\mathrm{read}}}\right)\right]$
Low unbalance	$V_{\mathrm{L}j} \neq 0$	$\frac{1}{2}\left[\left(1 + W + \frac{Y_{\mathrm{L}}}{Y_1}\right)\left(\frac{V_{\mathrm{LF}}}{E_{\mathrm{1F}}^{\mathrm{read}}} + \frac{V_{\mathrm{LR}}}{E_{\mathrm{2R}}^{\mathrm{read}}}\right) + \frac{1-W}{2}\left(\frac{\Delta V_{\mathrm{LF}}}{E_{\mathrm{1F}}^{\mathrm{read}}} + \frac{\Delta V_{\mathrm{LR}}}{E_{\mathrm{2R}}^{\mathrm{read}}}\right)\right]$
High unbalance	$V_{\mathrm{H}j} \neq 0$	$-\frac{z}{2Z_{\mathrm{m}}}\left(\frac{V_{\mathrm{H1F}}}{E_{\mathrm{1F}}^{\mathrm{read}}} - \frac{V_{\mathrm{H1R}}}{E_{\mathrm{1R}}^{\mathrm{read}}} - \frac{V_{\mathrm{H2F}}}{E_{\mathrm{2F}}^{\mathrm{read}}} + \frac{V_{\mathrm{H2R}}}{E_{\mathrm{2R}}^{\mathrm{read}}}\right)$
Source loading	$Y_{\mathrm{H}j} \neq 0$	$z(Y_{\mathrm{H1}} - Y_{\mathrm{H2}})$

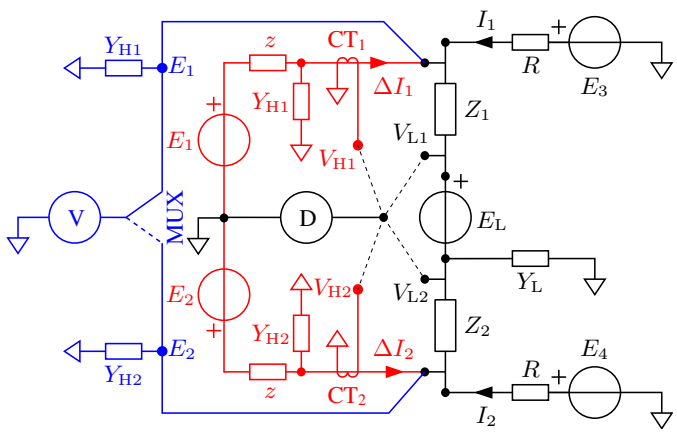

Fig. 1. Basic schematic of a typical four-terminal-pair fully-digital impedance bridge, with relevant stray parameters (smaller box elements): black and red lines represent the network of a sourcing bridge; black and blue lines represent that of a digitizing one. For a sourcing bridge, the impedance ratio Z_1/Z_2 is directly compared to the reference voltage ratio E_1/E_2 generated by two channels of a polyphase digital signal source. For a digitizing bridge, the impedance ratio Z_1/Z_2 is directly compared to the reference voltage ratio E_1/E_2 measured by the digitizer V, alternatively switched between the two impedances Z_1 and Z_2 through the multiplexer MUX. E_{L}, E_3 and E_4 are auxiliary signals used to realize the four-terminal-pair impedance definition. In particular, E_3 and E_4 generate, through the resistances R, the currents I_1 and I_2 driving Z_1 and Z_2. In a sourcing bridge, the current transformers CT_1 and CT_2 measure ΔI_1 and ΔI_2 with associated mutual impedances Z_{m}, such that $V_{\mathrm{H1}} = Z_{\mathrm{m}}\Delta I_1$ and $V_{\mathrm{H2}} = Z_{\mathrm{m}}\Delta I_2$. The output impedances of E_1 and E_2 are represented by z. Y_{H1} and Y_{H2} are the interconnection stray admittances between the channels outputs and ground. Y_{L} is the stray admittance between the low terminal pairs of Z_1 and Z_2 and ground. Sourcing bridges are balanced when $V_{\mathrm{L1}} = V_{\mathrm{L2}} = 0$ and $V_{\mathrm{H1}} = V_{\mathrm{H2}} = 0$ (or, equivalently, $\Delta I_1 = \Delta I_2 = 0$). The balance is checked by cycling the synchronous detector D, referenced at the frequency f, through the terminals V_{L1}, V_{L2}, V_{H1} and V_{H2}. Digitizing bridges are instead balanced when $V_{\mathrm{L1}} = V_{\mathrm{L2}} = 0$.

reinterpreting the meaning of some bridge parts. In this type of bridge, the actual voltages differ from the readings due to the ADC non-idealities, instead of the source non-idealities. The complex gain error is usually partially compensated by performing the measurements of E_1 and E_2 and, respectively, V_{L1} and V_{L2}, with the same digitizer. The usage of just one digitizer in the bridge requires a multiplexer (MUX in Fig. 1) to switch the digitizer input between different measurement points. The crosstalk between the channels of this multiplexer, which is counterpart to the crosstalk between channels in the sourcing bridge, causes a measurement error. Finally, the digitizer with its finite input impedance and the interconnecting cables load the high-potential ports of Z_1 and Z_2 with the admittances Y_{H1} and Y_{H2}, as a counterpart to the source loading effect. However, in the case of a digitizing bridge, the loading effect can be higher, and suitable buffers with high input impedance may need to be placed between the high-potential ports and the digitizer input.

IV. CONCLUSIONS

The error analysis herewith presented is intended as a tool useful both in the design of digital bridges, by allowing an informed choice of the bridge topology and components, and during its operation, to calculate corrections to the bridge readings and to evaluate the measurement uncertainty.

The modelling presented allows one to analyze both sourcing and digitizing bridges. The influence of the different error sources on the measurement outcome is strongly dependent on the bridge type, specific properties of the components employed, and the values of the standards being compared. As a rule of thumb, sourcing bridges might be more suitable for the comparison of high-valued impedances, digitizing bridges for low-valued ones.

At the time of the Conference, we shall present the application of this error analysis to digital bridges and impedance measurements performed in the framework of the project EMPIR 17RPT04 VersICaL: *A versatile impedance calibration laboratory based on digital impedance bridges*.

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