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ABSTRACT - Power electronic systems employing Printed Circuit Boards (PCBs) are broadly used in many applications, including some safety-critical ones. Several standards (e.g., ISO26262 for the automotive sector and DO-178 for avionics) mandate the adoption of effective test procedures for all electronic systems. However, the metrics to be used to compute the effectiveness of the adopted test procedures are not so clearly defined for power devices and systems. In the last years, some commercial fault simulation tools (e.g., DefectSim by Mentor Graphics and TestMAX by Synopsys) for analog circuits have been introduced, together with some new fault models. With these new tools, systematic analog fault simulation finally became practically feasible. The aim of this paper is twofold: first, we propose a method to extend the usage of the new analog fault models to power devices, thus allowing to compute a Fault Coverage figure for a given test. Secondly, we adopt the method on a case study, for which we quantitatively evaluate the effectiveness of some test procedures commonly used at the PCB level for the detection of faults inside power devices. A typical Power Supply Unit (PSU) used in industrial products, including power transistors and power diodes, is considered. The analysis of the gathered results shows that using the new method we can identify the main points of strength / weakness of the different test solutions in a quantitative and deterministic manner, and pinpoint the faults escaping to each one.

INDEX TERMS - End-of-manufacturing test, Functional test, In-circuit test, Incoming inspection test, PCB test, Power electronics, Fault Coverage, Fault models

I. INTRODUCTION

Electrical systems are often composed of a digital and an analog part. The digital part is normally devoted to the control of the system, while the analog part performs different functions, such as managing the sensors and/or the actuators (including power devices). Some of the applications using mixed analog and digital components are safety critical. In this case, a fault in the system can cause significant physical damage to people or produce a considerable economic damage. To increase the reliability of safety-critical systems, testing plays a crucial role: by detecting permanent faults before they produce critical failures, the dependability of the system can be increased. Numerous test techniques have been developed for testing the digital electronics, for example by resorting to Design for Testability [1]. The identification of well-accepted fault models for the digital electronic parts has allowed to develop efficient test strategies. For example, the stuck-at fault model is widely adopted to estimate the effectiveness of a test procedure for digital components and to quantitatively compare the Fault Coverage (FC) [1] results obtained with different test approaches. The stuck-at fault model is easily defined thanks to the binary behavior of digital electronics. In contrast, in analog electronics the electrical quantities are continuous in time. Therefore, it is not easy to identify a suitable fault model, as discussed in [1][2]. The absence of a fault model does not allow to quantitatively assess the real effectiveness of a test procedure for analog components and to quantitatively compare the effectiveness of different test procedures. For this reason, the test procedures for analog circuits or modules are often qualitatively evaluated [3], only. Currently, the effectiveness of a test procedure for an analog circuit or module is often assessed first resorting to an empirical approach based on functional coverage, and then on statistical evidence based on the defective items returned from the field [3]. In particular, each returned defective item is analyzed to identify the cause of the malfunction; thereafter, the tests are then improved for detecting the new malfunction cause. This method is strongly based on the engineers' experience and requires a long time and a high cost to obtain effective tests.

An electronic system may consist of one or more Printed Circuit Boards (PCBs), which clearly require some test strategies, matching the target reliability figures and the quality of the manufacturing process. Different test strategies have been developed over the years for the test of PCBs, e.g., based on in-circuit and functional test. Furthermore, some testing strategies have been developed to test the power devices on the PCBs after they have been mounted on the PCB. However, there is no universally accepted metric for evaluating the ability of the different test strategies to detect faults possibly existing in the PCB at the end of the manufacturing process. The PCOLA/SOQ [4] method is an effort in this direction. However, the PCOLA/SOQ metric mainly addresses defects in the PCB assembly (e.g., the absence of a component, or its wrong assembly, or a defect in the connections), while it is weaker in targeting defects affecting the components themselves. In particular, only the Live attribute is in charge of verifying that each component works correctly, by generically checking that it is alive, i.e., that the component responds correctly to an electrical stimulus.

As a result, the effectiveness of a test method targeting power devices on a PCB is normally evaluated in a qualitative way, due to the lack of any well-established fault model.

The issue of evaluating the effectiveness of a test procedure for a power device has been faced in the past in the frame of the test of analog modules, for which different solutions have been proposed, such as the sensitivity approach or the Monte Carlo analysis.
The sensitivity approach [5] is useful for calculating a possible fault coverage and for assessing the diagnostic capabilities of a test. However, the sensitivity approach requires the manual identification of numerous mathematical relationships in the circuit. This approach is simply not feasible in circuits composed of numerous components.
Another possible technique is the Monte Carlo analysis [6]. This approach can be used to generate a large number of possible faults by varying the nominal parameters of the components. However, it requires at least one circuit simulation for each possible variation. Hence, the CPU time requirements of this method can quickly become unaffordable.
Different research teams have proposed some strategies for performing some sort of systematic and automatic analog fault simulation of a test procedure [2][8][9][10] considering a list of possible faults affecting analog components; however, these faults are manually identified. The faults are identified resorting to different strategies which are often specific for each different case study. Currently, identifying the list of the faults that must be considered during the fault simulation is an open problem. Other research teams have proposed some methodologies for generating the fault list. In [2], the authors propose a statistical approach to identify a significant subset of faults. In [11], the faults to be considered are identified by analyzing the behavioral description of the netlist provided in Verilog-AMS. However, the methodologies proposed in [2] and [11] are based on a high-level circuit abstraction or on a manual estimation of the occurrence probability of each fault.
Partly due to the pressure coming from functional safety standards, in the last years significant efforts have been performed to introduce effective and widely accepted fault models for analog components (see for example [7]). These efforts also led to the introduction of some new commercial tools (e.g., DefectSim by Mentor Graphics and TestMAX by Synopsys), and analog fault models are now starting to be systematically used. These tools support both parametric and catastrophic fault models [1][5]. A parametric fault is a variation of one parameter of the device characteristics out of its nominal range. On the other side, catastrophic faults correspond to either open-circuit defects in the electrical network, or short-circuit defects between two normally disconnected nodes of the network.

The aim of this paper is to extend the usage of the metrics introduced by the new analog fault simulation tools to power devices and to use them in the assessment of test procedures to check their correct behavior once they are mounted on a PCB. The basic idea is to rely on the equivalent electrical model which is often provided together with a power device in order to generate a list of possible faults, which can then be fault simulated in order to compute a metric (Fault Coverage, or FC) for each test solution. The possible fault list is generated systematically and automatically resorting to general rules independent of the specific device or system.

In particular, the contribution of this paper consists in:

- defining a possible method to systematically generate a list of catastrophic faults for a power device, starting from its equivalent electrical model; this list of faults can then be used to quantitatively evaluate (via fault simulation) the effectiveness of a test procedure for a given power device at the end of the PCB production or during the system operational life
- validating the proposed method on a realistic test case, showing the advantages and limitations of well-assessed test procedures (incoming inspection, in-circuit test and functional test). Moreover, our work shows that neither in-circuit test, nor functional test alone can fully test possible faults inside the considered power devices on a PCB, while a clever combination of them allows to significantly increase the number of detected faults.

The proposed method allows to compute a FC figure for a given test solution, and thus to compare its effectiveness, evaluating the real contribution of each test step to the final FC and possibly removing any ineffective or redundant test, or adding new test steps to detect any previously untested fault.

This paper extends the work in [12] and [13]. In [12] we proposed an approach aimed at evaluating the effectiveness of a test procedure for a stand-alone power device before its mounting on the PCB. In [13] we extended the approach proposed in [12] to PCBs. In this paper, the proposed approach is further generalized and evaluated on a real case study. In particular, we formalize here a method for systematically generating the list of faults to be considered when testing a power device, knowing its equivalent electrical model. The most widely adopted test solutions (i.e., incoming inspection, in-circuit and functional test) are then evaluated resorting to the considered metric and referring to a representative case study. Interestingly, some faults within power devices can hardly be detected, because they are tolerated by the system and do not produce visible effects. However, they may create unplanned stress conditions for the device itself which may limit its life and reliability.

The rest of the paper is organized as follows. Section II summarizes the main fault models used for analog and power electronics and describes the main strategies used for testing power devices on a PCB. Moreover, Section II shows the state of the art about the different fault simulation methodologies for analog circuits and components and about the fault list generation. The approach we propose to generate the list of faults to be considered and to evaluate a given test procedure is described in Section III. Section IV introduces a case study, while Section V describes the experimental results obtained on it. Finally, Section VI draws some conclusions.

II. BACKGROUND

This section first provides some information about the fault models used for analog electronics. Subsequently, the main solutions adopted in real practice to test power devices during and at the end of the production of PCBs are outlined.

A. ANALOG FAULT MODELS

In analog electronics, any signal can be seen as a variation over time of an electrical quantity. Therefore, by definition, all electrical quantities, such as voltages or currents, are continuous over time. With this behavior it is difficult to define a fault model, as it happens for digital electronics. The binary behavior of the digital circuits allows, for example, the

definition of a very practical fault model called stuck-at [1]. In the stuck-at fault model, a fault can be modelled assuming that the logic value of an input or an output of a gate is always fixed at the high logical value (stuck-at one) or at the low logical value (stuck-at zero). Moreover, in the analog circuit the electrical quantities depend on many external factors, including the temperature, the tolerance of the component, the ageing of the device and the presence of the electrical disturbances (electrical noise). Many of these parameters are random and some are due to phenomena which are external to the circuit itself. Some of these undesirable phenomena may have a negligible impact on the circuit if the same has been correctly designed and its components correctly sized. Therefore, it is difficult to define a practical fault model for analog and power circuits. Among the different possible fault models used for analog circuits, the most frequently used models are the catastrophic faults models and the parametric faults models [1][5], as suggested also by the emerging standard IEEE P2427 [2][14]. Catastrophic faults correspond to short or open circuits in the circuit electrical network. It is possible to consider a catastrophic fault as a large variation of a nominal parameter of the component. For example, considering a resistor, a catastrophic fault corresponds to turning it into a resistor of zero resistance (short circuit) or into a resistor of infinite resistance (open circuit).

A parametric fault is a variation of one of the nominal parameters of the component outside of its nominal range. Usually, all the possible parameters of an electronic component are associated with a validity range. For example, considering a resistor belonging to the E12 standard series, the resistance value has a nominal range of ±10%. For a resistor component, a parametric fault corresponds to varying the value of the resistance more than 10%. Since the faulty value assumed by the parameter may vary freely, in the case of parametric faults their number is infinite. An example of a single parametric fault analysis appears in [15], whose results can be used either to validate the design and its fault tolerance, or to support the Failure Mode and Effect Analysis (FMEA), as discussed in [16].

This paper focuses only on single permanent faults belonging to the category of catastrophic faults. As proposed in some new commercial analog fault simulation tools, such as DefectSim by Mentor Graphics and TestMAX by Synopsys, the focus is placed on catastrophic faults, only. Although parametric fault models are also used in some cases, their adoption hardly allows to compute a uniquely defined fault coverage metric, mainly because they are uncountable by definition.

Moreover, a single permanent fault [1] is considered at a time, as commonly done for digital circuits. In other words, only one single fault is considered to be possibly present in the circuit at a time. As discussed in [1], a single permanent fault at a time is preferred rather than a combination of different faults simultaneously, mainly to simplify the reliability analysis, unless the specific scenario (e.g., in terms of adopted technology and/or environment) mandates differently.

Recently, different methods are been proposed to estimate the effectiveness of an analog test procedure [8][9][10][17][18]. All the proposed methodologies need first to identify a limited number of interesting faults to be used during the fault simulation. The test procedure quality is evaluated considering the number of faults it detects. A possible approach for generating the fault list is proposed in [17]: the authors define the concept of severity of a fault and the fault list is composed of the faults with the highest severity. These faults are identified by simulating a number of high-level defects. Then, the effectiveness (i.e., the achieved FC) of three different functional tests is assessed considering the fault list identified. In [18], the fault list is generated by Simple Random Sampling (SRS). In [8], the fault list is chosen considering the experience of the system designer. In particular, 34 catastrophic faults on the last analog stage of a serial transmitter are considered. Subsequently, the FC of two self-tests periodically performed on the serial interface is evaluated. In [9] and in [10], the fault list is generated considering the designer's experience, too; in both papers, the FCs of some functional tests are assessed and compared. The fault list generation methodologies proposed in [8][9][10][17][18] may require a considerable effort and experience to identify the faults. Moreover, they cannot be easily generalized to different case studies.

Recently, different research teams have faced the issue of how to cleverly select a representative subset of parametric faults [19][20][21]. In this paper we focus on catastrophic faults, only.

In recent years numerous works also proposed methodologies to perform fault simulation of analog circuits. For example, in [22] an analog fault simulator based on the one-step Newton-Raphson iteration is proposed. An algorithm for determining the effects of faults in analog circuits based on neural networks is proposed in [23]. The approach proposed in [23] is useful for analyzing the electrical circuit behavior even in the multiple faults scenario. In [24], a further alternative based on genetic algorithms is proposed. The proposed approach focuses on catastrophic faults, only; in particular, the method generates the failure dictionary used in the simulation-before-test (SBT) approaches to perform analog circuit diagnostic [25][26]. Finally, a methodology for accelerating analog fault simulation is proposed in [27], based on partitioning the Circuit Under Test into numerous independent sub-circuits. Faults are simulated in the sub-circuits and the effects propagated in the connected sub-circuits.

B. THE TEST METHODS

The aim of this sub-section is to provide the reader with an overview of the main strategies used for testing devices immediately before or after they are mounted on a PCB, with emphasis on the test of power devices: the incoming inspection, in-circuit and functional test are considered [28][29]. These different tests are normally combined during the test of a given PCB, aiming at covering the highest percentage of possible defects with minimum cost. Each of the three different test strategies considered is performed by applying some specific voltage or current to the circuit under test. In the rest of the paper, we will use the term "stimulus" referring to an electrical test signal applied to the circuit under test inputs.

1) INCOMING INSPECTION TEST

The incoming inspection test is performed by the company producing the PCB on the single devices before they are assembled on it. This step can be avoided if the PCB company has enough confidence and trusts in the quality of the devices. The incoming inspection test of each device can be performed having full controllability and observability on each input/output signal of the device. According to [28], about 75% of the faults occur during the assembly of the PCBs, and

about 20% is associated with devices malfunctions before their assembly. Finally, 5% of the faults are associated with a production defect of the PCB (bare board defects). Then, the electronic devices may suffer some damages during the assembly, due for example to mechanical movements or to the welding process of the device. In other cases, components can be assembled with a different orientation from the correct one or a different device is welded. For this reason, it is not enough to perform an incoming inspection test on the devices before their assembly.

2) IN-CIRCUIT TEST

This test is performed during or at the end of the PCB manufacturing [28][29][30]. The in-circuit test is used first of all for testing the correct assembly of the components on the PCB. A test machine, called Automatic Test Equipment (ATE), is able to contact the pins of one or more components on the PCB and to perform a test. The electrical contact operation is performed with high mechanical precision by means of electric probes called *needles*. Depending on whether needles are statically or dynamically managed (and on their number), in-circuit test is implemented resorting to a *bed of nails* or a *flying probes* approach. In any case, the electrical probes are used to apply the stimuli and to measure the response of the components. In these tests, there is the problem of electrical interference between the components on the PCB. The voltages or currents applied to the device under test can propagate to other components. This propagation may not allow the complete test of the component, or can damage other devices in the PCB. Some *guard* probes can be used to prevent the propagation of the applied voltages and currents. In general, the guard probes allow to place some points at the same electric voltage to avoid the propagation of the currents, or some points of the circuit are connected to the ground. During the in-circuit test the board is normally not powered and no other electrical stimuli are applied to the board in addition to the stimuli imposed by the ATE. The in-circuit test also allows to check the electrical connections between the components. A limitation of the in-circuit test is related to the impossibility of contacting all the pins of the components on the board, for example, because the component is covered by heat sinks or because they are physically inaccessible.

3) FUNCTIONAL TEST

The functional test verifies the circuit with respect to its design specifications. A board is considered as a black box and it is possible to interact with it only through its functional interfaces, i.e., through the input and output ports of the PCB. Some electrical functional stimuli are applied to the input ports and the behavior of the PCB is verified by observing the responses on its output ports. The applied input stimuli are compliant with the technical specifications of the board. The functional response obtained from the output circuit ports must comply with its technical specifications. In other words, the functional test verifies that the circuit works respect the circuit design specifications. For example, a possible functional test for an audio amplifier verifies that the band gain respects the desired gain value. An electrical stimulus is applied at the input to the PCB, the response provided by the PCB must comply with the expected one; i.e., the amplifier output signal must be amplified of a known expected gain.

III. PROPOSED APPROACH

In this section we describe the method (summarized in Figure 1) we propose to deterministically and automatically generate the list of faults for a given power device (corresponding to the Device Under Test, or DUT), and then the method (based on simulation) to determine their effects when the PCB the device is mounted on is subject to a given test procedure. The whole approach allows to identify those faults out of the considered ones, which produce some visible effect, and thus can be marked as *detected*. The fault simulation is performed on the Circuit Under Test (CUT); the CUT can be the whole PCB or a portion of it. The percentage of the detected faults out of the total number of considered faults is the Fault Coverage, which measures the quality of the test procedure.

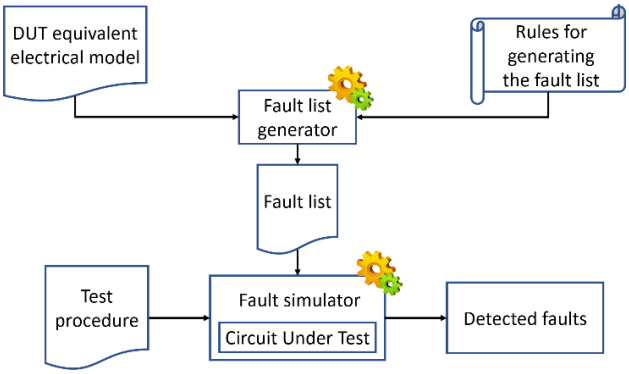

Figure 1: Overall proposed flow

The first sub-section describes the proposed fault list generation algorithm, while the second sub-section reports an example showing its application to a sample device. Finally, the last sub-section outlines the procedure for Fault Coverage computation.

A. FAULT LIST GENERATION

In this sub-section, the algorithm used to generate the list of faults in the equivalent electrical circuit for a power device is discussed. The proposed approach uses the equivalent electrical model of the Device Under Test (DUT). Typically, the equivalent electrical model is provided by the manufacturer of the device. In other cases, the model can be built by the user knowing the characteristics of the device. In general, the parameters of the equivalent electrical model of the DUT are provided by the device manufacturer together with its electrical model; in some case, the model parameters are reported in the technical manual of the DUT.

The proposed algorithm aims at systematically generating a fault list composed of a finite and numbered list of possible catastrophic faults for the device. This list can be automatically generated using some well defined rules. The rules proposed are independent of the implementation details of the DUT and of the physical meaning of the possible defects that may affect the DUT, as discussed in [1].

The idea is to add some switches in the equivalent electrical model of the DUT and use them to model possible faults. Three different types of switches can be inserted:

- switches to be introduced in series to the model components
- those to be introduced in parallel to the model components
- "topological" switches, which model possible shorts between the model lines.

Each switch corresponds to a catastrophic fault in the equivalent electrical model. The serial switches are added in series to each component present in the equivalent electric model, while the parallel switches are placed in parallel with each component of the equivalent electrical model. Finally, the "topological" switches introduce some short circuits between nodes of the model that are normally not connected.
The algorithm consists of the following steps (from A to D):

- **Step A** In the equivalent electrical model, the ideal and parasitic components must first be identified.
- **Step B** The serial electrical switches are inserted in series to each component of the circuit. However, two switches placed in series in the same electrical branch can be replaced by a single equivalent switch. Furthermore, the switches that disconnect only the parasitic components are not considered (by removing a parasitic component the characteristics of the device under test are improved). Opening the switch means activating the fault.
- **Step C** The parallel electrical switches are inserted in parallel to each component of the circuit. However, two switches placed in parallel to the same component are replaced by a single equivalent switch. Furthermore, the switches that short-circuit only the parasitic components are not considered, in order not to improve the features of the device. Closing the switch means activating the fault.
- **Step D** In order to model the topological faults, a graph representing the circuit connections is considered. In the graph, the vertices are the nodes of the electrical network, while the components are the edges. The graph is obtained by collapsing the adjacent electrical nodes and by collapsing the edges that connect the same nodes; this graph is called the *incidence graph*. A "topological" fault is considered (corresponding to a switch) for each missing edge in the graph. Furthermore, as for the parallel switches, the switches that short-circuit only the parasitic components are not considered. Closing the switch means activating the fault.

B. EXAMPLE OF FAULT LIST GENERATION

To better explain the proposed algorithm, in this sub-section we generate the list of catastrophic faults for a simple capacitor. The equivalent electrical model of the capacitor [31] is shown in Figure 2, where some parasitic components are added to the equivalent electrical model.

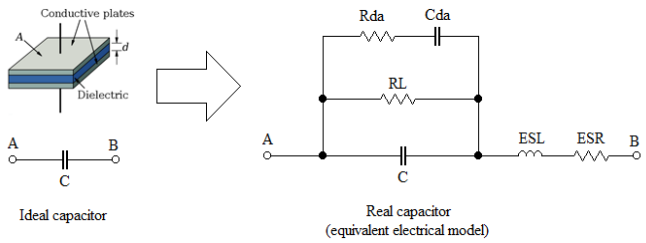

Figure 2: Equivalent electrical model of the capacitor

In the equivalent electrical model of the capacitor, the C component identifies the nominal capacity of the ideal component. The resistor RL models the electrical permeability of the dielectric present in the capacitor. The non-ideal dielectric causes a small migration of electric charges between the two capacitor plates. The ESL equivalent series inductance represents the distributed inductances present in a real capacitor. The ESR equivalent series resistance is due to the resistance of access to the capacitor plates. Finally, the Rda and Cda components are related to the absorption of the dielectric, i.e., the ability of a dielectric to retain some electrical charges inside it. To summarize, the C component is ideal, while the components Rda, Cda, RL, ESL and ESR correspond to the parasitic components.
The serial switches are added as shown in Figure 3 (a). Considering the *serial equivalence*, the switches placed in series to the ESL and ESR components are replaced with a single switch. Furthermore, the switches that disconnect only the parasitic components are not considered; this is the case of the switches placed in series to the Rda, Cda and RL parasitic components. The switches considered are shown in green, those excluded in red and the equivalent switches in blue. Figure 3 (b) shows the parallel equivalent switches and the excluded switches.
Figure 4 (a) shows the collapsed electrical nodes (A and N1) and the collapsed parallel components (RL and C) in the equivalent electrical model of the capacitor; furthermore, Figure 4 (b) shows the obtained *incidence graph*.
Finally, Figure 5 shows all the switches considered for the capacitor (Fp stands for parallel faults, Fs for serial faults and Ft for topological faults). Overall, five faults are considered for the capacitor, each corresponding to a switch in the equivalent electrical model.

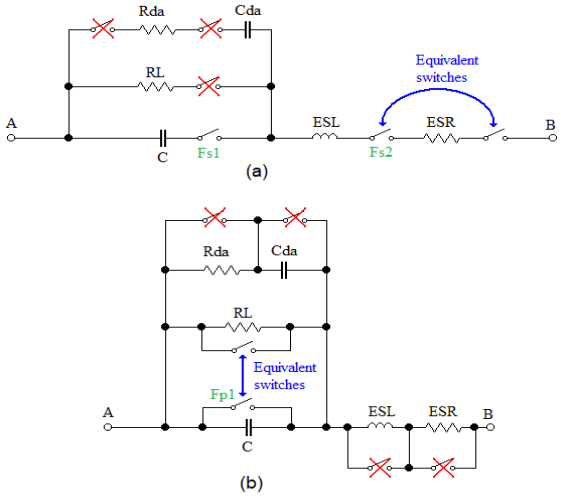

Figure 3: The serial switches (a) and the parallel switches (b) in the equivalent electrical model of the capacitor

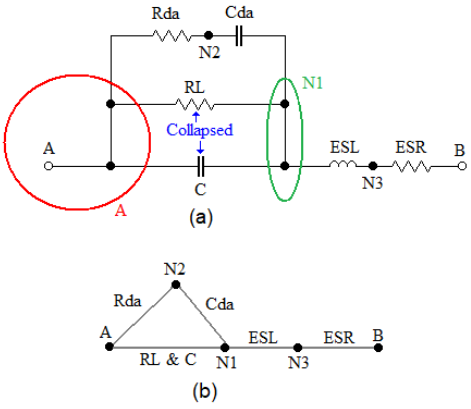

Figure 4: (a) The nodes and the components collapsed in the capacitor's equivalent electrical model. (b) The incidence graph of the capacitor's equivalent electrical model

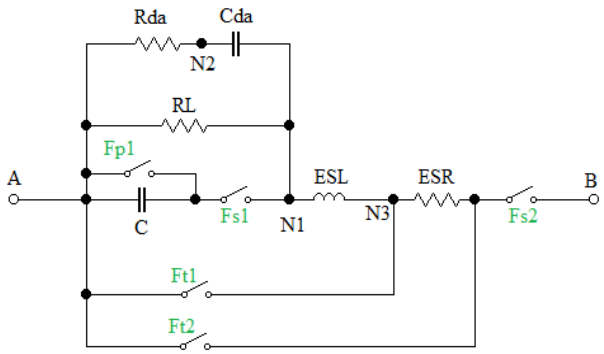

Figure 5: The equivalent electrical model of the capacitor with the switches modelling possible faults

C. FAULT COVERAGE COMPUTATION

Once the list of faults to be considered for a given power device has been generated, and a given test procedure is available, we can identify those faults in the list which produce some visible differences in the system behavior, i.e., are detected by a given test procedure (thus computing a Fault Coverage (FC) figure) resorting to circuit simulation. Figure 6 shows the fault simulation flow considered [9]. The fault simulation process depends on the tester constraints, i.e., on the point of application of the stimuli and on the point where we observe the effects of the stimulus. In some case, the stimuli are applied and observed directly on the test points connected to the DUT pins. Instead, the stimuli are applied to the input port of the circuit. For the purpose of the simulation of each fault, the circuit is replicated in two different circuits; the first one is used as reference, while the second one, called Circuit Under Test (CUT), is the one where the fault is injected. The same electrical stimuli are applied to both circuits and the circuit output signals are compared. The output of the reference circuit is called *golden behaviour*, while the CUT *behaviour* is the output produced by the CUT. A comparator module generates an *error signal* [10] according to equation (1). The *error signal* is used to evaluate the Fault Coverage. The *error signal* is evaluated continuously at each time instant, thus obtaining a continuous curve over time. If at any time the error curve exceeds a limit threshold the fault is labelled as *detected*. The final FC is calculated as the number of faults labelled as detected divided by the total number of faults generated out of the equivalent electrical model of the DUT.

$$\text{error\%}(t) = \frac{|\ \text{golden behaviour}(t) - \text{CUT behaviour}(t)\ |}{\text{reference output}(t)} \qquad (1)$$

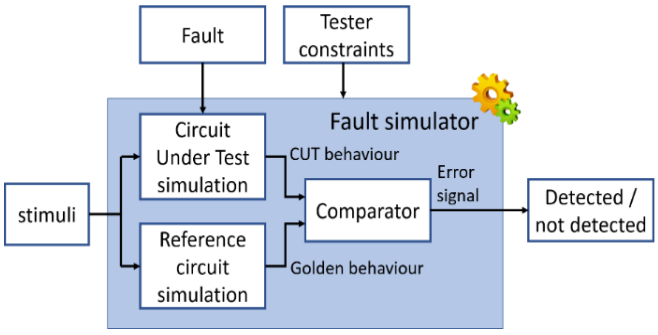

Figure 6: Analog fault simulation flow

IV. CASE STUDY

This section describes the case study we considered, corresponding to a Power Supply Unit (PSU) including some power diodes and IGBTs. For each of them, we generated the list of catastrophic faults to be considered and performed the simulations required to compute the Fault Coverage achieved by the different test procedures, following the method described in the previous Section.

A. POWER SUPPLY UNIT

The considered case study corresponds to an industrial Power Supply Unit (PSU). A PSU is often used to power the electrical motors in many applications, such as in industrial compressors or in many appliances. The board considered was designed and produced by the Power Electronics Innovation Center (PEIC) of the Politecnico di Torino; the board was developed in an industrial collaboration aimed at improving the energy efficiency of electrical converters in power applications. Similar PSUs can be used in safety-critical applications, such as on board chargers for electric and hybrid vehicles. The different stages of the PSU are shown in Figure 7.

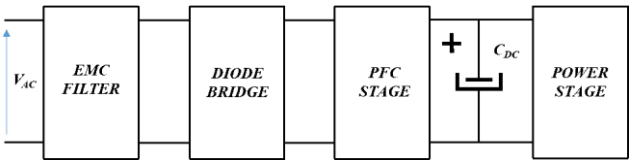

Figure 7: PSU stages

The PSU we considered is able to supply an output voltage of 400 V in continuous with a maximum ripple of ±7 V, and a maximum current of 12 A. The boost converter works with an input voltage between 110 V and 250 V, with a frequency of 50 Hz or 60 Hz. The Electro Magnetic Compatibility (EMC) Filter consists of a common mode choke and film capacitor used to reduce the conduction electromagnetic emission caused by the Power Factor Correction (PFC) switching. In the PFC stage there are three legs of the interleaved PFC structure, as reported in Figure 7. Each leg is a simple boost cell composed of an inductor, a diode, and an IGBT. During the design of the PSU, the STTH12S06 and STGF19NC60 devices were chosen respectively for the diode and IGBT. The output capacitor is in common with the DC-Link. The measures are performed with the 4-points shunt resistors placed in series to the IGBT (Rs1, Rs2, Rs3). The FAN9673 controller measures the current on the IGBT in differential mode through the shunt resistance. Moreover, it measures the input voltage on the CIN capacitor and in feedback the output voltage with the RF1 and RF2 voltage divider. The FAN9673 produces an output three signals (DRIVE1, DRIVE2, DRIVE3) that are applied to the IGBTs (T1, T2, T3). The aim of the control system is to obtain a sinusoidal shape of the current absorbed from the grid and with a power factor almost unitary. The output of the PFC is then connected to a classic three-phase inverter for the motor control. The FAN9673 analog controller [32] produced by ON Semiconductor® is a three-leg PFC controller. The controller drives the boost inverters of each PFC leg independently with its own IGBT control signal. Each boost converter operates in Continuous Conduction Mode (CCM); the control signal is a square wave with a frequency between 55 and 75 kHz. Considering the

PSU in steady-state and with a rectified sinusoidal signal at 50 Hz 230 V in its input, the command signal produced by the controller to the IGBT is about 60 kHz. The FAN9673 controller is compatible with the IEC1000−3−2 standard related to electromagnetic compatibility; moreover, it incorporates the TriFault Detect system [32] in compliance with the UL 1950 safety standard. The TriFault Detect system implements many protection systems, including the peak current limitation, input voltage brownout protection, the output short-circuit and the over-voltage protection. However, the protections implemented by the FAN9673 device are intended for protecting the PFC components, such as IGBTs and diodes, from faults external to the PFC stage [32]. For example, the protections are useful for saving the PFC circuit from a short circuit at the outputs of the PFC; other protections are useful in presence of a significant inductor current increase due to a grid voltage increase. Finally, a protection system is implemented to save the PFC from meaningful variations of the grid voltage at the PFC input. However, possible faults affecting the PFC power devices cannot trigger in any way these protection mechanisms. The analyzed circuit shown in Figure 8 is realized on a PCB together with the whole system, as shown in Figure 9. Overall, in addition to the analyzed PSU the system also includes a power stage and a three-phase electrical motor control system. The portion of the circuit analyzed in this paper is well defined already from the first phase of the system's design. Figure 9 shows the portion of the board occupied by the PSU; the power connector (AC input) and the output connector (Vout) are also shown. Furthermore, the main components of the system are indicated, such as the diode bridge, the EMC filter, the PSU controller (FAN9673), the tree-phase inverter for the electrical motor. The IGBTs and diodes of the PFC are assembled on the other side of the board, as shown in Figure 9. The PSU circuit can be isolated from the rest of the system. For the purpose of this work, we only considered the PFC circuit shown in Figure 8. In blue we highlighted the connector including the input/output signals used by the functional stimuli.

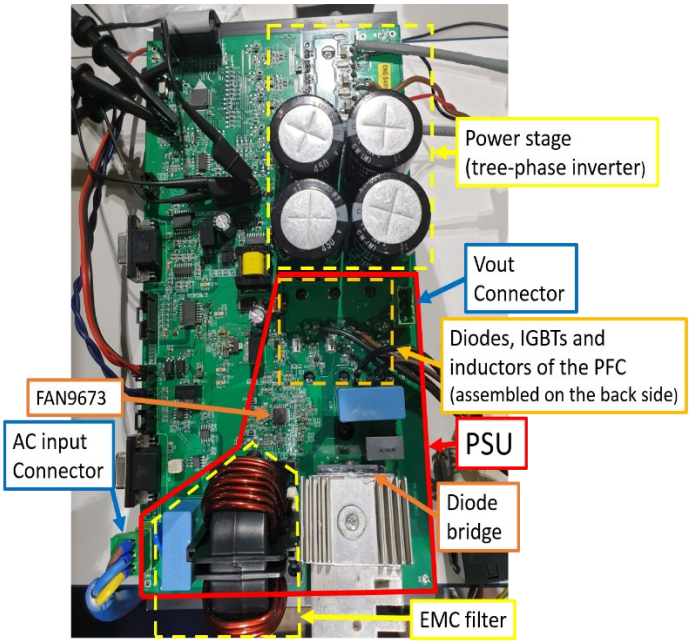

Figure 9: The PCB of the whole system

B. THE STTH12S06 POWER DIODE

The STTH12S06 [33] power diode produced by STMicroelectronics is a diode belonging to the *ultrafast high voltage Turbo 2* diode family. It has a forward voltage (Vf) of 1.5V and it supports a maximum current of 12A and a maximum inverse voltage of 600V. Its fast switch time, around 14ns, makes it suitable for power switching applications. The power diode device is assembled in the TO-220FPAC package to allow the assembly of an additional heatsink. A possible equivalent electrical model of a diode is discussed in [34][35][36]. In [36] the model is based on an ideal diode that includes some parasitic components. Figure 10 shows the equivalent electrical model of the diode used in this paper. The parasitic components describe the presence of unwanted electrical phenomena.

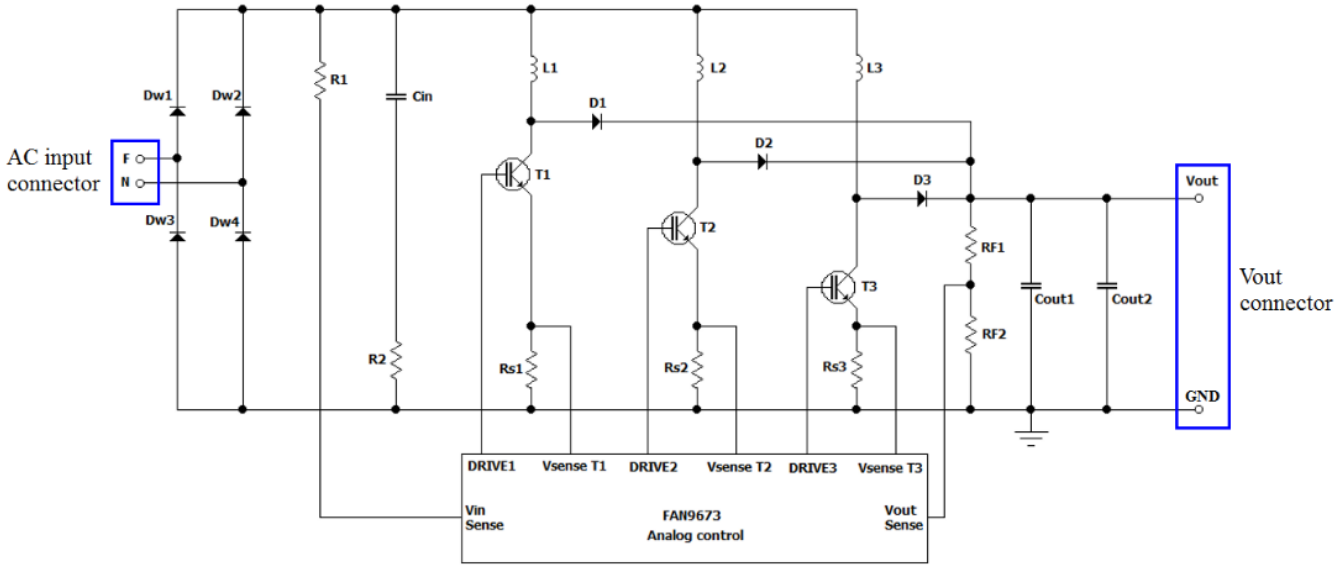

Figure 8: The PFC structure

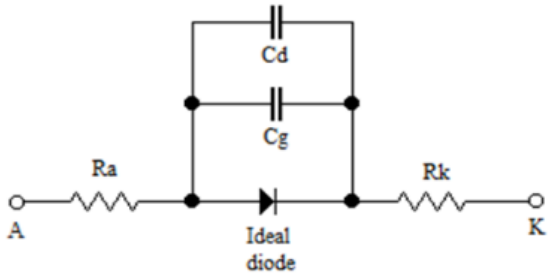

Figure 10: The adopted diode equivalent electrical model

The unwanted electrical phenomena are physically present in the component and influence its behavior. The parasitic components influence the diode in terms of performance or efficiency of the device. The parasitic components considered in the diode are the access resistances to the PN junction (Ra and Rk) and the junction and diffusion capacities (Cg and Cd). The values of the parameters of the equivalent electrical model are shown in Table 1.

Equivalent electrical model parameters	Value
Ra	7.21 mΩ
Rk	7.21 mΩ
Cg	0.13 pF
Cd	95 pF
Vf	1.5 V

Table 1: Parameter values of the equivalent electrical model of the diode

C. THE STGF19NC60 POWER IGBT

The Insulated Gate Bipolar Transistor (IGBT) combines the input characteristics of the Metal-Oxide-Semiconductor Field Effect Transistor (MOSFET) with the output characteristics of the Bipolar Junction Transistors (BJT) in a new monolithic integrated device. The DUT considered is the IGBT STGF19NC60 [37] produced by STMicroelectronics; it belongs to the Power MESH family [38], including power devices specifically designed for electric motors application. In particular, this IGBT is a very fast device, with a switching time of 200ns, and an ultrafast anti-parallel diode. The chosen IGBT is assembled in the TO-220FP package, and it is able to handle a maximum voltage of 600V and a maximum current of 19A.

An equivalent electrical model is shown in Figure 11. The model is built using the basic model proposed in [39] with the parasitic components proposed in the model suggested in [40]. The equivalent electrical model shown in Figure 11 considers the parasitic access resistances to the collector (Rc) and to the emitter (Re). The parasitic resistance of the body (R_body) of the device is also considered; ideally the body resistance assumes a null value. Moreover, the parasitic capacitances related to the oxide layer on the gate (Cgd, Cge, Cgc) are considered. The Cgc and Cce parasitic capacities related to the IGBT parasitic input and output capacities are also considered; the Cds capacitance is present in the vertical PN junction, as discussed in [41]. The drift parasitic resistance (R_drift) [42] is also considered. The drift resistance is associated with the injection of holes in the IGBT drift region.

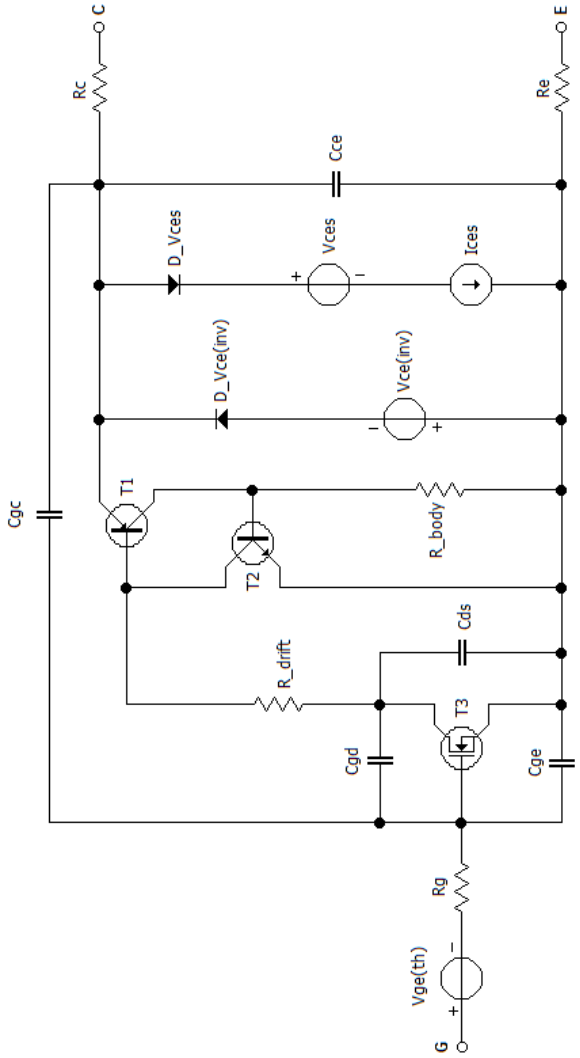

Figure 11: The adopted IGBT equivalent electrical model

These holes reduce the mobility of the carrier, with the effect of increasing the resistance of the drift region. Finally, the parasitic NPN transistor (T2) is considered [40]. The transistor T2 can block the IGBT device if the voltage drop on the R_body is sufficient to trigger the T2 transistor in saturation. The equivalent electrical model used is widely discussed in [12]. The values of the parameters of the equivalent electrical model are shown in Table 2.

Equivalent electrical model parameters	Value
Vge(th)	4 V
Rg	10 MΩ
Cgd	5 pF
Cge	1.15 nF
Cds	20 pF
R_drift	1.3 Ω
Cgc	36 pF
R_body	9 Ω
Vce(inv)	2.5 V
Vces	600 V
Ices	15 A
Cce	94 pF
Rc	5.6 mΩ
Re	5.4 mΩ

Table 2: Parameter values of the equivalent electrical model of the IGBT

D. INCOMING INSPECTION TEST PROCEDURES

This sub-section describes the incoming inspection test procedures for the two power devices considered. The two test procedures consist of some sub-tests we called *test steps*. Each test step is able to check a DUT feature. The purpose of the incoming inspection test, as discussed in section II.B, is to verify the correct operation of the device before it is assembled on the board. In both cases, we selected test procedures which can be considered as state-of-the-art solutions in current practice.

1) INCOMING INSPECTION TEST PROCEDURE FOR THE DIODE

The incoming inspection test procedure proposed in [43] is able to test a power diode device. The test procedure is performed in two steps, shown in Table 3. The first one tests the PN junction polarized directly, while the second step tests the PN diode junction polarized inversely.

Test steps	Diode Test description
A	PN junction test polarized directly
B	PN junction test polarized inversely

Table 3: Diode test procedure

2) INCOMING INSPECTION TEST PROCEDURE FOR THE IGBT

A possible incoming inspection test procedure for an IGBT device is proposed in [44]. This test is composed of 8 steps (from A to H). The aim of each test step is reported in Table 4. Each test step is discussed in detail in [12].

Test step	Test step description
A	PN junction test polarized inversely
B	PN junction test polarized directly
C	Gate-emitter impedance test
D	Gate-collector impedance test
E	Vce(sat) test
F	Vf test on free wheel diode
G	Ices test (blocking devices)
H	Vge(th) test

Table 4: IGBT test procedure

E. IN-CIRCUIT TEST PROCEDURE

The in-circuit test is performed by replicating as much as possible the incoming inspection test procedure on the assembled PCB. An ATE is used to perform the test. Some test steps cannot be performed due to the limited number of probes available in the ATE or due to the specific characteristics of the circuit. Moreover, some test steps are not effective due to the circuit itself, e.g., because the three legs of the PSU placed in parallel mask the effects of numerous faults. Therefore, some untestable faults may exist with the in-circuit approach.
The in-circuit test procedures implementations for the D1 diode and the T1 IGBT are now discussed. For the D1 diode, the 2 test steps can be implemented by an ATE using 7 distinct contacts on the PCB. Instead, the steps C and D of the IGBT test procedure are not feasible, because they require to modify the PSU circuit by disconnecting the IGBT terminals. Hence, these two test steps are not considered in the in-circuit test.

F. FUNCTIONAL TEST PROCEDURE

The functional test is performed by applying some functional stimuli to the circuit inputs and observing the circuit outputs.
In particular, the functional stimuli are applied to the input connector of the PFC, as shown in Figure 8. The functional stimuli are chosen according to the circuit design features. For the case study, 4 stimuli (S1, S2, S3, S4) were used considering the power supply voltages and frequencies accepted by the PSU under test. The 4 stimuli used are AC sinusoidal components with amplitude of 230V or 100V RMS and with frequency of 50Hz or 60Hz, as shown in Table 5. Other stimuli which do not comply with the PFC technical specifications would be harmful to the devices assembled on the PCB.

Stimuli	AC sinusoidal stimuli	
	Amplitude	Frequency
S1	230 V RMS	50 Hz
S2	110 V RMS	50 Hz
S3	230 V RMS	60 Hz
S4	110 V RMS	60 Hz

Table 5: Functional stimuli

The functional test is performed in three different modes: 1) comparing the output of the circuit in steady state in accord to the definition of the functional test approach described in Section II.B. This mode is called *base functional*. 2) considering also the initial transient of the circuit during the test. This mode, called *timely enhanced functional*, is possible only if the test equipment used to perform the test supports it. 3) by performing further measurements in some points of the circuit during the test. This last mode, called *observability enhanced functional*, can be performed when the test equipment can probe some internal points of the PCB during the execution of the functional test.

V. EXPERIMENTAL RESULTS

We applied the approach proposed in section III to evaluate the effectiveness of the different test approaches on the selected case study described in Section IV and analyzed the results. With reference to the PFC inverter of Figure 8, the power diodes D1, D2 and D3 and the IGBTs T1, T2 and T3 are considered.
This section is organized in different sub-sections. Initially, the simulation environment is discussed in the first sub-section. Afterwards, the list of catastrophic faults is generated with the approach proposed in Section III.A and results are presented in the second sub-section. The incoming inspection test procedure for the diode devices proposed by the Fluke company [43] and the test procedure for the power IGBT devices proposed by the Galco company [44] (see sub-section IV.D) are simulated and results reported in the sub-section V.C. Furthermore, in the sub-sections V.D and V.E the results of the simulation of the in-circuit test described in sub-section IV.E and the functional test described in sub-section IV.F are reported for the diode and the IGBT devices. Finally, the last sub-section compares the different simulation results.

A. SIMULATION ENVIRONMENT

The Matlab-Simulink software environment was used to perform all the simulations. In particular, the PLECS [45] tool by Plexim was used. PLECS is a circuit simulation tool integrated in the Simulink environment. It is specifically designed to simulate the electrical and electronic power systems. The numerical solver used in Simulink is the ODE45 [46]. Which is able to operate using an adaptive variable integration step during the simulation. Each simulation of the whole system (fault-free or faulty) required about 4 hours of CPU time. The system is simulated for a period of 0.5 seconds.

This time is sufficient for completing the initial transient and to observe a sufficient number of cycles in the steady state. The experiments were performed on a PC equipped with an 8 cores AMD FX-8370 processor operating at 4GHz and 32 GB of RAM memory.

B. FAULT LIST

This sub-section reports the catastrophic faults considered for the diode and the IGBT.

1) DIODE FAULTS

Figure 12 shows the equivalent electrical model of the diode with the 4 catastrophic faults identified using the method described previously.

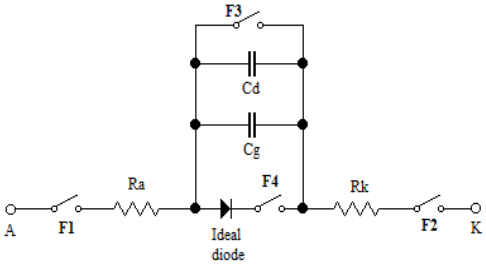

Figure 12: Equivalent electrical model of the diode with the considered faults

2) IGBT FAULTS

In the equivalent electrical model of the IGBT device, 31 catastrophic faults are identified using the proposed approach (Figure 13).

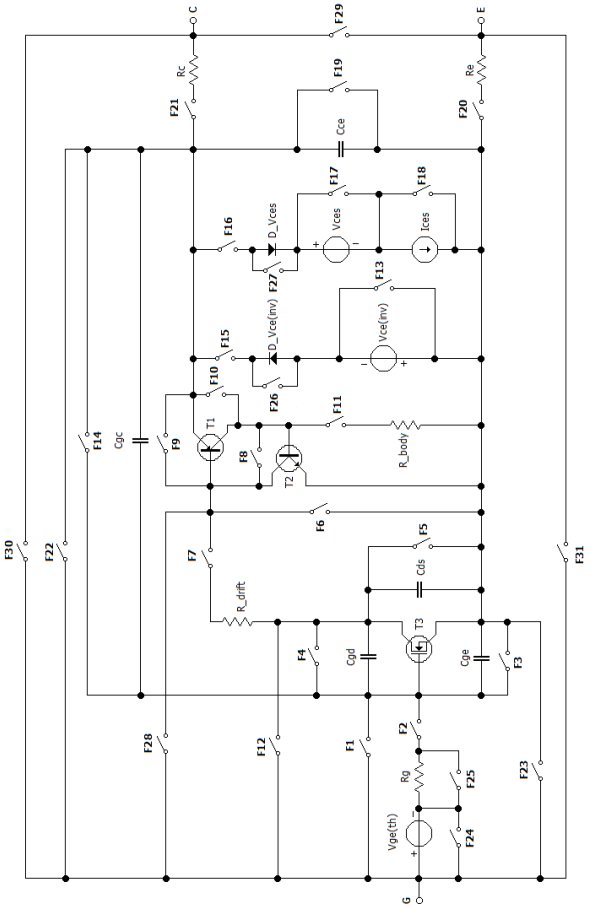

Figure 13: Equivalent electrical model of the IGBT with the switches corresponding to the catastrophic faults

C. INCOMING INSPECTION TEST EFFECTIVENESS ASSESSMENT

Table 6 and Table 7 show the number of catastrophic faults detected by the incoming inspection test procedures for the diode and in the IGBT devices for each test step. A threshold value of ±50% is chosen around the fault-free value: if a larger discrepancy is detected, the fault is considered as detected. In general, the value of this threshold must be carefully chosen and depends on the specific case. The last column (TOT) shows the number of faults detected by the test procedure. For both DUTs, all the possible catastrophic faults are detected with the incoming inspection test. The incoming test results should be considered as a reference test procedure, only, because the incoming test is performed in an ideal test condition, where the DUT is isolated from the other devices, its input and output signals are fully accessible, and the test is not affected by other devices present in the rest of the circuit. Finally, from Tables 6 and 7 it is possible to see the contribution given by each test step on the total number of faults detected. In the IGBT case, some faults are detected different times by different test steps. However, there are some faults that have only been detected by a single test step. Therefore, removing any test step leads to a reduction of the test completeness. This observation not only confirms the effectiveness of the considered incoming inspection procedure, but also shows the effectiveness of our approach.

	Test Step		TOT
	A	B	
Incoming inspection*	3	1	4

*Table 6: Incoming inspection test results for the diode (*used as reference results)*

	Test Step								TOT
	A	B	C	D	E	F	G	H	
Incoming inspection*	15	9	9	10	6	11	14	7	31

*Table 7: Incoming inspection test results for the IGBT (*used as reference results)*

D. IN-CIRCUIT TEST EFFECTIVENESS ASSESSMENT

Table 8 shows the number of faults detected by each step of the in-circuit test procedure for the diode. The step A does not cover any fault due to the presence of the PFC circuit: during the in-circuit test, the ATE forces a constant current in the diode to perform the test. As it can be seen from the electrical circuit of the PFC, the diodes D1, D2 and D3 are connected in parallel during the in-circuit test, and this greatly limits the effectiveness of in-circuit test. Overall, only one fault is detected with the in-circuit test.

Table 9 shows the number of faults detected by each test step for the IGBT device. Overall, the FC obtained with the in-circuit test is 80.64%, with 25 faults detected out of 31. The steps B and F of the test procedure are not effective due to the diodes DW1, DW2, DW3 and DW4 of the rectifier bridge. The current injected by the ATE flows to ground through these diodes. Moreover, the test steps C and D cannot be performed on the considered PCB, because they would require to modify the circuit by disconnecting an IGBT terminal. The test steps that do not introduce a contribution in the number of detected faults may clearly be skipped, such as step A for the diode and steps B and F for the IGBT.

	Test Step		TOT
	A	B	
In-circuit test	0	1	1

Table 8: In-circuit test results for the diode

	Test Step								TOT
	A	B	C	D	E	F	G	H	
In-circuit test	11	0	-	-	8	0	5	8	25

Table 9: In-circuit test results for the IGBT

E. FUNCTIONAL TEST EFFECTIVENESS ASSESSMENT

This section shows the simulation results for the diode and the IGBT considering the functional test methodology

1) FUNCTIONAL TEST RESULTS FOR THE DIODE

Table 10 shows the number of faults in the diode detected by each different stimulus applied to the PSU and each different test approach.

With the *base functional* approach, the S2 and S4 stimuli are able to detect all faults, while S1 and S3 are less effective. This is due to the PSU architecture. The PSU is composed of three parallel boost cells, and a fault in a cell may inhibit its operation. The boost cell with a non-functioning diode can be partially or totally inhibited. The PSU control system compensates the effect of a fault using the other two boost cells and increasing the frequency of the command signal that drives the boost cells. However, the control system cannot compensate the effect of a fault in presence of the S2 or S4 stimuli. In this case the output voltage produced by the PSU is lower than the expected one, and the fault can be detected. Based on these observations, we could state that in some operating conditions some faults can be tolerated by the system, which continues to provide the expected functionality despite their presence. Clearly, the effects of these faults on the duration and reliability of the system should also be considered. This phenomenon does not occur with the S1 and S3 stimuli which use a higher input voltage.

The *timely enhanced functional* approach is able to detect the faults by observing the duration of the initial transient. In the faulty case, the duration of the initial transient may be greater than expected, so faults can be detected with any stimulus.

In the *observability enhanced functional* approach, the voltage drop of the diode is measured during the test. For this purpose we assume that the diode pins are physically accessible by the tester probes (in some cases, this may not be true due to the heatsink). This last approach makes it possible to increase the observability in the steady state, thus detecting a larger number of faults. Table 10 shows that for the diode device in the considered case study only by complementing the basic functional test strategy with additional capabilities we can detect all possible faults and all possible stimuli.

	Stimuli				TOT
	S1	S2	S3	S4	
Base functional	1	4	2	4	4
Timely enhanced functional	4	4	4	4	4
Observability enhanced functional	4	4	4	4	4

Table 10: Functional test results for the diode

2) FUNCTIONAL TEST RESULTS FOR THE IGBT

Table 11 shows, for the three functional approaches, the number of faults in the IGBT detected by each different stimuli applied to the PSU. As for the diode, the S1 and S3 stimuli do not allow to detect all the catastrophic faults in the IGBTs. Comparing the three different approaches, the *base functional* approach reaches a FC of 48% (15 out of 31 faults are detected), while the FC with the *timely enhanced functional* approach is 64% (20 out of 31 faults). The *observability enhanced functional* approach achieves a 77% FC (24 out of 31 faults). In the last approach the frequency and the duty cycle of the IGBT gate command signal are also observed. The command signal is a good discriminant to possibly detect a fault. In the cases where the IGBT is unable to switch to the ON state, the controller always keeps high the command signal value on the gate terminal of the IGBT. Normally, a square wave of about 60 kHz is present on the IGBT gate terminal. In the presence of a fault that does not switch the transistor to the ON state, a fixed constant voltage is present on the gate terminal. Therefore, an error of 100% is found if the frequency of the square wave of the command signal is considered. Table 11 shows that, for the IGBT device in the case study considered, the Observability enhanced functional strategy is the most effective. However, different numbers of faults are detected when considering different stimuli . As we already observed for the diodes, also for IGBTs we can state that

- some faults only change the system output with some specific stimuli, while in some cases some faults are compensated by the system features
- some faults are always compensated by the system, thus becoming untestable. Since these faults may induce additional stress, their effects on the long-term reliability of the system should be investigated if the system is used in a safety-critical application.

	Stimuli				TOT
	S1	S2	S3	S4	
Base functional	0	11	0	12	15
Timely enhanced functional	15	12	13	13	20
Observability enhanced functional	19	19	15	19	24

Table 11: Functional test results for the IGBT

Finally, for sake of completeness, the simulation results obtained in presence of a sample fault are reported. In particular, the fault F21 of the IGBT device is considered. The stimulus S1, corresponding to a grid voltage of 230 V RMS at 50 Hz, is applied to the PCB input port.

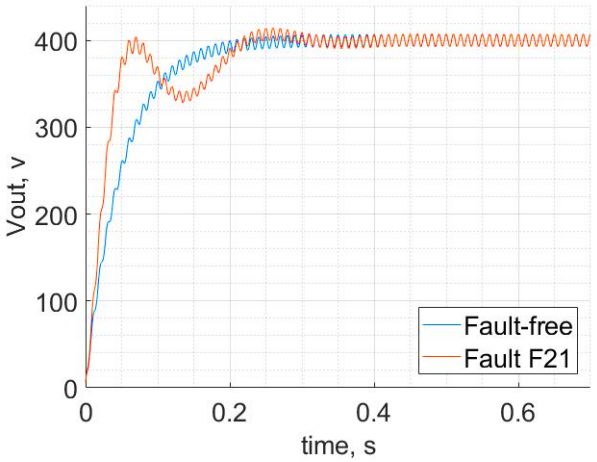

Figure 14: The F21 fault effects, compared to the fault-free behavior.

Figure 14 shows the trend of the PSU output voltage in two cases, i.e., the fault-free scenario and in presence of the considered fault. With the *base functional* approach it is not possible to observe the fault; in fact, in steady-state the behavior of the circuit affected by the fault is similar to the expected one. Instead, with the *timely enhanced functional* approach it is possible to detect the fault observing the transient behavior it produces, which is considerably different from the expected one, as shown in Figure 14. Moreover, the F21 fault can be observed with the *observability enhanced functional* approach by measuring the signal present on the IGBT gate. The analogue controller FAN9673 modifies the duty cycle value of the square wave applied to the IGBTs. In the fault-free scenario, the duty cycle is approximately 40%, while in the presence of the fault the duty cycle is approximately 58%.

F. RESULT ANALYSIS

In this sub-section the results obtained with the different test methods are compared. The reported results refer only to the tests performed at the end-of-line (i.e., at the end of the PCB manufacturing process); thus, the incoming inspection test is excluded and is considered as a reference method, only. Overall, all the catastrophic faults considered for the power diode are detected. The diode is almost always tested satisfactorily by all the different functional approaches considered. Therefore, in this case a base functional approach is sufficient to test the diode, as shown in Table 10. On the other side, the in-circuit test is not particularly effective, as it detects only one of the faults considered, as shown in Table 8. Different considerations can be drawn concerning the IGBT test. Figure 15 summarizes the previously shown results. Overall, 28 faults out of 31 are detected in the IGBT device. Figure 15 shows the number of faults detected by each test method considered. Furthermore, Figure 15 shows the number of faults detected exclusively by a single test method; for example, the *in-circuit* test detects 4 faults that are not detected by any other test method. From Figure 15 it is possible to note that the *base functional* approach detects just 15 faults out of 31: this is due to the low observability of this approach. Instead, the in-circuit test and the *observability enhanced functional* detect 24 and 25 out of 31 faults, respectively. In the IGBT devices, three faults are never detected. These faults (F13, F16 and F17) are associated with the antiparallel diode present in the IGBT. In this PSU this antiparallel diode is unknot used, causing the 3 faults to become untestable. However, they will never be able to produce any failure in the considered PCB.

Results similar to those reported in Figure 15 can be easily and automatically computed using our method for any system and for different test methods. They can be very useful for the test engineer to preliminarily estimate the effectiveness of every test method and select the best mix, able to achieve the right trade-off between the achieved FC and the affordable test cost. In general, it can be seen that the test of a more complex component, e.g., the IGBT, requires a greater number of different test methods to achieve an adequate FC.

Moreover, from the experimental results it is possible to see that the three boost cells introduce a significant redundancy in the PSU. In some situations, the PSU control system is able to compensate the effect of a fault, as discussed in sub-section V.E. In general, more boost cells are added to the PSU to increase the power delivered by the PSU to the electrical load. In safety-critical systems, it may be useful to add more parallel boost cells in the PSU not only to increase the output power of the system, but also to create a redundant system which is more tolerant to faults. Clearly, this will introduce faults which may be untestable, and whose long-term effects on the system reliability should also be considered.

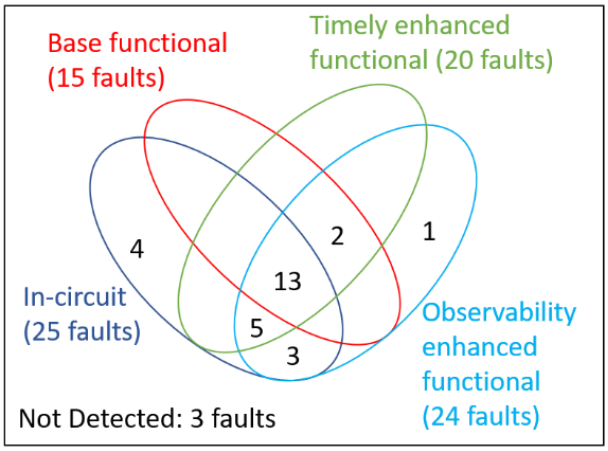

Figure 15: Comparison of the different test approaches for the IGBT

VI. CONCLUSIONS

Given the increasing usage of power electronic systems in safety-critical applications, it is crucial not only to devise effective test procedures at the end of the production process and in the field, but also to quantitatively assess their effectiveness, as mandated by the different standards and regulations.

This paper investigates the applicability of the fault models recently introduced for analog circuits when assessing the effectiveness of the test procedures for power devices at the PCB level. A systematic method able to generate the list of possible catastrophic faults starting from the equivalent electrical model of the device under test is proposed. A simulation-based approach can then be adopted to evaluate the percentage of faults in this list that can be detected (Fault Coverage), given different test procedures and different input stimuli. To practically evaluate the effectiveness of the considered approach, the Fault Coverage achieved by different test procedures on 2 power devices used in an industrial power supply unit is evaluated. Different test strategies are considered and compared (incoming inspection, in-circuit and functional).

To the best of our knowledge, this is the first paper describing a method to automate the assessment of the quality of different test procedures for testing power devices on a PCB. In particular, resorting to the case of study we selected, we show that using the proposed approach it is possible to automatically identify all faults detected by a given test solution, and thus to select the right mix of test steps, which can provide a satisfactory trade-off between the FC, the test duration and cost. Furthermore, it is possible to identify any redundant tests that do not introduce any contribution to the final FC. The method also allows to quickly identify those faults that cannot be detected, in some cases due to the fault tolerance features existing in a given design. The results provided by our method may also allow the designer to introduce changes in the PCB

design (e.g., to introduce further test points) to increase the number of testable faults.

In this work only 2 power devices have been considered, representing the key elements of the PSU considered. However, it is possible to extend the proposed approach to any electrical component whose equivalent electrical model is available, e.g., capacitors. Furthermore, the paper considers the permanent single fault scenario; however, there is no theoretical obstacle in considering multiple faults at a time using the same approach we proposed.

Finally, our approach paves the way to automate the test generation and test quality assessment process, reducing the amount of required manual effort and expertise.

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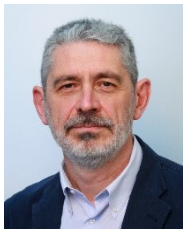

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