Single-ended to differential output converter for a 4-Channel front-end integrated circuit in liquid argon

Single-Ended to Differential Output Converter For a 4-Channel Front-End Integrated Circuit in Liquid Argon

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***Abstract*—This work contains the structure and transistor-level design of CMOS single-ended to differential-ended converter for the front-end integrated circuit. The front-end is used to readout large area SiPM at LAr temperature (87 K). The converter circuit, a fully-differential amplifier and two non-inverter amplifiers, was implemented using a standard 110 nm CMOS technology. Fully differential stage was designed using a Folded Cascode Operational Trans-impedance Amplifier (OTA) with a common mode feedback, a power rail of +1.25 V and -1.25 V, a power consumption of 20 mW and an unity gain in closed-loop. The converter circuit is connected, on the input, to a front-end integrated circuit. The front-end readout a SiPM tile of 24 cm^2 produced in the Darkside collaboration project. The circuit converts a single-ended signal, with a peaking time of 250 ns, a timing jitter of 10 ns and SNR larger than 10, into a differential output.**

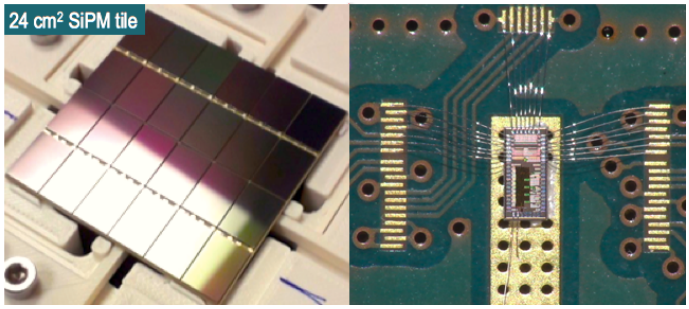

Fig. 1: A 24 cm^2 SiPM tile and front-end electronic developed [10]

I. INTRODUCTION

Time projection chamber (TPC) technology used with Xenon and Liquid argon (LAr) are being used on experiments for direct dark matter and neutrino detection such as DarkSide20K [1] or ProtoDUNE [2], Xenon100 [3], [4]. The silicon photomultipliers (SiPMs) have gained an important role in these experiments due to the low cost, the robustness and the high photodetection efficiency (PDE $>$ 45 %). The ultra-violet SiPM technology presents an optimal behaviour to operate at Xenon and Lar temperature because of the excellent cryogenic performance of silicon sensors [5], [7]. This work describes the transistor-level design of a single-ended to differential converter with LVDS output signal. The converter will be connected, on the input, to an amplifier chain, which readout a large area (24 cm^2) of SiPMs, produced by FBK [6] at Liquid Argon (LAr) temperature (87 K) using a standard CMOS 110 nm technology. The front-end electronic and the target sensor have been developed by the Darkside collaboration (Fig. 1).

The single-ended to differential converter has been designed with two kind of circuits. Primarily, a fully differential Folded Cascode with a common mode feedback and secondly, a single-ended folded cascode proposed by the book in [8], [9].

The Folded Cascode architectures (fully and single ended) have been designed to reduce the probability of hot carrier effect in the 110 nm standard CMOS technology. Thus, some hot carrier reduction techniques were applied to increase the lifetime of transistor, such as the reduction of drain-source voltage in order to reduce the stress on transistors, and a longer channel length to reduce the internal electric field. Additionally, the NMOS transistors present a larger channel length than PMOS transistor, due to the fact that these are more susceptible under low temperature conditions [11].

Under cryogenic temperature of 77 K, the mismatch variables, A_{th} and A_{β}, present negligleble modification [12]. Furthermore, the ratio $\frac{G_m}{I_d}$ remains almost invariable in comparison with 300 K [13]. Thus, the converter circuit was designed considering these values (mismatch and $\frac{G_m}{I_d}$) at room temperature for 110 nm technology. The converter circuit has been simulated using a cryogenic SiPM electrical model [14] and a tested front-end electronic at 77K.

The single-ended to differential converter is connected, on the input, to the cryogenic front-end for readout a SiPM tile of 24 cm^2. This allows a differential output signal to be processed by a cryogenic optical driver with differential input used in the DarkSide framework. The converter circuit keeps signal-to-noise ratio (SNR), defined as the peak value of a single photo-electron (PE) signal divided by total r.m.s. output noise voltage, and a Jitter, defined as the standard deviation of the output baseline over the slew rate, equal to the single-ended signal.

II. DESIGN AND IMPLEMENTATION

This work presents a transistor-level design and simulations for a single to differential converter. The converter, shown in Fig. 2, is composed by 2 blocks. First, a fully differential amplifier with a common mode feedback (A2) to guarantees a stable and fixed common mode output voltage. Furthermore, the circuit includes two non-inverter amplifier (A3 and A4) with a class AB output stage and a gain equal 2. The class AB stage guarantees a symmetrical slew rate with a high power efficiency.

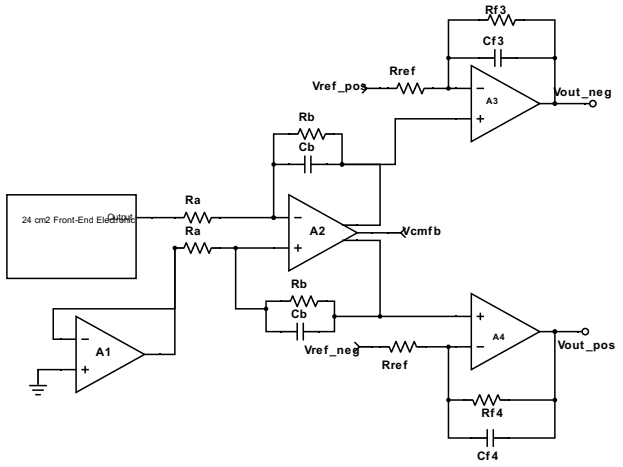

Fig. 2: Simplified schematics for the single to differential converter

The fully differential and non-inverter circuit are designed using a Folded Cascode (FC) architecture with a PMOS input transistor and an NMOS cascode. This transistor topology develops a low Flicker noise [15], and the architecture provides a maximum common mode voltage range necessary to process hundreds of PEs. The input transistors (M1 and M2) operate in week inversion with an inversion coefficient, IC, equal to 1. This generates a large trans-conductance with low power consumption [9] and a negligible variation of $\frac{G_m}{I_d}$ over temperature [13]. The aspect ratio of the input transistors, to guarantee a gainbandwidth (GBW), is calculated following Eq. (1). Additionally, the input transistor area should be large enough to improve the matching and reduce the capacitive noise induced by the detector capacitor (9 nF). The bias current is fixed following Eq. (2) and Eq. (3).

$$\left(\frac{W}{L}\right)_{1,2} \geq \frac{(C_o * GBW)}{2\beta_p \Phi_t e^{\frac{V_{gs}-V_{th}}{n\Phi_t}}}\Bigg\} \tag{1}$$

$$I_{spec} = K_p \left(\frac{W}{L}\right)_{1,2} (2n * \Phi_t)^2\Bigg\} \tag{2}$$

$$I_{d1,2} = IC * I_{spec}\Big\} \tag{3}$$

With:

- $I_{d1,2}$ = 500 uA;
- GBW, Gain Bandwidth product;
- C_m, Capacitance on the output node;
- n, Slope factor $\frac{C_{ox}-C_{dep}}{C_{ox}}$;
- K_p =$\frac{\mu_p C_{ox}}{2n}$, μ_p carrier mobility of PMOS and C_{ox}, Silicon oxide capacitance;
- Φ_t, Thermal voltage, 6.7 mV at 77 K;

The fully differential amplifier, shown in Fig. 3, presents a unity gain configuration. The non-inverter stages, shown in Fig. 4, are voltage amplifiers with a gain equal to 2. In these stages, the baselines are shifted to the top and the bottom in order to obtain a LVDS signal. The simplified schematics of the full converter is illustrated in Fig. 2.

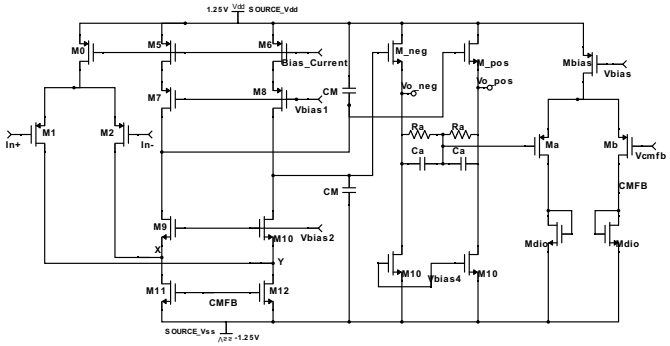

Fig. 3: Transistor-level design of Fully differential amplfier (A2).

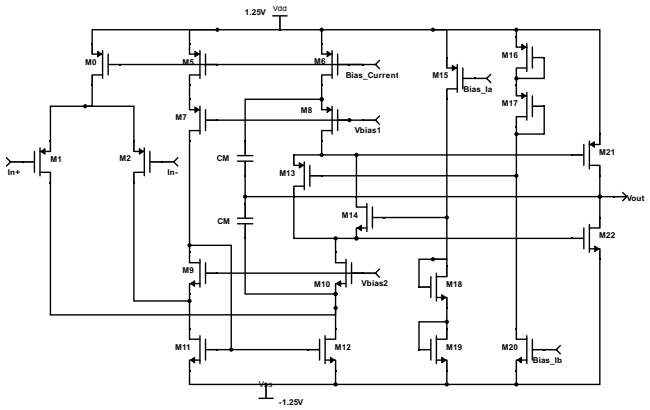

Fig. 4: Transistor-level design of non-inverter stage (A1, A3 and A4) implemented in the Front-End Electronic [10].

The stability is a crucial factor in this kind of circuit with unity or low gain, because the closer the bandwidth to the GBW value, the higher the peak created at GBW frequency, as shown Fig. 5c, which causes instability. Thus, a strong pole splitting compensation is applied in these circuits, which present capacitors of 5-7 pF.

In each circuit stage, a pole splitting compensation is applied to shift the second pole, produced by the parasitic capacitance, 3 times higher than the GBW value. This compensation guarantees a safe phase and gain margin as shown

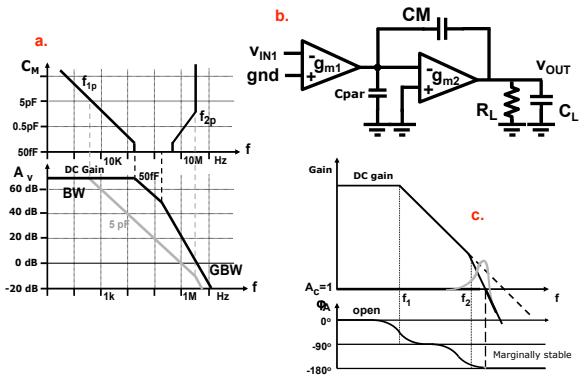

Fig. 5: Pole splitting compensation technique

Fig. 5a. The compensation is realised by the capacitor C_M together with the trans-conductance of the second stage, G_{m2}, shown in Fig. 5b.

On the other hand, the non-inverter amplifiers have a voltage control, which allows to fix the baseline on the top and bottom. For this design, the output baselines are placed at 700 mV and -700 mV. Hence, the total output swing is 1.4 V.

III. SIMULATION RESULTS

The converter circuit was simulated using standard Spice models of 110 nm CMOS technology provided by the foundry PDK (Process Design Kit). On the other hand, the mathematical extrapolation of the BSIM models provide an approximate response of the MOSFET to be obtained at cryogenic temperature of 77K, since semiconductor foundries do not provide characterisation qualified models for temperature corners below $-40°$. However, we assumed the reliability of the drain current and trans-conductance of transistors within simulation at 77K justified by internal tests of the single transistors and previous work realised under this temperature conditions. The SNR, Jitter and noise simulations were done by connecting a cryogenic SiPM electrical model [16], and a front-end electronic [10]. The front-end electronic design was already tested at 77 K with successful results . The output signal of the front-end circuit, obtained by 200 photo-electrons, is converted to a differential waveform as shown Fig. 6.

The transient simulation was performed using a post-layout netlist of the converter circuit. In the meantime, the front-end circuit was simulated at schematic level. Additionally, a post-layout summary of the electrical parameters for the cryogenic converter circuit can be appreciated in Table. I. The stability fully differential presents a phase margin of $60°$ and the non-inverter equal to $50°$ with 1 MΩ of load.

To perform a precise Monte Carlo simulation, a voltage waveform generated by the front-end electronic is applied on the input. This allows to generate Monte Carlo simulations without the front-end effects (mismatch and process variation). After that, a Monte Carlo simulation was executed to estimate the robustness of the circuit under a statistical variations of the active and passive device process parameters. Fig. 7 and

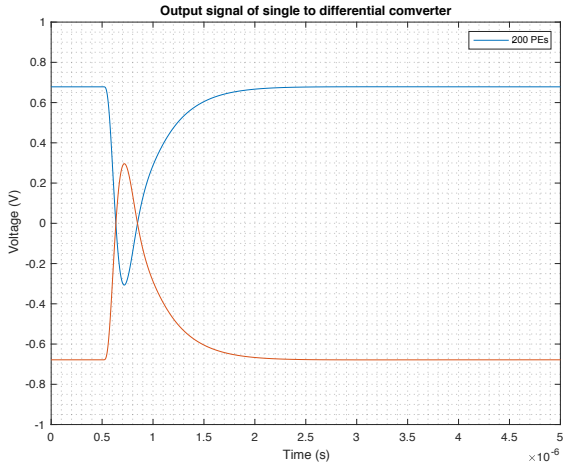

Fig. 6: Differential output signal with 200 PEs.

TABLE I: Parameters and simulation results of converter circuit

Parameters	Simulation Results
W/L$_{M1,M2}$	12000
Cm(unity gain) (fpF)	5 pF
Dynamic Range (PEs)	$>$ 300
PM(unity gain)	50
Vout(mV)	9
Vnoise(mV)	0.82
SNR	11
Jitter (ns)	12

Fig. 8 show the positive and negative baseline variation at 77 K for the circuit. The converter presents a mean V$_{outpos}$ = 692 mV with std. dev. = 8 mV and a mean V$_{outneg}$ = -706 mV with std. dev. = 8.7 mV.

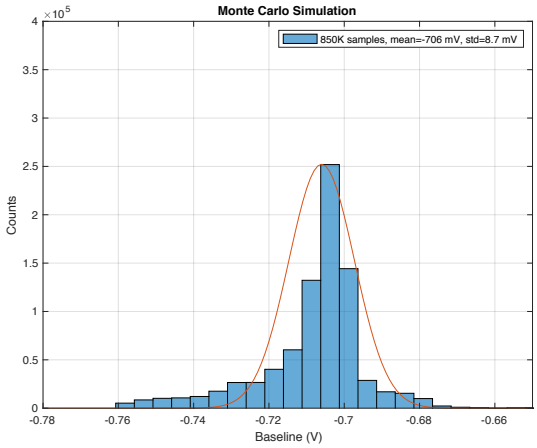

Fig. 7: Monte Carlo simulation of negative output converter.

IV. CONCLUSION

This paper provides the transistor-level design and post-layout simulation of a CMOS single-ended to differential

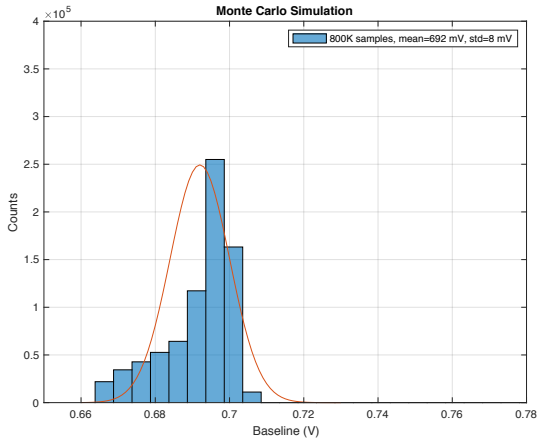

Fig. 8: Monte Carlo simulation of positive output converter.

converter for the front-end circuit for readout the large area SiPM at cryogenic temperature of 77 K in the darkside collaboration. The circuit was designed using the standard CMOS 110 nm technology. This first prototype was sent to fabrication and will be tested with a front-end included in the same test-chip but this was already tested in a previous tapeout. The post-layout simulation results show a SNR above 10 and a timing Jitter better than 15 ns for the signal produced by a single photo-electron.

REFERENCES

[1] C. E. Aalseth, F. Acerbi, et al., "DarkSide 20K: A Yellow book technical proporsal/pre-technical design report" INFN, 2016

[2] J. Stewart, "The ProtoDUNE Single-Phase Detector", IEEE Nuclear Science Symposium and Medical Imaging Conference, 2017

[3] XENON100 Collaboration, "The XENON100 Dark Matter Experiment", Astropart. Phys. 35 (2012), 573-590.

[4] G. Geronimo et al, "Front-end ASIC for a Liquid Argon TPC ", NUCLEAR SCIENCE, VOL. 58, NO. 3, JUNE 2011.

[5] F. Acerbi et al., "Cryogenic Characterization of FBK HD Near-UV Sensitive SiPMs", IEEE Transactions on Electron Devices, Vol. 64, Iss. 2, 2017.

[6] A. Gola et al., *NUV-Sensitive Silicon Photomultiplier Technologies Developed at Fondazione Bruno Kessler*, National Center for Biotechnology Information, Sensors (Basel). 2019 Jan; 19(2): 308.

[7] C. Aalseth et al., "DarkSide-20k: A 20 tonne two-phase LAr TPC for direct dark matter detection at LNGS", Eur.Phys.J.Plus 133 (2018) 131.

[8] J. Huijsing, "Operational Amplifier Theory and Design", Springer 2011.

[9] W. Sansen, "Analog Design Essentials", Springer Verlag, edition 2016.

[10] A. Martinez, "4-Channel Front-End Integrated Circuit For Readout of Large Area of SiPM under Liquid Argon", PRIME 2019.

[11] J. Hoff, G. Deptuch, et al., "Cryogenic Lifetime Studies of 130nm and 65nm nMOS Transistors for High-Energy Physics Experiments", IEEE Transactions on Nuclear Science, 62(3), pp.1255-1261, 2015.

[12] P. A. Hart, et al, "Characterization and Model Validation of Mismatch in Nanometer CMOS at Cryogenic Temperatures", 48th European Solid-State Device Research Conference, 2018.

[13] Arnout Beckers, Farzan Jazaeri, et al, "28-nm Bulk and FDSOI Cryogenic MOSFET", IEEE International Conference on Integrated Circuits, Technologies and Applications 2018.

[14] M. Biroth, P. Achenbach, et al, "Modelling and Characterization of SiPM Parameters at Temperatures between 95K and 300K," IEEE Transaction on Nuclear Science, pp.1-1, Oct, 2017.

[15] A. Rivetti, "CMOS Front end electronics for radiation sensors,", CRC press, 2015.

[16] F. Corsi et al, "Modelling a silicon photomultiplier (SiPM) as a signal source for optimum front-end design", Nuclear Instruments and Methods in Physics Research A 572 (2007) 416418.