Summary

The LHC accelerator complex aims to enhance its own performances with the purpose of increasing the potential for discoveries in the next years. The main objective of the HL-LHC upgrade is to enhance luminosity by a factor of 10 beyond the LHC design value in order to obtain an extensive dataset for new physics searches.

The HL-LHC should be operational from 2026 and the upgrade consists of a massive improvement of both the accelerator machine and the experiments. Its development will be a significant technological challenge both in terms of hardware and software.

The increase in peak luminosity will provoke unprecedented levels of event pile-up and all the experiments must plan to upgrade their detectors in order to perform a better event reconstruction, to improve the performances in an harsher radiation environment, and to overcome the aging effect.

This PhD activity is part of the CMS EB upgrade group effort. Indeed the custom LiTE-DTU ASIC developed at the INFN Torino belongs to the baseline choice for the upgraded VFE board. The enhanced board will allow to reduce the shaping time of the signal, mitigate the APD noise, improve the spike identification, and increase the signal information through an higher sampling rate.

The LiTE-DTU ASIC has been fabricated in a 65 nm CMOS technology and has a size of 2×2 mm^2. The ASIC embeds two 12-bit 160 MS/s ADCs, a PLL, and a digital architecture (DTU) dedicated to the online data selection, lossless compression and data serialization at 1.28 Gb/s. The LiTE-DTU ASIC is designed to be placed inside the experimental area, close to the detector. Therefore, considering the harsher radiation environment foreseen for Phase-2, several radiation-hard design techniques have been implemented in the design.

This thesis reports the design and characterization of the first prototype of the LiTE-DTU ASIC and it is organized as follows.

Chapter 1 briefly describes the LHC complex with a focus on the CMS experiment along with its own sub-systems. Moreover, an introduction of the HL-LHC upgrade and the scientific and technological goals are presented.

The legacy readout chain of the EB is introduced in Chapter 2, with particular emphasis on the on-detector electronics. Moreover, the technical reasons of the upgrade for the HL-LHC are presented along with the chosen strategy for the on-detector electronics upgrade. Then, an overview of the two new custom ASICs, CATIA and LiTE-DTU, are described likewise the hardware requirements for the upgraded electronics.

Chapter 3 is subdivided into several parts and provides an outline of the LiTE-DTU ASIC architecture and a detailed description of the building blocks included in the design of the first prototype. In the last part of the chapter, the implementation of the DTU is discussed along with the performed post-layout simulations and the latency study.

Chapter 4 is a report of the electrical characterization of the first prototype of the LiTE-DTU, showing the functionality of each block.

In Chapter 5 the TID and SEU qualification tests performed on the ASIC are reported along with the results.

Chapter 6 closes the thesis with a summary of the PhD activity along with the future development for the following chip submissions.