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03 September 2025

Fully-Synthesizable Current-Input ADCs for Ultra-Low Area and Minimal Design Effort

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***Abstract*— A fully synthesizable ADC architecture is proposed for low-end current sensing applications. Being based on standard cells and designed with a fully-automated flow, the proposed ADC allows very low area, digital-like scaling across CMOS technology generations, technology and design portability, minimal design effort, and immersed-in logic design (i.e., low integration effort), compared to traditional analog-intensive designs. In addition, it allows direct current readout without requiring a transresistance stage.**

Testchip measurements show a 5-nA to 1-µA input range, 6.7-bit ENOB and 2.2-kS/s sample rate, at 940-nW power and 4,580-µm^2 area. To the best of the authors' knowledge, this testchip is the first demonstration of a fully-synthesizable input-current ADC. Along with the analysis of the specific limitations of the presented demonstration, this work aims to pave the way for a new class of current-input ADCs that can be designed and integrated with logic within hours, and occupy a silicon area in the order of 10kgates.

Keywords*— *Fully-synthesizable, standard cell-based, Analog-to-Digital Converter, current sensing, low design effort, low area.

I. Introduction

Analog-digital converters (ADCs) are an essential component of Systems on Chip where sensing capabilities are required, either as part of the interface towards off-chip sensors, or to sense on-chip physical parameters. Although voltage sensing is predominant, current sensing and conversion are required for the readout of sensors with current output or high output resistance [1]. A few examples of applications requiring current sensing are electrochemical biosensors [2], temperature sensing [3] (e.g., thermistor-based), environmental monitoring [4] (e.g., gas sensing), biomedical signal acquisition [5] (e.g., potentiostat-based), light sensing [6] (e.g., photodiodes and photoconductors), imaging [7], and on-chip leakage/variation monitoring [8], which require relatively coarse conversion in the µA and kHz range or below.

In low-cost systems (e.g., sensor nodes), on-chip integration of ADCs is subject to significant limitations in terms of acceptable silicon area, as well as design and integration effort [1]. In addition, the high design effort and cost required in recent CMOS technologies has motivated significant research on architectures and sub-systems that reduce the design effort by an order of magnitude, and are technology scaling-friendly or portable [9]. Accordingly, various ADC architectures that can be partially or fully synthesized with standard cells and fully automated design flows have been explored, for applications allowing relaxed specifications (e.g., resolution in the 6-9 bit range), and restricted to voltage-input ADCs [10]-[19]. Fully-synthesizable ADCs are also inherently amenable for low-voltage operation, simplifying system integration with the digital sub-system and the on-chip power delivery. Also, the adoption of voltage-input ADCs to convert current signals requires analog-intensive design of a transresistance amplifier to first convert the input current into a voltage, negating the benefits offered by full synthesizability. Similarly, current-voltage conversion via a large shunt resistor imposes a lower input current bound to assure adequate dynamic range at the voltage ADC input, significant area penalty at currents in the tens of µA range and below compared to the ADC itself, and additional temperature dependence.

In this work, the first fully-synthesizable current-input ADC architecture for direct acquisition of current signals is proposed, with no need for a transresistance amplifier stage. Being based on standard cells and an automated digital design flow, it retains the benefits of digital circuits in terms of ultra-low design effort (e.g., man-hours instead of months), ultra-low area, technology and design portability, and inherent integration with logic. A 40nm testchip demonstration exhibits a 5nA-1µA input range, 7-bit resolution, 2.2-kHz sample rate, 940-nW power, very compact area of 4,580µm^2.

The paper is structured as follows. Section II introduces the proposed ADC architecture. Testchip design and measurement results are reported in Section III. Conclusions are drawn in Section IV, along with remarks on prospective performance improvements on this first demonstration.

II. Proposed ADC

A. Proposed ADC Architecture and Qualitative Analysis

The architecture of the proposed current-input N-bit ADC is illustrated in Fig. 1. As basic principle, the negative feedback loop in this figure assures that the feedback current $I_{feedback}$ has equal magnitude (and opposite direction) as the input current I_{in} by the end of each conversion, as a result of a successive approximation current search.

As first component of the forward path of the feedback loop, the digital buffer *BUF* acts as a voltage comparator, as its output OUT_{BUF} is high (low) when its input is above (below) its logic threshold V_{LT}. Being symmetrically-sized, $V_{LT} = V_{DD}/2$ under a supply voltage V_{DD} (see considerations on matching in Section III). OUT_{BUF} drives the successive approximation logic that is commonly used in SAR ADCs [15]-[18]. The SAR logic generates a sequence of digital values that progressively converges to the value corresponding to the input in N SAR iterations.

At each SAR step, the digital output of the SAR logic is converted into the corresponding analog current by the fully-digital current DAC in Fig. 1. Fully-digital current DAC operation is obtained by first converting the digital SAR logic output to a 2^N-cycle pulse train via Dyadic Digital Pulse Modulation [19]-[21] (DDPM, see right inset). As shown in Fig. 2, the output of the DDPM modulator OUT_{DDPM} is a pulse train containing a number $n_{1,DDPM}$ of 1's that is given by $\sum_{i=0}^{N-1} OUT_{SAR,i}\, 2^i$ (i.e., it is equal to the integer $OUT_{SAR} = OUT_{SAR,N-1} \dots OUT_{SAR,0}$ itself), and a number of 0's given by $n_{0,DDPM} = 2^N - \sum_{i=0}^{N-1} b_i\, 2^i$. In other words, the DDPM modulator converts the SAR logic output into a pulse train whose pulse density $n_{1,DDPM}/2^N$ is equal to OUT_{SAR}.

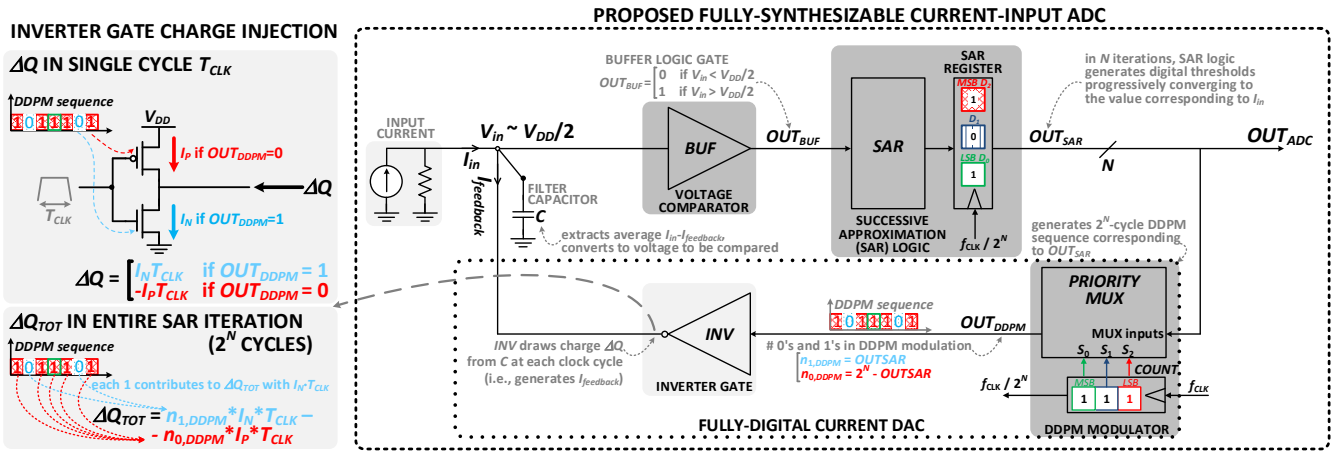


Fig. 1. Proposed fully-synthesizable current-input ADC architecture (example with N=3 bit).

In turn, the pulse density of OUT_{DDPM} is converted into an average current $I_{feedback}$ by the subsequent inverter gate *INV* loaded by the filter capacitor C, which closes the loop. In detail, in each single clock cycle, the inverter gate draws from (injects into, if negative) C an amount of charge ΔQ equal to

$$\Delta Q = \begin{cases} I_N T_{CLK} \text{ if } OUT_{DDPM} = 1 \\ -I_P T_{CLK} \text{ if } OUT_{DDPM} = 0 \end{cases} \quad (1)$$

where I_N is the NMOS on-current as in Fig. 1 (see left inset), and is equal to the PMOS on-current I_P under symmetric sizing. The filter capacitor C is sized in view of the strength of the inverter and of the DDPM clock frequency, to have a negligible voltage ripple $\Delta Q/C$ on V_{in}, as to have drain-voltage induced variations in I_N and I_P below 1LSB.

When considering the entire set of 2^N clock cycles within each SAR iteration, the average current $I_{feedback}$ generated by *INV* is equal to the overall charge ΔQ_{TOT} injected in C divided by the overall time period $2^N T_{CLK}$, where

$$I_{feedback} = \frac{\Delta Q_{TOT}}{2^N T_{CLK}} = \frac{n_{1,DDPM} - n_{0,DDPM}}{2^N T_{CLK}} I_N T_{CLK} = \\ = \frac{OUT_{SAR} - (2^N - OUT_{SAR})}{2^N} I_N = \frac{OUT_{SAR} - 2^{N-1}}{2^{N-1}} I_N \quad (2)$$

Ultimately, the voltage across C at the end of each SAR iteration is set by the overall current $I_{in} - I_{feedback}$ applied to it, as discussed in the following subsection.

B. Detailed ADC Operation and Properties

To gain a first insight into the feedback loop operation, let us first analyze the circuit in Fig. 1 at the zero-current bias point, i.e. when I_{in}=0. At the end of the conversion, *INV* has to provide an average current $I_{feedback} = I_{in} = 0$, or equivalently ΔQ=0. From (2), this requires that the DDPM sequence has an equal number of 1's and 0's (i.e., $n_{1,DDPM} = n_{0,DDPM}$), leading to a square wave with 50% duty cycle. In turn, this requires that the DDPM input is invariably 100…0, i.e. the SAR input is equal to 1 for the first SAR iteration and 0 for the subsequent ones. Equivalently, the input voltage V_{in} of the voltage comparator *BUF* is equal to the middle-point value $V_{LT} = V_{DD}/2$, as desired for a current range centered around zero. It is worth noting that the condition $V_{in} = V_{DD}/2$ is invariably true at the end of the conversion, even under non-zero inputs. Indeed, $I_{feedback}$ systematically converges to I_{in} at the last SAR iteration, thus making the overall current $I_{feedback} - I_{in}$ equal to zero in any case.

Since $I_{feedback} = I_{in}$ at the end of any conversion under arbitrary input currents, *INV* always needs to inject an extra charge ΔQ to compensate the charge drawn by I_{in} during the $2^N T_{CLK}$ cycles of the last DDPM sequence at the N-th SAR iteration. In other words, ΔQ must make the average *INV* current in (2) equal to I_{in}, thus immediately yielding to the following condition on the ADC output OUT_{ADC}

$$OUT_{ADC} = OUT_{SAR} = 2^{N-1} \frac{I_{in}}{I_N} + 2^{N-1}. \quad (3)$$

As desired, (3) is the output characteristics of an ADC having an input centered around I_{in}=0 (i.e., leading to an output equal to the output 2^{N-1}, corresponding to OUT_{ADC}=100…0). From (3), the dynamic range of the proposed current-input ADC goes from $I_{in} = -I_N$ (i.e., OUT_{ADC}=00…0) to $I_{in} = I_N$. From (3), the LSB is equal to $I_N/2^{N-1}$. In other words, the ADC characteristics is defined by the on-current I_N in *INV* in Fig. 1, and the bit width N of the SAR and DDPM logic. When non-idealities are accounted for, the effective resolution is degraded compared to the ideal value N. The effect of such non-idealities is summarized in the testchip demonstration in Section III.

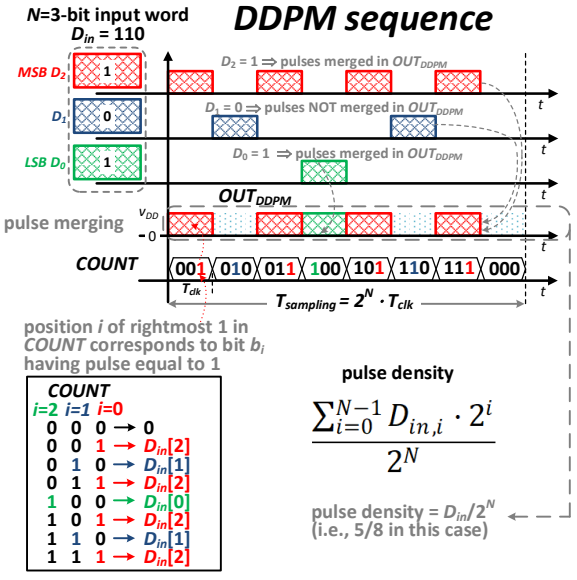


Fig. 2.Properties of DDPM modulation [19] - [21] (example with N=3 bit).

III. Experimental Results

The ADC architecture introduced in Section II was implemented in the 40nm CMOS testchip shown in Fig. 3. The standard cell logic includes the buffer, the inverter gate, the SAR logic and the DDPM modulator in Fig. 1. These were synthesized, placed and routed automatically, and occupy a silicon area of 780 μm^2. The filter capacitor C was implemented by automatically instantiating (e.g., via scripting), placing and routing a p-cell of a Metal Oxide Metal (MOM) capacitor. The overall 10-pF capacitance assures operation at clock frequency down to 27MHz under minimum strength *INV*, and occupies an area of 3,800μm^2 when using the first four metal layers (it could be approximately halved using the full 10-metal stack). Both the inverter *INV* and the buffer *BUF* in Fig. 1 were symmetrically sized with minimum strength. From Table I, the overall ADC area of 4,580μm^2 is the lowest reported to date, and such benefit is expected to be retained at finer technologies in view of the standard cell nature of the proposed architecture. In detail, the area is 39-111X smaller than other fully-synthesizable designs [11],[12].

The testchip was characterized at 25°C and 600mV supply, at 2.2-kHz sample rate. The measured power consumption is 940nW, of which 10% is due to leakage. The power consumption was found to be nearly the same under both constant and dynamic inputs. From the static characterization of the ADC in Fig. 4, the dynamic range is 45.2dB. The maximum integral nonlinearity (INL) is $\pm$1.5 LSB at 8-bit resolution, whereas the RMS INL is 0.5 LSB. The maximum and RMS differential nonlinearity (DNL) are respectively $\pm$1.9 LSB and 0.3 LSB.

The dynamic characterization of the ADC was performed under a 30-Hz sine wave input with 90% of full scale amplitude. Results in Fig. 5 show an SNDR of 42.1dB, which translates into 6.7-bit ENOB. As shown in Table I, such resolution is better than state-of-the-art digital standard cell-based [11] and custom digital ADCs [10], comparable to

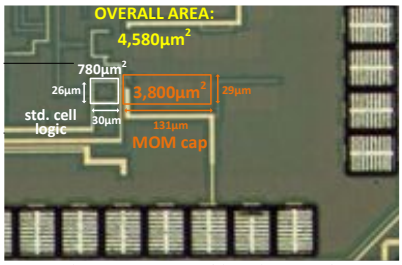
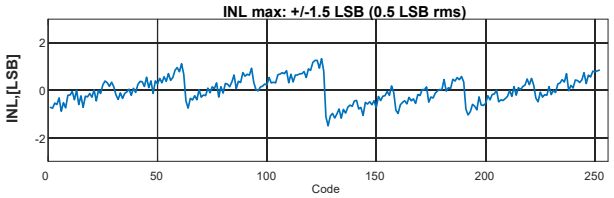
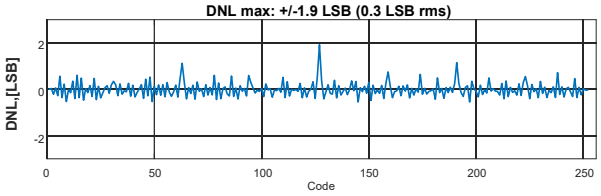


Fig. 3. 40nm testchip micrograph.

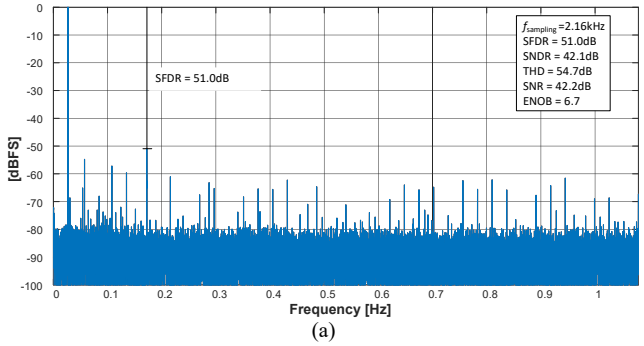


(a)

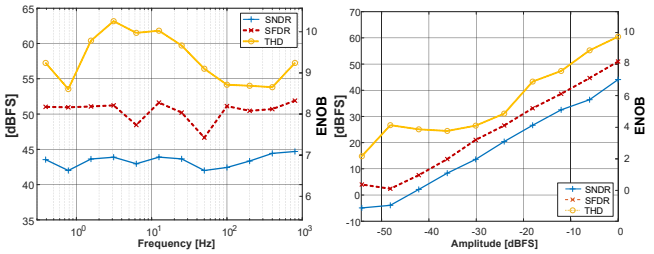


(b)

Fig. 4. ADC static characterization: a) INL and b) DNL vs code.



(a)



(b) (c)

Fig. 5. ADC dynamic characterization: a) output spectrum @ 30Hz sine wave input, b) SNDR, SFDR and THD versus frequency, c) SNDR, SFDR and THD versus amplitude.

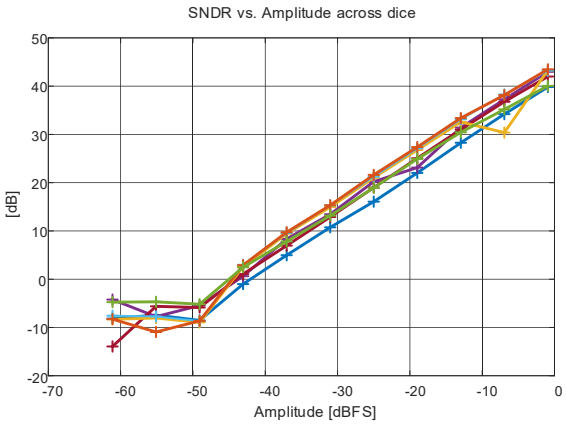


Fig. 6. ADC dynamic characterization (SNDR) across other five dice.

ADCs designed with analog generators [15] (although at a 1000x lower sample rate), 1.4-bit worse than VCO-based ADCs based on custom digital circuits, design resolution is also comparable to [13]. ΔΣ based on digital custom circuits outperform all other classes. From Fig. 5a, the SFDR (THD) performance of 51dB (54.7dB) is rather better than the SNR performance (42.2dB), and leads to 8 (9) equivalent bits.

In other words, the testchip effective resolution is mainly limited by the input noise of the *BUF* voltage comparator in Fig. 1, as expectable in view of its minimum size. Figs. 5b-c reveal that SNDR, SFDR and THD have consistent performance over frequency up to the Nyquist frequency, and a fair 1dB/dB roll-off versus the input signal amplitude. The above results were found to be consistent across dice, as shown in Fig. 6. This figure shows that the maximum SNDR difference across five other dice is 8dB, leading to 1.3ENOB change.

From the above considerations, the resolution can be improved by adopting a *BUF* standard cell with larger strength, at the cost of larger power consumption. Similarly, the adoption of an *INV* cell with larger size improves NMOS/PMOS matching. Beyond sizing, digital PMOS/NMOS strength calibration can improve matching

TABLE I. COMPARISON WITH STATE-OF-THE-ART FULLY- OR PARTIALLY-SYNTHESIZABLE ADCS

	[10]	[11]	[12]	[13]	[14]	[15]	[16]	[17]	[18]	This work
type of input	voltage	voltage	voltage	voltage	voltage	voltage	voltage	voltage	voltage	current
architecture	Flash	Flash	Flash	VCO-based	MASH ΔΣ	SAR	SAR	SAR	SAR	SAR
technology	180nm	90nm	130nm	65nm	65nm	28 FDSOI	28nm	40nm	28nm	40nm
area [μm^2]	94,000	180,000	510,000	26,000	14,000	32,120	8,600	31,000	2,000	4,580
F_S [S/s]	50M	21M	140M	205M	150M	2M	50M	32M	500k	2.2k
SNDR [dB]	35.6	34.61	28.5	50.3	56.3	46.43	56.8	47.37	34.2	42.1
SFDR [dB]	44	41.46	37	55.3	N/A	61.72	69.2	N/A	N/A	51
ENOB [bit]	5.62	5.45	4.5	8.1	9.06	7.42	9.2	7.6	5.4	6.7
supply voltage	1.3V	0.7V	0.7V	0.6V	1V	0.47V	N/A	1V	0.5V	0.6V
input range	±280mV	±140mV	±400mV	full scale	full scale	full scale	full scale	full scale	full scale	1μA
power [mW]	0.312	1.11	2.3	3.3	0.872	0.94	0.399	0.187	0.092	0.00094
FoM [fJ/convstep]	127	1,200	726	940	348.6	2.7	14.1	30.7	4,390	4,110
synthesizable*	partially	fully	fully	partially	partially	partially	partially	partially	fully	fully
degree of design automation	digital, custom cells	std. cell design flow	std. cell design flow	digital, custom circuits	digital, special std. cells added	analog generator	analog generator	analog generator (reusable code)	std. cell design flow	std. cell design flow

* Partially synthesizable = mixture of standard cells and custom design, fully synthesizable = standard cells only w/ automated digital design flow

further, especially under the presence of die-to-die variations.

As another possible circuit non-ideality that limits resolution once larger *BUF* and *INV* strength is used, the limited small-signal voltage gain of the comparator *BUF* in Fig. 1 might limit its ability to discriminate small changes down to the LSB. To overcome such limitation, the comparator voltage gain can be easily increased by cascading multiple buffers, instead of inserting only one as in Fig. 1.

IV. CONCLUSION

In this work, a fully-synthesizable architecture has been proposed for ultra-compact current-input ADCs requiring very low design effort, as only digital standard cells and automated design flows are required. The proposed ADC achieves the minimum area (4,580μm^2 with an active area of 780μm^2 only, corresponding to only 10kgates) and the highest resolution compared to prior fully-synthesizable ADCs (6.7 bits in dynamic conditions, 8 bits in static conditions).

Measurements on a 40-nm testchip showed operation at 2.2kS/s and 940nW. Although the sampling frequency is significantly lower than other fully-synthesizable ADCs, its operation in the kHz range makes suitable for a wide range of current sensing applications (see Introduction). To the best of the authors' knowledge, the testchip is the first demonstration of a fully-synthesizable current-input ADC. Hence, the ADC in this work allows direct current readout without requiring a transresistance stage, suppressing the related additional analog-intensive design effort that would be conventionally required by voltage-input ADCs.

This work aims to pave the way for a new class of current-input ADCs that can be designed and integrated with logic within hours, and occupy a silicon area in the order of 10kgates. Future work will focus on the improvement of the current-input ADC performance beyond this first demonstration, based on the performance bottlenecks identified from the measurements.

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