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***Abstract*—This paper presents an innovative stacked-FET cell useful to enhance both, gain and output power of RF and mm-wave power amplifiers. The new structure has been validated through the design of a downlink Ka-band Doherty Power Amplifier. The resulting module is a two stages Microwave Monolithic Integrated Circuit (MMIC) fabricated on a commercial 100nm gate length Gallium nitride on Silicon technology. The design was carried out to satisfy not only the power requirements but also to meet the thermal constraints for space use. Simulation results have shown a power added efficiency (PAE) greater of 30% at 6dB of output power back-off with a peak of output power of 38dBm inside the operative band, from 17.3 GHz to 20.3 GHz. Whereas, a saturated gain above 17dB has been achieved with a gain flatness better than 0.5dB in the overall band. The chip area is 5x3.7mm².**

Keywords—Stacked-FET, Doherty, power amplifier, Ka-band, GaN, silicon, MMIC.

I. INTRODUCTION

The growing demand of high data rate, higher system capacity, and massive device connectivity is posing severe challenges in the development of new communication systems. This is true not only for terrestrial networks [1], with the incoming 5G standard, but also for satellite systems [2]. On the one hand, there is the spectral crowding that imposes the selection of higher and higher frequencies [3], with a consequent increase of the devices losses and the issues related with multipath interferences. On the other hand, there is the need of adopting advanced coding techniques, and to use wider RF bandwidth, to maximize the system capacity. Therefore, forthcoming front-ends should be able to efficiently work with signals characterized by a large envelope variation with carrier frequency in the mm-wave range. These aspects further aggravate the challenges in the design of every sub-circuit within the front-end. Therefore, research activities aiming to improve the performance of solid state front-end are of significant importance [4].

To this purpose, a Ka-band Doherty power amplifier (DPA) which makes use of an innovative stacked-FET cell is presented. As know, the DPA architecture is promising for 5G systems due to its ability to provide high average efficiency when working with signals characterized by high peak-to-average power ratio without sacrificing too much the linearity. The designed Microwave Monolithic Integrated Circuit (MMIC) has been fabricated in a commercial 100 nm gate length GaN on Si technology [5]. The MMIC was developed for high throughput satellite, thus particular care was devoted in the design phases to find viable solution to respect the maximum junction temperature allowed for the devices.

The paper is organized as following: the DPA operating principle is briefly recalled in Section II together with the design requirements. Section III introduces the proposed stacked-cell underlying its advantages with respect to traditional approaches. Finally, the design of the DPA and the expected performances are reported in Section IV and V, respectively.

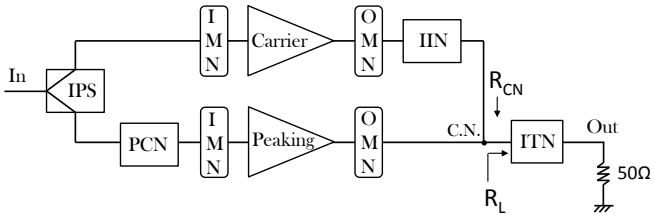

Fig. 1. DPA block diagram.

II. DPA BACKGROUND

The scheme of a typical DPA is shown in Fig.1. It consists of two branches of amplification, the Carrier (biased in class AB) and the Peaking (biased in class C) that cooperate each other to increase the average efficiency of the whole architecture [6]. Basically, the Peaking current is exploited to active modulate the load impedance seen by the Carrier device in order to keep its efficiency at maximum for input power from *break* to *saturation point*. The peaking mitigates also the gain compression of the Carrier thanks to its gain expansion when starts to conduct. In the standard DPA architecture, several sub-networks are present. An impedance transformation network (ITN) is used to transform the 50Ω termination in the required R_L at the common node (C.N.). Then, the impedance inverter network (IIN) is adopted to invert the R_{CN} behavior allowing a reduction of the Carrier impedance while the output power increases. A phase compensation network (PCN) is added at the input of to Peaking device to recover the phase shift introduced by the IIN. Finally, an input power splitter (IPS) is used to provide the required power splitting between the two branches.

The requirements of the developed DPA are reported in Table 1. The aim is to reach a saturated output power of 38dBm with a power added efficiency greater of 30% at 6dB of output-power back-off. As a starting point, a power budget analysis was carried out in order to select properly the periphery of the active devices to be used. Accounting for the power density of the selected GaN-on-Si process, and the unavoidable losses expected in the passive structures, a total active periphery of about 3.2mm resulted to be necessary in the final stage for reaching the specified saturated output power. Clearly, space de-ratings have been considered, thus the drain bias voltage has been reduced from 15V to 11V, and

particular care has been devoted to keep the junction temperature of the devices lower than 160°C.

Table 1: DPA requirements.

Feature	Symbol	Unit	Value
Bandwidth	BW	GHz	17.3-20.3
Small signal Gain	G	dB	>20
Sat. Output power	Psat	dBm	>38
Return Loss	RL	dB	>15
Power Added Efficiency @ 6dB OBO	PAE	%	>30
Junction temperature	Tj	°C	<160
Backside temperature	T_{BP}	°C	75

The overall periphery in the final stage was implemented by using four devices with 8x100um geometry each. In this respect, two possible solutions can be implemented, as graphically shown in Fig. 2. The first one is to use a parallel configuration in which the FETs are traditionally contacted to sum their current. In the second case, the FETs are stacked one over the other, resulting in a series connection, i.e., same drain current but double overall bias voltage. The latter has remarkable advantages with respect to the former. Indeed, a stacked-FET solution allows to quadruple the optimum impedance as compared to the parallel solution, since it allows a double voltage swing and half current swing. Consequently, this significantly simplifies the design of the output combiner of the DPA since the impedance transformation ratio from the output termination (50Ω) to the optimum load of the Carrier and Peaking devices resulted to be four times lower than that required in the parallel configuration. Consequently, this brings to a relevant advantage in terms of achievable bandwidth.

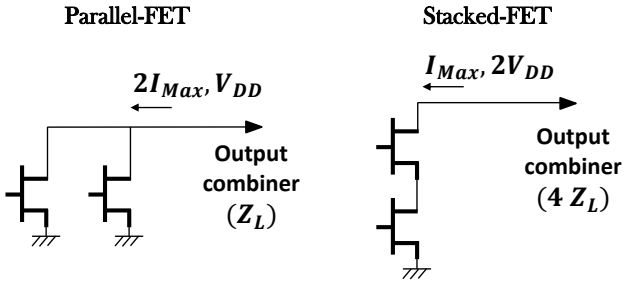

Fig. 2. Parallel and Stacked FETs connections.

III. Implementation of the Stacked-cell

As mentioned above, the basic stacked-FET employs a common source (CS) device loaded by a common gate (CG) one. A resistive-capacitive network is also employed on the gate of the CG transistor to assure the stability of the overall cell and to optimize its power performance. Both, stability and nonlinear features are also heavily affected by the way in which the two active devices are interconnected each other. In this respect, Fig. 3 shows three possible approaches. The first two topologies [7][8] are the most commonly adopted, in which the drain terminal of a CS FET is connected to the source terminal of a CG FET by using either an ad-hoc fork structure or a wide transmission line. However, both solutions show some drawbacks that significantly affect the exploitation of the theoretical advantages of a stacked cell with respect to a parallel FETs combination, in a real MMIC implementation. Indeed, in the first topology, the fork structure introduces a relevant resistive-inductive parasitic, that prevents the realization of a broadband DPA, especially at mm-wave. In the second topology, this is partially mitigated by using a wide transmission line to connect the two devices. On the other hand, this introduces an asymmetry among the fingers of the CG device that has a growing negative impact on the achievable performance as the frequency and the number of fingers increase. The third topology allows to alleviate such issues thanks to the splitting of the common source device (8x100µm) in two smaller devices (4x100µm), which can be easily connected with the source terminals of the common gate device. In this way, the final cell resulted to be more compact, symmetric and with almost negligible parasitic introduced by the connection. Moreover, smaller devices are characterized by higher gain and power density, which can boost up the performance of the overall stacked cell.

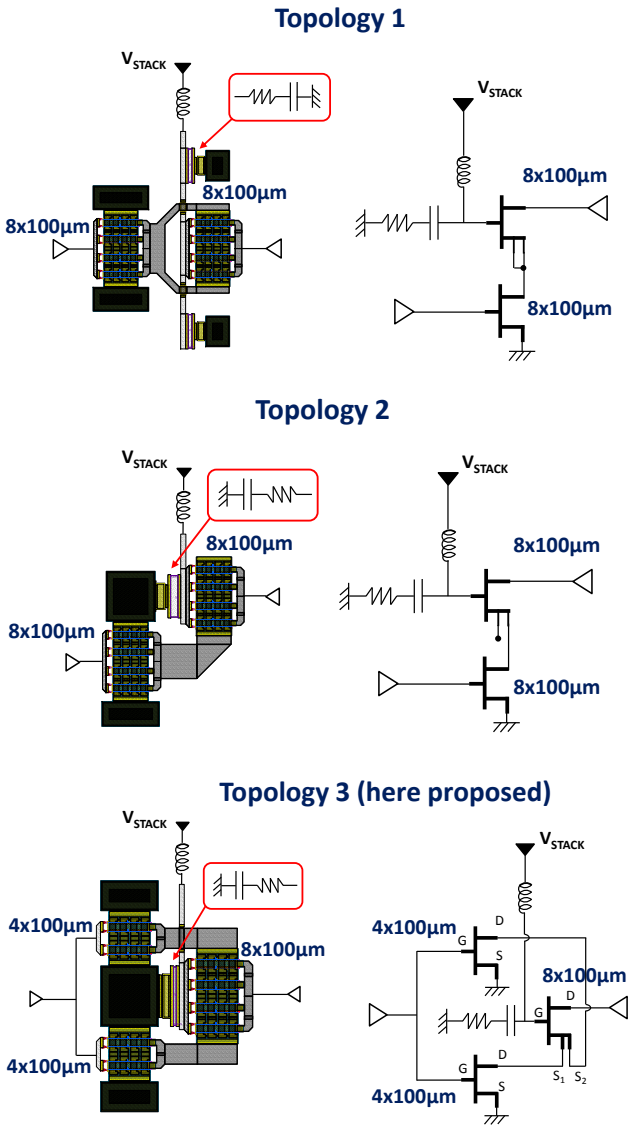

Fig. 3. Possible topologies for implementing a Stacked-cell.

The stacked-cells described above have been made unconditionally stable through the optimization of the values of the passive components, and some harmonic balance simulations have been carried out in order to evaluate the achievable nonlinear performances in a DPA implementation. In particular, for all the topologies, the gate bias of the CS

devices has been fixed to V_{GG}=-1.55V for the carrier cell (class AB), whereas a V_{GG}=-4.5V has been selected for the peaking one (class C). Similarly, a V_{STACK}=8.8V and a V_{DD}=22V have been used to bias the CG transistor. Fig.4 compares the output power as a function of the input power at the center frequency (18.8 GHz) under the same loading condition, for both the Carrier and Peaking cells. Notably, the third topology provides significant advantages with respect to the other two, being able to achieve an output power of about 1dB higher than the other.

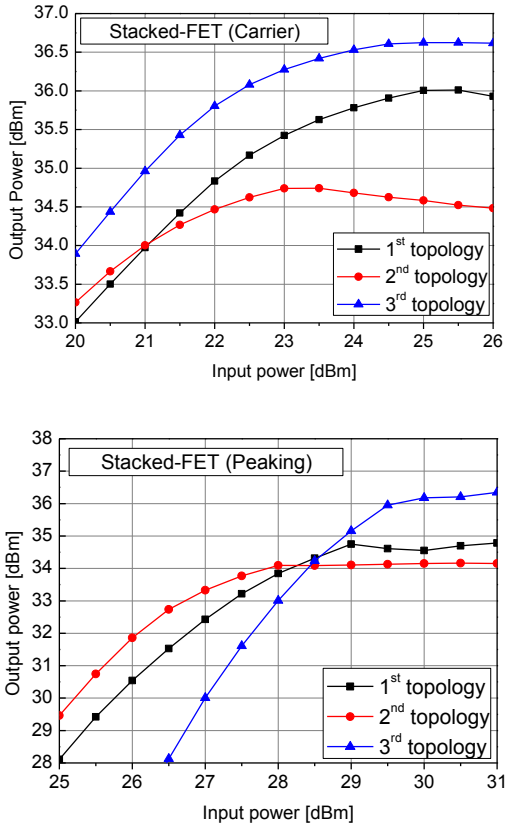

Fig. 4. Output power as a function of the input power of the carrier (top) and of the peaking (bottom) stacked-cell topologies.

Additionally, the proposed stacked-cell supplies a gain boost effect on the carrier branch for all the power range, reducing the gain penalty usually experience when a DPA architecture is compared with a more traditional balanced PA. On the other hand, the Peaking stacked-cell shows a lower gain for low input power, whereas this trend becomes opposite for high input power. Also, this aspect easies the DPA implementation, since it allows to have a sharp turning on of the Peaking cell. Indeed, such device has to draw off minimal input power before the break point (i.e., typically up to 6-7dB of output power back-off) to prevent a negative impact on the first peak of the efficiency, whereas it has to show a sudden gain increase after its turning point in order to correctly modulate the impedance seen by the Carrier cell.

IV. DPA DESIGN

The designed DPA is a two-stage architecture implemented on the 100nm gate length GaN-on-Si process available at OMMIC foundry. The schematic of the realized circuit is shown in Fig.5. The final stage is based on the innovative stacked-cell presented above in both, Carrier and Peaking branches. Each one consists of two 4x100µm FETs in CS configuration and one 8x100µm CG device. The cell stability was ensured by optimizing the RC-series network on the gate of CG devices, and through an appropriate choice of the RC-elements in the stability network connected in series to the gate of the common source devices.

The output combiner was implemented by using the network proposed in [9], based on three lambda-quarter transmission lines (TL) at center frequency. Referring to Fig.5, the first TL with Z1 characteristic impedance works as impedance inverter for the Carrier cell, whereas the other two forms an equivalent half lambda TL in front of the Peaking cell. As described in [9], through a careful selection of the characteristic impedances Z1, Z2 and Z3, it is possible to simultaneously achieve a wideband behavior while matching directly to the 50Ω standard termination, thus avoiding additional impedance matching networks. Finally, the drain bias voltage is applied through the two short circuit stubs, also used to neutralize the output parasitic, mainly the drain to source capacitance of the CG devices.

The driver stage in the Carrier branch was implemented with a 2x75µm FET, whereas a 4x100µm was used in the Peaking branch. The latter is slightly larger than the former to account for the higher input power required by the final stage biased in class C. Also, the driver devices were made unconditional stable by adopting a resistive network in series to the gate. The inter-stage matching networks were designed to transform the input loads of the two 4x100µm FETs of the Stacked-cells in the optimum output load of the driver stages, minimizing the insertion loss and allowing the biasing of the devices.

Finally, the input splitter was realized. It was designed to match the inputs of the two drivers to 50Ω, while recovering and assuring the right phase shift and power splitting ration ($K=P_{IN,peak}/P_{IN,carr}=3$) between the two branches, respectively.

Lastly, the internal stability was checked under small- and large-signal regime by implementing the Ohtomo test [10] and Stan tool algorithm [11], respectively. No issues have been detected.

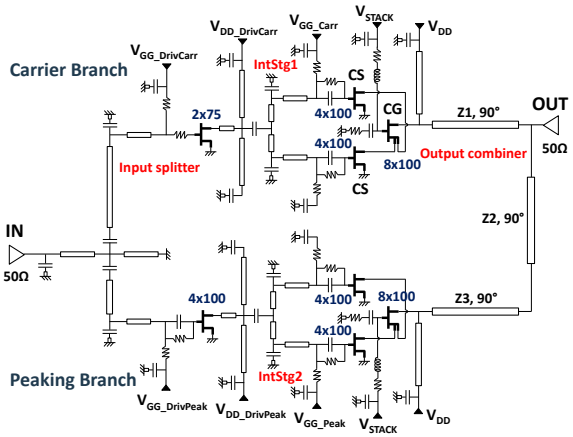

Fig. 5. DPA schematic.

V. DPA PERFORMANCE

Fig. 6 reports the final layout of the DPA at the end of the design phase. In the same figure is also highlighted the LC-block introduced to mitigate the parasitic of the gate to source

capacitance of the common source device, in order to further improve the performance of the Stacked- cell [12].

Small signal parameters are reported in Fig.7 showing an input and output return loss of about 15dB and 7dB, respectively.

Finally, Fig.8 shows the expected nonlinear performances of the designed DPA at the band edges, i.e., 17.3GHz and 20.3GHz, and at center frequency, i.e., 18.8GHz. As can be noted, the typical Doherty behavior is obtained in around 6dB of output power back-off. At saturation, the peak power is of 38.4dBm with a power added efficiency and a gain higher than 30% and 18dB, respectively.

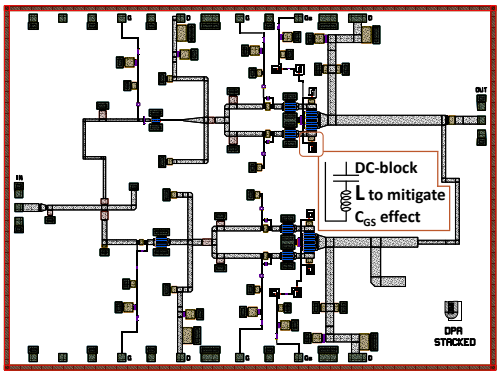

Fig. 6. Circuit layout. The chip area is 5.0 x 3.7 mm^2.

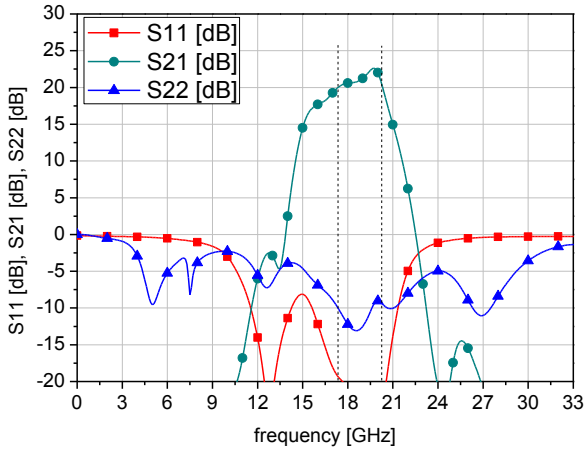

Fig. 7. S parameters.

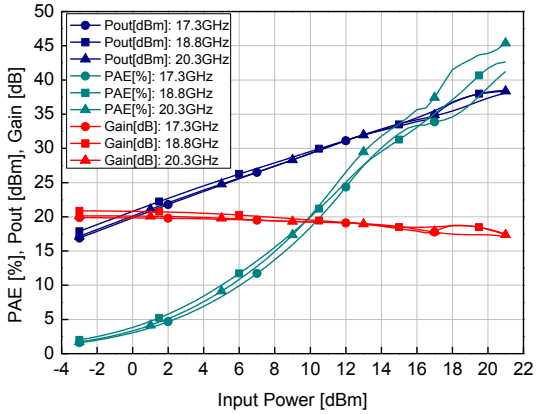

Fig. 8. DPA performance at 17.3 GHz, 18.8 GHz and 20.3 GHz.

VI. Conclusion

In this paper, an innovative stacked-cell configuration has been presented and compared with traditional solutions, demonstrating significant advantages in terms of both, gain and power features. The novel stacked-cell was adopted to design a Ka-band DPA for Ka-band satellite systems, from 17.3GHz to 20.3GHz. The nonlinear simulation results of the DPA have shown more than 40% an 30% of peak and 6dB back-off efficiencies all over the bandwidth, with a saturated output power and a gain of 38dBm and 18dB, respectively.

ACKNOWLEDGED

This research work was supported by European Space Agency (Single-chip Ka-band Doherty Amplifier n. 4000123873/18/NL/HK).

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