Depleted MAPS on a 110 nm CMOS CIS Technology

Depleted MAPS on a 110 nm CMOS CIS Technology

Raffaele Aaron Giampaolo
Politecnico di Torino
INFN Torino
Torino, Italy
raffaele.giampaolo@polito.it

Andrea Di Salvo
Politecnico di Torino
INFN Torino
Torino, Italy
andrea_disalvo@polito.it

Lucio Pancheri
Università di Trento
TIFPA
Trento, Italy
lucio.pancheri@unitn.it

Tommaso Croci
INFN Perugia
Perugia, Italy
tommaso.croci@pg.infn.it

Jonhatan Olave
INFN Torino
Torino, Italy
olave@to.infn.it

Angelo Rivetti
INFN Torino
Torino, Italy
rivetti@to.infn.it

Manuel Da Rocha Rolo
INFN Torino
Torino, Italy
darochar@to.infn.it

Serena Mattiazzo
Università di Padova
INFN Padova
Padova, Italy
serena.mattiazzo@pd.infn.it

Piero Giubilato
Università di Padova
INFN Padova
Padova, Italy
piero.giubilato@unipd.it

***Abstract*—A high-voltage monolithic active pixel sensor, designed to be compatible with standard deep sub-micron CMOS production lines, is described. The device can support a reverse bias voltage of -180 V and combines small collection electrodes with full wafer depletion, demonstrated up to a thickness of 300 μm. Test structures consisting of matrices with an area of 2 mm $\times$ 2 mm embedding 576 pixels with 50 μm pitch have been fabricated in a 110 nm CMOS process. The sensor concept is discussed and experimental measurements obtained on first prototypes are presented.**

***Index Terms*—Monolithic integrated circuits, sensors, Active Pixel Sensors, CMOS integrated circuits, CMOS technology**

I. Introduction

There is a growing interest in using Fully Depleted Monolithic Active Pixel Sensors (FD-MAPS) as radiation imagers for both charged particles and X-rays. Solutions based on highly scaled technologies would allow a highly spatial resolution, with a pixel pitch in the order of 20 μm, and a sensor capacitance of a few fF, needed for low-noise readout. In addition, the adoption of an advanced CMOS process node enables the integration of an event-driven readout circuitry with a power consumption in the order of tens of mW/cm^2, thus greatly simplifying the thermal management of the sensor.

In FD-MAPS, the wafer substrate is depleted and acts as the sensitive volume. The signal charge generated by the impinging particles is collected primarily by drift, which improves the sensor radiation hardness. Highly energetic charged particles cross the full detecting volume, leaving an almost uniform ionization track along their path. In this case, the Signal-to-Noise Ratio (SNR) can be significantly enhanced as the signal amplitude is proportional to the active device thickness. On the other hand, a larger sensitive volume improves the detection efficiency for X-rays.

Several approaches for the implementation of FD-MAPS have been proposed. The first FD-MAPS achieving a full wafer depletion of 300 μm were developed at Stanford [1]. The adopted solution allowed to collect the signal charge on a small electrode, which led to very good SNR because of the resulting small capacitance. PMOS-only readout circuitry could be implemented in the sensitive area, while full CMOS electronics was possible in the periphery. In High Voltage CMOS (HV-CMOS) [2] a large n-well collection electrode is employed. The very front-end electronics is incorporated in the sensing electrode itself. The use of large collection electrodes favors a uniform electric field inside the sensor, but leads to a larger capacitance, thereby affecting SNR and power consumption. Embedding the front-end electronics inside the collection electrode further exacerbates this issue. In the Silicon-on-Insulator (SOI) approach, the epitaxial layer, necessary for CMOS implantations, is physically separated by the lightly doped sensor substrate via the buried oxides (BOX). This concept implies a process customization to properly address and overcome the coupling between the high-voltage bias and the electronics, (back-gate effects) and to improve total ionizing dose (TID) resistance [3]. An interesting modification to a standard CMOS Image Sensors (CIS) process that combines full depletion and small collection electrodes has recently been proposed in the framework of the R&D for the ALICE ITS upgrade [4]. In this case, the full depletion is limited to the epitaxial layer.

In this paper we describe FD-MAPS that address the main issues affecting the aforementioned technologies. The depletion extends to the full wafer thickness, the collection electrode in small and full CMOS electronics can be embedded in pixel. These results are achieved through use of suitable starting wafers and simple patterned back-side which is compatible with a standard CMOS production line. The sensors were implemented in a 110 nm CIS process provided by LFoundry in Avezzano, Italy.

II. Prototype Description

The main prototype is a pixel matrix with an area of $2\,\mathrm{mm} \times 2\,\mathrm{mm}$. The matrix contains an array of 24×24 pixels with 50 μm pitch. Additional test structures such a simple diodes with different guard-ring design and small pixel arrays deprived of the front-end electronics are also provided for detail characterization of the process.

A. Sensor Concept

A simplified cross-section of the sensor is shown in Fig. 1. An n-type high resistivity wafer is used as the main substrate. The collection electrodes are provided by small n-well implants. A deep pwell hosts the CMOS readout electronics and isolates it from the sensor high-voltage. In the top-side of the wafer a more doped n-type epitaxial layer is used as a buffer between the depleted substrate and the pwells in order to increase the punch-through voltage. N-well guard rings (GR) have been designed on the top perimeter of the matrix to isolate the pixels from parasitic edge currents. At the bottom, a p+ junction is implanted in order to deplete the sensor and a series of p-doped GRs are implemented. GRs have been included to avoid premature edge breakdown at the sensor edges and to protect the pixels from possible spikes in the high-voltage biasing modules. The depletion layer starts to grow from the bottom to the top when a negative reverse bias is applied. Thus, only when full depletion is achieved are the pixels isolated from each other and signals can be observed.

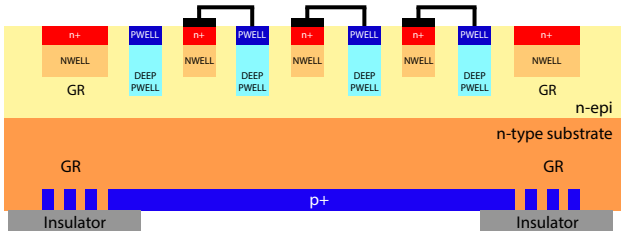

Fig. 1. Section illustration of the the depleted MAPS electrode-to-FE connection and substrate. Each collection electrode is connected to it's neighboring pixel front-end contained in the p-well implantation.

B. Read-Out Electronics

The in-pixel analog readout chain is depicted in Fig. 2, [5].

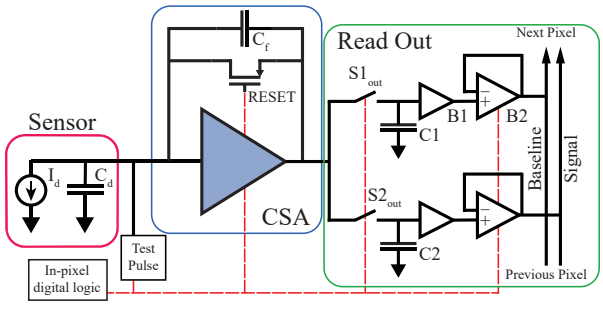

Fig. 2. Read-Out block scheme.

In order to amplify the signal collected by the n-well sensing electrode and maximize the SNR, a charge sensitive amplifier (CSA) is adopted. The CSA schematic is reported in figure 3a. The circuit is based on a telescopic cascode configuration with a feedback capacitor, C_f, depicted in Fig. 3a. The feedback branch includes, in addition, a PMOS transistor in order to reset the CSA output node after each charge integration and stabilize the DC operation points of the pre-amplifier. To decrease the charge injection on both input and output nodes and the occupied area on pixel, a minimum size transistor has been used.

Current and aspect ratios of the input and biasing cascode transistors, respectively M1 and M4, have been chosen in order to fix the input and, in turn, the n-well electrode voltage around 0.8 V. The value sets the operation point of the front-end and it has been chosen on the basis of a compromise between the maximization of the detector's working region, the power supply limit imposed by the technology (1.2 V) and the threshold voltage of the input transistor. The collection electrode must be biased to a voltage of at least 0.6 V to achieve a satisfactory punch-through voltage [6].

In order to initialize the circuit and increase the front-end dynamic range, the baseline voltage can be regulated externally through the circuit represented in figure 3b. This circuit uses CMOS switches connected between the regulation voltage, V_{REG}, and ground, gnd, to inject a fixed charge on the feedback capacitor changing the output voltage to the desired baseline, V_{bsl}. In a similar manner, current pulses can be generated closing the switches connecting the test pulse voltage, V_{TP}, to gnd in order to test the device linearity. The front-end works thus as follows. First, switch M6 is closed to reset the preamplifier and to allow self-biasing of the input node. After M6 is opened, a fixed-voltage is injected to lower the baseline. The swing at the preamplifier output is expected to be positive, which calls for a baseline as close as possible to ground to achieve a satisfactory dynamic range. After the baseline is settled, its value is sampled on capacitor C_1 (see Fig. 2). A global shutter signal allows to sample the preamplifier output after a given time which is programmed in the Data Acquisition System. The two samples are then serially shifted-out and digitized by an external 12-bit ADC.

In the read-out of MAPS it is common to use simple source followers to buffer the pixel output. This approach was not suitable in our case as only low-leakage transistors with a threshold voltage of about 0.4 V could be used in the prototype. In order to maximize the dynamic range, a different buffering scheme was thus deployed. The buffer is based on the switched current mirror Operational Trans-conductance Amplifier (OTA) depicted in Fig. 4. The circuit allows to drive directly the analogue signals off-chip. When the pixel is not addressed for readout, switches S1, S2 and S4 are closed while S5 is opened. This cuts the current to the OTA and sets its output in high impedance state, which allows to share the output line among the pixels. The OTA allows a readout frequency of at least 5 MHz with an output load of 10 pF.

In addition to the main OTA, indicated as B_2 in Fig. 2 a low

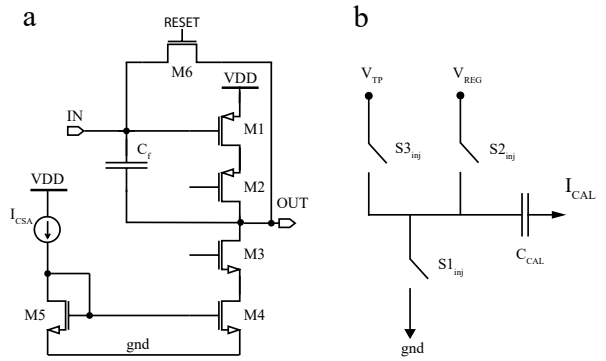

Fig. 3. *a* Transistor level of the CSA front-end *b* Pulse injection and baseline regulation circuit scheme.

power op-amp (B_1 in the same figure) has been used to continuously buffer the voltage stored in the sampling capacitors and protect the information from the spikes generated during the activation of the main buffer.

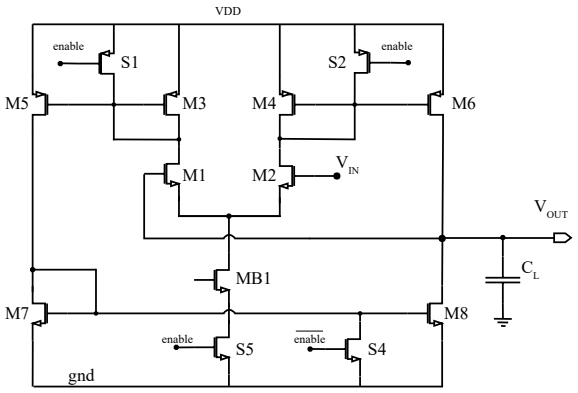

Fig. 4. Switched current mirror OTA schematic.

III. Experimental Results

A series of characterization tests have been performed to verify the properties of the sensor and the functionality of its front-end electronics. The ASIC has been bonded to a mezzanine and successively connected to a customized PCB that serves as the interface with the DAQ system.

A. Linearity and Dynamic Range

Using the test pulse calibration circuit in figure 3b, the linear response and output dynamic range can be tested. The largest pulse that can be generated on chip corresponds to an input charge of 2.4 fC. In the test, the baseline is set to $V_{bsl} = 400$ mV, which allows to keep in saturation, with a reasonable margin, the cascode current source that provides the preamplifier active load. A back-side bias voltage of -160 V is applied, which allows full depletion of the sensor. Figure 5 shows the voltage amplitude as a function of the input charge which follows a linear trend with a 1% deviation. The measured analog gain is $G_{exp} \approx 116$ mV/fC, should be compared with the schematic and post-layout simulations, respectively $G_{sch.} \approx 150$ mV/fC and $G_{p.l.} \approx 131$ mV/fC. This difference is due to parasitics in the feedback capacitance which reduce the pre-amplifier closed-loop gain.

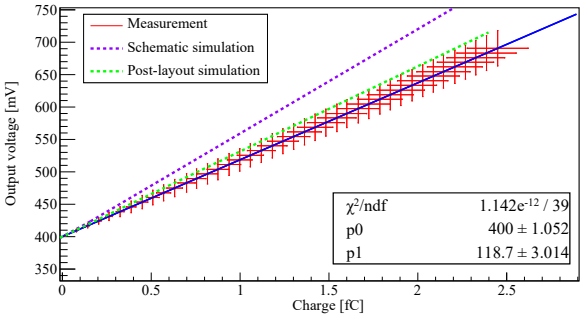

Fig. 5. The output voltage generated for different injected charges

B. I-V curves characterization

The I-V characterization of the sensor has been carried out connecting the test matrix to a KEYSIGHT B1505A power device analyzer. The guard rings, p-wells and the collecting electrodes have been biased to respectively $V_{GR} = 1.2$ V, $V_p = 0$ V and $V_{PIX} = 1.2$ V. The backside voltage has been varied measuring the currents passing through the GRs, the pixels and the backside.

Analyzing the resulting I-V curves in figure 6, three regions are identifiable. The first is the one in which the sensor back-bias voltage is increased from 0 to 150 V. In this region the pixel current is dominated by surface currents due to free charges that provide resistive paths between the GRs and the pixels. In the second region, where the sensor is fully depleted, the pixel current drops below the sensitivity of the instrument (1 nA). In the third region the sensor reaches the punch-through voltage and the p-well starts conducting current. This region is identifiable by the increase of the I_{HV} and the plateau of the I_{GR}.

Clearly, the second region from $V_{HV} \approx -140$ V to $V_{HV} \approx -250$ V is the appropriate operating region for the detector. Adopting a higher voltage is of great interest because a higher electric field implies faster carrier collection. The effect of full depletion is showed by the map acquired in figure 7. The expected shape of the depleted zone is sketched in the upper part of the figure. The depletion starts from the bottom and reaches first the pixels in the central part of the matrix. When the depletion is not yet complete, pixels in the matrix periphery are still interconnected with a moderate resistive path and the resulting currents quickly discharge the preamplifier feed-back capacitor. When the depletion is complete, all pixels are fully isolated from each other and a uniform and stable baseline can be maintained as long as permitted by the off leakage current of the analogue switches.

C. C-V curves characterization

The depletion region investigation was further carried out studying the C-V curve. The analyzer has been set with

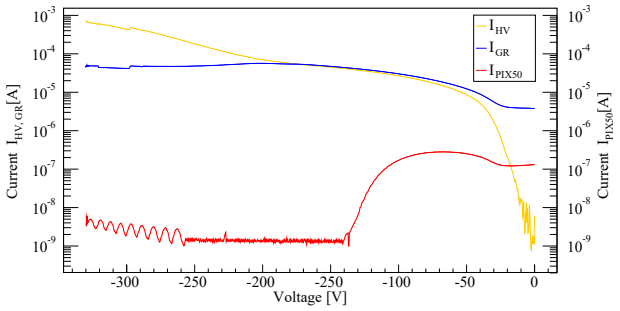

Fig. 6. The plot shows the high voltage current (I_{HV}) passing through the backplane of the sensor, the guard ring current (I_{GR}) and the $50\,\mu m$ pixel matrix leakage current (I_{PIX50}).

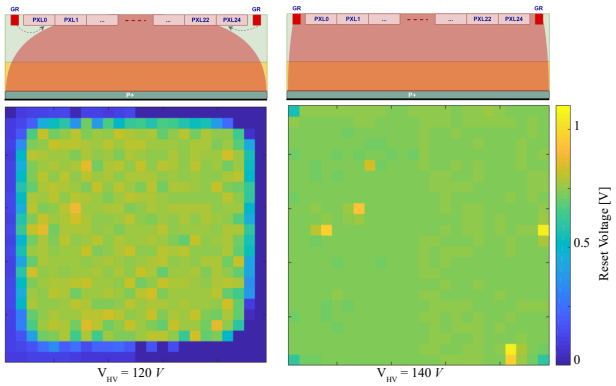

Fig. 7. Comparison between un-depleted and fully depleted sensor in a readout map.

a parallel capacitance model measurement working with a 10 kHz frequency and a 1 V voltage step. The capacitance assumes its maximum value (22 pF) at the starting point (0 V). As expected, this value sharply decreases at the beginning and it achieves the minimum capacitance (˜1 pF) around -140 V.

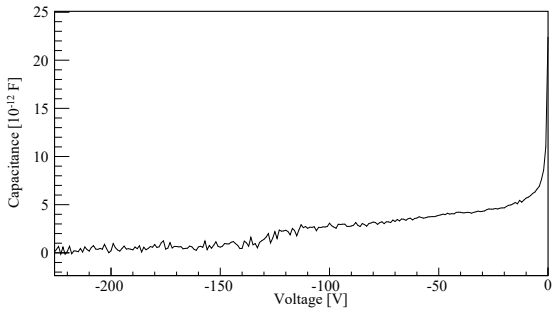

Fig. 8. C-V trend of 50 µm pixel pitch. The noise at low voltages is due to the high voltage module's low sensitivity at low voltages.

IV. Conclusions

In this paper the design and test results of a 300 µm fully depleted CMOS sensor have been presented. The solution presented in this work combines the best features from the different approaches currently employed in the fabrication of MAPS [2]–[4]: a fully-depleted substrate, as thick as a few 100s µm, and a low electrode capacitance, which imply a high SNR and a low charge collection time. Furthermore, radiation hardness is potentially improved by adopting a scaled CMOS technology node and avoiding the use of buried oxide layers. These features make the proposed technology a competitive platform for the implementation of future tracking detectors and radiation imagers. The device combines a quadruple well commercial CMOS CIS process with a back-side patterned implantation. Full depletion over a thickness of 300 µm is achieved with a backside bias voltage of -140 V. The collection electrode is provided by a small n-well implant, with an estimated capacitance of 20 fF. Pixels with a pitch of 50 µm have been implemented in the prototype. About 80% of the pixel remains available for the implementation of fully CMOS signal processing electronics. Future planned activities include beam and infra-pixel LASER tests and charge time collection measurements.

V. Acknowledgements

We would like to thank M. Ferrero and F. Siviero for the help with the laboratory equipment and B. Pini and F. Dumitrache for the wire bondings.

References

[1] W. Snoeys, J. D. Plummer, S. Parker and C. Kenney, "PIN detector arrays and integrated readout circuitry on high-resistivity float-zone silicon," in IEEE Trans. on Electron Devices, vol. 41, no. 6, pp. 903-912, June 1994. doi: 10.1109/16.293300

[2] Ivan Peric, "A novel monolithic pixelated particle detector implemented in high-voltage CMOS technology", Nucl. Instr. Methods A. vol. 582, pp. 876885, 2007

[3] W. Kucewicz et al., "Fully depleted monolithic active pixel sensor in SOI technology," IEEE Nuclear Science Symposium Conference Records Rome, 2004, pp. 1227-1230 Vol. 2. doi: 10.1109/NSSMIC.2004.1462423

[4] W. Snoeys et al., "A process modification for CMOS monolithic active pixel sensors for enhanced depletion, timing performance and radiation tolerance", Nucl. Instr. Methods A, vol 871, pp. 90-96, 2017.

[5] Elias Jonhatan Olave, S. Panati, F. Cossio, A. Rivetti, M. Da Rocha Rolo, N. Demaria, L. Pancheri, S. Mattiazzo, P. Giubilato, D. Pantano, "MATISSE: A Low power front-end electronics for MAPS characterization", Topical Workshop on Electronics for Particle Physics, 11-14 September 2017, Santa Cruz, California.

[6] L. Pancheri, J. Olave, S. Panati, A. Rivetti, F. Cossio, M. Rolo, N. Demaria, P. Giubilato, D. Pantano, S. Mattiazzo, "A 110nm CMOS process for fully-depleted pixel sensors", Journal of Instrumentation Vol. 14, No. 06, pp. C06016, 2019.

[7] S. Panati; J. Olave; et all. Flexible readout electronics for monolithic active pixel sensors characterization. IEEE Nuclear Science Symposium Conference Records, 2017.

[8] Lars Evensen, Anders Hanneborg, Berit Sundby Avset and Martin Nese, "Guard ring design for high voltage operation of silicon detectors", Nucl. Instr. and Methods A: vol 337, pp. 44-52, 1993.

[9] V. Mishra, V.B. Chandratre, M.Y. Dixit, V.D. Shrivastava, A. Topkar, S.K. Kataria, Y.P. Prabhakar Rao, N.P. Shankarnarayana, "Studies on reducing leakage current and improving breakdown voltage of large-area silicon detectors: technology and results" Nucl. Instr. Methods A, vol. 527, pp. 308-318, 2004.

[10] G. F. Dalla Betta, N. Ayllon, M. Boscardin, M. Hoeferkamp, S. Mattiazzo, H. McDuff, R. Mendicino, M. Povoli, S. Seidel, D.M.S. Sultan, and N. Zorzi, "Investigation of leakage current and breakdown voltage in irradiated double-sided 3D silicon sensors", Journal of Instrumentation, Volume 11, September 2016.