Front-End Integrated Circuits For Readout of Large Area SiPMs at cryogenic temperature

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***Abstract*—This work describes the architecture and transistor-level design of CMOS front-end amplifiers for the readout of large area SiPMs at LAr temperature (87K). Two circuit topologies, based on trans-impedance and common-gate input stages, are discussed and compared. Both circuits were designed using a standard CMOS 110nm technology, and the simulation results obtained with the foundry PDK are presented. The circuits use a power rail of +1.25 V and -1.25 V, and a power budget below 100 mW, for a total gain of 58 dB. The target sensor is a $24cm^2$ SiPM tile developed in the framework of the Darkside Collaboration. Post-layout simulations with a cryogenic SiPM electrical model indicate that a signal-to-noise ratio above 8 and a jitter better than 15 ns should be achieved for a single photoelectron.**

***Index Terms*—Photomultipliers, Hot carriers, Cryogenic electronics, Operational amplifiers**

I. Introduction

Liquid argon (LAr) time projection chamber (TPC) technology will be used on future experiments for neutrino and direct dark matter detection [1] [2]. The high photodetection efficiency, robustness and the low cost of state-of-the-art silicon photomultipliers (SiPMs) has created wide interest on the possibility to use these sensors for the instrumentation of such frontier detectors. Extensive R&D on the cryogenic performance of silicon sensors allowed for the development of near ultra-violet SiPM technology optimised for operation at LAr temperature [3]. While typical SiPM sizes are below 10 mm2, LAr TPC detectors use large areas of SiPMs connected together in an effort to minimise the total number of readout channels. This constraint is imposed not only by the number of feedthroughs from the cryostat, but because the requirement for low radioactive background in experiments looking for rare events imply the minimisation of the total mass of photodetectors, associated electronics and cabling.

This work, developed in the framework of the Darkside Collaboration [4], describes the design of two alternative front-end amplifier topologies for the readout of large areas of SiPMs at LAr boiling temperature (87 K) using a standard CMOS 110nm technology. The target sensor is a 24 cm^2 SiPM tile developed for the Darkside-20K TPC photodetector module. A 2-series 3-parallel grouping configuration is used to decrease the total sensor capacitance, estimated 7 nF/cm^2, and thereby the tile is divided into 4 quadrants of 6 cm^2 each, for a capacitance of 10 nF per quadrant. The proposed amplifiers read independently each one of the 4 SiPM channels and sum together the total signal, providing a single-ended output voltage signal for digitisation with warm electronics.

A first design uses a trans-impedance configuration based on the work proposed in [5]. The input stage is based on a folded-cascode amplifier [6], providing a large gain and dynamic range with a large unity-gain frequency [7]. The second stage is configured as a voltage amplifier, and sums the signal from the 4 input branches.

A second design, based on a regulated common-gate configuration, uses the input stage as a current conveyor in order to decouple the effect of the large detector capacitance from the transfer function [8] [9]. A second stage, based on a folded-cascode amplifier, amplifies and sums the signal from the 4 branches.

A Spice model was developed, based on extracted characterisation parameters, for simulations at 300K and 77K [13]. The electrical characterisation of the CMOS prototypes will be performed at 77K using Liquid Nitrogen.

II. Design and Implementation

This paper describes the transistor-level design and simulations for both the Trans-impedance input stage amplifier (TIA) and that based on a regulated common-gate input stage (RCG).

A. TIA amplifier

The transistor-level design of the folded-cascode operational amplifier is shown in Fig. 1. The circuit uses a PMOS input stage with an NMOS cascode, a typical choice for the minimisation of the flicker noise [12]. The input transistors (M1, M2) operate in weak inversion (Eq. (1)) and with a transconductance of 80 mS, using a bias current below 1 mA.

$$\left.\frac{W}{L} = \frac{Id}{2n * Cox * \mu c * \Phi t^2 * e^{\frac{Vgs-Vth}{n*\Phi t}}}\right\} \quad \text{Weak Inversion} \tag{1}$$

The circuit uses a class AB amplifier circuit on the output of cascode stage, which provides an increment in the total gain (¿ 40dB). Additionally, a Miller compensation capacitor is used in order to avoid instability related to the second pole and right-hand zero (RHZ). The Miller capacitors (C_m) together

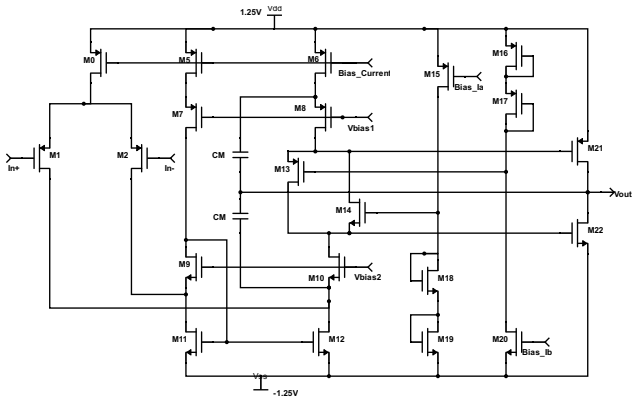

Fig. 1. Transistor-level circuit of Folded Cascode.

with the trans-conductance of M21 and M22 compose the new second pole, which keeps the circuit in a stable area, consequently limiting the total bandwidth.

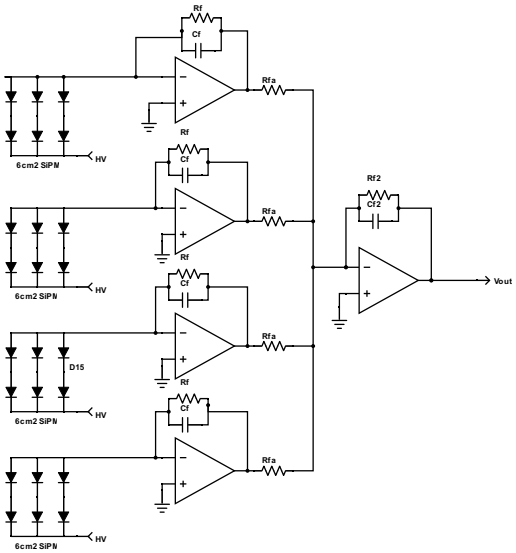

Fig. 2. Folded Cascode Front-End for readout of large area sensor (i.e $24cm^2$ SiPM.

In order to minimise the effect of hot carriers, which would otherwise have an impact on the reliability of the device, we choose to use a minimum channel length of 4 times the minimum length (110nm). This technique reduces the internal electric field of the MOSFET and increases the transistor lifetime [11].

B. RGC

The use of a common-gate input allows to use an input resistance that is inversely proportional to the trans-conductance of M1. The use of a local feedback further reduces the input impedance by a factor of A. Figure 3 illustrates the transistor-level design of a regulated common-gate (or regulated gate cascode) circuit using a cascoded common-source amplifier, a technique that is often called g_m-boosting.

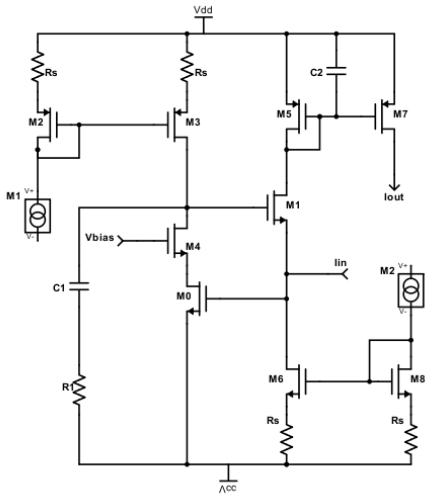

Fig. 3. Transistor-level circuit of Regulated Common Gate(RCG).

In this configuration, the main contributor to the total output noise voltage of the circuit is the common-source amplifier NMOS M0. The transistor M4, in series with M0, reduces the drain-source voltage of M0 for an increased lifetime of the device at cryogenic operation. Therefore, this transistor was designed with a large aspect-ratio (20mm/800nm) increase its trans-conductance to 120 mS, which minimises its thermal noise.

The four RCG input stages are connected to the adder circuit, as shown in Fig. 4.

III. Simulation results

The designs were simulated using standard Spice models provided by the foundry PDK (Process Design Kit). The mathematical extrapolation of the BSIM models allows to have an approximate response of the MOSFET at cryogenic temperature, since semiconductor foundries do not provide characterisation qualified models for temperature corners below -40 C. To perform the simulations, a $1cm^2$ SiPM electrical model with an output capacitance around 7 nF and a quenching resistance of 6MΩ at 77K [10] is used, as shown in Fig. 5. The SiPM model is connected in series and parallel to obtain $6cm^2$, as shown in Fig. 4.

The output signal of the TIA circuit for a single photoelectron (PE) impinging the SiPM is shown in Fig. 6.

A summary of electrical simulation of the post-layout netlist for both amplifier topologies is shown in Table I. The comparison is done in terms of trans-impedance gain, total r.m.s. output noise voltage, peaking time, power, signal-to-noise ratio (SNR) and jitter for 1 PE, considering a timing

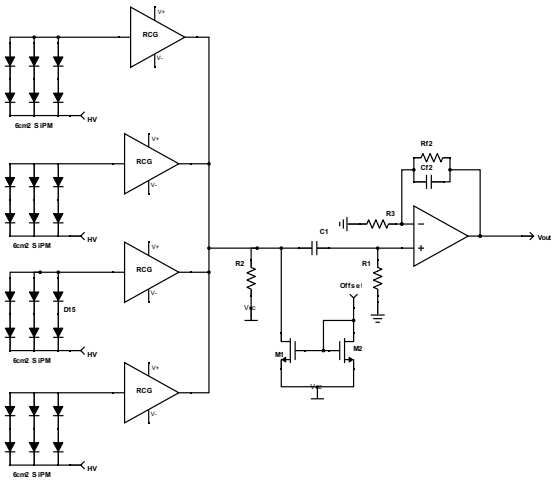

Fig. 4. RCG Front-End for readout of large area sensor (i.e $24cm^2$ SiPM.

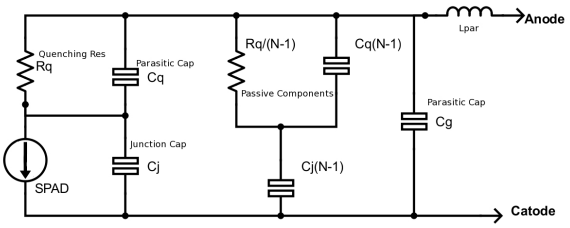

Fig. 5. SiPM electrical model with the interconnection inductance

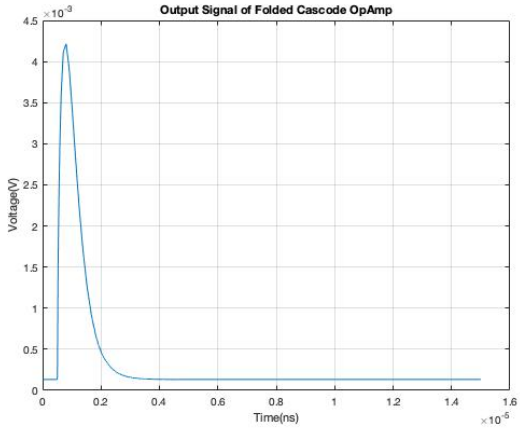

Fig. 6. Output voltage signal of TIA for a single PE.

TABLE I
SIMULATED PARAMETERS OF RCG AND TIA CIRCUITS

Parameters	FE Topology	
	RCG	*TIA*
Gain (dB V/I)	74	58
RMS noise (mV)	2.5	0.5
SNR	10.1	8.8
Jitter (ns)	10.9	7.2
Peaking Time (ns)	700	250
Power (mW)	82	95
Dynamic Range (pe)	40	75

measurement derived from a leading-edge discriminator at the output of the amplifier. The dynamic range, which is a function of the raill-to-rail voltage used (2.5V), is normalised to the signal produced by one photoelectron.

The higher dynamic range of the TIA in respect to the RGC circuit will not be used for comparison, since this is inevitably a function of the total gain. However, the seemingly worst performance of the RGC in terms of noise and, consequently, jitter, are caused by an excessive series resistance of the metal interconnects at the gate of the input transistor and the larger gain which amplifiers the RMS noise from the input. In schematic level simulations, these figures-of-merit are approximately equivalent.

A Montecarlo simulation was performed to estimate the stability of the circuit for stochastic variations of the active and passive devices. Figures 7 and 8 show the behaviour of the timing jitter and SNR at 77K for both circuits. The TIA provides a mean SNR = 8.8 (std. dev. = 0.3) and a mean jitter = 7.2 ns (std. dev. = 530 ps), while the RGC shows a mean SNR = 10.1 (std. dev. = 0.1) and a mean jitter = 10.9 ns (std. dev. = 520 ps).

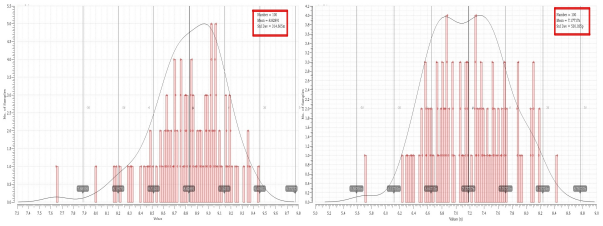

Fig. 7. Montecarlo simulation of TIA, SNR(left) and Jitter(right).

IV. CONCLUSION

We present the design and simulation results of two front-end amplifiers for the readout of large area SiPMs at LAr temperature. Both circuits were designed using a standard CMOS 110nm technology and fit in a test-chip of $\approx 2\ mm^2$. The prototype was sent to fabrication and will be tested with external charge injectors and a 24 cm^2 tile in a liquid nitrogen bath. Post-layout simulation results show that both circuits should achieve a SNR above 8 and a jitter better than 15 ns for the signal produced by a single photo-electron. The design

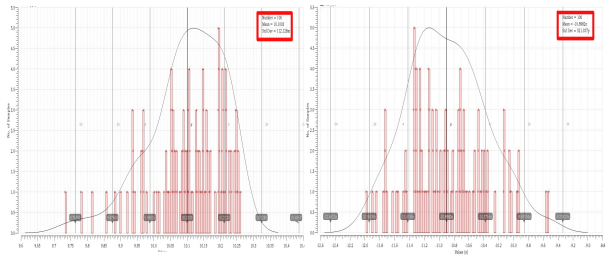

Fig. 8. Montecarlo simulation of RGC, SNR(left) and Jitter(right).

of the RGC circuit, which uses rather large W/L on the input transistor, suffers from a degradation of the noise caused by excessive resistive parasitics at the input net.

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