A Criterion for an Optimal Switching of Power Transistors

A Criterion for an Optimal Switching of Power Transistors

Matteo Vincenzo Quitadamo, Erica Raviola, Franco Fiori
μEMC Group, Electronics and Telecommunication Department
Politecnico of Torino, Italy
{matteo.quitadamo, erica.raviola, franco.fiori}@polito.it

***Abstract*—Power converters, especially those exploiting fast-switching devices, suffer from ringing, which worsens efficiency, EMI performance and increases the stress of components. Traditional approaches, such as RC snubber and series gate resistance, only partially mitigate the problem, whereas, active gate driver implies sub-optimal switching waveforms. This paper presents a new criterion for controlling the turn-on and the turn-off of a power transistor using a three-levels current driver, which results in optimal switching waveforms. The method shows better performance in terms of efficiency and transient slopes compared to traditional approaches.**

***Index Terms*—gate driver, EMI reduction, ringing suppression**

I. Introduction

The increasing use of fast-switching transistors in power applications poses a challenge to designers in terms of suppression of both electromagnetic interference (EMI) and oscillations. When a power switch is turned on or off, parasitic inductances and capacitances in the power loop are excited with high di/dt and dv/dt, thus a continuous exchange of energy among them takes place until the oscillations are naturally damped by the circuit itself. The traditional approach consists of placing an RC snubber in parallel to the power switch to increase the damping factor, however, power dissipated by the snubber may exceed the required one and the values of components may be manually tuned. Active gate driving is a popular solution to address the EMI reduction issue. Such technique mainly deals with the modulation of the driver strength during transients. In particular, gate resistance modulation [1], [2], stair-case shaped gate voltage [5] or current [3], [4] have been exploited to damp oscillations. The key idea underlying all the mentioned works is that the power device has to be slowed down during the Miller's plateau, which results in a limitation of the output current slope, and eventually of the overshoot itself. This work presents a new driving technique to address the oscillation phenomenon on the gate side, introducing a method to evaluate the optimal switching waveforms as a function of parasitics, and driving the power switch by means of a current source with a proper piecewise constant waveform. With respect to previous works, during Miller phase the power transistor is not just slowed down, but charge is extracted from the gate of the switching device. In such way, the transition time is less affected, and power dissipation is minimized.

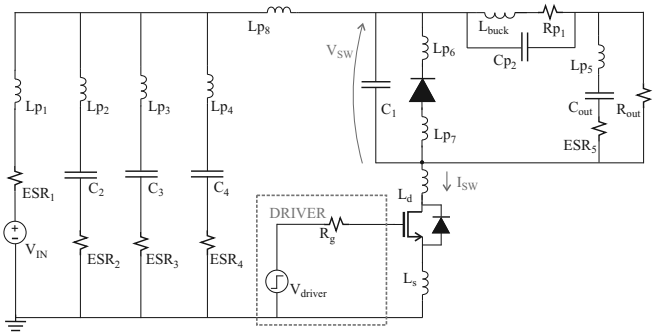

Fig. 1. Buck converter topology circuit including its parasitic elements.

II. Analysis of Oscillations in a Buck Converter

The switching behavior of an asynchronous low side buck converter was analyzed. The circuit, shown in Fig. 1, was simulated *Cadence Virtuoso* environment, including parasitic elements. The first step was to investigate voltage and current transitions to determine which of them causes ringing, with the aim of finding out a simpler equivalent circuit.

The analysis of the switching voltage $\mathrm{V_{sw}}$ and of the switching current $\mathrm{I_{sw}}$ allows one to identify two ringing phenomena, one after the switch turn-on and one after its turn-off, occurring at different frequencies. This means that the parasitic elements excited in such commutations are different. From simulation results of the considered circuit (Fig. 1), $\mathrm{f_{r_1}}$ is approximately equal to $37\,\mathrm{MHz}$, and $\mathrm{f_{r_2}}$ to $27\,\mathrm{MHz}$.

A. Turn-on Analysis

After the closing of the switch, the current $\mathrm{I_{sw}}$ starts to increase and it is only limited by the parasitic inductance Lp_{eq}. In that phase, the voltage $\mathrm{V_{sw}}$ is kept constant by the freewheeling diode and all parasitic capacitances are not subjected to voltage variations, which prevents any oscillation to take place (Fig. 2 on the left side). When the current reaches its nominal value, the high side diode turns-off and the voltage $\mathrm{V_{sw}}$ begins to rise, exciting the resonance (Fig. 2 on the right side). Thus, to damp the turn-on oscillations, it is sufficient to focus on this last voltage transient.

B. Turn-off Analysis

When the driver starts the turn off process, the voltage decreases but the current $\mathrm{I_{sw}}$ continues to flow in the switch

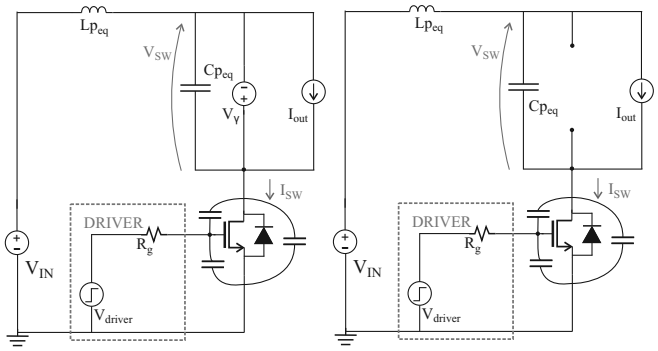

Fig. 2. Equivalent circuits for the current transition (left side) and for the voltage transition (right side) during turn-on and turn-off.

until its command is not under the threshold. During this phase, the current is constant and Lp_{eq} is not subjected to any current variation, so no resonance is excited (Fig. 2 on the right side). When the voltage $\mathrm{V_{sw}}$ has reached the value $-V\,\gamma$, the freewheeling diode turns-on and the current $\mathrm{I_{sw}}$ starts to decrease (Fig. 2 on the left side), exciting the resonant circuit. As a result, to damp such resonance, the turn-off current transient has to be controlled.

III. Preventing the Oscillation

As described in the previous section, only the voltage $\mathrm{V_{sw}}$ transition excites the resonant circuit during the turn-on, resulting in the undesired oscillations. On the other hand, the $\mathrm{I_{sw}}$ current transition, is responsible for ringing during the low side switch turn-off. The key point is that, to prevent oscillations from taking place, it is required to dissipate energy only during the aforementioned transitions. Thus, a resistance and a conductance were inserted in series and in parallel to the low side power switch, respectively. Such elements, $\mathrm{R_t(t)}$ and $\mathrm{G_t(t)}$, dissipate energy only during the resonance exciting transitions, with a time-variant values that depend on the derivative of $\mathrm{V_{sw}}$ (Fig. 3 on the left side) and of $\mathrm{I_{sw}}$ (Fig. 2 on the right side), respectively. In such way only the needed amount of energy is dissipated, without affecting the efficiency. The values of $\mathrm{R_t(t)}$ and $\mathrm{G_t(t)}$ are chosen to follow (1).

$$R_t(t) = k_1 \frac{dV_{sw}}{dt} \qquad G_t(t) = k_2 \frac{dI_{sw}}{dt} \tag{1}$$

The values of coefficients $\mathrm{k_1}$ and $\mathrm{k_2}$ were evaluated performing parametric simulations on their values.

$\mathrm{R_t(t)}$ and $\mathrm{G_t(t)}$ were introduced in the power loop only to obtain the optimal switching waveforms. During the voltage transition of the turn-on phase, the switch should be driven so that the voltage $\mathrm{V_{turn_{on}}}$ (Fig. 3) drops on power transistor. Instead, for the turn off phase, the switch should be driven to limit the current flowing in the parasitic inductance, thus absorbing the excess of current $\mathrm{I_{turn_{off}}}$. The diodes included in the optimal driver circuit are required to clamp the driving voltage to the maximum and minimum desired values.

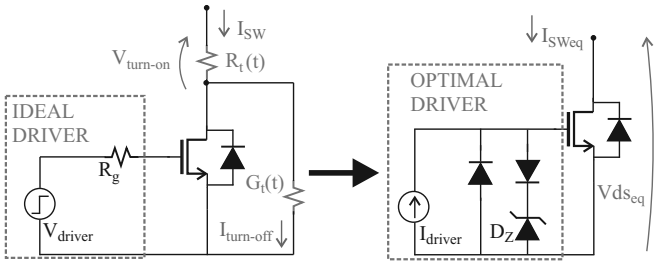

Fig. 3. Equivalent switch circuit with $R_t(t)$ and $G_t(t)$ (left side) and switch with optimal current driver (right side).

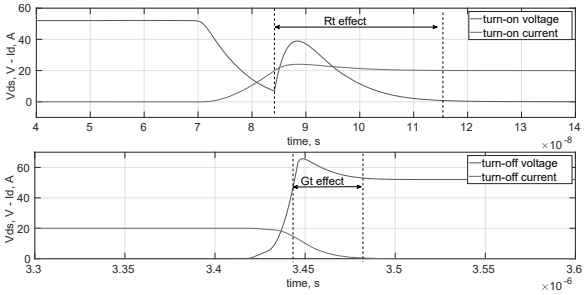

Fig. 4. Voltage and current waveforms that should be reproduced using the switch to obtain the optimal commutation during turn-on and during turn-off.

The optimal transistor waveforms, shown in Fig. 4, can be closely reproduced exploiting a three-level current driver.

1) Turn-on: The three phases for the turn-on (Fig. 5), can be explained as follows:

- The first level consists of the switch turn-on with all the driver available current $\mathrm{I_{A,on}}$. During this phase the switching current $\mathrm{I_{sw}}$ reaches the nominal value and the drop voltage on it starts to decrease from the V_{in} value.
- The level $\mathrm{I_{B,on}}$ should be negative and its goal is to increase the voltage drop on the switch, to reproduce the behavior shown in Fig. 4.
- The level $\mathrm{I_{C,on}}$ leads slowly the switch voltage approximately to $0\,V$ while the switching voltage $\mathrm{V_{sw}}$ reaches $\mathrm{V_{in}}$.

2) Turn-off: The turn-off behavior is the dual of the turn-on and consists of the following three steps:

- The first level $\mathrm{I_{A,off}}$ is the maximum current that the driver can absorb, and allows the switch voltage to reach rapidly its nominal value.
- Level $\mathrm{I_{B,off}}$ turns-on the switch to reduce the $\mathrm{I_{sw}}$ slope.
- The third level $\mathrm{I_{C,off}}$ is negative and leads the switch off.

IV. Simulation results

In this section the three-level gate driver technique is validated performing parametric simulations, and a comparison in terms of speed and dissipated power with the classical solution, i.e. fixed $\mathrm{R_g}$ and two RC snubber, is reported.

A. Three level current driver validation

Once defined $\mathrm{t_0}$ and $\mathrm{I_A}$ for both the commutations, parametric simulations were performed to tune $\mathrm{t_1}$, $\mathrm{t_2}$, $\mathrm{I_B}$ and $\mathrm{I_C}$. Fig.

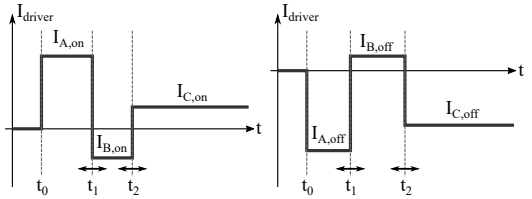

Fig. 5. Current driver for the turn-on phase (on the left side) and for the turn-off phase (on the right side).

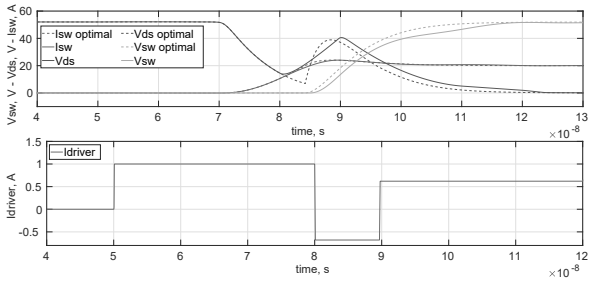

Fig. 6. Comparison between the optimal switching waveform and the ones obtained with the thee level gate driver during the turn on.

6 shows, in the top graph, a comparison between the optimal turn-on waveforms and the ones obtained driving the power transistor with the proposed driver. All the curves are in good agreement and both the switching voltage and current are not affected by oscillations.

B. Comparison with standard solution

The traditional solution consists of an high side snubber in parallel to the freewheeling diode and a low side snubber in parallel to the power switch, with a fixed R_g. A diode is insert in parallel to R_g to create a low impedance path for the turn-off. The comparison was conducted considering three different topologies, i.e, no snubber, traditional approach and proposed technique. Table I lists the considered figures of merit. The data shows that the proposed technique removes completely the switching voltage overshoot, reduces the current peak but the maximum value reached by the $\mathrm{V_{ds}}$ voltage is slightly greater. In both cases, the commutation times of the proposed solution are between the other two topologies. Finally the most significant improvement is the power saving which is greater than 50% compared to the classical solution. Finally, Fig. 7 shows a comparison between the amplitudes of the frequency spectra of the switching current for the analyzed circuits. The spectrum of the no snubbered circuit presents two peaks at $27\,\mathrm{MHz}$ and $37\,\mathrm{MHz}$ as expected, while the other two are smoothed, and are characterized by a less rich frequency content.

V. Conclusion

This paper proposed a novel criterion for controlling the switching waveforms of power transistor avoiding oscillations and reducing the stress of components. In the first part, the commutations of a lowside buck are analyzed to determine

TABLE I
Comparison between the most significant parameters interesting the buck converter working

	No Snubber	**Proposed technique**	**Snubber RC with Rg**
$\mathbf{P_{sw}}$	$1.42\,W$	$3.78\,W$	$4.95\,W$
$\mathbf{P_{diode}}$	$231\,mW$	$199mW$	$200\,mW$
$\mathbf{P_{lsnb}}$	//	//	$1,17\,W$
$\mathbf{P_{hsnb}}$	//	//	$1,95\,W$
$\mathbf{P_{tot}}$	$1.65\,W$	$4\,W$	$8.27\,W$
$\mathbf{t_{I_{sw,on}}}$	$8.22\,ns$	$8.22\,ns$	$24.5\,ns$
$\mathbf{t_{V_{sw,on}}}$	$6\,ns$	$38\,ns$	$70\,ns$
$\mathbf{t_{I_{sw,off}}}$	$18\,ns$	$60\,ns$	$60\,ns$
$\mathbf{t_{V_{sw,off}}}$	$9\,ns$	$9\,ns$	$18\,ns$
$\mathbf{V_{sw_p}}$	$104\,V$	$52\,V$	$52\,V$
$\mathbf{V_{ds_p}}$	$81\,V$	$67\,V$	$62\,V$
$\mathbf{I_{sw_p}}$	$32\,A$	$24.5\,A$	$33.8\,A$

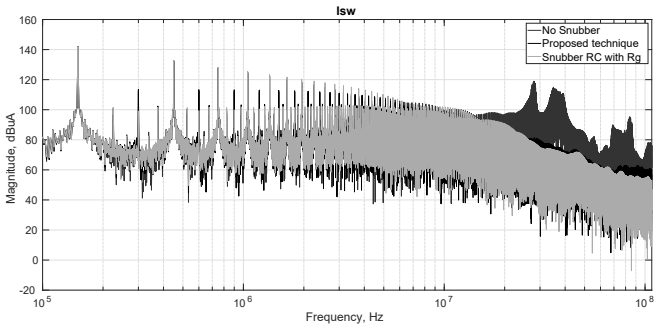

Fig. 7. Comparison between the EM spectrum of the analyzed topologies.

which phases are truly responsible for the starting of oscillations. A three levels current gate driver is proposed, and its parameters are extracted by means of parametric simulations in order to match the optimal waveforms. With respect to previous works, in the second phase of the turn-on/turn-off, charge is extracted/injected from/to gate, with the effect of avoiding ringing shorting the commutations less respect to the classical RC snubber solution. From efficiency point of view, preliminary results have shown a 50% power saving with respect to the traditional approach. The complete version of the paper will contain further simulation results, focusing on the extrapolation of the optimal switching waveforms.

References

[1] L. Middelstaedt, J. Wang, B. Stark, and A. Lindemann, "Direct Approach of Simultaneously Eliminating EMI-Critical Oscillations and Decreasing Switching Losses for Wide Bandgap Power Semiconductors", IEEE Transactions on Power Electronics, vol XX, pages YY, April 2019.

[2] H. Dymond, J. Wang, et al. "A 6.7-GHz Active Gate Driver for GaN FETs to Combat Overshoot, Ringing, and EMI", IEEE Transactions on Power Electronics , vol. 33, issue 1, pp. 581-594, Jan. 2018.

[3] M. Rose, J.Krupar, and H. Hauswald, "Adaptive dv/dt and di/dt control for isolated gate power devices", 2010 IEEE Energy Conversion Congress and Exposition, Sept. 2010.

[4] M. Blank, T. Glück, A. Kugi and H.-P. Kreuter, "Slew rate control strategies for smart power ics based on iterative learning control", in Proceedings of Applied Power Electronics Conference and Exposition (APEC), Fort Worth, TX,USA, Mar. 2014, pp. 2860–2866

[5] N. Idir, R. Bausiere and J. J. Franchaud, "Active gate voltage control of turn-on di/dt and turn-off dv/dt in insulated gate transistors," in IEEE Transactions on Power Electronics, vol. 21, no. 4, pp. 849-855, July 2006.