Suppression of Quantization-Induced Limit Cyclesin Digitally Controlled DC-DC Converters by Dyadic Digital Pulse Width Modulation

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***Abstract*—Quantization-induced limit cycle oscillations (LCOs) in digitally controlled DC-DC converters are addressed in this paper. The novel Dyadic Digital PWM (DDPWM) is proposed to increase the effective pulse-width-modulator (PWM) resolution, as required for LCO-free operation, at low cost, without sacrificing DC accuracy and with no detrimental effects on the ripple voltage. Experimental results on a synchronous buck validate the approach highlighting effective LCOs suppression and DC accuracy enhancement at 5x reduced output voltage ripple compared to thermometric dithering for the same resolution increase.**

***Index Terms*—Limit Cycle Oscillations, Dyadic Digital Pulse Width Modulation (DDPWM), Dyadic Digital Pulse Modulation (DDPM), Dithering, High Resolution PWM, Digital Control of Power Converters**

I. Introduction

Digital controllers in switching-mode power converters show unquestionable advantages in terms of cost, versatility and less sensitivity to environmental conditions compared to their analog counterparts [1], [2]. As a further advantage, the design of a digital controller can be carried out starting from an hardware description language (HLD) source code by a standard digital design flow, thus allowing the implementation of advanced control techniques, enabling reconfigurability and portability and reducing development time and design effort [3], [4].

Digital control systems are particulary attractive to implement complex control algorithms in high-power applications, where the dissipation and the cost of the controllers represent a small fraction of the total and in which the transistors are operated at low switching frequency (i.e. in the kilohertz range) and timing constraints are therefore not very stringent. By contrast, in low-to-medium power applications, where the switching frequency can reach several megahertz, as demanded to reduce size and weight, and where faster dynamic response is required, the adoption of digital controllers faces some difficulties due to the simultaneous requirement of real-time operation and minimum power dissipation to avoid the degradation of the overall efficiency [5], [6].

Under this perspective, one of the most critical blocks in digitally controlled power converters is the pulse-width-modulator (DPWM). A high resolution DPWM in fact, is necessary for output voltage accuracy, for fast transient response and, in particular, to avoid the onset of limit cycle oscillations (LCOs) [5]. Unfortunately, in a standard counter-comparator DPWM operated at a given switching frequency, high resolution is traded off with counter clock frequency and hence power consumption [2]. To address this problem, specific techniques for DPWM resolution enhancement have been proposed at the hardware level and alternative approaches for high-resolution, LCO-free DPWMs have been the subject of extensive research [7]–[10]. Most of the proposed solutions, however, result either in a degraded DC accuracy and/or in an increased cost and complexity.

Delay-line based high-resolution DPWM modulators [11], [12], in particular, achieve sub-clock cycle resolution by employing a set of delay elements, require large silicon area and their performance is strongly dependant on supply, temperature and manufacturing process variations. Sigma-delta ($\Sigma\Delta$) DPWM [13], [14] techniques have proven to be effective to increase resolution, but they operate at slow conversion speed and the feedback loop nonlinearity is responsible for the generation of low frequency idle tones inducing additional ripple onto the output voltage. Finally, in DPWM featuring dithering [6] a high resolution is obtained at low cost by changing the DPWM duty cycle over several switching periods according to an empirically optimized dithering pattern but also dithering may have a detrimental effects on the output voltage ripple.

In this paper, the novel Dyadic Digital PWM (DDPWM), based on the recently proposed Dyadic Digital Pulse Modulation (DDPM) [15], is adopted as a systematic approach to achieve accurate, LCO-free operation in a digital power converter at negligible cost and design effort and minimum output voltage ripple.

The paper has the following structure: in Section II, the role played by the DPWM resolution in the onset of LCOs in digitally controlled power converters is revised and the conventional thermometric dithering technique is introduced. In Section III, the proposed high resolution DDPWM technique is introduced starting from the DDPM technique in [15] and the advantages in terms of reduced ripple voltage of the new approach compared to thermometric dithering are highlighted.

The results presented in Section III are experimentally

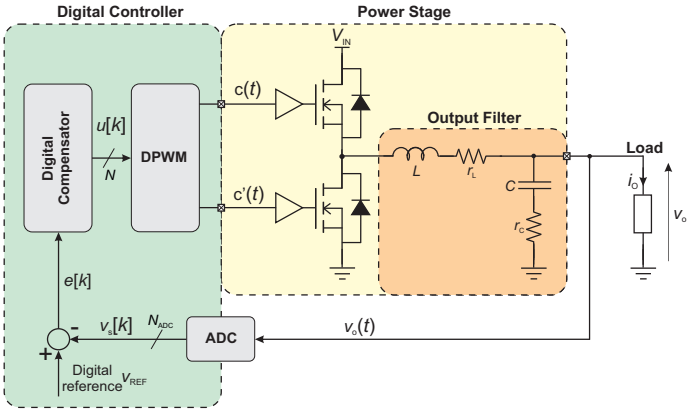

Fig. 1. Digitally controlled synchronous buck DC-DC converter with PID compensator.

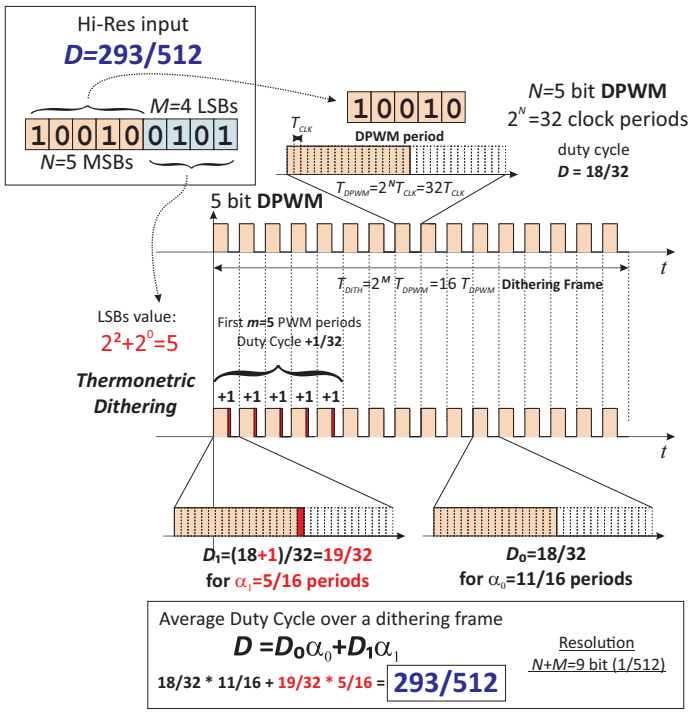

Fig. 2. High resolution DPMW by thermometric duty cycle dithering over 2^M switching periods.

validated in Section IV with reference to a synchronous buck converter digitally controlled by a specifically designed Field Programmable Gate Array (FPGA)-based test setup, which enables real time monitoring and on-the-fly reconfiguration of all the relevant parameters of the controller and of the DPWM modulator. Experimental results highlight effective LCOs suppression and DC accuracy enhancement at 5x reduced output voltage ripple compared to thermometric dithering at the same resolution. Finally, in Section V, some concluding remarks are drawn.

II. Onset of Limit Cycle Oscillations

The proposed DDPWM technique for LCO free operation is illustrated in this paper with reference to a digitally controlled synchronous buck DC-DC converter operated at $f_\mathrm{s} = 1/T_\mathrm{s}$ switching frequency with a digital proportional, integral, derivative (PID) compensator, as shown in Fig.1. The output voltage $v_\mathrm{O}(t)$ of the buck is converted into a digital stream $v_\mathrm{s}[k] = v_\mathrm{O}(kT_\mathrm{s})$ by an analog-to-digital converter (ADC) at $1/T_\mathrm{s}$ sample rate with a resolution:

$$q_\mathrm{ADC} = \frac{V_\mathrm{FS}}{2^{N_\mathrm{ADC}}}, \tag{1}$$

where $[0, V_\mathrm{FS}]$ is the ADC input swing and N_ADC is the number of bits of the converter. The digital error signal, $e[k] = v_\mathrm{REF} - v_\mathrm{s}[k]$, where v_REF is the constant digital reference, is fed to the PID compensator, which drives a DPWM modulator clocked at the $f_\mathrm{clk} = 1/T_\mathrm{clk}$. Since both the switching period $T_\mathrm{s} = KT_\mathrm{clk}$ and the active period $T_\mathrm{ON} = HT_\mathrm{clk}$ $(H, K \in \mathbb{N})$ are constrained to be integer multiples of T_clk, the duty cycle turns out to be quantized over $K = T_\mathrm{s}/T_\mathrm{clk}$ levels, resulting in a DC output voltage resolution

$$q_\mathrm{DPWM} = V_\mathrm{IN}\frac{T_\mathrm{clk}}{T_\mathrm{s}} = \frac{V_\mathrm{IN}}{K} \tag{2}$$

being V_IN the input voltage.

Based on [8], LCO-free operation requires that the Nyquist stability criterium under large-signal conditions is respected, that the integral control coefficient is not zero and that:

$$q_\mathrm{ADC} > q_\mathrm{DPWM}, \tag{3}$$

i.e., that the ADC quantization bin is larger than the LSB of the DPWM, so that at least one of the quantized DC output voltages $n/K \cdot V_\mathrm{IN}$ at fixed duty cycle n/K falls in the zero-error bin of the controller. Such conditions are normally taken as LCO-free design criteria [8].

While the first two requirements can be met by design with convenient PID coefficients, (3) is related just to the resolution of the ADC (q_ADC) and of the DPWM (q_DPWM) [5]. Assuming, for the sake of simplicity, that V_IN matches the input swing of ADC and replacing the expressions of q_DPWM and q_ADC from (2) and (1) in (3), the last condition for LCO-free operation requires that:

$$2^{-N_\mathrm{ADC}} = \frac{q_\mathrm{ADC}}{V_\mathrm{IN}} > \frac{1}{K} = \frac{f_\mathrm{s}}{f_\mathrm{clk}}. \tag{4}$$

Meeting (4) results in a stringent tradeoff between f_s, f_clk and N_ADC, which limits the DC accuracy of the buck converter at high switching frequency f_s for a given digital clock frequency f_clk and/or imposes operation at inconveniently high clock frequency f_clk to achieve a target static accuracy at high switching frequency f_s.

For example, for a $f_\mathrm{clk} = 5\mathrm{MHz}$ system clock and a $f_\mathrm{s} = 100\mathrm{kHz}$ switching frequency, the resolution of the ADC, and hence the DC accuracy of the converter, is limited by (4) to 5 bits or less, which is not acceptable for most practical purposes. Conversely, operating at switching frequencies in the 10MHz range, which are enabled by emerging GaN and SiC power semiconductors, a DC accuracy equivalent to $N_\mathrm{ADC} = 8$ bit or more requires impractically high digital clock frequencies exceeding 2GHz.

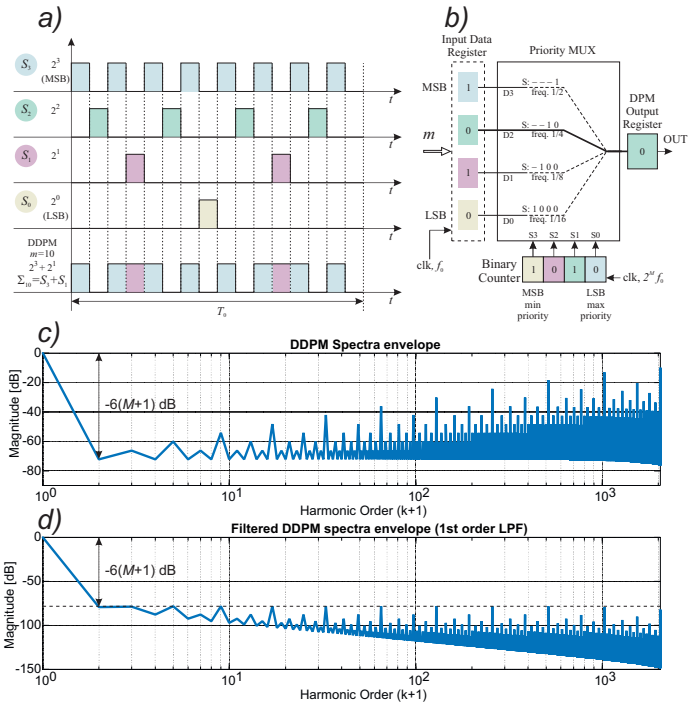

Fig. 3. Dyadic Digital Pulse Modulation (DDPM) [15]: a) DDPM pattern, b) DDPM modulator hardware, c) envelope of the spectra of the 4096 12-bit DDPM patterns, d) spectral envelope as in c) after first-order filtering.

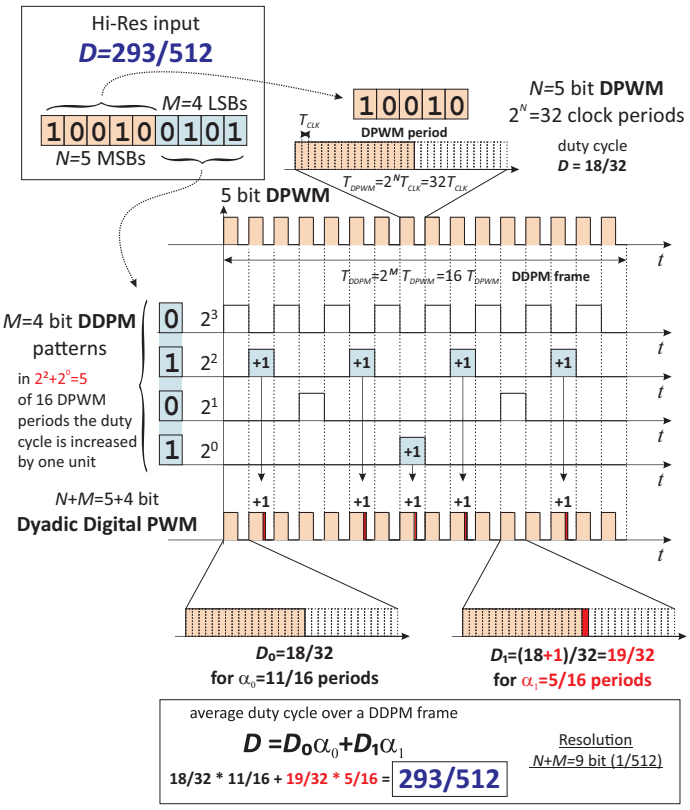

Fig. 4. $N+M$ bit Dyadic Digital Pulse Width Modulation (DDPWM) technique to increase the effective resolution of N bit DPWM to $N+M$ bits by M-bit DDPM dithering over 2^M periods.

A. High Resolution PWM Techniques

In order to enhance the DPWM resolution without increasing the digital clock rate, dithering techniques consisting in the variation of the duty cycle of one LSB over pre-defined patterns have been proposed so that to control the average duty cycle in a dithering pattern with a sub-LSB resolution [8]. For example, adopting the thermometric dithering approach illustrated in Fig.2, the digitally quantized duty cycle is $(n+1)/2^N$ in the first m switching periods of a 2^M dithering pattern and $n/2^N$ in the remaining periods, so that an average duty cycle $(n\cdot 2^M+m)/2^{N+M}$ quantized over $N+M$ bits can be achieved, thus increasing the effective DPWM resolution of M bits.

Thermometric dithering is inexpensive and amenable of a simple digital implementation, but unfortunately it may introduce noise at switching frequency sub-harmonics, which cannot be properly rejected by the buck output filter and generally lead to relevant sub-switching frequency output ripple (not to be confused with chaotic output fluctuations related to LCO).

While empirically optimized dithering patterns [8] and $\Sigma\Delta$ modulation can be adopted to mitigate these issues, the new, deterministic, Dyadic Digital Pulse Width Modulation (DDPWM) approach is proposed in this paper to achieve optimal resolution enhancement at minimum ripple and dynamic performance degradation.

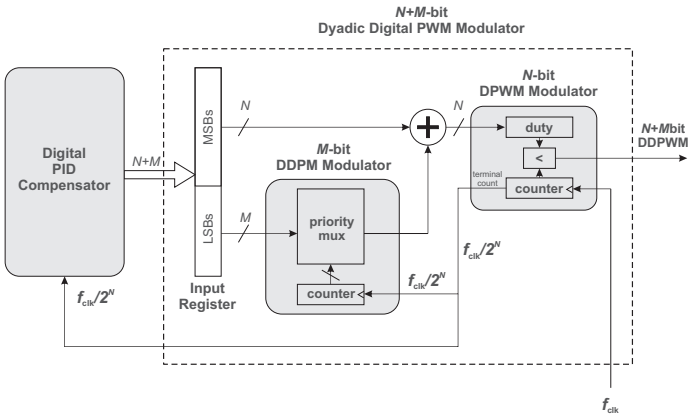

Fig. 5. Architecture of the proposed DDPWM modulator.

III. High Resolution Dyadic Digital Pulse Width Modulation (DDPWM)

The Dyadic Digital Pulse Modulation (DDPWM) adopted in this paper to overcome the limitations of previous dithering techniques is based on the Dyadic Digital Pulse Modulation (DDPM) introduced in [15] and illustrated in the following with reference to Fig.3.

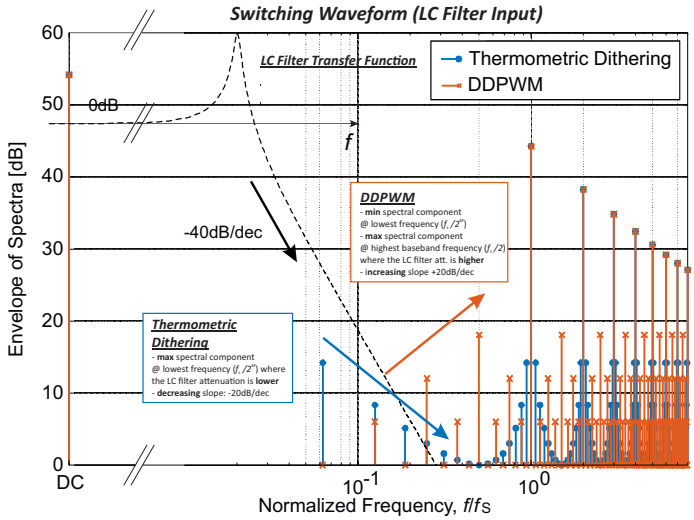

Fig. 6. Envelope of the spectra of $N = 4$-bit DPWM with $M = 5$ bit thermometric dithering over 2^M periods as in Fig.2 and of $N+M$ DDWPM patterns.

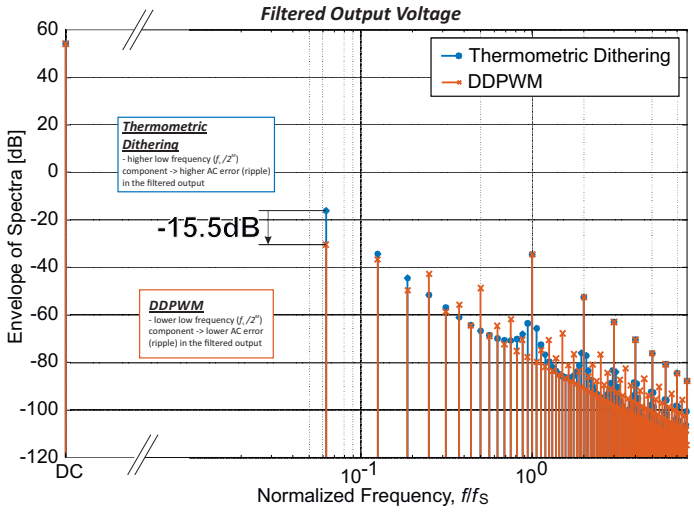

Fig. 7. Envelope of the spectra of $N = 4$-bit DPWM with $M = 5$ bit thermometric dithering over 2^M periods as in Fig.2 and of $N+M$ DDWPM patterns, filtered by a 2^{nd} order LC filter, as in the buck converter in Fig. 1, with corner frequency $2 \cdot 10^{-2} f_{\text{s}}$.

A. Dyadic Digital Pulse Modulation (DDPM)

The DDPM modulation presented in [15] associates to any binary number m, represented on M bits in terms of its binary digits $b_i \in \{0,1\}, i = 0 \dots M-1$ as

$$m = \sum_{i=0}^{M-1} b_i 2^i,$$

the 2^M-bit long digital stream

$$\Sigma_m(t) = \sum_{i=0}^{M-1} b_i S_i(t) \quad 0 < t < T_0 \tag{5}$$

obtained by superposition of the dyadic basis signals $S_i(t)$ for $i = 0 \dots M-1$, which include exactly 2^i digital "ones" separated by $2^{M-i}-1$ digital "zeros", arranged so that to be orthogonal (i.e. $S_i(t) \cdot S_j(t) = 0 \ \forall i \neq j$) as defined in [15] and illustrated in Fig.3a. Since "one" pulses in a dyadic basis signal $S_i(t)$ are exactly 2^i and are non-overlapping, it follows that $\Sigma_m(t)$ includes a number of "one" pulses equal to m and has a mean value of $(m/2^M)V_{\text{IN}}$.

Moreover, looking at the envelope of the spectra of DDPM signals corresponding to different m, i.e.

$$S(kf_0) = \max_m |\text{DFT}\{\Sigma_m(nT_{\text{clk}})\}| \tag{6}$$

where DFT $\{\cdot\}$ is the Discrete Fourier Transform operator and $f_0 = 1/(2^M T_0)$, which is reported in Fig.3c for $M = 12$ bit, it can be observed that the AC spectral components of DDPM streams are concentrated at high frequencies and can be easily filtered out. In detail, the dominant spectral components of a DDPM stream are found to be at $k = 2^h$, $h = 0 \dots (M-1)$ harmonics, increase with k with a slope of 20dB/dec and can be kept $-6(M+1)$dB below the DC by a first-order filter with a cutoff frequency $f_{\text{c}} = f_0/\sqrt{3}$, as illustrated in Fig.3d.

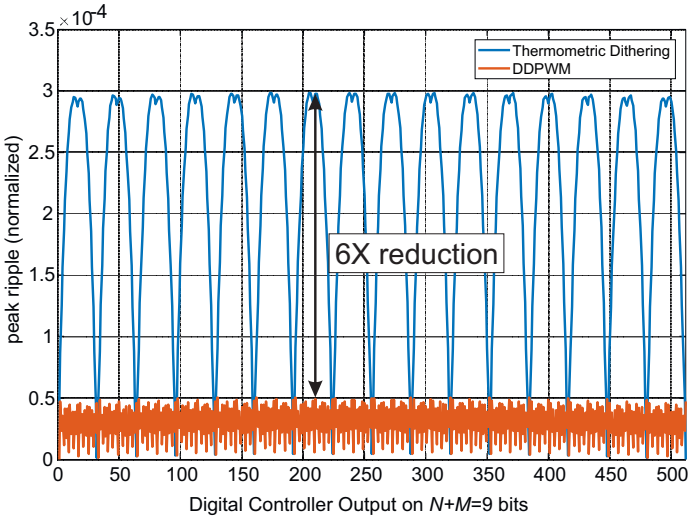

Fig. 8. Simulated dithering-induced ripple voltage in open loop configuration (normalized with respect to the DC output voltage) vs. hi-res duty cycle by $M = 5$ bit thermometric dithering (Fig.2) and by $N = 4$-bit, $M = 5$ bit DDPWM (Fig.4).

Last but not least, DDPM streams corresponding to M-bit binary numbers can be generated by simple digital hardware including a priority multiplexer driven by an M bit binary counter, as shown in Fig.3b and discussed in details in [15].

B. Dyadic Digital Pulse Width Modulation (DDPWM)

In this paper, the DDPWM technique is adopted to increase the effective resolution of an N-bit DPWM modulator to $N+M$ bits, so that to achieve LCO-free operation without trading off switching frequency and DC accuracy in a DC-DC converter.

According to the proposed technique, the duty cycle of a DPWM signal is modulated between two adjacent quantization

TABLE I
SYNCHRONOUS BUCK: POWER STAGE AND PID CONTROLLER PARAMETERS

Quantity	Symbol	Unit	Value
Input Voltage	V_{IN}	V	10
Output Voltage	V_{O}	V	5.12
Switching Frequency	f_{s}	kHz	100
Filter Inductance	L	μH	100
Inductace Series Resistance	r_{L}	mΩ	56
Filter Capacitance	C	μF	220
Capacitor Equivalent Series Resitance	r_{C}	mΩ	90
PID Proportional Gain	k_{P}	–	2.6781
PID Integral Gain	k_{I}	–	0.0408
PID Derivative Gain	k_{D}	–	6.5019

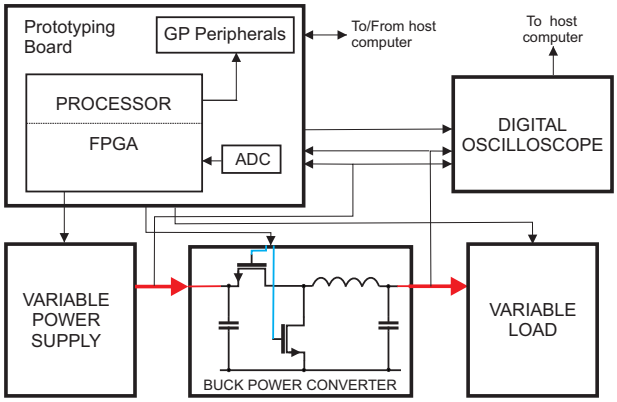

Fig. 9. Block diagram of the experimental testbench.

levels, i.e.

$$D_0 = \frac{n}{2^N},$$

and

$$D_1 = D_0 + 1\mathrm{LSB}_{\mathrm{DPWM}} = \frac{n+1}{2^N},$$

where n is the value represented in the first N MSBs of the input, according to the M-bit DDPM pattern which corresponds to the integer m represented by the last M LSBs of the digital input, as shown in Fig.4. Since a duty cycle D_0 is applied $2^M - m$ times and a duty cycle D_1 is applied m times over a pattern of 2^M switching periods, the average duty cycle over 2^M periods is

$$D = \frac{n}{2^N}\frac{2^M - m}{2^M} + \frac{n+1}{2^N}\frac{m}{2^M} = \frac{n \cdot 2^M + m}{2^{N+M}} \qquad (7)$$

and is therefore equal to the duty cycle corresponding to the value of the digital input $n \cdot 2^M + m$ quantized over 2^{N+M} levels.

As a consequence, replacing the DPWM module in the digitally controlled DC-DC converter in Fig.1 by the DDPWM modulator in Fig.5, which is operated at the same clock frequency f_{clk} and includes an N bit DPWM modulator and an M bit DDPM modulator as in Fig.3, the output voltage can be quantized at $N + M$ bit resolution, making it possible to meet LCO-free operation condition (3) with $+M$ bits ADC resolution and overall output accuracy compared to plain DPWM.

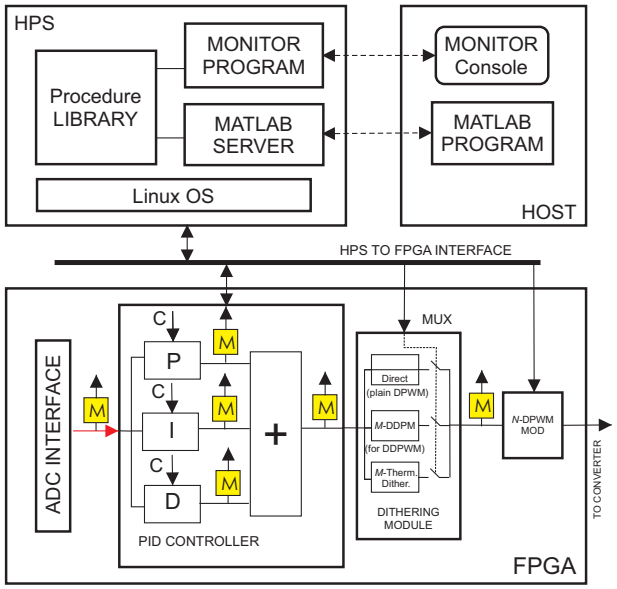

Fig. 10. Internal Hardware/Software organization of the SOC system.

Compared to thermometric dithering, DDPWM modulation provides an optimal distribution of the baseband, sub-switching frequency spectral energy towards high frequencies, which follows from the spectral properties of DDPM streams (Fig.3c-d).

The favorable spectral properties of DDPWM streams are illustrated in Fig.6, where the envelope of the spectra of DDPMW and thermometric dithering patters for the same $M = 5$ bit increased resolution are compared. In particular, it can be observed that DDPWM shows minimum energy at lowest-frequency harmonic components, which are closer to the pass band of the LC filter and give a particularly critical contribution to the output voltage ripple.

As a consequence, for the same LC filter, adopting DDPWM results in significantly lower baseband spurious, as shown in Fig.7, and hence to a lower ripple under all possible quantized duty cycle values, as emerges from the simulation results in Fig.8, where a reduction of 6x in the worst-case peak ripple, which corresponds to the 15.5dB reduction in the lowest spectral component of Fig.7, is observed.

Finally, since the PID compensator output is updated every DPWM period as in a plain N-bit DPWM modulator, and not every DDPWM pattern, the increased output resolution and LCO-free operation is not traded off with the sampling frequency and dynamic performance, thus resulting in a net improvement at negligible hardware and software cost.

IV. EXPERIMENTAL RESULTS

To validate the proposed approach, a two-layer printed circuit board (PCB) has been specifically designed to accommodate the power stage in Fig.1 with the parameters listed in Tab.I, while the digital control algorithm has been implemented on an Altera prototyping board [16] by referring to the parallel implementation form of the PID compensator

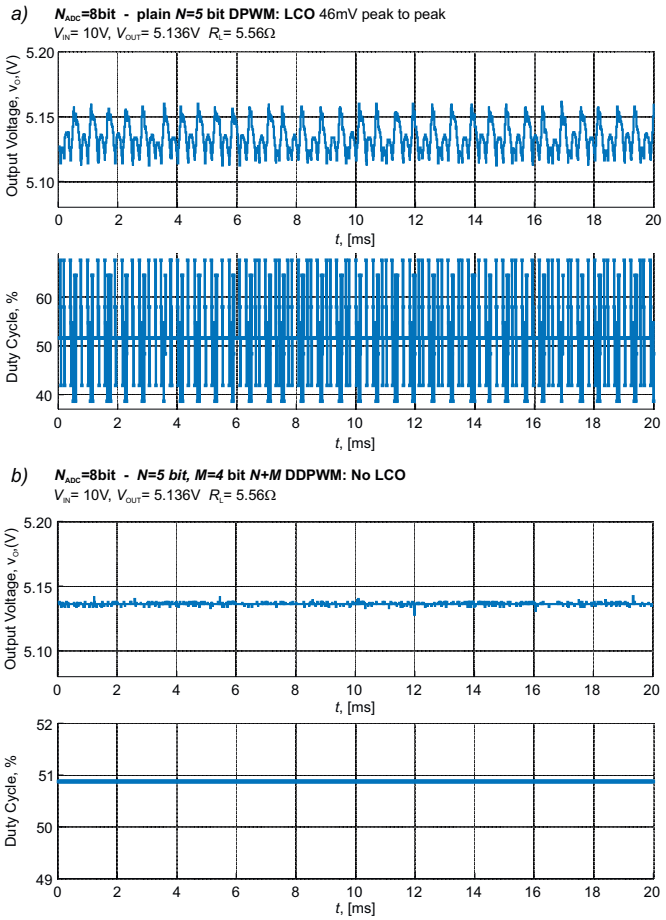

Fig. 11. Output voltage waveforms and duty cycle waveforms of the synchronous buck at $f_s = 100$kHz switching frequency and $f_{clk} = 3.2$MHz digital clock frequency for $N_{ADC} = 8$: a) using plain DPWM at $N = 5$ bit resolution and resulting in LCOs, b) using $N + M$ bit DDPWM with $N = 5$ and $M = 4$, revealing LCO suppression.

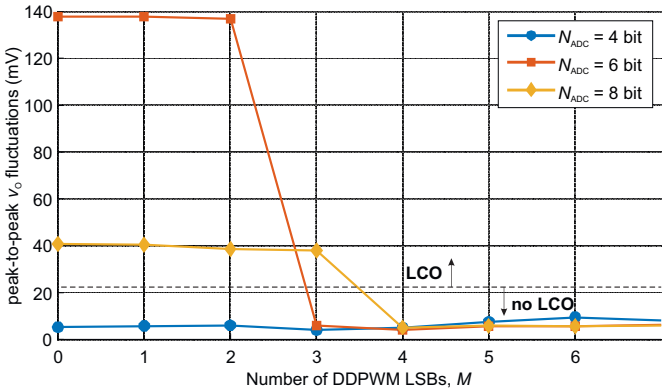

Fig. 12. Amplitude of LCOs for $N+M$-DDPWM with $N = 5$ under different values of M for $N_{ADC} = 4$, $N_{ADC} = 6$ and $N_{ADC} = 8$, open-circuit load.

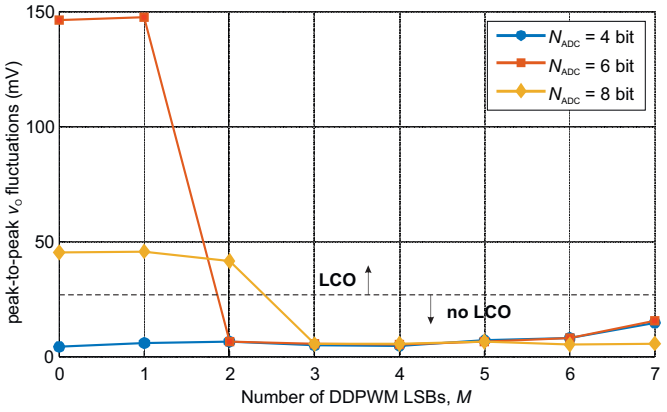

Fig. 13. Amplitude of LCOs for $N+M$-DDPWM with $N = 5$ under different values of M for $N_{ADC} = 4$, $N_{ADC} = 6$ and $N_{ADC} = 8$, $I_O = 1$A load current.

[5]. Compensator gains are also reported in Tab.I and have been computed to set the crossover frequency to $f_c = 5$kHz and the phase margin at $\varphi = 55°$.

A. Experimental Test Setup

The testbench for the experimental verification of the algorithm has been designed using a System On Chip (SOC) approach which in the same integrated circuits combines an embedded high performance general processor and a large amount of programmable logic. The latter allows to easily experiment with different ADC and DPWM settings without major hardware changes. The embedded processor provides the capabilities for a user-friendly interface and connection to other processing systems.

The testbench has five main components as shown in Fig.9. The main elements are the synchronous buck power converter introduced before and an Altera DE1-SOC prototyping board [16] which operates as a programmable digital controller. The board contains a dual core hard processor ARM-based system (HPS) and a FPGA in a single chip and a 12 bit ADC. The testbench also includes a digitally programmable power supply, a digitally programmable resistive load and a 4-channel digital oscilloscope.

The functional organization of SOC/FPGA system is shown in Fig.10. The lower part shows the hardware architecture implemented in the FPGA while the upper part represents the software operations performed by the HPS hard processor.

The FPGA configuration and the embedded processor code are downloaded from a host computer in a configuration phase. The FPGA comprises an interface to the ADC, which acquires the input and output voltages of the synchronous buck, a PID controller (or compensator), whose gain coefficients may be externally programmed, and a DPWM modulator, which can be configured by a multiplexer (MUX) so that to implement plain N-bit DPWM, $N + M$-bit DDPWM (architecture in Fig.5) or thermometric dithering over 2^M switching cycles.

The PID coefficients, the MUX and the DPWM control signals are provided by the embedded processor through a digital interface. Each output signal from the hardware modules in the bottom of Fig.10 is sampled periodically and acquired samples are stored in memories M, whose content may be read by the processor for monitoring purposes.

The application software on the embedded processor runs on the Linux operating system which provides access to all

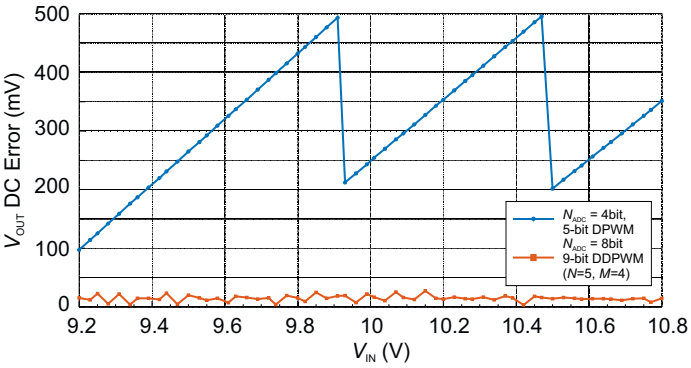

Fig. 14. Static error in the output voltage under different input voltages.

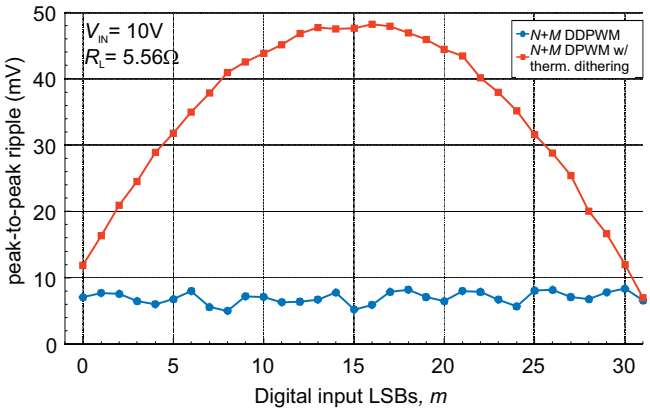

Fig. 15. Measured dithering-induced ripple voltage (open loop configuration) vs. hi-res duty cycle by the thermometric dithering (Fig.2) and by DDPWM (Fig.4) under the same $M = 5$ resolution enhancement.

the system peripherals of the board and can be interfaced to a host computer running Matlab through a dedicated data server. A Matlab script may be used to run a sequence of experiments with different converter parameters, to acquire the corresponding data, to process them and to display parametrically the results.

B. Experimental Results

The effectiveness of DDPWM in suppressing LCOs is experimentally verified in Fig.11. In Fig.11a, in particular, the output voltage of the buck converter with an $N_{\rm ADC} = 8$ bit ADC operated at $f_{\rm s} = 100$kHz switching frequency by a plain DPWM modulator clocked at $f_{\rm clk} = 3.2$MHz, resulting in a $N = 5$ bit DPWM resolution, not meeting the LCO-free operation condition (3). is reported. Significant, 46mV peak-to-peak amplitude LCOs can be observed consistently with the theory [8]. By contrast, in Fig.11b LCO-free operation is observed under the same $N_{\rm ADC} = 8$ bit ADC resolution, switching frequency and digital clock rate by using $N + M$ DDPWM with $N = 5$ and $M = 4$.

The same tests have been performed for an ADC resolution $N_{\rm ADC} = 4$, $N_{\rm ADC} = 6$ and $N_{\rm ADC} = 8$ under different number of bits of the dyadic modulator M ($M = 0$ being plain DPWM). The corresponding experimental results are summarized in Fig.12 and in Fig.13 for an open circuit load and for a 1A output current, respectively.

The results reveal a reduced LCO amplitude for $N_{\rm ADC} = 8$ while increasing M, up to a complete LCO suppression from $M = 4$ for open-circuit load and from $M = 3$ for 1A load current. For $N_{\rm ADC} = 6$, the complete LCO suppression is achieved starting from $M = 3$ ($M = 2$) for open-circuit load (1A load current) as expected from (4) in view of the reduced ADC resolution.

Finally, for $N_{\rm ADC} = 4$, LCO-free operation is achieved also for plain DPWM (i.e. $M = 0$), but at the cost of a coarse output voltage regulation, as shown in Fig.14. Looking at the same Fig.14, by contrast, it can be observed that LCO-free operation and DC accuracy can be obtained at the same time by adopting DDPWM.

The low-frequency output ripple resulting from $N = 5$, $M = 5$ DDPWM is then compared in Fig.15 with thermometric dithering. To avoid possible confusion of ripple and LCOs related to the closed-loop operation, the ripple test has been performed under open-loop conditions, by sweeping the M LSBs of the modulator output from 0 to 31, for a value $n = 16$ of the N MSBs, which corresponds (for $m = 0$) to a 50% duty cycle. The experimental results presented in Fig.15 are consistent with Fig.7 and Fig.8 and reveal negligible low frequency ripple (not distinguishable from the ESR-related ripple voltage) for DDPWM, when compared with the significant ripple up to about 50mV of the thermometric dithering.

V. Conclusions

The DDPWM modulation technique has been proposed as a systematic approach to increase the effective resolution of DPMW so that to suppress quantization-induced LCOs in digitally controlled power converters at reduced hardware complexity and minimum performance degradation.

Measurements on a synchronous buck converter confirm the effectiveness of the technique, enabling LCO-free operation at higher switching frequency and/or DC accuracy than in plain DPWM at the same digital clock frequency. Compared to thermometric dithering, a lower frequency ripple (up to 5X measured reduction) has been observed with the proposed technique for the same 5-bit DPWM resolution enhancement.

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