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Thesis Abstract
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Digital Design Techniques for Dependable High Performance Computing

The overall goal of my doctoral research activity is oriented in development of high performance computing design techniques for high reliability of digital circuits. One of the most critical environment aspects that could reduce the reliability of modern VLSI technologies used for high performance computing is radiation. When a set of radiation particle interact within the electronic systems by an exchange of energy, several kinds of effects can be observed. The impact of radiation effects on electronic devices can cause a misbehavior on the functionality of the circuit. In order to apply strategies and techniques to tolerate these faults and errors, these effects must be analyzed in detail. Considering high frequency and smaller size of recent technologies, the sensitivity of High Performance Computing toward radiation is expected to be higher. Therefore, having more resilient mitigation technologies is more relevant and necessary, which is the focus of my research activity.

Radiation-induced effects can lead different effects depending on the location and time of the incident. If the effects of radiation incident last for a short period of time, it is known as a Transient fault. While if the effects last for a longer duration, it is known as a permanent fault. Therefore, my PhD dissertation is divided into two main parts. The first part as the main part is dedicated to the transient fault, mostly focusing on Single Event Transient while the second part is dedicated to the permanent fault such as Micro Single Event Latch-up and Total Ionizing Dose.

Considering Single Event Transient as the golden part my research, it covers different phases of this phenomena from the generation until the mitigation. The first phase is dedicated to the physical modeling of these effects and evaluating the impact of the radiation environment profile on the generated SET pulse. The second phase is devoted to development of tools and algorithms for analyzing and predicting the behavior of the effected device. As a last phase, the developed physical model and performed analysis have been the golden keys to propose an efficient mitigation solution for robustness of the developed system against this phenomenon. The

proposed mitigation solution has been known as the first method able to filter Single Event Transient pulses with zero-timing overhead. These methodologies have been applied to modern High Performance Computing technologies with high frequency and smaller size which leads to more critical condition for Single Event Transient effect.

This comprehensive proposed flow for analyzing and mitigating Single Event Transient has been applied to several industrial projects such as EUCLID space mission project with the goal of monitoring the dark space which the lunch planned for 2020 carrying by European Space Agency. The developed SET analysis and mitigation work-flow has been part of the handbook *Space Product Assurance Techniques for Radiation Effects Mitigation in ASICs and FPGAs handbook*, published by European Space Agency.

Moreover, the developed set of tools has been known as the best *Best EDA Tool for improving design automation for integrated circuits and systems* by IEEE Council on Electronic Design Automation.

However, as a part of my research activity, not only I focused on the Transient effects, but I dedicated the second part of my dissertation to the evaluation of permanent effects such as Single Event Latch-up and total Ionizing Dose. The second effect I focused on is Single Event Latch-up which is one of the major reliability concerns for VLSI device applied in safety critical applications. The reduction of the circuit feature size and operating voltage levels are leading to a new kind of latch-up called micro Single Event Latch-up. Single Event Latch-up tends to occur near the input/output terminals of logic gates while micro Single Event Latch-up may occur at various locations between layers. One of my main research contributions is to propose a first 3D model for describing the 3D physical layout description of the design including the interconnection resources and logic versatile. This 3D layout description leads to analyze the sensitivity of the sub-micron circuitry to Micro Single Event Latch-up phenomena while considering the layout, depth, size and density of the design. This methodology is considered as the first one applicable to large industrial designs.

Bench-marking technologies are becoming increasingly attractive since their configuration memory is almost immune to Single Event Upset. However, applied in mission critical application, especially long-term missions, the FPGA devices are subject to cumulative ionizing damage, known as Total Ionizing Dose. Total Ionizing

Dose may affect the FPGA, causing performance degradation and eventually permanent damage. Therefore, I dedicated part of my research activity to propose a physical model of Total Ionizing Dose effect in order to analyze the Total Ionizing Dose effect on recent modern technologies.