Summary

The LHC complex at CERN is the world's high energy particle accelerator and collider. By accelerating two beams of protons at near-light speed, it allows the experiments placed along its circular path to study the results of proton-proton collisions. The standard model of physics provides a detailed account of the collisions products and their production rates, and by studying the results of the experiments, it is possible to assess whether the model is correct, or if new theories must be put forward in order to explain the observations.

At the core of the experiments at CERN lies a tracker: a silicon detector capable, thanks to its layered structure, to reconstruct the path of the particles generated by the collisions as they escape the interaction point.

The next upgrade of the LHC complex will increase its luminosity, and, with it, the amount of radiation produced and the number of proton-proton collisions per beam crossing. The innermost layers of the trackers, composed of hybrid pixel chips, must therefore be replaced with new electronics capable of sustaining unprecedented radiation doses, and keep track of a much higher number of particles.

The original contribution of this thesis is the design of new digital architectures for hybrid pixel detectors. The new readout chips must be capable of recording particles at rates of 750 MHz for trigger latencies above 12.5 μs. The expected radiation doses that the chips have to withstand before replacement are in the order of 500 Mrad. The pixels' area has been scaled to 50×50 um^2, 8 times smaller than that of the current chips, in order to enhance the spatial granularity of the detector.

A variety of buffering and readout schemes have been proposed, implemented, and analyzed with respect to their performances. The efficiency has been assessed with realistic inputs by a verification environment. The proposed solutions rely on the advantages brought about by hierarchically grouping pixels together in the matrix, and share the buffering and control logic in order to achieve higher efficiencies while reducing the power consumption and area occupancy.

The architectures designed have been implemented in 3 main projects which share the common goal of exploiting the CMOS 65nm technology for the creation of highly integrated radiation-hard electronics capable of satisfying the requirements for the HL-LHC inner tracker.

The CHIPIX65 collaboration by INFN developed a 64×64 pixel chip demonstrator,

including many IP blocks and 2 Analog Front-Ends. The author designed the chip's readout scheme and buffering architecture, using 4×4 Pixel Regions, whose shared logic achieved > 99 % efficiency with a power consumption of 7.5 μW/pixel. The chip has been verified to be working after 600 Mrad of Total Ionizing Dose, and its performances characterized with a variety of sensors.

The second pixel chip has been developed in the context of the RD53 collaboration. The RD53A chip is a half-scale prototype with a 400×192 pixel matrix, integrating 3 different Analog Front-Ends, and 2 digital architecture, including a re-engineered version of the one proposed in CHIPIX65. The much bigger pixel matrix posed several integration issues, which had to be solved to ensure timing consistency across the matrix, and to allow for fast event readout. The chips have been tested with 2 DAQ setups, a variety of sensors and test beams, all showing the chip's functionalities to 500 Mrad irradiation.

The RD53 collaboration is currently working for the final full-chip prototypes for the CMS and ATLAS experiments. A thorough architectural performance assessment has been done with the new physics simulations available, in order to converge into a common digital architecture for the final chip.