


Doctoral Dissertation
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Motor Overvoltage and Power Losses Analysis in Industrial AC Drives Based on Si and SiC Devices

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Summary

In recent years, SiC based switches have become an attractive solution in the field of high-speed motors for replacing traditional Si based switches, mostly because of their higher switching frequency capability. The adoption of SiC devices in three-phase inverters has a series of advantages and drawbacks. The advantages include higher converter efficiency and the possibility to increase the switching frequency, which results in the reduction of heat sink size and inductive elements. The insulation stress on the electric machine due to the overvoltages caused by high dv/dt and long cables are the main drawbacks of the drive when SiC devices are used.

The research activity was sponsored by Fidia S.p.A, which is active in the realization of machine tools. The aim of the company was to realize an industrial inverter based on SiC devices controlled by an FPGA. A new converter was designed, built and tested. This converter offers the possibility to perform fair comparisons between different switch configurations: all-Si, Si-SiC and all-SiC. The comparison reveals remarkable losses reduction in all-SiC configuration however, serious problems at the motor terminals were found even with few meters of connecting cable.

In order to solve this problem, a detailed study of the drive was conducted and a more accurate model of the cable was derived. Using this model, formulae used for RL filter design were derived and a filter was designed, build and tested. A new issue emerged from the experimental results when RL filter was used in combination with all-SiC. An unpredicted additional motor overvoltage was detected which was due to the combination of the filter resistor parasitic inductance and the high dv/dt. The design formulae were readapted and then experimentally were validated. Finally, a circuital solution for the compensation of the resistor parasitic inductance issue was proposed.

To the memory of my father, Renato,
who always believed in me.

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Chapter 1

Introduction

In the last century, the introduction of Silicon Insulated Gate Bipolar Transistors (Si IGBTs) in converters used for low voltage industrial AC drive had led to increasing of switching frequency and operating voltage compared to the cutting-edge technology of that era [1]. Companies have been continuing to improve Si IGBT devices performances reaching almost the maximum technology exploitation. However, minority charge phenomena, as Tail Current (TC) and Reverse Recovery Current (RR), give rise to high switching losses and do not permit faster commutations, that turn out to be an obstacle in the switching frequency increment [2].

An important trend in the development of new switches based on Silicon Carbide (SiC) material has been registered in recent years [3, 4]. Interest in this material has increased due to the higher dielectric strength and energy gap presented by SiC with respect to silicon counterpart [4, 5]. By virtue of these valuable proprieties, unipolar devices, which do not present minority charge phenomena, can be made by having low-on voltage drop, high voltage rating and high operating junction temperature [6]. Unipolar components present in the market based on SiC material with Safe Operating Area (SOA) comparable with Si IGBT and Si Diode are: Metal Oxide Semiconductor Field Effect Transistor (MOSFET) and Schottky Barrier Diode (SBD) [4]. Different inverter leg configuration for Voltage Source Inverter (VSI) could be obtained by combining devices of the new and old generations. Combination of Si IGBT and SiC SBD, also called hybrid or Si-SiC, permits the reduction of the switching losses by removing the reverse recovery charge. While, SiC MOSFET plus SiC SBD combination, also called full SiC or all-SiC, permits the reduction of the switching losses by removing the tail current and the reverse recovery. Using these two solutions, faster commutations can be achieved leading to the possibility to increase the converter switching frequency [7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17].

The high switching frequency capability presented by converters based on SiC devices has attracted the attention of high-speed and low inductance machines users

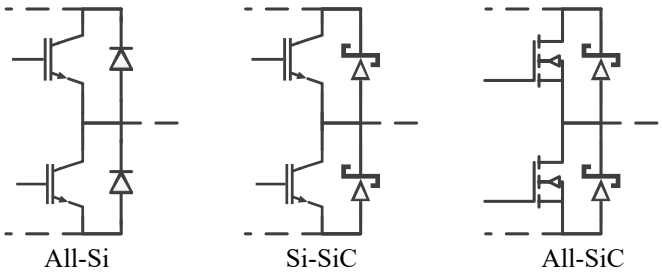


Figure 1.1: Switch configurations using devices based on Si and SiC materials.

[18, 19]. SiC VSIs benefits include lower motor current ripple, higher motor and inverter efficiencies, higher current bandwidth and lower acoustic noise [20, 21, 22]. Nevertheless, once high-speed devices are used and connected to ac drives standard issues are amplified and new drawbacks are experienced. High current derivative (more than 5 kA/μs) can lead to overvoltage at the device terminals causing the switch destruction [23], thence a careful design of the commutation loop is required [24]. In [9], the electromagnetic interference (EMI) introduced by these Si-SiC and all-SiC devices is quantified showing an important increase of the high-frequency spectral content. In [25], common-mode chokes were introduced in the drive and a detrimental effect in noise reduction was registered when the drive switching frequency was increased. In [7, 26], overvoltage at the motor side was found even with few meters of connecting cable.

Designers of electric drives should accurately investigate the real pros and cons introduced by inverter based on SiC devices with respect to standard inverter based on all-Si devices. Thus, fair comparisons between three-phase inverters based on all-Si, Si-SiC and all-SiC are required.

The research activity conducted during these three years is sponsored by Fidia S.p.A. The Fidia S.p.A. company is active in the realization of highly specialist tooling machines adopting fast spindle drives and axes drives. The aim of the company is to do fair comparisons between all-Si, Si-SiC and all-SiC devices when these devices are used in the company applications. Converter based on the different configuration switches has been compared with the aim to determine pros (losses reduction), cons (implementation issues, drive issues, cost) and retrofitting features (replacement of their standard drives with SiC based drives). For this purpose, an industrial converter composed of twin three-phase inverters has been developed. The developed electronic has been realized with the aim to do comparisons with the same power module package, PCB layout, heat sink, connections between the power module terminals and the converter terminals including the control firmware.

1.1 Personal contribution

The main contributions presented in this thesis are summarized here.

- Design details of an industrial power converter composed of two three-phase inverters with a power rating of 15 kW each are provided. The power converter is controlled by an FPGA and it is compatible with all-Si, Si-SiC and all-SiC devices. By using this converter fair comparisons between the three technologies can be done.
- Experimental comparison between the AC losses presented by all-Si, Si-SiC and all-SiC devices were conducted using the same power board. Thence, the same power module package, layout, heat sink and connections between the power module terminals and the converter terminals were used during the experiments. Losses were measured by means of very accurate instrumentation by applying the most accurate measurement method present in the literature, the opposition method.
- Experimental comparisons of issues present in ac drives, between all-Si, Si-SiC and all-SiC devices, were conducted using the same power board. From experimental results, dangerous motor overvoltage, present when few meters of connecting cable are used with SiC devices, was measured.
- With the aim to design solution for motor overvoltage issue, two-conductor and multi-conductor transmission line theory applied to power cables was revised and corrected. Line-to-ground and the line-to-line motor overvoltages caused by the connecting cable were investigated in detail.
- A novel parameters drive measurement method is presented and these parameters can be used for different purposes as filter design.
- By adopting the theory proposed in this thesis, an experimental comparison of the performance presented by the RL filter used for motor surge voltage mitigation was conducted. Performance loss of the RL filter was discovered when SiC MOSFET devices were used. This problem was analytically investigated and a solution was introduced.

1.2 Thesis content

The content of this thesis is summarized here.

- In Chapter 2, functionalities and specifications of the converter, that is compatible with all-Si, Si-SiC and all-SiC devices, developed during my research activity are given.

- A converter based on the defined specifications is implemented and its design process is described in Chapter 3. Preliminary tests results of the power converter are provided. Furthermore, problems found during the tests are described.

- In Chapter 4, a literature review of converter loss measurement methods is provided. Among all the methods, the opposition method is chosen and applied to the designed power converter. The losses measurement results of the converter with mounted all-Si, Si-SiC or all-SiC devices are proposed. Finally, the AC power losses of all the configurations are compared.

- Side effects caused by the introduction of VSIs in the industrial field are reviewed in Chapter 5. Experimental comparisons of these issues, by adopting all-Si, Si-SiC and all-SiC devices, are proposed in this chapter. Experimental results revealed dangerous surge voltage at the motor winding even with few meters of connecting cable.

- In Chapter 6, two-conductor and multi-conductor transmission line theories are revised and corrected. By virtue of the rigours formulation provided in this section, new concepts about motor over-voltage, which could be used by inverter software designers and power cable designers are provided.

- The drive parameters are necessary for motor overvoltage filter design, thus in Chapter 7 existing drive parameter measurement methodologies are given. In addition to the existing methods, a parameter measurement method that leads the faster design of filters is proposed. Furthermore, a new simple elementary component of transmission line, which permits the simulation of both high and low-frequency phenomena is given.

- In Chapter 8, a literature review of filtering topologies used for motor over-voltage issue is provided. Between all the solutions, RL filter at the inverter side has been selected and studied in detail. Comparison results of the motor overvoltage mitigation task using the same filter and changing the power module technology are given in this chapter. From the comparison, it emerges a performance loss of the filter when SiC MOSFET is used. Then, the analytical analysis of this problem is proposed and a novel solution is introduced.

Chapter 2

Power converter

2.1 Introduction

In this chapter, functionalities and specifications of the converter developed during my research activity are described and given. This converter must meet the requirements defined below.

- It needs to be compatible with power modules based on all-Si, Si-SiC and all-SiC. This option permits to do fair comparisons (from an industrial point of view) between novel switches (i.e. Si-SiC and all-SiC) and the standard one (i.e. all-Si).
- This converter needs to be compatible with the other ones of the same family (XPOWER) [27]. The compatibility needs to be maintained from a mechanical, electronic and firmware point of view. This feature permits the possibility to do retrofit actions.
- The required inverter needs to be a hybrid version of two existing converters (XP100-75-A and XP50-30-D), thus allowing the creation of a new converter with diverse power rating.

2.2 Standard power converters

Power converters present in XPOWER family have the same width and height. Considering Computer Numerical Control (CNC), many power converters are connecting in parallel as can be noticed from Fig. 2.1. Thence, by virtue of having equal mechanical sizes, power converters can be simply connected in parallel by using copper bars. The standard size proposed by Fidia S.p.A company is 338 mm for the width and 440 mm for the height.

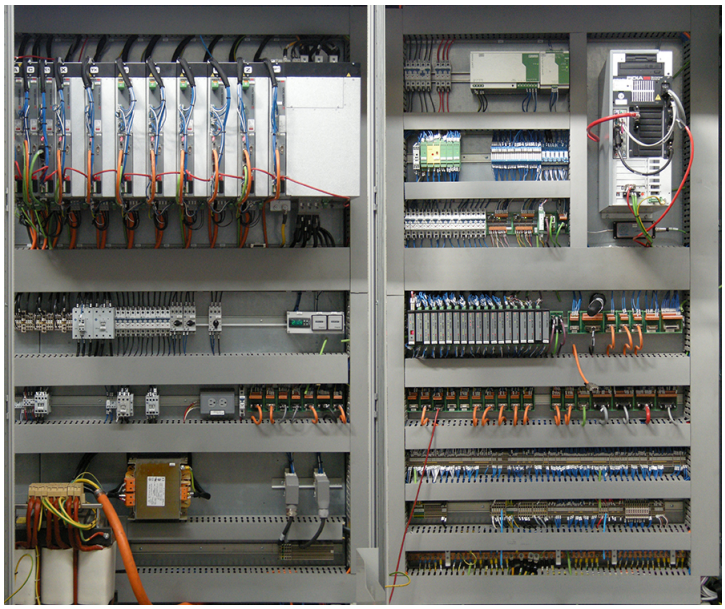


Figure 2.1: Cabinet of a computer numerical control (GTF).

The power converter length is the mechanical parameter that differs between all the products of the XPOWER family. The length value indices the converter name and its current rating. For example, XP50 is a converter which presents a length of 50 mm and a nominal current of 10 A, while the XP100 presents a length of 100 mm and a rated current of 30 A.

2.2.1 XPOWER converters

The XPOWER converters are composed of two separated electronic boards: the control and the power board. From Fig. 2.2 two electronic boards can be noticed: the smaller one is the control board (at the right side) while the bigger one is the power board.

A schematic representation of how these two boards work together is represented in Fig. 2.3. In these equivalent schemes, the measurement conditioning circuit and the control circuit functionalities are graphically described.

2.2.2 Control board

In Fig. 2.4, a control board called FDIB is shown. Two electronic devices are highlighted in the figure: a Digital Signal Processor (DSP) and a Field Programmable Gate Array (FPGA). These two components are key elements in the application of motor control and their tasks are described below.

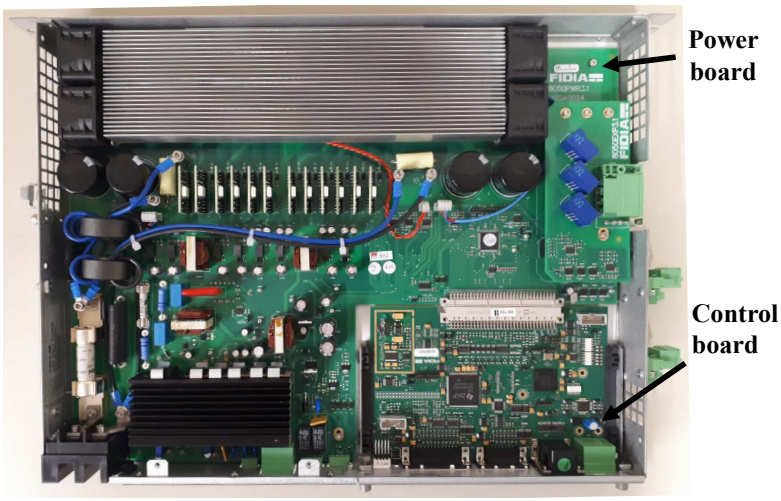
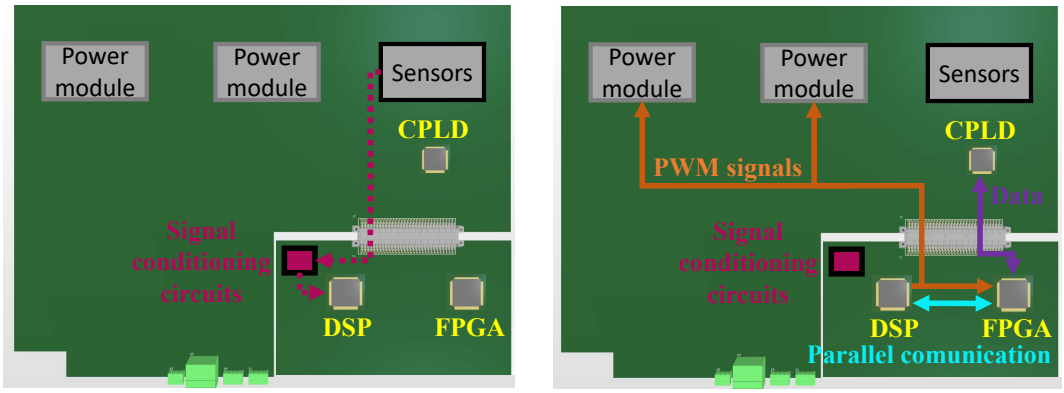


Figure 2.2: A XPOWER converter: XP50-30-D with connected an FDIB4 control board.



(a) (b)

Figure 2.3: Schematic converter operation of XPOWER converter family. (a) Measurement conditioning circuit, (b) PWM and communications signals.

Tasks conducted by the DSP

Tasks conducted by the DSP are summarized as follows.

- Position or speed controls of the motors are done. So, it is obvious that current, speed and position controls together with flux observers are performed. Moreover, multiple stages of notch and low pass filters can be implemented in the control scheme by permitting to avoid mechanical resonance issues caused by the mechanical load.
- As evident from the schematic representation in Fig. 2.3(b), the duty cycles generated by the current control are directly sent to the power board, thus

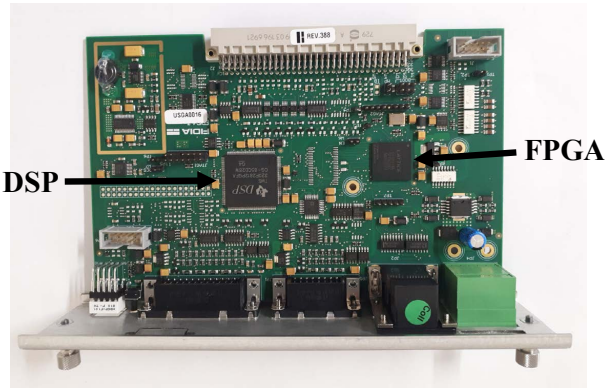


Figure 2.4: Control board: FDIB4.

to the drivers of the power modules, and to the FPGA present in the control board.

- As illustrated in Fig. 2.3(a), inverters currents, bus voltage, and heat sink temperature measurements signal come from the power board. These signals are conditioned on the control board, then the measurements are acquired by the Analog to Digital Converters (ADC) converter of the DSP.
- Important information, as mechanical angles of the motor and the speed, are sent by FPGA to the DSP. DSP communicates with the FPGA by using a parallel communication.

Tasks conducted by the FPGA

Duties conducted by the FPGA are summarized below.

- The FPGA communicates with the machine control unit. Position or speed references are sent by a master, while the FPGA sends back all the measurements by permitting to close the higher level control loops.
- Positions derived by all the position transducers are acquired by the FPGA.
- The FPGA communicates with the Complex Programmable Logic Device (CPLD) present at the power board side as can be noticed from Fig. 2.3(b). Communications about faults and protections (e.g. overcurrents etc. etc.) at the inverter side are managed by the CPLD.

2.2.3 Power boards

In this subchapter, the technical details of two power converters of the XPOWER family are given (XP100-75-A and XP50-30-D).

Figure 2.5: XPOWER converter model XP100-75-A.

XP100-75-A

In Fig. 2.5, an XP100-75-A inverter is shown. This inverter is a standalone converter. Inside, a three-phase half controlled rectifier and a three-phase inverter are present. The converter is composed of the sequent important components:

- currents, voltage and temperature sensors;
- power fuses;
- high and low voltage Switch Mode Power Supplies (SMPS);
- three-phase half controlled rectifier, which is used also as bus pre-charge;
- three-phase power module (PM75RSD120) with opto-isolator stages;
- switch and diode used from braking purpose;
- cooling system composed of a heat sink and fans;
- bus capacitors;
- CPLD connected to the measurement signals. The CPLD manages the faults of the power converter.

In conclusion, XP100-75-A technical data are listed in Table 2.1. In this table, the data related to the nominal and overload conditions of the converter are shown. The power converter needs to satisfy the overload condition for 10 s every minute. The power converter load profile is depicted in Fig. 2.6.

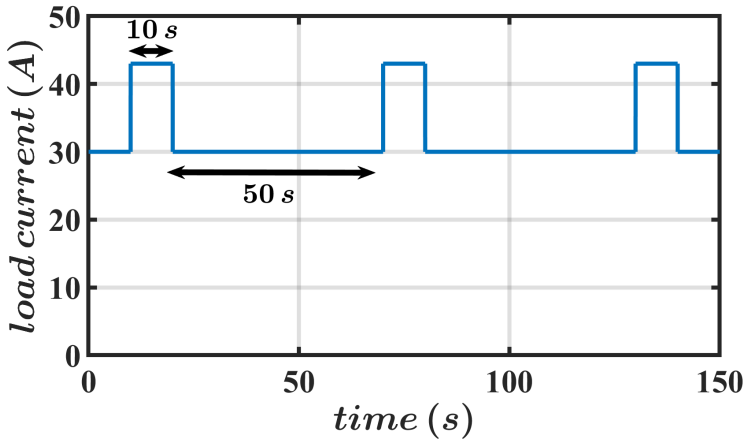


Figure 2.6: Load profile that the power converter needs to satisfy.

Table 2.1: XP100-75-A and XP50-30-D power converters technical data. Switching frequency[1] represents the maximum limit imposed by the heat sink. Switching frequency[2] represents the maximum limit imposed by digital control.

Requirement	Symbol	XP100-75-A	XP50-30-D
Dimensions	H×W×L	440 × 338 × 100 mm	440 × 338 × 50 mm
Number of inverters		1	2
Nominal power	P	15 kW	5 kW
Nominal current	I	30 A	10 A
Overload current	I	42.5 A	14 A
Nominal voltage	V_{dc}	590 V	590 V
Bus capacitance	C_{dc}	0.82 mF	0.22 mF
Ambient temperature	θ_a	40 °C	40 °C
Switching frequency[1]	f_{sw}	8 kHz	8 kHz
Switching frequency[2]	f_{sw}	$4 \div 14$ kHz	$4 \div 5$ kHz

XP50-30-D

The XP50-30-D is represented in Fig. 2.7. This converter is a dual-axis inverter. Inside, two three-phase inverters are present. The power of this converter can only be supplied from the outside (i.e. through the bus bar). The converter is composed of the sequent important components:

- currents, voltage and temperature sensors;
- power fuse;
- high and low voltage Switch Mode Power Supplies (SMPS);

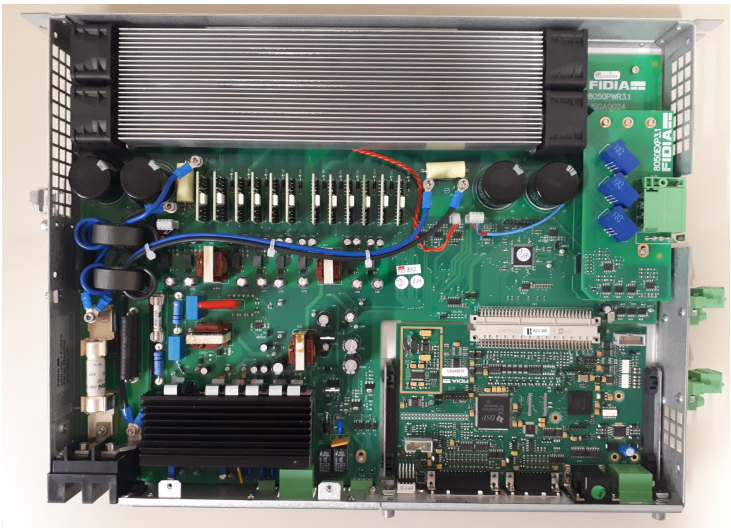


Figure 2.7: XPOWER converter model XP50-30-D.

- two three-phase inverters with the opto-isolator circuits;
- heat sink and fans;
- bus capacitors;
- CPLD connected to the measurement signals. The CPLD manages the faults of the power converter.

In conclusion, XP50-30-D technical data are listed in Table 2.1. In this table, the data related to the nominal and overload conditions of the converter are shown. The power converter needs to satisfy the overload condition for 10 s every minute. The power converter load profile presents the same shape of the load profile shown in Fig. 2.6.

2.3 New converter: XP100-75-D

As described in the introduction, the new power converter needs to satisfy multiple requests. The targets of the new converter are summarized here.

- The converter should be composed of two three-phase inverters. The power rating of each inverter needs to be equal to the power rating of the inverter present inside the XP100-75-A. All the proprieties that must be taken from the previous generation of converters are highlighted in Table 2.1.
- Compatibility from a control point of view is required by the power converter. Thence, the FDIB described in Chapter 2.2.2 needs to be able to control two inverters, as it currently does with the XP50-30-D.

- The converter needs to present compatibility with switches based on all-Si, Si-SiC and all-SiC technologies.
- The converter needs to perform high-resolution computational tasks due to the increase of the switching frequency.
- Additional components are also required by the converter: common mode filters for each inverter and RC filters for EMI purpose.

By virtue of all the specifications defined for this new power converter, a detailed analysis of the schematics of XP50-30-D, XP100-75-A and FDIB4 is required.

2.3.1 Hardware specification

By taking into account all the design targets defined previously, the new power converter specification can be defined as presented in Table 2.2.

Table 2.2: New converter specifications. Switching frequency[1] represents the maximum limit imposed by the heat sink. Switching frequency[2] represents the maximum limit imposed by digital control.

Specifications	Symbol	XP100-75-D
Dimensions	H×W×L	440 × 338 × 100 mm
Number of inverters		2
Nominal power	P	15 kW
Nominal current	I	30 A
Overload current	I	42.5 A
Bus voltage	V_{dc}	590 V
Bus capacitance	C_{dc}	1.5 mF
Ambient temperature	θ_a	40 °C
Switching frequency[1]	f_{sw}	8 kHz
Switching frequency[2]	f_{sw}	$\gg$ 8 kHz

From Table 2.2, it can be noticed that the bus capacitance is roughly double than XP100-75-A converter. In fact, the capacitance has been doubled in order to avoid non-uniform current ripple distribution between other inverters connected in parallel. Details can be found in Chapter 3.

2.3.2 Firmware specification

As can be noticed from Table 2.2, the switching frequencies of the two inverters are equal to 8 kHz. When the PWM carries of the two power converters work in a synchronous way, the equivalent time task seen by the DSP is equal to the

one related to an inverter working at 16 kHz. Anyway, when SiC devices are used the maximum switching frequency can be considerably increased (i.e. more than 20 kHz). This statement corresponds to reduce the computational time presented by the control, thus controller with higher performance is required. Unfortunately, the DSP, that is present on the control board, is only capable to sustain an equivalent switching frequency of less than 14 kHz. Thence, a possible solution to the computational task time issue needs to be found. Field Programmable Gate Array (FPGA) can solve the computational task time issue.

It has been demonstrated that by using FPGA the computational task time can be impressively reduced [28]. A solution to this problem is to move the current control loops from the DSP to the FPGA. Thence, lower speed control loop (i.e. position and speed) can be maintained at a high level. A schematic presentation of the described control hierarchy is depicted in Fig. 2.8.

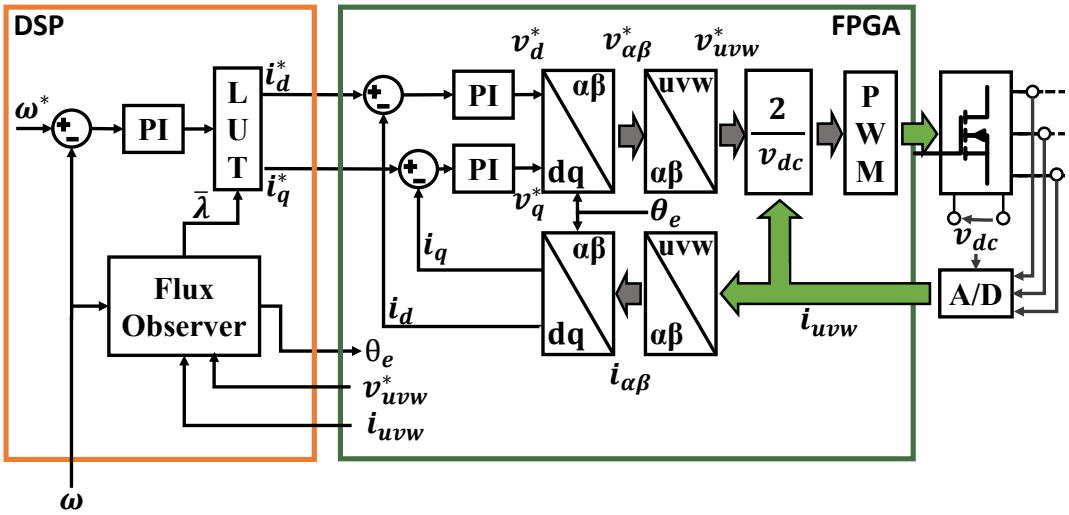


Figure 2.8: Schematic presentation of the control done by FIDIA to the new prototype.

Electronic management and organization of the motor control task

It has been observed previously that the control task needs to be done by an FPGA when high-switching frequency is required. The FPGA of the control board (FDIB) does not contain enough LookUP Tables (LUTs) because its dimension is optimized only for communication purpose and mechanical angle measurement. As a consequence, a possible solution is to replace the CPLD, mounted on the power board (see Fig. 2.3(b)), with an FPGA.

By applying this replacement, the first issue that can be encountered is the retrofit propriety, defined previously, that is not satisfied. In fact, as explained

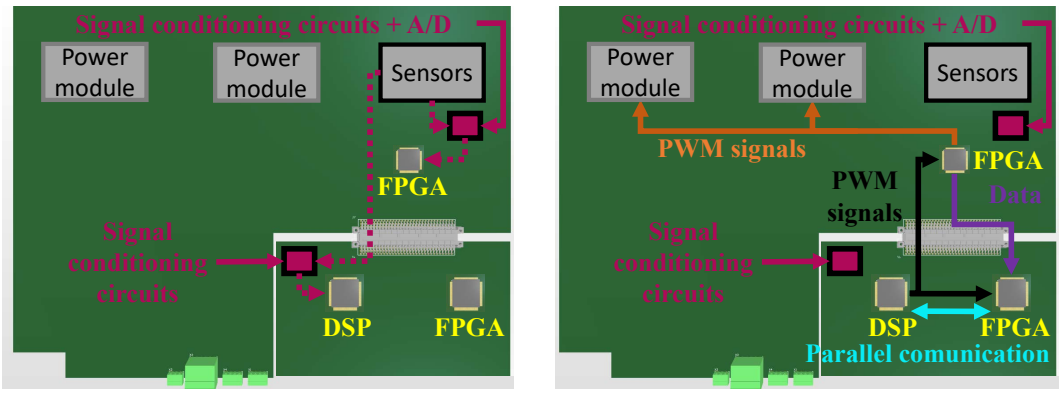


Figure 2.9: Schematic novel converter operation controlled in the standard way (a) Measurement conditioning circuit, (b) PWM and communication signals.

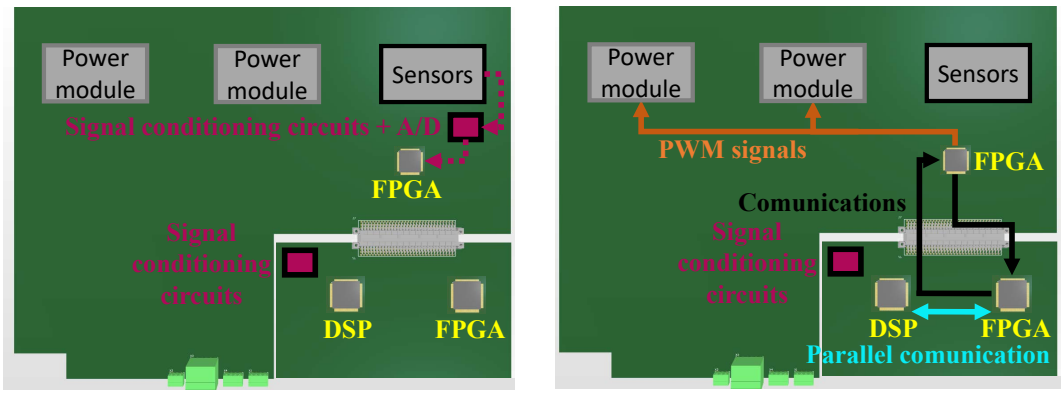


Figure 2.10: Schematic novel converter operation controlled by applying the control scheme shown in Fig. 2.8. (a) Measurement conditioning circuit, (b) PWM and communications signals.

previously the DPS controls directly the switches of the inverters (see Fig. 2.3(b)), but this goes in contrast because the FPGA also wants to control directly the power modules. A solution to the retrofit action is to send the DSP signals directly to the FPGA place on board as schematically shown in Fig. 2.9(b). In case that the converter needs to be controlled by the DSP, DSP signals can be pass through the FPGA and the signals can be sent directly to the power modules. In addition, in order to maintain the compatibility, the FPGA present on the power board can be programmed by using the firmware implemented for the CPLD.

When the converter is controlled by the FPGA, communication between the DSP and the FPGA is required as schematically represented in Fig. 2.8. Thence

by observing Fig. 2.10(b), the pins of the DSP are programmed in three states and communication between the two FPGAs can be established. The data required by the DSP are taken back from the FPGA placed on the control board, using the existing parallel communication presented previously.

In order to permit the control task by the FPGA, additional components are required on the power board. The converter variables (i.e. currents, voltage, and temperature) are needed by the FPGA, thence Analog to Digital Converters (ADCs) with good resolution can be used. These ADCs need to be connected directly to the FPGA as can be noticed from the equivalent scheme shown in Fig. 2.10(a).

2.4 Conclusions

Features of the XPOWER family have been given with particular attention brought to the power and the control boards. Design specifications of the new converter, that needs to be compatible with all-Si, Si-SiC and all-SiC devices, have been given. It has been observed that using SiC devices the control board presents an incompatibility issue caused by the high task time of the DSP. For this reason, it has been decided to introduce a faster logic unit (FPGA), which takes care of the control loops, instead of the DSP. Thanks to this solution two operating modes have been defined.

- When all-Si devices are used in the converter, the DSP can control the power board without problems. This feature becomes important from a retrofitting point of view.
- When Si-SiC and all-SiC are used and consequently the switching frequency is increased, the FPGA can take under its proprieties low-level control loops while the high-level control loops are done by the DSP.

Chapter 3

Converter design, realization, and preliminary tests

3.1 Introduction

In Chapter 2, dual-axis converter specifications have been defined in order to have a converter compatible with the family products (i.e. XPower). Starting from these specifications, the converter schematic has been realized by considering all these aspects: control, thermal, power, measurements, control and power supplies. Furthermore, the converter has been developed with the aim to be compatible with power devices based on all-Si, Si-SiC and all-SiC. From the schematics, a Printed Circuit Board (PCB) has been realized by considering also the mechanical constrains imposed by the company.

In this chapter, important details about the converter design process are provided. Moreover, tests and problems found during the tests of the PCB are described and explained.

3.2 Dimensioning of the FPGA

As explained in Chapter 2, SiC devices permit to increase the converter switching frequency. Thence, controller with high computing capacity is required, if you want to obtain the benefit of having a higher bandwidth [29, 30]. For reasons of versatility required during the project, it was decided to use a Field Programmable Gate Array (FPGA). Different FPGAs are present on the market, thence the cheapest one needed to be chosen. In order to choose an FPGA between all the producers a VHDL firmware, which contains a tentative firmware, was created, synthesized and implemented in different brands of FPGA (Xilinx, Altera, Lattice).

3.2.1 Firmware

The VHDL firmware used for evaluating the FPGA size needs to be able to manage a converter composed of two three-phase inverters.

Firmware improvement

The developed firmware is a continuation of the work done by other colleagues from Politecnico di Torino in the past [31, 32, 33]. The codes are based on a fixed-point convection which present word length in bits of 16. Important modifications have been conducted during my Ph.D. career and some of them are described below.

- The measurement unit manages the communication process with external Analog to Digital Converters. Multisampling technique is applied by this unit, by permitting to increase the bandwidth of the current loops and avoid possible measurement noise issues [29, 30]. By taking the existing unit, interleaved measurements of the currents were implemented in the nine-phase interleaved boost converter application [34].

- A single current loop (with feed-forward, anti-wind-up, and voltage normalization) was written. This code has been successfully demonstrated in the application of a nine-phase interleaved boost converter used for dynamic wireless power transfer [34].

- Voltage control (with feed-forward and anti-wind-up) was written. This code can be used for Active-Front-End application (control the bus voltage) or in the wireless power transfer in combination with a resistance control. This code has been successfully demonstrated in the application of a nine-phase interleaved boost converter used for dynamic wireless power transfer [34].

- The PWM unit takes the index modulations and convert them in the switches' signals. This PWM unit has been improved by removing some code bugs (e.g. issue presented at extreme duty cycle values). In addition, phase-shifting between the PWM carriers was implemented. The shifting propriety has been successfully demonstrated in the application of a nine-phase interleaved boost converter used for dynamic wireless power transfer [34] and in the application of a three-3-phase motor control [35].

- A communication unit, which permits the communication with a sBrio 9651 programmed in LabVIEW environment [36], was written.

- A unit, that manages the internal memory (RAM) of the FPGA, was written. The sequent unit permits to use the memory as a First Input First Output (FIFO) buffer. All the measurements and internal variables of the FPGA can be acquired, then for example in case of fault these variables can be observed.

Firmware components

The size analysis of the FPGA is done using a tentative firmware composed of the units listed below.

- A clock unit is implemented. This unit takes the external clock and provides a series of clock signals used by all the logic. In addition, this unit manages the interrupts of the system.
- Protection manager and state machine are implemented. The state machine has to manage basic operations such as sensor offset, bootstrap operation, faults manager, acquisition of the constant used by the control during the startup of the drive, etc. etc. The protection manager has the task to bring the converter in a safe condition when a fault is detected.
- A measurement unit which manages six currents (three for each inverter), one voltage and one temperature measurements has been used.
- A communication unit, which manages the communication between the master and the slave is used. All these data are multiplied by two because two inverters are controlled. The data sent from the master to the slave are: current references (i.e. i_d^*, i_q^*), electric angle references (i.e. θ_e), state of the master, etc. etc. The data sent from the slave to the master are: measured current (i.e. i_1, i_2, and i_3), bus voltage v_{dc}, duty cycles (i.e. m_1, m_2, and m_3), state of the slave, etc. etc.
- Two Clarke and Parke transformations of the currents are implemented. Two Clarke and Parke transformations of the reference voltages (obtained from the current control) are implemented.
- Two Lookup tables with implemented the sin and cos values used by the Parke transformations are implemented. Using these tables, the conversion from degree to sin and cos can be achieved.
- Two third harmonic injection units are adopted. By using these units, the fundamental output voltage can be increased for the same bus voltage.
- Two *dq* current loops have been implemented. Each current loop presents the feed-forward, anti-windup and the voltage normalization.

3.2.2 FPGA choice

By knowing the number of pins of the application, thin quad flat pack package was preferred instead of ball grid array package because:

- the board size is too big because it needs to contain control and power stages, thence mechanical stresses due to flexing and vibration can be presented [37];
- higher cost;
- difficulty in the inspection of soldering faults is present.

A package, that presents 144 pins, was selected. Between all the FPGAs presented in the market at that time (2016), the one that fits the required code was 10M25SCE144. 67 % of the resources were occupied by the code.

3.3 Thermal sizing of the converter

3.3.1 Converter thermal design methodology

The following steps need to be followed in the thermal design of a power converter:

1. At first, switches with Safe Operating Area (SOA) compatible with current and voltage of the power converter need to be identified.
2. Once the devices are identified their power losses need to be evaluated. Therefore, conduction and switching losses are required. These losses can be found by means of simulation tools or formulae.
3. By knowing the devices losses, it is possible to choose at first approximation a heat sink compatible with the dissipate power.
4. Using the power losses and the thermal equivalent circuit of the cooling system, it is possible to verify the maximum junction temperature of the devices.
5. This temperature is compared with the maximum temperature rating. If the temperature is higher the process needs to be restarted from point "1" or from point "3". If the temperature is lower the thermal design is complete.

Between all the switch configurations (see Fig. 1.1), all-Si presents higher losses with respect to Si-SiC and the all-Si devices. For this reason, the thermal design has been done by considering all-Si technology. As mentioned above, the power converter is composed of two inverters. Thus, the losses are derived by considering the two inverters based on all-Si devices. In this chapter, the two inverters are marked with the letter "A" and with the letter "B".

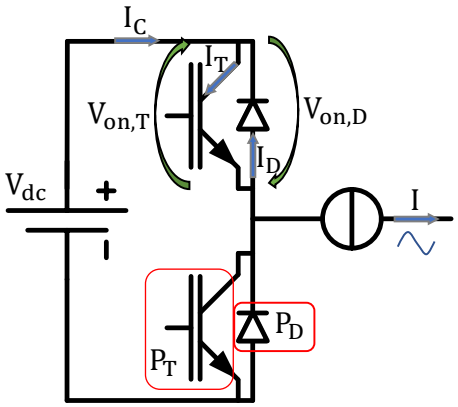


Figure 3.1: Inverter leg based on all-Si configuration device.

The conduction losses

The conduction losses are caused by the switches ON voltage drops. Two characteristic features can be distinguished using all-Si, Si-SiC and all-SiC devices: presence or not of reverse conduction property [11]. The power losses of all-Si are required, thus the inverter leg behavior when reverse conduction propriety is present it is not considered in the design. When reverse conduction is not present (i.e. using Si-SiC and all-Si), the switches voltage drops can be represented by the piecewise linear model

$$V_{on,T(I_T)} = V_{th,T} + R_{d,T} I_T \tag{3.1}$$

$$V_{on,D(I_D)} = V_{th,D} + R_{d,D} I_D. \tag{3.2}$$

where V_{th} represents the threshold voltage and R_d the differential resistance [38]. These parameters are highly temperature dependent (i.e. dependency caused by the junction temperature variation), then the worst-case scenario needs to be considered during the thermal design of the converter.

Using the ON voltage drop model, it is possible to define the AC conduction losses [2, 38, 39]. AC power losses, of the inverter leg depicted in Fig. 3.1, can be calculated for the switch and the diode by using:

$$P_{c,T} = \sqrt{2} I V_{th,T} \left(\frac{1}{2\pi} + \frac{M cos\varphi}{8} \right) + 2 I^2 R_{d,T} \left(\frac{1}{8} + \frac{M cos\varphi}{3\pi} \right) \tag{3.3}$$

$$P_{c,D} = \sqrt{2} I V_{th,D} \left(\frac{1}{2\pi} - \frac{M cos\varphi}{8} \right) + 2 I^2 R_{d,D} \left(\frac{1}{8} - \frac{M cos\varphi}{3\pi} \right) \tag{3.4}$$

where M is the index modulation, I is current RMS value and φ is the phase between the current and the voltage. Eq.(3.3) and (3.4) are valid when the sequent hypotheses are respected.

- When the device is off, no losses are present because the component is considered an ideal open circuit.

- The current of the leg is a sinusoid. Accordingly, the ripple current caused by the PWM modulation is neglected. If the current ripple is present the conduction losses will be increased.
- The inverter works in continuous modulation mode [39].
- The third harmonic voltage is not inserted in the control. The conduction losses formulae valid when the third harmonic voltage is injected in the voltage reference can be found in [39].
- The fundamental electrical frequency of the current (f_e) is high enough to permit the junction temperatures of the devices to reach a steady state temperature. Therefore, the threshold voltage $V_{th,x}$ and the differential resistance $R_{d,x}$ of the devices can be considered constant.
- Turn-on and turn-off time of the switches and diodes can be neglected.

The switching losses

The switching losses are present when the inverter leg changes its states. In AC, the current changes periodically, thus the switching losses change too. Considering the energy loss linearity, the equivalent energy loss is equal to the energy loss when the current mean value is commutated [38]. Therefore, fixing the switching frequency (f_{sw}) the switching losses can be calculated by:

$$P_{sw,T} = (E_{on(\sqrt{2}I/\pi)} + E_{off(\sqrt{2}I/\pi)})f_{sw} \tag{3.5}$$

$$P_{sw,D} = (E_{rr(\sqrt{2}I/\pi)})f_{sw} \tag{3.6}$$

where E_{on} is the switch turn-on energy in function of the current, E_{off} is the switch turn-off energy in function of the current and E_{rr} is the reverse recovery charge in function of the current. The defined formulae are valid when the sequent hypotheses are respected.

- The leg current is sinusoidal.
- The inverter needs to work in continuous modulation. Discontinuous modulation techniques reduce switching losses [39].
- The electrical frequency is high enough to permit a steady-state junction temperature. Therefore, the turn-on, turn-off, and reverse recovery charge losses as a function of the current can be considered constant.

3.3.2 Converter thermal sizing

The power converter needs to satisfy the load profile defined in Fig. 2.6, that corresponds to the spindle load profile. As can be noticed from this figure, two different load conditions are present, therefore the power module losses for both the cases are required. As mentioned before, the thermal design is conducted for all-Si switch configuration because it presents the higher losses.

Power module choice

As explained in Chapter (2), power modules made of all-Si, Si-SiC and all-SiC were required with the same package. For this purpose, power modules with the sequent declared Safe Operating Area (SOA) were identified: 75 A x 1200 A. The package of these power modules is shown in Fig. 3.2. Inside this power module, three inverter legs are present. As can be noticed from the figure, the output terminals of each leg are indicated with U, V, and W, while the bus terminals are marked with P and N. Details of the power modules are given here.

- All-Si configuration: PM75CL1A120 of Mitsubishi was chosen. This power module was commercially available at the moment of the design.
- Si-SiC configuration: PMH75CL1A120 of Mitsubishi was chosen. This power module was not commercially available at the moment of the design because it was a tentative device.
- All-SiC configuration: PMF75120S002 of Mitsubishi was chosen. This power module was not commercially available at the moment of the design because it was a tentative device.

The selected power modules are Intelligent Power Modules (IPMs). By adopting these devices, the sequent advantages can be exploited:

- additional driver circuits are not required. In fact, inside the power module the gate turn-on and turn-off circuits are already implemented;
- the protection circuit is not required. The over-current fault with the soft shut-down is present;
- under-voltage and over-temperature protections are present;
- a high degree of integration in comparison to other power module solutions can be achieved [2].

By virtue of these features, the sequent power converter features can be improved: maintenance, reliability and debugging. The disadvantages of this technology are the sequent: switching speed cannot be modified and special logic functions cannot be implemented.

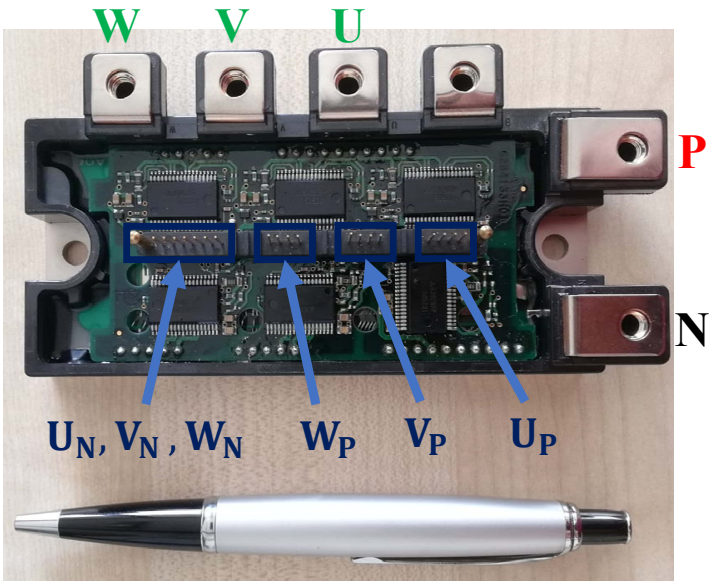


Figure 3.2: Three-phase intelligent power module (PMF75120S002).

Conduction loss calculation of device based on all-Si

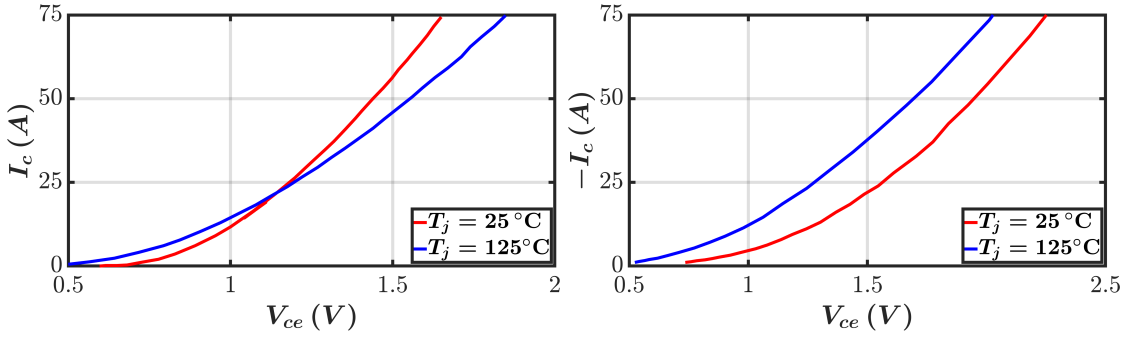


Figure 3.3: ON voltage drops of the devices present inside the power module PM75CL1A120, where T_j are the device junction temperatures. (a) Si IGBT and (b) Si diode.

The ON-voltage drops of the components are required, in this way the $V_{th,x}$ and $R_{d,x}$ parameters can be derived, where x indexes the transistor "T" or the diode "D".

In Fig. 3.3(a) and Fig. 3.3(b), Si IGBT and Si diode forward characteristic taken from the datasheet are depicted. As can be noticed from these figures, traces of ON-voltage drop of the switches at 25 °C and 125 °C are illustrated. Between the two curves, the worst-case scenario for both the devices has been chosen during the

heat sink design:

- conduction parameters of the Si IGBT are derived at 125 °C;
- conduction parameters of the Si diode are derived at 25 °C.

From Fig. 3.3(a) and Fig. 3.3(b) the power converter parameters are derived by applying a linearization near the inverter leg nominal current. The parameters obtained from the linearization process are resumed in Table 3.1.

Table 3.1: Piecewise voltage drop of the switches present inside the PM75CL1A120 power module.

	$V_{th,x}$ (V)	$R_{d,x}$ (mΩ)
Si IGBT	0.88	13.8
Si diode	1.36	11.8

Using eq. (3.3), eq. (3.4) and the table parameters, the conduction losses of the switch and the diode are calculated for the two-operating condition of the inverter: nominal current (30 A) and overload current (42.5 A). The derived power losses are resumed in Table 3.2.

Table 3.2: Calculated conduction losses of Si IGBT and Si diode ($M = 0.9$, $cos\varphi = 0.9$).

I	$P_{c,T}$	$P_{c,D}$
30 A	16.2 W	2.4 W
42.5 A	26.16 W	3.6 W

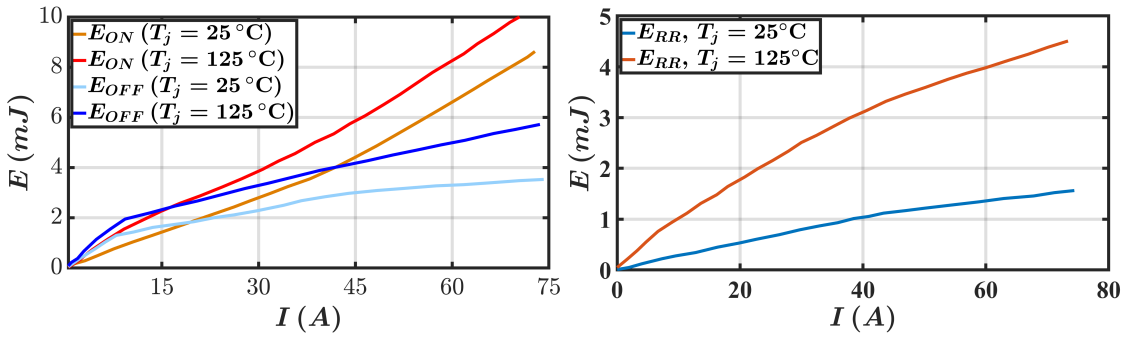
Switching losses calculation of device based on all-Si

The switching losses are derived from the switching curves represented in Fig. 3.4(a) and Fig. 3.4(b) (i.e. found in the device datasheet). The losses are calculated by following the methodology proposed in Chapter 3.3.1 and are resumed in Table 3.3. In this table, the switching loss of the diode and the IGBT at two different operating conditions are derived (see Fig. 2.6).

Power module losses

The IGBT and the diode power losses are obtained by summing the conduction and the switching losses as shown in:

$$P_{T(I)} = P_{c,T} + P_{sw,T} \tag{3.7}$$



(a) (b)

Figure 3.4: Switching losses of the devices present inside the power module PM75CL1A120, where T_j is the device junction temperature. (a) Si IGBT and (b) Si diode.

Table 3.3: Switching losses (V_{dc} = 600 V, f_{sw} = 8 kHz).

I	$P_{sw,T}$	$P_{sw,D}$
30 A	35.4 W	6.9 W
42.5 A	42.6 W	9.9 W

$$P_{D(I)} = P_{c,D} + P_{sw,D}. \tag{3.8}$$

Calculated conduction and the switching losses have been summed by obtaining the total power loss of each switch (i.e. IGBT and diode). These results are resumed in Table 3.4.

Table 3.4: Conduction, switching and total losses (V_{dc} = 600 V, M = 0.9, $cos\varphi$ = 0.9 and f_{sw} = 8 kHz).

I	$P_{c,T}$	$P_{c,D}$	$P_{sw,T}$	$P_{sw,D}$	P_T	P_D
30 A	16.2 W	2.4 W	35.4 W	6.9 W	51.6 W	9.3 W
42.5 A	26.16 W	3.6 W	42.6 W	9.9 W	68.76 W	13.5 W

The total power losses dissipated by the power modules "A" and "B" are calculated by multiplying the switch and the diode power losses by six as shown in

$$P^A_{loss} = 6(P^A_{sw,T} + P^A_{sw,D} + P^A_{c,T} + P^A_{c,D}) = 6(P^A_T + P^A_D) \tag{3.9}$$

$$P^B_{loss} = 6(P^B_{sw,T} + P^B_{sw,D} + P^B_{c,T} + P^B_{c,D}) = 6(P^B_T + P^B_D). \tag{3.10}$$

Using the data presented in Table (3.4) and the formulae (3.9) and (3.10) the module power losses can be evaluated.

The two power modules share the same heat sink, thence the power dissipated by the heat sink can be evaluated as the sum two power terms:

$$P_{loss} = P^{A}_{loss} + P^{B}_{loss}. \tag{3.11}$$

Heat sink power losses profile

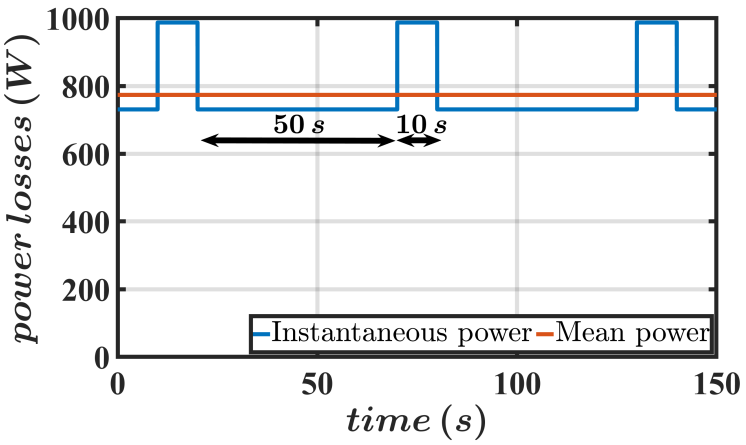


Figure 3.5: Heat dissipated by two inverters when the load current profile is imposed ($f_{sw} = 8$ kHz, $V_{dc} = 600$ V, $cos\varphi = 0.9$ and $M = 0.9$).

Using the power losses summarized in Table 3.4, the power profile dissipated by the heat sink can be defined using (3.11). The power that the heat sink needs to dissipate is given in Fig. 3.5. As can be noticed from this figure, the power losses trend corresponds to the load profile defined in Fig. 2.6. Analyzing the two figures, it can be noticed that an increase in the inverter current of 41 % corresponds to an increase in the losses of 36 %. Two heat sink sizing methodologies can be followed:

- design the heat sink by considering the power loss at the overload condition;
- design the heat sink by considering the mean value of the power loss of the converter.

The first solution involves an oversizing of the power converter while the second solution permits to optimize the size of the converter. Thence, in order to do not oversize the heat sink the mean power loss method is followed. The mean value has been evaluated by means of

$$P^{A}_{loss(avg)} + P^{B}_{loss(avg)} = \frac{5}{6}(P^{A}_{loss(30)} + P^{B}_{loss(30)}) + \frac{1}{6}(P^{A}_{loss(42.5)} + P^{B}_{loss(42.5)}) \tag{3.12}$$

and this value is depicted in red in Fig. 3.5. The equivalent power loss value is equal to 773 W.

In conclusion, three power losses have been calculated and can be used in the sizing process of the heat sink:

- power loss at the nominal load condition ($P_{loss(30\,\mathrm{A})}$): 731 W;
- power loss at the overload condition ($P_{loss(42.5\,\mathrm{A})}$): 987 W;
- mean power loss when the spindle load profile is selected ($P_{loss(avg)}$): 773 W.

3.3.3 Heat sink choice

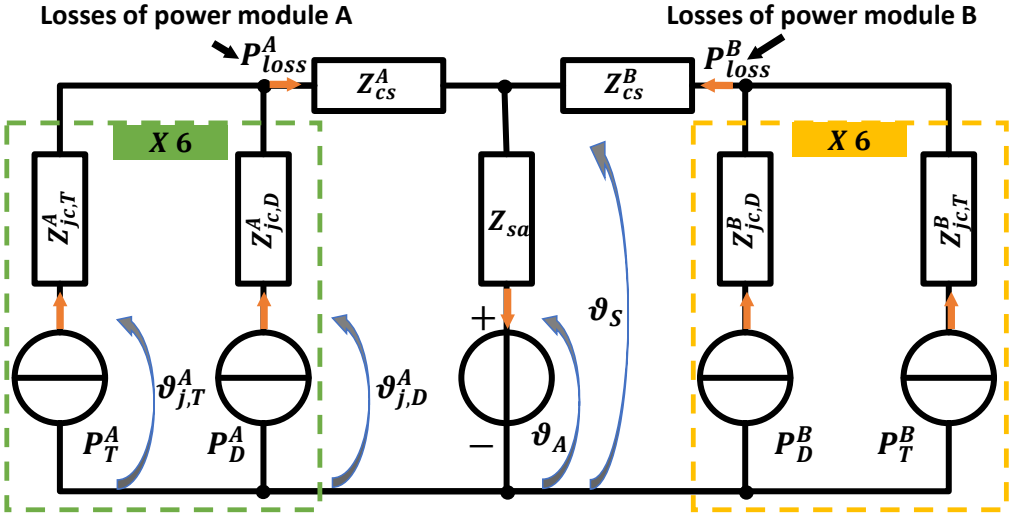


Figure 3.6: Equivalent thermal circuit of the converter. In the dashed rectangle region, the components of each inverter are presented.

The equivalent thermal circuit of the converter is required in order to evaluate the junction temperature of the devices. These temperatures are dependent on the power losses and the thermal impedance net of the power converter.

A simplified thermal model of the designed converter, which can be used for the heat sink design, is shown in Fig. 3.6. The voltages of the circuit are temperatures (e.g. θ_s), the currents are losses (e.g. P_T^A) and the impedances are thermal impedances. The elements of the equivalent thermal circuit have been identified using the apexes "A" and "B". Elements of the thermal equivalent circuit shown in Fig. 3.6 are described below.

- Current generators represent the losses of each device. P_T^A is the loss term of the transistor and P_D^A is the loss term of the diode. In particular, in the equivalent circuit, losses of each inverter have been introduced. Inside the dotted rectangles, "X 6" has been placed because it represents the six diodes and six IGBTs of each power module.

- $Z_{jc,T}$ is the switch junction-to-case thermal impedance, while $Z_{jc,D}$ is the diode junction-to-case thermal impedance.
- The case-to-sink (i.e. thermal resistance cause by the thermal interface between the power module and the heat sink) is represented by the impedance Z_{cs}.
- The thermal impedance of the heat sink is Z_{sa}, where the subscript term "a" represents the ambient. Anyway, this parameter is influenced by the power module displacement, then this value needs to be carefully evaluated.
- The ambient temperature is fashioned by means of a voltage generator (θ_A).

Conversions of thermal impedances into resistances and power dissipation trends into its average values are required (e.g. $Z_{sa} = R_{sa}$). In order to do not oversize the heat sink for the overload condition the temperature was evaluated for the average condition, the sequent assumptions are applied.

- The temperature variation seen by the heat sink is caused by the mean value (avg) of the dissipated power as described in:

$$\Delta\theta_{sa} = (P^A_{loss(avg)} + P^B_{loss(avg)})R_{sa} = (P_{loss(avg)})R_{sa} \tag{3.13}$$

  where $P^A_{loss(avg)}$ and $P^B_{loss(avg)}$ are the average power dissipated by the heat sink when the load profile is applied.

- The temperature variation seen by the thermal resistance of the case-to-sink (R_{CS}) is caused by the peak power of the load profile as described in:

$$\Delta\theta_{cs} = P^A_{loss(42.5\text{ A})}R^A_{cs}. \tag{3.14}$$

  where P^A_{loss} is the maximum power dissipated by the power module "A". The sequent hypothesis has been imposed for this reason: 10 s of peak power (when the converter works at 42.5 A) imposed by the converter is a time laps much major than the typical constant time of this thermal impedance (Z_{cs}).

- The temperature variations seen by the thermal resistance of the junction-to-case are caused by the peak power of the load profile as described in:

$$\Delta\theta_{jc} = P^A_{T(42.5\text{ A})}R^A_{jc,T} \tag{3.15}$$

  where P^A_T is the power loss of the device. The switch temperature was considered instead of the diode because its power loss is higher. The peak power has been selected because 10 s of peak power imposed by the converter is a time much major than the typical constant time of this thermal impedance ($Z_{jc,T}$).

Finally, the junction temperature of the switch, when the hyphothesis described previously are applied, is represented by:

$$\begin{aligned} \theta_{j,T} &= \theta_A + \Delta\theta^A_{jc,T} + \Delta\theta^A_{cs} + \Delta\theta_{sa} = \\ &= \theta_A + P^A_{T(42.5\text{ A})}R^A_{jc,T} + P^A_{loss(42.5\text{ A})}R^A_{cs} + (P^A_{loss(avg)} + P^B_{loss(avg)})R_{sa} \end{aligned} \tag{3.16}$$

Imposing the maximum junction temperature of the device ($\widehat{\theta}_{j,T}$) is possible to evaluate the required thermal resistance of the heat sink.

As described in Chapter 3.3.2, the IPM has an internal temperature protection circuit. Junction over temperature protection is activated when the temperature is higher than 135 °C than the maximum temperature has been imposed equal to 125 °C, in this way overtemperature trigger, owing to temperature ripple, can be avoided. Considering the thermal circuit and knowing all the circuit parameters, it is possible to define the maximum permitted thermal resistance (R_{SA}) as shown in:

$$R_{sa} = \frac{\widehat{\theta}_{j,T} - \theta_a - P^A_{T(42.5\text{ A})}R^A_{jc,T} - P^A_{loss(42.5\text{ A})}R^A_{cs}}{(P^A_{loss(avg)} + P^B_{loss(avg)})}. \tag{3.17}$$

The permissible maximum heat sink resistance is equal to 42 °C/kW. Knowing the

Table 3.5: Thermal resistances presented by all-Si power module (PM75CL1A120).

	R_{jc} (°C/W)	R_{sc} (°C/W)
Si IGBT	0.21	0.038
Si diode	0.36	0.038

required heat sink thermal resistance, and drive's maximum size, multiple combinations of heat sink, and fans were compared [40]. The solution, that was chosen, is composed of an aluminum heat sink (310 mm × 126 mm plan area ×62 mm height, 21 fins) and two ultra-fast fans (9GV0624P1M03). Ultra-fast fans were chosen by permitting to decrease the equivalent thermal resistance. Furthermore, these two fans give the possibility to control their speeds.

In order to see if the heat sink was correctly chosen, thermal simulations of the chosen heat sink and the cooling system were conducted by using finite element software for thermal analysis. The simulation was conducted by applying two heat sources to the heat sink. Thence, by knowing the power dissipation profile and using the thermal circuit shown in Fig. 3.6 the junction temperature could be derived. At first, steady state simulation was conducted by considering the power loss mean value (i.e. for each power module 387 W). Secondly, the system temperatures were taken from the previous simulation, therefore the power dissipation profiles (Fig. 3.5) were applied. From the simulation results, the maximum registered junction temperature was equal to 130 °C, then the maximum temperature limit imposed by the IPM is respected. This temperature corresponds to a heat sink maximum temperature near to 99.5 °C, as can be seen from Fig. 3.7.

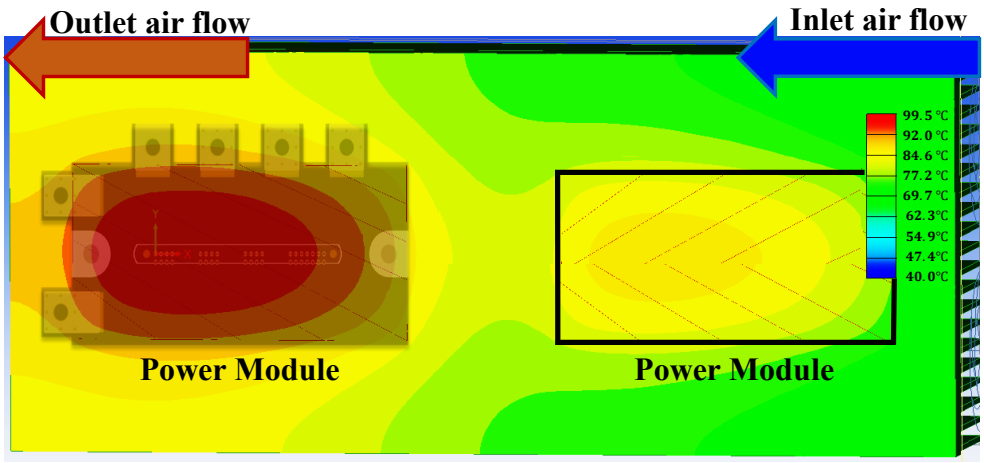


Figure 3.7: Thermal simulation results: heat sink bottom view of the temperature profile when the peak temperature is reached.

3.4 IPM operational circuit

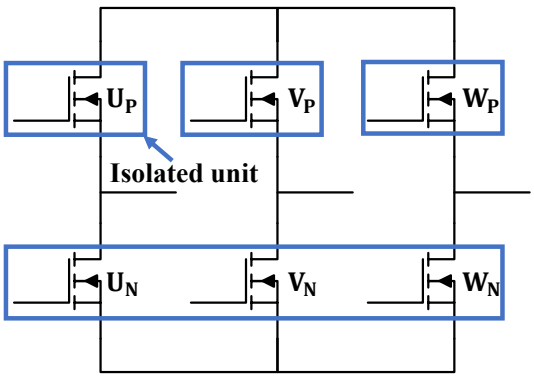


Figure 3.8: Isolated units of the intelligent power module.

The IPM requires isolating power supplies and commands because the circuit internally is not isolated. Four isolation units, which are composed of power supply and control signals, are required for each IPM as schematically represented in Fig. 3.8 in the blue rectangles.

- The upper switches of the power module (U_P, V_P, and W_P) requires three separated units.
- The lower switches of the power module (U_N, V_N, and W_N) requires only one isolated unit.

Inside each stage, a circuit composed of isolated power supplies and communication hardware are needed.

3.4.1 IPM power supply

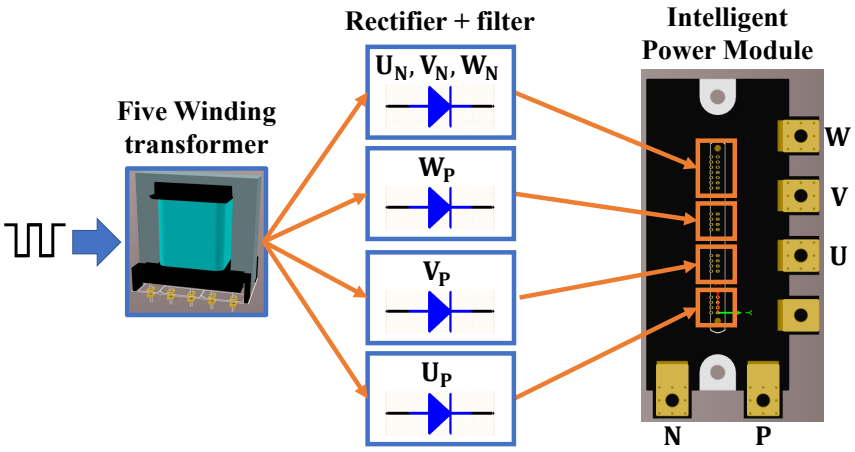


Figure 3.9: Equivalent scheme of isolated power supplies used for the IPM.

A macro scheme of the power supplies used for an IPM is depicted in Fig. 3.9. As can be seen from the figure, four isolated power supplies are required. It is important to note that the power supplies need to be isolated between each other. In Fig. 3.10, a schematic representation of the isolated power supply is given (i.e. U_P). Details of the implemented supply system are listed as follows.

- Five winding transformer is adopted. A negative voltage with respect to the emitter or source of the switch is no required by the IPM, therefore additional windings are not required.
- The primary winding is connected to a low voltage power supply of the board, where this circuit is referred to the ground of the power converter. An alternate voltage is supplied to the winding from a Single-Ended Primary Inductor Converter (SEPIC) converter. It is very important to note that the alternate voltage does not present DC component, therefore this feature permits the transformer core to do not saturate.
- The three windings of the secondary connected to the high side of the power supply are referred to the source or emitter (i.e. according to the chosen switch) of the corresponding switch. The secondary winding connected to the low side of the IPM module is referred to the negative terminal of the bus voltage.
- All the secondary voltages are rectified by means of a half wave rectifier. The

rectifier voltage is then filtered permitting to have a constant voltage. This voltage can be regulated in order to satisfy the IPM required voltage.

- PM75CL1A120 and PMH75CL1A120 need to be supplied by 16 V, while PMF75120S002 needs to be supplied by a diverse voltage (22 V).

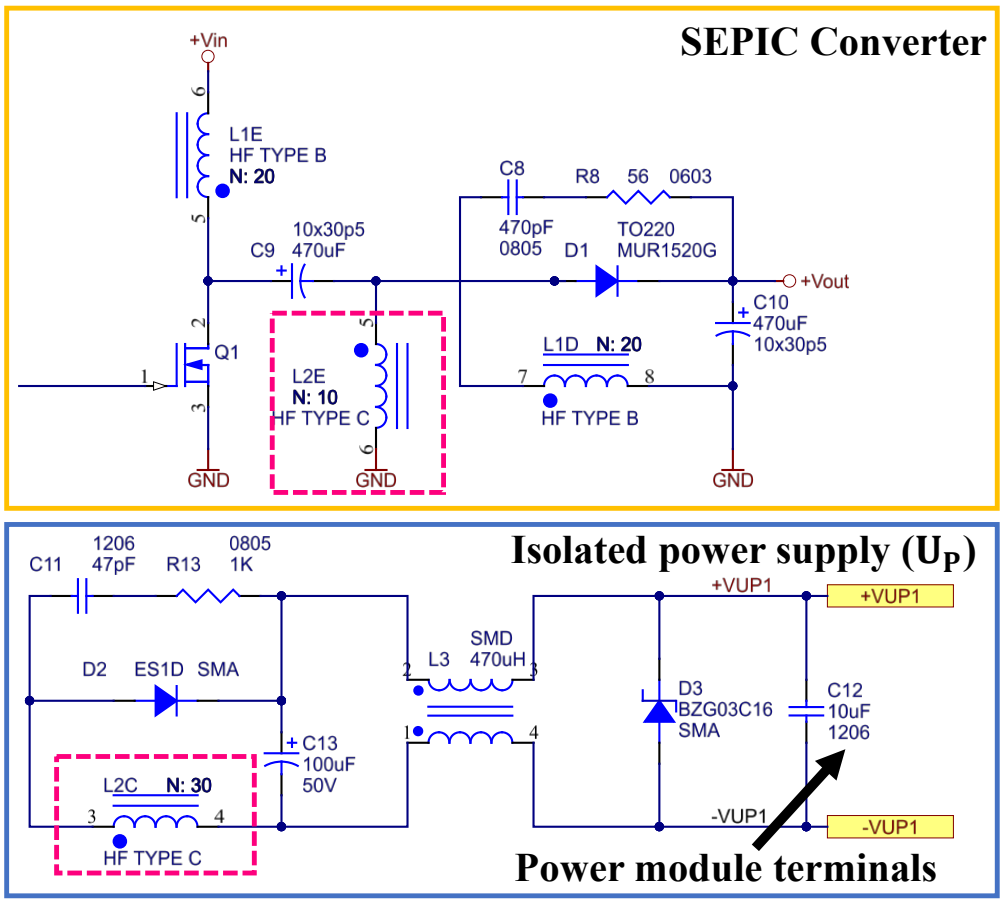


Figure 3.10: Schematic representation of the SEPIC circuit used for the isolated power supplies of the power modules.

3.4.2 IPM control signals

A schematic of the signal conditioning circuits used in this power converter is depicted in Fig. 3.11. In Fig. 3.12, a schematic representation of the isolated control circuit is given (i.e. U_P). Details of the isolated control circuit are listed as follows.

- The commands sent by the FPGA pass through open collector opto-isolators and thence are received by the IPM drivers.

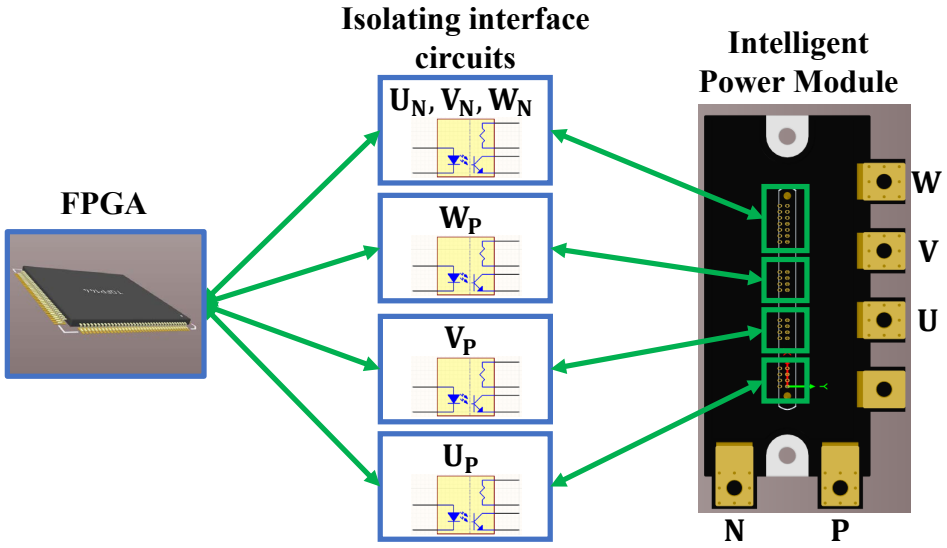


Figure 3.11: Equivalent scheme of isolated control and fault circuits used for the IPM.

- The faults (over-current, over-temperature, under voltage) sent by IPM are received from the FPGA again by means of open collector opto-isolators.
- The opto-isolators needs to present a high common mode transient rejection value. This feature is required because high dv/dt transient can introduce parasitic current which can trigger unintentional turn-on or turn-off of the LED [15]. Isolated interface circuits are based on Si87xx device. This device presents higher common-mode transient immunity with respect to standard opto-isolators ($> 50\,\mathrm{kV}/\mu\mathrm{s}$). Furthermore, a very small propagation delay between input and output signal is guaranteed by this device ($30\,ns$).

3.5 Converter capacitors

Multi-axis applications normally use a central DC power supply which is shared by a certain number of axes (i.e. inverters). Therefore, the ratio I_{dc}/C (i.e. DC current drained by the converter and converter capacitance) should be identical for all the converters connected in parallel (i.e. considering the same product family), thus permitting retrofit and avoiding non-uniform current ripple distribution between themselves. The converter needs to sustain the current ripple of the two inverters and of the rectifier stage. The capacitor RMS current caused by the

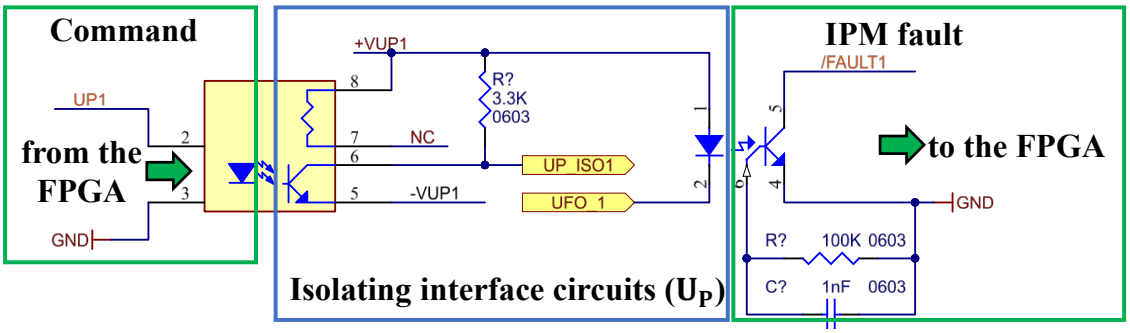


Figure 3.12: Schematic representation of the isolating interface circuit used for control purpose.

inverter can be evaluated by using:

$$I_{cap} = I\sqrt{\frac{M}{16\pi}[4\sqrt{3}(4cos(2\varphi+6) - 9\pi M(cos(2\varphi)+1))]} \tag{3.18}$$

where I is the leg current, M is the index modulation and φ is the angle between the current and the voltage [41]. In this converter, two series (i.e. one for each axis) of electrolytic capacitors (1.5 mF, 400 V), with a nominal current of 14 A, were adopted. Furthermore, ceramic (100 nF) and film capacitors (2.2 μF) were used for each inverter with the aim to reduce the parasitic layout inductance.

3.6 Measurement circuits

As described in Chapter 2, the mission is to move the current control of the inverters from the DSP to the FPGA. The chosen FPGA (see Chapter 3.2) has not ADCs, thus external ADCs are required. For this purpose, ADCs with 12 – bit resolution and an acquisition speed of 3 MSPS are used (AD7276). The analog voltage range of the chosen ADC converter spans from 0 V to 3.3 V. As a consequence, all the analog signals of the measurements need to be compliant with the ADC voltage range.

3.6.1 Current measurement circuit

Between all the existing current measurement configurations hall effect sensors are chosen. The inverters currents are acquired by means of CASR50-NP. This is a current sensor that presents galvanic isolation between the low voltage and the high voltage circuits. Moreover, it presents good dv/dt immunity (20 kV/μs).

This sensor has an internal 2.5V reference, which becomes very useful for the acquisition in differential mode of the currents. In fact, long traces can be disturbed

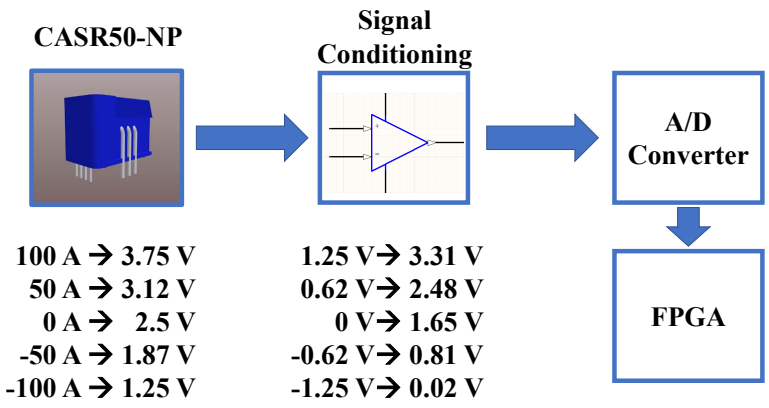


Figure 3.13: Equivalent scheme of the current acquisition circuit.

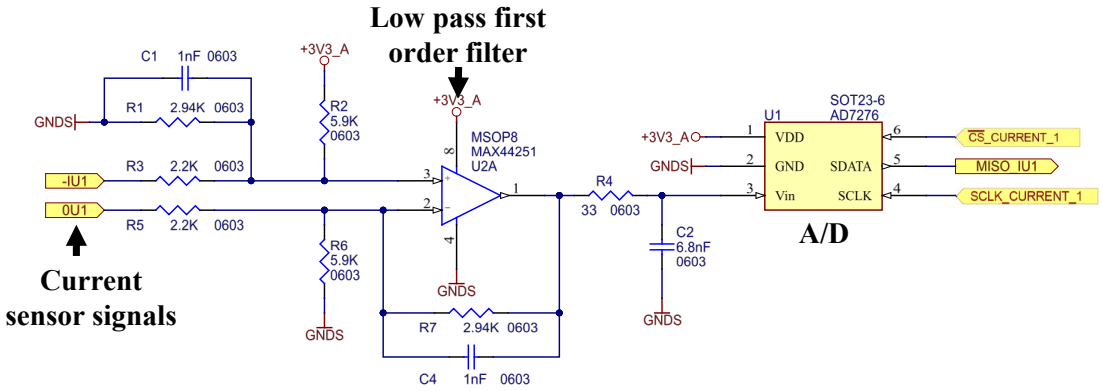


Figure 3.14: Schematic representation of the circuit used for acquisition of the inverter current.

by incident field excitation [42]. Thus, during the wire routing the reference and signal traces, which are referred to the same ground, can be pulled in parallel. Thence, by means of an operational amplifier that is configured in differential mode, common mode rejection of the disturbance can be achieved.

Considering the inverter current rating (see Table 2.2), the current measurement range is imposed between −100 A and 100 A. An equivalent scheme of the measurement scales of the circuit is represented in Fig. 3.13. Correspondingly, the schematic representation of the circuit used for the acquisition of the current is shown in Fig. 3.14. Details of this measurement circuit scheme are given below.

- The current sensor: the measurement signal is composed of an offset (2.5 V) plus the measured signal.
- The signal conditioning circuit: the output signal sensor is filtered (i.e. low-pass filter $f_t = 55$ kHz) and multiplied by a gain factor (i.e. 0.75). Furthermore, the offset is shifted from 2.5 V to 1.65 V

- ADC converter is connected to the FPGA by means of a communication system (i.e. CS, SCLK and Data). Inside the FPGA the measurement is converter in two's complement, thus the correspondent binary number can consider the sign of the current.

3.6.2 Voltage measurement circuit

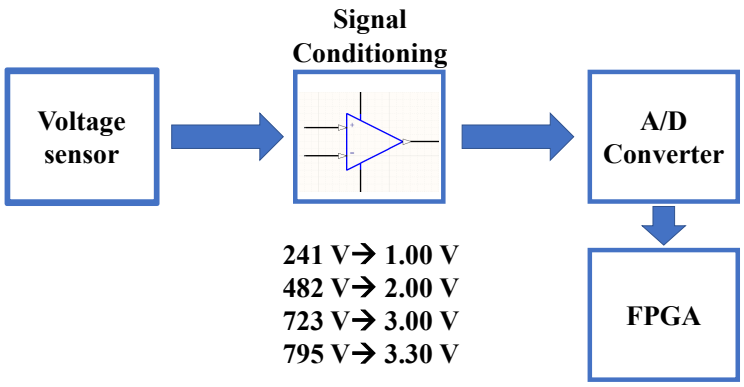


Figure 3.15: Equivalent scheme of the voltage acquisition circuit.

The bus voltage is measured by means of resistors with high values. The insulation between the low voltage circuit and the high voltage circuit is guarantee by high ohmic value.

Considering the inverter bus voltage rating, the measurement range is imposed between 0 V and 800 V. In fact, the maximum voltage is imposed by the capacitor voltage rating. An equivalent scheme of the measurement circuit is represented in Fig. 3.16. Details of the measurement circuit are given below.

- Signal conditioning circuit: by means of the operational amplifier the measured voltage is filtered and a gain factor is applied.
- ADC is connected to the FPGA. Inside the FPGA the measurement is converter in a binary number. In this case, the sign of the voltage is not necessary because the bus inverter voltage cannot be negative.

3.6.3 Temperature measurement circuit

The heat sink temperature is measured by means of a PTC. No galvanic insulation is required because the heat sink is mechanically connected to the inverter frame, thence to the power plant ground.

The maximum temperature measured by the thermal sensor needs to reach almost 80 °C. An equivalent scheme of the measurement circuit implemented on

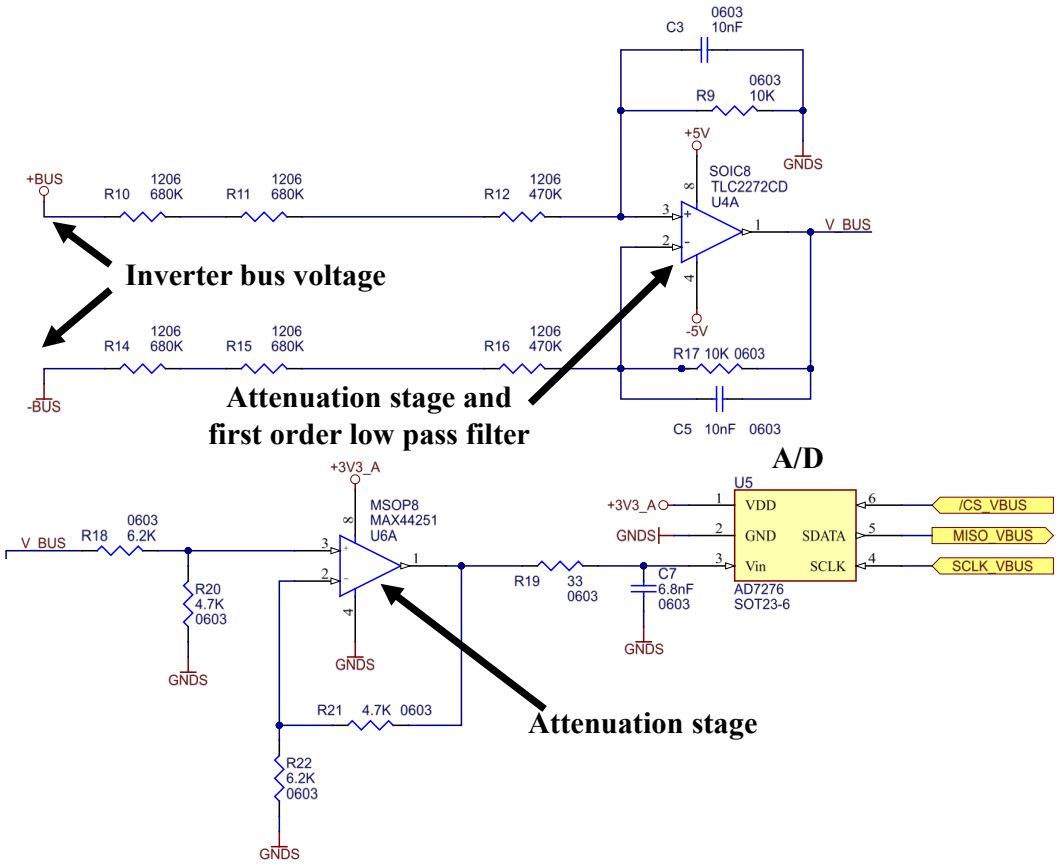


Figure 3.16: Schematic representation of the circuit used for acquisition of the bus voltage.

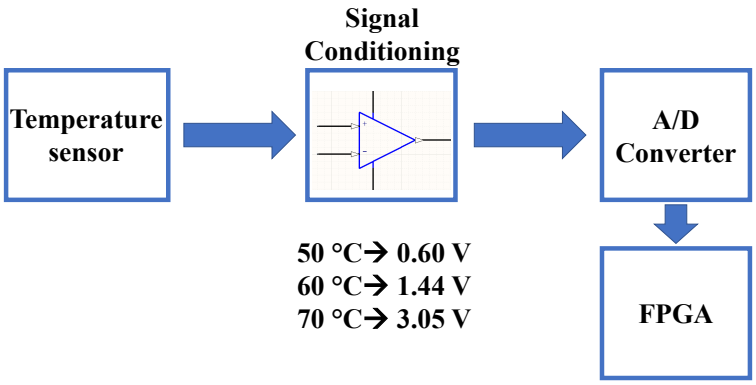


Figure 3.17: Equivalent scheme of the temperature acquisition circuit.

board is represented in Fig. 3.17. Details of the measurement circuit are given below.

- The signal conditioning circuit: by means of the operational amplifier the

measured voltage is filtered and a gain factor is applied.

- ADC converter is connected to the FPGA. The sign is not necessary because the heat sink temperature cannot be negative.

3.7 PCB design

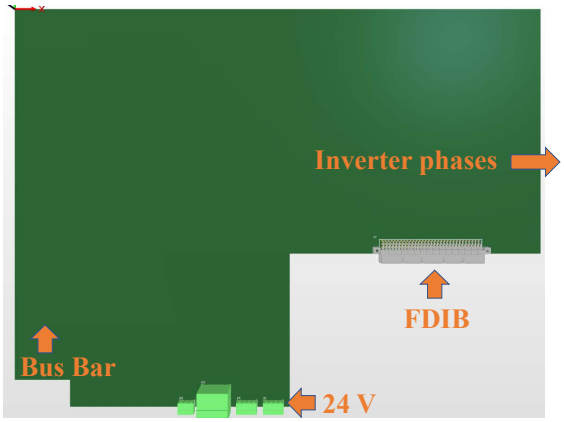


Figure 3.18: Power converter: mechanical constraints of connections with the external world.

All the circuit components are disposed on the same board; therefore no piggy-back boards are used. As a consequence, high and low voltage circuits live together on the same board.

Table 3.6: PCB layer stack-up.

Top Solder	0.01 mm	
Top Layer	0.07 mm	
Dielectric 1	0.23 mm	
Signal layer 1	0.07 mm	
Dielectric 3	0.96 mm	
Signal layer 2	0.07 mm	
Dielectric 2	0.23 mm	
Bottom layer	0.07 mm	
Bottom Solder	0.01 mm	

The power board is realized with a shape compatible mechanically with the other power converters of the same family (i.e. XPower). The power board shape

is depicted in Fig. 3.18. The board is realized with four layers and the chosen layer stack-up is shown in Table 3.6. As can be seen from this table, for all the four layers a copper thickness of 70 μm is selected. The copper thickness is high because the currents in the board are high. Higher copper thickness is not recommended because between two electrical nets the minimum guarantee distance increases with the thickness, thence going in contrast with the constraint of the pins of the FPGA. Then, 70 μm is a reached trade-off which considers the smallest distance (i.e. 7 mil) and the high current which flows in the board (i.e. more than 60 A). In order to obtain additional benefits from cost and debugging process point of view, all the components board are arranged on one side of the board.

3.7.1 Components placement

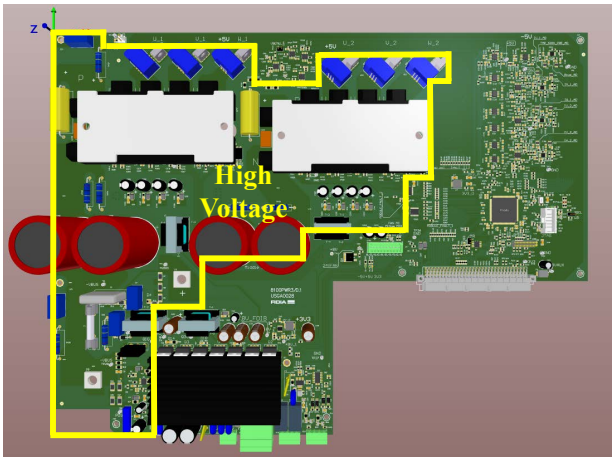


Figure 3.19: High voltage room of the power converter is highlighted in yellow while the rest is considered low voltage circuit.

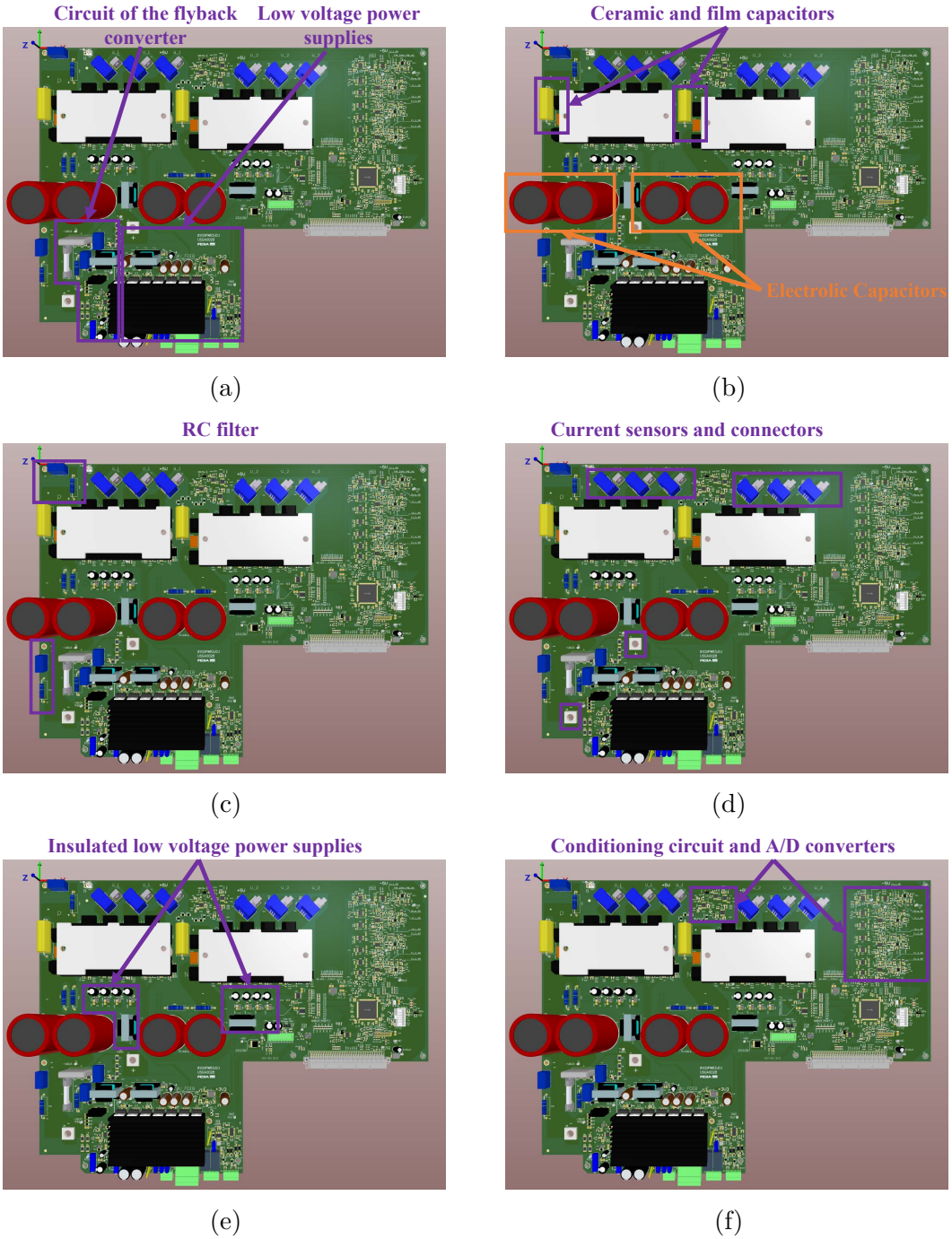


Figure 3.20: Components placement: (a) flyback converter and low voltage power supplies, (b) bus capacitors, (c) RC filters which connect the bus to the drive ground, (d) current sensors and connectors, (e) power module isolating power supplies and (f) sensor conditioning circuits are highlighted.

All the board components were placed on the board. The board is divided into low and high voltage areas as can be seen in Fig. 3.19. Inside the high voltage room, the components listed below can be found.

- A flyback converter is present inside the electronic board. It can be noticed from (Fig. 3.20(a)) the presence of the transformer and the switch. This converter is connected to the bus voltage and it is controlled by a current mode controller (UC3843B).
- In Fig. 3.20(b), the capacitors connected to the bus voltage are highlighted. It can be noticed the presence of the ceramic and the film capacitors near the power module terminals, thence permitting to reduce the parasitic layout inductance.
- Two resistors and capacitors can be noticed in Fig. 3.20(c). These components are RC filters that connect the plus and minus terminals of the converter to the ground. This solution permits to create a low impedance path for the common mode currents, thus avoiding the problem to near electronic devices.
- The current sensors described previously are highlighted in Fig. 3.20(d). Moreover, in the same figure, the power connectors are highlighted. The positive terminal of the inverter bus is connected to the fuse box, then to the bus bar. The negative terminal of the inverter is directly connected to the negative terminal of the bus bar. The output terminals of the power modules are connected to the terminals of the converter by means of cables.
- Isolated power supplies of the IPM power modules, which details have been provided previously are highlighted in Fig. 3.20(e).

3.7.2 Wire routing issues

Current measurement

An important problem that was encounter during the wire routing is described here: the measurement signals of the current sensors run near the output of the switches, thence EMI problem can be found. This issue has been represented schematically in Fig. 3.21(a). As can be seen from the figure, the measurement signals generated by the current sensors need to reach the opposite side of the board. A solution to this problem is proposed and it is shown in Fig. 3.21(b), Fig. 3.21(e) and Fig. 3.21(d). The problem is solved by placing the critical signals in the inner layer and at the bottom and at the top a ground shielding is adopted. This solution has been adopted because the skin depth presented by the inverter disturbance (10 MHz) is lower than the board copper thickness. In this way, the disturbances are damped by the two layers.

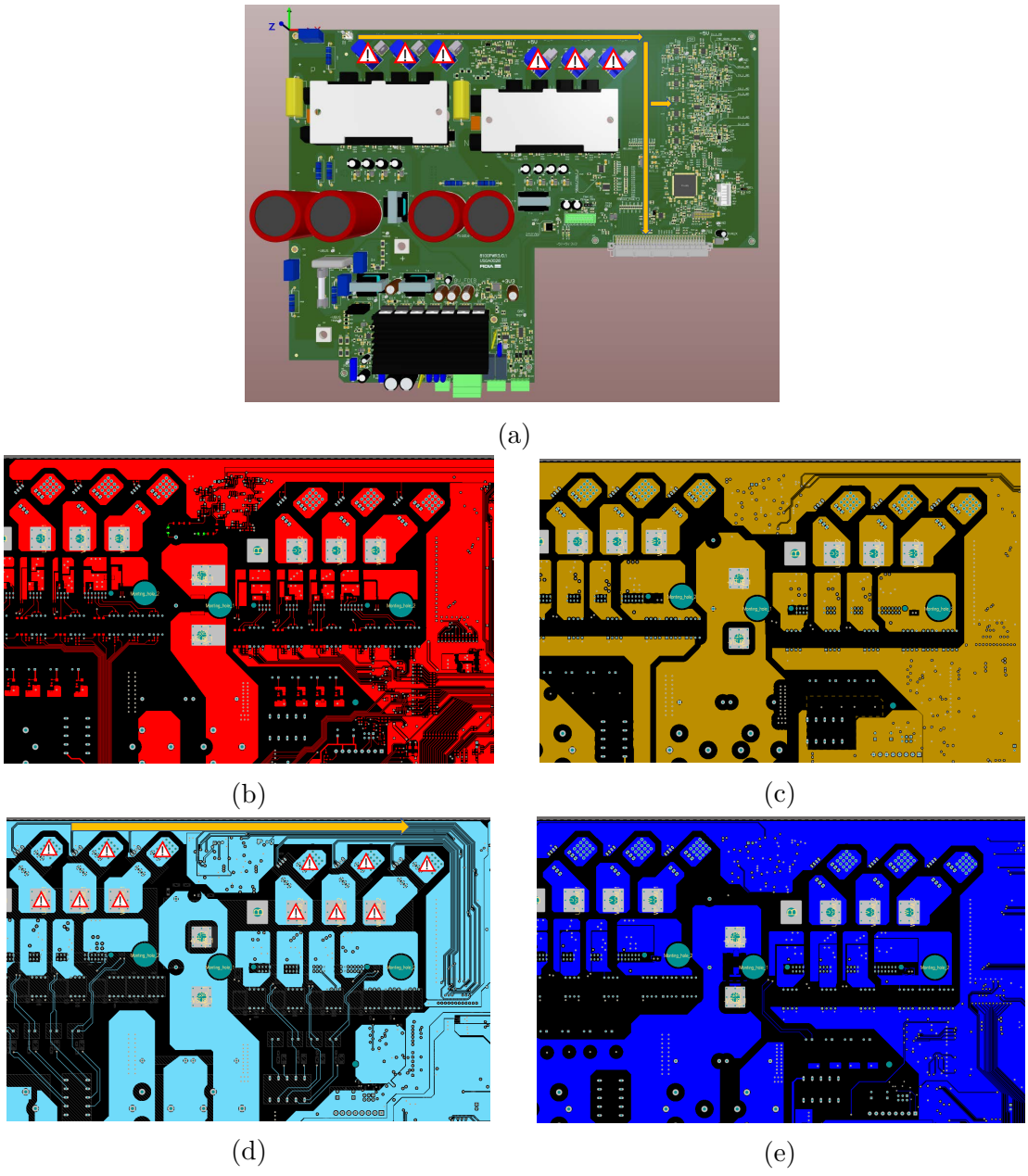


Figure 3.21: Shielding of the current measurement signals. (b) Top layer, (c) inner layer 1, (d) inner layer 2 and (e) bottom layer

Power modules

Wire routing criticalities were found for the IPM power modules. Owing to the impossibility to introduce additional piggyback boards, insulation and space issues are encountered. In fact, the IPM can be reached only from four sides. As a

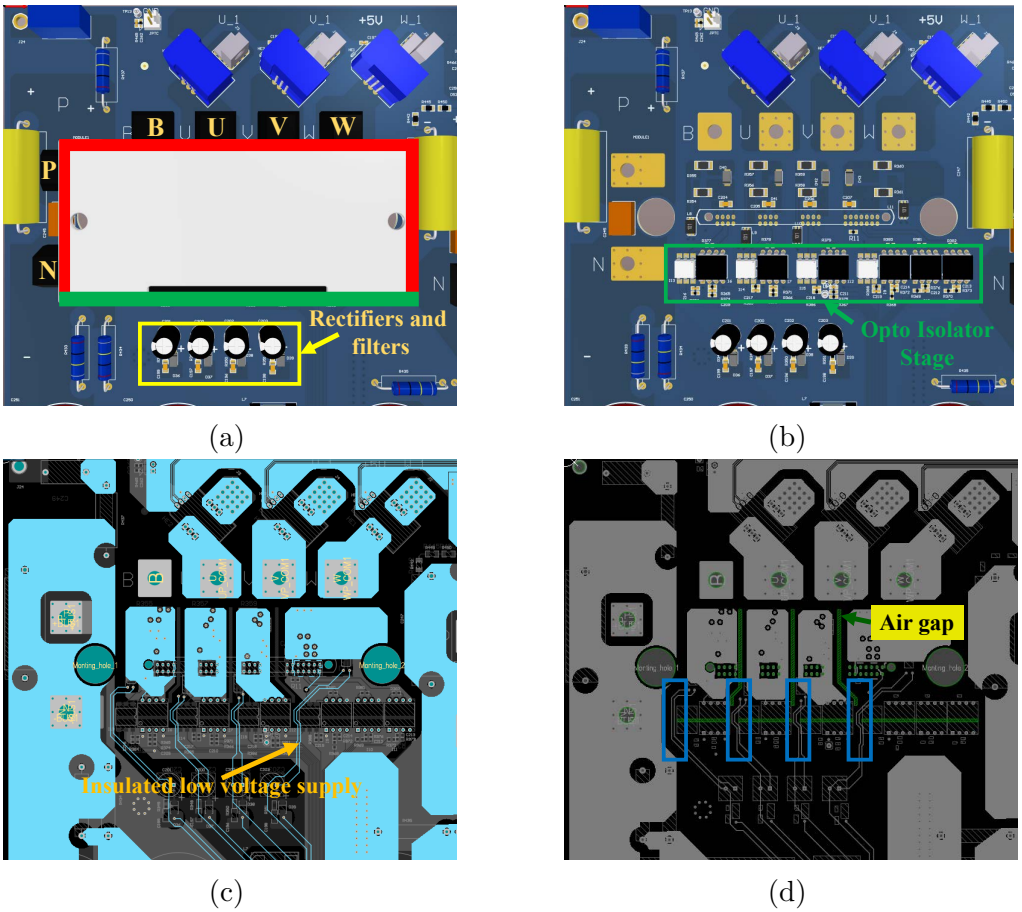


Figure 3.22: IPM wire routing issue. (a) The rectifier and the filter of each power supply are highlighted. (b) Components presented below the IPM power modules are highlighted. (c) Signal layer 2 and the insulated low voltage supply are highlighted. (d) The clearance holes are highlighted.

consequence, bring the power supplies and the control signal to the IPM becomes a very complicated task. As can be seen from Fig. 3.22(a), four sides can be detected. The no available sides are indicated in red, while the available sides are indicated in green. Considering the four available sides, two sides are completely not available because the "P", "N", "U", "V", "W" and "B" terminals are present. Two other sides can be used for bringing the power supplies and the control signals, however, one side is unavailable because it is close to the second power module. Thus, as depicted in Fig. 3.22(a) only one side is available for the routing of the power supplies and control signals (the one indicated in green). The routing issue was solved by following the solution described below.

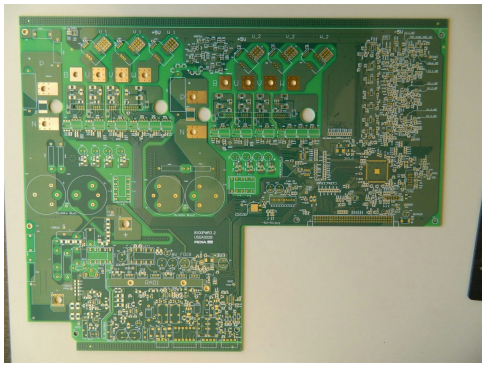
- The space issue was solved by putting all the opto-isolators below the IPM as can be seen from Fig. 3.22(b). In this way, EMI problems are reduced too.

In fact, the insulated signals are placed as close as possible near the power module terminals.

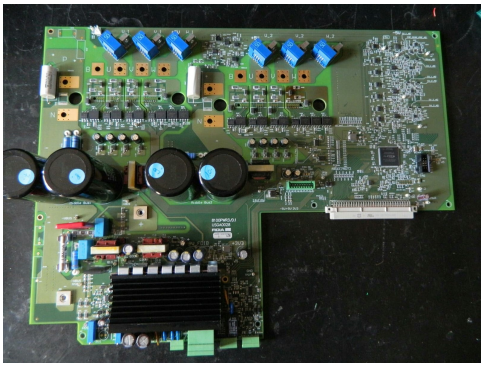
- Owing to space issues the low voltage power components cannot be placed below the IPM, thus the only available solution was to place them as close as possible near the IPM (Fig. 3.22(a)).
- The insulated low voltage supplies pass between dedicated area (Fig. 3.22(c)) which have been created between the opto-isolator. Furthermore, clearance holes were introduced by permitting to increase the safety insulation distance (Fig. 3.22(d)).

3.8 PCB and initial tests

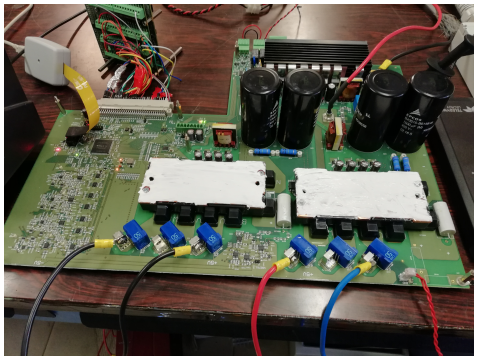
3.8.1 PCB



(a)



(b)



(c) PCB and the power modules.

Figure 3.23: Electronic components mounted on the PCB board.

The final PCB board is depicted in Fig. 3.23(a). The PCB board with mounted all the components is shown in Fig. 3.23(b). Standard tests (e.g. power supplies,

protections, desaturation, etc. etc.) were conducted by changing the power module configuration devices. A good power converter functionality was demonstrated by the experimental results. By virtue of this feature, the power converter was connected to a three-phase load.

It was noticed during the experiments that using all-SiC IPM, sometimes the IPM sent a fault error (IPM fault). In the beginning, the origin of the fault was not clear. In fact, this fault can be identified as:

- short circuit leg;
- drive under voltage;
- junction over temperature.

As a consequence, a detailed investigation of the origin of the problem was required.

3.8.2 IPM fault when all-SiC is used

Methodology

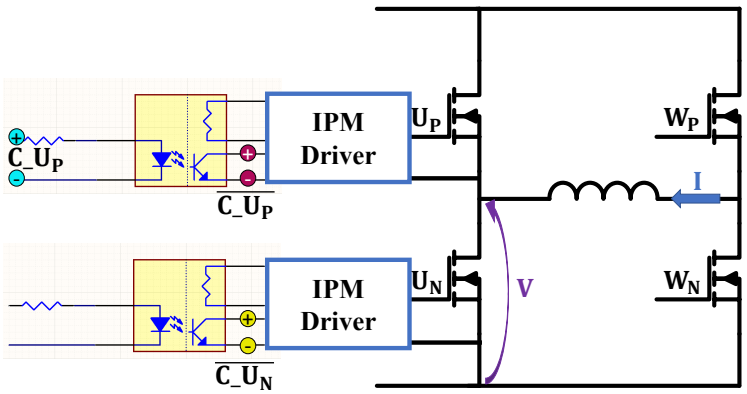


Figure 3.24: IPM issue origin investigation: equivalent scheme of the experimental setup where probes placement are highlighted.

As described previously, IPM fault was detected sometimes, thence the variables of the converter were measured. Opposition method was applied between two inverter legs (U and W legs). The current of one leg is controlled (W), while the other one works with an imposed duty cycle (U). In this way, different current and duty cycle values can be performed. The measurement was conducted by adopting the scheme proposed in Fig. 3.24. The heat sink and the middle point of the DC bus were connected to the earth. The voltages were measured by means of well-insulated differential probes (HVD3206), which presents a good common-mode rejection ratio.

Experimental results

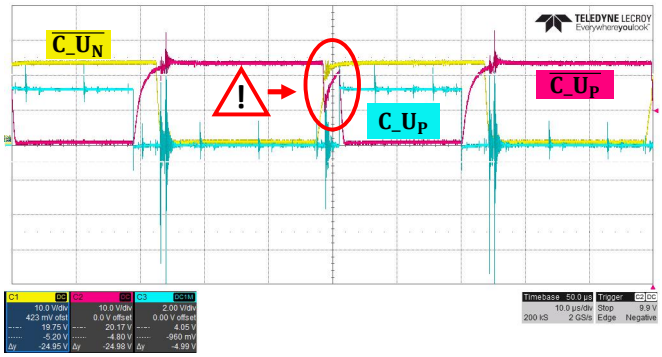


Figure 3.25: Experiment results: voltages measured by the differential probes.

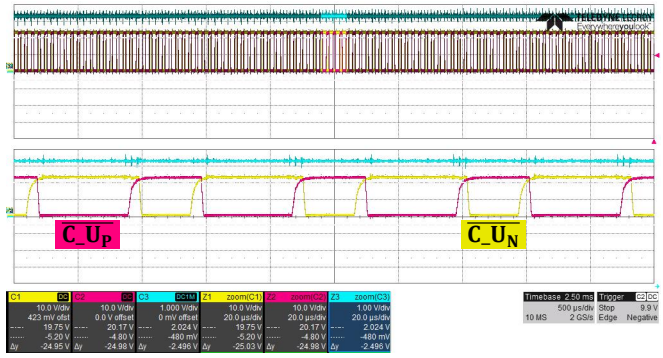


Figure 3.26: Experiment results: voltages measured by fiber optically isolated probes.

In Fig. 3.25 experimental results, where 20 A with 600 V of dc bus and a duty cycle near 50% were imposed are shown. Owing to the current sign, only the low switch (U_N) can commutate, thus the commutation is controlled by the yellow trace depicted in Fig. 3.25. As can be seen from this figure, when the yellow trace changes the state the red trace is disturbed. This happens because of the MOSFET U_N changes the state. This condition seems to be critical because it can cause leg short circuit (when U_N and U_P are low).

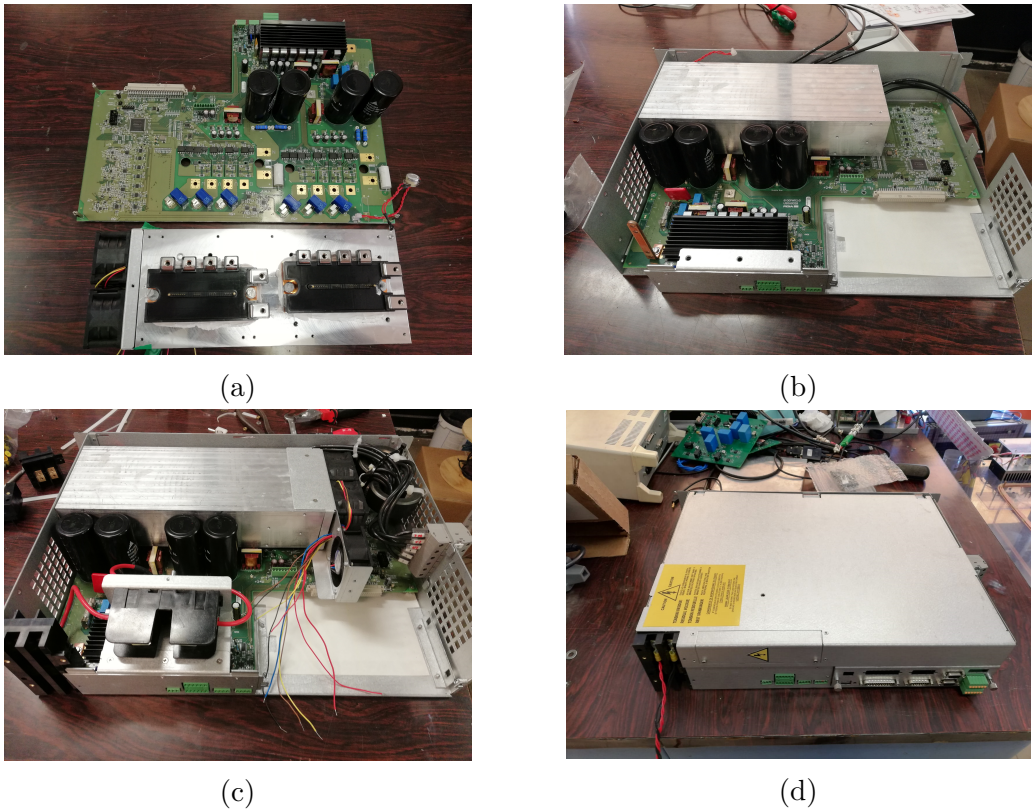
At the beginning, it was thought that the opto-isolators were not able to keep the output signals well. As a result, buffers were implemented but not major changes were recorded. After different tentative, it was discovered that the voltage probe did not really measure what was happening. In fact, by changing the voltage probe and using fiber optically isolated probes it was discovered that the phenomena shown in Fig. 3.25 was not present as can be seen in Fig. 3.26. The reason was due to the very high voltage derivative imposed by the SiC MOSFET.

Thence, short circuit leg caused by the command itself is not the origin of the IPM fault. In order to understand if the problem was still the short circuit leg a Rogowski coil was used and no overcurrent was measured.

The solution

Once the right instrumentation was detected, the IPM problem was again put under the light. It was seen that voltage short pulse width (i.e. less than 800 ns) is the cause of this issue. The experimental results suggested that the resonances that occurred inside the power module do not have time to damp out. The problem was avoided by the firmware, where the IPM fault was removed by avoiding extreme duty cycle region (i.e. near 0% and near 100%).

3.9 Mounting process of the power converter



(a) (b) (c) (d)

Figure 3.27: Mounting process of the power converter: (a) PCB, power modules and heat sink, (b) PCB, power modules and heat sink mounted inside the mechanical box, (c) PCB, power modules, heat sink, fans and common mode chokes mounted inside the mechanical box and (d) final version of the power converter.

Finally, once all the circuits of power converter were tested the PCB board was mounted in the mechanical structure as can be seen from Fig. 3.27(a), Fig. 3.27(b), Fig. 3.27(c) and Fig. 3.27(d)

3.10 Conclusions

A prototype of a dual-axis converter was developed. The developed device is compatible with all-Si, Si-SiC and all-SiC power modules based on IPM technology. Bulky components, as power modules, heat sink and capacitors, had been designed and chosen. The bulky components together with all the required ones (i.e. signal conditioning, low and high voltage power supplies) were organized in the board shape, by following the mechanical constraints imposed by the company. Some criticalities found during wire routing are described with also details about the applied solutions. Once the PCB project was complete, for each technology device a board was built. Standard tests and checks were done and no important problems were discovered by the prototype.

Subsequently, the inverters were connected to an inductive-resistive load. IPM power module fault was registered when the converter based on all-SiC device was used. Investigations about the source of the issue were conducted by measuring all the system signals. Control signals were measured by means of high voltage differential probes, which are standard instrumentation used in the industrial environment. During the measurement process, it was discovered that the presence of the probe itself influence in a significant way the measurement. Accordingly, the use of standard probes could be inadequate, when SiC devices are adopted. Measurement issue was confirmed when high voltage fiber optically isolated probes were used, in fact, the problem was not registered. Once the right instrumentation was detected, the IPM problem was again put under light. It was seen that voltage short pulse width (i.e. less than 800 ns) is the cause of this issue. The problem was avoided by the firmware, where the IPM fault was removed by avoiding extreme duty cycle region (i.e. near 0% and near 100%).

Finally, the designed boards were placed inside the mechanical boxes, permitting to reach a condition much similar to the industrial applications and then new tests were conducted.

Chapter 4

Losses and thermal comparisons between all-Si, Si-SiC and all-SiC devices

4.1 Introduction

In this chapter, losses comparisons between the all-Si, Si-SiC and all-SiC technologies have been done by using the converter designed for ac drive applications, which has been described in Chapter 3. This power converter has been used and comparisons have been done by having the same package, layout, heat sink, connections between the power module terminals and the converter terminals. Close attention is paid to the well-known measurement methodologies. Among all the methods proposed by the literature, the opposition method has been selected letting to reach precise comparisons. AC power losses of the three-phase inverter have been measured by means of an accurate test bench. By virtue of precise measurements, switching and conduction AC power losses have been extrapolated from the measurements. Finally, a summary of the comparisons between all-Si, Si-SiC and all-SiC is proposed.

4.2 Converter loss measurement methods

Different loss measurement methodologies have been proposed [9, 10, 12, 13, 14, 15, 16, 43, 44, 45, 46, 47, 48]. These widely recognized methods are summarized as follows:

- Double-Pulse Test (DPT)
- measuring the electrical input and output power of the converter

- calorimetric method
- opposition method.

The best method needs to be selected in order to evaluate, precisely, the losses of each technology.

4.2.1 Double pulse test

The DPT is adopted for evaluating the switching performance of a device [45]. In most of the cases, these experimental results can be found in the device datasheet. The data obtained from these tests together with the ON voltage drop of the switch could be introduced in simulations, thus permitting to obtain a performance comparison between the devices [9, 10, 12, 13, 14, 15, 16]. Anyway, in [43, 45] it was demonstrated that the switching loss measurements can present problems, especially when fast devices are adopted. The problems that could appear, when this method is used, are explained here.

- Time alignment issues between the voltage and the current probes can be found. Moreover, the losses could be not anymore well measured [45].
- Current and voltage probes can present problems caused by capacitively coupled ground. The coupling results in no real current presence, which can badly affect the measured switching loss energy [45]
- High bandwidth probes are required, thus standard probe as Rogowski coil is not anymore a valid option for all-SiC devices. Solutions as a current shunt can be implemented, however, the layout of the power converter is negatively influenced [43, 44, 45, 49]. Therefore, switch overvoltage and switching energy are higher when the layout is not optimized [50, 51].
- The switching energy is influenced by the connecting cable present between the switch and the load [44]. As a consequence, precise switching loss measurements cannot be guaranteed.

Criticalities in the switching loss measurements and comparisons between the performances of the technologies could be found.

4.2.2 Calorimetric method

The calorimetric method is a way used for measuring power converter losses [43, 46]. This method is based on the principle of measuring the enthalpy variation of the power converter coolant. This solution can be used with air or water cooling solutions. However, it is more popular for water cooling solutions because it is

simpler. In fact, the losses can be easily obtained by measuring the temperature variation of the liquid. Instead, for air cooling solution a calorimetric chamber is required. The temperature of this chamber is controlled by a thermal exchanger. The problems that could appear, when this method is used, are explained here.

- Very high accurate temperature and flowmeter probes are required.
- It is a difficult task to maintain the adiabatic condition of the thermal chamber because parasitic thermal exchanges could be present (i.e. walls, connections).
- The variance of specific heat capacitance and density of the coolant could be present.
- In the case of big converter, a big chamber capable of containing the converter is required.
- Varying the converter load, accurate measurements are not guaranteed because the test bench is optimized for a certain operational point.

Criticalities in the loss measurements and comparisons between the performances of the technologies could be found.

4.2.3 Input and output power measurements

The sequent method is very easy to be applied. The input and output powers of the converter are measured. Subsequently, the losses are obtained as the difference between the two power terms. However, the accuracy of the measurements is small especially when the efficiency of the converter is higher [43]. Criticalities in the loss measurements and comparisons between the performances of the technologies could be found when this method is used.

4.2.4 Opposition method

The opposition method is a method that requires twin three-phase inverters [43, 47, 48]. Losses of the power converters can be measured without requiring any dissipative load and power supply. Furthermore, using this measurement methodology, very good accuracy can be achieved without requiring high-bandwidth probes even if fast switches are adopted. Using this method the layout of the power converter can be optimized because additional probes are not required, thus issues described previously could be avoided [50, 51]. The problems that could appear, when this method is used, are explained here.

- When the opposition method is applied to two three-phase inverters a common mode current is generated. This current is generated by the dead times of the PWM and the zero-sequence voltage injection [47, 48].

- The total losses of the converter are not always equally distributed between the twin inverters [43].
- The losses of the inductors used during the application of this method need to be removed from the total losses [43].

No important problems are associated with this method. Thus, close attention needs to be paid to the defects presented by this method.

4.3 AC losses measurement with opposition method

AC losses comparisons between the all-Si, Si-SiC and all-SiC devices have been conducted by adopting the opposition method. Using this method, the sequent positive feature can be exploited: the power converter layout can be designed optimally because no current probes are required in the circuit. During this work, close attention has been paid to the defects presented by this method: common mode current presence and inductor losses measurements.

4.3.1 Measurement equivalent circuit

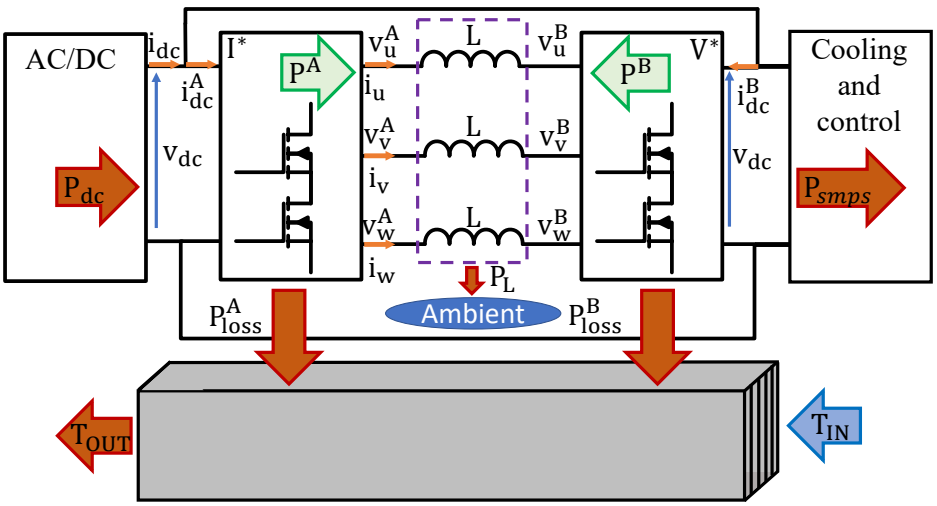


Figure 4.1: Equivalent scheme of the opposition method applied to the designed power converter.

AC losses were measured using the opposition method [43, 47, 48]. Using this method twin inverters with the same power rating are required, where one works as a generator and the other one emulates the load [43, 47, 48]. This method was applied to the described power converter (see Chapter 3), which is composed of two three-phase inverters, as schematically shown in Fig. 4.1. As illustrate in this

figure, the inverter A controls the current (I^A) and its angle φ_i^A, while the inverter B imposes fixed modulation index (i.e. M^B and φ_v^B). By virtue of this feature, power testing by varying the power factor and the load can be conducted without requiring any special components (i.e. high power DC generator and load with high power rating).

4.3.2 Opposition method methodology

As schematically represented in Fig. 4.1, using opposition method the AC/DC supplies only the losses of the system (P_{dc}) as follows:

$$P_{dc} = P_{smps} + P_L + P_{loss}^A + P_{loss}^B \tag{4.1}$$

where, the DC source provides the sequent power terms:

- power module loss of the inverter A (P_{loss}^A)
- power module loss of the inverter B (P_{loss}^B)
- auxiliary services plus cooling (P_{smps})
- the inductors losses (P_L).

The power module losses are calculated by subtracting the known P_{smps} and the inductors losses as follows:

$$P_{loss}^A + P_{loss}^B = P_{dc} - P_{smps} - |\left(P^A + P^B\right)| \tag{4.2}$$

where, the inductor power losses can be evaluated as the difference between the active powers of the two inverters (i.e. P^A and P^B).

The power term expressed in (4.2) can be used for a comparison purpose between the technologies, however, it is composed of the power terms of the two inverters. In fact, as seen in (4.2), the power module losses are summed together ($P_{loss}^A + P_{loss}^B$). However, the two power terms need to be separated in the interest of doing accurate comparisons between all-Si, Si-SiC and all-SiC devices. As a matter of fact, the losses sharing between the two power modules depends on the power converter working point. Thus, loss sharing study between the two inverters requires an investigation of the switching loss and conduction loss terms of each power module, as evident from

$$P_{loss}^A + P_{loss}^B = P_{sw}^A + P_c^A + P_{sw}^B + P_c^B \tag{4.3}$$

where, P_{sw} represents the power module switching loss and P_c is the power module conduction loss.

Switching losses

The switching losses are present when the inverter leg changes its state. In AC, the current changes periodically, thus the switching losses change periodically with the current too. Considering to have linear dependence of energy loss with respect to the current, the equivalent energy loss is equal to the energy loss dissipated when the current mean value is commutated [38]. Therefore, by fixing the switching frequency (f_{sw}), the switching losses can be calculated by [38]:

$$P_{sw,T} = (E_{on(\sqrt{2}I/\pi)} + E_{off(\sqrt{2}I/\pi)})f_{sw} \tag{4.4}$$

$$P_{sw,D} = (E_{rr(\sqrt{2}I/\pi)})f_{sw} \tag{4.5}$$

In (4.4), transistor turn-on and turn-off switching losses are considered, while in (4.5) the diode turn-off switching term is considered. It can be noticed from (4.4) and (4.5) that these power terms are independent of the power factor (φ) and the modulation index (M), thus the switching losses of the two inverters are always the same (i.e. $P^A_{sw} = P^B_{sw}$).

Conduction losses

The conduction losses are caused by the switches ON voltage drops. Two characteristic features can be distinguished using the three technologies: with or without reverse conduction property. When no reverse conduction is present (i.e. using Si-SiC and all-Si), the switches voltage drops can be represented by the piecewise linear model, where V_{th} represents the threshold voltage and R_d is the differential resistance [38]. Using ON voltage drop model, it is possible to define simple AC conduction losses formulae [38]. AC power losses can be calculated by:

$$P_{c,T} = \sqrt{2}IV_{th,T}\left(\frac{1}{2\pi} + \frac{Mcos\varphi}{8}\right) + 2I^2R_{d,T}\left(\frac{1}{8} + \frac{Mcos\varphi}{3\pi}\right) \tag{4.6}$$

$$P_{c,D} = \sqrt{2}IV_{th,D}\left(\frac{1}{2\pi} - \frac{Mcos\varphi}{8}\right) + 2I^2R_{d,D}\left(\frac{1}{8} - \frac{Mcos\varphi}{3\pi}\right) \tag{4.7}$$

where, M is the modulation index, I is the current leg (RMS amplitude) and φ is the phase. Instead, when reverse conduction is present (i.e. using all-SiC devices), the conduction losses analytical expressions become more complicate as mentioned earlier in [11]:

$$\begin{aligned} P_{c,T} = {} & \frac{R_{on}}{4\pi}2I[(1-2t_{bl}f_{sw})(\frac{\pi}{2}+\beta-\frac{sin\beta}{2}) + (2Mcos\varphi)(cos\beta - \frac{cos^3\beta}{3}))] + \\ & + \frac{R_{on}}{4\pi(R_{on}+R_{d,D})^2}[2R_d^2I^2((1-2t_{bl}f_{sw})(\frac{\pi}{2}+\beta-\frac{sin\beta}{2}) - 2Mcos\varphi(cos\beta - \frac{cos^3\beta}{3})) + \\ & + V_d^2((\pi-2\beta)(1-2t_{bl}f_{sw}) - 2Mcos\varphi cos\beta) + \\ & + 2R_{d,D}\sqrt{2}IV_{th,D}(2cos\beta(1-2t_{bl}f_{sw}) - Mcos\varphi(\frac{\pi}{2}+\beta-\frac{sin\beta}{2}))] \end{aligned} \tag{4.8}$$

while the diode conduction loss, when it is in parallel to a MOSFET is:

$$P_{c,D} = \frac{R_{d,D}}{4\pi(R_{on}+R_{d,D})^2}[2R_{on}^2 I^2(\frac{\pi}{2} - \beta + \frac{sin\beta}{2} - 2Mcos\varphi(cos\beta - \frac{cos^3\beta}{3}))+$$
$$+V_{th,D}^2(\pi - 2\beta - 2Mcos\varphi cos\beta) - 2R_{on}\sqrt{2}IV_{th,D}(2cos\beta - Mcos\varphi(\frac{\pi}{2} - \beta + \frac{sin\beta}{2}))]-$$
$$-\frac{V_{th,D}}{4\pi(R_{on}+R_{d,D})}(\sqrt{2}IMR_{on}cos\varphi(\frac{\pi}{2} - \beta + \frac{sin\beta}{2}) + 2R_{on}\sqrt{2}Icos\beta-$$
$$-V_{th,D}(\pi - 2\beta) + 2V_{th,D}Mcos\varphi cos\beta) + t_{bl}f_{sw}\sqrt{2}I(\frac{R_{d,D}I}{\sqrt{2}} + \frac{2V_{th,D}}{\pi}) \tag{4.9}$$

where, β is the parallel conduction angle and it is defined by:

$$sin\beta = \frac{V_{th,D}}{R_{on}\sqrt{2}I} \tag{4.10}$$

and t_{bl} is the blanking time. Anyway, in both cases, the losses are dependent on the power factor and the modulation index, thus the conduction power losses of the two power modules are not always equal.

Power loss sharing

The power loss of each module, which is composed of switching and conduction losses are shown in (4.11) and in (4.12).

$$P_{loss}^A = 6P_{sw,T}^A(I, f_{sw}) + 6P_{sw,D}^A(I, f_{sw}) + 6P_{c,T}^A(I, M^A, \varphi_{vi}^A) + 6P_{c,D}^A(I, M^A, \varphi_{vi}^A) \tag{4.11}$$

$$P_{loss}^B = 6P_{sw,T}^B(I, f_{sw}) + 6P_{sw,D}^B(I, f_{sw}) + 6P_{c,T}^B(I, M^B, \varphi_{vi}^B) + 6P_{c,D}^B(I, M^B, \varphi_{vi}^B) \tag{4.12}$$

As can be seen from the formulae, the loss sharing unbalancing is caused by the conduction losses, which are dependent on the modulation index and the power factor. As detailed in Fig. 4.2, the current supplied by inverter A is seen by inverter B shifted of π, thus the two power factors are not equal, as a consequence the total loss could not be divided. Therefore, a strategy in the measurement setup needs to be implemented in order to avoid bad power loss distribution between the power modules.

4.3.3 Useful hints valid for the opposition method

Equal power sharing

In order to obtain accurate comparisons, the single power module loss needs to be measured. Therefore, power losses between the two power modules need to be determined. The power loss between the power modules can be divided in

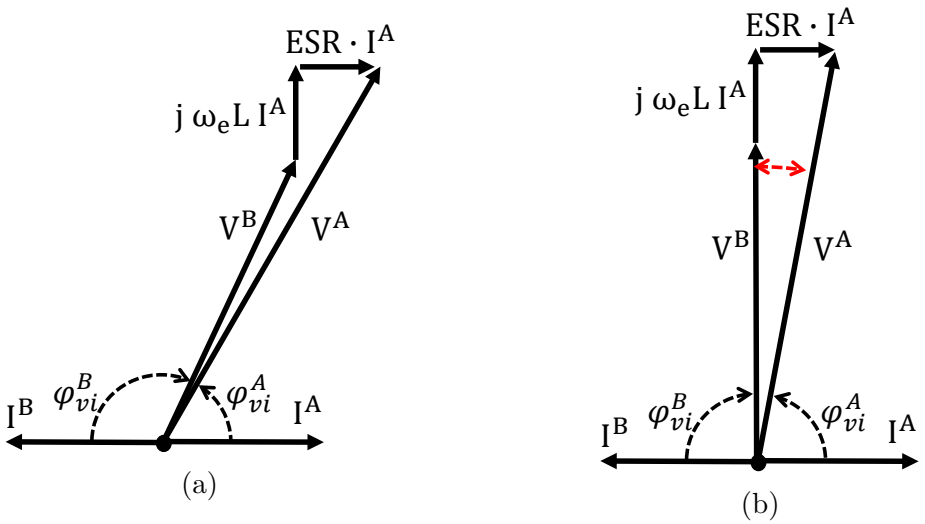


Figure 4.2: Opposition method phasor diagrams following the convention of the equivalent scheme shown in Fig. 4.1. (a) Case with a generic power factor. (b) Case with power factor imposed equal to "0" with highlighted in red the phase error introduced by the ESR of the inductor.

special operational condition of the two inverters. Considering the conduction loss formulae, it is possible to divide the power losses by applying two conditions:

- $M^A = M^B = 0$
- $\varphi_i^A - \varphi_v^B = \pi/2$

Forcing the voltages or the index modulations equal to zero is not a valid option because current control becomes impractical. Then, the most successful solution is to impose the correct power factor.

Inductors for opposition method

Care should be taken in the selection of the filter inductors. When ideal inductor is used and by imposing $\varphi_i^A = 0$ and $\varphi_v^B = \pi/2$, the power sharing between the two modules is determined because these conditions are present: $\varphi_{vi}^A = \pi/2$ and $\varphi_{vi}^B = -\pi/2$. However, when real inductors are used different problems can emerge. Experimentally, inductors with high Q are required. In fact, as can be noticed from Fig. 4.2(b), the Equivalent Series Resistance (ESR) can lead to a phase shift of the inverter voltage (inverter A) that accompanies it to move from its ideal position. Consequently, the phase shift (i.e. double arrow in red in Fig. 4.2(b)) varies the angle from the ideal condition ($\varphi_{vi}^A = \pi/2$), then the power loss sharing is not well satisfied. Consequently, the phase shift (i.e. double arrow in red in Fig. 4.2(b)) deviates from the ideal condition ($\varphi_{vi}^A = \pi/2$), and thus the power loss sharing is not

well satisfied anymore. Furthermore, the inductance value of the filters should be lower as possible permitting to reduce the difference between the two modulation indexes of the inverters (i.e. M^A and M^B), thus going in contrast with the current ripple peak (i.e. lower current ripple is achieved with higher inductance value).

4.4 The test bench

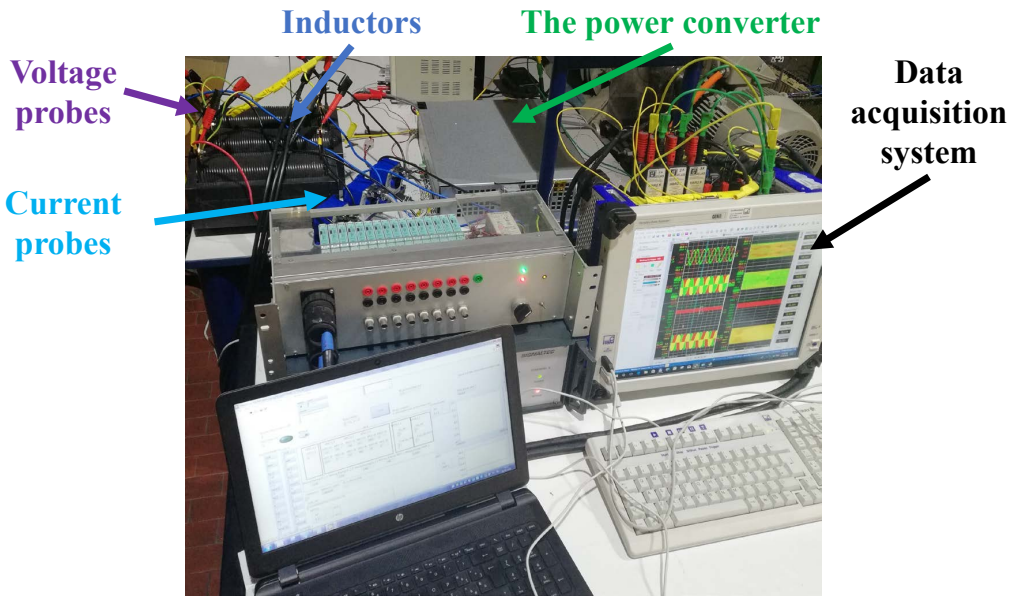
The experimental setup is displayed in Fig. 4.3(a). The power converter was connected to an insulated AC/DC converter (EA-PSI 91000-30 3U) with a nominal power rating equal to 10 kW, which is compatible with the maximum estimated losses. In all tests, the bus voltage (V_{dc}) was imposed equal to 600 V. Good quality inductors are required as described in Chapter 4.3.3, for this purpose three ferrite inductors were selected (680 μH, I = 100 A). These inductors present a higher current rating with respect to the converter in order to avoid magnetic saturation.

The two inverters were controlled by the same FPGA (10M25SCE144) allowing the synchronization of the two PWM carriers. As follows, the current ripple is minimized and low-frequency beating interferences are canceled. The FPGA controlled the current reference (I^A) and φ_I^A of the inverter A, while the inverter B imposed fixed modulation index (M^B) and φ_V^B.

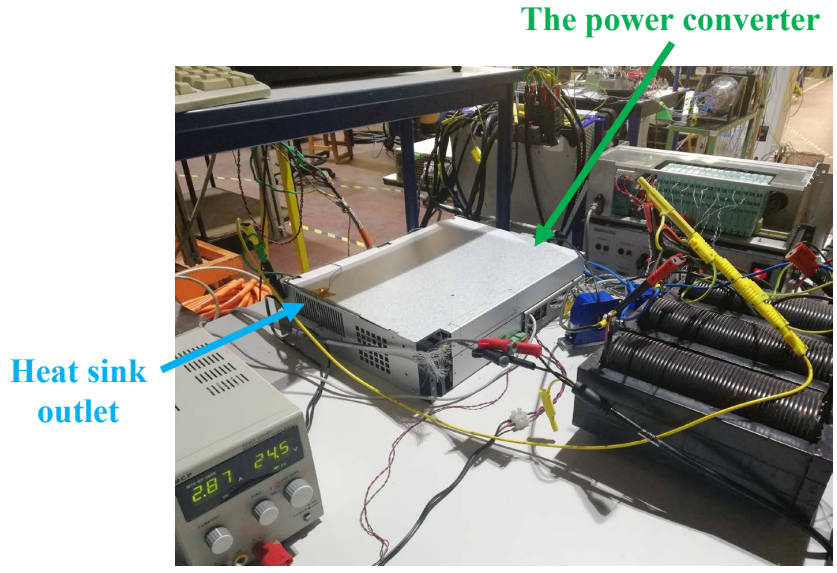
In all the tests, the dead time equal to 1.5 μs was imposed, while the fundamental electrical frequency was imposed equal to 50 Hz. The electrical frequency is high enough to permit a steady-state junction temperature instead of having a junction temperature which follows the sinusoidal trend [17]. The third harmonic current is present when dq current control is used and it is generated by the inverters' dead times and zero sequence voltage injection. This current presents the same magnitude of line currents, then power loss measures are affected. This issue was removed using a common-mode current controller [47, 48].

The electrical variables of the inverters were acquired using a high-speed data acquisition system (HBM, GEN3i) having a resolution of 18 bit. Inverters line-to-line voltages (i.e. v_{uw}^A, v_{uw}^B etc. etc), bus voltage (v_{dc}), line currents and the bus current (i_{dc}) were measured. The temperature probes (i.e. type K thermocouples) were placed in different parts of the power converter heat sink, as schematically represented in Fig. 4.4. The inductors, inlet and outlet air temperatures were measured too using K thermocouples.

The measurement test bench was synchronized with the FPGA of the power converter permitting to acquire the measured variables in precise time moment (e.g. acquire the samples when the variables reach the target imposed by the FPGA). Each time that measurement was required by the FPGA, 100 ms of synchronized data were acquired. In this period of time, the voltages and the currents were sampled simultaneously at 2 MSPS, while the temperatures were sampled at 1 KSPS.



(a)



(b)

Figure 4.3: Experimental setup composed of the measurement system, the power converter, and the inductors.

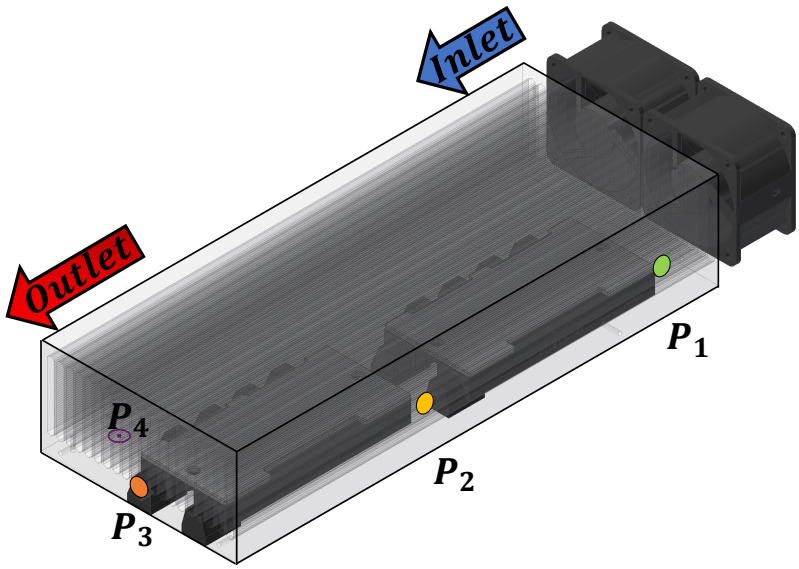


Figure 4.4: Heat sink power converter CAD representation of the thermal measurement points.

4.4.1 Post-process elaboration data

Once all the measurements were conducted, using an appropriate code run on Perception (HBM), data were elaborated. Power factors, first harmonic voltages, switching frequency and current were derived, permitting to associate all these variables to the power loss value. For each sweep (100 ms), all the line-to-line voltages were converted into line-to-neutral voltages and then multiplied by their corresponding currents obtaining the instantaneous inverter output power, as applied in eq. (4.13) for the inverter A. The same procedure applied for inverter A was applied for inverter B as in (4.14).

$$p^A_{(t)} = \frac{v^A_{uv} - v^A_{wu}}{3} i^A_u + \frac{v^A_{vw} - v^A_{uv}}{3} i^A_v + \frac{v^A_{wu} - v^A_{vw}}{3} i^A_w \tag{4.13}$$

$$p^B_{(t)} = \frac{v^B_{uv} - v^B_{wu}}{3} i^B_u + \frac{v^B_{vw} - v^B_{uv}}{3} i^B_v + \frac{v^B_{wu} - v^B_{vw}}{3} i^B_w \tag{4.14}$$

The instantaneous input power was obtained by multiplying the DC voltage and DC current, as

$$p_{dc} = v_{dc} i_{dc}. \tag{4.15}$$

Applying the mean value function to all the instantaneous powers, the system active powers were determined by:

$$P^A = \frac{1}{T_e} \int_0^{T_e} p^A_{(t)} dt \tag{4.16}$$

$$P^B = \frac{1}{T_e}\int_0^{T_e} p^B_{(t)}dt \tag{4.17}$$

$$P_{dc} = \frac{1}{T_e}\int_0^{T_e} p_{dc(t)}dt \tag{4.18}$$

where T_e is the fundamental electric period. Finally, the total power dissipated by the power modules were derived using (4.2).

A phase between the current and the voltage of the inverter was associated with each measurement. The phase is evaluated by following this procedure.

- A digital low pass filter was applied to the line current (i.e. Filter Butterworth LP), thus removing the residual current ripple.
- The zero crossing of the current was identified, thus permitting to obtain the fundamental electrical frequency. A square wave signal, which is in phase with the fundamental frequency is obtained from this process.
- The square wave signal permits to obtain the phase shifting between the current and each measured variable.

4.5 Comparisons at the power converter nominal condition

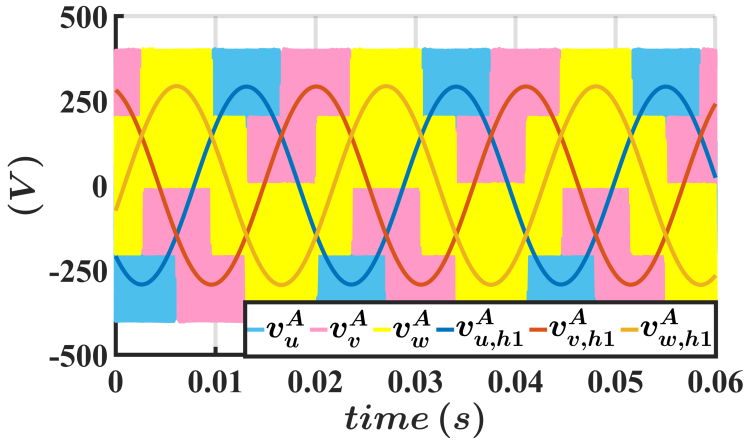


Figure 4.5: Experiment results using all-SiC (V_{dc} = 600 V, I = 30 A, f_{sw} = 7.8 kHz). Inverter A: phase-to-neutral voltages and their first harmonics.

The nominal current of the power converter (see Table 2.2) was imposed by the FPGA and measurements using the three technologies were conducted. During these tests, the inlet temperature was maintained equal to the nominal condition

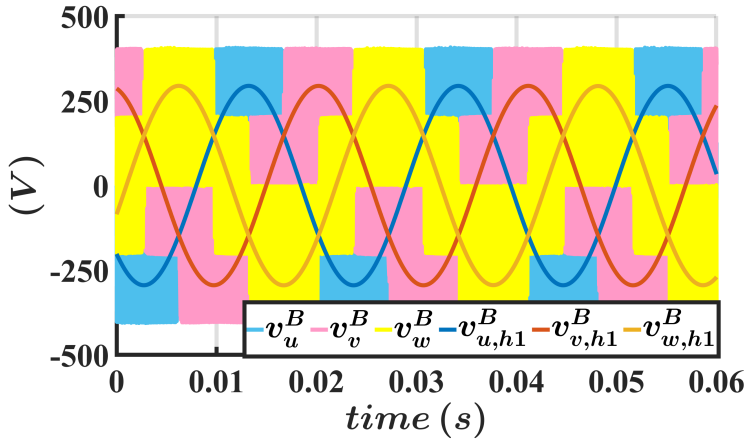


Figure 4.6: Experiment results using all-SiC (V_{dc} = 600 V, I = 30 A, f_{sw} = 7.8 kHz). Inverter B: phase-to-neutral voltages and their first harmonics.

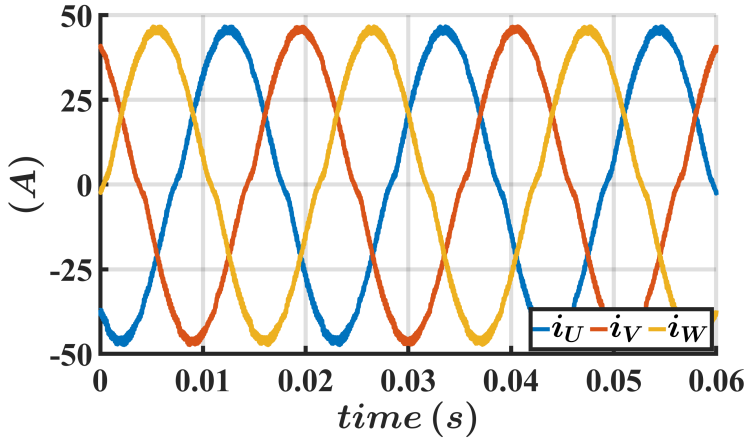


Figure 4.7: Experiment results using all-SiC (V_{dc} = 600 V, I = 30 A, f_{sw} = 7.8 kHz). Inverter line currents.

(40 °C). Electrical variables and temperatures were acquired in continuous mode, in fact, every 200 ms a sweep was acquired and subsequently processed.

In Fig. 4.5 and Fig. 4.6 the line-to-neutral voltages of the two inverters are depicted. In both figures, the evaluation of the first harmonic component of each voltage is presented. It can be observed that the voltages of two inverters are approximately equal and in phase (see Fig. 4.8), because of inductors with good quality factors. Moreover, as can be seen in Fig. 4.7, the current ripple is not important with respect to the fundamental current thanks to the PWM carriers synchronization.

Power converter response results to the nominal load are depicted in Fig. 4.9. In this figure, the power modules losses are depicted and as expected the all-SiC

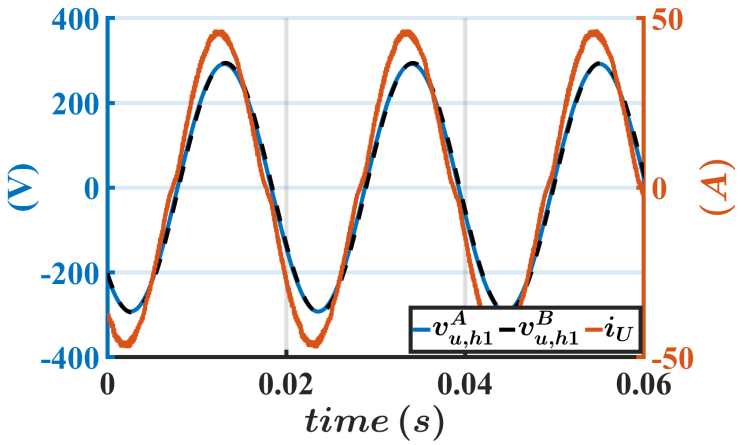


Figure 4.8: Experiment results using all-SiC (V_{dc} = 600 V, I = 30 A, f_{sw} = 7.8 kHz). Electrical variables of the phase "U".

and the Si-SiC present always better performances with respect to all-Si. In three cases, it can be observed the presence of a noticeable power losses increase.

The losses of all-Si power modules changed from 634 W (i.e. when the power converter was turned on) to 698.7 W, thus presenting an increase of 9% in the loss. The Si-SiC presented a loss rising of 5%, while in all-SiC, an increase of 3% was observed. Owing to the constant time presented by the losses, it appears that this phenomenon is associated with a thermal transient. No important temperature increase was measured in the inductors (no more than 5 °C), thus no Joule loss effect was associated with this phenomenon. This evidence suggests that the power loss variation is due to the junction temperature increase. In fact, the IGBT tail current and the diode reverse recovery charge get worse with the temperature increase. Thus, as can be seen from the experimental results, the all-Si presents a more important effect with respect to Si-SiC because all-Si presents both the phenomena while the Si-SiC presents only the tail current.

Observing the heat sink power dissipation (Fig. 4.10), two exponential trends can be identified as depicted in the zoomed area of the figure. The faster evolution is attributed to the junction transient thermal impedance, the slower evolution is associated with the temperature evolution of the heat sink. As a matter of fact, in Fig. 4.10(a), Fig. 4.11(a) and Fig. 4.12(a), the heat sink temperatures reached the steady state temperatures after 500 s, where this time is consistent with the time evolution of the losses. The heat sink thermal constant has been derived from the experimental data and it is equal to 126 s.

Considering the steady state (i.e. losses reached the maximum) and doing a comparison with all-Si, power loss reduction of 63.9% using all-SiC was identified while using Si-SiC a reduction of 20.1% was measured. Evidently, the reduction in power losses is seen from the heat sink temperatures. In fact, the maximum

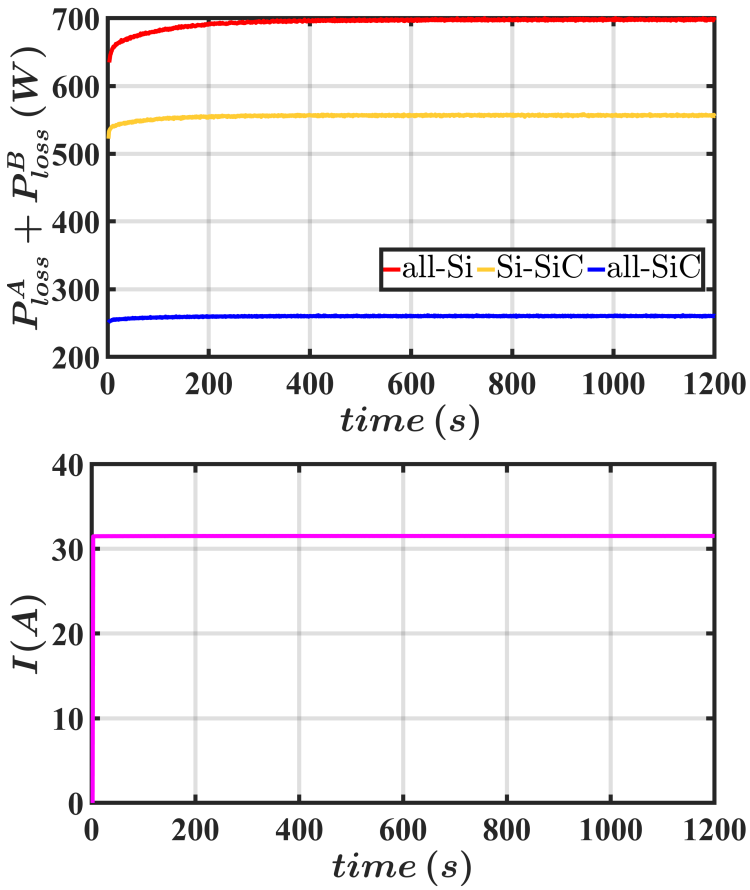
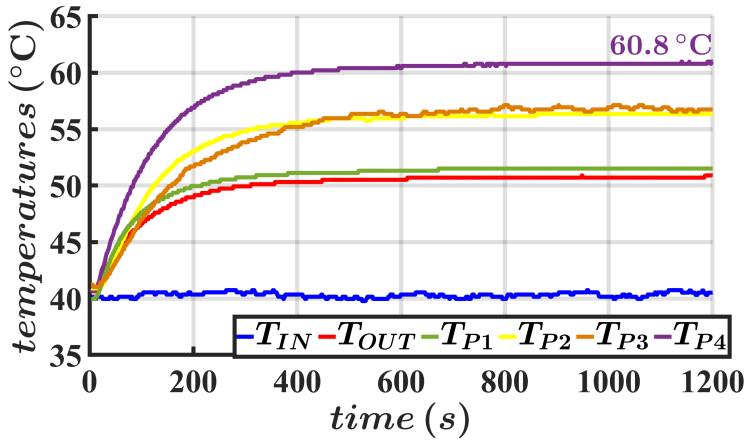


Figure 4.9: Experimental results: thermal step response to the inverter power rating ($V_{dc} = 600$ V, $I = 30$ A, $f_{sw} = 7.8$ kHz). (a) Power dissipated by the heat sink for each technology and (b) measured phase current of the inverter.

registered temperature decreased from 61 °C to 57 °C using Si-SiC, and to 48.36 °C using all-SiC. Finally, the efficiencies of the drive were evaluated at the rated load by considering also the auxiliary services and the results are shown in Table 4.1.

Table 4.1: Power converter efficiencies at the nominal condition (30 A, 600 V and 7.8 kHz).

	all-Si	Si-SiC	all-SiC
(η)	97.86%	98.2%	98.8%



(a)

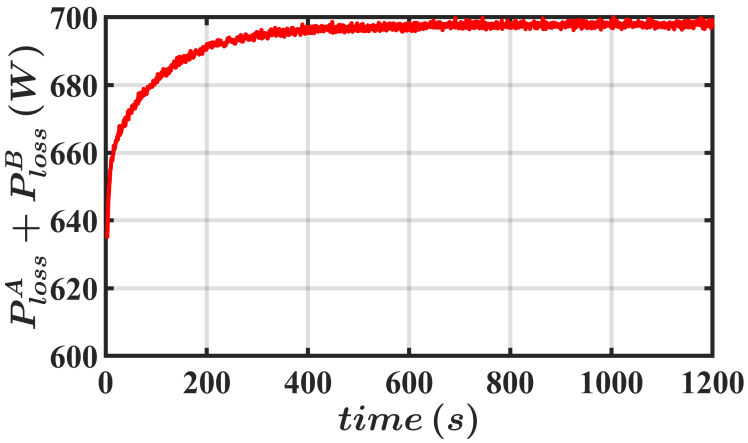


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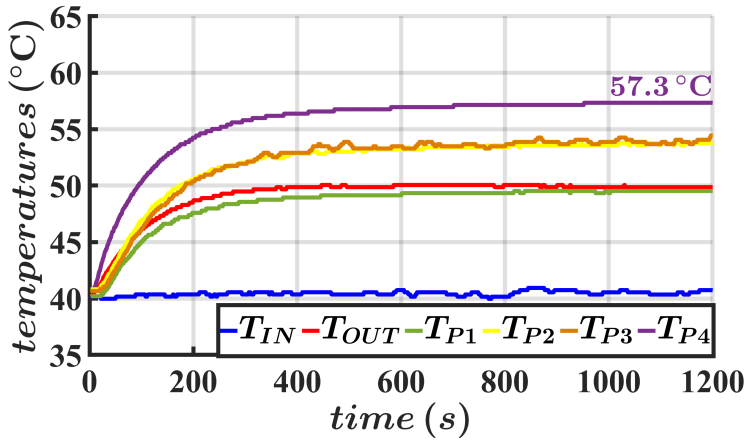
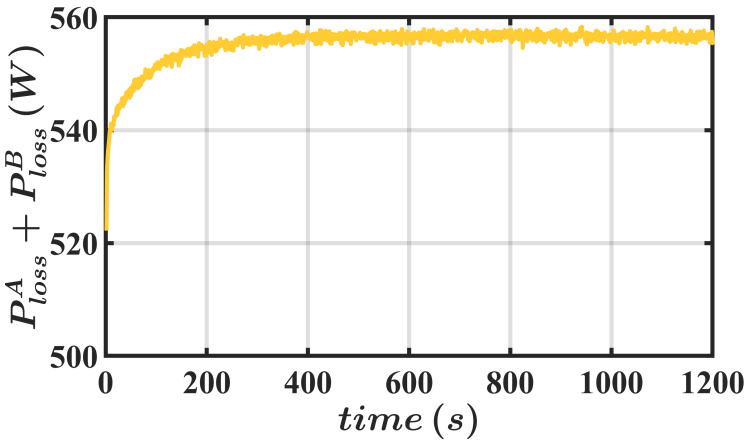
Figure 4.10: Experimental results: thermal step response to the inverter power rating ($V_{dc} = 600$ V, $I = 30$ A, $f_{sw} = 7.8$ kHz). (a) Temperatures of the heat sink using all-Si device. (b) Power dissipated by the heat sink for each technology.

4.6 Module AC power losses comparisons

In this section, closed attention is paid to the AC losses dependency with respect to the leg current (I) and the switching frequency (f_{sw}). In all the measurements, the same modulation index ($M = 0.5$) and power factor ($\cos\varphi = 0$) were maintained permitting the power module losses identifications. All the measurements were conducted by fixing the hottest heat sink temperature ($P_4 = 60\,°C$), where this point is schematically represented in Fig. 4.4. The temperature of the power converter was controlled by itself. A temperature control loop was implemented for this purpose. The output of a PI is the current reference of inverter A (I^A), while inverter B has fixed imposed voltage (V^B). Every 30 s, the current reference



(a)



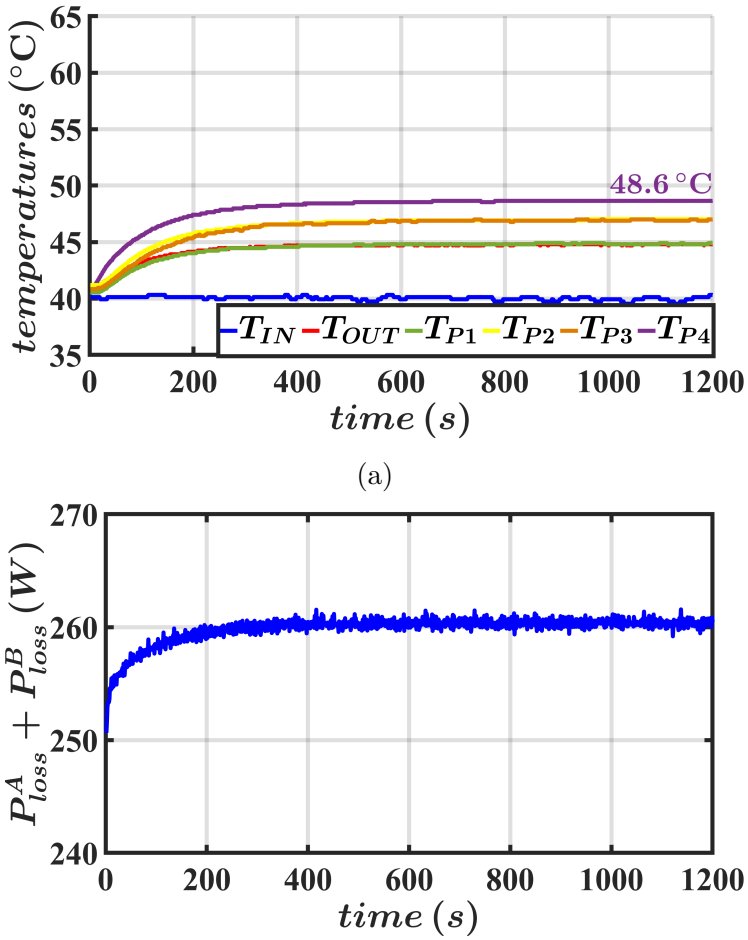
(b)

Figure 4.11: Experimental results: thermal step response to the inverter power rating ($V_{dc} = 600$ V, $I = 30$ A, $f_{sw} = 7.8$ kHz). (a) Temperatures of the heat sink using Si-SiC device. (b) Power dissipated by the heat sink for each technology.

of the temperature loop is masked, and the required voltage and current references, taken by a look-up-table, are applied for 500 ms. The time application of the new references is small enough not to permit perturbation of the heat sink temperature. In this instant of time, three actions are achieved.

1. The inverter currents reach the references imposed by the look-up table. Junctions temperatures arrive at the steady-state temperature condition. The junctions reach the steady state temperature after 100 ms (owing to thermal impedance value).

2. One sweep is acquired, thus the measurements are done for 100 ms.



(a)

(b)

Figure 4.12: Experimental results: thermal step response to the inverter power rating ($V_{dc} = 600$ V, $I = 30$ A, $f_{sw} = 7.8$ kHz). (a) Temperatures of the heat sink using all-SiC device. (b) Power dissipated by the heat sink for each technology.

3. Finally, the temperature control loop takes back control.

4.6.1 Comparisons of conduction and switching losses

Modules power losses measurements were conducted by changing the switching frequency and fixing the current. Converter switching frequency and inductance value are strongly related to the ripple current of the inverter. The ripple current could slight affect the losses of the inverter. If the ripple current is not well monitored during the tests, problems may arise in the assessment of device losses. A solution to this problem could be the use of inductor with an inductance value proportional to the converter switching frequency, thence permitting to do tests with

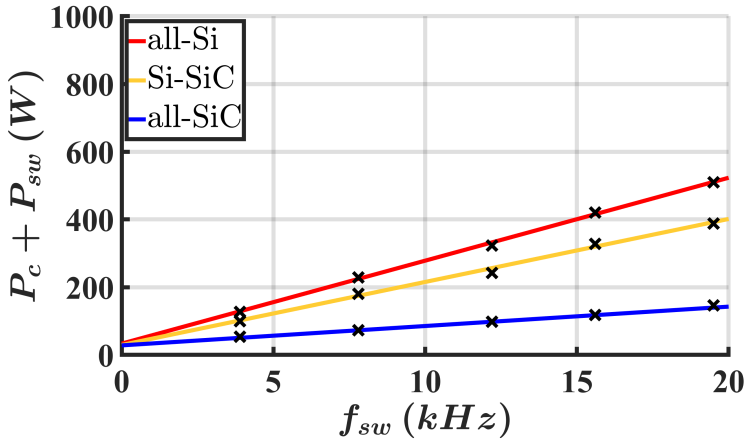


Figure 4.13: Experiment results: power module losses in function of the frequency fixing the current value ($V_{dc} = 600$ V, $cos\varphi = 0$, $M = 0.5$, $I = 20$ A).

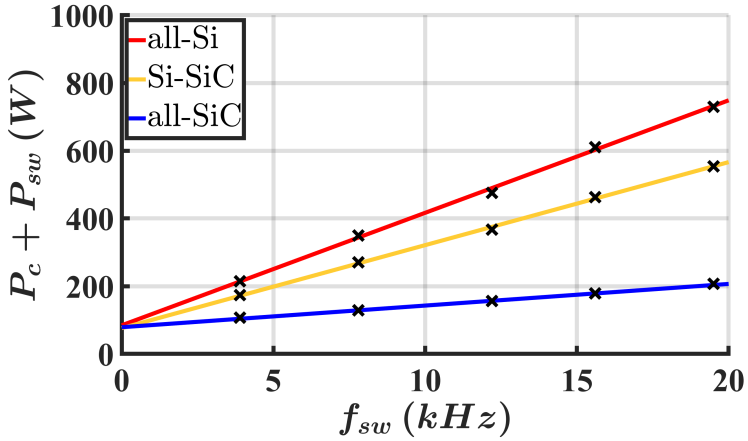


Figure 4.14: Experiment results: power module losses in function of the frequency fixing the current value ($V_{dc} = 600$ V, $cos\varphi = 0$, $M = 0.5$, $I = 30$ A).

constant ripple. Unfortunately, during the tests, no other good quality inductors were available in the laboratory. Anyway, the measurements were conducted by avoiding high ripple current (less than 1.5 A peak-to-peak) and low nominal current (higher than 20 A). Furthermore, comparisons between the three technologies were fairly conducted because the same ripple condition was guaranteed by the fact that the same experimental setup was used. The minimum imposed frequency was 3.9 kHz, because in frequencies lower than this value the current ripple becomes important, which affects the conduction losses of the inverters. The maximum frequency that was reached is 19.5 kHz owing IPM fault protection trigger.

Inverter power losses measurement results by doing the switching frequencies sweeps are shown in Fig. 4.13, Fig. 4.14 and Fig. 4.15. In these figures, the dotted

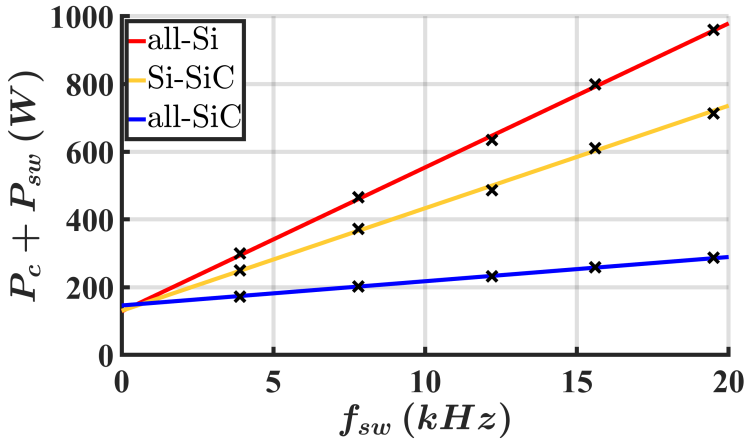


Figure 4.15: Experiment results: power module losses in function of the frequency fixing the current value ($V_{dc} = 600$ V, $cos\varphi = 0$, $M = 0.5$, $I = 40$ A).

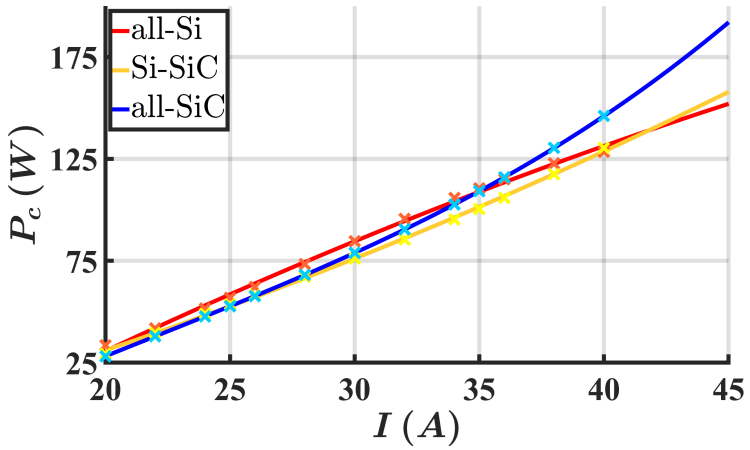


Figure 4.16: Mathematical elaboration: power module conduction losses as a function of the inverter current ($cos\varphi = 0$, $M = 0.5$)

.

points represent the experimental results, while the interpolations of these measurements are illustrated with solid lines. Firstly, it can be noticed from the figures that Si-SiC and all-SiC present always lower losses with respect to all-Si. Secondly, a marked linear correlation of the losses with the switching frequency is present for all the technologies. Finally, the evidence suggests that this linear trend changes the slope ($\Delta P_{loss}/\Delta f_{sw}$) when the current value changes. The gradient increases proportionally with the current value. Thus, as a consequence of the details derived previously, a simple function that fits power module loss can be defined by:

$$P_{loss} = P_c(I) + P_{sw}(I, f_{sw}) = P_c(I) + K\, I\, f_{sw} \tag{4.19}$$

where, K is bounded with the switching loss and P_c is linked with the conduction

loss.

By deriving the K factor for each technology, it is possible to compare the switching losses of all-Si, Si-SiC and all-SiC. These parameters have been determined by calculating the slopes of Fig. 4.14. The average K factors derived from the experimental results are summarized in Table 4.2.

Table 4.2: Switching losses of all-Si, Si-SiC and all-SiC power modules.

	all-Si	Si-SiC	all-SiC
(K)	1.1325 W/ (A kHz)	0.8321 W/ (A kHz)	0.2146 W/ (A kHz)

From these data, the switching loss reduction of 26.5% is achieved when Si-SiC is used instead of all-Si. Meanwhile, using all-SiC instead of all-Si, a switching loss reduction of 81% was observed.

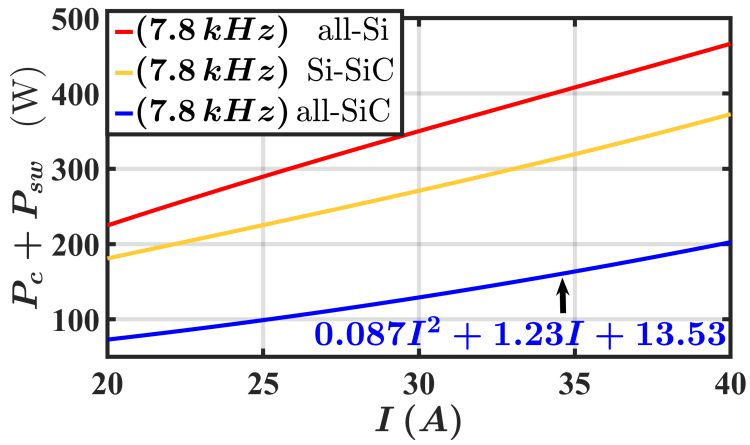
The conduction losses comparison between the three technologies requires the study of the P_c terms present in (4.19). In Fig. 4.13, Fig. 4.14 and Fig. 4.15, it can be seen that the losses are not negligible when the switching frequency is equal to zero. This term is related to the inverter conduction loss and it is dependent on the current. Several frequency sweep curves have been obtained from measurements by changing the current values. The intersection points between all the interpolated curves and the power axis have been collected and plotted in Fig. 4.16. These traces represent the power module conduction loss in function of the current.

As seen in Fig. 4.16, losses linear dependencies with current can be noticed using all-Si and Si-SiC. The evidence suggests that the losses are in prevalence caused by the threshold term (V_{th}) of the ON voltage drops instead of the resistive term (R_d). While, the quadratic trend can be noticed for the all-SiC, apparently in accordance with the resistive behavior of the MOSFET.

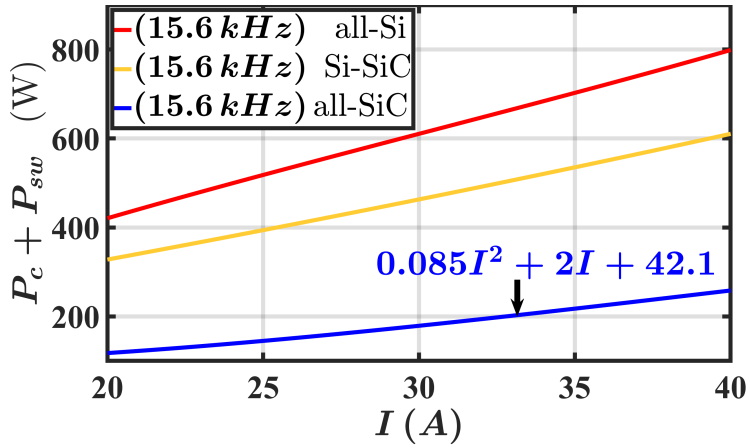
Comparing the conduction losses of the three technologies, when the current is higher than 35 A, higher conduction loss using all-SiC instead of all-Si and Si-SiC is present. It seems there is a tendency to achieve better performance thanks to better conduction proprieties of IGBT with respect to MOSFET. This evidence suggests that in some special cases all-Si and Si-SiC performance are comparable with the all-SiC. In fact, when the switching frequency is smaller than 1 kHz and the inverter current is higher than 40 A the three power modules approximately present the same total losses (Fig. 4.15).

4.6.2 Total power losses comparison

Comparison results of the total power modules losses in function of the currents are proposed and shown in Fig. 4.17(a) and Fig. 4.17(b). In these figures, power losses results in function of the current are illustrated for two switching frequencies: 7.8 kHz and 15.6 kHz. As can be noticed from both figures, the all-Si and the Si-SiC



(a)



(b)

Figure 4.17: Experiment results: power module losses in function of the current ($V_{dc} = 600$ V, $cos\varphi = 0$, $M = 0.5$). (a) 7.8 kHz and (b) 15.6 kHz.

presents a linear pattern with the current. This feature is a consequence of the linear trend presented by both conduction and the switching losses of the two technologies. Meanwhile, by comparing Fig. 4.17(a) and Fig. 4.17(b), it can be observed that the all-SiC presents an appreciable difference in the parabolic trend. It is evident from the results that for high switching frequency (Fig. 4.17(b)) the trend appears more linear with respect to the trend with a low switching frequency (Fig. 4.17(a)). This evidence suggests that for low switching frequency the conduction loss is comparable with the switching loss, while for high switching frequency the losses linearity rises because the switching loss begins to predominate the conduction loss.

Gains in performances using the novel technologies instead of all-Si are analysed and the results are given in Fig. 4.18. In this figure, the per unit losses reduction using Si-SiC and all-SiC instead of all-Si are proposed considering different working

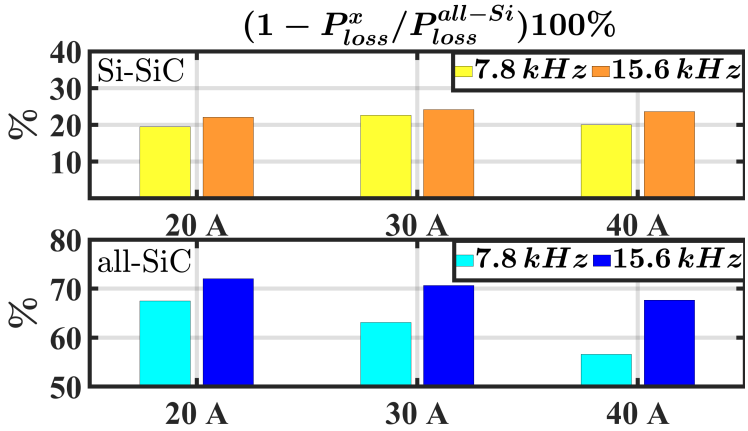


Figure 4.18: Per unit loss reductions using Si-SiC and all-SiC instead all-Si at different load conditions ($V_{dc} = 600$ V, $cos\varphi = 0$, $M = 0.5$).

conditions of the power converter.

$$LRF = (1 - \frac{P_{loss}^{x}}{P_{loss}^{all-Si}})100\% \quad ; \quad x = (\,\text{all}-\text{SiC or Si}-\text{SiC}) \tag{4.20}$$

When the all-SiC inverter works at 7.8 kHz, it can be noticed from Fig. 4.18, that for small current (20 A, 67.5%) the all-SiC loss reduction factor is higher respect to working with higher current value (40 A, 56.6%). The performance deterioration of 10.9 % is present when the current increases, because the MOSFET conduction loss predominate the IGBT conduction loss. Meanwhile, when the all-SiC inverter works at 15.6 kHz, the performances are considerably improved for all the current values with respect to lower switching frequency (i.e. 20 A, 72% and 40 A, 67.6%). This evidence suggests that the all-SiC presents more benefits in terms of losses with respect to all-Si when the switching frequency increases and the current level decreases.

By adopting an inverter with Si-SiC device, the presence of consistent gain performances for all the switching frequencies and currents values is present. An average value of performance gain for all the operational points of 22 % has been obtained.

4.7 Results summary

The most important results, that were obtained from the comparison between all-Si, Si-SiC and all-SiC devices used for an industrial application (600 V and 30 A), are summarized here.

- The converter efficiency at the nominal condition declared in Table 2.2 (97.86 %),

when the opposition method is adopted, in comparison to all-Si device, is improved 0.4% using Si-SiC and 1% using all-SiC.

- When the nominal condition was imposed from an unpowered condition to powered, the power losses of all-Si increases by 9%, while for Si-SiC and all-SiC , the power losses increased by 5% and 3%, respectively.
- Using Si-SiC instead of all-Si, switching losses are reduced by 26.5%. While using all-SiC instead of all-Si, switching losses are reduced by 81%.
- The Si-SiC and the all-Si present lower conduction losses for currents higher than 35 A, with respect to all-SiC.
- The Si-SiC is well exploited for all the currents and switching frequencies values of the converter. While using all-SiC higher exploitation is present for high switching frequency and low current value.

4.8 Conclusions

In this chapter, a literature review of converter loss measurement methods has been provided. Among all the methods proposed by the literature, the opposition method has been selected letting to reach accurate comparisons. This method has been studied in detail for three-phase ac drives. From this study, useful hints, that can be used during the experiments, have been proposed.

The losses of the converter were measured for different load conditions using a precise data acquisition system. Losses reduction has been found using Si-SiC instead of all-Si for each converter operating point. The experiments demonstrated that using the power modules based on Si-SiC, the nominal switching frequency can be increased from 8 kHz to 11.2 kHz without additional side effects. Remarkable losses reduction using all-SiC instead of all-Si and Si-SiC were measured. From the experimental results, the conduction losses were derived suggesting that for very low switching frequency and high current applications greater benefits could be found using all-Si and Si-SiC instead of all-SiC. During the experiments, by adopting all-SiC device, the converter was able to reach 19.5 kHz. Due to the limitations imposed by the IPM module fault, the converter was not able to reach higher switching frequency. Finally, at the converter nominal condition, an important efficiency increasing of 1 % was measured when all-SiC devices were used.

Chapter 5

Drive side effect comparisons between all-Si, Si-SiC and all-SiC devices

5.1 Introduction

In the last decades the use of Voltage Source Inverter (VSI) for Adjustable Speed Drives (ASDs) in the industrial field has progressively become remarkable by virtue of the simplicity, reliability, efficiency and, cost of these drives [1]. Anyway, it is known that when electric motors are connected to VSIs a series of problematics are generated in all the electric drive because fast voltages are imposed by the inverter. Issues can be found in the AC/DC, inverter, motor and in susceptible equipment located near the drive [52].

In this chapter, a literature review of most of the problems present in ASDs is provided. Subsequently, the converter designed in Chapter 3 has been connected to an electric drive. An experimental investigation of issues caused by all-Si, Si-SiC and all-SiC devices has been conducted by virtue of having the same package, layout, heat sink, connections between the power module terminals and the converter terminals. Finally, the experimental results have been compared showing the presence of an unexpected overvoltage at the power converter terminals when power module based on all-SiC device was used.

5.2 General background

Switches used nowadays in ac drives can commutate their voltages and currents very fast. As a consequence, high-frequency components that can trigger possible system resonances come into play. In this chapter, the issues present in ASDs are reviewed in detail.

5.2.1 AC drive structure

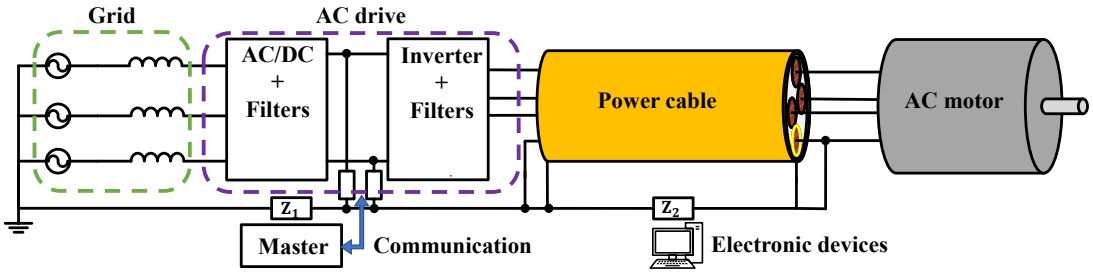


Figure 5.1: Schematic representation of a typical electric drive.

In Fig. 5.1, an AC drive is illustrated schematically. Details about the drive composition and its components are given and summarized here.

- The grid can be represented by the transformer of the power plant. The earth of the power plant can be connected in different ways: Y grounded system, High Resistance Grounding (HRG) system and unground system. The way that it is connected to the ground becomes important in the common mode solicitations presented by the drive components [53, 54, 55].
- AC/DC converter can be realized by using different converter topologies such as a three-phase rectifier or three-phase boost converter. In addition to the rectifier structure, filters are required. A filter such as LCL filter can be placed by permitting to be compliant with standards [56, 57]. Common mode filters as described in [58, 59] can be used for being compliant with standards [60].
- In low voltage applications (i.e. lower than 690 V), the most used converter topology is the three-phase two-level converter.
- Master has the task to control the AC drive (e.g. speed reference, state machine, faults, etc. etc.). Examples of masters in an industrial environment are Programmable Logic Controller (PLC).
- The cable, which connects the inverter to the motor, has been represented. Long connections (i.e. more than 3 m) between inverters and motors are very common in the industrial field.
- Z_1 and Z_2 are impedances that reproduce the ground connection of the power plant.
- Electronic devices have been represented in this equivalent scheme because they can be susceptible to common mode current generated by the ac drives.

5.2.2 AC drive issues caused by high dv/dt

Rectifier and inverter can be a source of issues in the electric drive. A list of issues encountered in the past is proposed here.

Inverter overcurrent caused by long cable

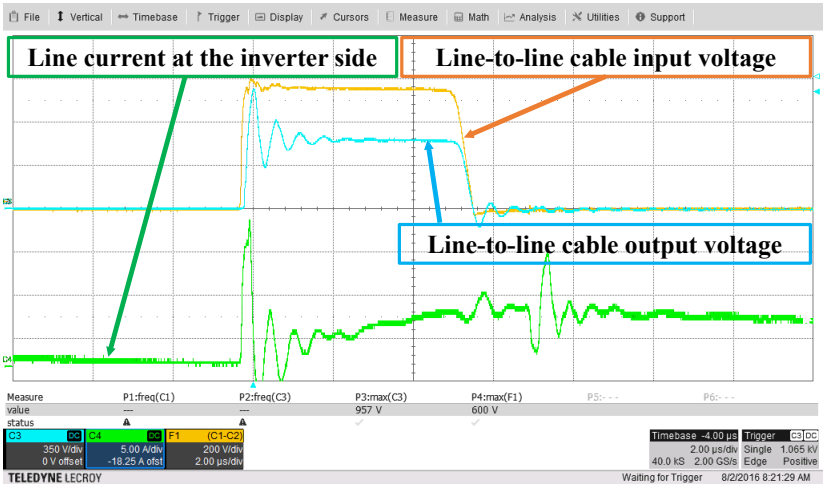


Figure 5.2: Experimental results: inverter overcurrent and motor overvoltage of an industrial drive (with a nominal power of 20 kW) connected by 12.25 m of power cable (AWG 8).

When the inverter is connected to the motor through a power cable overcurrent at the inverter side can be experienced [26, 44, 52, 61, 62, 63, 64, 65, 66, 67, 68]. The overcurrent is caused by the presence of cable parasitic capacitance. These overcurrents could have the same magnitude of the current rating of the converter, in addition, they present a high-frequency component (order of MHz). This overcurrent can cause additional losses of the power devices and trigger the overcurrent fault of the inverter [61]. In [52], an experience where an inverter was destroyed by the cable overcurrent is explained in detail.

Experimental measurement of the overcurrent seen by the converter mounted in an industrial field was conducted. The experimental results are depicted in Fig. 5.2. An overcurrent of 15 A was registered at the input of the inverter.

Inverter overcurrent caused by the motor

The capacitive current caused by the parasitic capacitance of the motor can be present when high dv/dt is imposed by the inverter [62]. This current spike can

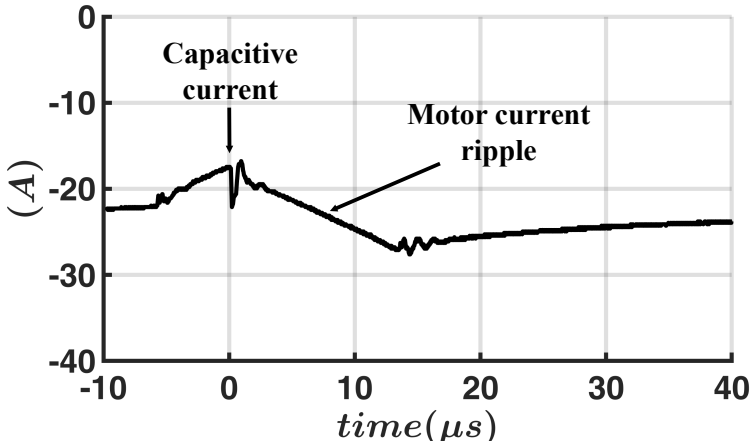


Figure 5.3: Experimental results: inverter capacitive current caused by the parasitic capacitance of the motor (with a nominal power of 20 kW).

increase the inverter losses and causes EMI issue.

The experimental measurement of the motor current driven by a Si inverter is depicted in Fig. 5.3. It can be observed from this figure two current trends: one is the motor current PWM ripple while the other one is the spike current caused by the dv/dt.

Drive components stress

In [53, 54, 55], the voltage stresses of the components (i.e. opto-isolators, PCB, sensors SMPS etc. etc.) present in the power converter have been investigated. In these works, it has been analyzed the correlation between the voltage stresses seen by the drive components, the grounding system and the inverter load capacitance (i.e. the cable). It has been demonstrated that sometimes standard design guidelines cannot be followed in the choice of the components of the drive, in fact, higher voltages appear at the terminals of the components, thus causing possible failures.

DC bus voltage pump-up

DC Bus voltage pump-up issue has been described in [69]. This phenomenon triggers the bus overvoltage fault of the inverter. This issue is present when the AC/DC is a three-phase rectifier and high capacitive currents, caused by multiple long cables placed in parallel, are present. This capacitive current causes the increase of the dc link voltage until than the protections are triggered or the capacitors explode.

5.2.3 Motor issues caused by high dv/dt

Bearing currents

The bearing of the motor can be damaged by currents caused by the voltage derivate imposed by the inverter [70]. These can generate molten pits in the bearing, hence reducing its lifetime. These currents reduce the mechanical life of the bearing. Three reasons are at the base of the problem: high dv/dt is applied to the motor parasitic capacitances, thence generating currents; common mode voltage applied by the inverter is seen from the motor bearings; the motor is connected to a well-grounded mechanical load. Details about the causes of this issue are described here.

- When high dv/dt is applied to the motor, capacitive currents are generated. These capacitive currents generate a magnetic flux, which induces a shaft voltage. The shaft voltage is applied to the two bearings of the motor. In case that this voltage overpasses the dielectric strength presented by the lubricant a current is generated [71].
- When the common mode voltage is applied by the inverter to the motor, a portion of this voltage appears at the bearing side. Again, if this voltage overpasses the dielectric strength of the lubricant a current is generated [72].
- When a well-grounded mechanical load is used (e.g. mechanical reducer is connected to the motor shaft), the leakage currents of the motor prefers to move through the bearings, instead of the motor frame [73].

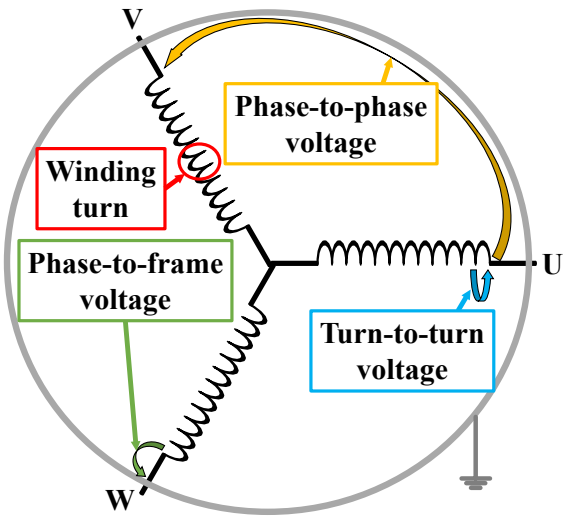


Figure 5.4: Schematic representation of all the overvoltages that can be present in electrical motors.

Stator winding insulation issues

The stator insulation of an electric machine is put under stress when it is powered by an inverter. The square wave pulses imposed by the power electronics to the winding can cause overvoltages inside the machine. The motor overvoltages can be present between two phases of the machine, between phase-to-frame and between two turns of the coil. These overvoltages are represented schematically in Fig. 5.4. High voltages generate a high electric field in the air gaps, where these gaps are present in the insulation of the winding.

When these electric fields overpass the dielectric strength of the air (3 kV/mm), partial discharges are created. Partial discharges generate ions, which bombards the winding insulation [74, 75]. This phenomenon reduces the lifetime of the motor insulation, until then a catastrophic event happens, thence causing insulation failures [76, 77].

The overvoltage rise time and its value are important in the dielectric failure mechanism. Furthermore, the frequency with which this phenomenon occurs (e.g. switching frequency) becomes important because it determines the number of stresses given to the insulation. The dielectric is present in different parts of the electric motor, such as the insulation present between two phases of the motor. Each parameter of the inverter can reduce the life of these insulations in its own way. A table, which summarized the electrical parameters that influence the life of each insulation present into the motor is shown in Table 5.1.

Table 5.1: Inverter parameters vs. Insulation life.

	phase-to-phase	phase-to-frame	turn-to-turn
Voltage peak	**yes**	**yes**	**yes**
Voltage rise time	no	no	**yes**
Electrical frequency	**yes**	**yes**	**yes**

Impedance mismatching between motor and cable

When a long cable connects the motor to the inverter, voltages higher than the inverter dc link can be experienced at the motor terminals [26, 62, 63, 64, 65, 66, 67, 68, 77, 78, 79, 80, 81, 82, 83]. This phenomenon is caused by an impedance mismatching present between the load and the power cable. In fact, the mismatching is present because the impedance presented by the motor is much greater than the characteristic impedance of the cable.

It has been demonstrated that the maximum phase-to-phase motor voltage can reach three times the bus voltage (i.e. $V_{ph,ph} = 3\,V_{dc}$). Meanwhile, the peak phase-to-frame motor overvoltage it has been demonstrated to be equal to 1.5 times the bus voltage (i.e. $V_{ph,gnd} = 1.5\,V_{dc}$) [77].

At first approximation, the overvoltages are influenced only by the reflection factor presented by the combination of the cable and the motor, when the cable is considered long and not by the rise time (see Table 5.1).

The cable is considered long when its length is higher that the critical length [62]. The critical length is defined by:

$$L_{crit} = \frac{1}{2} \cdot t_r \cdot V_d \tag{5.1}$$

where L_{crit} is the critical length, t_r is the voltage rise time imposed by the inverter and V_d is the velocity of propagation presented by the differential sequence of the three-phase cable.

Experimental results that show the presence of overvoltage at the motor terminals are depicted in Fig. 5.2. An electric motor (brushless motor) was connected to an inverter by 12.5 m of power cable. The inverter was connected to a three-phase rectifier (560 V) and overvoltage of 960 V was registered at the motor terminals (blue trace).

Winding voltage distribution vs. inverter voltage rise time

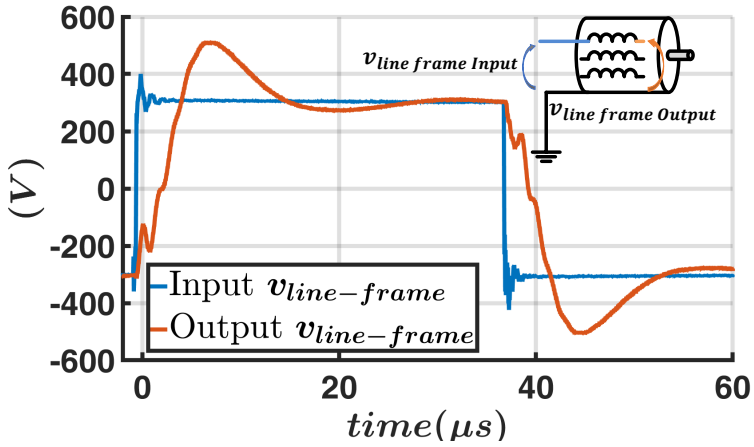


Figure 5.5: Experimental results: motor voltage distribution when high dv/dt inverter is connected to the motor (with a nominal power of 20 kW).

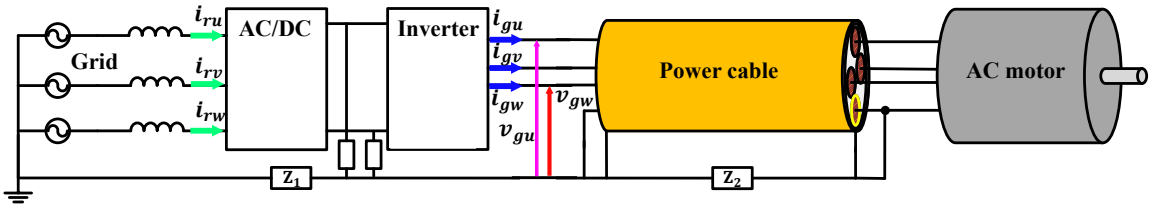
The voltage applied by the source to the motor winding is normally well distributed between each turn of the coil. Anyway, when high voltage derivate is applied to the winding undistributed voltage is present [84]. This means that when voltage with a small rise time is applied to the motor, the input voltage is not equally distributed between the turns of the coil. This phenomenon is caused by the presence of a series of capacitive (i.e. turn-to-turn and turn-to-frame leakage capacitances) and inductive elements presented by the coil. The series of these

lumped parameters emulate the behavior of a transmission line, thence this is the reason why there is a delay between the input and the output voltages.

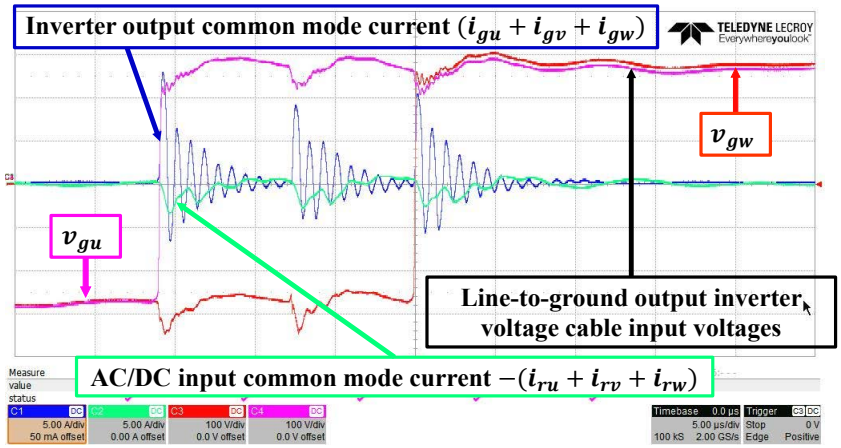
It has been demonstrated in [85], that the voltage rise time seen by an electric motor is more dangerous from a turn-to-turn perspective instead of a turn-to-frame perspective. This information has been introduced in Table 5.1.

In Fig. 5.5, results of an experiment done by feeding the motor with the SiC converter is shown. The inverter output voltage was applied between the phase and frame of a squirrel cage motor, while the motor end was left open. In blue the input voltage is shown, while in red the output voltage is shown. It can be noticed from the figure the presence of an important delay between the two voltages. This delay causes important voltage amplitudes inside the coil (turn-to-turn), which can damage the insulation presented between the winding turns.

5.2.4 EMI



(a)



(b)

Figure 5.6: Experiment results: (a) Scheme of the experimental setup, (b) common mode currents present in the drive (with a nominal power of 20 kW).

High-frequency phenomena are present when voltages and currents are switched by fast devices [52].

An example of experimental results of an issue caused by fast devices is represented in Fig. 5.6. Experimental results were obtained by using a complete drive as schematically shown in Fig. 5.1. A 20 kW electric drive connected by 35 m of cable was used. Important current values were recorded during the tests: at the rectifier stage, a peak of almost 2.5 A was registered. At the inverter terminals a peak of almost 10 A every time that an inverter leg switches was registered. In addition, by using the same experimental setup a common mode current of 28 A was registered. This condition corresponds to the moment when the motor is controlled with a reference speed equal to zero (i.e. very common in axis applications). The amplitude (28 A) and the frequency (1.2 MHz) of this current can be very dangerous for electronic devices placed near the cable from conducted and radiated emissions [86].

Communication issues

The electric drive in most of the applications is always controlled by a master. Thence, a communication channel between the converter and the master is required. As observed in Fig. 5.6, important values of common mode current can be present. This current can cause data-transmission failure, thence affecting communication [87].

5.3 Drive issues experimental comparisons by using converter based on all-Si, Si-SiC and all-SiC devices

The problems present in electric drive, when high dv/dt converters are used, have been recalled previously (see Chapter 5.2).

By increasing the voltage derivate imposed by the inverter to the cable, issues previously described become worse. Therefore, a detailed investigation is required when inverter based on SiC devices are adopted in the electric drive.

In this chapter, experimental comparisons of the issues presented in the drive between the standard technologies (all-Si) and the new ones (all-SiC) are proposed. The Si-SiC has not been included in the study because it presents the same voltage rise time of the all-Si.

5.3.1 Experimental setup

A schematic representation of the experimental setup is shown in Fig. 5.7. The details and the descriptions of each component of the electric drive are explained

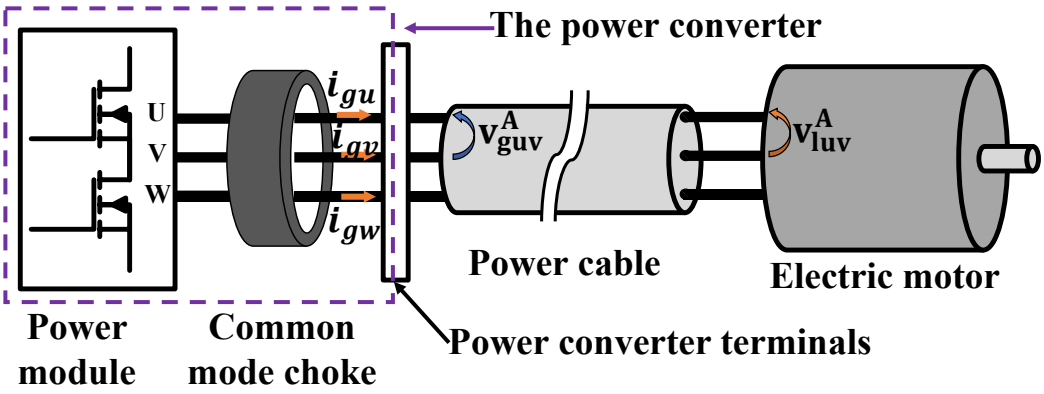


Figure 5.7: Schematic representation of the experimental setup.

as follows.

- An isolating AC/DC with imposed a voltage equal to 600 V was used.
- The cable and motor ground were connected to the middle point of two series connected electrolytic capacitors linked to the bus inverter (2 X 3.3 mF 350 V). This connection permits to emulate the ground connection of a real electric drive (i.e. TN networks).
- The converter designed in Chapter 3 was used during the experiment. All-Si inverter and all-SiC inverter with the same package, PCB layout and mechanical structure were adopted.
- A common-mode choke has been introduced in the converter with the aim to mitigate the common-mode current of the system [25, 88]. The installed filter is composed by a toroidal inductor with the sequent dimensions: $\emptyset_{est}$ = 63 mm × $\emptyset_{int}$ = 25 mm × 38 mm. This toroidal inductor is made of SM-100 and it presents an inductance value of 25 $\mu H/N^2$.
- 2 m and 5 m lengths of power cable were adopted during the experiments. Four-pole cables with screen were used. The selected cables have a nominal section compatible with the rated current of the drive (8 AWG).
- A 15 kW induction motor was connected to the inverter by means of a cable.

In all the tests, one inverter of the power converter was turned on. V/Hz motor control strategy was adopted by the converter. No mechanical load has been attached to the shaft of the electric motor. The electric motor was running during the tests at a mechanical speed of 1500 rpm.

The rise time of the voltage imposed by the inverter, in the worst-case scenario, was measured and the results are summarized in Table 5.2. By assuming the typical

velocity of propagation of power cable ($V_d = 0.15 \cdot 10^9$ m/s) the critical length is calculated by using (5.1).

Table 5.2: Critical length vs. inverter rise times based on all-Si, Si-SiC and all-SiC devices.

	all-Si	Si-SiC	all-SiC
Voltage rise time	28 ns	120 ns	120 ns
Critical length	2.1 m	9 m	9 m

5.3.2 Inverter issues comparison

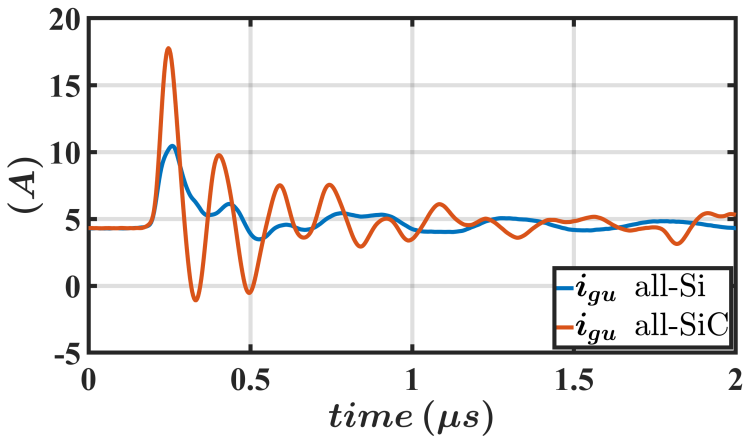


Figure 5.8: Experimental results: inverter and motor connected by 2 m of cable. Inverter phase current (i_{gu}) when all-Si and all-SiC devices are used.

The overcurrent present at the inverter side is investigated in this section. In detail, the overcurrents caused by the connection cable are analyzed and compared. The observations are done for Fig. 5.8 and Fig. 5.9 and they are summarized below.

- In Fig. 5.8, when all-SiC device is used, a higher peak phase current (i_{gu}) is presented with respect to the one caused by all-Si device. The overcurrent caused by the commutation is equal to 13.5 A when all-SiC is used, while all-Si causes an overcurrent equal to 6 A. As a consequence, the rms current of the switches are higher thus causing higher conduction losses.
- In Fig. 5.9, when all-SiC device is used, a higher peak phase current (i_{gu}) is presented with respect to one caused by all-Si device. The overcurrent caused by the commutation is equal to 14.2 A when all-SiC is used, while all-Si causes an overcurrent equal to 9.72 A. As a consequence, the rms current of

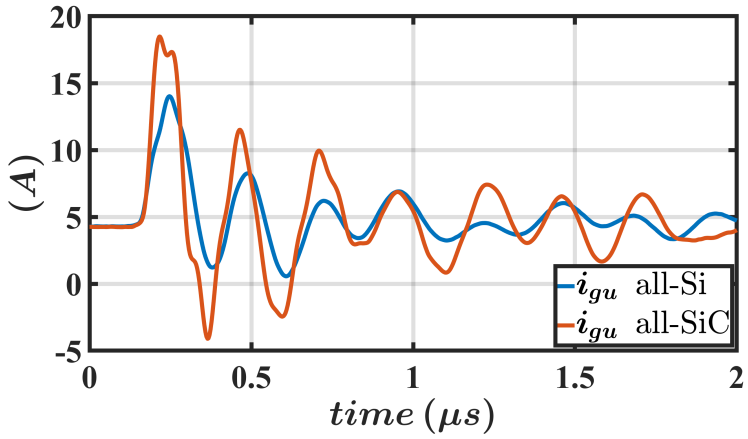


Figure 5.9: Experimental results: inverter and motor connected by 5 m of cable. Inverter phase current (i_{gu}) when all-Si and all-SiC devices are used.

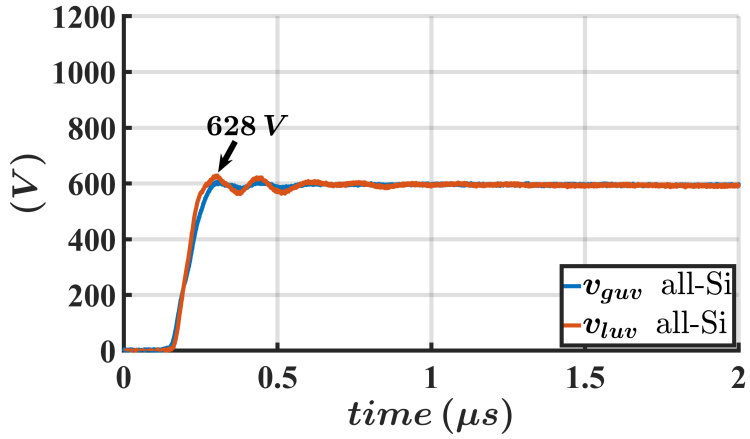
the switches are higher thus causing higher conduction losses. In addition, it can be noticed that traces of Fig. 5.8 present a higher fundamental frequency instead of the traces present in Fig. 5.9. The difference in frequency is caused by the difference in length presented by the cables [62].

In conclusion, the results obtained from the experiment suggest that for each cable length, when all-SiC devices are used, the peak current becomes worse.

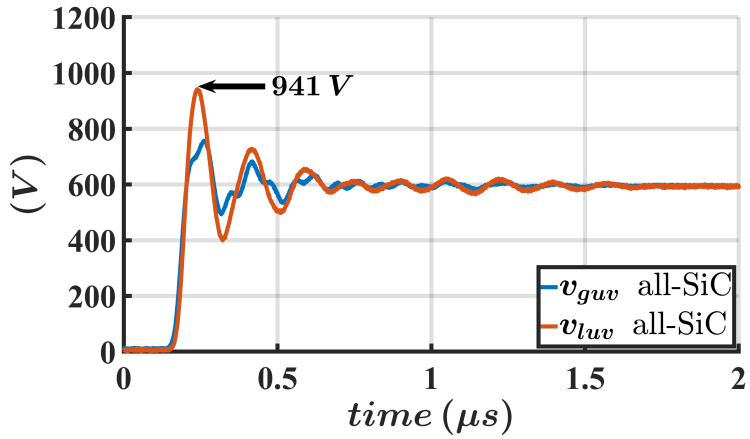
5.3.3 Motor issues comparison

The overvoltage present at the motor side is investigated in this section. In detail, the overvoltages caused by the mismatching between the cable and the motor are analyzed and compared. In Fig. 5.10 and in Fig. 5.11, the experimental results are depicted. The blue traces represent the input cable voltage, thence the voltages at the converter terminals. The red traces denote the output cable voltage, thence the voltages at the motor terminals. The observations are done for Fig. 5.10 and Fig. 5.11 and they are summarized below.

- In Fig. 5.10(a), it can be seen that using all-Si no overvoltage is present at the motor side, because of smaller cable respect the critical length. However, in Fig. 5.10(b) as expected overvoltage at the motor side is present. In fact, the cable presents a length comparable with the critical length (see Table 5.2).
- In Fig. 5.11(a), it can be observed the presence of overvoltage using all-Si because of cable length is starting to reach the critical length. Whereas, the all-SiC presents already the maximum motor overvoltage as can be noticed from Fig. 5.11(b).



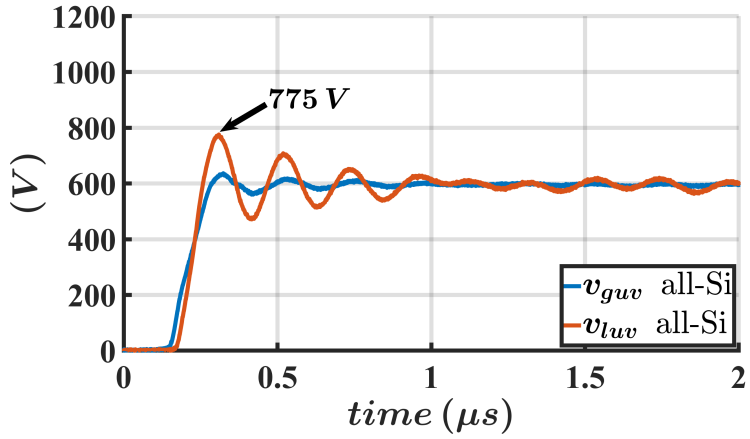
(a)



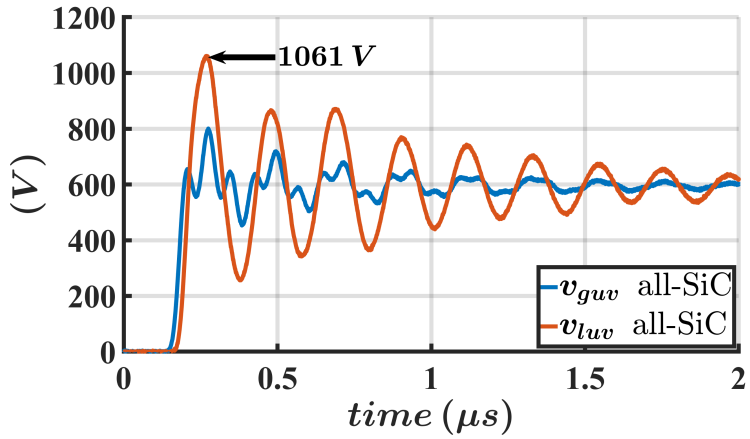
(b)

Figure 5.10: Experiment results: inverter and motor connected by 2 m of cable. (a) Inverter and motor line-to-line voltages when all-Si is used. (b) Inverter and motor line-to-line voltages when all-SiC is used.

- In Fig. 5.10(b) and Fig. 5.11(b), it can be found presences of oscillating voltage at the inverter terminals instead of seeing a smooth voltage as depicted in Fig. 5.10(a) and Fig. 5.11(a). In addition, the voltage ringing causes an overvoltage at the inverter terminals even reaching 800 V. Additional, tests were conducted connecting directly the load to the power module terminators, showing no important voltage ringing at the input cable. Thus, this evidence suggests that this phenomenon is caused by the differential-mode leakage inductance presented by the common-mode choke plus the inductance of the remaining piece of cable [88]. As a matter of fact, the connecting cable presents a length (25 cm) comparable with the critical length presented when all-SiC is used. Thus, the wiring should be reduced in length in order to



(a)



(b)

Figure 5.11: Experiment results: inverter and motor connected by 5 m of cable. a) Inverter and motor line-to-line voltages when all-Si is used. b) Inverter and motor line-to-line voltages when all-SiC is used.

avoid this problem. However, this cable presents two aims: create an electrical connection between the power modules and the power converter terminals and permits to winding the common mode choke. As a consequence, the easier solution is to place the power module terminals as close as possible to the power converter terminals. Meanwhile, reduce the cable filter length could be complicated, leading thus the side effects unavoidable.

5.3.4 EMI issues comparison

The common mode current present at the inverter side is investigated in this section. In detail, the common mode current caused by the connection cable are

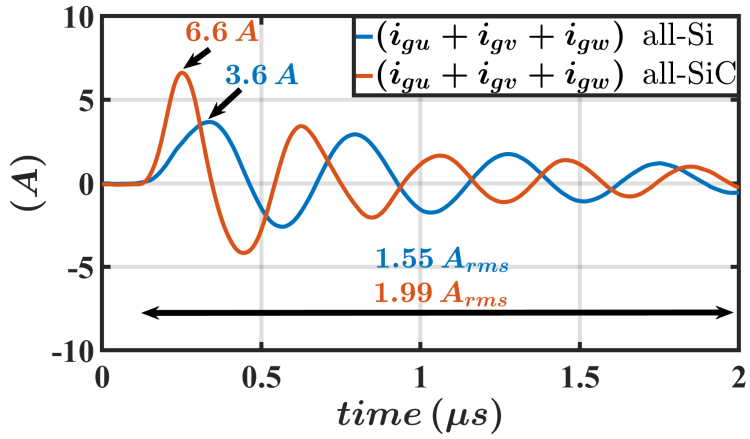


Figure 5.12: Experiment results: inverter and motor connected by 2 m of cable. Inverter common mode currents when all-Si and all-SiC devices are used.

analyzed and compared. The experiments were conducted by removing the common mode filters present in Fig. 3.27(c). In this way, this problem can be assessed without mitigating it.

A comparison between the experimental results is proposed in Fig. 5.12. It can be noticed from this figure that the common mode current present when all-SiC devices is higher. In addition, it can be noticed that also the rms value of the common mode current becomes higher when all-SiC devices are used. In conclusion, experimental results suggest that the EMI when all-SiC devices are used are exacerbated.

5.4 Conclusions

It is widely accepted that when electric motors are connected to voltage source inverters, a series of issues are present in all drives. In this chapter, a review of the main problems exist in the drive has been provided. In addition, experimental measurement results are provided in order to confirm the presence of these problems.

An experimental comparison of the drive issues, obtained by changing the technologies between all-Si, Si-SiC and all-SiC devices, has been conducted. During the experiments, same converter (i.e. power module package, layout, heat sink, connections between the power module terminals and the converter terminals), cable and motor were used by permitting to have a rigorous investigation. It has been observed that all the problems previously described became worst when all-SiC technology was used (i.e. inverter overcurrent, common mode current and motor overvoltage).

Overvoltage inside and outside the converter, caused by the small voltage rise

time, were observed when all-SiC power module was adopted. It has been discovered the presence of overvoltage at the converter terminal. This overvoltage can be reduced by shortening the cable connecting the power module to the converter terminals during the converter design process. In addition, motor overvoltages were observed with only 2 m of cable connecting the converter to the motor.

By virtue of all the problems introduced by these novel fast devices, a detailed analysis of the drive using distributed parameters is required in order to find solutions that could mitigate these issues.

Chapter 6

Electric Drive Modelling

Part of the work described in this chapter has been previously published in [62, 89].

6.1 Introduction

In Chapter 5, the designed power converter has been connected to an electric motor. The presence of drawbacks as motor overvoltage and inverter overcurrent were registered with also few meters of power cable. Furthermore, it has been noticed that these issues become worst when SiC MOSFET is used. In order to avoid these problems, a rigours mathematical analysis of all the electric drive is required.

In this chapter, the basic theory of distributed parameter line has been revised by focusing on modeling of single and multi-conductor transmission lines. A rigours formula, which predicts the overvoltage at the load side as a function of impedance mismatching and voltage rise time, has been discovered. Subsequently, the transmission line model has been merged with the model of the drive components permitting to understand the motor overvoltage phenomenon. By virtue of the rigours formulation, new concepts about motor overvoltage, which can be used by inverter software designer and power cable designer, have been discovered and validated by means of simulation tools.

6.2 Two-conductor line

6.2.1 Solution to transmission line equations

The model of a cable is composed of an infinite series of circuit elements [42]. In Fig. 6.1, an infinitesimal piece of transmission line, which is considered uniform

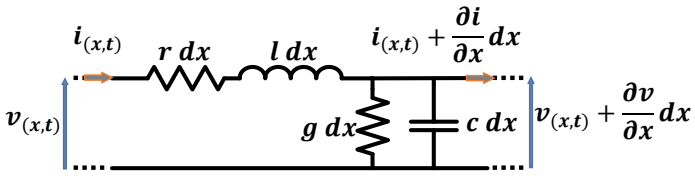


Figure 6.1: Schematic representation of an elementary component of transmission line.

(i.e. line parameters are the same in all the point) and with loss, is shown. In this equivalent model:

- r represents the resistance per unit length $[\,\Omega\,/\,\mathrm{m}]$;
- l represents the inductance per unit length $[\,\mathrm{H}\,/\,\mathrm{m}]$;
- g represents the conductance per unit length $[\,\mathrm{S}\,/\,\mathrm{m}]$;
- c represents the capacitance per unit length $[\,\mathrm{F}\,/\,\mathrm{m}]$.

By writing Kirchhoff's voltage law for the circuit shown in Fig. 6.1, the sequent partial differential equation is obtained:

$$-\frac{\partial v(x,t)}{\partial x} = ri\,(x,t) + l\frac{\partial i(x,t)}{\partial t}. \tag{6.1}$$

By writing Kirchhoff's current law for the circuit shown in Fig. 6.1, the sequent partial differential equation is obtained:

$$-\frac{\partial i(x,t)}{\partial x} = gv\,(x,t) + c\frac{\partial v(x,t)}{\partial t}. \tag{6.2}$$

The voltages and the currents in each section of the transmission line are required, but using only (6.1) and (6.2) these electrical variables cannot be derived. The variables can be found by doing the partial derivatives of (6.1) and (6.2) with respect to the position and the time:

$$-\frac{\partial^2 v(x,t)}{\partial^2 x} = r\frac{\partial i(x,t)}{\partial x} + l\frac{\partial^2 i(x,t)}{\partial x \partial t} \tag{6.3}$$

$$-\frac{\partial^2 v(x,t)}{\partial x \partial t} = r\frac{\partial i(x,t)}{\partial t} + l\frac{\partial^2 i(x,t)}{\partial^2 t} \tag{6.4}$$

$$-\frac{\partial^2 i(x,t)}{\partial^2 x} = g\frac{\partial v(x,t)}{\partial x} + c\frac{\partial^2 v(x,t)}{\partial x \partial t} \tag{6.5}$$

$$-\frac{\partial^2 i(x,t)}{\partial x \partial t} = g\frac{\partial v(x,t)}{\partial t} + c\frac{\partial^2 v(x,t)}{\partial^2 t}. \tag{6.6}$$

where, all these equations are second-order partial differential equations. A simplified solution of the partial differential equations can be found by imposing $r=0$ and $g=0$ (i.e. lossless transmission line). Thence, the sequent equations are obtained:

$$\frac{\partial^2 v(x,t)}{\partial^2 x} = lc\frac{\partial^2 v(x,t)}{\partial^2 t} \tag{6.7}$$

$$\frac{\partial^2 i(x,t)}{\partial^2 x} = lc\frac{\partial^2 i(x,t)}{\partial^2 t}. \tag{6.8}$$

The solution of (6.7) and (6.8) can be found by recalling the solving method related to a generic waveform (e.g. one-dimensional wave). A generic one-dimensional wave can be described by:

$$\frac{\partial^2 W(x,t)}{\partial^2 t} = c^2\frac{\partial^2 W(x,t)}{\partial^2 x} \tag{6.9}$$

where, W is the function associated with the wave and c is a constant. The general solution of (6.9) is defined by:

$$W_{(x,t)} = F_{(x-tc)} + G_{(x+tc)} \tag{6.10}$$

where, $F_{(x-tc)}$ is the backward traveling wave, while $G_{(x+tc)}$ is the forward traveling wave.

The same solving method can be applied to (6.7) and (6.8). The two solutions are described by:

$$V_{(x,t)} = V^{+}_{(x+tU)} + V^{-}_{(x-tU)} \tag{6.11}$$

$$I_{(x,t)} = I^{+}_{(x+tU)} + I^{-}_{(x-tU)} \tag{6.12}$$

$$I_{(x,t)} = \frac{V^{+}_{(x+tU)}}{Z} - \frac{V^{-}_{(x-tU)}}{Z} \tag{6.13}$$

where, U represents the velocity of propagation and Z is the line characteristic impedance (called also surge impedance). The literary convention applied to the signal traveling waveforms are described as follows:

- A forward traveling waveform moves from the input to the output side. This wave is identified by the sequent superscript: "+" (e.g. v_l^{1+} is the first reflected voltage which moves from the input to the output cable)
- A backward traveling waveform moves from the output to the input side. This wave is identified by the sequent superscript: "-" (e.g. v_l^{1-} is the first reflected voltage which moves from the output to the input cable)

The transmission line parameters can be calculated using:

$$U = \sqrt{\frac{1}{lc}} \tag{6.14}$$

$$Z = \sqrt{\frac{l}{c}} \tag{6.15}$$

where, the velocity of propagation of the waveform cannot be major than the light speed. Once the propagation speed has been defined, the propagation delay of a transmission line with a length equal to "D" can be expressed as:

$$t_d = \frac{D}{U} \tag{6.16}$$

where, U is the velocity of propagation. t_d represents the time taken by a waveform (i.e. voltage or current) to travel from one side to the other side of the transmission line.

By using (6.11) and (6.12) the voltages and the currents in each part of the transmission line are known.

6.2.2 Boundary conditions

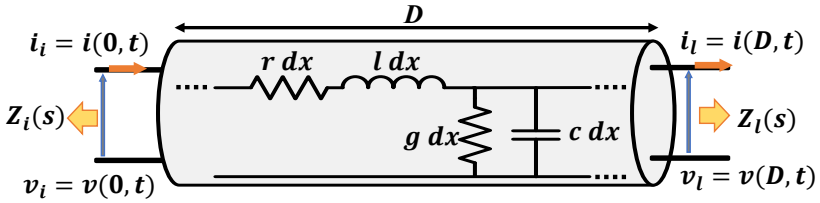


Figure 6.2: Two-conductor transmission line: schematic details about the impedances saw at the input and output cable terminations.

Eq. (6.11) and (6.12) need to be correlated with a cable with finite length (Fig. 6.2). The value of the cable length is represented by ("D"). At the cable terminations, circuit elements could be present (e.g. inductor, generators, resistor). An equivalent network can be derived at the cable terminals (e.g. using Thevenin's theorem). As a consequence, in $x = 0$ and in $x = D$, the correspondents' electrical variables are present: v_i, i_i, v_l and i_l. The "i" subscripts identify the variables at the cable input, while the "l" subscripts identify the variables at the cable output side.

v_i, i_i, v_l and i_l are composed of a series of reflected waveforms as described for example by:

$$v_l = v_l^{1+} + v_l^{1-} + v_l^{2+} + \cdot\cdot = \sum_{n=1}^{n=\infty} v_l^{n+} \tag{6.17}$$

Each time that a signal reached the load side or the generator side a reflected signal is generated. The amplitude of the reflected signal depends on the reflection coefficients. The reflection coefficient at the generator side can be defined:

$$\Gamma_i = \frac{v_i^{(n)+}}{v_i^{(n-1)-}} = \frac{Z_{i(s)} - Z}{Z_{i(s)} + Z} \tag{6.18}$$

where, $Z_{i(s)}$ is the impedance seen at the generator terminals and Z is the characteristic impedance of the cable. The reflection coefficient at the load side can be defined:

$$\Gamma_l = \frac{v_l^{+}}{v_l^{-}} = \frac{Z_{l(s)} - Z}{Z_{l(s)} + Z} \tag{6.19}$$

where, $Z_{l(s)}$ is the impedance seen at the cable input terminals.

6.3 Load overvoltage and generator overcurrent

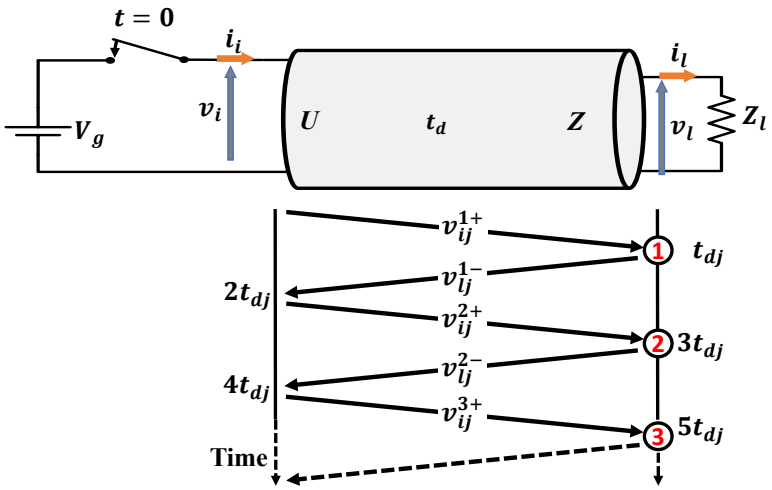


Figure 6.3: Schematic representation of a transmission line connected to a voltage step generator with the corresponding Bewley lattice diagram.

In this section, the load overvoltage and the generator overcurrent are studied. The investigation is conducted by means of an equivalent circuit, which is shown in Fig. 6.3. In this figure, the equivalent circuit is composed of a voltage generator and a resistor. In addition, the correspondent Bewley lattice diagram is introduced. This diagram is a space-time diagram, which presents space measured in horizontally and time vertically.

The circuit has been simulated by means of PSpice simulations. The schematic of the simulated circuit is shown in Fig. 6.4. It can be noticed from this figure that

a lossless transmission line has been implemented because only the characteristic impedance (Z) and the propagation delay (t_d) are present. Furthermore, a voltage generator which allows the rise time to be varied has been introduced.

Different operating conditions of the circuit shown in Fig. 6.4 are investigated:

- output cable terminated by an open circuit;
- output cable terminated by a resistor;
- output cable terminated by a resistor and the voltage rise time is changed.

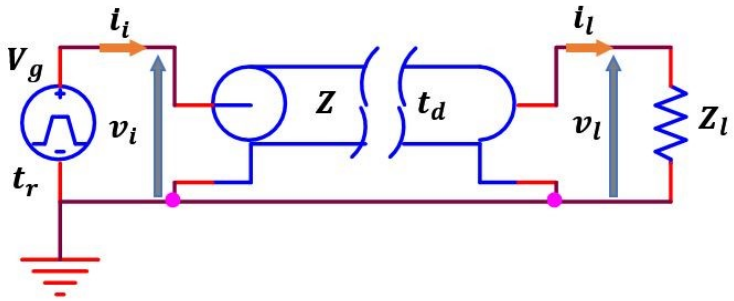


Figure 6.4: PSpice schematic circuit.

6.3.1 Cable connected to an open circuit

Starting from the model described above (Fig. 6.4), an infinite impedance has been placed at the load side. This condition corresponds to an open circuit load. The reflection coefficients are equal to:

- reflection coefficient at the output cable is equal to $"+1"$;
- reflection coefficient at the input cable is equal to $"-1"$;

Simulations were conducted and the results are depicted in Fig. 6.5 and Fig. 6.6. All the simulation results have been represented in per unit. The voltages are normalized with respect to the input peak voltage (V_g). The currents are normalized with respect to the input peak current (V_g/Z).

The sequent observations can be conducted from the simulation results depicted in Fig. 6.5.

- The generator applies the voltage to the cable. This voltage arrives at the load side with a time delay equal to t_d;
- The load voltage is twice the generator voltage. This is caused by the impedance matching presented at the load side.

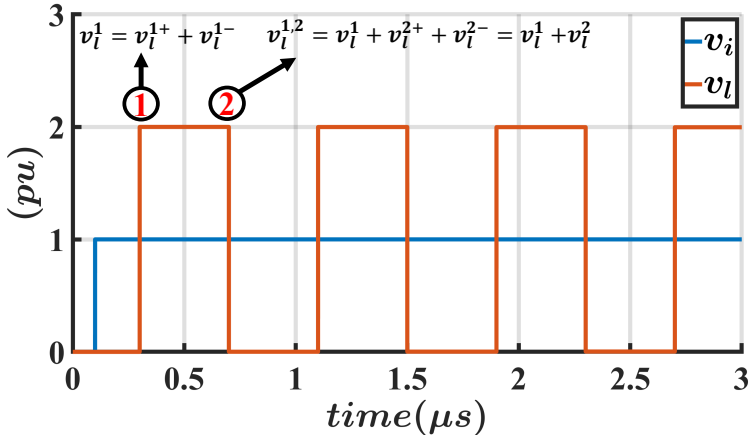


Figure 6.5: Step response of a lossless line: input and output voltages ($Z = 25\,\Omega$, $t_d = 200\,\text{ns}$, $Z_l = \infty$ and $\Gamma_l = 1$).

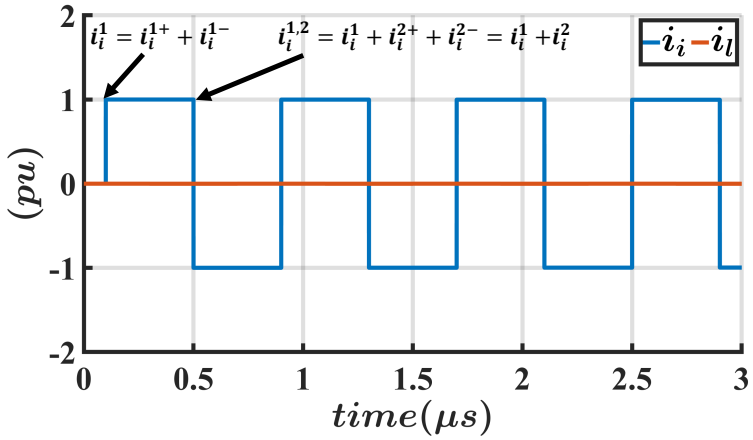


Figure 6.6: Step response of a lossless line: input and output currents ($Z = 25\,\Omega$, $t_d = 200\,\text{ns}$, $Z_l = \infty$ and $\Gamma_l = 1$).

- No damping effect is offered by the load. In fact, the voltage is not damped because no resistive element was introduced in the simulation.

The sequent observations can be conducted from the simulation results depicted in Fig. 6.6.

- At the generator side, instead of having zero current (because the load is an open circuit) there is the presence of an overcurrent which amplitude is equal to V_g/Z. The current is inversely proportional to the characteristic impedance (Z). As much the characteristic impedance is low as the overcurrent is high.
- The generator current is not damped because no resistive element has been introduced in the simulation. It can be noticed that the generator current

presents a mean value equal to zero. This means that once energy is inserted in the circuit

$$E = \frac{V_g^2}{Z} \cdot 2t_d = V_g^2 \cdot 2cD \tag{6.20}$$

energy bouncing (E) between cable and generator is present. This is due to the fact that the load cannot receive the energy because it is an open circuit.

6.3.2 Impedance load major than cable surge impedance

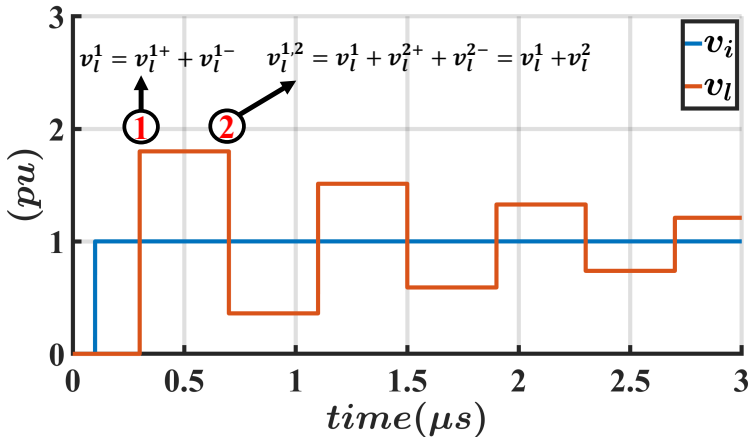


Figure 6.7: Step response of a lossless line: input and output voltages ($Z = 25\,\Omega$, $t_d = 200\,\text{ns}$, $Z_l = 225\,\Omega$ and $\Gamma_l = 0.8$).

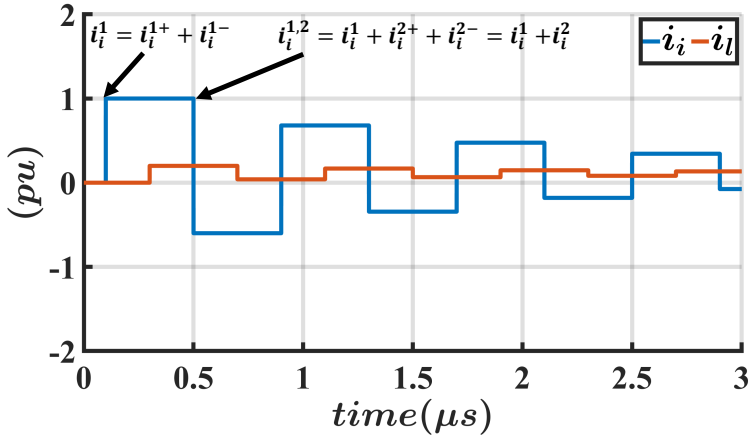


Figure 6.8: Step response of a lossless line: input and output currents ($Z = 25\,\Omega$, $t_d = 200\,\text{ns}$, $Z_l = 225\,\Omega$ and $\Gamma_l = 0.8$).

An impedance has been placed at the load side. The reflection coefficients are equal to:

- reflection coefficient at the load side is equal to " + 0.8";
- reflection coefficient at the input side is equal to " − 1";

Simulations have been conducted and the results are depicted in Fig. 6.7 and Fig. 6.8.

As can be noticed from Fig. 6.7, at the load side there is the presence of an overvoltage, but this time is lower than twice the voltage generator amplitude. Furthermore, this time the load overvoltage is damped out because a resistive element is present in the circuit (i.e. load resistance).

As can be noticed from Fig. 6.8, at the generator side, the peak current is still the same (V_g/Z). Anyway, the generator current is damped out during the successive reflections.

6.3.3 Load overvoltage vs. generator voltage rise time

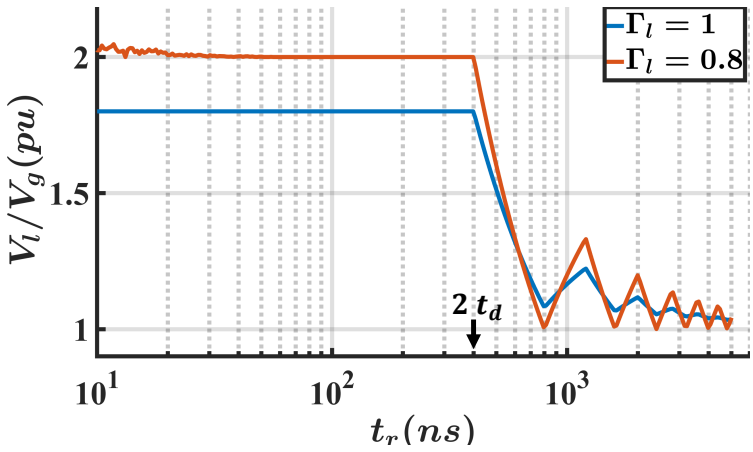


Figure 6.9: Peak load voltage caused by the mismatching, as a function of the generator voltage rise time ($Z = 25\,\Omega$, $t_d = 200\,\text{ns}$).

In Fig. 6.5, Fig. 6.6, Fig. 6.7, and Fig. 6.8, simulation results have been proposed by using a step voltage generator. This involved the voltage rise time (t_r) presented by the voltage generator is equal to zero.

It has been demonstrated in the past, that load overvoltage is reduced or canceled when the rise time becomes major than two times the propagation delay of the cable [62, 70, 90]. The not correct formula, which relates the peak load voltage and the rise time have been proposed [90, 91, 92, 93, 94, 95, 96]. In this section, the relation between the generator voltage rise time (t_r) and the propagation delay (t_d) of the transmission line are investigated. Moreover, the correct formula, which related the peak load voltage vs. the rise time, is derived and validated by means of simulations.

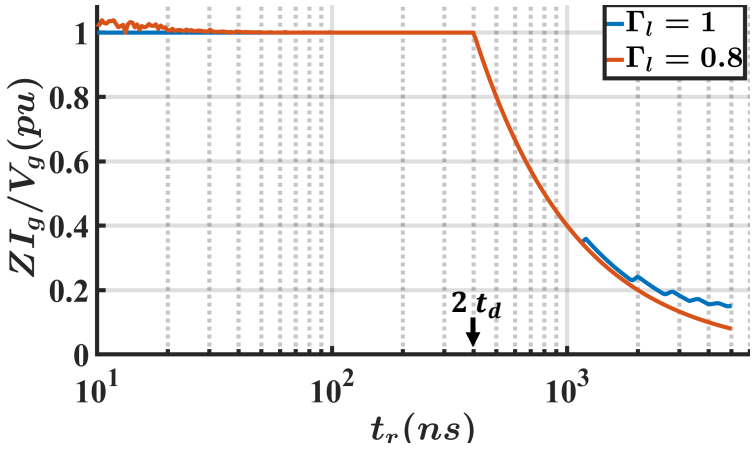


Figure 6.10: Peak generator current caused by the cable, as a function of the generator voltage rise time ($Z = 25\,\Omega$, $t_d = 200\,\text{ns}$).

PSpice simulations

PSpice simulations have been conducted by changing the voltage rise time and finding the maximum load overvoltage. The simulation results are depicted in Fig. 6.9 and Fig. 6.10. In accordance with many works proposed in the past [62, 90, 97, 98], it can be noticed from Fig. 6.9 that the load overvoltage is reduced, when the voltage rise time is major than twice the propagation delay of the transmission line ($2t_d$). The same improvement can be observed in the generator. In fact, as can be seen from Fig. 6.10 the generator overcurrent is reduced too. As a result of the simulations, the important note that needs to be highlighted from the simulation is:

$$D_{crit} = \frac{1}{2} \cdot t_r \cdot U \tag{6.21}$$

where D_{crit} is the critical length. When the cable length (D) exceeds the critical length, the maximum overvoltage is always present.

By observing (6.21), it can be noticed that with very high-speed devices (i.e. small t_r) the critical length is very small for the same velocity of propagation (U). Considering the typical velocity of propagation of power cables, that approach half the speed of the light, and using the voltage rise times derived in Chapter 5, critical length for IGBT can be 9 m while for SiC can be 2.25 m.

Proposed formula

Considering all the information collected, it is better to work with cable length lower than the critical length. A formula which predicts the peak load voltage when

the rise time is high enough is proposed in:

$$\begin{cases} V_l = V_g((1+\Gamma_l)) \quad ; \quad t_r < 2t_d \\ V_l = V_g((1+\Gamma_l) - (\Gamma_l + \Gamma_l^2)(1 - \frac{2t_d}{t_r})) \quad ; \quad 2t_d \leq t_r \leq 4t_d \end{cases} \tag{6.22}$$

where this function is discontinuous and defined in parts and Γ_l is the load reflection coefficient, t_d is the propagation delay of the transmission line and t_r is the rise time of the generator. In Fig. 6.11, comparison between the formula and the simulations results are depicted. It can be identified in this figure that a good matching between the formula and the simulations results is obtained.

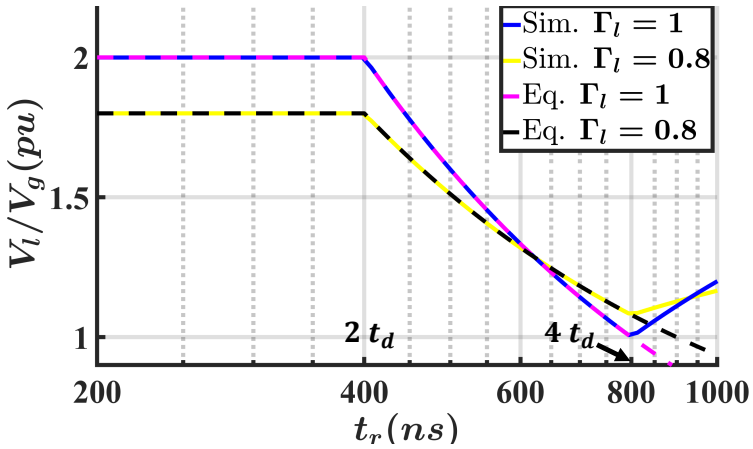


Figure 6.11: Zoomed portion of Fig. 6.9: load surge voltage derived from simulations and formulae. Dotted lines represent the formulae and continuous lines are the simulations results ($Z = 25\,\Omega$, $t_d = 200\,\text{ns}$).

6.4 Multiconductor transmission line

The equations previously derived are valid for a two-conductor line, thence the overvoltage present at the load side has been studied. Many authors investigate the motor overvoltage issue by using the equivalent two-conductor line [64, 78, 82, 99, 100, 101]. This model becomes valid for study the phase-to-phase motor overvoltage. However, the phase-to-ground overvoltage present at the motor side in most of the works escape scrutiny. The phase-to-ground overvoltage needs to consider both the differential and the common mode components of the voltage imposed by the cable. For this reason, a complete model of the cable is required.

6.4.1 Solution to transmission line equations

The model of the three-phase cable is composed of an infinite series of circuit elements [42, 62]. In Fig. 6.12, the infinitesimal piece of a three-phase cable is shown. This circuit is adopted for a uniform lossy transmission line (i.e. line parameters are the same in all the points of the transmission line). In this equivalent model:

- r_u, r_v and r_w are the per unit length resistances of the phases, while r_g is the per unit length resistance of the ground conductor [Ω / m];
- l_u, l_v and l_w are the per unit length self-inductance of the phases, while l_g is the per unit length inductance of the ground conductor [H / m];
- m_{uv}, m_{uw} and m_{vw} are the per unit length mutual inductance between the phases, while m_{ug}, m_{vg} and m_{wg} are the per unit length mutual inductance between the phase and the ground conductor [H / m];
- c_{uv}, c_{uw} and c_{vw} are the per unit length capacitance between the phases, while c_{ug}, c_{vg} and c_{wg} are the per unit length capacitance between the phases and the ground; [F / m]
- g_{uv}, g_{uw} and g_{vw} are the per unit length capacitance between the phases, while g_{ug}, g_{vg} and g_{wg} are the per unit length conductance between the phases and the ground [S / m];

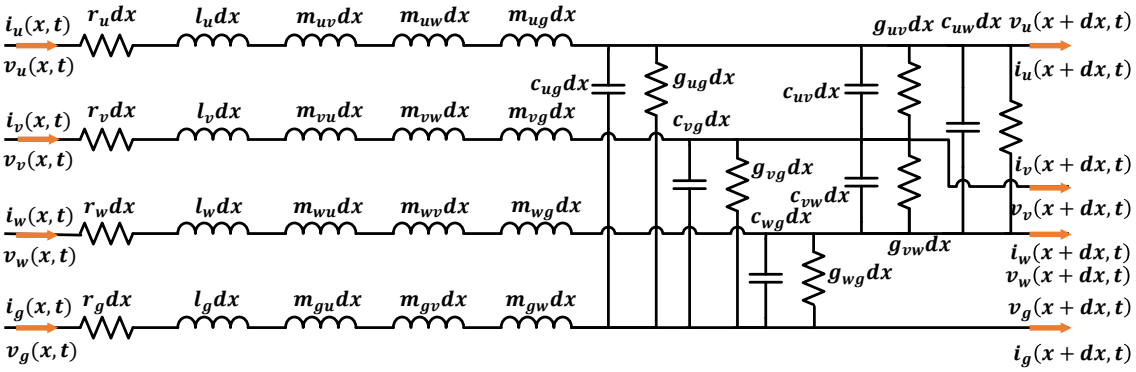


Figure 6.12: Four-conductor transmission line: schematic representation of an elementary component of transmission line.

By writing Kirchhoff's voltage law for the circuit shown in Fig. 6.12, the sequent

partial differential equations are obtained:

$$\begin{aligned} -\frac{\partial v_{ug}(x,t)}{\partial x} &= [r_u + r_g]\, i_u(x,t) + [r_g]\, i_v(x,t) + [r_g]\, i_w(x,t) \\ &\quad + [l_u - 2m_{ug} + l_g]\, \frac{\partial i_u(x,t)}{\partial t} \\ &\quad + [l_g + m_{uv} - m_{ug} - m_{vg}]\, \frac{\partial i_v(x,t)}{\partial t} + [l_g + m_{uw} - m_{ug} - m_{wg}]\, \frac{\partial i_w(x,t)}{\partial t} \end{aligned} \tag{6.23}$$

$$\begin{aligned} -\frac{\partial v_{vg}(x,t)}{\partial x} &= [r_v + r_g]\, i_v(x,t) + [r_g]\, i_u(x,t) + [r_g]\, i_w(x,t) \\ &\quad + [l_v - 2m_{vg} + l_g]\, \frac{\partial i_v(x,t)}{\partial t} \\ &\quad + [l_g + m_{uv} - m_{ug} - m_{vg}]\, \frac{\partial i_u(x,t)}{\partial t} + [l_g + m_{vw} - m_{vg} - m_{wg}]\, \frac{\partial i_w(x,t)}{\partial t} \end{aligned} \tag{6.24}$$

$$\begin{aligned} -\frac{\partial v_{wg}(x,t)}{\partial x} &= [r_w + r_g]\, i_w(x,t) + [r_g]\, i_v(x,t) + [r_g]\, i_u(x,t) \\ &\quad + [l_w - 2m_{wg} + l_g]\, \frac{\partial i_w(x,t)}{\partial t} \\ &\quad + [l_g + m_{vw} - m_{wg} - m_{vg}]\, \frac{\partial i_v(x,t)}{\partial t} + [l_g + m_{uw} - m_{wg} - m_{ug}]\, \frac{\partial i_u(x,t)}{\partial t} \end{aligned} \tag{6.25}$$

where the equations are derived by using this:

$$i_u(x,t) + i_v(x,t) + i_w(x,t) + i_g(x,t) = 0. \tag{6.26}$$

Eq. (6.23), (6.24) and (6.25) can be collected by obtaining:

$$-\frac{\partial v_{uvw}}{\partial x} = (R_{uvw} + R_g) \cdot i_{uvw}(x,t) + (M_{uvw} + M_{uvwg}) \cdot \frac{\partial i_{uvw}(x,t)}{\partial t} \tag{6.27}$$

where the electrical variables are represented by:

$$v_{uvw}(x,t) = \begin{bmatrix} v_{ug}(x,t) \\ v_{vg}(x,t) \\ v_{wg}(x,t) \end{bmatrix} \quad ; \quad i_{uvw}(x,t) = \begin{bmatrix} i_u(x,t) \\ i_v(x,t) \\ i_w(x,t) \end{bmatrix} \tag{6.28}$$

$$\frac{\partial i_{uvw}(x,t)}{\partial x} = \begin{bmatrix} \partial i_u(x,t)/\partial x \\ \partial i_v(x,t)/\partial x \\ \partial i_w(x,t)/\partial x \end{bmatrix} \quad ; \quad \frac{\partial i_{uvw}(x,t)}{\partial t} = \begin{bmatrix} \partial i_u(x,t)/\partial t \\ \partial i_v(x,t)/\partial t \\ \partial i_w(x,t)/\partial t \end{bmatrix} \tag{6.29}$$

$$\frac{\partial v_{uvw}(x,t)}{\partial x} = \begin{bmatrix} \partial v_{ug}(x,t)/\partial x \\ \partial v_{vg}(x,t)/\partial x \\ \partial v_{wg}(x,t)/\partial x \end{bmatrix} \quad ; \quad \frac{\partial v_{uvw}(x,t)}{\partial t} = \begin{bmatrix} \partial v_{ug}(x,t)/\partial t \\ \partial v_{vg}(x,t)/\partial t \\ \partial v_{wg}(x,t)/\partial t \end{bmatrix} \tag{6.30}$$

and where the matrices are represented by:

$$R_{uvw} = \begin{bmatrix} r_u & 0 & 0 \\ 0 & r_v & 0 \\ 0 & 0 & r_w \end{bmatrix} \quad R_g = r_g \begin{bmatrix} 1 & 1 & 1 \\ 1 & 1 & 1 \\ 1 & 1 & 1 \end{bmatrix} \tag{6.31}$$

$$M_{uvw} = \begin{bmatrix} [l_u] & [m_{uv}] & [m_{uw}] \\ [m_{uv}] & [l_v] & [m_{vw}] \\ [m_{uw}] & [m_{vw}] & [l_w] \end{bmatrix} \tag{6.32}$$

$$M_{uvwg} = \begin{bmatrix} [l_g - 2m_{ug}] & [l_g - m_{ug} - m_{vg}] & [l_g - m_{ug} - m_{wg}] \\ [l_g - m_{ug} - m_{vg}] & [l_g - 2m_{vg}] & [l_g - m_{vg} - m_{wg}] \\ [l_g - m_{wg} - m_{ug}] & [l_g - m_{wg} - m_{vg}] & [l_g - 2m_{wg}] \end{bmatrix} \tag{6.33}$$

By writing Kirchhoff's current law for the circuit shown in Fig. 6.12, the sequent partial differential equations are obtained:

$$\begin{aligned} -\frac{\partial i_u(x,t)}{\partial x} = {} & [g_{uv} + g_{uw} + g_{ug}]\, v_{ug}(x,t) - [g_{uv}]\, v_{vg}(x,t) - [g_{uw}]\, v_{wg}(x,t) \\ & + [c_{uv} + c_{uw} + c_{ug}] \frac{\partial v_{ug}(x,t)}{\partial t} \\ & - [c_{uv}] \frac{\partial v_{vg}(x,t)}{\partial t} - [c_{uw}] \frac{\partial v_{wg}(x,t)}{\partial t} \end{aligned} \tag{6.34}$$

$$\begin{aligned} -\frac{\partial i_v(x,t)}{\partial x} = {} & -[g_{uv}]\, v_{ug}(x,t) + [g_{uv} + g_{vw} + g_{vg}]\, v_{vg}(x,t) - [g_{vw}]\, v_{wg}(x,t) \\ & - [c_{uv}] \frac{\partial v_{ug}(x,t)}{\partial t} \\ & + [c_{uv} + c_{vw} + c_{vg}] \frac{\partial v_{vg}(x,t)}{\partial t} - [c_{vw}] \frac{\partial v_{wg}(x,t)}{\partial t} \end{aligned} \tag{6.35}$$

$$-\frac{\partial i_w(x,t)}{\partial x} = -\left[g_{uw}\right] v_{ug}(x,t) - \left[g_{vw}\right] v_{vg}(x,t) + \left[g_{uw}+g_{vw}+g_{wg}\right] v_{wg}(x,t) - \left[c_{uw}\right]\frac{\partial v_{ug}(x,t)}{\partial t} - \left[c_{vw}\right]\frac{\partial v_{vg}(x,t)}{\partial t} + \left[c_{vw}+c_{uw}+c_{wg}\right]\frac{\partial v_{wg}(x,t)}{\partial t}. \quad (6.36)$$

Eq. (6.34), (6.35) and (6.36) can be grouped as shown in:

$$-\frac{\partial i_{uvw}(x,t)}{\partial x} = (G_{uvw})\cdot v_{uvw}(x,t) + (C_{uvwg})\cdot\frac{\partial v_{uvw}(x,t)}{\partial t} \quad (6.37)$$

where the C_{uvwg} and G_{uvw} matrices are described by:

$$G_{uvw} = \begin{bmatrix} [g_{uv}+g_{uw}+g_{ug}] & [-g_{uv}] & [-g_{uw}] \\ [-g_{uv}] & [g_{uv}+g_{vw}+g_{vg}] & [-g_{vw}] \\ [-g_{uw}] & [-g_{vw}] & [g_{uw}+g_{vw}+g_{wg}] \end{bmatrix} \quad (6.38)$$

$$C_{uvwg} = \begin{bmatrix} [c_{uv}+c_{uw}+c_{ug}] & [-c_{uv}] & [-c_{uw}] \\ [-c_{uv}] & [c_{uv}+c_{vw}+c_{vg}] & [-c_{vw}] \\ [-c_{uw}] & [-c_{vw}] & [c_{vw}+c_{uw}+c_{wg}]. \end{bmatrix} \quad (6.39)$$

In conclusion, the voltages and the currents of the transmission lines are express by:

$$\begin{cases} -\dfrac{\partial v_{uvw}}{\partial x} = (R_{uvw}+R_g)\cdot i_{uvw}(x,t) + (M_{uvw}+M_{uvwg})\cdot\dfrac{\partial i_{uvw}(x,t)}{\partial t} \\ -\dfrac{\partial i_{uvw}(x,t)}{\partial x} = (G_{uvw})\cdot v_{uvw}(x,t) + (C_{uvwg})\cdot\dfrac{\partial v_{uvw}(x,t)}{\partial t} \end{cases} \quad (6.40)$$

The solution of this system of equations is very complicated and their treatments is not easy. Transmission line composed of four conductors can be decouple in three-decoupled-transmission-line [62, 89, 102, 103]. Coordinate transformation can be used, such as the Clarke transformation that maintain invariant the power. The matrix used for the coordinate transformations is:

$$x_{\alpha\beta 0} = T_{\alpha\beta 0}\cdot x_{uvw} = \sqrt{\frac{2}{3}}\cdot\begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \\ \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \end{bmatrix}\cdot x_{uvw}. \quad (6.41)$$

By applying the Clarke transformation to the equations defined (6.40) it is possible to do the decoupling process:

$$\begin{aligned} -\frac{\partial v_{\alpha\beta0}(x,t)}{\partial x} &= T_{\alpha\beta0}(R_{uvw}+R_g)T_{\alpha\beta0}^{-1}\cdot i_{\alpha\beta0}(x,t) \\ &+T_{\alpha\beta0}\cdot(M_{uvw}+M_{uvwg})\cdot T_{\alpha\beta0}^{-1}\cdot\frac{\partial i_{\alpha\beta0}(x,t)}{\partial t} \end{aligned} \tag{6.42}$$

$$-\frac{\partial i_{\alpha\beta0}(x,t)}{\partial x} = [T_{\alpha\beta0}G_{uvw}T_{\alpha\beta0}^{-1}]\cdot v_{\alpha\beta0}(x,t)+[T_{\alpha\beta0}C_{uvwg}T_{\alpha\beta0}^{-1}]\cdot\frac{\partial v_{\alpha\beta0}(x,t)}{\partial t} \tag{6.43}$$

where, the two new partial differential equations can be represented by:

$$-\frac{\partial v_{\alpha\beta0}(x,t)}{\partial x} = R_{\alpha\beta0}\cdot i_{\alpha\beta0}(x,t)+M_{\alpha\beta0}\cdot\frac{\partial i_{\alpha\beta0}(x,t)}{\partial t} \tag{6.44}$$

$$-\frac{\partial i_{\alpha\beta0}(x,t)}{\partial x} = G_{\alpha\beta0}\cdot v_{\alpha\beta0}(x,t)+C_{\alpha\beta0}\cdot\frac{\partial v_{\alpha\beta0}(x,t)}{\partial t}. \tag{6.45}$$

By imposing the hypothesis of having a symmetrical cable, the problem can be simplified. The per meter parameters of the cable needs to be force as follows:

$$c_{pg} = c_{ug} = c_{vg} = c_{wg} \tag{6.46}$$

$$m_{pg} = m_{ug} = m_{vg} = m_{wg} \tag{6.47}$$

$$m_{pp} = m_{uv} = m_{vw} = m_{vw} \tag{6.48}$$

$$l_p = l_u = l_v = l_w \tag{6.49}$$

$$r_p = r_u = r_v = r_w \tag{6.50}$$

$$g_{pp} = g_{uv} = g_{vw} = g_{vw} \tag{6.51}$$

where, "pg" subscript is related to the phase-to-ground parameters, while "pp" is related to the line-to-line parameters. The matrices presented previously are modified by obtaining:

$$R_{uvw} = \begin{bmatrix} r_p & 0 & 0 \\ 0 & r_p & 0 \\ 0 & 0 & r_p \end{bmatrix} \quad R_g = r_g \begin{bmatrix} 1 & 1 & 1 \\ 1 & 1 & 1 \\ 1 & 1 & 1 \end{bmatrix} \tag{6.52}$$

$$M_{uvw} = \begin{bmatrix} [l_p] & [m_{pp}] & [m_{pp}] \\ [m_{pp}] & [l_p] & [m_{pp}] \\ [m_{pp}] & [m_{pp}] & [l_p] \end{bmatrix} \tag{6.53}$$

$$M_{uvwg} = \begin{bmatrix} [l_p - 2m_{pp}] & [l_p - 2m_{pp}] & [l_p - 2m_{pp}] \\ [l_p - 2m_{pp}] & [l_p - 2m_{pp}] & [l_p - 2m_{pp}] \\ [l_p - 2m_{pp}] & [l_p - 2m_{pp}] & [l_p - 2m_{pp}] \end{bmatrix} \tag{6.54}$$

$$G_{uvw} = \begin{bmatrix} [2g_{pp} + g_{pg}] & [-g_{pp}] & [-g_{pp}] \\ [-g_{pp}] & [2g_{pp} + g_{pg}] & [-g_{pp}] \\ [-g_{pp}] & [-g_{pp}] & [2g_{pp} + g_{pg}] \end{bmatrix} \tag{6.55}$$

$$C_{uvwg} = \begin{bmatrix} [2c_{pp} + c_{pg}] & [-c_{pp}] & [-c_{pp}] \\ [-c_{pp}] & [2c_{pp} + c_{pg}] & [-c_{pp}] \\ [-c_{pp}] & [-c_{pp}] & [2c_{pp} + c_{pg}] \, . \end{bmatrix} \tag{6.56}$$

The elements of the matrices defined in (6.44) and (6.45), which are results that comes from the coordinate transformation, are represented by:

$$R_{\alpha\beta 0} = T_{\alpha\beta 0}(R_{uvw} + R_g)T^{-1}_{\alpha\beta 0} = R_{uvw} + \begin{bmatrix} 0 & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & 3r_g \end{bmatrix} = \begin{bmatrix} r_p & 0 & 0 \\ 0 & r_p & 0 \\ 0 & 0 & r_p + 3r_g \end{bmatrix} \tag{6.57}$$

$$L_{\alpha\beta 0} = T^{-1}_{\alpha\beta 0}(M_{uvw} + M_{uvwg})T_{\alpha\beta 0} = \\ = \begin{bmatrix} l_p - m_{pp} & 0 & 0 \\ 0 & l_p - m_{pp} & 0 \\ 0 & 0 & 3(l_g - 2m_{pg}) + l_p + 2m_{pp} \end{bmatrix} \tag{6.58}$$

$$C_{\alpha\beta 0} = T_{\alpha\beta 0}C_{uvwg}T^{-1}_{\alpha\beta 0} = \begin{bmatrix} c_{pg} + 3c_{pp} & 0 & 0 \\ 0 & c_{pg} + 3c_{pp} & 0 \\ 0 & 0 & c_{pg} \end{bmatrix} \tag{6.59}$$

$$G_{\alpha\beta 0} = T_{\alpha\beta 0}G_{uvw}T^{-1}_{\alpha\beta 0} = \begin{bmatrix} g_{pg} + 3g_{pp} & 0 & 0 \\ 0 & g_{pg} + 3g_{pp} & 0 \\ 0 & 0 & g_{pg} \end{bmatrix} \tag{6.60}$$

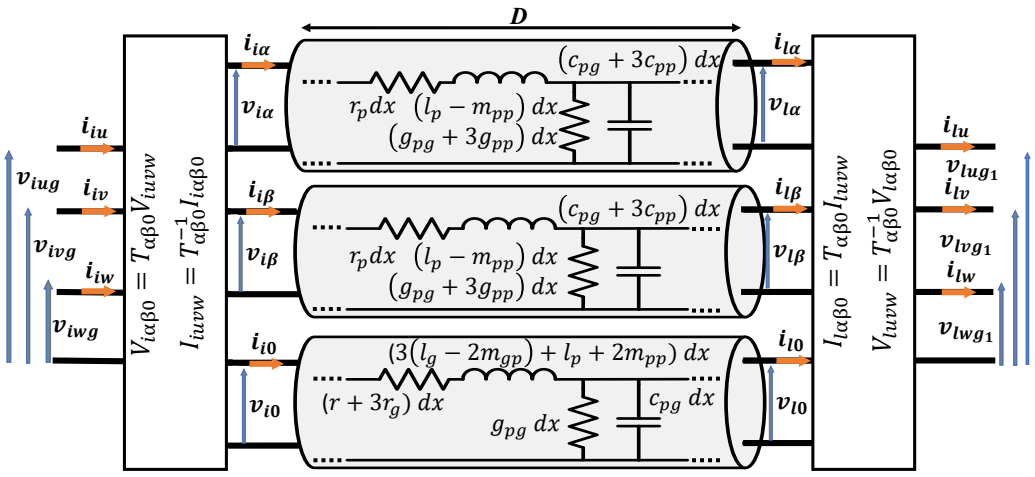


Figure 6.13: Three decoupled transmission lines that represent a simplify three-phase power cable with their equivalent parameters. "p" phase parameter, "pp" phase to phase parameter, "pg" phase to ground parameter.

It can be noticed from (6.57),(6.58),(6.59) and (6.60) that these matrices are diagonal matrix. This feature involves that the three components are decoupled by each other. For example, what happens in the sequent α is not seen by the 0 component. By virtue of this assumption, an equivalent model of the three-phase transmission line can be derived. The equivalent model is depicted in Fig. 6.13.

As can be noticed from this figure, three independent transmission lines are defined. Therefore, three propagation speeds and three characteristic impedances, for each component, can be defined.

By applying the procedure used in Chapter 6.2.1, r_p, r_g, g_{pp} and g_{pg} are imposed equal to zero (as done previously) and the cable parameters can be calculated as follows:

$$Z_\alpha = \sqrt{\frac{l_\alpha}{c_\alpha}} = \sqrt{\frac{l_p - m_{pp}}{c_{pg} + 3c_{pp}}} \tag{6.61}$$

$$Z_\beta = \sqrt{\frac{l_\beta}{c_\beta}} = \sqrt{\frac{l_p - m_{pp}}{c_{pg} + 3c_{pp}}} \tag{6.62}$$

$$Z_0 = \sqrt{\frac{l_0}{c_0}} = \sqrt{\frac{3(l_g - 2m_{pg}) + l_p + 2m_{pp}}{c_{pg}}} \tag{6.63}$$

$$U_\alpha = \frac{1}{\sqrt{l_\alpha c_\alpha}} = \frac{1}{\sqrt{(l_p - m_{pp})(c_{pg} + 3c_{pp})}} \tag{6.64}$$

$$U_\beta = \frac{1}{\sqrt{l_\beta c_\beta}} = \frac{1}{\sqrt{(l_p - m_{pp})(c_{pg} + 3c_{pp})}} \tag{6.65}$$

$$U_0 = \frac{1}{\sqrt{l_0 c_0}} = \frac{1}{\sqrt{(3(l_g - 2m_{pg}) + l_p + 2m_{pp})(c_{pg})}}. \tag{6.66}$$

From this mathematical model, the sequent important proprieties can be derived:

- Z_α and Z_β present the same numeric value. The characteristic impedance is proportional to the characteristic impedance of the differential mode derived by previous authors [104].
- U_α and U_β, which are the velocity of propagations of the α and β components, are equal. This propagation speed is identical to the differential mode propagation speed defined by different authors [104]. In fact, these velocities are independent of the used coordinate transformation.
- Z_α and Z_0 do not present the same numeric value. It means that the differential mode and the common mode could not present the same behavior.
- U_α and U_0 do not present the same numeric value. It means that the differential mode and the common mode waveforms could travel at different speeds.

6.4.2 Boundary condition

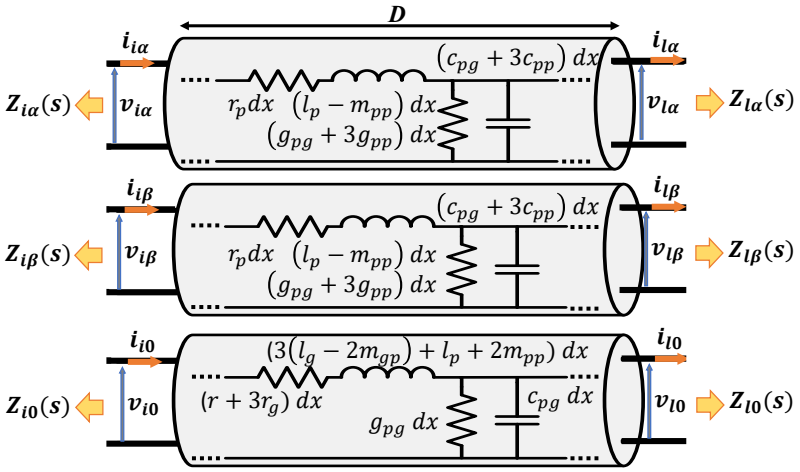


Figure 6.14: Four-conductor transmission lines: schematic details about the impedances seen at the input and output cable terminations for each component obtained by means of the Clarke transformation.

As described in Chapter 6.2.2, the power cable needs to be connected to the load and to the generator. The reflection coefficients seen at the input and the output

terminals are important because the motor overvoltage solution can be found. It can be observed from Fig. 6.14, six reflection coefficients can be defined: three for the input ($\Gamma_{i\alpha}$, $\Gamma_{i\beta}$ and Γ_{i0}) and three for the output ($\Gamma_{l\alpha}$, $\Gamma_{l\beta}$ and Γ_{l0}). The reflection coefficients are defined below:

$$\Gamma_{i\alpha} = \frac{Z_{i\alpha(s)} - Z_\alpha}{Z_{i\alpha(s)} + Z_\alpha} \;;\; \Gamma_{i\beta} = \frac{Z_{i\beta(s)} - Z_\beta}{Z_{i\beta(s)} + Z_\beta} \;;\; \Gamma_{i0} = \frac{Z_{i0(s)} - Z_0}{Z_{i0(s)} + Z_0} \tag{6.67}$$

$$\Gamma_{l\alpha} = \frac{Z_{l\alpha(s)} - Z_\alpha}{Z_{l\alpha(s)} + Z_\alpha} \;;\; \Gamma_{l\beta} = \frac{Z_{l\beta(s)} - Z_\beta}{Z_{l\beta(s)} + Z_\beta} \;;\; \Gamma_{l0} = \frac{Z_{l0(s)} - Z_0}{Z_{l0(s)} + Z_0} \tag{6.68}$$

where, the "i" subscript identifies the equivalent Thevenin impedance, correspondent to the component α, β and 0, seen at the cable terminals input, while the "l" subscript identifies the equivalent Thevenin impedance seen at the cable terminals output.

6.5 Electric drive model

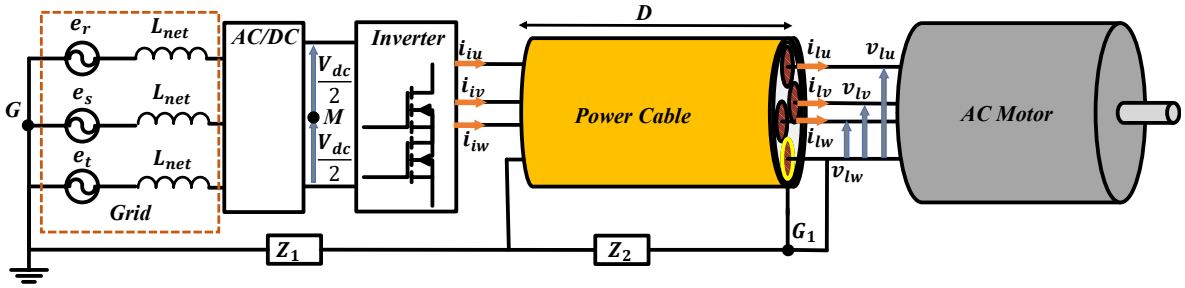


Figure 6.15: Industrial three-phase electric drive representation with: power grid, rectifier, inverter, cable and motor.

It has been observed from Chapter 6.4.1 than the transmission lines needs to be studied by means of three independent transmission lines (i.e. by means of the α, β and 0 components). A typical electric drive is represented in Fig. 6.15. The converter is usually composed of:

- AC/DC converter, which can be a total three-phase rectifier or an inverter connected to the grid;
- a three-phase inverter which can be composed of power modules based on different technologies, such as all-Si, Si-SiC, and all-SiC devices;
- a three-phase power cable which can be available in different solutions (e.g. with shield and ground cable, without shield, etc. etc.) [98].

- a three-phase electric motor.

A detailed analysis of the equivalent model of each element is required. In particularly, special attention is required by the differential (α, β) and common mode (0) components. Thence, a detailed study of each drive component is required.

6.5.1 AC/DC converter

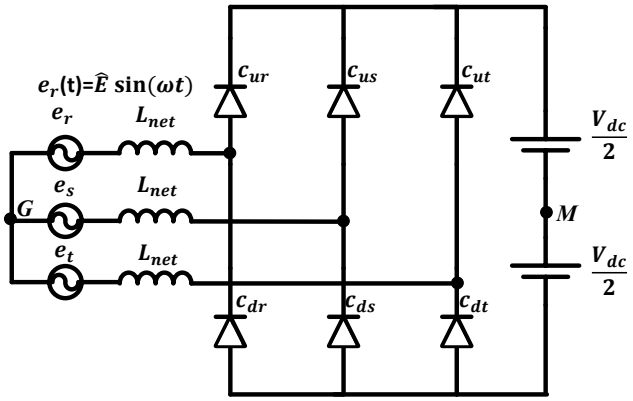


Figure 6.16: Three-phase diode bridge rectifier.

Two important rectifier topologies are used in the industrial field: three-phase diode bridge rectifier and three-phase boost rectifier.

The three-phase bridge rectifier is a simple and robust converter because it does not require special control techniques. Anyway, different disadvantages can be found when this structure is used:

- line currents present a high total harmonic distortion;
- the power flow is unidirectional.

The scheme of the three-phase diode bridge rectifier is shown in Fig. 6.16. The rectifier voltage, which corresponds to the bus voltage (V_{dc}), can be calculated by using:

$$V_{dc} = \frac{3\sqrt{3}}{\pi}\hat{E} \tag{6.69}$$

where, $\hat{E}$ is the peak voltage of phase to ground voltage. The rectifier voltage is important in the differential mode circuit. The common mode voltage introduced by the electronic structure could become important in the motor overvoltage phenomenon [55]. The equivalent model is composed of an equivalent voltage generator and an equivalent impedance as shown in Fig. 6.17. Anyway, the common mode introduced by this converter is not important with respect to the issues caused by

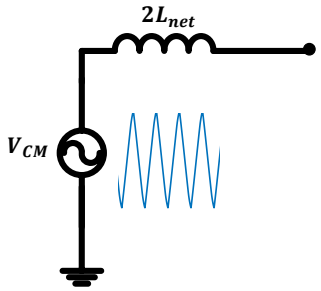


Figure 6.17: Common mode equivalent circuit of a three-phase diode bridge rectifier.

the PWM modulation. In fact, the common mode variation is very slow. As a consequence, this variation, most of the time, is not dangerous for the motor insulation winding.

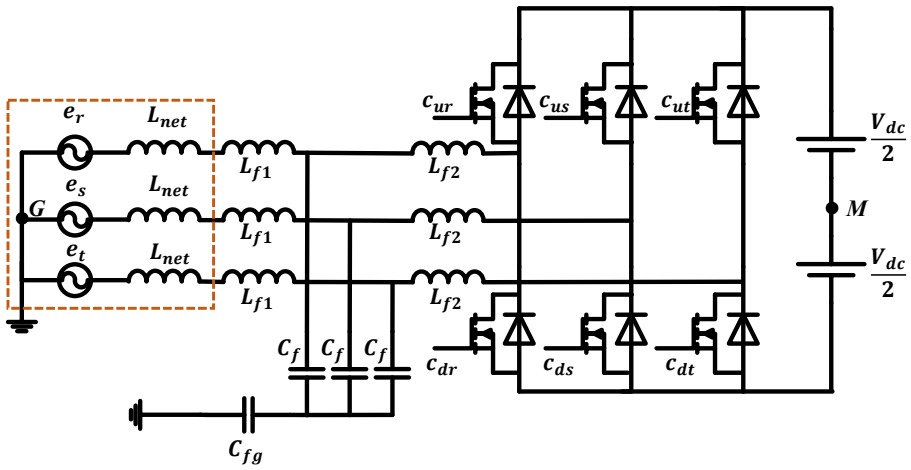


Figure 6.18: Three-phase boost rectifier.

The three-phase boost rectifier is a converter capable of introducing a series of significant benefits that are listed below:

- lower total harmonic distortion factor with respect to the passive rectifier;
- filter connected to the power grid can be reduced in dimension, especially if the switching frequency is increased;
- the bus voltage can be increased instead of the standard limit reached by the passive rectifier (6.69);
- this structure permits to have regenerative braking.

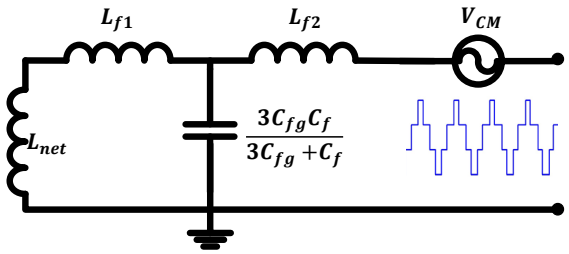


Figure 6.19: Common mode equivalent circuit of a three-phase boost rectifier.

The equivalent common mode circuit of an active rectifier with LCL filter is shown Fig. 6.18. The common mode introduced by an active rectifier becomes important in the motor overvoltage study [53]. In fact, the common mode can be introduced to the motor side causing additional overvoltages.

6.5.2 Three-phase inverter

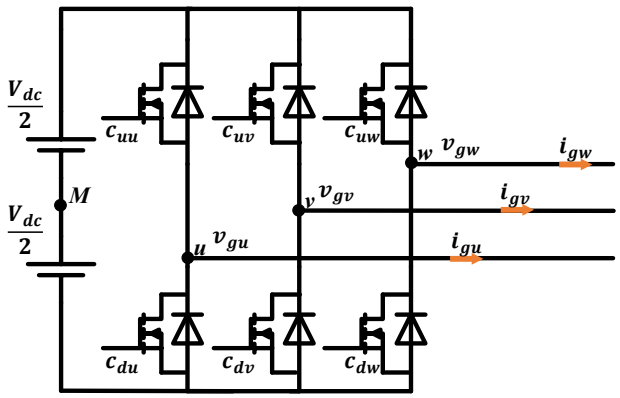


Figure 6.20: Three-phase inverter

An equivalent scheme of a three-phase inverter is shown in Fig. 6.20. In this figure, parasitic elements, as bus bar parasitic inductance, have been neglected in order to simplify the problem. By referring the voltage with respect to the middle point of the DC bus (indicated with M in Fig. 6.20), the inverter output voltages can be calculated by using:

$$v_{gu} = m_u \frac{V_{dc}}{2} \tag{6.70}$$

$$v_{gv} = m_v \frac{V_{dc}}{2} \tag{6.71}$$

$$v_{gw} = m_w \frac{V_{dc}}{2} \tag{6.72}$$

where, m can be −1 or 1. Eq. (6.70),(6.71), (6.72) are simplified formulae because the voltage drop of the switch or diode is not considered. By applying the Clarke transformation to (6.70), (6.71) and (6.72), the α, β and 0 components can be derived:

$$v_{g\alpha}(m_u, m_v, m_w) = \sqrt{\frac{2}{3}}\left(m_u - 0.5m_v - 0.5m_w\right)\frac{V_{dc}}{2} \tag{6.73}$$

$$v_{g\beta}(m_u, m_v, m_w) = \sqrt{\frac{1}{2}}\left(m_v - m_w\right)\frac{V_{dc}}{2} \tag{6.74}$$

$$v_{g0}(m_u, m_v, m_w) = \sqrt{\frac{1}{3}}\left(m_u + m_v + m_w\right)\frac{V_{dc}}{2}. \tag{6.75}$$

Using these equations for each inverter state, the correspondent $v_{g\alpha}$, $v_{g\beta}$ and v_{g0} can be evaluated. The dv/dt of these variables depends on the used device technology. Typical voltage rise time for all-Si devices spans 100 to 500 ns [26, 62, 77, 81], whereas, for all-SiC, the rise time spans 10 to 100 ns [18, 26].

The Clarke transformation can be applied to the currents of the inverter:

$$i_{g\alpha} = \sqrt{\frac{2}{3}}\left(i_{gu} - 0.5i_{gv} - 0.5i_{gw}\right) \tag{6.76}$$

$$i_{g\beta} = \sqrt{\frac{1}{2}}\left(i_{gv} - i_{gw}\right) \tag{6.77}$$

$$i_{g0} = \sqrt{\frac{1}{3}}\left(i_{gu} + i_{gv} + i_{gw}\right). \tag{6.78}$$

6.5.3 Power cable

As derived previously, the velocities of propagation presented α, β and 0 can be different, but using a symmetrical cable, differential cable parameters are equal:

$$t_\alpha = t_\beta \tag{6.79}$$

$$Z_\alpha = Z_\beta \tag{6.80}$$

$$U_\alpha = U_\beta. \tag{6.81}$$

Cable surge impedances span 20 to 120 Ω [80], while typical cables propagation speeds can be around half the speed of the light.

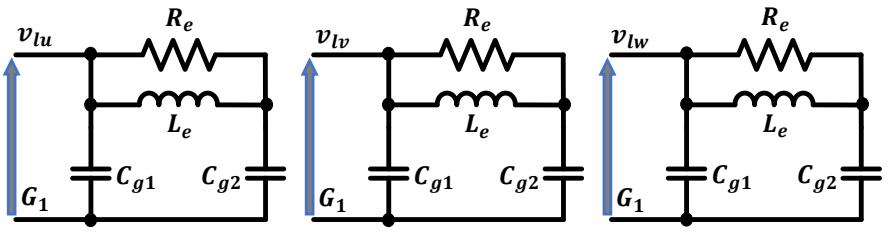


Figure 6.21: Three-phase motor equivalent circuit: high frequency lumped parameter for AC motors.

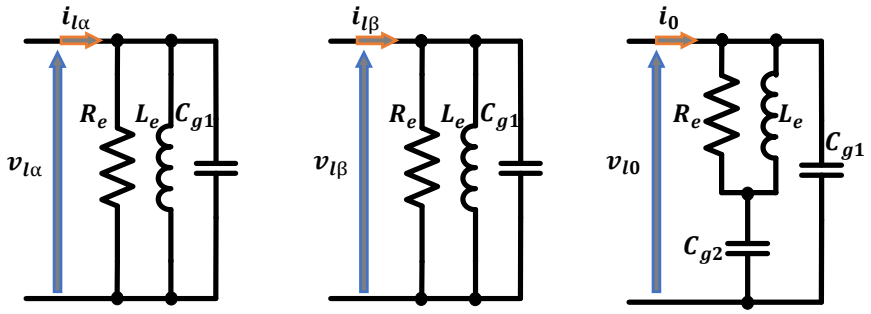


Figure 6.22: Equivalent α, β and 0 circuits of the high frequency motor lumped parameter circuit shown in Fig. 6.21.

6.5.4 Three-phase AC motor

Precise equivalent motor circuits composed of many elements, as shown in Fig. 6.21, have been proposed in previous works [62, 67, 78, 79, 105, 106, 107, 108]. The equivalent circuit represented in α, β and 0 components of Fig. 6.21 is shown in Fig. 6.22. The equivalent circuits can be a very good solution to be used in the simulation, but if the formulation is required the problem becomes more complicated. For this reason in other works, the motor is considered to have a fixed impedance [26, 63, 64, 66, 68, 82]. An example of an equivalent model of the motor can be represented by Fig. 6.23. The motor equivalent impedance value depends on the power rating. Typical values span 500 Ω to 4000 Ω [80]. The voltages at the Z_{lj} terminals permit to study the motor overvoltages. The voltages at the motor terminals in function of the α, β and 0 components are described in:

$$(v_{lu} - v_{G1}) = \sqrt{\frac{2}{3}}\left(v_{l\alpha} + \frac{1}{\sqrt{2}}v_{l0}\right) \tag{6.82}$$

$$(v_{lv} - v_{G1}) = \sqrt{\frac{2}{3}}\left(-0.5v_{l\alpha} + \frac{\sqrt{3}}{2}v_{l\beta} + \frac{1}{\sqrt{2}}v_{l0}\right) \tag{6.83}$$

$$(v_{lw} - v_{G1}) = \sqrt{\frac{2}{3}}\left(-0.5v_{l\alpha} - \frac{\sqrt{3}}{2}v_{l\beta} + \frac{1}{\sqrt{2}}v_{l0}\right) \tag{6.84}$$

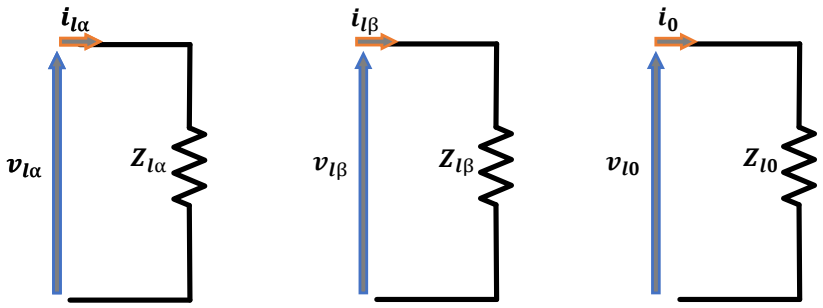


Figure 6.23: Simplified motor equivalent circuits of the α, β and 0 components.

where, G_1 is connected to the motor earth. The phase-to-phase motor voltages are defined by:

$$(v_{lu} - v_{lv}) = \sqrt{\frac{2}{3}}\left(1.5v_{l\alpha} - \frac{\sqrt{3}}{2}v_{l\beta}\right) \tag{6.85}$$

$$(v_{lu} - v_{lw}) = \sqrt{\frac{2}{3}}\left(1.5v_{l\alpha} + \frac{\sqrt{3}}{2}v_{l\beta}\right) \tag{6.86}$$

$$(v_{lv} - v_{lw}) = \sqrt{\frac{2}{3}}\left(\sqrt{3}v_{l\beta}\right). \tag{6.87}$$

As can be noticed from these equations, phase-to-phase and phase-to-ground motor voltages have been defined. The observations done about these equations are listed below.

- The phase-to-phase motor voltage is independent of the common mode sequence. In accordance with the previous work, the line-to-line motor overvoltage depends on the α and β components.
- The phase-to-ground motor voltage depends on all the components.

6.6 Motor overvoltage

By observing the equivalent impedance values presented by the cable and the motor (see Chapter 6.5.3 and Chapter 6.5.4), the reflection factors at the load side, for each component, are almost near to one. As explained in Chapter 6.3 when the load reflection coefficient is near to one, overvoltage at the load side is present for each sequence. Thence, overvoltages at the motor side (phase-to-phase and phase-to-frame) can be obtained from α, β and 0 overvoltages using the inverse Clarke transformation.

In most of the previous works, the phase-to-phase motor overvoltage was always studied without considering the phase-to-ground motor overvoltage. In this section,

by virtue of having a precise model, which considers the common mode sequence, both the overvoltages have been studied.

6.6.1 Formulation hypotheses and equivalent drive model

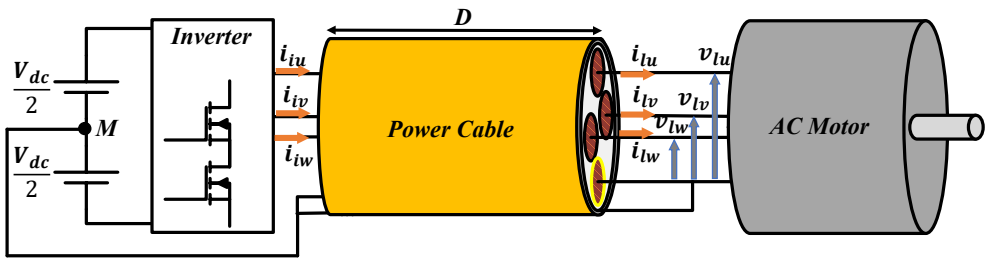


Figure 6.24: Schematic representation of a drive, which presents the ground reference connected to the middle point of the DC bus.

The novel analysis of the motor overvoltage is conducted by applying the sequent hypothesis.

- The three-phase transmission line is symmetric, thence the characteristic impedances and the propagation speeds of the differential components (α and β) are equal.
- A lossless power cable has been considered. This hypothesis allows the search for the worst case scenario.
- The ground of the power cable is connected to the middle point of the DC bus (Fig. 6.24). In this way, the common mode voltage and impedance introduced by the AC/DC stage have been removed [109]. This connection method is common in aircraft applications [110].
- No other current paths are presented by the common mode currents. The motor is connected to the ground only by means of the power cable.
- In order to simplify the analysis, the load has been considered as resistive load with fixed reflection coefficients Γ_l.

The equivalent model of the drive depicted in Fig. 6.24, which considers the α, β and 0 components, it is shown in Fig. 6.25. In this figure, the inverter has been represented by six voltage generators:

- $V_{i\alpha}$, $V_{i\beta}$ and V_{i0} represent the voltage status presented by the inverter before the switching. These voltages can be obtained by applying the Clarke transformation to the inverter voltage as done in (6.73), (6.74) and (6.75);

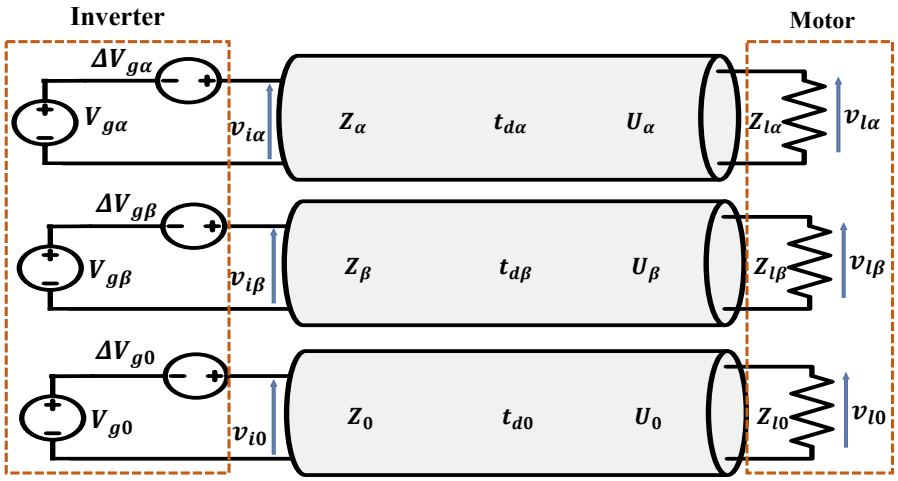


Figure 6.25: Equivalent model of the drive used for study the motor overvoltages.

- $\Delta V_{i\alpha}$, $\Delta V_{i\beta}$ and ΔV_{i0} are step voltage generators, which imposed their status when $t = 0s$. Using these generators, it is possible to force the inverter voltages after the switching event.

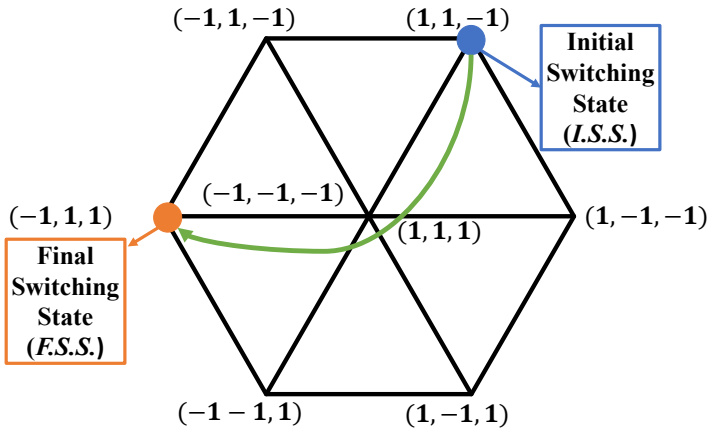


Figure 6.26: Schematic representation of the initial and final inverter switching states.

Multiple switching patterns can be followed by three-phase inverter. Totally, 56 switching patterns can be executed, thence all these switching paths need to be analyzed in the motor overvoltage phenomena. Each time that the switching status is changed, diverse voltages are applied to each transmission line. As a consequence, a detailed study of the voltages applied by the inverter to the cable is required.

It is common to represent the voltages imposed by the inverter by means of a hexagon, as depicted in Fig. 6.26. The sequent convention has been attributed to the switching path presented by the inverter:

- the inverter switching state before the transition is called: Initial Switch State (I.S.S.) (i.e. indicated in blue);
- the inverter switching state after the transition is called: Final Switch State (F.S.S.) (i.e. indicated in orange).

6.6.2 Mathematical formulae

The voltages imposed by the generators, as a function of the time, that are depicted in Fig. 6.25, are described by the sequent equations:

$$\Delta V_{g\alpha} = (V_{g\alpha}(F.S.S.) - V_{g\alpha}(I.S.S.)) \tag{6.88}$$

$$\Delta V_{g\beta} = (V_{g\beta}(F.S.S.) - V_{g\beta}(I.S.S.)) \tag{6.89}$$

$$\Delta V_{g0} = (V_{g0}(F.S.S.) - V_{g0}(I.S.S.)) \tag{6.90}$$

$$V_{g\alpha} = V_{g\alpha}(I.S.S.) \tag{6.91}$$

$$V_{g\beta} = V_{g\beta}(I.S.S.) \tag{6.92}$$

$$V_{g0} = V_{g0}(I.S.S.) \tag{6.93}$$

where, I.S.S. represents the initial switching state of the inverter, while F.S.S. represents the final switching state of the inverter.

The voltages imposed by the generators to the input terminals of each cable are described by:

$$v_{i\alpha}(t = 0^-) = V_{g\alpha}(I.S.S.) \tag{6.94}$$

$$v_{i\beta}(t = 0^-) = V_{g\beta}(I.S.S.) \tag{6.95}$$

$$v_{i0}(t = 0^-) = V_{g0}(I.S.S.) \tag{6.96}$$

$$v_{i\alpha}(t) = V_{g\alpha}(I.S.S.) + \Delta V_{g\alpha} u(t) = V_{g\alpha}(F.S.S.)\ ;\ t > 0 \tag{6.97}$$

$$v_{i\beta}(t) = V_{g\beta}(I.S.S.) + \Delta V_{g\beta} u(t) = V_{g\beta}(F.S.S.)\ ;\ t > 0 \tag{6.98}$$

$$v_{i0}(t) = V_{g0}(I.S.S.) + \Delta V_{g0} u(t) = V_{g0}(F.S.S.)\ ;\ t > 0. \tag{6.99}$$

At the load side the voltages of the load are represented by:

$$v_{l\alpha}(t) = V_{g\alpha}(I.S.S.) \quad ; \quad 0 \leq t < t_{d\alpha} \tag{6.100}$$

$$v_{l\beta}(t) = V_{g\beta}(I.S.S.) \quad ; \quad 0 \leq t < t_{d\beta} \tag{6.101}$$

$$v_{l0}(t) = V_{g0}(I.S.S.) \quad ; \quad 0 \leq t < t_{d0} \tag{6.102}$$

where, $t_{d\alpha}$, $t_{d\beta}$ and t_{d0} represent the propagation delays presented by each component (i.e. α, β and 0). In fact, the voltages at the load side are equal to the one of the initial state because the waveform from the input have not arrived. The load

voltages of each transmission line, after that the input voltages arrives at the load side, are defined by:

$$\begin{aligned} v_{l\alpha}(t) &= V_{g\alpha}(I.S.S.) + (1+\Gamma_{l\alpha})(V_{g\alpha}(F.S.S.) - V_{g\alpha}(I.S.S.)) = \\ &= V_{g\alpha}(F.S.S.) + (\Gamma_{l\alpha})(V_{g\alpha}(F.S.S.) - V_{g\alpha}(I.S.S.)) \ ; \ t_{d\alpha} < t < 3t_{d\alpha} \end{aligned} \tag{6.103}$$

$$\begin{aligned} v_{l\beta}(t) &= V_{g\beta}(I.S.S.) + (1+\Gamma_{l\beta})(V_{g\beta}(F.S.S.) - V_{g\beta}(I.S.S.)) = \\ &= V_{g\beta}(F.S.S.) + (\Gamma_{l\beta})(V_{g\beta}(F.S.S.) - V_{g\alpha}(I.S.S.)) \ ; \ t_{d\beta} < t < 3t_{d\beta} \end{aligned} \tag{6.104}$$

$$\begin{aligned} v_{l0}(t) &= V_{g0}(I.S.S.) + (1+\Gamma_{l0})(V_{g0}(F.S.S.) - V_{g0}(I.S.S.)) = \\ &= V_{g0}(F.S.S.) + (\Gamma_{l0})(V_{g0}(F.S.S.) - V_{g0}(I.S.S.)) \ ; \ t_{d0} < t < 3t_{d0} \end{aligned} \tag{6.105}$$

where, $\Gamma_{l\alpha}$, $\Gamma_{l\beta}$ and Γ_{l0} represents the load reflection coefficients.

By taking the load voltages defined in (6.100), (6.101), (6.102), (6.103), (6.104) and (6.105), the respective discontinuous functions can be defined as in:

$$\begin{cases} v_{l\alpha}(t) = V_{g\alpha}(I.S.S.) \ \ ; \ \ 0 \leq t < t_{d\alpha} \\ v_{l\alpha}(t) = V_{g\alpha}(F.S.S.) + \Gamma_{l\alpha}(V_{g\alpha}(F.S.S.) - V_{g\alpha}(I.S.S.)) \ ; \ t_{d\alpha} \leq t < 3t_{d\alpha} \end{cases} \tag{6.106}$$

$$\begin{cases} v_{l\beta}(t) = V_{g\beta}(I.S.S.) \ \ ; \ \ 0 \leq t < t_{d\beta} \\ v_{l\beta}(t) = V_{g\beta}(F.S.S.) + \Gamma_{l\beta}(V_{g\beta}(F.S.S.) - V_{g\beta}(I.S.S.)) \ ; \ t_{d\beta} \leq t < 3t_{d\beta} \end{cases} \tag{6.107}$$

$$\begin{cases} v_{l0}(t) = V_{g0}(I.S.S.) \ \ ; \ \ 0 \leq t < t_{d0} \\ v_{l0}(t) = V_{g0}(F.S.S.) + \Gamma_{l0}(V_{g0}(F.S.S.) - V_{g0}(I.S.S.)) \ ; \ t_{d0} \leq t < 3t_{d0} \end{cases} \tag{6.108}$$

From (6.106), (6.107) and (6.108) the sequent observations can be done.

- The additional voltage, which causes the overvoltage at the load side, is proportional to the voltage variation seen at the input side.
- Overvoltage for each component is present after the propagation delay time. Therefore, different motor voltage combinations can be found.

By virtue of following the idea proposed in the second observation, three distinct cases could be defined. The corresponding phase-to-ground motor voltages are defined by:

$$\begin{bmatrix} v_{lu} - v_{G1} \\ v_{lv} - v_{G1} \\ v_{lw} - v_{G1} \end{bmatrix} = T_{\alpha\beta 0} \begin{bmatrix} v_{l\alpha}(t_{d\alpha}) \\ v_{l\beta}(t_{d\beta}) \\ v_{l0}(0) \end{bmatrix} \ \ ; \ \ t_{d\alpha} < t_{d0} \tag{6.109}$$

$$\begin{bmatrix} v_{lu} - v_{G1} \\ v_{lv} - v_{G1} \\ v_{lw} - v_{G1} \end{bmatrix} = T_{\alpha\beta 0} \begin{bmatrix} v_{l\alpha}(0) \\ v_{l\beta}(0) \\ v_{l0}(t_{d0}) \end{bmatrix} \quad ; \quad t_{d0} < t_{d\alpha} \tag{6.110}$$

$$\begin{bmatrix} v_{lu} - v_{G1} \\ v_{lv} - v_{G1} \\ v_{lw} - v_{G1} \end{bmatrix} = T_{\alpha\beta 0} \begin{bmatrix} v_{l\alpha}(t_{d\alpha}) \\ v_{l\beta}(t_{d\beta}) \\ v_{l0}(t_{d0}) \end{bmatrix} \quad ; \quad t_{d\alpha} = t_{d0}. \tag{6.111}$$

The line-to-line motor voltage is not highlighted because it is only dependent by the differential mode components.

An example of the problem that can emerge when the speeds presented by the differential mode and the common mode are different is described below. The case when the differential components are faster than the common mode component is considered (i.e. $U_\alpha > U_0$). A PSpice simulation was conducted by using the circuital elements depicted in Fig. 6.13, Fig. 6.20 and Fig. 6.21. The cable considered in this simulation is 12.5 m long. The circuital parameters used in the simulation are summaries in Table 6.1 and Table 6.2. The voltage rise time of the inverter was imposed equal to 30 ns.

Table 6.1: Three-phase cable parameters used in the simulation.

	$r_j(\Omega/\text{m})$	$l_j(\mu\text{H/m})$	$c_j(\text{nF/m})$	$g_j(\mu\Omega/\text{m})$
α	0.8	0.267	0.167	10
β	0.8	0.267	0.167	10
0	0.4	0.237	1.05	10

Table 6.2: Three-phase motor parameters used in the simulation.

$C_{g1}(\text{nF})$	$C_{g2}(\text{nF})$	$L_e(\mu\text{H})$	$R_f(\Omega)$
1.5	1.5	800	1000

Results of a simulation, where $t_{d\alpha} < t_{d0}$, are shown in: Fig. 6.27, Fig. 6.28 and Fig. 6.29. All the voltages represented in the pictures are normalized with respect to the bus voltage of the inverter (V_{dc}).

In Fig. 6.27, the phase-to-ground voltages at the input and at the output terminals of the cables are depicted. As evident from Fig. 6.27(a), the phase-to-ground voltages are limited between -0.5 pu and 0.5 pu. While the load voltages presented

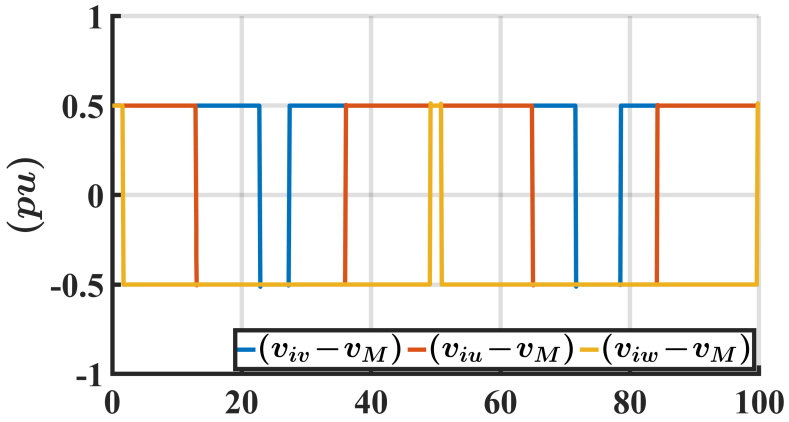
in Fig. 6.27(b) are composed of the voltage trend present at the input of the cable plus overvoltages.

In Fig. 6.28, the phase-to-phase voltages at the input and at the output terminals of the cables are depicted. As illustrated in Fig. 6.28(a), the phase to ground voltages can be equal to 1 pu, −1 pu and 0 pu. While, the load voltages presented in Fig. 6.28(b) are composed of the voltage trend present at the input of the cable plus overvoltages.

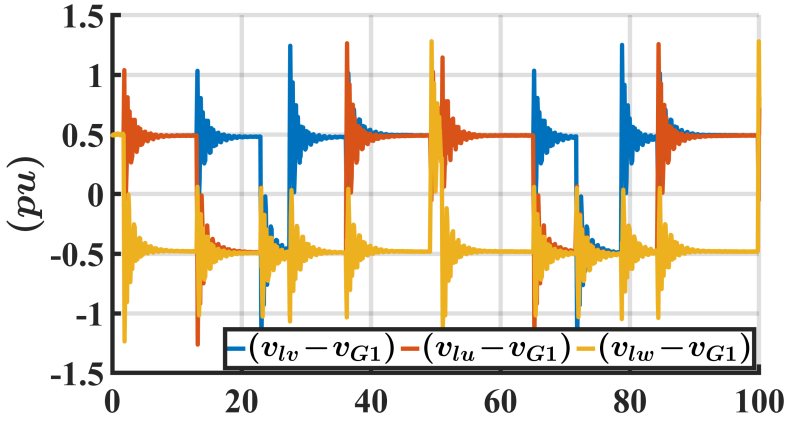
The coordinate transform of the voltages depicted in Fig. 6.27 are shown in Fig. 6.29. In Fig. 6.29(c), a portion of the graph shown in Fig. 6.29 is zoomed. It can be noticed, that differential components present a higher speed with respect to the homopolar component because the propagation delay presented by the differential components is smaller than the common mode one.

By observing the phase-to-phase and the phase-to-ground motor overvoltage the sequent observations can be done

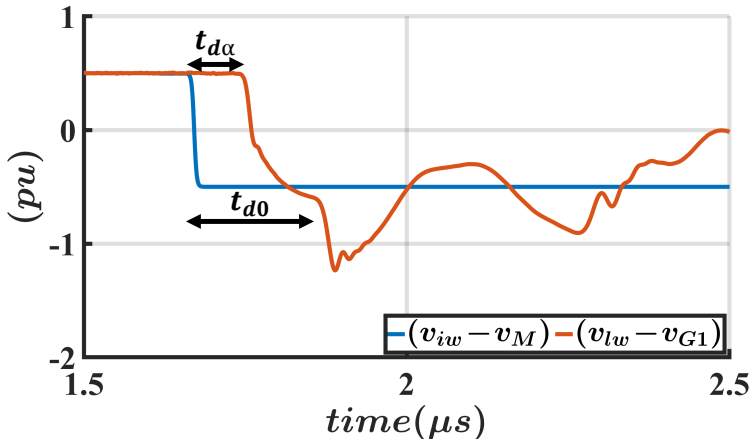
- In Fig. 6.27(c), the differential output voltage is not influenced by the common mode component. This feature is in accordance with what is written in Chapter 6.5.4.
- In Fig. 6.28(c), the phase to ground voltage is shown. It can be noticed that the overvoltage is influenced by both the common and the differential mode.



(a)



(b)



(c)

Figure 6.27: Simulation results when the ground is connected to the middle point of the DC bus: phase-to-ground voltages. (a) voltages at the input terminals of the cable. (b) voltages at the output terminals of the cable. (c) Zoomed portion of (a) and (b).

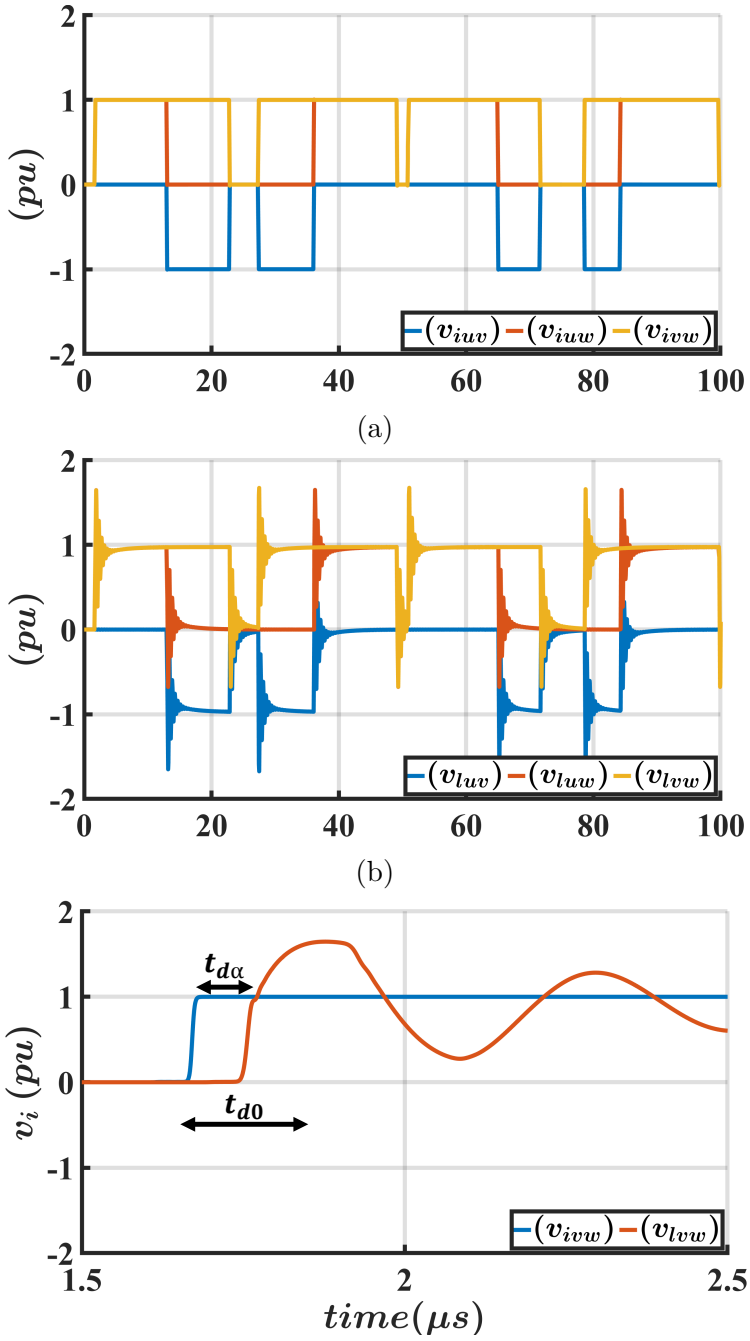
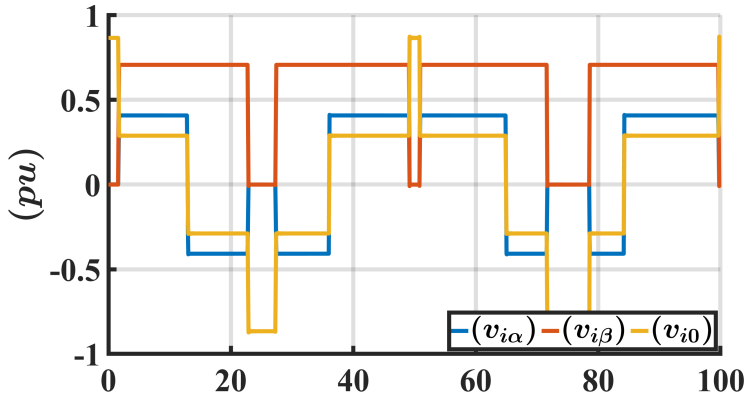
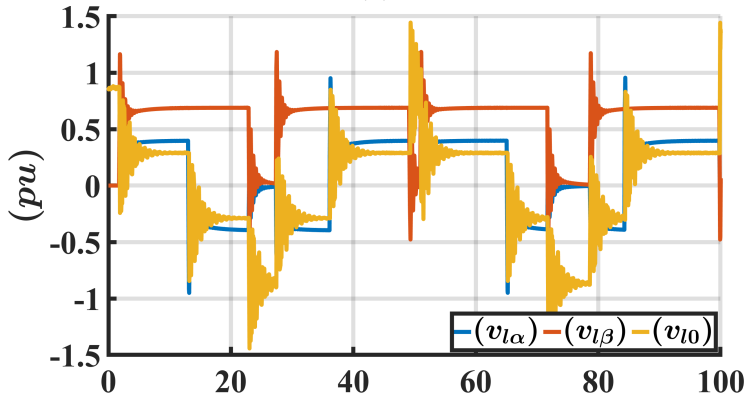


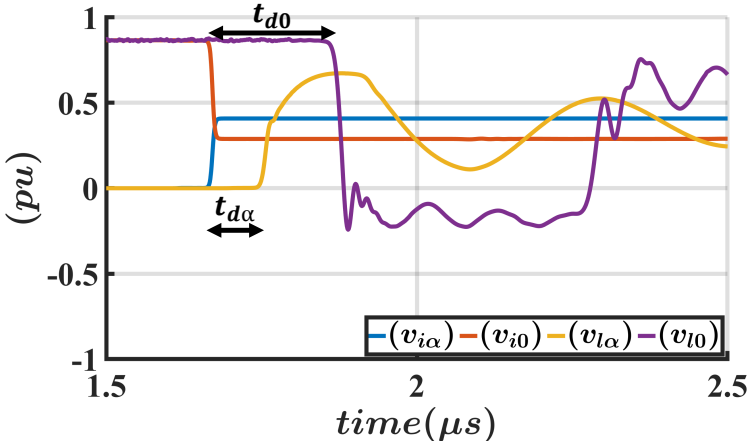
Figure 6.28: Simulation results when the ground is connected to the middle point of the DC bus: phase-to-phase voltages. (a) voltages at the input terminals of the cable. (b) voltages at the output terminals of the cable. (c) Zoomed portion of (a) and (b).



(a)



(b)



(c)

Figure 6.29: Simulation results when the ground is connected to the middle point of the DC bus: α, β and 0 voltages. (a) voltages at the input terminals of the cable. (b) voltages at the output terminals of the cable. (c) Zoomed portion of (a) and (b).

6.6.3 Differential mode propagation speed major than the common mode one

In this section, the motor overvoltages are analyzed when cable present the sequent feature:

$$U_\alpha > U_0 \tag{6.112}$$

which corresponds also to:

$$t_{d\alpha} < t_{d0} \tag{6.113}$$

where U_α is the propagation speed presented by the α component, U_0 is the propagation speed presented by 0 component. The study has been derived by imposing the reflection coefficients equal to 1, thence by having:

$$\Gamma_l = \Gamma_{l\alpha} = \Gamma_{l\beta} = \Gamma_{l0} = 1. \tag{6.114}$$

By using (6.106), (6.107) and (6.108), and applying these statuses to the (6.109) for all the switching states, phase-to-ground and phase-to-phase motor voltages are derived.

Phase-to-frame motor overvoltage

The phase-to-ground voltage values obtained from the formulae have been confirmed by means of simulations tools. From these voltages, the maximum values have been extrapolated and these data have been collected as shown in Table 6.3. The values represented in lines are the initial switching states of the inverter (I.S.S.), while the values represented in the column are the final switching states of the inverter (F.S.S.).

Table 6.3: Maximum phase-to-frame motor voltage: velocity of propagation presented by α and β components is major than the velocity of propagation of the 0 component ($U_\alpha > U_0$).

I \ F	1,-1,-1	1,1,-1	-1,1,-1	-1,1,1	-1,-1,1	1,-1,1	1,1,1	-1,-1,-1
1,-1,-1	$0.5V_{dc}$	$1.17V_{dc}$	$1.5V_{dc}$	$2.17V_{dc}$	$1.5V_{dc}$	$1.17V_{dc}$	$0.83V_{dc}$	$0.83V_{dc}$
1,1,-1	$1.17V_{dc}$	$0.5V_{dc}$	$1.17V_{dc}$	$1.5V_{dc}$	$2.17V_{dc}$	$1.5V_{dc}$	$0.83V_{dc}$	$0.83V_{dc}$
-1,1,-1	$1.5V_{dc}$	$1.17V_{dc}$	$0.5V_{dc}$	$1.17V_{dc}$	$1.5V_{dc}$	$2.17V_{dc}$	$0.83V_{dc}$	$0.83V_{dc}$
-1,1,1	$2.17V_{dc}$	$1.5V_{dc}$	$1.17V_{dc}$	$0.5V_{dc}$	$1.17V_{dc}$	$1.5V_{dc}$	$0.83V_{dc}$	$0.83V_{dc}$
-1,-1,1	$1.5V_{dc}$	$2.17V_{dc}$	$1.5V_{dc}$	$1.17V_{dc}$	$0.5V_{dc}$	$1.17V_{dc}$	$0.83V_{dc}$	$0.83V_{dc}$
1,-1,1	$1.17V_{dc}$	$1.5V_{dc}$	$2.17V_{dc}$	$1.5V_{dc}$	$1.17V_{dc}$	$0.5V_{dc}$	$0.83V_{dc}$	$0.83V_{dc}$
1,1,1	$1.83V_{dc}$	$1.17V_{dc}$	$1.83V_{dc}$	$1.17V_{dc}$	$1.83V_{dc}$	$1.17V_{dc}$	$0.5V_{dc}$	$0.5V_{dc}$
-1,-1,-1	$1.17V_{dc}$	$1.83V_{dc}$	$1.17V_{dc}$	$1.83V_{dc}$	$1.17V_{dc}$	$1.83V_{dc}$	$0.5V_{dc}$	$0.5V_{dc}$

The observations done for Table 6.3 are described as follows.

- Values presented in the diagonal of the matrix (highlighted in grey) are not important because they do not represent any voltage transaction.
- The maximum phase-to-ground voltage reached at the motor side is equal to $2.17V_{dc}$. This voltage is much higher with respect to the maximum declared voltage ($1.5\,V_{dc}$) presented in this work [77].

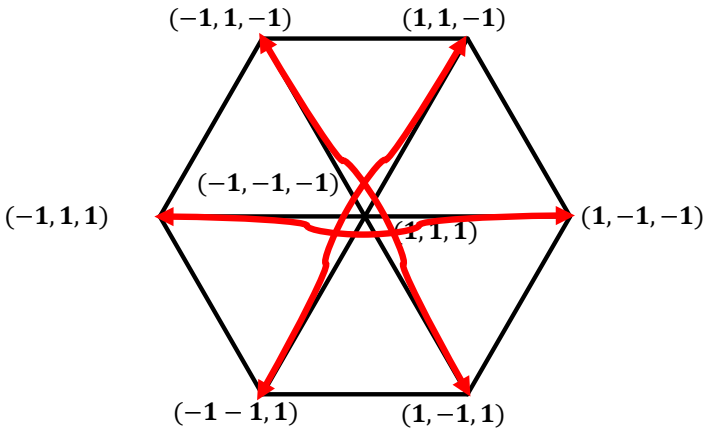


Figure 6.30: Inverter hexagon: dangerous inverter switching path that the inverter must not follow when: the velocity of propagation presented by α and β components major than the velocity of propagation of the 0.

The dangerous switching patterns are represented in Fig. 6.30. These voltage patterns should not be followed by the PWM control unit, thus permitting to limit the phase-to-ground overvoltage.

Phase-to-phase motor overvoltage

The phase-to-phase voltage values obtained from the formulae have been confirmed by means of simulations tools. From these voltages, the maximum values have been extrapolated and these data have been collected as shown in Table 6.4. The values represented in lines are the initial switching states of the inverter (I.S.S.), while the values represented in the column are the final switching states of the inverter (F.S.S.). The observations done for Table 6.4 are described as follows.

- Values presented in the diagonal of the matrix (highlighted in grey) are not important because they do not represent any voltage transaction.
- The maximum phase-to-phase voltage reached at the motor side is equal to $3\,V_{dc}$. The peak voltage that has been found by the mathematical analysis is in accordance with the previous works [77, 111].

Table 6.4: Maximum phase-to-phase motor voltage: velocity of propagation presented by α and β components major than the velocity of propagation of the 0 component ($U_\alpha > U_0$).

I \ F	1,-1,-1	1,1,-1	-1,1,-1	-1,1,1	-1,-1,1	1,-1,1	1,1,1	-1,-1,-1
1,-1,-1	V_{dc}	$2V_{dc}$	$3V_{dc}$	$3V_{dc}$	$3V_{dc}$	$2V_{dc}$	V_{dc}	V_{dc}
1,1,-1	$2V_{dc}$	V_{dc}	$2V_{dc}$	$3V_{dc}$	$3V_{dc}$	$3V_{dc}$	V_{dc}	V_{dc}
-1,1,-1	$3V_{dc}$	$2V_{dc}$	V_{dc}	$2V_{dc}$	$3V_{dc}$	$3V_{dc}$	V_{dc}	V_{dc}
-1,1,1	$3V_{dc}$	$3V_{dc}$	$2V_{dc}$	V_{dc}	$2V_{dc}$	$3V_{dc}$	V_{dc}	V_{dc}
-1,-1,1	$3V_{dc}$	$3V_{dc}$	$3V_{dc}$	$2V_{dc}$	V_{dc}	$2V_{dc}$	V_{dc}	V_{dc}
1,-1,1	$2V_{dc}$	$3V_{dc}$	$3V_{dc}$	$3V_{dc}$	$2V_{dc}$	V_{dc}	V_{dc}	V_{dc}
1,1,1	$2V_{dc}$	$2V_{dc}$	$2V_{dc}$	$2V_{dc}$	$2V_{dc}$	$2V_{dc}$	0	0
-1,-1,-1	$2V_{dc}$	$2V_{dc}$	$2V_{dc}$	$2V_{dc}$	$2V_{dc}$	$2V_{dc}$	0	0

6.6.4 Common mode propagation speed major than the differential one

In this chapter, the motor overvoltages are analyzed when cable present the sequent feature:

$$U_\alpha < U_0 \tag{6.115}$$

which corresponds also to:

$$t_{d\alpha} > t_{d0} \tag{6.116}$$

where U_α is the velocity of propagation presented by the α component, U_0 is the propagation speed presented by 0 component. The study has been derived by imposing the reflection coefficients equal to 1, thence by having:

$$\Gamma_l = \Gamma_{l\alpha} = \Gamma_{l\beta} = \Gamma_{l0} = 1. \tag{6.117}$$

By applying (6.106), (6.107) and (6.108) to (6.110) for all the switching states, phase-to-ground and phase-to-phase motor voltages are derived.

Phase-to-frame motor overvoltage

The phase-to-ground voltage values obtained from the formulae have been confirmed by means of simulations tools. From these voltages, the maximum values have been extrapolated and these data have been collected as shown in Table 6.5. The values represented in lines are the initial switching states of the inverter (I.S.S.), while the values represented in the column are the final switching states of the inverter (F.S.S.). The observations done for Table 6.5 are described as follows.

- Values presented in the diagonal of the matrix (highlighted in grey) are not important because they do not represent any voltage transaction.

- The maximum phase-to-ground voltage reached at the motor side is equal to $1.83\,V_{dc}$. This voltage is higher than the maximum declared voltage ($1.5V_{dc}$) presented in this work [77].

The dangerous switching patterns, that cause the maximum phase-to-ground overvoltages, are represented in Fig. 6.31. These voltage patterns should not be followed by the PWM control unit, thus permitting to limit this value.

Table 6.5: Maximum phase-to-frame motor voltage: velocity of propagation presented by 0 component major than the velocity of propagation of the α and β components ($U_0 > U_\alpha$).

I \ F	1,-1,-1	1,1,-1	-1,1,-1	-1,1,1	-1,-1,1	1,-1,1	1,1,1	-1,-1,-1
1,-1,-1	$0.5V_{dc}$	$1.17V_{dc}$	$0.5V_{dc}$	$1.17V_{dc}$	$0.5V_{dc}$	$1.17V_{dc}$	$1.83V_{dc}$	$1.17V_{dc}$
1,1,-1	$1.17V_{dc}$	$0.5V_{dc}$	$1.17V_{dc}$	$0.5V_{dc}$	$1.17V_{dc}$	$0.5V_{dc}$	$1.17V_{dc}$	$1.83V_{dc}$
-1,1,-1	$0.5V_{dc}$	$1.17V_{dc}$	$0.5V_{dc}$	$1.17V_{dc}$	$0.5V_{dc}$	$1.17V_{dc}$	$1.83V_{dc}$	$1.17V_{dc}$
-1,1,1	$1.17V_{dc}$	$0.5V_{dc}$	$1.17V_{dc}$	$0.5V_{dc}$	$1.17V_{dc}$	$0.5V_{dc}$	$1.17V_{dc}$	$1.83V_{dc}$
-1,-1,1	$0.5V_{dc}$	$1.17V_{dc}$	$0.5V_{dc}$	$1.17V_{dc}$	$0.5V_{dc}$	$1.17V_{dc}$	$1.83V_{dc}$	$1.17V_{dc}$
1,-1,1	$1.17V_{dc}$	$0.5V_{dc}$	$1.17V_{dc}$	$0.5V_{dc}$	$1.17V_{dc}$	$0.5V_{dc}$	$1.17V_{dc}$	$1.83V_{dc}$
1,1,1	$0.83V_{dc}$	$0.17V_{dc}$	$0.83V_{dc}$	$0.17V_{dc}$	$0.83V_{dc}$	$0.17V_{dc}$	$0.5V_{dc}$	$1.5V_{dc}$
-1,-1,-1	$0.17V_{dc}$	$0.83V_{dc}$	$0.17V_{dc}$	$0.83V_{dc}$	$0.17V_{dc}$	$0.83V_{dc}$	$1.5V_{dc}$	$0.5V_{dc}$

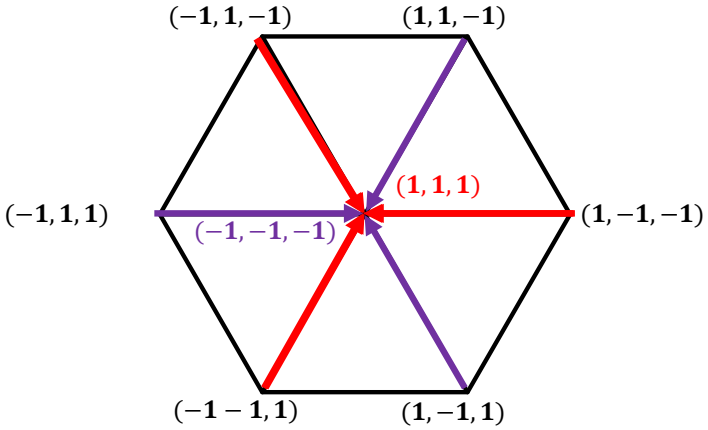


Figure 6.31: Inverter hexagon: dangerous inverter switching path that the inverter must not follow when: the velocity of propagation presented by the 0 component is major than the velocity of propagation of the α and β components.

Phase-to-phase motor overvoltage

The phase-to-phase voltage values obtained from the formulae have been confirmed by means of simulations tools. From these voltages, the maximum values have been extrapolated and these data have been collected as shown in Table 6.6. The values represented in lines are the initial switching states of the inverter (I.S.S.), while the values represented in the column are the final switching states of the inverter (F.S.S.). The observations done for Table 6.6 are described as follows.

- Values presented in the diagonal of the matrix (highlighted in grey) are not important because they do not represent any voltage transaction.
- The maximum phase-to-phase voltage reached at the motor side is equal to V_{dc}. In fact, the differential components have not arrived at the load side. Thence, no variance from the differential point of view is present.

Table 6.6: Maximum phase-to-phase motor voltage: velocity of propagation presented by 0 component major than the velocity of propagation of the α and β components ($U_0 > U_\alpha$).

I \ F	1,-1,-1	1,1,-1	-1,1,-1	-1,1,1	-1,-1,1	1,-1,1	1,1,1	-1,-1,-1
1,-1,-1	V_{dc}	V_{dc}	V_{dc}	V_{dc}	V_{dc}	V_{dc}	V_{dc}	V_{dc}
1,1,-1	V_{dc}	V_{dc}	V_{dc}	V_{dc}	V_{dc}	V_{dc}	V_{dc}	V_{dc}
-1,1,-1	V_{dc}	V_{dc}	V_{dc}	V_{dc}	V_{dc}	V_{dc}	V_{dc}	V_{dc}
-1,1,1	V_{dc}	V_{dc}	V_{dc}	V_{dc}	V_{dc}	V_{dc}	V_{dc}	V_{dc}
-1,-1,1	V_{dc}	V_{dc}	V_{dc}	V_{dc}	V_{dc}	V_{dc}	V_{dc}	V_{dc}
1,-1,1	V_{dc}	V_{dc}	V_{dc}	V_{dc}	V_{dc}	V_{dc}	V_{dc}	V_{dc}
1,1,1	0	0	0	0	0	0	0	0
-1,-1,-1	0	0	0	0	0	0	0	0

6.6.5 Differential mode propagation speed equal to the common mode one

In this section, the motor overvoltages are analyzed when cable present the sequent feature:

$$U_\alpha = U_0 \tag{6.118}$$

which corresponds also to:

$$t_{d\alpha} = t_{d0} \tag{6.119}$$

where U_α is the propagation speed presented by the α component, U_0 is the propagation speed presented by 0 component. The study has been derived by imposing the reflection coefficients equal to 1, thence by having:

$$\Gamma_l = \Gamma_{l\alpha} = \Gamma_{l\beta} = \Gamma_{l0} = 1. \tag{6.120}$$

By applying (6.106), (6.107) and (6.108) to (6.111) for all the switching states, phase-to-ground and phase-to-phase motor voltages are derived.

Phase-to-frame motor overvoltage

The phase-to-ground voltage values obtained from the formulae have been confirmed by means of simulations tools. From these voltages, the maximum values have been extrapolated and these data have been collected as shown in Table 6.7. The values represented in lines are the initial switching states of the inverter (I.S.S.), while the values represented in the column are the final switching states of the inverter (F.S.S.). The observations done for Table 6.7 are described as follows.

- Values presented in the diagonal of the matrix (highlighted in grey) are not important because they do not represent any voltage transaction.
- The maximum phase-to-ground voltage reached at the motor side is equal to $1.5V_{dc}$. This voltage is in accordance with the peak voltage presented in this paper [77].

No switching pattern need to be avoided because the maximum phase-to-ground motor overvoltage is always reached.

Table 6.7: Maximum phase-to-frame motor voltage: velocity of propagation presented by 0 component equal to the velocity of propagation of the α and β components ($U_\alpha = U_0$).

I \ F	1,-1,-1	1,1,-1	-1,1,-1	-1,1,1	-1,-1,1	1,-1,1	1,1,1	-1,-1,-1
1,-1,-1	$0.5V_{dc}$	$1.5V_{dc}$	$1.5V_{dc}$	$1.5V_{dc}$	$1.5V_{dc}$	$1.5V_{dc}$	$1.5V_{dc}$	$1.5V_{dc}$
1,1,-1	$1.5V_{dc}$	$0.5V_{dc}$	$1.5V_{dc}$	$1.5V_{dc}$	$1.5V_{dc}$	$1.5V_{dc}$	$1.5V_{dc}$	$1.5V_{dc}$
-1,1,-1	$1.5V_{dc}$	$1.5V_{dc}$	$0.5V_{dc}$	$1.5V_{dc}$	$1.5V_{dc}$	$1.5V_{dc}$	$1.5V_{dc}$	$1.5V_{dc}$
-1,1,1	$1.5V_{dc}$	$1.5V_{dc}$	$1.5V_{dc}$	$0.5V_{dc}$	$1.5V_{dc}$	$1.5V_{dc}$	$1.5V_{dc}$	$1.5V_{dc}$
-1,-1,1	$1.5V_{dc}$	$1.5V_{dc}$	$1.5V_{dc}$	$1.5V_{dc}$	$0.5V_{dc}$	$1.5V_{dc}$	$1.5V_{dc}$	$1.5V_{dc}$
1,-1,1	$1.5V_{dc}$	$1.5V_{dc}$	$1.5V_{dc}$	$1.5V_{dc}$	$1.5V_{dc}$	$0.5V_{dc}$	$1.5V_{dc}$	$1.5V_{dc}$
1,1,1	$1.5V_{dc}$	$1.5V_{dc}$	$1.5V_{dc}$	$1.5V_{dc}$	$1.5V_{dc}$	$1.5V_{dc}$	$0.5V_{dc}$	$1.5V_{dc}$
-1,-1,-1	$1.5V_{dc}$	$1.5V_{dc}$	$1.5V_{dc}$	$1.5V_{dc}$	$1.5V_{dc}$	$1.5V_{dc}$	$1.5V_{dc}$	$0.5V_{dc}$

Phase-to-phase motor overvoltage

The phase-to-phase voltage values obtained from the formulae have been confirmed by means of simulations tools. From these voltages, the maximum values have been extrapolated and these data have been collected as shown in Table 6.8. The values represented in lines are the initial switching states of the inverter (I.S.S.), while the values represented in the column are the final switching states of the inverter (F.S.S.). The observations done for Table 6.8 are described as follows.

- Values presented in the diagonal of the matrix (highlighted in grey) are not important because they do not represent any voltage transaction.
- The maximum phase-to-phase voltage reached at the motor side is equal to $3\,V_{dc}$. The peak voltage that has been found by the mathematical analysis is in accordance with the previous works [111].

Table 6.8: Maximum phase-to-phase motor voltage: velocity of propagation presented by 0 component equal to the velocity of propagation of the α and β components ($U_\alpha = U_0$).

I \ F	1,-1,-1	1,1,-1	-1,1,-1	-1,1,1	-1,-1,1	1,-1,1	1,1,1	-1,-1,-1
1,-1,-1	V_{dc}	$2V_{dc}$	$3V_{dc}$	$3V_{dc}$	$3V_{dc}$	$2V_{dc}$	V_{dc}	V_{dc}
1,1,-1	$2V_{dc}$	V_{dc}	$2V_{dc}$	$3V_{dc}$	$3V_{dc}$	$3V_{dc}$	V_{dc}	V_{dc}
-1,1,-1	$3V_{dc}$	$2V_{dc}$	V_{dc}	$2V_{dc}$	$3V_{dc}$	$3V_{dc}$	V_{dc}	V_{dc}
-1,1,1	$3V_{dc}$	$3V_{dc}$	$2V_{dc}$	V_{dc}	$2V_{dc}$	$3V_{dc}$	V_{dc}	V_{dc}
-1,-1,1	$3V_{dc}$	$3V_{dc}$	$3V_{dc}$	$2V_{dc}$	V_{dc}	$2V_{dc}$	V_{dc}	V_{dc}
1,-1,1	$2V_{dc}$	$3V_{dc}$	$3V_{dc}$	$3V_{dc}$	$2V_{dc}$	V_{dc}	V_{dc}	V_{dc}
1,1,1	$2V_{dc}$	$2V_{dc}$	$2V_{dc}$	$2V_{dc}$	$2V_{dc}$	$2V_{dc}$	0	0
-1,-1,-1	$2V_{dc}$	$2V_{dc}$	$2V_{dc}$	$2V_{dc}$	$2V_{dc}$	$2V_{dc}$	0	0

6.7 Conclusions

Overvoltages at the motor side have regained importance due to the introduction of SiC devices. In this chapter, the transmission line theory has been revised. The theory of two-conductor transmission line has been provided by considering also the aspect of the voltage rise time versus the load overvoltage. Existing formulae present in the literature give the load overvoltage in function of the voltage rise time and the cable length. However, this formula shows inaccuracy after an accurate study. Thus, a novel formula that permits to calculate correctly the load overvoltage has been proposed and validated through simulations.

In order to analyse the motor overvoltage, the theory of two-conductor transmission line has been extended to four-conductor transmission line. It has been demonstrated that the power cable can be analyzed by means of three independent two-conductor transmission lines. In this model, diverse velocities of propagation for differential (α and β) and common mode (0) components have not been considered before. However, after careful analysis, it was found that diverse velocities of propagation may affect the motor overvoltage. Motor overvoltages, caused by all switching patterns of the three-phase inverter, have been calculated for three different cases:

1. When the velocity of propagation presented by α and β components is higher than the velocity propagation of the 0 component.

2. When the velocity of propagation presented by 0 component is higher than the velocity propagation of the α and β components.

3. When the velocity of propagation presented by α and β components is equal to velocity propagation of the 0 component.

Formulation results obtained for a drive where the ground is connected to the middle point of the DC bus, are summarized below:

- the phase-to-frame motor voltage can reach to $2.17\,V_{dc}$ instead of $1.5\,V_{dc}$, when the velocity of propagation presented by α and β components is higher than velocity propagation of the 0 component;

- the phase-to-frame motor voltage can reach to $1.83\,V_{dc}$ instead of $1.5\,V_{dc}$, when the velocity propagation presented by 0 component is higher than the velocity propagation of the α and β components;

- the phase-to-frame motor voltage can reach $1.5\,V_{dc}$, when velocity propagation presented by α and β components is equal to velocity propagation of the 0 component;

- the phase-to-phase motor voltage can always reach to $3\,V_{dc}$.

Following these results, the sequent implications can emerge:

- the power cable should be designed with equal velocity propagation for all components (α, β and 0), thence, the motor insulation between the phases and the frame is treated better;

- Criticalities can be present by the sequent control strategies: Finite Control Set Model Predictive Control (FCS-MPC) or Direct Torque Control (DTC). Based on the installed cable, the PWM unit of the inverter should avoid the switching patterns defined in this chapter.

Chapter 7

Drive parameter identification and motor overvoltage simulation

Part of the work described in this chapter has been previously published in [62, 89].

7.1 Introduction

In Chapter 6, the electric drive model was defined. According to this chapter, important parameters such as characteristic impedance, velocity of propagation are required. For drive simulations and filter designing, parameters of the drive must be identified precisely. One of the conventional methods to derive these parameters is the application of an LCR meter.

In this chapter, measurement methodologies and simulations of electric drive for motor overvoltage analysis are studied. The measurement methodology with LCR meter has been described in detail. In addition to this method, a novel method for the parameter estimation of the drive has been proposed that makes the filter design faster. Then, by taking as a reference an existing drive, the overvoltage presented by the motor has been studied using the equivalent drive model described in Chapter 6. By the measurement of the drive parameters, it has been noticed that the simulation of both overvoltage and the line current owing to the skin effect presented by the cable was not possible. Thus, a new simple elementary component of the transmission line, which permits the simulation of both high and low-frequency phenomena, has been developed. The simulation conducted by this circuit showed good agreement with the experimental results.

7.2 LCR measurements method

Simulation and filter design processes require the parameters of inverter, cable and motor. The rise time voltage imposed by the three-phase inverter can be derived easily by using an oscilloscope. The cable parameters can be derived using an LCR meter and by applying a series of formulae [78, 112]. The motor parameters can be derived by applying the methodology described in [107]. Standard cable and motor parameter identification processes are described here.

7.2.1 Power cable parameters identification

Per unit length parameters defined in (6.57), (6.58), (6.59) and (6.60) are required. In this section, symmetrical cable is considered. However, in case that an asymmetrical cable is used, the methodology proposed in [62] can be adopted. In fact, the methodology proposed in this work permits to study the motor overvoltage phenomenon using an equivalent symmetrical cable by considering the worst-case scenario from the differential point of view. The lowest differential characteristic impedance indeed can be determined by choosing the right terminals of the cable.

In this section, the description of the measurement methodology has been split into two sections: differential mode and common mode. The differential mode is associated with the components α and β, while the common mode is associated with the 0 component (see Chapter 6).

Differential mode cable parameters

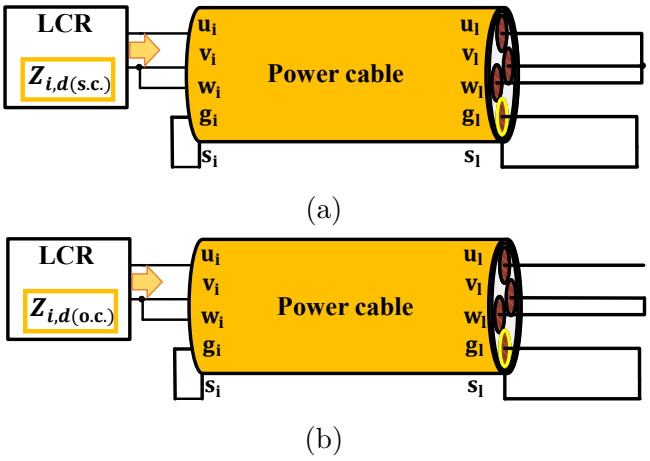


Figure 7.1: Differential mode parameter measurements of the cable. (a) Short-circuit configuration and (b) Open-circuit configuration.

Cable parameters can be derived by applying the short and open circuit tests.

In Fig. 7.1, it is schematically described how should the short circuit and the open circuit tests be done. In order to maintain the convection used in Chapter 6 (Clarke transformation which maintains invariant the power), the results of these two tests need to be multiplied by a factor equal to 2/3. Thence, the measurement can be described by:

$$\bar{Z}_{i,\alpha}(s.c.) = \frac{2}{3}\bar{Z}_{i,d}(s.c.) \tag{7.1}$$

$$\bar{Z}_{i,\beta}(s.c.) = \frac{2}{3}\bar{Z}_{i,d}(s.c.) \tag{7.2}$$

$$\bar{Z}_{i,\alpha}(o.c.) = \frac{2}{3}\bar{Z}_{i,d}(o.c.) \tag{7.3}$$

$$\bar{Z}_{i,\beta}(o.c.) = \frac{2}{3}\bar{Z}_{i,d}(o.c.) \tag{7.4}$$

where, $Z_{i,d}(s.c.)$ represents the short circuit test (indicated with s.c.) and $Z_{i,d}(o.c.)$ represents the open circuit test (indicated with o.c.). The complex characteristic impedances of the α and β components can be derived by using the short and open circuit measurements as in:

$$\bar{Z}_{\alpha} = \sqrt{\bar{Z}_{i,\alpha}(s.c.) \cdot \bar{Z}_{i,\alpha}(o.c.)} \tag{7.5}$$

$$\bar{Z}_{\beta} = \sqrt{\bar{Z}_{i,\beta}(s.c.) \cdot \bar{Z}_{i,\beta}(o.c.)}. \tag{7.6}$$

The complex propagation constant of the cable can be derived by:

$$\bar{\gamma}_{\alpha} = \frac{1}{D} atanh\left(\sqrt{\frac{\bar{Z}_{i,\alpha}(s.c.)}{\bar{Z}_{i,\alpha}(o.c.)}}\right) \tag{7.7}$$

$$\bar{\gamma}_{\beta} = \frac{1}{D} atanh\left(\sqrt{\frac{\bar{Z}_{i,\beta}(s.c.)}{\bar{Z}_{i,\beta}(o.c.)}}\right) \tag{7.8}$$

where D represents the cable length. It can be demonstrated that the factor 2/3 is not important for the complex propagation constant. As it is reasonable to think the multiplicative factor introduced by the coordinate transformation could never change the velocity of propagation of the waveform.

By using (7.5), (7.6), (7.7) and (7.8) the per unit length parameters of each component can be derived as follows:

$$r_{\alpha}(\omega) + j\omega l_{\alpha}(\omega) = \bar{Z}_{\alpha}\bar{\gamma}_{\alpha} \tag{7.9}$$

$$r_{\beta}(\omega) + j\omega l_{\beta}(\omega) = \bar{Z}_{\beta}\bar{\gamma}_{\beta} \tag{7.10}$$

$$g_{\alpha}(\omega) + j\omega c_{\alpha}(\omega) = \frac{\bar{\gamma}_{\alpha}}{\bar{Z}_{\alpha}} \tag{7.11}$$

$$g_\beta(\omega) + j\omega c_\beta(\omega) = \frac{\bar{\gamma}_\beta}{\bar{Z}_\beta}. \tag{7.12}$$

The per unit parameters of each component are in function of the frequency. The per unit length parameters that are most affected by the frequency are the resistance and the inductance. The variation of these values is caused by the skin effect presented by the cable.

Standard simulation tools accept only a constant value, thence the right frequency needs to be chosen. The preferred method is to impose the frequency equal to the natural frequency of the cable [78]. Unfortunately, by choosing a frequency very close to the natural frequency, there is a risk of encountering large measurement errors. Thence, the solution is to get closer to the natural frequency value. In case that the natural frequency is not well known, a reasonable frequency can be chosen (e.g. 300 kHz). Thence, using this frequency the cable parameter can be measured. In case that higher accuracy is required by the simulation, the per unit parameters derived previously can be used in:

$$f_\alpha = \frac{1}{4 \cdot D \cdot \sqrt{l_\alpha \cdot c_\alpha}} \tag{7.13}$$

$$f_\beta = \frac{1}{4 \cdot D \cdot \sqrt{l_\beta \cdot c_\beta}} \tag{7.14}$$

where, f_α and f_β represent the natural frequency of the two components, while D represents the cable length. Thence, this time the cable parameters can be evaluated by using a frequency much closer to the natural frequency of the cable. This process can be repeated until then the desired convergence is reached.

Common mode cable parameters

Cable parameters can be derived by applying the short and open circuit tests. In Fig. 7.2, it is schematically described how should the short circuit and the open circuit tests be done. In order to maintain the convection used in Chapter 6 (Clarke transformation which maintains invariant the power), the results of these two tests need to be multiplied by a factor equal to 3. Thence, the measurement can be described by:

$$\bar{Z}_{i,0}(s.c.) = 3\bar{Z}_{i,c}(s.c.) \tag{7.15}$$

$$\bar{Z}_{i,0}(o.c.) = 3\bar{Z}_{i,c}(o.c.) \tag{7.16}$$

where, $\bar{Z}_{i,c}(s.c.)$ represents the short circuit test (indicated with s.c.) and $\bar{Z}_{i,c}(o.c.)$ represents the open circuit test (indicated with o.c.). The complex characteristic impedance of the ”0” component can be derived using the short and open circuit measurements as in:

$$\bar{Z}_0 = \sqrt{\bar{Z}_{i,0}(s.c.) \cdot \bar{Z}_{i,0}(o.c.)} \tag{7.17}$$

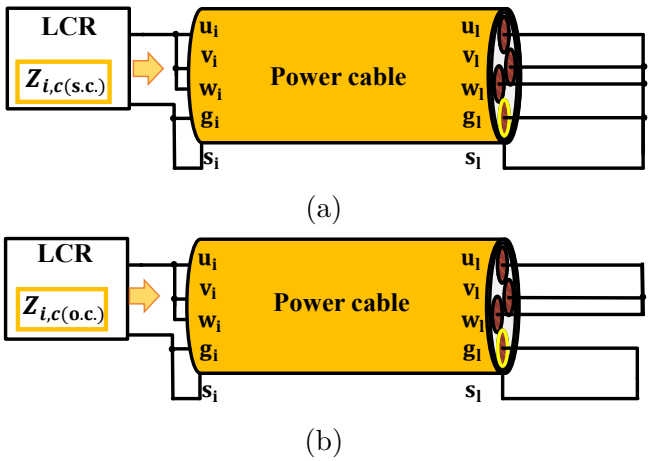


Figure 7.2: Common mode parameter measurements of the cable. (a) Short-circuit configuration. (b) Open-circuit configuration.

The complex propagation constant of the cable can be derived by:

$$\bar{\gamma}_0 = \frac{1}{D} atanh\left(\sqrt{\frac{\bar{Z}_{i,0}(s.c.)}{\bar{Z}_{i,0}(o.c.)}}\right) \tag{7.18}$$

where D represents the cable length. It can be demonstrated that the factor 3 is not important for this parameter. As it is reasonable to think the multiplicative factor introduced by the coordinate transformation could never change the velocity of propagation of the waveform.

By using (7.17) and (7.18) the per unit length parameters of each component can be derived as shown in:

$$r_0(\omega) + j\omega l_0(\omega) = \bar{Z}_0 \bar{\gamma}_0 \tag{7.19}$$

$$g_0(\omega) + j\omega c_0(\omega) = \frac{\bar{\gamma}_0}{\bar{Z}_0}. \tag{7.20}$$

The per unit length parameters that are most affected by the frequency are the resistance and the inductance. The variation of these values is caused by the skin effect presented by the cable.

Standard simulation tools accept only a constant value, thence the right frequency needs to be chosen. The preferred method is to impose the frequency equal to the natural frequency of the cable [78]. Unfortunately, by choosing a frequency very close to the natural frequency, there is a risk of encountering large measurement errors. Thence, the solution is to get closer to the natural frequency value. In case that the natural frequency is not well known, a reasonable frequency can be chosen (e.g. 300 kHz). Thence, using this frequency the cable parameter can be

measured. In case that higher accuracy is required by the simulation, the per unit parameters derived previously can be used in:

$$f_0 = \frac{1}{4 \cdot D \cdot \sqrt{l_0 \cdot c_0}} \tag{7.21}$$

where, f_0 represents the natural frequency, while D represents the cable length. Thence, cable parameters can be evaluated by using a frequency much closer to the natural frequency of the cable. This process can be repeated until then the desired convergence is reached.

7.2.2 Motor parameters identification

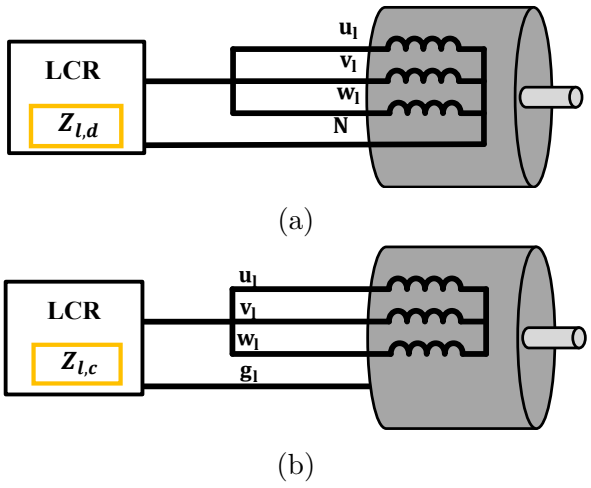


Figure 7.3: Motor parameter measurement. (a) Phase-to-neutral and (b) phase-to-ground.

The parameters of the equivalent lumped circuit represented in Fig. 6.21 are required. Using an LCR meter and following the measurement method presented schematically in Fig. 7.3, the frequency response of the motor can be measured. Then, parameters of the lumped equivalent circuit can be determined by using the least squares method [67, 107, 108].

7.3 Oscilloscope parameter identification method

A novel measurement method which permits to identify the parameters associated with the motor overvoltage phenomenon is proposed. This method becomes effective for the sizing of filters [89]. In fact, characteristic impedances (Z_α, Z_β and Z_0), propagation delays ($t_{d\alpha}$, $t_{d\beta}$ and t_{d0}) and reflection coefficients at the load side

($\Gamma_{l\alpha}$, $\Gamma_{l\beta}$ and Γ_{l0}) can be evaluated using this method. Instead of using an LCR meter, multichannel oscilloscope is adopted. In practice, using the oscilloscope voltages and currents at the cable terminals can be sampled. Thence, exploiting the Clarke transformation, α, β and 0 variables are obtained. This procedure permits to identify the parameters of a drive already mounted, even without the need to block the production process of the industrial plant.

7.3.1 Experimental data and their processing

Figure 7.4: The experimental setup.

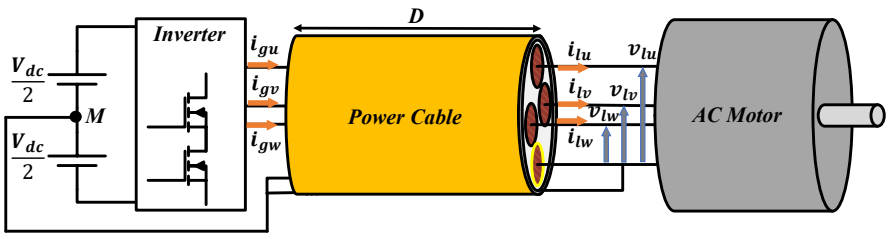


Figure 7.5: Schematic representation of a drive, which presents the ground reference connected to the middle point of the DC bus.

The proposed method was applied to a real experimental setup (Fig. 7.4) without the RL filter. An equivalent scheme of the laboratory test bench that represents the place where the probes were placed is depicted in Fig. 7.5.

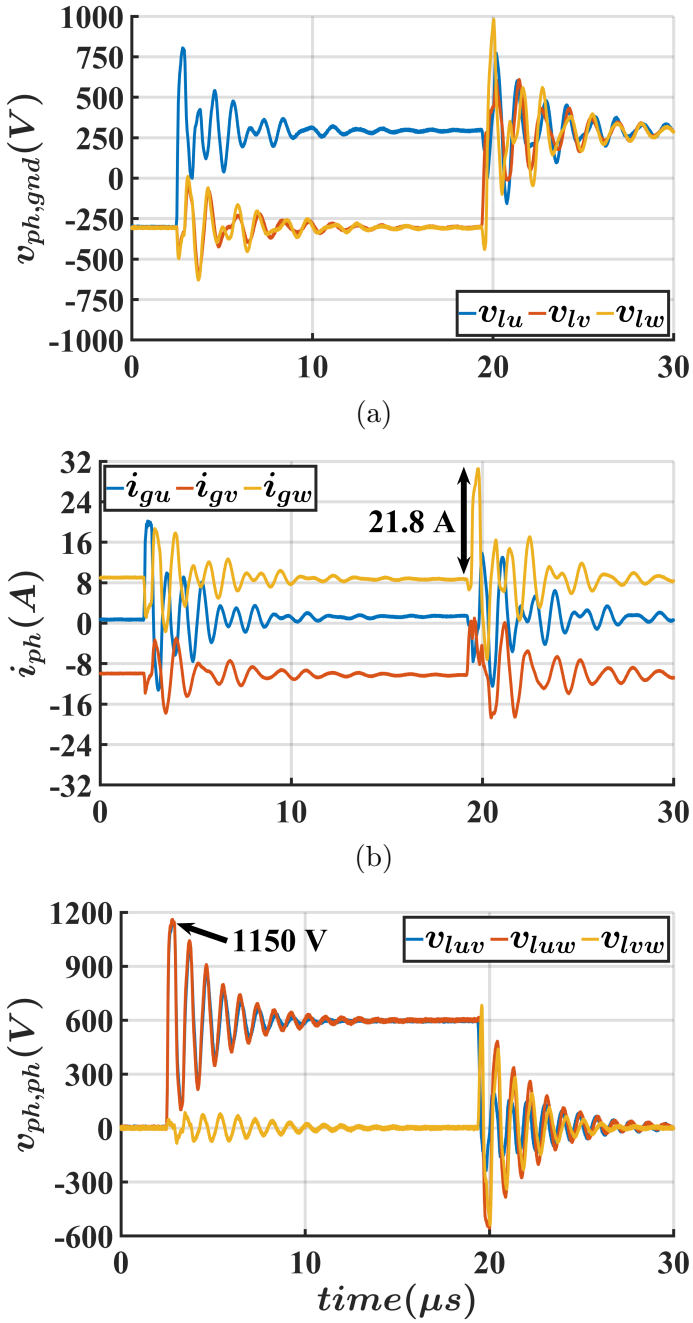


Figure 7.6: Experimental results obtained from the drive shown in Fig. 7.4. (a) Line-to-ground motor voltage, (b) inverter currents and (c) line-to-line motor voltages.

The experimental measurements of the cable are presented in Fig. 7.6. Cable input currents and cable output voltages were simultaneously measured. During the experiments, the motor was running without any mechanical load connected to the shaft. The motor was running at a mechanical speed of 1500 rpm. The bus voltage of the inverter was imposed equal to 600 V. Fig. 7.6(c) and Fig. 7.6(a) report the presence of overvoltage at the motor line-to-line terminals (i.e. 1150 V instead of 600 V) and overvoltage at the motor phase-to-ground terminals (i.e. 980 V instead of 300 V). Meanwhile, current spikes (21 A) added to the inverter current can be noticed (Fig. 7.6(b)).

It can be seen that identifying an electrical frequency of evolution of the overvoltage and overcurrent from the waveforms shown in Fig. 7.6(a) and Fig. 7.6(b) is a complicated task. This is caused by the fact that the common and differential modes phenomena are superimposed. As a consequence, in order to simplify the analysis, the Clarke transformation can be applied.

The Clarke transformation has been applied to the motor line-to-frame voltages and to the input cable currents, as depicted in Fig. 7.7. In order to simplify the study, only α and 0 components have been considered in this example. It can be noticed from both these figures that overvoltage at the load side and overcurrent at the inverter side are still present. Anyway, this time the electrical variables are undistorted damped sinusoids thence permitting to identify the electrical frequency.

7.3.2 Power cable parameters identification

Characteristic impedance

Surge impedances (α, β and 0) are identified as the ratio between the cable input voltage variation and the correspondent peak current. In Fig. 7.7(a), each time the voltage α component changes a correspondent overcurrent appears. The ΔV_α and the corresponding i_α amplitude leads to a characteristic impedance of 25.82 Ω ($Z_\alpha = 490\,\text{V}/18.98\,\text{A}$). In the same way, using data from Fig. 7.7(b), the ΔV_0 and the corresponding i_0 amplitude leads to a characteristic impedance of 44.3 Ω ($Z_0 = 346\,\text{V}/7.8\,\text{A}$).

Propagation delay

The time the voltage takes to travel from the cable input to the cable output is the propagation delay (t_{dj}). The propagation delay of the α component ($t_{d\alpha}$) was measured and it is equal to 205 ns while the propagation delay of the 0 component is equal to 210 ns.

In case that the same oscilloscope cannot be used for measurement of the input and the output voltages, because the two places (i.e. inverter and motor) are placed far away, the time delay of the cable can be identified by measuring the frequency of the overvoltage waveform.

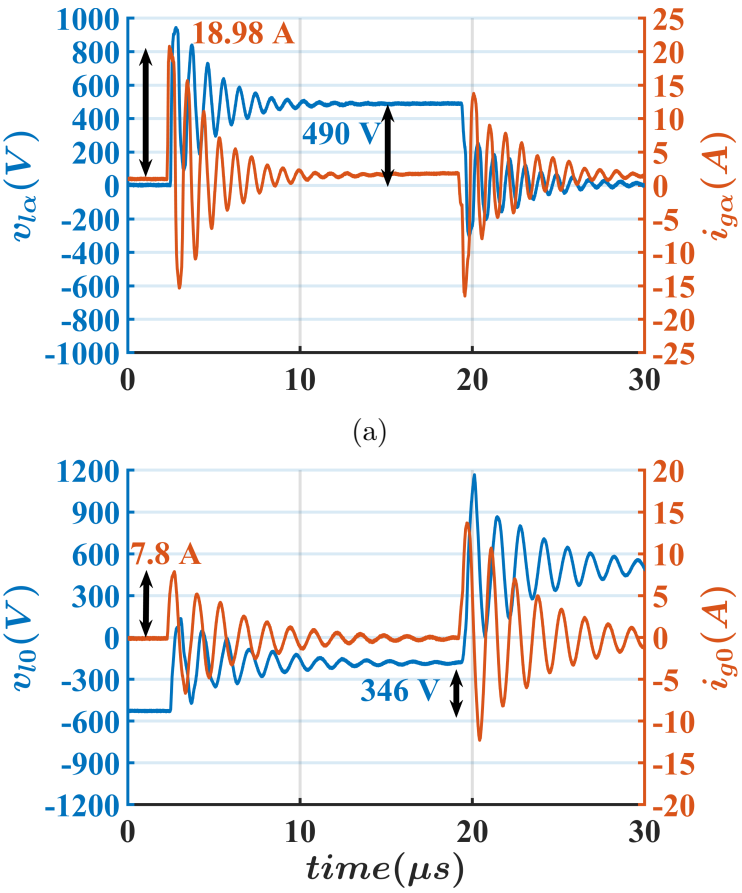


Figure 7.7: Clarke transformation of the experimental results shown in Fig. 7.6. (a) Inverter α component current and motor α component voltage. (b) Inverter 0 component current and motor 0 component voltage.

7.3.3 Motor parameters identification

The load reflection coefficient (Γ_{lj}) is identified as the ratio between the peak voltage at the cable output ($\widehat{V}_{lj}$) and the voltage at the cable input (v_{gj}). Equal reflection coefficient was found for the three components:

$$\Gamma_{l\alpha} = \Gamma_{l\beta} = \Gamma_{l0} = 0.92 \tag{7.22}$$

These three reflection load coefficients can be associated to the equivalent motor model depicted in Fig. 6.23.

7.4 Motor overvoltage simulation

In this section, the simulation results adopting the drive model proposed in Chapter 6 are compared with the laboratory tests. It has been deduced from the comparison that the simulation of both motor overvoltage and line current was not possible owing to the cable skin effect. Thence, a new transmission line model has been proposed. Simulation results obtained by using a new model of transmission line and experimental results obtained from an electric drive are compared.

7.4.1 The experimental setup

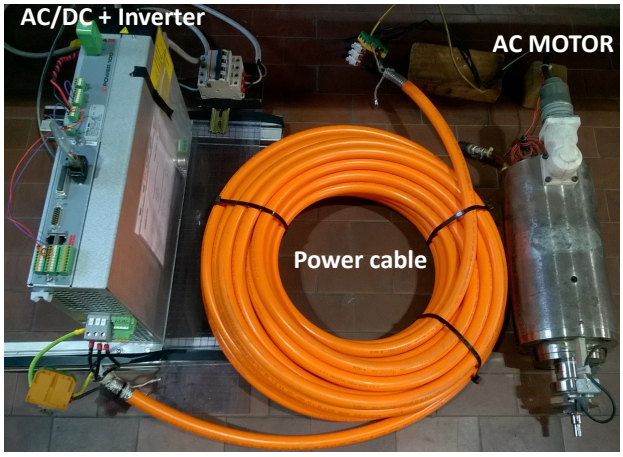


Figure 7.8: Laboratory test bench used for the comparison between experimental measurements and proposed simulation results.

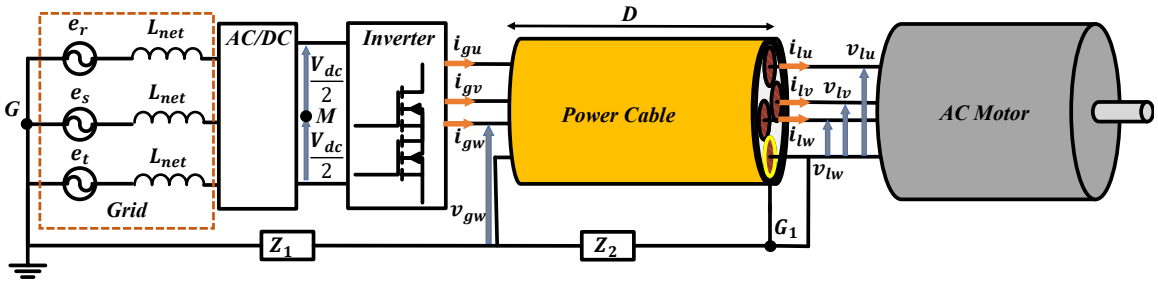


Figure 7.9: Schematic circuital representation of the drive represented in Fig. 7.8.

The used electric drive is illustrated in Fig. 7.8. The details and the descriptions of each component of the electric drive are explained as follows.

- XP100-75-A described in Chapter 2.2.3 was used. This converter is composed by an all-Si inverter plus a three-phase diode rectifier, which was connected to the grid.

- 35 m of power cable was adopted (Igus Chainflexd CF27.D). It is a cable composed of three conductors plus an earth conductor with a copper section of 10 mm^2. Furthermore, the cable has a shield that permits to reduce the EMI issues.
- A 13.7 kW high-speed induction motor was used (Gamfior GP18).

All-Si inverter was connected to the motor by means of the described power cable, as schematically depicted in Fig. 7.9. The rectifier present inside the power converter was connected to the power grid of the laboratory. The inverter was controlled by using V/Hz strategy. No mechanical load was connected to the motor shaft.

7.4.2 Drive parameters identification

Cable parameters

The parameters of the cable shown in Fig. 7.8 are derived by using the methodology proposed in Chapter 7.2. The measurements were conducted using an LCR meter (Hioki 3532-50). The data have been processed and the results are depicted in Fig. 7.10 and Fig. 7.11. It can be noticed from the experimental results that the per unit length inductance and resistance of the cable vary a lot with the operating frequency. For this reason, an operating frequency close to the natural frequency of the cable has been selected. These parameters were derived by setting the operating frequency of the impedance meter near the natural frequency of the cable. Per unit length parameters of α, β and 0 components are summarized in Table 7.1. Furthermore, characteristic impedance (Z_j), natural cable frequency (f_j) and the velocity of propagation (U_j) are added to the table.

Table 7.1: Standard parameters of the experimental setup shown in Fig. 7.8.

	$r_j(\Omega/\text{m})$	$l_j(\mu\text{H/m})$	$c_j(\text{nF/m})$	$g_j(\mu\text{S/m})$	$U_j(\text{Gm/s})$	$f_j(\text{MHz})$	$Z_j(\Omega)$
α	0.1571	0.1512	0.2273	56.54	0.17058	1.2	25.79
β	0.1571	0.1512	0.2273	56.54	0.17058	1.2	25.79
0	0.2713	0.2659	0.1358	34.68	0.166	1.2	44.25

Motor parameters

The parameters of the equivalent circuit defined in Fig. 6.21 need to be identified. The process described in Chapter 7.2.2 was applied. In fact, the least squares method was used. The motor parameters were derived from the data depicted in Fig. 7.12 and these coefficients are summarized in Table 7.2. In this figure, the simulation (i.e. transfer function of the equivalent circuit) and the measurements are plotted and compared. As can be seen from these two traces, there is an agreement

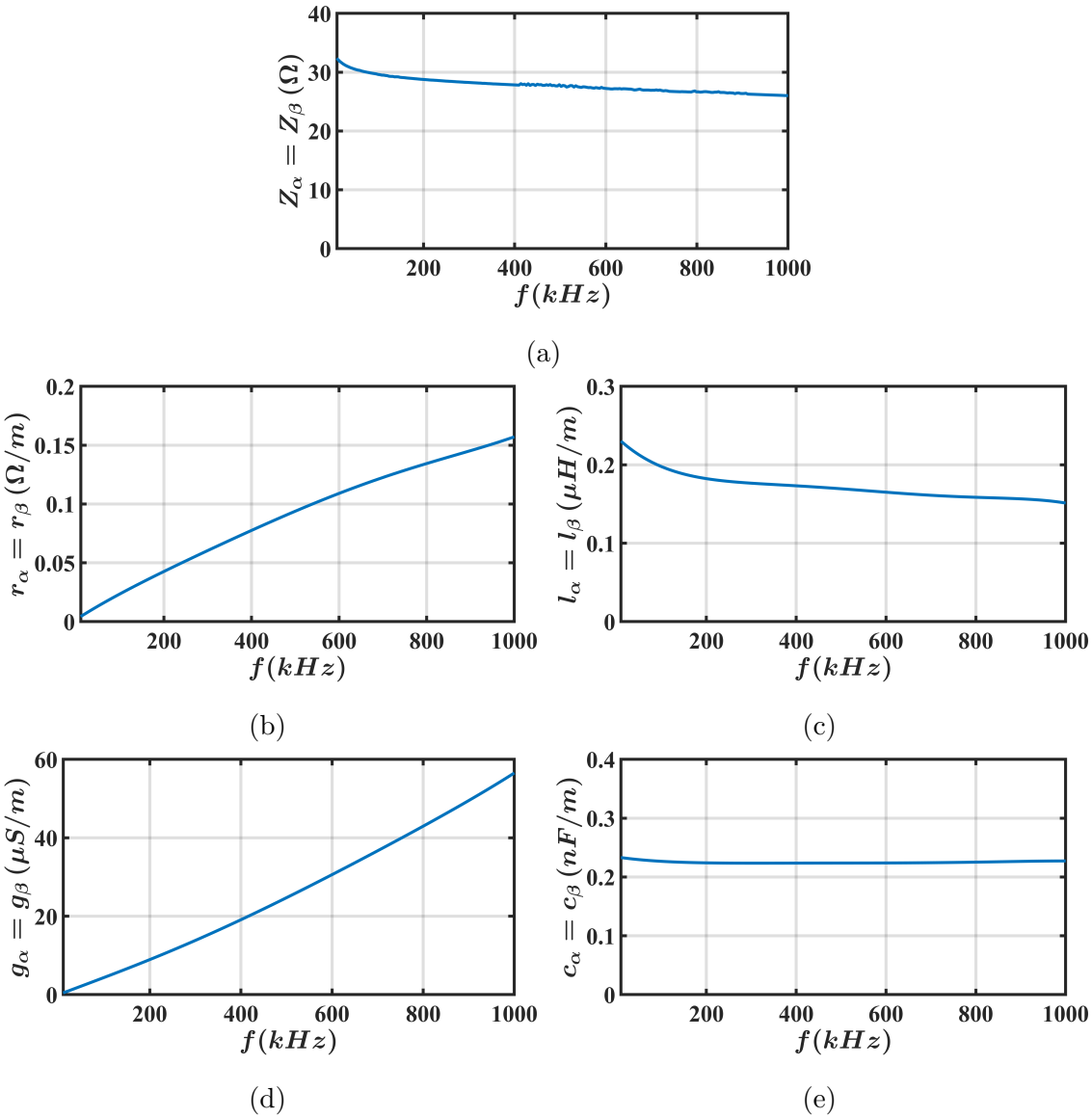


Figure 7.10: Measured parameters of the differential components in function of the frequency: (a) cable characteristic impedance, (b) per unit cable resistance, (c) per unit cable inductance, (d) per unit cable conductance and (e) per unit cable capacitance.

between the transfer function of the equivalent circuit defined in Chapter 6.5.4 and the experimental results.

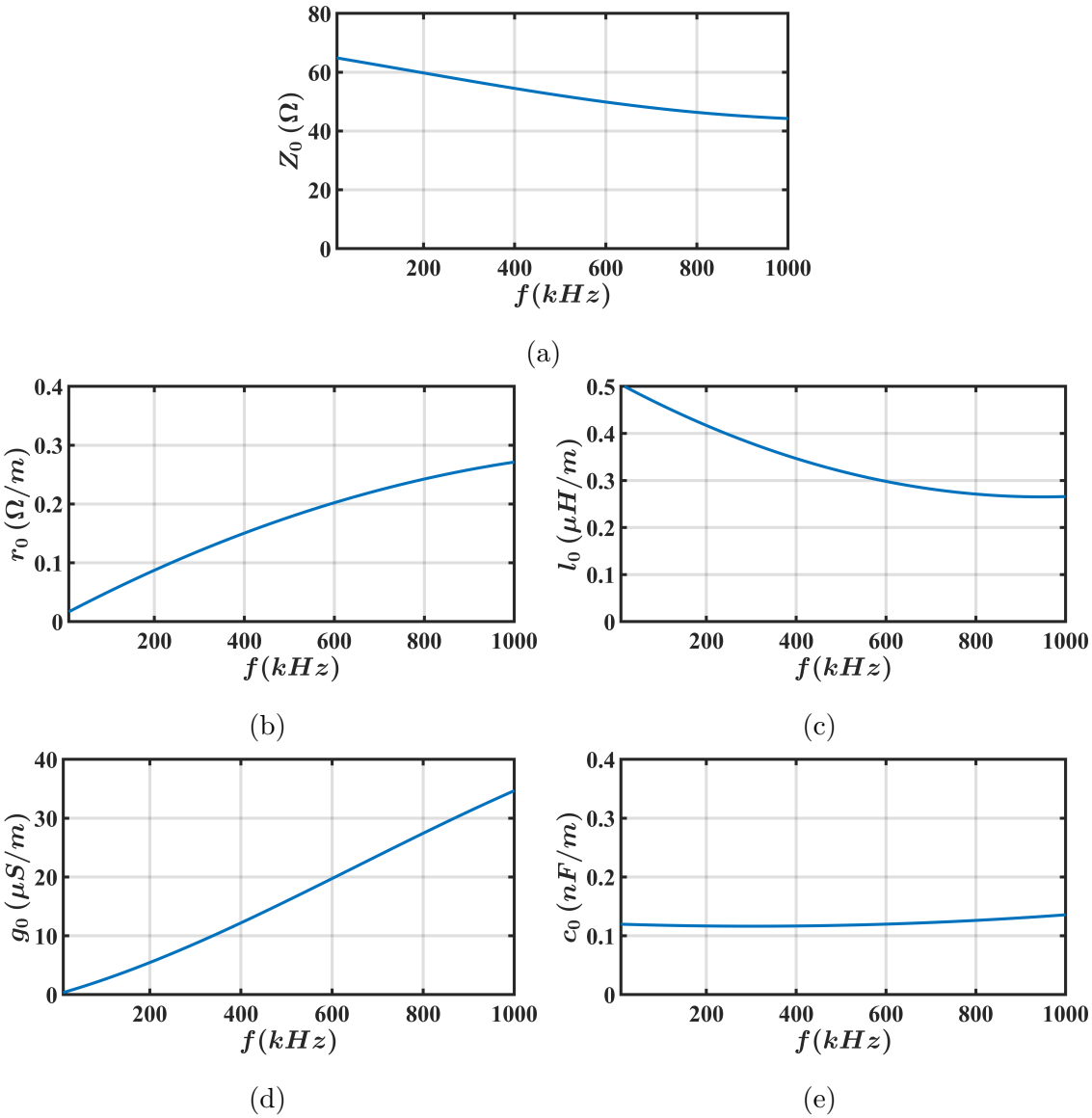


Figure 7.11: Measured parameters of the common mode component in function of the frequency: (a) cable characteristic impedance, (b) per unit cable resistance, (c) per unit cable inductance, (d) per unit cable conductance and (e) per unit cable capacitance.

Table 7.2: Motor parameters derived by using the least squares method.

C_{g1}(nF)	C_{g2}(nF)	L_e(μH)	R_f(Ω)
3.13	10.86	62.3	140

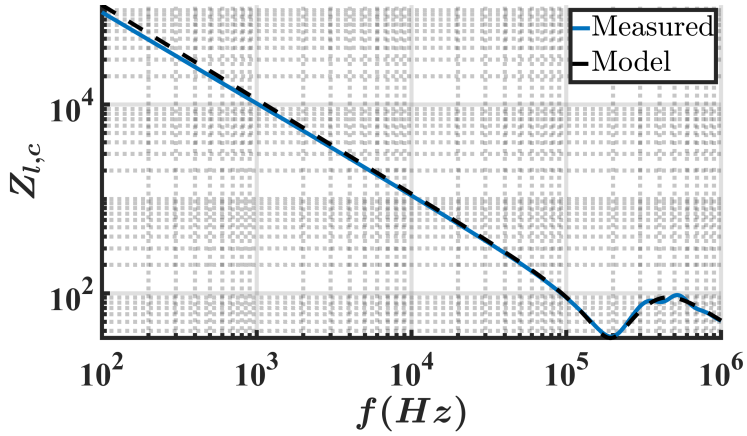


Figure 7.12: Motor frequency responses: magnitude of the phase-to-ground impedance.

7.4.3 Simulation issues

The parameters identified previously were introduced in a simulation containing the circuital elements illustrated in Fig. 6.13, Fig. 6.20 and Fig. 6.21. From the simulation results, no congruence between the experimental and simulation results was found. The important issues found during the simulation are described below.

- Issues are present if both the overvoltage and the line current are under analysis.
- If low per unit resistance is inserted in the simulation, motor overvoltage and inverter overcurrent are undamped, thus the motor overvoltage and the inverter overcurrent are damped out after many cycles.
- If high per unit resistance is used in the simulation, motor overvoltage and inverter overcurrent are damped but the inverter current could not flow in the cable owing to the high resistive value presented at that frequency (look in Table 7.1 where the results are highlighted). In fact, at a nominal current of 30 A, the voltage drop that would occur on the line is approximately equal to 160 V.

By virtue of all the problems described, a new model that permits to simulate two different phenomena, motor voltage and inverter current, at the same time is required.

7.4.4 New proposed model of transmission line

The need for a new model is due to the willingness to observe simultaneously the motor overvoltage and the inverter line current. With only a resistive (r) and

an inductive (l) element (see Fig. 6.1), it is not possible to include the skin effect phenomenon of the cable. Many authors studied the phenomena of overvoltage with the consideration of the skin effect [113] but many circuital components are needed in the simulation, thus causing an increase of the simulation time.

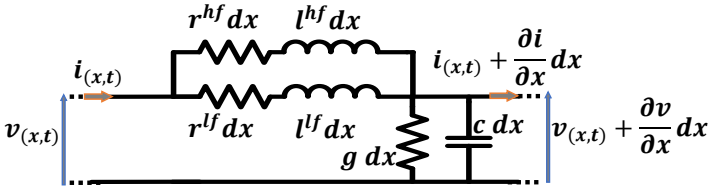


Figure 7.13: Schematic representation of an elementary component of transmission line: the proposed one.

The introduction of the other two electrical parts, a resistance, and an inductance, gives the opportunity to study the phenomena skin effect phenomenon. The schematic representation of an elementary novel component of the transmission line is depicted in Fig. 7.13. Four parameters are defined in Fig. 7.13: two low-frequency and two high-frequency parameters. The high-frequency parameters are the parameters of the system derived at the natural frequency of the cable, where this frequency has been defined in (7.13), (7.14) and (7.21). The low-frequency parameters are derived at the frequency imposed by the PWM unit of the control.

- r_j^{hf} is the high-frequency resistance per unit length of a generic component j. This parameter is evaluated by measuring the resistance at the natural frequency of the cable. For a 30 m cable, there is a natural frequency of about 1 MHz.
- r_j^{lf} is resistance per unit length of a generic component j. This parameter is evaluated by measuring the resistance of the cable at the PWM frequency (order of kHz).
- l_j^{hf} and l_j^{lf} are the inductance per unit length. These two values are equal. These values are evaluated by taking the inductance per unit length at natural frequency of the cable and by multiplying by a factor two. Factor two is needed because at an infinitesimal value of time, which corresponds in Laplace domain to a high-frequency, the two inductance are in parallel. This factor maintains the characteristic impedance and the velocity of propagation equal to the standard model.

The novel transmission line circuit, which models the skin effect, is implemented for the three components and it is illustrated in Fig. 7.14. The parameters of the novel transmission line theory are summarized in Table 7.3.

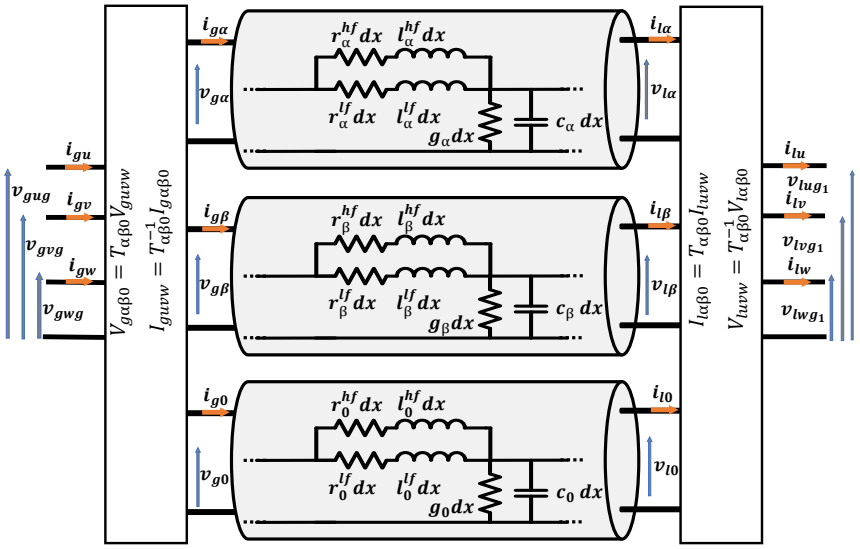


Figure 7.14: Three decoupled transmission lines with the proposed transmission line model.

Table 7.3: Parameters used in the novel simulation.

	r_j^{lf} (mΩ/m)	r_j^{hf} (Ω/m)	l_j^{lf} (μH/m)	l_j^{hf} (μH/m)	c_j (nF/m)	g_j (μS/m)
α	5	0.1571	0.3024	0.3024	0.2273	56.54
β	5	0.1571	0.3024	0.3024	0.2273	56.54
0	18	0.2713	0.5318	0.5318	0.1358	34.68

7.4.5 Simulations vs. experimental results

The parameters identified previously were introduced in a simulation containing the circuital elements illustrated in Fig. 6.20, Fig. 6.21 and Fig. 7.14. From the comparison between the experimental and simulation results, congruence was found, because the model fits well with the high and low frequencies phenomena. In Fig. 7.9, the places where the probes were placed are schematically represented.

In Fig. 7.15, the visible variables are the experimental and simulated common mode current at the inverter side. As can be noticed from the experimental results accordance with the simulations is present. However, there are a few differences between the simulation and experimental results. In fact, it can be observed that the common mode peak current is well estimated, but the natural frequency of the oscillation is not perfectly fitted. This is because the proposed model considers symmetrical cable, while the real one is asymmetrical.

In Fig. 7.16, the selected differential step voltage applied to the system is shown. The represented variables are the voltages and the currents at the input and output

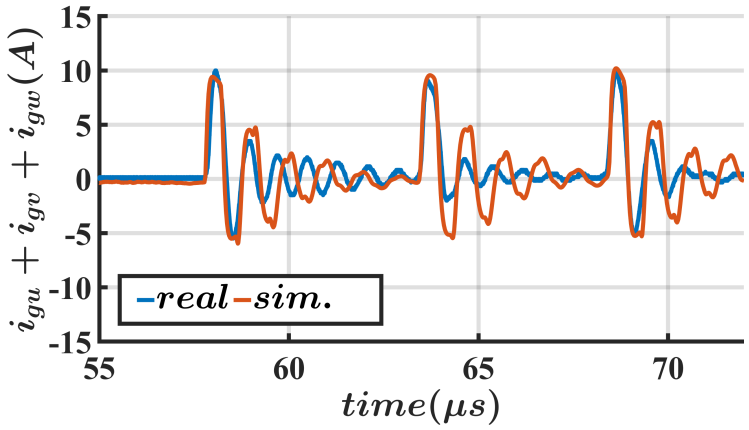


Figure 7.15: Comparison between the proposed simulation and the experimental results: common mode current ($i_{gu} + i_{gv} + i_{gw}$).

of the cable. These variables were sampled at the same time. As can be noticed from this figure, congruence between experimental and simulation results is present. The model estimates well the load peak voltage and the inverter overcurrent. However, the difference between simulation and experimental results can be noticed in Fig. 7.16(a). In fact, from measurement, a voltage oscillation can be seen when the inverter changes from the state (1,1,1) to the state (1,1,-1). This is again caused by the cable asymmetry.

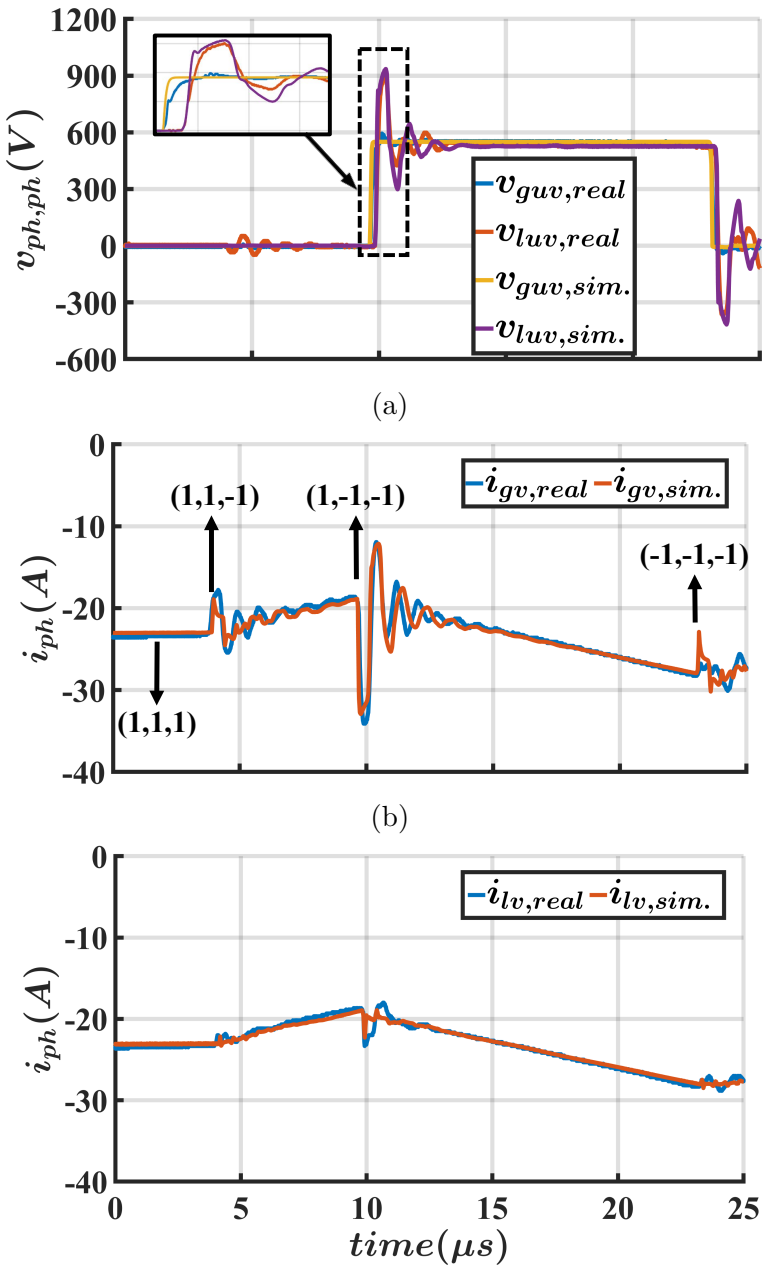


Figure 7.16: Comparison between the proposed simulation and the experimental results. (a) Input and output line voltages. (b) Inverter phase currents. (c) Motor phase currents.

7.5 Conclusions

In Chapter 6, it has been observed that in electric drive the motor overvoltage should be studied by applying the Clarke transformation to all its electrical variables.

In this chapter, a novel measurement methodology, that permits to identify the parameters of the drive, which can be used in motor overvoltage analysis, is proposed. The coordinate transformation has been applied to all the electrical variables of the drive. By using the transformed variables, it was possible to identify the drive parameters. The described method has been experimentally validated during a filter process design by showing its accuracy [89]. The current weakness of the proposed method is that for short cables (e.g. around 2 m) the propagation delay becomes difficult to be measured by the oscilloscope (e.g. presence of skew). Therefore, the conventional measurement method such as the use of LCR meter can be applied.

In the second place, parameters of an experimental setup were measured. These parameters were introduced in the equivalent drive model defined in Chapter 6. PSpice simulations were conducted and the sequent criticalities were found when the simulations were compared with the experimental results.

- Experimental motor overvoltage is in accordance with simulation results when parameters measured at the natural frequency of the cable are used. However, experimental inverter current is totally in disagreement with the simulation.

- Experimental inverter current is in accordance with simulation results when parameters measured at a lower frequency (near the converter switching frequency) than the natural frequency of the cable is used. However, experimental motor overvoltage is totally in disagreement with the simulation.

It has been discovered that this issue is caused by the cable skin effect. A new elementary component of the transmission line, which considers high and low frequencies behavior, has been developed. Thence, the drive circuit was modified and simulated. Good matching between experimental and simulation results has been found.

By virtue of the experience acquired during my Ph.D. period, I have observed that in the filter design process, at first approximation the standard model is very valid (see Chapter 6). In fact, by using this model is possible to derive very precise filter design formulae. Anyway, the novel model proposed in this chapter can be used for second approximation studies where for example the peak current of the filter inductor or power losses of the filter are required.

Chapter 8

RL filter for motor overvoltage mitigation

Part of the work described in this chapter has been previously published in [89]

8.1 Introduction

In Chapter 6, the equivalent model of an electric drive has been presented with the aim to study the motor overvoltage phenomenon. Drive parameters required by the equivalent drive model can be obtained by applying the methodology proposed in Chapter 7. By using the model, solutions to this issue can be studied and designed.

In this chapter, a literature review, of most of the existing filters used for motor overvoltage mitigation task, is provided. Among all the filter topologies proposed in the past, the RL filter at the inverter side has been selected and studied because it is the most suitable option for industrial applications.

An RL filter was designed for an existing drive in order to reduce the motor overvoltage. Different tests were conducted using the power converter designed in Chapter 3. The proposed converter was connected to the electric drive. Filter performances comparisons between inverter based on all-Si, Si-SiC and all-SiC were conducted. However, using the filter with the all-SiC inverter, a detrimental effect in the overvoltage mitigation task was discovered. From PSpice simulations, it was noticed that the combination of filter resistor parasitic inductance and high-speed devices causes unpredicted high-frequency motor over-voltages. This problem was not predicted in the past by the formulae. Therefore, in this chapter new RL filter design formulae are proposed and experimentally validated. Adopting the new formulae, it was observed that the best filter resistance is not equal to the characteristic impedance of the cable. A design guideline that considers the suppression task degradation of the filter is proposed.

In conclusion, a compensation circuit used for mitigating the resistor parasitic inductance issue when high-speed inverters are used is proposed.

8.2 Filters for motor overvoltage mitigation

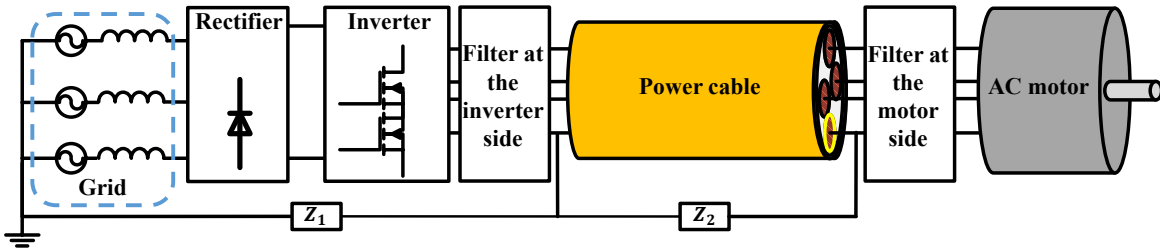


Figure 8.1: Schematic representation of an electric drive and standard location of the overvoltage filters.

Filters for motor overvoltage mitigation can be placed at the beginning and at the end of power cable, as schematically represented in the equivalent drive circuit shown in Fig. 8.1. In this section, the most important filters proposed in the literature are described.

8.2.1 dv/dt filters

These filters are composed of multiple reactive components. The aim of these filters is to increase the voltage rise time imposed at the cable input.

dv/dt filters

These filters are specifically designed for reducing the dv/dt imposed by the inverter to the load, in fact, the rise and fall times imposed on the cable and motor are increased [63, 66, 67, 79, 114, 115, 116, 117]. By considering Fig. 8.1, these filters are usually placed at the inverter side. By reducing the dv/dt, all the problems described in Chapter 5 could be avoided, in particular, the common standards regarding the peak and rise time voltage applied to the motor can be respected [118]. In addition, in case that the filter is well designed, by considering the cable critical length, the overvoltage present at the motor terminals can be mitigated.

These filters are composed of inductive and capacitive elements, thus permitting to implement a low pass filter. The cut-off frequency of the filter is usually higher than the fundamental electrical frequency applied to the motor and higher than the switching frequency. To avoid problems introduced by filter resonances, resistances could be added in order to damp the filter resonance [119, 120].

The drawbacks presented by these filters are listed below.

- These filters are not compact as the impedance matching filters.
- Control scheme should be modified because the current is drained by the filter capacitors.
- Losses of the drive are increased.

Sine wave filters

These filters are specifically designed with the aim to filter all the PWM harmonics, thus, obtaining a sinusoidal waveform at the output terminals of the filters [115, 120, 121]. By considering Fig. 8.1, these filters are usually placed at the inverter side. By virtue of having a good filtering action, all the problems associated with high dv/dt, described in Chapter 5, are removed. These filters are composed of inductive and capacitive elements, thus permitting to implement a low pass filter. The cut-off frequency of the filter is between the switching frequency and the fundamental frequency. Additional resistors are not mandatory if the filter is well designed.

The drawbacks presented by these filters are listed below.

- These filters are very bulky with respect to all existing filters.
- The control scheme must be modified because a very important current is drained by the filter capacitors.
- Losses of the drive are increased.
- Derating of the filter is required when the switching frequency of the converter is increased.
- Issues can be present when the motor needs to work in full voltage operation. The voltage drop over the line inductor can be important.
- The inverter of the drive needs to be oversized [121]. Capacitors during the start-up process behave as short-circuits. In addition, high reactive power is required by the inverter.

Line filters

Line filters, called also output reactors, are very common in the industrial field because it is the easiest solution [81, 115]. In practice, inductive elements are placed between the inverter and the power cable. The combination of the inductive element with the cable gives the possibility to reduce the dv/dt applied to the motor.

The drawbacks presented by this filter are listed below.

- In case the motor needs to work at full voltage operation, criticalities can be found. The voltage drop over the inductor can be important.
- Underdamped motor overvoltage can be present. Thence, if the residual voltage is present in the next commutation of the inverter the winding motor can be more stressed [81]. Consequently, when inverter with high switching frequency and long cable are combined, dangerous overvoltages can be registered at the load side.

8.2.2 Impedance matching filters

These filters are specifically designed for the motor overvoltage mitigation task. The big advantage presented by these filters is the possibility to have a compact filter instead of other existing filter solutions. However, the dv/dt cannot be reduced, thus issues such as bearing current and bad voltage distribution cannot be removed.

The aim of the filters is to reduce the voltage at the motor terminals by matching the characteristic impedance of the cable. The impedance matching task can be done at the inverter and at the motor sides.

RC filter at the motor side

The impedance matching at the motor side can be conducted by using RC filters [63, 79, 80, 94, 101, 115, 122, 123]. Practically, the resistance value is matched with the cable, while the capacitor permits to decouple the resistors for low-frequency values. Without the capacitor, the line voltage is directly applied to the resistance, thus leading to high power dissipation. This filter can reduce common mode and differential modes overvoltages. An important advantage presented by this solution is that the capacitor does not need to be dimensioned for the line current but for the line voltage, thence becoming suitable for high current applications.

The drawbacks presented by RC filter are listed below.

- The power losses of the drive are higher with respect to other impedance matching filter topologies [124]. In fact, the power loss is proportional to the cable length (the needed capacitor is proportional to the cable length) and to the switching frequency of the converter, thence this solution is not the best for very long cable applications.
- It is difficult to place the filter near the motor terminals. Space and power dissipation issues can be found.

RL filter at the inverter side

The motor overvoltage can be reduced by doing impedance matching at the inverter side. The matching can be conducted by placing a resistor within parallel an inductor between the converter and the cable. The matching task is conducted by the resistor, while the inductor presents a low impedance path for the motor currents. The advantages that can be exploited by using this filter are summarized here.

- The additional losses introduced by this filter are negligible.
- Common mode issues such as common mode overvoltage and common mode currents can be mitigated.
- Line voltage drop introduced by this filter is very low with respect to other filters (e.g. dv/dt, line filters and sine wave filters).

The disadvantage of this filter is that the inductive part needs to be dimensioned by considering the line current of the inverter.

Three varieties of RL filters RL can be found in the literature.

- Standard RL filter [78, 89]: this filter is composed of three standard resistors and three standard inductors.
- RL filter without filter resistors: in this filter, the resistive element is emulated by the iron loss of the inductor, thence permitting to reduce the cost [102, 125, 126].
- Integrated RL filter: in [64] an RL filter has been optimally designed by doing a special design of the inductor magnetic core.

Surge suppression cable

The motor overvoltage can be reduced by doing impedance matching at the load side. A very interesting solution of impedance matching at the load side has been proposed in [112, 127]. In this solution, the cable at the load side is matched with another cable connected in parallel to the load called surge suppression cable. This cable at high-frequency behaves like a resistor with a fixed value, where this value is equal to the characteristic impedance of the surge suppression cable. Another side of the cable is disconnected, thence in order to avoid problems of overvoltages at successive reflections, this cable needs to present a damped behavior. A very important advantage presented by this solution is that no local components are required at the load side, thus avoiding the issue of inserting additional elements in the terminal box of the motor. Furthermore, a power cable which contains the cable surge suppressor can be made, thence eliminating completely the space issue.

8.2.3 Active filters

Using active filters, the energy dissipated into the resistive element of passive filters can be regenerated.

Voltage clamping circuit plus surge suppression cable

A simple overvoltage mitigation solution that mitigates the motor overvoltage, with the possibility to regenerate the energy back, has been proposed in [82, 128]. In this solution, the regenerated energy is sent back to the inverter bus. This filter is composed of a surge suppression cable, a three-phase diode rectifier and RC filter. The advantage presented by this solution is that the diode rectifier is located near the inverter, thus avoiding problems of space and cooling at the motor side [96, 129].

Voltage clamping circuit plus synchronous modulation technique

An overvoltage mitigation solution that relieves the motor overvoltage with the possibility to regenerate it has been proposed in [68]. In this solution, the regenerated energy is sent to the electric motor. The problem associated with this solution is that many components and complexity are introduced in the drive.

Voltage clamping circuit plus dv/dt filter

In [130], the motor overvoltage has been reduced by means of a dv/dt filter plus a three-phase rectifier connected to the bus bar of the inverter. By means of this connection, a part of the extra energy can be taken back by the inverter

8.2.4 Special filters for specific applications

Dual-winding motor overvoltage solution

In [131], an interesting motor overvoltage mitigation technique used for open-end winding AC motor configuration is proposed. By using this method no additional components are required. Exploiting the presence of two inverters the motor overvoltage can be reduced.

Three-level approach

In [132], the motor overvoltage has been reduced by using a three-level VSI inverter. Thence, by exploiting the presence of an additional level and by controlling correctly this inverter, the overvoltage can be reduced.

Two-level inverter plus dv/dt filter

In [133], the motor overvoltage has been reduced by means of special control techniques plus a dv/dt filter. The dv/dt filter is smaller with respect to the standard dv/dt filter but higher switching losses are presented by the converter.

8.3 Design of RL filter

Between all the existing filter solutions used for motor overvoltage mitigation task the RL filter has been selected. This filter has been chosen, because for an electric drive with low power rating (e.g. 20 kW), it is not bulky. In addition, it is the most valuable option in the industry due to its simplicity.

In [65, 78, 81, 83], formulae design derived without applying the transmission line theory of the RL filter can be found. In [78], an RL filter was designed following the cable natural frequency criterion while ignoring the traveling waves theory. Good correspondence with the experimental data was anyway achieved. In [64], the exact mathematical formulae (transmission line theory) were obtained, considering the traveling wave phenomenon. In this section, the formulae derived by applying the transmission line theory are provided.

8.3.1 RL filter formulae

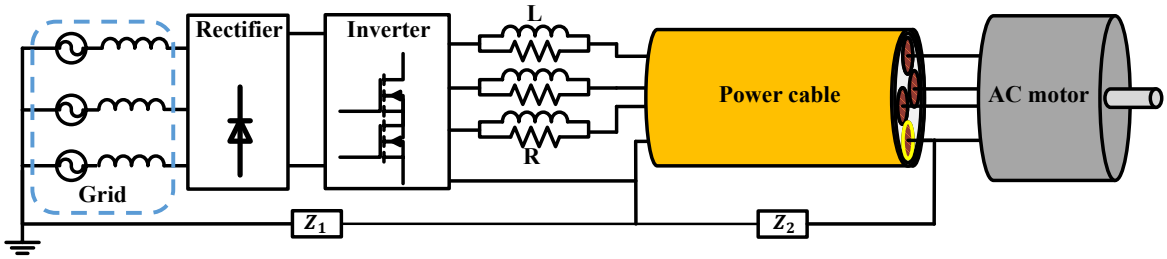


Figure 8.2: Schematic representation of an electric drive with mounted the RL filter.

In the filter design process, the peak load voltage formula as a function of the filter parameters (R and L) is required. During the development of the formulae the following observations are conducted:

- the load peak voltage can be caused by diverse reflected voltages, thus the correct reflection needs to be identified;
- all the equations are obtained using a step voltage generator at the input of the cable, in this way the worst-case scenario is considered.

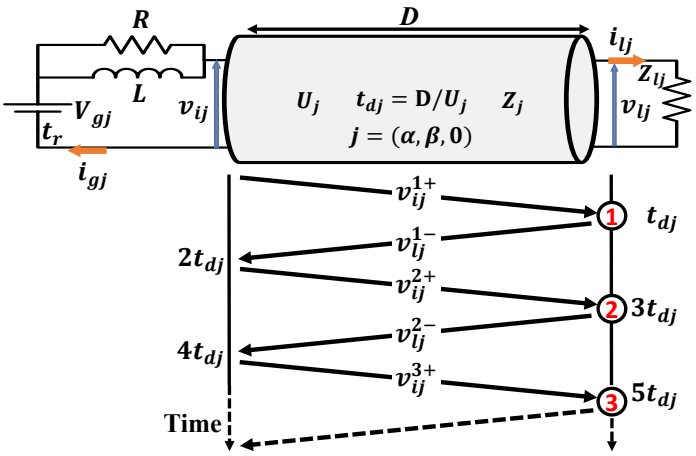


Figure 8.3: α, β and 0 drive model plus RL filter equivalent model and the corresponding Bewley lattice diagram. In red circles, the order of the propagation is indicated.

These formulae were derived from studying the first reflection at the load side (v_{lj}^1), while successive reflections were not analyzed because the best resistance is well known [64]. By considering the drive equivalent model defined in Fig. 8.2, the equivalent circuit obtained by the Clarke transformation of the RL filter is shown in Fig. 8.3. The Laplace load voltage, which considers only the first reflection at the load side is described by:

$$V_{lj(s)} = V_{lj(s)}^{1+} + V_{lj(s)}^{1-} = (1 + \Gamma_{lj}) \frac{V_{gj}\,(R + sL)}{sR\,(s\tau_{gj} + 1)} \tag{8.1}$$

where, the constant time of the filter plus cable, defined as τ_{gj} is:

$$R_{eqj} = \frac{RZ_j}{R + Z_j} \;;\; \tau_{gj} = \frac{L}{R_{eqj}}. \tag{8.2}$$

The time solution of (8.1) can be defined by:

$$v_{lj(t)} = v_{lj(t)}^1 = V_{gj}\,(1+\Gamma_{lj}) \left[1 - \left(\frac{R}{R+Z_j}\right) e^{-\frac{t}{\tau_{gj}}}\right] \tag{8.3}$$

where, the peak load voltage occurs at $2t_{dj}$ and its value is defined by:

$$\widehat{V}_{lj}^1 = v_{lj(2t_{dj})} = V_{gj}\,(1+\Gamma_{lj}) \left[1 - \left(\frac{R}{R+Z_j}\right) e^{-\frac{2t_{dj}}{\tau_{gj}}}\right]. \tag{8.4}$$

As illustrated in Bewley's lattice diagram in Fig. 8.3, $2t_{dj}$ corresponds to the time needed by the voltage to travel from the load to the filter (v_{lj}^{1-}) and back (v_{ij}^{2+}).

It can be demonstrated that, (8.4) shows a decreasing trend of the peak voltage as a function of R. However, the peak voltage decreases till $R{=}Z_j$, in fact, with $R > Z_j$, the peak voltage is registered at the successive reflections. Thence, the minimum peak load voltage is present when $R{=}Z_j$.

8.3.2 Simulations and design guideline

Using (8.4), which gives the value of the peak load voltage caused by the first reflection, and by knowing the cable parameters and the desired peak load voltage ($\widehat{V}^*_{lj}$), it is possible to obtain the filter inductance value

$$L = -\frac{2DR_{eqj}}{U_j \ln(\Phi_j)} \quad ; \quad R \leq Z_j \tag{8.5}$$

$$\Phi_j = \frac{R + Z_j}{R}\left(1 - \frac{\Lambda^*_j}{1 + \Gamma_{lj}}\right) \; ; \; \Lambda^*_j = \frac{\widehat{V}^*_{lj}}{V_{gj}} \tag{8.6}$$

where Λ^*_j is the desired overvoltage factor and Φ_j is defined in (8.6). The filter inductor value derived in (8.5) is minimized when the filter resistance (R) matches the surge impedance of the cable (Z_j) [64, 78].

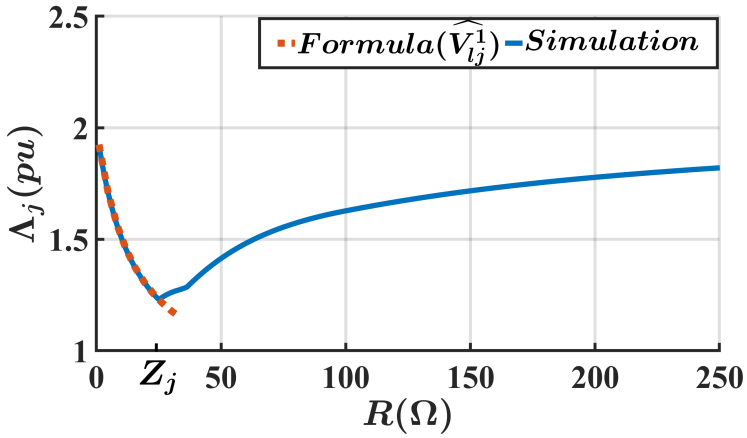


Figure 8.4: Comparison of the resistance sweep using the same filter inductance ($L = 21\ \mu$H) between equation and simulation data ($Z_j = 25\ \Omega$, $t_r = 0$, $\Gamma_{lj} = 1$ and $t_{dj} = 200$ ns). The results are normalized by the generator voltage (V_{gj}).

Parametric sweep analysis of the equivalent circuit (Fig. 8.3) with R variations were conducted. The peak voltage simulation results have been compared with eq. (8.4). The results and the formula have been normalized by V_{gj}, permitting a per unit comparison. The results are shown in Fig. 8.4. It can be seen that (8.4) is in accordance with the simulation results when $R \leq Z_j$. In fact, a formula that predicts the peak load voltage, when $R > Z_j$ (i.e. study of successive reflections), is not required because the voltage is always minimized when $R{=}Z_j$ [64].

8.4 RL filter performance comparison when all-Si, Si-SiC and all-SiC devices are used

An experimental investigation, which compares the filter performances when the converter changes the device configuration between all-Si, Si-SiC and all-SiC, was done. In detail, the experiments focused on the motor overvoltage mitigation task (phase-to-phase motor peak voltage) of the RL filter when the device technology is changed.

8.4.1 Laboratory test bench

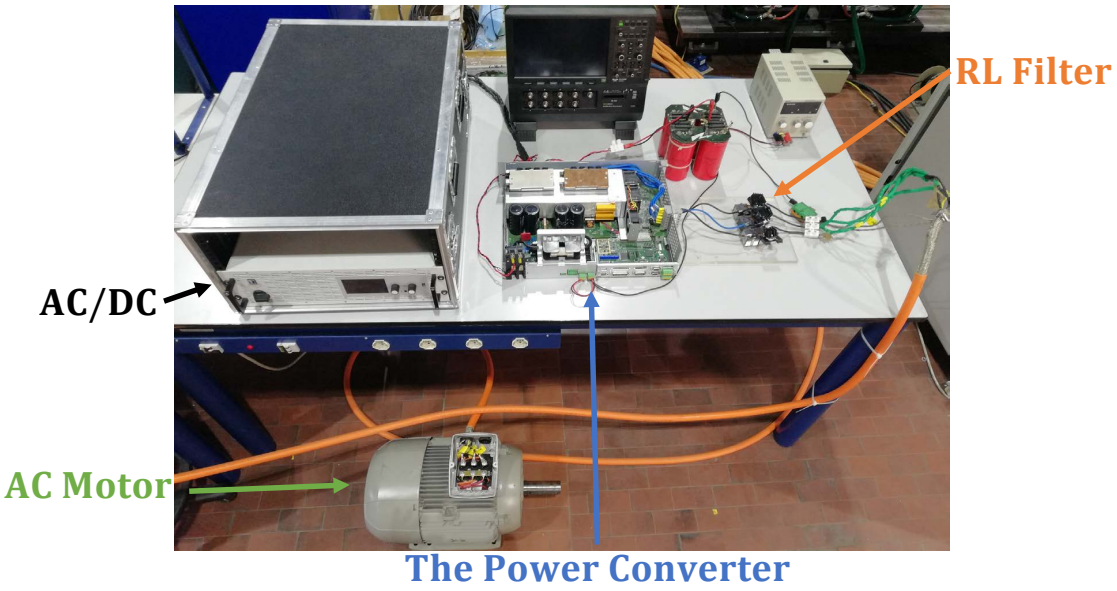


Figure 8.5: The experimental setup: electric drive plus RL filter.

The RL filter was designed for the drive depicted in Fig. 8.5. The details and the descriptions of each component of the electric drive are explained as follows.

- The additional common-mode voltage, introduced by converter attached to the power grid (see Chapter 6), was removed using a unidirectional well insulated AC/DC converter (EA-PSI 91000-30 3U). Thence, only the three-phase inverter common-mode voltage needs to be investigated. The bus voltage (V_{dc}) during the experiments was imposed equal to 600 V by the AC/DC.
- The cable and motor ground were connected to the middle point of two series connected electrolytic capacitors linked to the bus inverter (2 X 3.3 mF 350 V).

This connection permits to emulate the ground connection of a real electric drive (i.e. TN networks).

- The converter described in Chapter 3 was used during the experiment. All-Si inverter, Si-SiC inverter and all-SiC inverter with the same package, PCB layout and mechanical structure were used.
- 35 m of power cable was used (Igus Chainflexd CF27.D PUR servo Cable, (4G+2), (10+1.5)). The cable was unrolled on the laboratory floor in order to obtain a condition similar to the industrial application, thus removing any possibility of proximity effect.
- A squirrel-cage rotor motor (400 V, 15 kW, $cos\varphi = 0.84$), self-ventilated, one poles pair was adopted.
- A set of three ferrite inductors (TH Power Inductors-AGP4233 from Coilcraft), wire wound resistors (HS aluminum housed resistors from Arcol) and anti-inductive resistors (AP101 from Arcol) were used. The connections between these elements were realized using 10 AWG cable (PVC), which has a current rating compatible with the converter (i.e. 30 A).
- An eight channels oscilloscope (MDA805A) with the sequent voltage (HVD3206) and current (CP030) probes were used.

8.4.2 RL filter design

As explained previously, the drive parameters (i.e. characteristic impedances, propagation speeds, and reflection factors at the load side) are required during the RL filter design process. The parameters of the drive were derived by using the methodology proposed in Chapter 7. These values are summarized in Table 8.1.

As can be noticed from the data resumed in Table 8.1, the motor overvoltage phenomenon is always present even if the IGBT technology is used because the condition dictated by the critical length of the cable

$$2t_{dj} < t_r \tag{8.7}$$

is not satisfied with all the components (see Chapter 6.3.3). By virtue of this condition, the overvoltage filter presence is mandatory in order to guarantee good drive reliability.

The filter used for mitigating the motor overvoltage was designed by following the requirements imposed by the motor insulation standards. By knowing the rise time voltage imposed by the inverter is possible to fix the maximum motor voltage [134]. The design process was simplified by limiting the line-to-line motor

Table 8.1: Parameters of the used drive depicted in Fig. 8.5: characteristic impedance (Z_j), propagation time (t_{dj}) and load reflection coefficient (Γ_{lj}).

j	$Z_j(\Omega)$	$t_{dj}(ns)$	Γ_{lj}
α	25.82	205	0.92
β	25.82	205	0.92
0	45	210	0.92

overvoltage and not the phase-to-frame voltage. By virtue of this simplification, only the differential components are involved in the design process (see Chapter 6).

Following the procedure, 23 Ω resistors, with a value near to the cable impedance (25.82 Ω), were identified. The sequent resistors are compatible with the drive voltage and power rating. Subsequently, imposing the line-to-line over-voltage factor (Λ_α) equal to 20 % ($V_{ph,ph}$ = 720 peak when V_{dc} = 600), the required inductance that satisfies the voltage target is equal to 19 μH. This inductance value was calculated by using the formulae defined in Chapter 8.3. Finally, 21 μH ferrite inductors were chosen to sustain the nominal drive current ($\sqrt{2} \cdot 30$ A) plus the over-current commutation of inverter leg, avoiding thus the core saturation.

8.4.3 Experimental comparison and filter issue

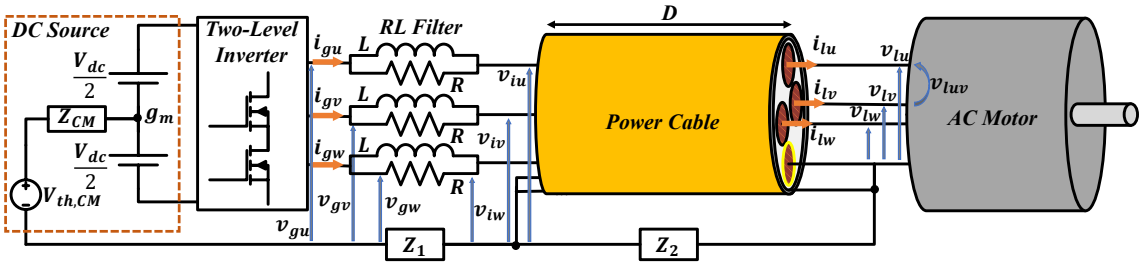


Figure 8.6: Equivalent circuit scheme of the used experimental setup with a detailed representation of the electrical variables of the system. In this scheme, the common mode voltage term, introduced by the power grid, is neglected ($V_{th,CM}$).

RL Filter performance comparisons by using all-Si, Si-SiC and all-SiC devices are here proposed. The same RL filter was used in the same drive and the motor over-voltages were measured. As schematically illustrated in Fig. 8.6, the inverter (v_{guv}) and motor (v_{luv}) terminals voltages were measured.

In Fig. 8.7, the experimental results obtained by changing the three technologies are depicted and the main results are resumed below.

- It can be noticed from the experimental results of both Fig. 8.7(a) and Fig. 8.7(b), no performance variation in the motor overvoltage mitigation

were observed when using all-Si and Si-SiC devices. Furthermore, the motor overvoltage is near the target imposed for the filter.

- When inverter based on all-SiC (Fig. 8.7(c)) is used drawbacks in all the parts of the drive were registered. At the inverter side, even if the filter is present the ringing voltage outlined in Chapter 5 is still present. At the motor side, an unpredictable additional overvoltage was registered. In fact, the peak voltage is equal to 912 V instead of 753 V. This overvoltage can be dangerous for motor insulation.

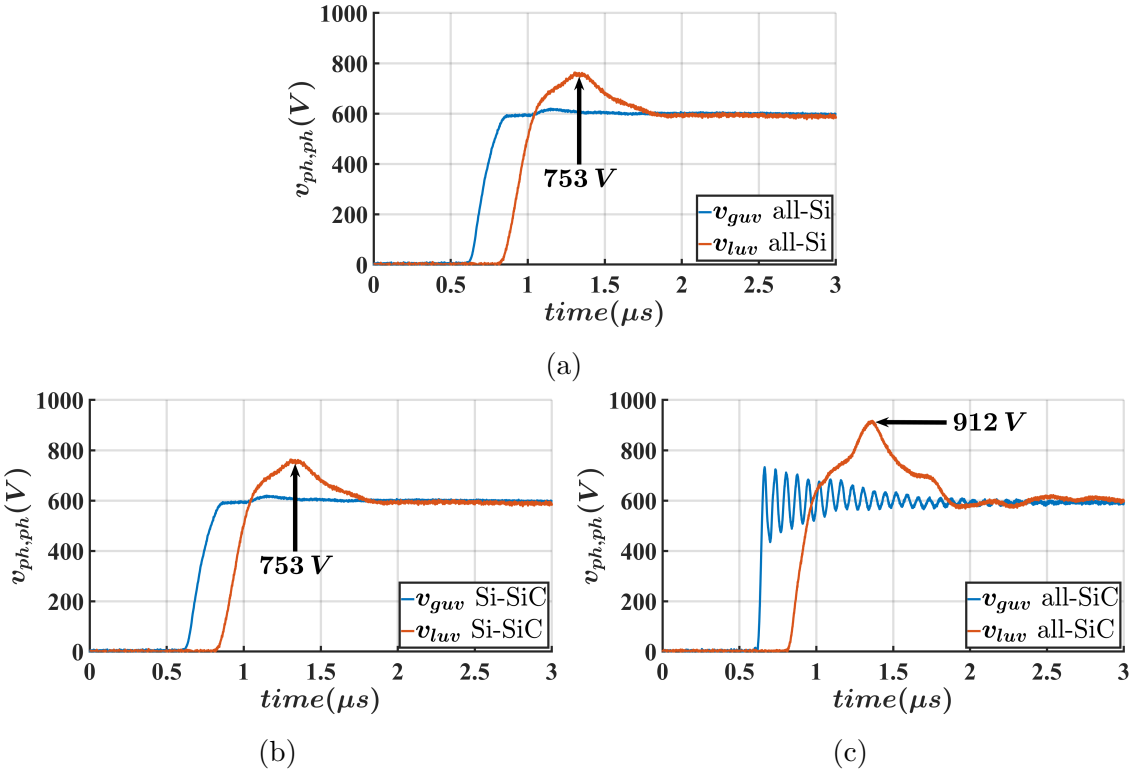


Figure 8.7: Experimental results: line-to-line voltages at the converter and motor terminals when RL filter is adopted. (a) all-Si. (b) Si-SiC. (c) all-SiC.

The emerged problem has been analyzed by comparing the motor overvoltage between Si-SiC and all-SiC. The conducted comparison is shown in Fig. 8.8. The observations drafted about Fig. 8.8 are listed below.

- It can be observed that the same propagation time ($t_{d\alpha}$) in the two experimental results is present, by virtue of using the same drive configuration.
- The voltage rise time (t_r) imposed by the two technologies are extremely different.

- The voltage rise time imposed by all-SiC is so small that voltage ringing is present at the converter terminals (yellow trace).
- An additional voltage at the motor side is present. This issue was registered after many bouncing of the waveform in the transmission line. This phenomenon is not present when the first voltage waveform arrives at the load side, but it was measured later. This evidence suggests that this issue needs to be analyzed by means of transmission line theory.

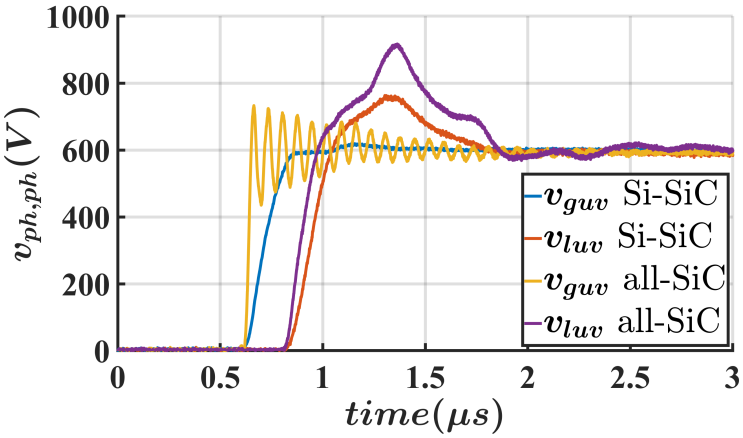


Figure 8.8: Inverter and motor line-to-line voltages comparisons using the same filter ($R = 23\ \Omega, L = 21\ \mu$H) and two inverters: Si-SiC ($tr = 200$ ns) and all-SiC ($tr = 30$ ns).

Table 8.2: Peak line-to-line motor voltage ($V_{ph,ph}$) comparison by changing the switch configuration when RL filter is used ($R = 23\,\Omega, L = 21\,uH$).

	Predicted	*Measured*	Error
all-Si	$732\,V$	$753\,V$	2.9 %
Si-SiC	$732\,V$	$753\,V$	2.9 %
all-SiC	$732\,V$	$912\,V$	25 %

In conclusion, the peak voltages have been collected in order to extrapolate important information valid for the study of this problem. The peak voltages obtained by changing the technologies are compared with the predicted overvoltages that can be evaluated by using the formulae defined in Chapter 8.3.1. The formulae results (i.e. using 23 Ω and 21 μH) and the registered peak voltages are reported in Table 8.2. It can be observed that the classic formulae work perfectly when the all-Si and Si-SiC devices are used, in addition, presenting an error minor than

3 %. Meanwhile, adopting an inverter based on all-SiC device, an important filter performance degradation was reported by presenting with an error of 25 %.

The same power module package, PCB layout, mechanical structure and drive (i.e. including also the same RL filter) were used. By virtue of these features, it is suggested that the cause of this issue is the small voltage rise time imposed by SiC devices (i.e. less than 28 ns). Thence, there is a need for clarification in order to avoid this problem in the future for example in retrofit actions.

8.5 Origin of the issue

Multiple simulations were conducted in order to find the issue origin. A part of the simulations, that have been conducted, are summarized below.

- A capacitive load was introduced instead of a resistive load (e.g. this capacitor could represent the probe parasitic capacitance). Interaction with a very small rise time voltage generator was observed.
- An equivalent resistance at the filter side was introduced in parallel to the filter inductance (see Fig. 8.6). This resistance models the iron loss presented by the iron core of the inductor.
- A capacitance in parallel to the L filter was introduced. This component represents the parasitic capacitance present between the windings.
- An inductance was connected in series to the filter resistor. This element models the resistor parasitic inductance plus the stray inductance present in the interconnection between the resistor and the inductor. The resistor parasitic inductance depends on the resistor technology (e.g. wire wound resistor and anti-inductive resistance) and the inductance range can vary from some tens of nH to few μH.

Between all the analyzed cases, it has been discovered that the resistor parasitic inductance is the origin of this issue. Consequently, from here detailed analyses of the side effects generated by this lumped element are conducted.

8.5.1 Electric drive modeling

By knowing that the resistor parasitic inductance (L_σ) is at the origin of the issue, a new drive equivalent circuit has been derived. In Fig. 8.9, the equivalent circuit, which considers all the components of the drive represented in Fig. 8.6, is depicted. It is worth to mention that L_σ is equal to the resistor parasitic inductance because the transformation coefficient (i.e. when the variables of the system are changed from a three-phase reference to α, β and 0 components) is equal to 1.

PSpice simulations of the circuit represented in Fig. 8.9 were conducted for a generic component (j) extending the validity of the results for all the components (α, β and 0). In this circuit, the R represents the filter resistor, L_σ represents the resistor parasitic inductance and the L the filter inductance.

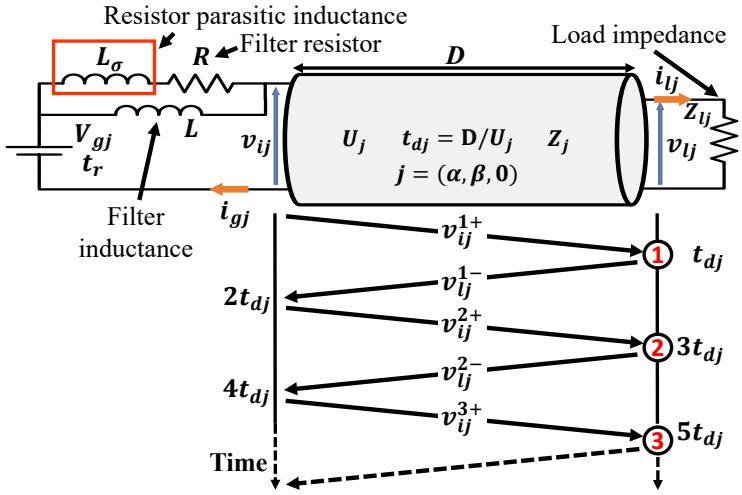


Figure 8.9: α, β and 0 drive model plus RL filter equivalent model and the corresponding Bewley lattice diagram. In red circles, the order of the propagation is indicated.

8.5.2 Resistor parasitic inductance effect

Analysis type: time domain transient

Simulations were conducted by varying the filter resistor value. The simulations were conducted by using a step voltage generator, in this way the worst-case scenario was considered. The load voltage has been acquired and normalized with respect to the input voltage generator (V_{gj}). The equivalent circuit (see Fig. 8.9) with three different resistance values were simulated with and without the resistor parasitic inductance (L_σ).

The simulation results are shown in Fig. 8.10(a), have been conducted by imposing the filter resistance (R) equal to the characteristic impedance (Z_i). Thence, in accordance with the theory explained in Chapter 8.3 the filter optimal design point is satisfied. In fact, the minimum peak load voltage is achieved when the filter resistance is equal to the characteristic impedance of the cable. It can be noticed from this figure when L_σ is not negligible, voltage spikes are present at the load (red trace). Thus, the overvoltage mitigation task has worsened. The voltage spike is superimposed on the voltage trend without the L_σ (yellow trace) and it is caused by a high-frequency mismatching present at the generator side, therefore

these voltages are present from the second load reflections. In fact, at a time "0", the filter inductance (L) and the parasitic element L_σ can be considered an open circuit, thus the reflecting factor condition $\Gamma_{gj} = 0$ is not guaranteed.

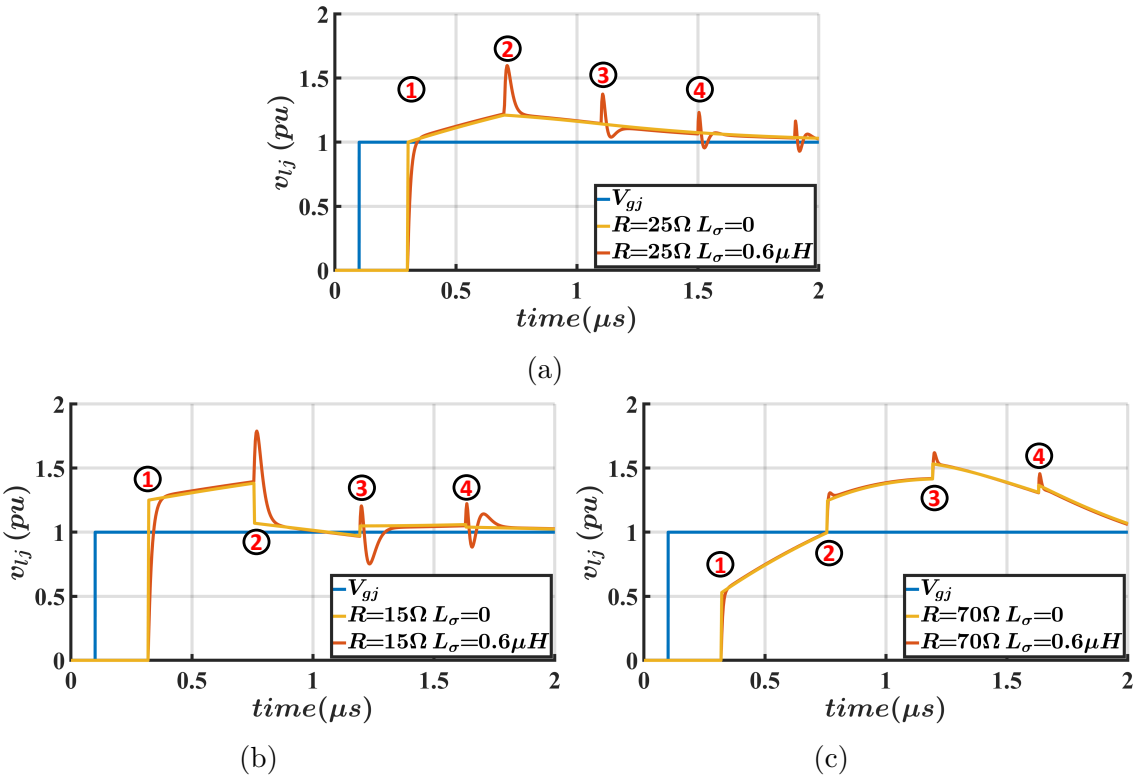


Figure 8.10: Simulations results fixing the filter inductance value: load voltages response to a unit step with and without the resistor parasitic inductance (Z_j = 25 Ω, L = 21 μH, Γ_{lj} = 1, t_{dj} = 200 ns and L_σ = 0.6 μH). (a) filter resistor is equal to the characteristic impedance (Z_j), (b) filter resistor is smaller than the characteristic impedance (Z_j) and, (c) the filter resistor is bigger than the characteristic impedance (Z_j).

As can be noticed from the simulation results depicted in Fig. 8.10(a), Fig. 8.10(b) and Fig. 8.10(c) the peak load voltage can be registered at a different time lapse.

- In Fig. 8.10(a), when the filter is matched with the cable the overvoltage is observed at the second propagation (indicated in the red circle). Therefore, the second reflected voltage at the load side causes the peak overvoltage (V_{lj}^2).
- In Fig. 8.10(b), when the filter presents an impedance minor than the cable impedance, the overvoltage is observed at the second propagation (indicated in the red circle). Consequently, the second reflected voltage at the load side causes the peak overvoltage (V_{lj}^2).

- In Fig. 8.10(c), when the filter presents an impedance major than the cable impedance, the overvoltage is observed at the third propagation (indicated in the red circle). Therefore, the third reflected voltage at the load side causes the peak overvoltage (V_{lj}^{3}).

Analysis type: filter resistance sweep

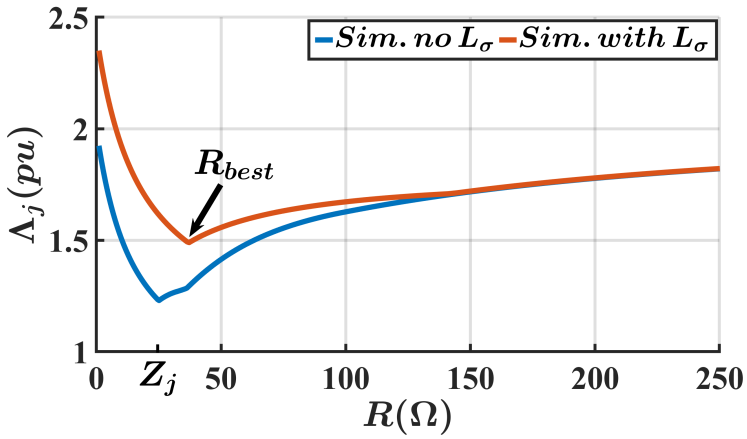


Figure 8.11: Simulation results: overvoltage factors (V_{lj}/V_{gj}) in function of the filter resistance. A comparison between the condition with and without the resistor parasitic inductance ($Z_j = 25\,\Omega$, $L = 21\,\mu H$, $\Gamma_{lj} = 1$ and $t_{dj} = 200\,ns$).

The simulations were conducted by using a step voltage generator, in this way the worst-case scenario was considered. The peak load voltage has been acquired and normalized with respect to the input voltage generator (V_{gj}).

In Fig. 8.11 results of the parametric sweep analysis of the equivalent circuit (Fig. 8.9) with R variations have been conducted by considering or neglecting L_σ, which are depicted. In this figure, all the peak load voltages have been collected. It can be noticed from this figure that an important effect is present at the load side when L_σ is present. In fact, the minimum load peak voltage registered at the load side is 20% higher. In addition, it can be noticed that the resistance value, that minimized the load overvoltage, is not anymore equal to the characteristic impedance of the cable (Z_j).

Other parametric sweep analysis of the equivalent circuit (Fig. 8.9) with R variations have been conducted by changing the resistor parasitic inductance value (L_σ). In these simulations, the filter inductance value was kept the same. The simulation results are depicted in Fig. 8.12 and in Fig. 8.13 an area of the graph has been enlarged. It can be noticed from these figures that at first approximation the peak load voltage, caused by the resistor parasitic inductance, it is independent of its own value. This important result suggests that the peak of the load voltage, once the resistor parasitic inductance cannot be neglected, is roughly constant.

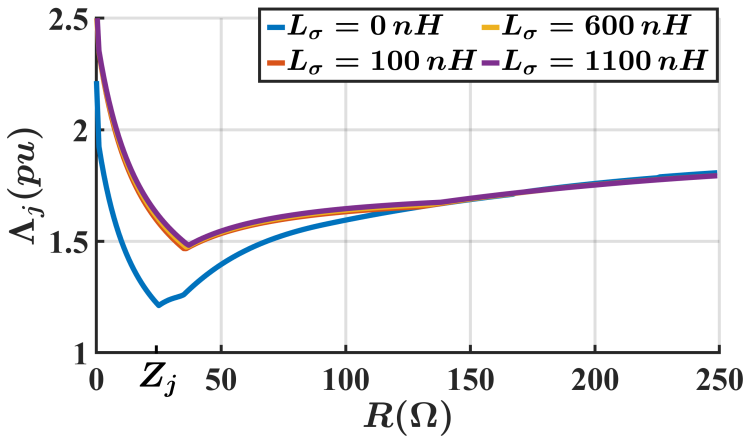


Figure 8.12: Simulation results: overvoltage factors (V_{lj}/V_{gj}) in function of the filter resistance. A comparison between different values of resistor parasitic inductance ($Z_j = 25\,\Omega$, $L = 21\,\mu H$, $\Gamma_{lj} = 1$ and $t_{dj} = 200\,ns$).

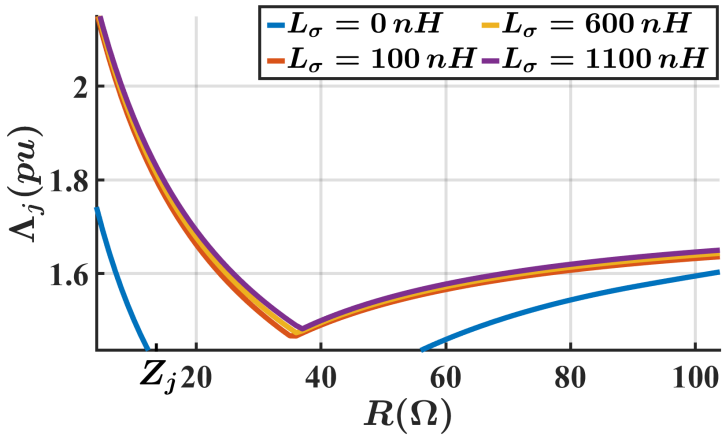


Figure 8.13: The zoomed portion of Fig. 8.12.

The observations derived by the simulations results are summarized below:

1. high-frequency mismatching caused by the resistor parasitic inductance causes the additional overvoltage;

2. the additional high-frequency voltages are present after the second propagation, thence depending on the filter resistor value, the peak load voltage can be registered at different instants.

3. the resistance value, which reduces the load overvoltage, is not equal anymore to the impedance presented by the cable;

4. the peak load voltage, when L_σ is not negligible, is at first approximation

always the same. Accordingly, also with a very small value of resistor parasitic inductance, the additional overvoltage is always present.

This phenomenon has not been observed in the past, thence there is a problem with the point "4" presented in the list. All the simulations have been conducted by considering a step voltage generator, the next step is to see the influence of the voltage rise time (t_r).

8.5.3 Resistor parasitic inductance vs. inverter dv/dt

The resistors always present a parasitic inductance, however, the related extra high-frequency voltages were not considered in the past due to low dv/dt technologies. Simulations with $R \leq Z_j$ were conducted by increasing the generator voltage rise time (t_r).

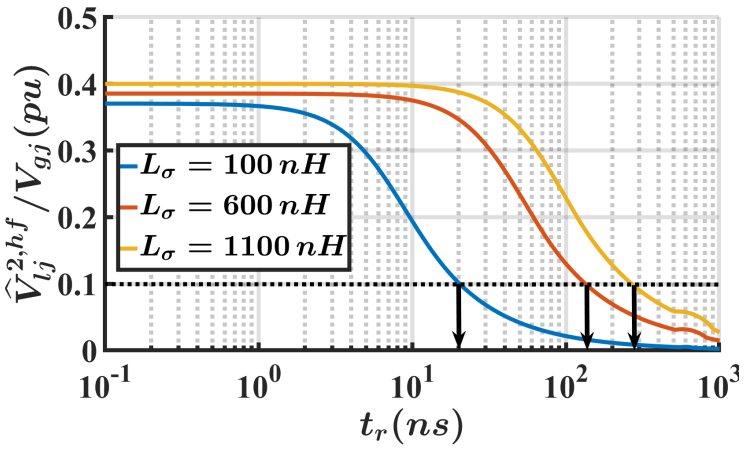


Figure 8.14: Simulation results: additional load voltage caused by L_σ, as a function of the V_{gj} rise time ($R = Z_j = 25\,\Omega$, $L = 21\,\mu H$, $t_{dj} = 200\,ns$ and $\Gamma_{lj} = 1$). The results are in per unit.

In Fig. 8.14, the additional peak voltages ($V_{lj}^{2,hf}$) have been extrapolated by changing the L_σ, as a function of t_r. It can be noticed that large voltage rise time or small parasitic inductance reduces the extra voltage amplitude. From simulation results have been found that $V_{lj}^{2,hf}$ starts to be not relevant when $t_r > 5L_\sigma/R$. This condition corresponds to 5 times the resistor constant time. According to this assumption and using typical drive components values, the extra voltage could be found when $L_\sigma > 40\,\text{nH}$ using SiC, while it could be found when $L_\sigma > 400\,\text{nH}$ using Si.

In conclusion, resistance sweeps considering a generator with a fixed rise time (50 ns) and the resistor parasitic inductance were conducted, as depicted in Fig. 8.15. The peak load voltage has been acquired and normalized with respect to the input

voltage generator (Λ_j). These results have been compared with the data of the resistor sweep done in Fig. 8.11. It can be noticed, that the trace related to a situation where the rise time is different from zero is included between the condition without L_σ and the condition with $t_r = 0$ and with L_σ. This evidence suggests that the overvoltages at the increasing of the rise time move from one condition were the L_σ is important (red trace) to the other one where L_σ can be neglected (blue trace).

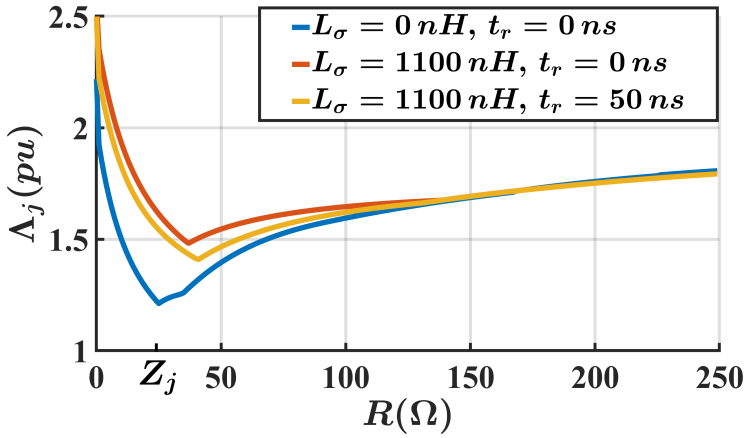


Figure 8.15: Simulation results: overvoltage factors (V_{lj}/V_{gj}) in function of the filter resistance: a comparison between simulation results using different values of voltage rise time and resistor parasitic inductance ($Z_j = 25\ \Omega$, $L = 21\ \mu$H, $\Gamma_{lj} = 1$ and $t_{dj} = 200$ ns).

8.5.4 Important points

The important observations derived by the simulations results are summarized below:

- The voltage rise time imposed by the inverter becomes important because it causes additional high-frequency voltage when the resistor parasitic inductance cannot be neglected.
- The maximum peak load voltage can be registered at a different time lapse.
- The best filter resistance value, which minimized the peak load voltage for the same filter inductance value, is different from the characteristic impedance of the power cable.

8.6 New RL filter design formulae

All RL filter formulae proposed in the past were developed assuming low dv/dt inverter technologies (e.g. BJT, IGBT). The impact of the resistor parasitic inductance has generally escaped scrutiny [64, 78, 83]. Thus, the high dv/dt imposed by SiC and resistor parasitic inductance requires attention during the design phase because of filter deteriorated performance [65, 81]. In case that the phenomenon cannot be avoided, new design formulae are required.

In this section, novel equations based on the resistor parasitic inductance (L_σ) presence have been formulated by extending their validity for each component (α, β and 0). Peak overvoltages caused by the second and the third propagations are derived by permitting the identification of the best resistance value. Furthermore, all the novel formulae are validated through simulations. Finally, the standard formulae have been readopted by considering the resistor parasitic inductance issue.

8.6.1 Formulation hypotheses

The sequent important hypotheses have been considered during the formulae developing.

- Other resistors and inductor parasitic elements are not considered (e.g. the parasitic capacitance present between the inductor coil). In fact, the other parasitic element does not play a key role in the motor overvoltage mitigation task (see Chapter 8.5).
- The formulae are derived by using a step voltage generator ($t_r = 0$), in this way the worst-case scenario is considered.
- The load is considered as a resistance, thence a fixed reflection coefficient is present at the load side (Γ_{lj}).
- The cable length (D) is always major than the critical length presented by the drive (D_{crit}). Major details about the critical length of a cable can be found in Chapter 6.3.3.
- The formulae are derived by splitting the study into high and low-frequency phenomena. The high-frequency phenomenon is associated with the time constant of the resistor parasitic element. The low-frequency phenomenon is associated with the time constant of the RL filter. The formulae derived for the low-frequency phenomenon are indexed using the "lf" superscript, while the equations derived for the high-frequency are indexed using "hf" superscript.
- The high-frequency phenomenon fades faster than the low-frequency phenomenon.

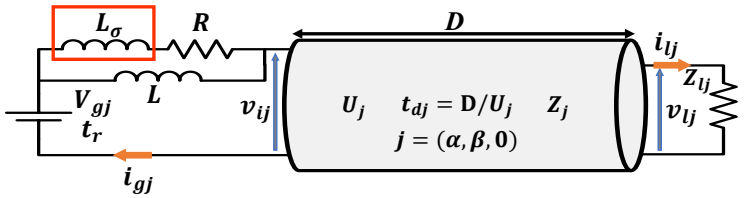


Figure 8.16: Transmission line model using the RL filter.

- The damping time presented by the high-frequency phenomenon is smaller with respect to the propagation delay presented by the cable (t_{dj}).

Useful equations in the study

Considering the circuit shown in Fig. 8.16, reflection factors at the load (Γ_{lj}) and at the input cable (Γ_{ij}) and the voltage divider formulae (G_{1j}) can be defined as follows.

Reflection factor seen by the cable input is defined by:

$$\Gamma_{ij(s)} = \frac{s^2 L L_\sigma + s\left(LR - Z_j\left(L + L_\sigma\right)\right) - Z_j R}{s^2\left(L L_\sigma\right) + s\left(Z_j\left(L + L_\sigma\right) + LR\right) + Z_j R} \tag{8.8}$$

where, R is the filter resistance, L is the filter inductance, L_σ is the resistance parasitic inductance and Z_j is the cable characteristic impedance.

The reflection factor at the load side is defined as follows:

$$\Gamma_{lj} = \frac{Z_{lj} - Z_j}{Z_{lj} + Z_j}. \tag{8.9}$$

The voltage divider effect presented by the RL filter is described in the following equation:

$$G_{1j(s)} = \frac{Z_j\left(s\left(L + L_\sigma\right) + R\right)}{\left(s^2\left(L L_\sigma\right) + s\left(Z_j\left(L + L_\sigma\right) + LR\right) + Z_j R\right)}. \tag{8.10}$$

where, this effect is caused by the voltage that is applied to the filter and the cable.

8.6.2 Low and high frequencies RL filter models

During the formulation, it will be possible to understand that this issue needs to be studied by considering high and low-frequency phenomenon. As a consequence, two circuit models need to be defined.

Low-frequency RL filter model

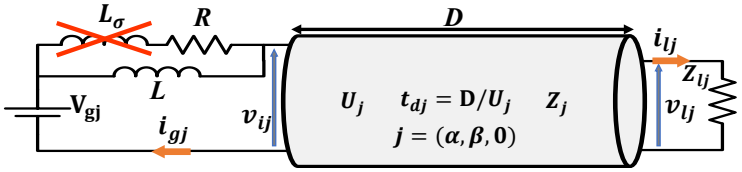


Figure 8.17: The RL filter equivalent low-frequency circuit. The parasitic inductance is considered as a short circuit.

An equivalent low-frequency model can be derived by the circuit shown in Fig. 8.16. The low-frequency equivalent circuit is shown in 8.17. In this circuit, the resistor parasitic inductance is considered as a short-circuit thanks to the premises defined previously. Considering the equivalent circuit, (8.8) and (8.10) need to be reformulated as follows:

$$G^{lf}_{1j(s)} = \frac{(R + sL)}{R(s\tau_{gj} + 1)} \tag{8.11}$$

$$\Gamma^{lf}_{ij(s)} = \frac{(sRL - ZR)}{sL(R + Z) + RZ}. \tag{8.12}$$

High-frequency RL filter model

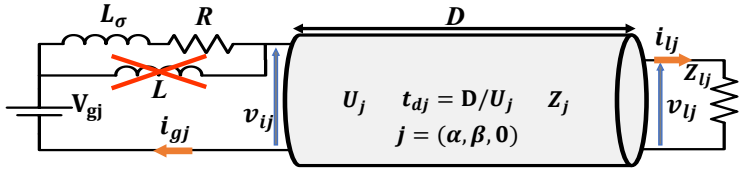


Figure 8.18: The RL filter equivalent high-frequency circuit. The inductance is considered as an open circuit.

An equivalent high-frequency model can be derived by the circuit shown in Fig. 8.16. The high-frequency equivalent circuit is shown in Fig. 8.18. In this equivalent circuit, the filter inductance is considered as an open circuit. Again, equations need to be reformulated:

$$G^{hf}_{1j(s)} = \frac{Z}{sL_\sigma + R + Z} \tag{8.13}$$

$$\Gamma^{hf}_{ij(s)} = \frac{R - Z_j + sL_\sigma}{R + Z_j + sL_\sigma}. \tag{8.14}$$

8.6.3 Load voltage peak formula caused by the second propagation

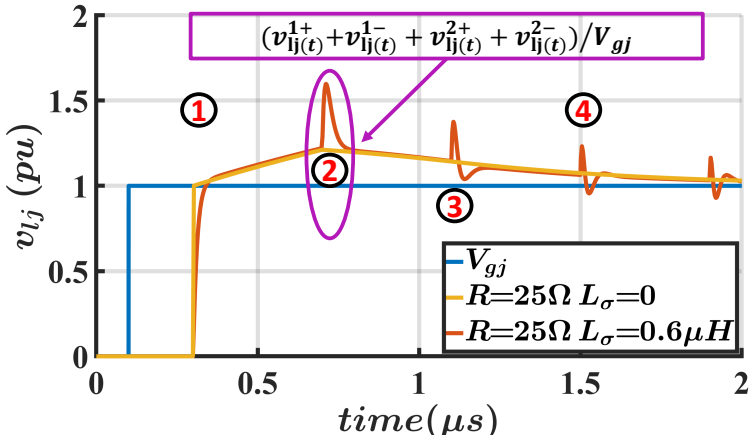


Figure 8.19: Simulations results fixing the filter inductance value: load voltages response to a unit step with and without the resistor parasitic inductance (Z_j = 25 Ω, L = 21 μH, Γ_{lj} = 1 and t_{dj} = 200 ns). The resistor is equal to the line characteristic impedance (Z_j). In detail, the analyzed component is highlighted in purple.

As can be seen from Fig. 8.19, an additional voltage is present at the load side when L_σ is different from zero. In fact, this additional overvoltage causes a detrimental effect on the motor overvoltage mitigation task. In this section, the overvoltage caused by the second reflection at the load side is under investigation. The considered overvoltage is highlighted in the purple circle shown in Fig. 8.19. It can be deduced from this figure that the overvoltage caused by the second propagation is composed of the first and second reflections (i.e. V^1_{lj}, V^2_{lj}). Therefore, a detailed study of the first and second reflected waveforms are required with the aim to find closed formulae of the voltage peak.

The load voltage Laplace transform, that is composed of the first and the second reflection is presented by:

$$V^{1,2}_{lj(s)} = V^{1+}_{lj(s)} + V^{1-}_{lj(s)} + (V^{2+}_{lj(s)} + V^{2-}_{lj(s)})e^{-2t_{dj}s} = V^{1}_{lj(s)} + V^{2}_{lj(s)}e^{-2t_{dj}s} \tag{8.15}$$

where, $e^{-2t_{dj}s}$ introduces the delay imposed by transmission line. The two voltage terms are represented by:

$$V^{1}_{lj(s)} = V^{1+}_{lj(s)} + V^{1-}_{lj(s)} = V^{1+}_{lj(s)}(1+\Gamma_{lj}) = \frac{V_{gj}}{s}G_{1j(s)}(1+\Gamma_{lj}). \tag{8.16}$$

$$V^{2}_{lj(s)} = V^{1}_{lj(s)}\Gamma_{ij(s)}\Gamma_{lj}(1+\Gamma_{lj}) = \frac{V_{gj}}{s}G_{1j(s)}\Gamma_{ij(s)}\Gamma_{lj}(1+\Gamma_{lj}). \tag{8.17}$$

The peak voltage present when the second reflected waveform arrived needs to be evaluated, thence the time solution of (8.15) is required.

Mathematical issues are present when the time solutions of each load voltage terms are required: (8.16) and (8.17). In fact, the mathematical solutions will present a high complexity owing to the high number of poles and zeros. Therefore, the formulae were simplified by splitting the study in high and low-frequency phenomena.

The first reflection voltage evolution is influenced by two reactive parts (i.e. L and L_σ). However, if the constant time of the RL branch (i.e. without the resistor parasitic inductance) is much higher than the constant time introduced by the resistor parasitic inductance (i.e. L_σ/R_j), it is possible to suppose damped the high-frequency phenomenon, thus only the low-frequency phenomenon is considered. By virtue of this assumption, the high-frequency component of $V^1_{lj(s)}$ is already damped out. Meanwhile, the second reflection presents a high-frequency evolution with respect to the first reflection, thus its high-frequency Laplace function transfer is used. In conclusion, the equivalent function can be expressed as:

$$V^{1,2}_{lj(s)} = V^{1,lf}_{lj(s)} + V^{2,hf}_{lj(s)} e^{-2t_{dj}s} \tag{8.18}$$

where, $V^{1,lf}_{lj(s)}$ is the low-frequency term of the first reflection and $V^{2,hf}_{lj(s)}$ the high-frequency term of the second reflected waveform.

The first reflected voltage is defined by:

$$V^{1,lf}_{lj(s)} = V^{1+,lf}_{lj(s)} \left(1+\Gamma_{lj}\right) = \left(1+\Gamma_{lj}\right) \frac{V_{gj}\left(R+sL\right)}{sR\left(s\tau_{gj}+1\right)}. \tag{8.19}$$

The time solution of eq. (8.19) is shown in:

$$v^{1,lf}_{lj(t)} = V_{gj}\left(1+\Gamma_{lj}\right)\left[1-\left(\frac{R}{R+Z_j}\right)e^{-\frac{t}{\tau_{gj}}}\right] \tag{8.20}$$

where, the constant time is determined by:

$$\tau_{gj} = \frac{L}{R_{eqj}}. \tag{8.21}$$

The peak load voltage caused by the first reflection (i.e. which is a part of the maximum voltage applied to the load) when the second waveform arrives at the load side is given by:

$$\widehat{V}^1_{lj} = v^{1,lf}_{lj\left(2t_{dj}\right)} = V_{gj}\left(1+\Gamma_{lj}\right)\left[1-\left(\frac{R}{R+Z_j}\right)e^{-\frac{2t_{dj}}{\tau_{gj}}}\right]. \tag{8.22}$$

The Laplace form of the second reflected waveform is shown below:

$$V^{2,hf}_{lj(s)} = V^{1,hf}_{lj(s)}\Gamma^{hf}_{ij(s)}\Gamma_{lj}\left(1+\Gamma_{lj}\right) = \frac{V_{gj}}{s}\Gamma^{hf}_{ij(s)}G^{hf}_{1j(s)}\Gamma_{lj}\left(\Gamma_{lj}+1\right) \tag{8.23}$$

The final form of the Laplace function obtained from (8.23) is shown below

$$V_{lj(s)}^{2,hf} = \Gamma_{lj}\left(1+\Gamma_{lj}\right)\frac{V_{gj}}{s}\frac{Z_j\left(L_\sigma s + R - Z_j\right)}{L_\sigma^2\left(s+\tau_{\sigma j}^{-1}\right)^2} \tag{8.24}$$

where, the constant time of the function is defined by:

$$\tau_{\sigma j} = \frac{L_\sigma}{R+Z_j}. \tag{8.25}$$

The time solution of the eq. (8.24) it is represented in:

$$v_{lj(t)}^{2,hf} = \Gamma_{lj}(1+\Gamma_{lj})\frac{V_{gj}}{2\xi_j}\left[K_j\left(1-e^{-\frac{t}{\tau_{\sigma j}}}\right)+\frac{2Z_j}{L_\sigma}te^{-\frac{t}{\tau_{\sigma j}}}\right] \tag{8.26}$$

where, the constant time is defined in (8.25) and the parameters are presented in:

$$\xi_j = \frac{R+Z_j}{2Z_j} \tag{8.27}$$

$$K_j = \frac{R-Z_j}{R+Z_j}. \tag{8.28}$$

By finding the maximum of the high-frequency voltage it is possible to determinate the peak voltage caused by the resistor parasitic inductance. For this purpose, the (8.26) has been derivate with the aim to find the maximum. Results of the mathematical process is described below:

$$\frac{dv_{lj(t)}^{2,hf}}{dt} = 0 \quad ; \quad t = \frac{L_\sigma}{2Z_j}. \tag{8.29}$$

The derivate is equal to zero when the time frame is the one represented in (8.26). Thus, the maximum presented by the high-frequency component is present when the time was equal to $t = L_\sigma/2Z_j$. The obtained value is substituted in (8.26) and the peak voltage is given by:

$$v_{lj(L_\sigma/2Z_j)}^{2,hf} = \widehat{V}_{lj}^{2,hf} = \Gamma_{lj}\left(1+\Gamma_{lj}\right)\frac{V_{gj}}{2\xi_j}\left[K_j\left(1-e^{-\xi_j}\right)+e^{-\xi_j}\right] \tag{8.30}$$

A very important observation can be seen from (8.30). This equation is independent of the resistor parasitic inductance value. This statement is in accordance with the simulation results shown in Fig. 8.12. This suggests that once the resistor parasitic inductance is present, the additional overvoltage is always present and it causes always the same peak.

Finally, the load overvoltage composed of each term is described by:

$$\widehat{V}_{lj}^{1,2} = \widehat{V}_{lj}^{1} + \widehat{V}_{lj}^{2,hf}. \tag{8.31}$$

As can be noticed from this equation, the peak load voltage is independent of the resistor parasitic inductance.

8.6.4 Load voltage peak formula caused by the third propagation

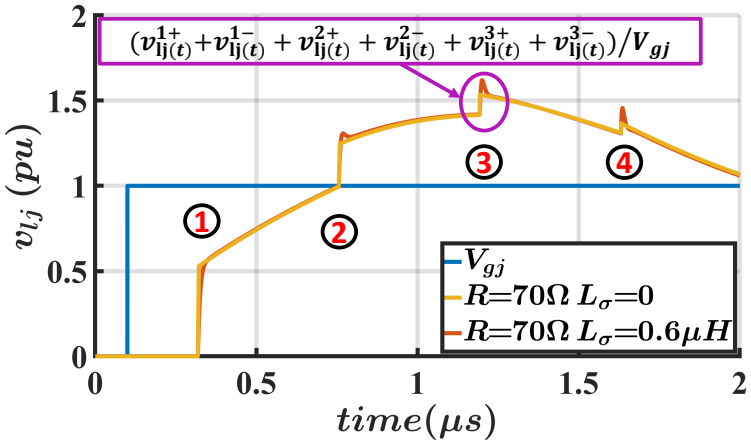


Figure 8.20: Simulations results fixing the filter inductance value: load voltages response to a unit step with and without the resistor parasitic inductance ($Z_j = 25\ \Omega$, $L = 21\ \mu$H, $\Gamma_{lj} = 1$ and $t_{dj} = 200$ ns). Resistor major than the line characteristic impedance (Z_j).

As can be seen from Fig. 8.20, an additional voltage is present at the load side when L_σ cannot be neglected. The overvoltage is highlighted in purple in Fig. 8.20. In fact, this additional overvoltage causes a detrimental effect on the motor overvoltage mitigation task. In this section, the overvoltage present at the load side, which is caused by the third propagation, is put under investigation. It is evident from this figure that the overvoltage caused by the third reflection at the load side is composed of the first, second and third reflected waveforms (i.e. V^1_{lj}, V^2_{lj} and V^3_{lj}). Therefore, a detailed study of the first, second and third propagation voltages are required with the aim to find closed formulae of the voltage peak.

The Laplace form of the load voltage is composed of the first, second and third reflection as presented below:

$$V^{1,2,3}_{lj(s)} = V^1_{lj(s)} + V^2_{lj(s)}e^{-2t_{dj}s} + V^3_{lj(s)}e^{-4t_{dj}s}. \tag{8.32}$$

It can be seen from the equation, that the second and third reflection is multiplied by an exponential function owing to the time shifting. Details of each Laplace function are described below.

- The first reflection voltage ($V^1_{lj(s)}$) closed form has been already defined in (8.16).
- The second reflection voltage ($V^2_{lj(s)}$) closed form has been already defined in (8.17).

- The third reflected waveform Laplace formulae is presented below:

$$V_{lj(s)}^{3} = V_{lj(s)}^{3+} + V_{lj(s)}^{3-} = \frac{V_{gj}}{s} G_{1j(s)} \Gamma_{ij}^{2} \Gamma_{lj}^{2} (\Gamma_{lj} + 1). \tag{8.33}$$

Eq. (8.32) presents the same problem encounter in Chapter 8.6.3. In fact, the Laplace function presents too many poles.

In order to evaluate the peak voltage presented at the third reflection, the time solution of (8.32) is required. The mathematical issue is present when the time solutions of each propagation term is required: (8.16), (8.17) and (8.33). In fact, the mathematical solutions will present a high complexity owing to the high number of poles and zeros. The complexity can be avoided by simplifying the problem by splitting the study into high-frequency and low-frequency domains.

Low-frequency domain solution for the first and second reflection can be used. This condition is satisfied when the time spent by v_{lj}^{1} and v_{lj}^{2} to travel, from the load to filter and back (i.e. $2t_{dj}$ and $4t_{dj}$), is higher than the resistor constant time (i.e. L_{σ}/R_{j}). This assumption permits to say that the high-frequency phenomenon is already damped out. Meanwhile, the third reflection presents its importance in the high-frequency domain. As a consequence, its high-frequency Laplace function transfer is used. By summing up these information, the equivalent function, which described the peak load voltage present at the third propagation, can be described by:

$$V_{lj(s)}^{1,2,3} = V_{lj(s)}^{1,lf} + V_{lj(s)}^{2,lf} e^{-2t_{dj}s} + V_{lj(s)}^{3,hf} e^{-4t_{dj}s}. \tag{8.34}$$

where, $V_{lj(s)}^{1,lf}$ has been already defined in (8.19) with also its time domain solution (8.20).

The low-frequency solution of the second propagation load voltage is presented in:

$$V_{lj(s)}^{2,lf} = V_{lj(s)}^{2+,lf} (1 + \Gamma_{lj}) = \Gamma_{lj} (1 + \Gamma_{lj}) \frac{V_{gj} (R + sL) (s\tau_{gj} - 1)}{sR (s\tau_{gj} + 1)^{2}}. \tag{8.35}$$

where, its time solution is defined by:

$$\begin{aligned} v_{lj}^{2}(t) = v_{lj}^{2+}(t) + v_{lj}^{2-}(t) = \Gamma_{lj} (1 + \Gamma_{lj}) \cdot \\ \cdot V_{gj} \left[-1 + e^{-\frac{t}{\tau_{gj}}} \left(\frac{R^{2} + 3Z_{j}R}{(R + Z_{j})^{2}} + \frac{2Z_{j}R^{3}t}{L (R + Z_{j})^{3}} \right) \right]. \end{aligned} \tag{8.36}$$

The Laplace transfer function of the third reflected waveform is described by:

$$V_{lj(s)}^{3,hf} = \frac{V_{gj}}{s} G_{1j}^{hf} \Gamma_{ij}^{hf} \Gamma_{ij}^{hf} \Gamma_{lj}^{2} (\Gamma_{lj} + 1) \tag{8.37}$$

where, its final form is shown below:

$$V_{lj}^{3,hf} = \frac{V_{gj}}{s} \frac{Z_{j} (L_{\sigma}s + R - Z_{j})^{2} \Gamma_{lj}^{2} (1 + \Gamma_{lj})}{L_{\sigma}^{3} \left(s + \tau_{\sigma j}^{-1} \right)^{3}}. \tag{8.38}$$

The time solution of eq. (8.38) is shown:

$$v_{lj(t)}^{3,hf} = \Gamma_{lj}^2 \left(1+\Gamma_{lj}\right) \frac{V_{gj}}{2\xi_j} \cdot \\ \cdot \left[K_j^2 \left(1-e^{-\frac{t}{\tau_{\sigma j}}}\right) + \frac{2R}{\xi_j L_\sigma} t e^{-\frac{t}{\tau_{\sigma j}}} - \left(\frac{Z_j}{L_\sigma} t\right)^2 e^{-\frac{t}{\tau_{\sigma j}}}\right]. \tag{8.39}$$

The maximum voltage presented by (8.39), it is required. The value time value that cancel the derivate of (8.39) needs to be found. The solution to this problem is described below:

$$\frac{dv_{lj(t)}^{3,hf}}{dt} = 0 \quad ; \quad t_{x_1} = \frac{L_\sigma}{Z_j}\left(1+\frac{1}{\sqrt{(2)}}\right) \simeq 0.3\frac{L_\sigma}{Z_j} \quad ; \quad t_{x_2} = \frac{L_\sigma}{Z_j}\left(1-\frac{1}{\sqrt{(2)}}\right) \tag{8.40}$$

Two solutions are present, only the positive time solution is valid, thence the overvoltage is maximum when $t = 0.3L_\sigma/Z_j$.

Finally, the peak voltage caused by the third reflection is shown in

$$\widehat{V}_{lj}^{1,2,3} = v_{lj}^{1,lf}\left(4t_{dj}\right) + v_{lj}^{2,lf}\left(2t_{dj}\right) + v_{lj}^{3,hf}\left(0.3L_\sigma/Z_j\right). \tag{8.41}$$

As can be noticed from this equation, the peak load voltage is independent of the resistor parasitic inductance.

8.6.5 Formulae validation

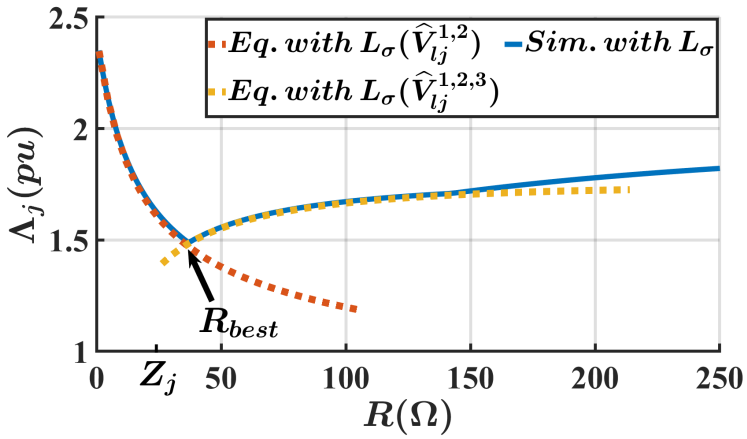


Figure 8.21: Simulation results: overvoltage factors (V_{lj}/V_{gj}) in function of the filter resistance when L_σ is not negligible: a comparison between simulation and formulae results ($Z_j = 25\ \Omega$, $L = 21\ \mu$H, $\Gamma_{lj} = 1$ and $t_{dj} = 200$ ns).

The formulae load peak voltage proposed in (8.31) and (8.41) are validated here through simulation. A per unit analysis is conducted, where the peak voltage has been normalized with respect to the generator voltage.

$$\Lambda_j = \frac{\widehat{V_{lj}}}{V_{gj}} \quad ; \quad j = \alpha, \beta, 0 \tag{8.42}$$

In Fig. 8.21, the comparison between the simulation results and the peak voltage derived by the formulae is done. It can be noticed from the figure the good agreement between the formula and the simulation results with L_σ has been reached when $R > R_{best}$. In addition, it can be noticed that the best resistance value is not anymore equal to the characteristic impedance. From the formulae, the best resistance value which optimizes the filter inductor can be found at the intersection between the voltage caused by the second reflected waveform and the third one as given by (8.31) and (8.41).

8.6.6 Filter design formulae

Using (8.31), and by knowing the cable parameters and the desired peak load voltage (V_{lj}^*), it is possible to obtain the filter inductance value

$$L^\sigma = \frac{-2D(R_{eqj})}{U_j \ln\left(\Phi_j + \Gamma_{lj}\frac{Z_j}{R}\left(K_j\left(1 - e^{-\xi_j}\right) + e^{-\xi_j}\right)\right)} \tag{8.43}$$

where, Λ_j^* is the desired overvoltage factor

$$\Lambda_j^* = \frac{\widehat{V_{lj}}^*}{V_{gj}} \tag{8.44}$$

and Φ_j is given by

$$\Phi_j = \frac{R + Z_j}{R}\left(1 - \frac{\Lambda_j^*}{1 + \Gamma_{lj}}\right). \tag{8.45}$$

L filter design formula with and without the resistor parasitic inductance can be compared as done below

$$\frac{L^\sigma}{L} = \frac{\ln\left(\Phi_j\right)}{\ln\left(\Phi_j + \Gamma_{lj}\frac{Z_j}{R_j}\left(K_j\left(1 - e^{-\xi_j}\right) + e^{-\xi_j}\right)\right)}. \tag{8.46}$$

This equation gives the information about how much will be bigger the filter inductance instead of the standard one. Again, it can be noticed from this equation that the formula is independent of the resistor parasitic inductance value.

8.6.7 The design guideline

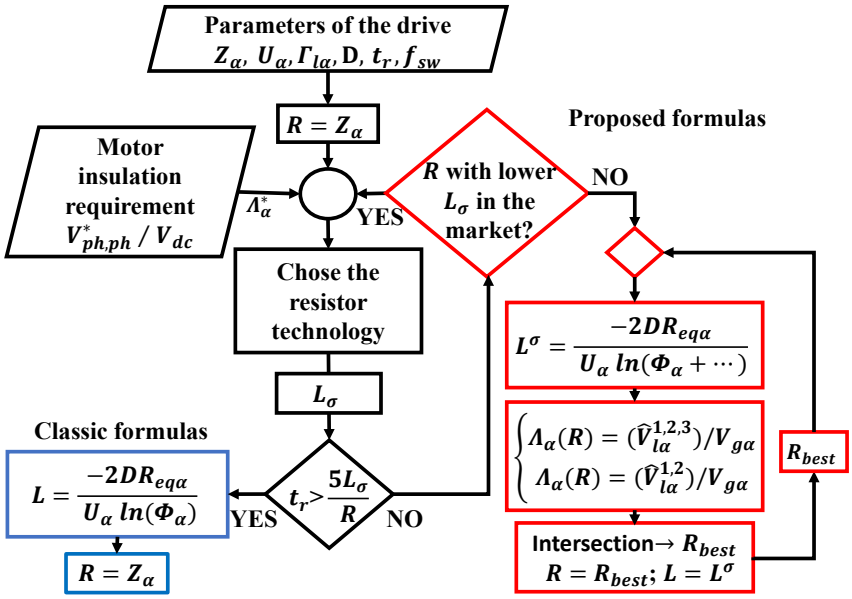


Figure 8.22: Flowchart of the proposed RL filter design guideline.

In this work, the target of the RL filter is to limit the motor line-to-line voltage ($V^*_{ph,ph}$). As described in Section 8.3, only the α and β components are involved in the design process, thus only α component has been chosen in this study having considered a symmetrical cable.

In Fig. 8.22, the RL filter design flowchart, that permits to choose the R and L values using classic and proposed formulae, is shown and described below. The desired $V^*_{ph,ph}$ is normalized by the bus voltage (V_{dc}) obtaining the defined overvoltage factor (i.e. Λ^*_j where j=α). Cable parameters (i.e. Z_α, U_α) can be measured or estimated using the methods proposed in the literature [62, 67, 78, 79]. The inverter voltage rise time (t_r) and the load reflection factor ($\Gamma_{l\alpha}$) can be evaluated from the experimental setup (i.e. when the RL filter is not mounted). Using the drive parameters and the switching frequency, it is possible to calculate the maximum power dissipation of the filter resistor (R)[135]. By knowing the power consumption and voltage rating of the filter resistor, it is possible to choose the resistor technology and then the order of magnitude of L_σ can be identified. At first approximation, the filter resistance (R) is equal to the cable characteristic impedance (Z_α), thus L_σ importance can be determined using the condition derived in Chapter 8.5.3. The correlation between L_σ, R and t_r define the high-frequency mismatching presence. Whenever the high-frequency mismatching is neglected (i.e. YES in Fig. 8.22), the standard formula (8.5) can be used and the best resistance is equal to Z_α. Nevertheless, if the high-frequency mismatching begins to be important (i.e.

NO in Fig. 8.22), it is better to choose another filter technology in order to avoid an oversizing of L. Otherwise, if better resistor cannot be used, L can be designed using the proposed formula (8.43). Subsequently, by intersecting (8.31) and (8.41) in function of R, the resistance that minimized the overvoltage can be found.

8.7 The experimental validation

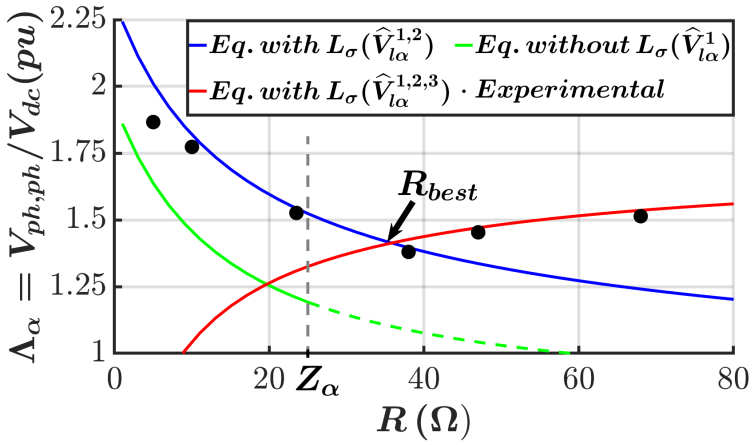
To validate the proposed RL filter formulae and the best filter resistance, the SiC inverter has been adopted. Using the drive parameters derived in Section 7.3, peak load voltages caused by different reflections (eq. (8.22), (8.31) and (8.41)) have been compared with the experimental results. Experiments have been conducted using the same filter inductor (21 μH) and different filter resistor values. In all the tests, the electrical variables have been processed using the Clarke transformation (as done in Chapter 7). Subsequently, overvoltage factors have been collected from α and 0 components.

8.7.1 Formulae validation

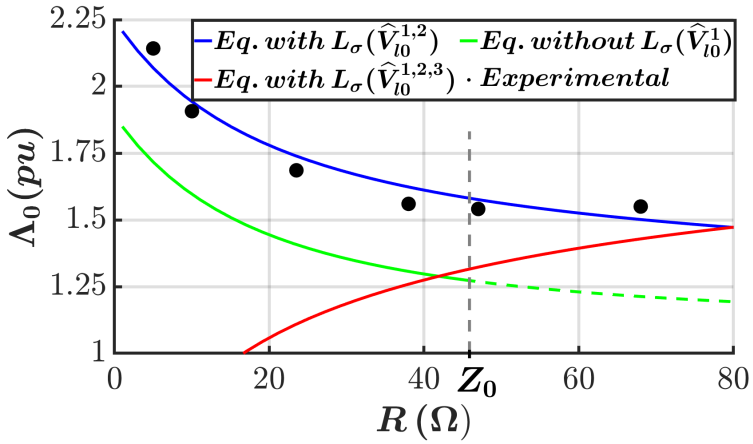
The per unit comparison between the formulae and the experimental results is depicted in Fig. 8.23. For the sake of completeness, comparisons between classic formula (8.22) and the experimental results are provided. As it can be seen from the figures, the experimental overvoltage factors (Λ_α and Λ_0) are not in accordance with the classic formula (green trace), therefore line-to-line motor overvoltage cannot be predicted. The presence of the error is attributed to the inequality proposed by the guideline ($t_r > 5L_\sigma/R$).

Meanwhile, as illustrated in Fig. 8.23, the experimental data are in good agreement with the proposed formulae (i.e. when $L_\sigma \neq 0$), where (8.31) is represented in blue and (8.41) in red. In this way, the $V_{ph,ph}$ motor overvoltage can be well predicted. The accordance is present even if the L_σ between each filter resistor moderately changes ($\pm$200 nH respect to the average value of 800 nH). In fact, the proposed formulae are independent of the L_σ value.

It can be noticed from the comparison that the formulae are piecewise in accordance with the experimental results. In fact, increasing the filter resistance value the overvoltage caused by the third reflection (8.41) overtakes the overvoltage caused by the second reflection (8.31). The optimum filter mitigation task is reached at the crossing of the two formulae. The experimental results in Fig. 8.23(a) show how Λ_α is minimized using a resistor equal to 38 Ω, thus different from Z_α (25.82 Ω). Consequently, using this filter resistance value the line-to-line overvoltage is minimized.



(a)



(b)

Figure 8.23: Experimental results using the same RL filter changing the technology

8.7.2 Second and third load reflected waveforms

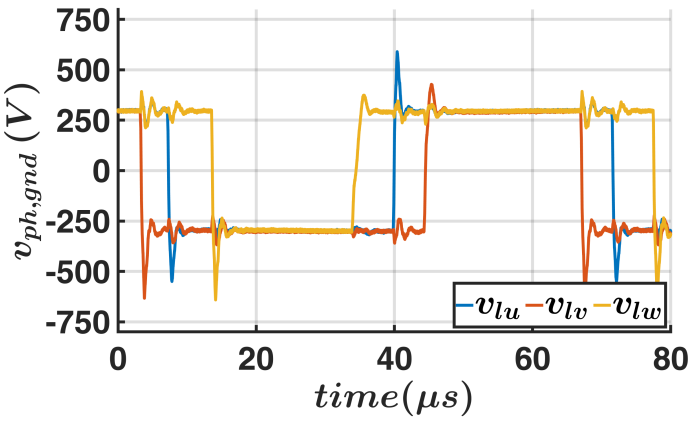
In this section, the individual reflection contributions that were analyzed previously are highlighted. Graphical details, based on experimental data, of the additional overvoltage caused by the second and third reflections are provided.

Traces related to a test done with a filter resistance lower than R_{best} are illustrated in Fig. 8.24 and Fig. 8.25. This condition corresponds to the prevalence of the (8.31) with respect to (8.41). In this test, a line-to-line overvoltage of 915 V has been identified. The zoomed areas of Fig. 8.24(c) and Fig. 8.25(a), show the presence of the high-frequency voltage caused by the high-frequency mismatching ($v_l^{2,hf}$).

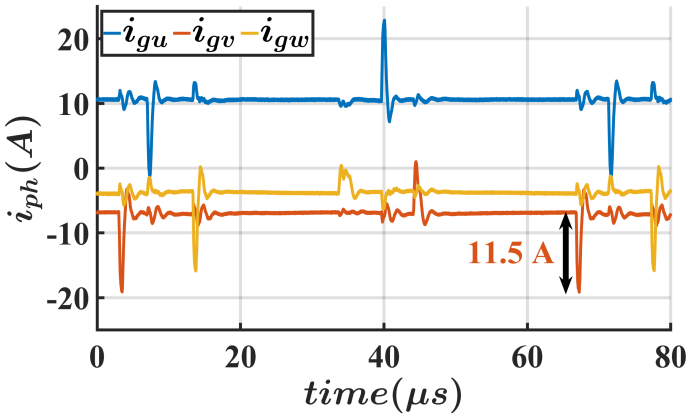
Traces related to a test done with a resistance higher than R_{best} are illustrated in Fig. 8.26 and Fig. 8.27. In this case, the overvoltage is caused by the third reflected

waveform. In this test, a line-to-line overvoltage of 904 V has been measured. The zoomed areas of Fig. 8.26(c) and Fig. 8.27(a), show again the presence of the high-frequency overvoltage caused by the high-frequency mismatching ($v_l^{3,hf}$).

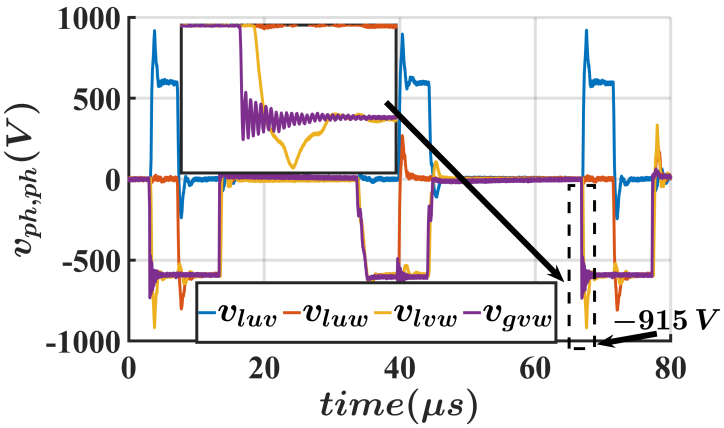
Finally, traces related to a test done with the best resistance are shown in Fig. 8.28(c) and Fig. 8.29(a). A line-to-line overvoltage of 810 V has been measured. Thus, the overvoltage has been reduced by 11% respect the classic condition ($R = Z_\alpha$). In both graphs, in the zoomed area the peaks overvoltages are put in evidence. The presence of two peaks with almost the same value is noticed in these plots, one peak corresponds to the ($V_l^{2,hf}$) and the other corresponds to ($V_l^{3,hf}$).



(a)

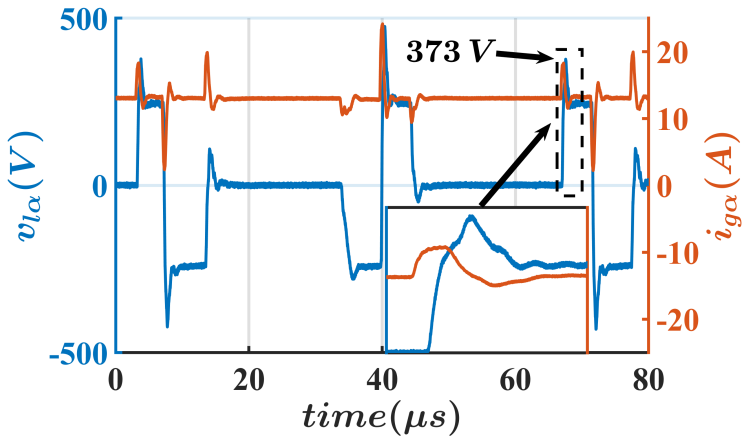


(b)

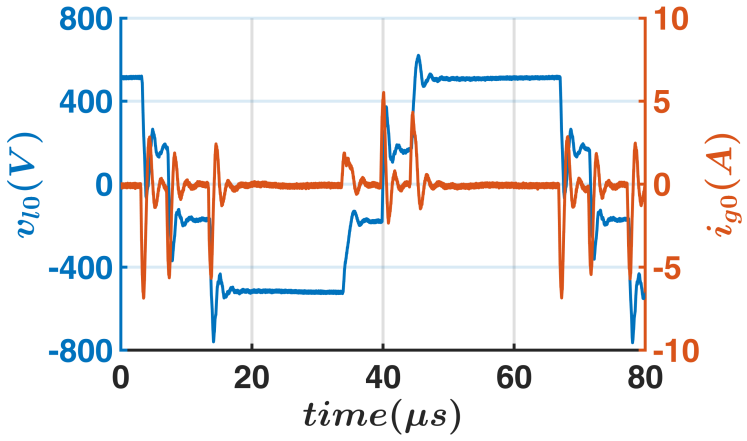


(c)

Figure 8.24: Experiment using SiC based drive with the filter ($R = 23\Omega$, $L = 21\mu$H). (a) Phase-to-frame motor voltages. (b) Inverter currents. (c) Line-to-line motor and inverter voltages.

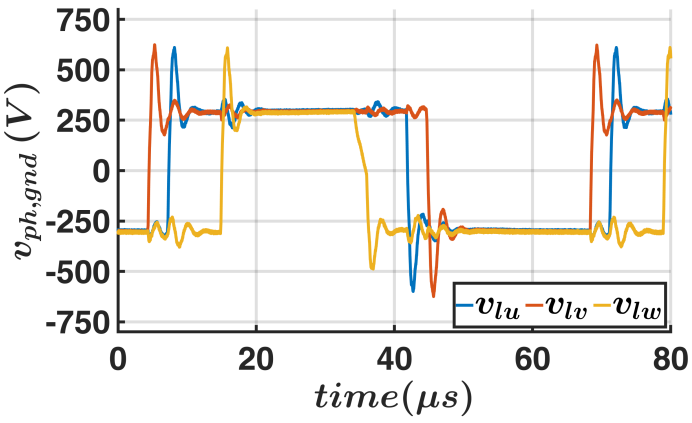


(a)

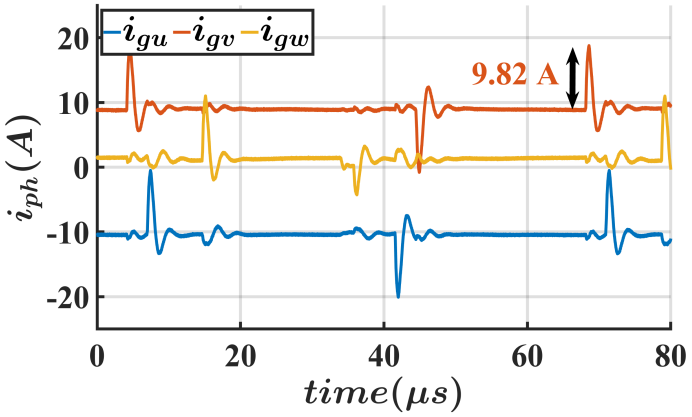


(b)

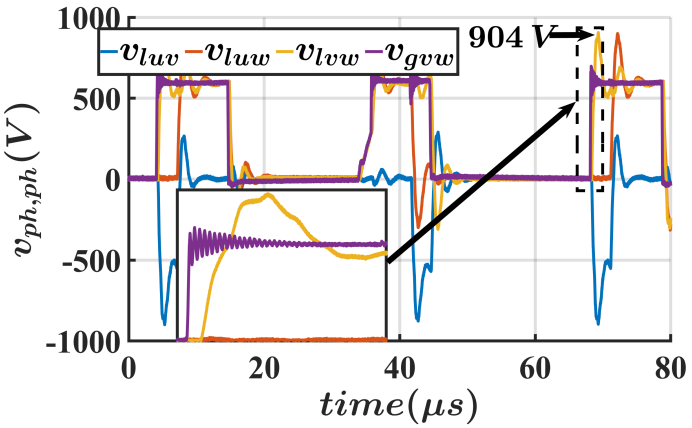
Figure 8.25: Experiment using SiC based drive with the filter ($R=23\Omega$, $L=21\mu$H). (a) Inverter α current and motor α voltage. (b) Inverter 0 current and motor 0 voltage.



(a)

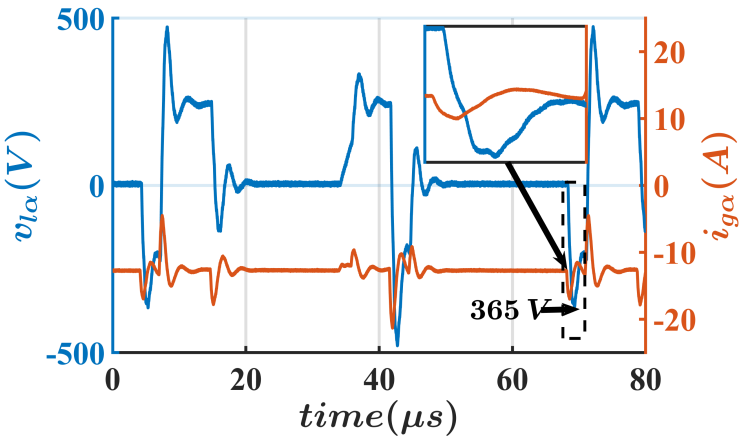


(b)

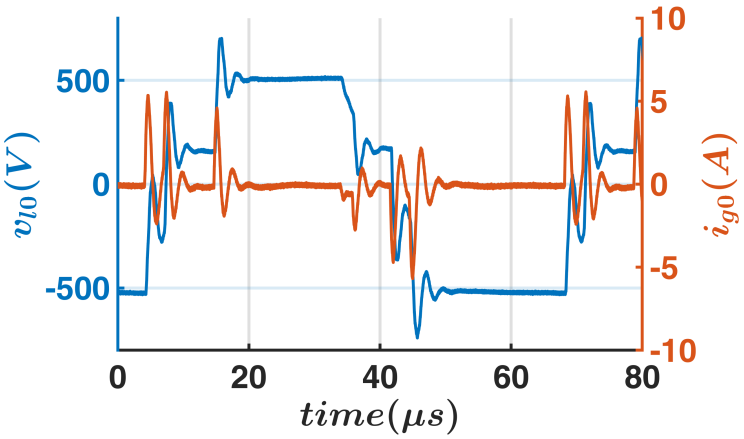


(c)

Figure 8.26: Experiment using SiC based drive with the filter (R=68Ω, L=21μH). (a) Phase-to-frame motor voltages. (b) Inverter currents. (c) Line-to-line motor and inverter voltages.

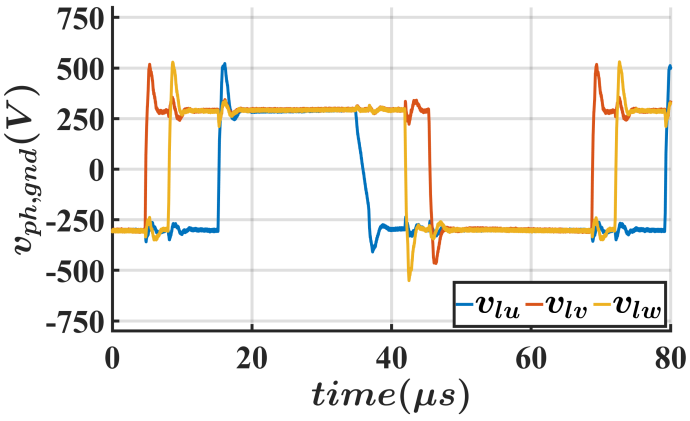


(a)

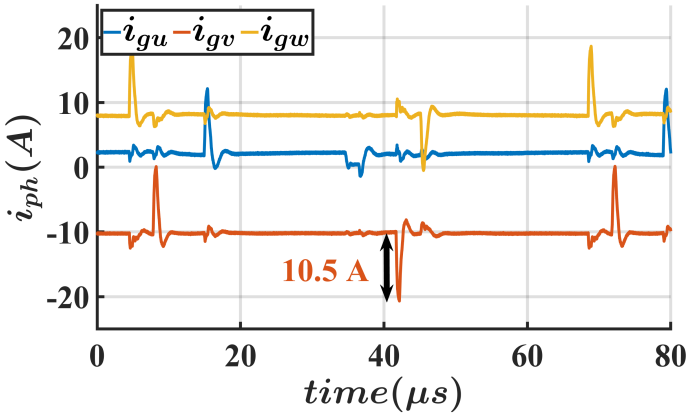


(b)

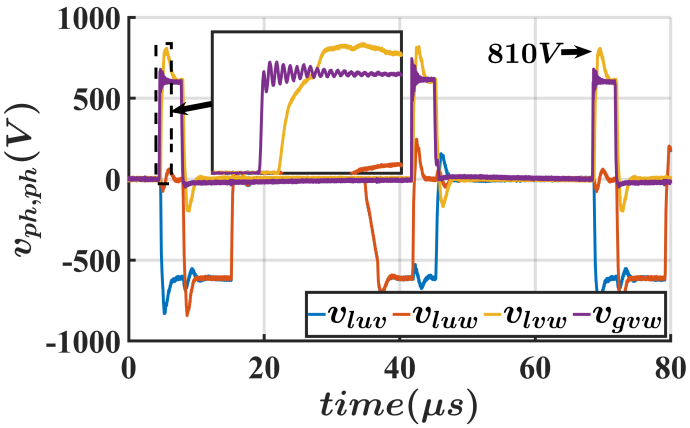
Figure 8.27: Experiment using SiC based drive with the filter ($R=68\Omega$, $L=21\mu$H). (a) Inverter α current and motor α voltage. (b) Inverter 0 current and motor 0 voltage.



(a)

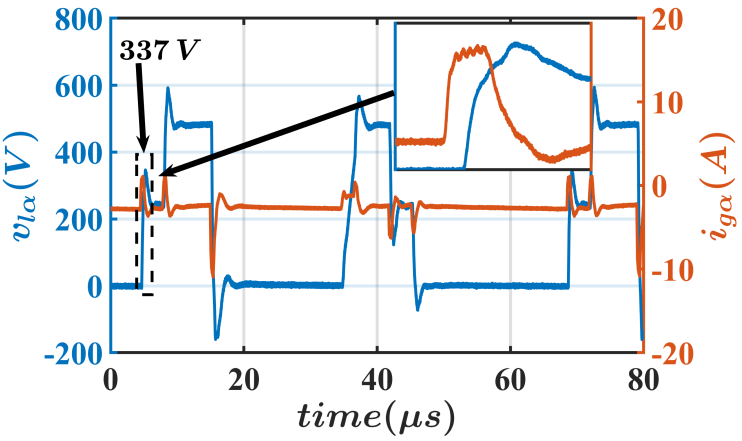


(b)

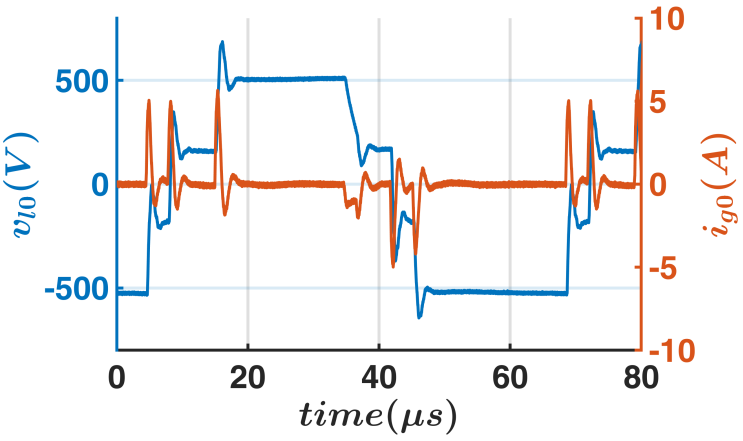


(c)

Figure 8.28: Experiment using SiC drive with the filter ($R = 38\Omega$, $L = 21\mu$H). (a) Phase-to-frame motor voltages. (b) Inverter currents. (c) Line-to-line motor and inverter voltages.



(a)



(b)

Figure 8.29: Experiment using SiC drive with the filter ($R = 38\Omega$, $L = 21\mu$H). (a) Inverter α current and motor α voltage. (b) Inverter 0 current and motor 0 voltage.

8.8 RC/RL filter

A novel compensation circuit used to mitigate the problem of the resistor parasitic inductance, present when high-speed devices are used with the RL filter, is proposed. The three-phase filter with its compensation circuit is presented in Fig. 8.30. With respect to a standard RL filter a branch composed of a resistance (R_c) and a capacitor (C_c) is added in parallel to the RL filter. This solution was found to be the simplest and the most effective among others (e.g. placing only a capacitive element in parallel to the RL filter). The circuit shown in Fig. 8.30 is converted by using the Clarke transformation to the equivalent circuit valid for the α, β and 0 components shown in Fig. 8.31.

The lumped parameters of this equivalent circuit are described as follows:

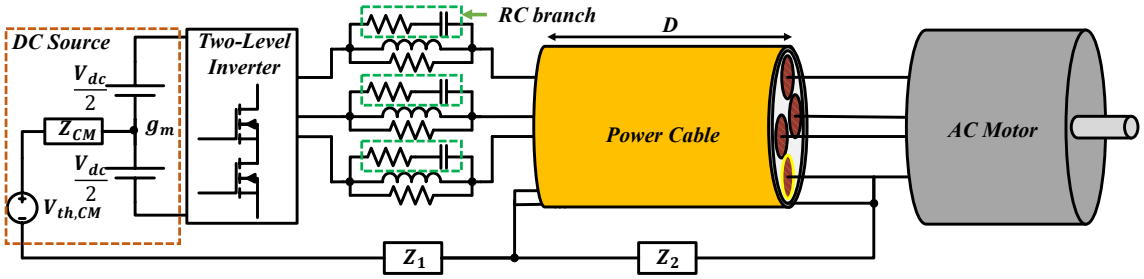


Figure 8.30: Equivalent circuit scheme of the drive with the proposed compensation topology: RL/RC filter.

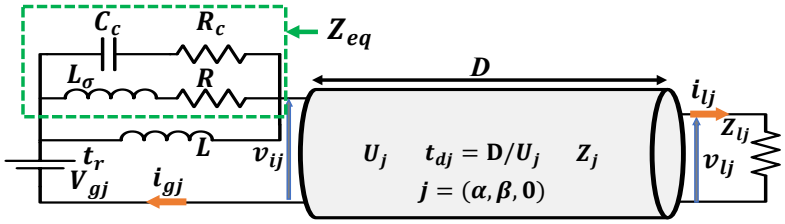


Figure 8.31: Drive model plus RL filter and the RC compensation branch equivalent model.

- R and L represent the element of the RL filter;
- L_σ represents the resistor parasitic inductance;
- R_c and C_c represent the additional compensation branch used for eliminating the resistor parasitic inductance (L_σ).

8.8.1 Theoretical analysis

In this section, the design methodology of the R_c and C_c elements is described. The equivalent impedance of the filter (Z_{eq}) without L, is represented in the equivalent circuit (Fig. 8.31), is defined by:

$$Z_{eq} = \frac{\frac{R_c C_c s + 1}{C_c s} \cdot (R + sL_\sigma)}{\frac{R_c C_c s + 1}{C_c s} + (R + sL_\sigma)} = R \left(\frac{s^2 \frac{R_c}{R} L_\sigma C_c + s\left(\frac{L_\sigma}{R} + R_c C_c\right) + 1}{s^2 L_\sigma C_c + s\left(RC_c + R_c C_c\right) + 1} \right). \quad (8.47)$$

The impedance presents two poles and two zeros that need to be removed. The solution to this problem can be found by imposing:

$$\frac{R_c}{R} L_\sigma C_c = L_\sigma C_c \quad ; \quad \left(\frac{L_\sigma}{R} + R_c C_c\right) = \left(RC_c + R_c C_c\right) \quad (8.48)$$

thence, the compensation circuit can be designed by imposing:

$$R_c = R \quad ; \quad C_c = \frac{L_\sigma}{R^2} \tag{8.49}$$

where, this condition corresponds to have equal constant time for the $R_c - C_c$ and $R - L_\sigma$ branches.

In conclusion, the equivalent impedance seen by the filter inductor, when the compensation circuit is well tuned, is:

$$Z_{eq} = R. \tag{8.50}$$

8.8.2 RC/RL filter PSpice simulations

The circuit shown in Fig. 8.31 was simulated by using PSpice. The results of the simulation are shown in Fig. 8.32 and in Fig. 8.33.

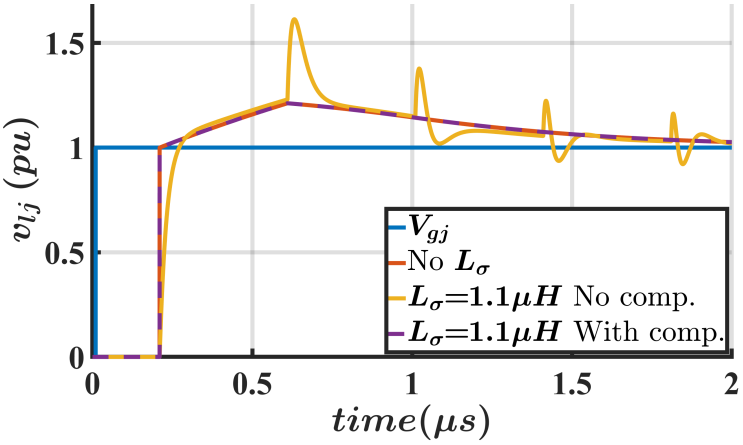


Figure 8.32: Simulations results: load voltage response to a unit step when RL/RC filter is used ($Z_j = 25\ \Omega$, $R = 25\ \Omega$, $L = 21\ \mu$H, $\Gamma_{lj} = 1$ and $t_{dj} = 200$ ns, $R_c = 25\ \Omega$ and $C_c = 1.76$ nF).

In Fig. 8.32, load voltage evolution response to a step voltage generator has been studied for three different circuits:

- RL filter without the presence of the resistor parasitic inductance, as depicted in Fig. 8.3 (red trace);
- RL filter with the presence of the resistor parasitic inductance, as shown in Fig. 8.9 (yellow trace);
- RL filter with the presence of the resistor parasitic inductance and the RC compensation branch, as represented in Fig. 8.31 (purple trace). In this simulation, the R_c and C_c are designed by following the eq. (8.49).

It can be noticed that using the compensation circuit the resistor parasitic inductance side effect is canceled. As a matter of fact, the traces that correspond to the load voltages with the compensation circuit and without the resistor parasitic inductance are equal. These results show that the RC branch is perfectly suited to the elimination of the resistor parasitic inductance.

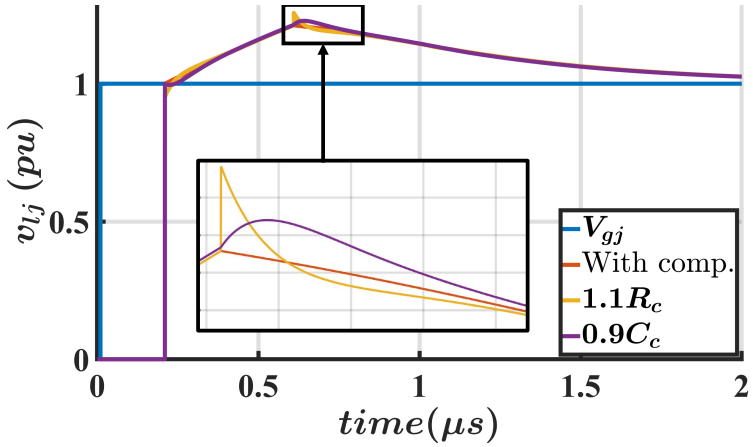


Figure 8.33: Simulations results: load voltage response to a unit step when RL/RC filter is used ($Z_j = 25\ \Omega$, $R = 25\ \Omega$, $L = 21\ \mu$H, $\Gamma_{lj} = 1$ and $t_{dj} = 200$ ns, $R_c = 25\ \Omega$ and $C_c = 1.76$ nF).

In Fig. 8.33, load voltage evolution response to a step voltage generator again has been studied for three different conditions and the results have been compared:

- RL filter with the presence of the resistor parasitic inductance and the RC compensation branch, as represented in Fig. 8.31 (red trace). In this simulation, the R_c and C_c are designed by following the eq. (8.49).
- RL filter with the presence of the resistor parasitic inductance and the RC compensation branch. The R_c value was decreased by 10% with respect to the optimal value (yellow trace).
- RL filter with the presence of the resistor parasitic inductance and the RC compensation branch. The C_c value was decreased by 10% with respect to the optimal value (purple trace).

As can be seen from both the condition where the RC branch has been not optimally designed, the resolution of the problem introduced by the compensation circuit is robust also to the variations of the parameters.

8.8.3 Parameter sensitivity analysis

A parameter sensitivity analysis of the compensation circuit is conducted in this section. Obviously, perfect tuning of the R_c and C_c is impossible to achieve because

electronic components present tolerance.

Thence, side effects, introduced by the parameter deviation presented by the compensation elements, are studied. The performances of the compensate filter are evaluated by using PSpice simulations. The sequent cases are investigated:

- deviation of R_c;
- deviation of C_c;
- parasitic inductance shows up in the $R_c - C_c$ branch.

The additional overvoltage caused by the combination of t_r and L_σ described in Chapter 8.5.3 has been analyzed. In case of perfect compensation, that it is present when (8.49) is respected, $V_{lj}^{2,hf}$ is perfectly canceled. Thence, performance variation owing to a deviation from the optimum filter design is investigated.

R_c parameter deviation

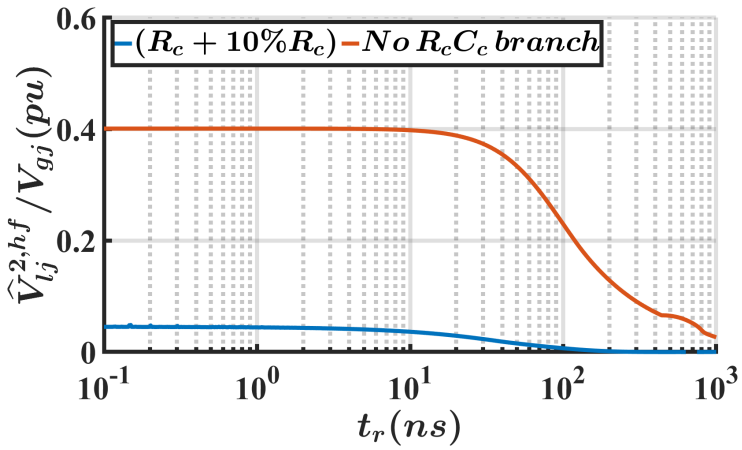


Figure 8.34: Simulation results: additional load voltage caused by L_σ, as a function of the V_{gj} rise time, when R_c is not well tuned ($R = Z_j = R_c = 25\,\Omega$, $L_\sigma = 1.1\,\mu H$, $L = 21\,\mu H$, $t_{dj} = 200\,ns$, $\Gamma_{lj} = 1$, $C_c = L_\sigma / R_c^2$).

A performance comparison with and without the RC branch when R_c deviates from the optimum condition is conducted. The rise time of the voltage generator (t_r) is included in the study. In Fig. 8.34, the simulation results of two different conditions are represented:

- simulation result of the additional load overvoltage without the compensation circuit is depicted in red;

- simulation result of the additional load overvoltage, when the resistance of the compensation circuit differs by 10% from the optimum design point is depicted in blue.

The sequent observations can be done from the experimental results:

- without R_c and C_c important additional overvoltage is always present until the rise time of the voltage generator reaches the critical condition defined in Chapter 8.5.3;
- in case that R_c differs by 10% from the optimum design point, an additional overvoltage of 0.05 pu has been registered, but this value is negligible with respect to the case without the compensation, where 0.4 pu is present.

In conclusion, the simulation results suggest that this compensation branch is robust to the resistance deviation.

C_c parameter deviation

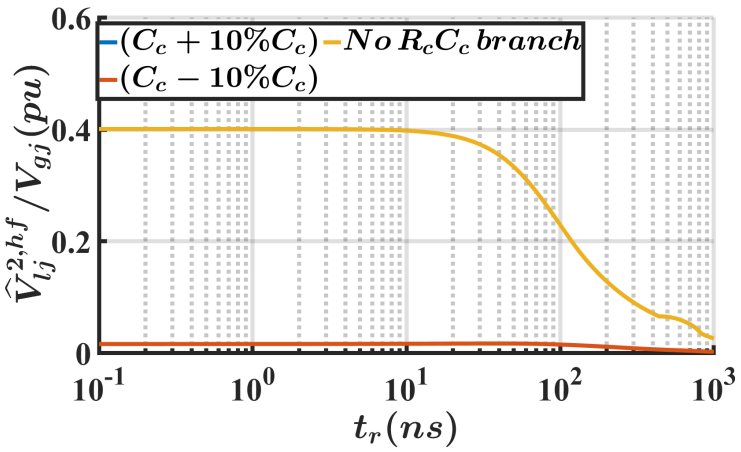


Figure 8.35: Simulation results: additional load voltage caused by L_σ, as a function of the V_{gj} rise time, when C_c is not well tuned ($R = Z_j = R_c = 25\,\Omega$, $L_\sigma = 1.1\,\mu H$, $L = 21\,\mu H$, $t_{dj} = 200\,ns$, $\Gamma_{lj} = 1$, $C_c = L_\sigma/R_c^2$).

A performance comparison with and without the RC branch when C_c deviates from the optimum condition is conducted. The rise time of the voltage generator (t_r) is included in the study. In Fig. 8.35, the simulation results of two different conditions are represented:

- simulation result of the additional load overvoltage without the compensation circuit is depicted in yellow;

- simulation results of the additional load overvoltage, when the capacitance of the compensation circuit differs by ±10% from the optimum design point are respectively depicted in blue and red.

The sequent observations can be done from the experimental results:

- in case that C_c differs by ±10% from the optimum design point, an additional overvoltage of 0.025 pu has been registered, but this value is negligible with respect to the case without the compensation, where 0.4 pu is present.

In conclusion, the simulation results suggest that this compensation branch is robust to the capacitance variation.

Parasitic inductance presented by the series of C_c and R_c

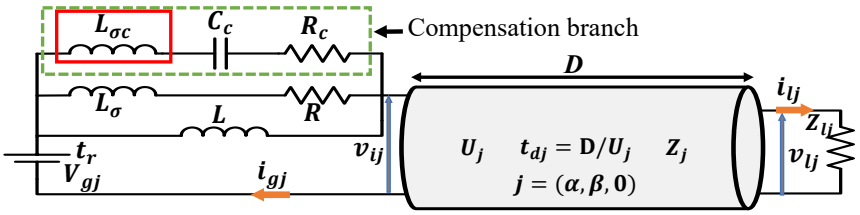


Figure 8.36: α, β and 0 drive model plus RL filter and the RC compensation branch equivalent model. The parasitic inductance presented by the compensation branch is highlighted ($L_{\sigma c}$).

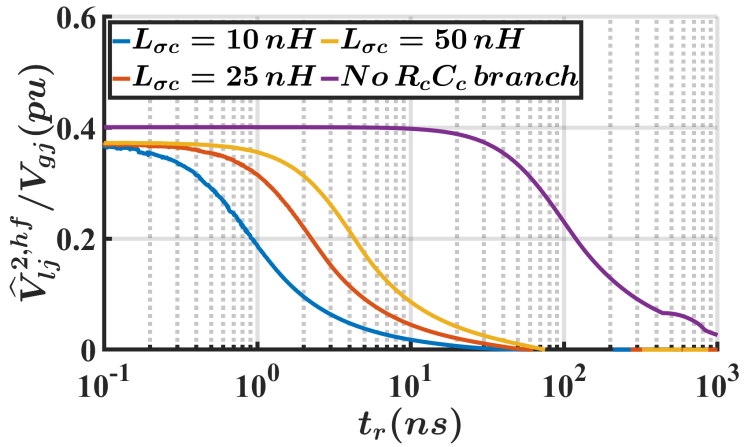


Figure 8.37: Simulation results: additional load voltage caused by L_σ and $L_{\sigma c}$, as a function of the V_{gj} rise time ($R = Z_j = R_c = 25\,\Omega$, $L_\sigma = 1.1\,\mu H$, $L = 21\,\mu H$, $t_{dj} = 200\,ns$, $\Gamma_{lj} = 1$, $C_c = L_\sigma/R_c^2$).

The performance variation caused by the parasitic inductance presented by the series of C_c and R_c is investigated. This circuital element is schematically depicted in Fig. 8.36. Different values of $L_{\sigma c}$ were considered during the analysis. In Fig. 8.37, the PSpice simulation results are depicted. The sequent observation can be done from the simulation results:

- a small advantage is always still present for all the L_σ values;
- the additional overvoltage presence can be shifted to lower values of rise time.

8.8.4 Compensation method evaluation

The simulations conducted in Fig. 8.37, when $L_{\sigma c}$ is considered, were conducted by imposing $L_{\sigma c}$ much smaller than L_σ. This hypothesis is applied because it can be demonstrated that the power loss presented by R is higher than the power loss of R_c.

During the simulations, it was observed that at maximum 10% of the total power dissipated by R was dissipated by R_c. The sequent points are suggested by the simulation results:

- as much the power cable is longer lower loss are presented by R_c. This happens because the constant time of the compensation circuit (R_cC_c) become negligible with respect to the propagation delay time of the cable.
- As much the resistor parasitic inductance is higher as much power is dissipated by the R_c. Thus, higher L_σ causes higher R_c power losses. This happens because the constant time (R_cC_c) is increased.

By virtue of all the results, the following conclusions can be made:

- resistors with higher power rating, which present, as a consequence, a higher parasitic inductance, can be used for the filter resistance (R).
- Resistors with low power rating, which present, as a consequence, a very low parasitic inductance, can be used for the compensation circuit (R_c).

8.9 Conclusions

In this chapter, the application of an RL filter to mitigate the motor overvoltage caused by inverters was investigated, focusing on the line-to-line motor overvoltages. Three power converters based on all-Si, Si-SiC and all-SiC were used with the same RL filter and drive. Using all-SiC instead of all-Si, an increase of 21% of the peak motor voltage was measured. It was observed that the matching task of the RL filter is not well satisfied when small voltage rise time interacts with

the filter resistor parasitic inductance. In fact, the high-frequency mismatching is a source of additional high-frequency voltages at the second and third load reflections, thus causing the detrimental effect seen in the experiment. Furthermore, it was discovered that the filter matching task can be improved with a filter resistance different from the cable surge impedance. Thus, new formulae for the RL filter have been derived, showing the necessity to increase the filter inductance value if the same target is kept. The proposed formulae were tested using different filter resistor values, showing good accordance with experimental results, even if the parasitic inductance between each resistor moderately changes. Moreover, the experimental details of the second and third reflected voltages have been provided, demonstrating the validity of the best filter resistance value.

A design guideline based on the existing and new formulae was presented. The proposed guideline makes it possible to optimize the design of R and L elements for a generic electric drive considering the voltage rise time of the inverter and the resistor parasitic inductance. By determining the resistor maximum parasitic inductance as a function of the dv/dt, it is possible to choose the cheapest resistor that fits the task. Otherwise, if the resistor technology cannot follow the increasing speed of WBG switches, the new formula proposed in this chapter can be used to properly size the RL filter.

In conclusion, a circuital topology used for eliminating the resistor parasitic inductance has been proposed. Theoretical and simulation analysis was conducted by showing its effectiveness.

Chapter 9

Conclusions and future developments

9.1 Conclusions

The conclusions derived in this Ph.D. thesis are summarized below.

- A prototype of a power converter controlled by an FPGA and compatible with all-Si, Si-SiC and all-SiC devices, was designed by following industrial standards. The designed converter used for ac drives passes all the stringent industrial regulations (e.g. UL). The converter with mounted all-Si power modules is right now under production. While converter based on Si-SiC and all-SiC devices is not under production because until now the power module producer company has no intention to put these power modules under mass production.

- Issues caused by the IPM itself were found during the preliminary test of the converter with mounted SiC devices. It was noticed that in extreme duty cycle condition IPM fault was triggered. This condition has been avoided by applying a workaround firmware. From this laboratory experience, it was discovered that standard voltage probes could be inadequate for the debugging of SiC switches due to their high speed. Thence, special and expensive instrumentations as fiber optically isolated probes could be necessary during the tests.

- By using FPGA instead of DSP the computational task of the drive has been increased from 16 kHz to 60 kHz.

- The losses of the converter were measured for different load conditions using a precise data acquisition system in combination with the opposition method technique. By virtue of having the same power module package, layout and heat sink fair comparisons between all-Si, Si-SiC and all-SiC were conducted.

  - Losses reduction has been found using Si-SiC instead of all-Si for each converter operating point. The experiments demonstrated that using the power modules based on Si-SiC, the nominal switching frequency can be increased from 8 kHz to 11.2 kHz. However, no important efficiency converter improvement at the nominal condition was revealed.
  - Remarkable losses reduction using all-SiC instead of all-Si and Si-SiC were measured. From the experimental results, the conduction losses were derived suggesting that for very low switching frequency and high current applications greater benefits could be found using all-Si and Si-SiC instead of all-SiC. During the experiments, by adopting all-SiC device, the converter was able to reach 19.5 kHz. Due to the limitations imposed by the IPM module fault, the converter was not able to reach a higher switching frequency. Finally, at the converter nominal condition, an important efficiency increasing of 1 % was measured, consequently raising the efficiency from 97.86 % to 98.8 %.

- Fair comparisons of drives issues presented when VSI are used between all-Si, Si-SiC and all-SiC devices were conducted. During the experiments, the same converter, cable, and motor were used. It has been observed that all the problems previously described in the literature became worse when all-SiC was used due to the high dv/dt. In fact, motor overvoltages were observed with only 2 m of cable connecting the converter to the motor. Furthermore, it has been observed the presence of overvoltage and ringing at the converter terminal caused by 25 cm of cable connecting the power module to the converter terminals. These problems can be reduced by shortening the distance between the two terminals (power module and converter terminals).

- The motor overvoltage issue has been investigated in detail. Novel and more precise formula of the load overvoltage in function of the voltage rise time and the cable length has been proposed. Furthermore, a detailed investigation validated through simulations of the phase-to-ground overvoltage was conducted by considering different velocities of propagation for the differential and the common mode components. The analysis shows that in special conditions the phase-to-ground motor voltage can reach to 2.17 V_{dc} instead of 1.5 V_{dc}. Moreover, the analysis suggests that the cable should be designed by maintaining the same velocity of propagation for the differential and the common mode components.

- A novel measurement methodology based on Clarke transformation that permits to identify the cable parameters of the drive has been proposed. By using these parameters, filters can be faster designed.

- A new elementary component of a transmission line, which permits to do

simulations of both high and low frequencies domains, has been defined and experimentally validated.

- An RL filter was designed for an existing drive and then a comparison of the filter performances was conducted by using all-Si, Si-SiC and all-SiC device configurations. It has been noticed that the small rise time imposed by the inverter combined with the resistor parasitic inductance causes an additional overvoltage at the load side. Thence, the standard design formulae were corrected and experimentally validated showing that the motor overvoltage is minimized for resistance value different from the differential surge impedance. In conclusion, a circuital topology used for eliminating this issue has been proposed and validated through simulations.

9.2 Final remarks

9.2.1 all-Si vs. Si-SiC

In conclusion, the sequent statements about inverter based on Si-SiC can be done by considering all the experimental results conducted in this research activity.

- Using Si-SiC devices instead all-Si the switching frequency of the converter can be increased by 40 %.
- No significant efficiency improvement has been registered at the nominal converter condition.
- The dv/dt is the same as the all-Si technology, thus no additional filters are required with respect to the standard case.
- No critical issues during the design (drive voltage) and testing of the converter were found.
- In the existing drive, retrofitting using inverter based on Si-SiC devices does not present contraindications.

9.2.2 all-Si vs. all-SiC

In conclusion, the sequent statements about inverter based on all-SiC can be expressed by considering all the experimental results conducted in this research activity.

- Using all-SiC devices instead of all-Si, the switching frequency of the converter could be increased theoretically by 525 %.

- Important efficiency improvement has been registered at the nominal converter condition.
- The dv/dt is very high with respect to the other two technologies. Motor overvoltage has been measured even with 2 m of cable. In industrial applications length of cables connecting drive are higher than 2 m, thence motor overvoltage would be always present. Furthermore, in case that the overvoltage is undamped and high switching frequency is applied, multiple overvoltage phenomena can happen. As a consequence, the motor overvoltage filter is very recommended.
- Special care is required during the design process of the converter (e.g. drive voltage, optocoupler) owing to the high dv/dt. Moreover, instrumentations with high bandwidth and good common mode rejection are required during the tests.
- In the existing drive, retrofitting using inverter based on all-SiC devices can be very dangerous even if an overvoltage filter is already installed.

9.3 Future developments

A series of open issues that can be addressed in the future are resumed below.

- By adopting the methodology applied in this work, it would be desirable to investigate in the future the pros and cons of using SiC devices in industrial converters with different voltage and current ratings, thus providing a full understanding of the performances introduced by these new components.
- Unfortunately, it was not possible to increase the switching frequency of the converter based on all-SiC devices to a frequency higher than 25 kHz. Thence, full exploitation of the thermal performances presented by this converter is required.
- It emerges from the equivalent model of the cable that common and differential components can travel at different speeds, thus causing higher motor overvoltages. It should be interesting to analyze the velocity of propagations of different cables in order to understand if these velocities of propagations are independent or not.
- It could be interesting to investigate the motor overvoltages in a drive with mounted an active front-end based on SiC devices also considering different grounding solutions.

- It has been demonstrated that the RL filter could present issues when inverters with high dv/dt are used. It might be interesting to study the performances of other filters when very fast devices are implemented in the drive.
- The compensation circuit developed for the issue found with RL filter should be experimentally validated.

Published papers

Journal papers:

- R. Ruffo, P. Guglielmi, E. G. Armando, "Inverter Side RL Filter Precise Design for Motor Overvoltage Mitigation in SiC Based Drives," in *IEEE Transaction on Industrial Electronics*. doi: 10.1109/TIE.2019.2898623.
- R. Ruffo, V. Cirimele, M. Diana, M. Khalilian, A. L. Ganga and P. Guglielmi, "Sensorless Control of the Charging Process of a Dynamic Inductive Power Transfer System With an Interleaved Nine-Phase Boost Converter," in *IEEE Transactions on Industrial Electronics*, vol. 65, no. 10, pp. 7630-7639, Oct. 2018. doi: 10.1109/TIE.2018.2803719.
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