On the Evaluation of the PIPB Effect within SRAM-based FPGAs

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***Abstract*— SRAM-based FPGAs are widely used in mission critical applications. Due to the increasing working frequency and technology scaling of ultra-nanometer technology, Single Event Transients (SETs) are becoming a major source of errors for these devices. In this paper, we propose an approach for evaluating the Propagation-induced Pulse Broadening (PIPB) effect introduced by the logic resources traversed by transient pulses. The proposed methodology is applicable to any recent technology to provide SET analysis, necessary for an efficient mitigation technology. Experimental results achieved from a set of benchmarks are compared with fault injection experiments executed on a 28 nm SRAM-based FPGA to demonstrate the effectiveness of our technique.**

Keywords—SRAM-based FPGAs, Single Event Transients, Propagation-Induced Pulse Broadening

I. Introduction and Background

In the last decades, Field Programmable Gate Arrays (FPGAs) have been used in many critical applications. Exploiting FPGAs, the development of customized electronic circuits can be achieved without the high costs and efforts of applying Application Specific Integrated Circuit (ASIC) solutions. Unfortunately, FPGAs used in space environment are subjected to cosmic rays and high energy particles that affects their reliability. Nowadays, commercially available FPGAs are widely used in space applications, especially when radiation-hardened ones cannot meet performance needs and cost limits of the missions. Due to the increasing of work frequency and the technology scaling that strongly characterize SRAM-based FPGAs, Single Event Transients (SETs) are becoming a major source of errors that should be investigated [1]. An ionized radiation particle which interacts with an FPGA can generate a voltage glitch known as SET. A SET pulse, generated in a sensitive node, propagates through a logic path, which includes several logic gates and routing interconnections. The propagation of the pulse continues until it reaches a memory element, where it can be latched and become a soft error. It is well known that a SET propagating through a logical gate chain may suffer from different effects (i.e. broadening or compression) that strongly affect its probability to be sampled. This phenomenon, known as Propagation-induced Pulse Broadening (PIPB), is of crucial importance to estimate if a SET could eventually produce a soft error. In [2], it has been shown that an initially narrow SET (i.e. 200 ps) can be broadened into the nanosecond range when it propagates through several combinational logic. The high work frequencies and the high technology scaling combined with the pulse broadening can make SEUs induced by SETs a relevant source of errors. Due to critical technology scaling and working frequencies of SRAM-based FPGAs, the value of the PIPB introduced by the combinational logic located between the node where the pulse is generated and the input of a memory element is fundamental to assert how much a memory element can be affected by soft errors caused by SETs. At best of our knowledge, very few works have investigated the SETs in SRAM-based FPGAs [3][4].

In this work, we propose an approach to statically evaluate the behavior of SETs propagating in the logic resources of SRAM-based FPGAs. The methodology evaluates the Propagation-induced Pulse Broadening (PIPB) effect while a SET pulse is propagating through the LUTs logic of an implemented design. The method takes into account the accurate behavior of SET pulse propagating through the Look-up Tables (LUTs) with respect to the used architectures and technologies. The algorithm has been applied to a set of benchmark circuits to evaluate their sensitivity to SETs and the results are compared with the ones obtained from fault injection experiments previously performed on a physical device.

This paper is organized in four sections. Section II explains our developed approach to static evaluate the PIPB effect. In section III, the evaluation is performed on a set of benchmarks using the proposed method. Lastly in section IV, conclusions and future works are discussed.

II. The Proposed PIPB Analyzer

The goal of the proposed approach is to statically evaluate the criticality to SETs of designs implemented on SRAM-based FPGAs making use of a SET characterization to predict the features of radiation-induced SETs and of a characterization of how PIPB affects the SET pulses when they propagates through the LUT logic in a specific FPGA technology. To do this, the approach aims to evaluate the sensitivity to SETs of user memory elements of a placed-and-routed design. Our developed Analyzer of PIPB effect on SETs (APES) exploits a graph structure obtained from an implemented design to analyze the effects induced by the LUTs logic on the SET propagation. APES can estimate how much SETs with a chosen starting width can be broadened, when they propagate until a memory element through several LUTs on a specific path of the design under test. The algorithm combines the different contributes introduced by the LUTs along the path, considering the width of the SETs and the LUT pins along which the pulses propagate accordingly with the characterizations provided.

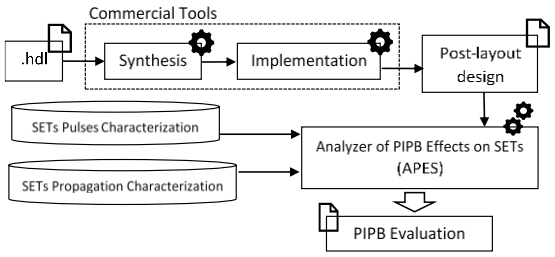

Fig. 1. Characterizations are provide to the Analyzer to obtain the PIPB evaluation for a design under test

The tool can obtain the PIPB value which may affect a SET generated in a specific node and reaching a memory element under test or it can compute the worst broadening effects that may affect SETs which reach the memory element under test. To compute the worst PIPB coefficient on each output pin of the logic elements in the logic cone of a flip-flop, the algorithm starts from the output of the elements in the top-level of the logic cone. These elements are mostly memory elements or input ports; hence they cannot propagate SETs. For this reason, the worst PIPB factor on their output is tagged as 1, which means that the worst SET observable in that position is the one that is generated right in the node, without any broadening effect. Differently, a PIPB factor greater than 1 would mean that the worst SET on the tagged node is a SET broadened (by the PIPB factor) by the elements it has passed through. Then, the nodes connected to these top-level elements are marked as candidates to have their worst PIPB computed. In each iteration, the worst PIPB is computed on the output of all the candidates which have each one of their inputs with a worst PIPB factor already computed. After that, the nodes they fed are added to the candidates set. This procedure is iterated until when the worst PIPB effect on the input of the flip-flops is found.

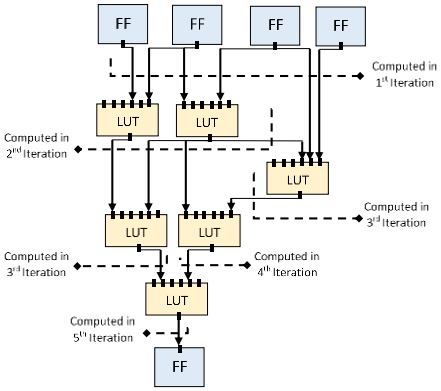

Fig. 2. A conceptual scheme of the functioning of the SET propagation analyzer.

III. Experimental Analysis and Results

The proposed approach has been applied on a set of benchmark circuits. The results have been compared with fault injection experiments exposed in [4]. Four designs have been chosen from ITC'99 benchmark collection [5] and implemented on a Xilinx Kintex-7 SRAM-based FPGAs. Table I provides information on the complexity of each design such as number of flip-flops cells, number of LUT cells, average depth of flip-flops logic cones and maximum depth among flip-flops logic cones. APES has been used to obtain an overview of the sensitivity to PIPB effects of the designs.

TABLE I. Benchmark Designs Characteristics

Circuits	**Benchmark Designs Characteristics**			
	FF CELL [#]	***LUT CELL [#]***	***Max FF Logic Cone Depth***	***Average FF Logic Cone Depth***
B05	34	91	6	3.2
B12	119	251	6	4.1
B14	215	1,071	14	11.1
B15	416	1,390	14	9.2

Figure 3 shows a figure of merit of the benchmark designs. In details, the graph reports the PIPB worst-case computed for each flip-flop in the designs. The flip-flops are plotted on x-axis using an identifier normalized on the total number of flip-flops. The IDs are assigned in ascend order accordingly with the PIPB value evaluated on each flip-flop.

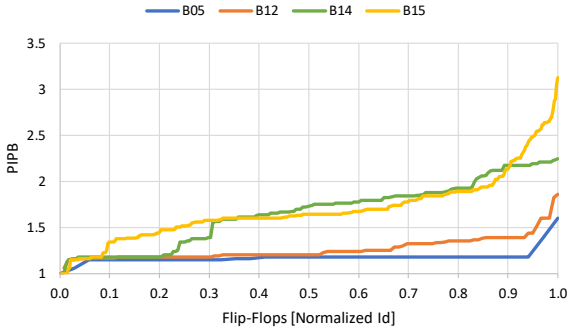

Fig. 3. Propagation-induced Pulse Broadening (PIPB) Figure of Merit of the benchmark designs.

The static analysis has been carried out for pulses with a width of 400 ps. The SET propagation characterization has been obtained by means of electrical simulations, taking into account the physical device technology. B14 and B15 circuits implement respectively a subset of Viper and 80386 processors. These two circuits have a greater complexity and longer combinational chains than B05 and B12 making them more sensitive to PIPB effect. The results we obtained are comparable to the ones reported in [4] through internal electrical injection on physical devices for designs B12 and B14. In details, our experiments report for B12 and B14, in case of SET width of 400 ps, PIPB effects of 1.86 and 3.12 respectively. Similarly, the experiments described in [4] showed a PIPB effects on SETs with width 400 ps of respectively 2 and 3.

IV. Conclusions and Future Work

In this paper, we presented a method for analyzing the design reliability regarding SETs for circuits implemented on SRAM-based FPGAs. The developed method has been evaluated on ITC99 testbenches implemented on Xilinx Kintex-7 SRAM-based FPGA, identifying the critical memory elements of the selected testbench.

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