Abstract

A novel lightweight detector based on CGEM (Cylindrical Gas Electron Multiplier) technology has been developed to replace the aging inner tracker of the BESIII Spectrometer, an experiment carried out at the Beijing Electron Positron Collider in China. The CGEM-IT (CGEM Inner Tracker) consists of three independent layers of cylindrical GEM and, thanks to its fast response, low material budget, high rate capability and excellent radiation tolerance, will provide an improved spatial resolution along the beam axis and the required performance for the entire experiment lifetime. In order to face the unprecedented challenge of achieving high level tracking performance in a strong magnetic field (1 T) with a cylindrical GEM detector, an analogue readout, implementing charge centroid and μTPC (micro Time Projection Chamber) reconstruction algorithms, has been adopted. Compared to a binary readout, this approach allows to reduce the total number of channels to about 10000 which are readout by a dedicated Application Specific Integrated Circuit (ASIC) providing simultaneous measurement of the input signals time-of-arrival and deposited charge.

The chip comprises 64 independent channels, each of which featuring an analogue front-end for signal amplification and conditioning followed by a versatile back-end for the digitization of the event timestamp and input charge. The design of the analogue front-end has been driven by the requirements set by the detector. The ASIC is thus optimized for the readout of signals up to 50 fC, with a maximum event rate of 60kHz per channel and a noise below 2000 electrons r.m.s. for an input capacitance up to 100 pF. A dual-branch architecture, with different peaking time shapers, is employed in order to provide time and charge measurement with the required resolution. The event timestamp is digitized by low-power, quad-buffered TDCs, based on analogue interpolation, delivering a sub-50 ps time binning. In default operation mode, the charge information is extracted by a Sample-and-Hold (S&H) circuit, working as a digitally-controlled peak detector, that allows to capture the voltage peak at the output of the slower shaper. This value is then digitized by a 10-bit Wilkinson ADC which is shared with the TDCs. In order to extend the input dynamic range and overcome the potential saturation of the measurement provided by the S&H circuit, the charge information can also be inferred from the Time-over-Threshold measurement. The ASIC has been fabricated in a cost-effective and well-established 110 nm CMOS technology node, which is largely adopted for radiation detection in particle physics. A first silicon iteration allowed to

fully characterize the chip and correct some design weaknesses before the ASIC was submitted for the mass production. In view of the 2020 installation, integration tests with the CGEM-IT detector coupled with the full-chain readout electronics are now ongoing.

This thesis describes and discusses the design and characterization of a mixed-signal ASIC for the readout of the CGEM-IT and is organized as follows.

Chapter 1 reports a brief description about the BESIII experiment, discussing some details of the detector system and providing some motivations for the CGEM-IT upgrade. The main features and innovations of the CGEM-IT project are described. Moreover, an overview of the full-chain readout electronics is given.

The basic features of a typical front-end ASIC for a particle detector are described in Chapter 2. The main building blocks of the system are discussed, following the signal path: after its formation in the sensor, the signal is amplified and shaped by the analogue front-end and then, before being transmitted off-chip, discriminated and, eventually, digitized. In the last part of this chapter several readout architectures are illustrated, providing for some of them an example of practical implementation.

In Chapter 3 the design and functionality of each block of the ASIC described in this thesis, from the analogue front-end amplifier to the digital controller, are discussed in detail and supported by computer simulations results. Chapter 4 presents the results from the ASIC electrical characterization, showing its full functionality, and from two beam tests which have been carried out to confirm the suitability of this chip for the readout of GEM detectors.

Keywords: ASIC; Readout electronics; Mixed-signal design; Charge and time measurement; BESIII; GEM.