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MOSFET ZTC Condition Analysis for a Self-biased Current Reference Design

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ABSTRACT

In this paper a self-biased current reference based on Metal-Oxide-Semiconductor Field Effect Transistor (MOSFET) Zero Temperature Coefficient (ZTC) condition is proposed. It can be implemented in any Complementary Metal-Oxide-Semiconductor (CMOS) fabrication process and provides another alternative to design current references. In order to support the circuit design, ZTC condition is analyzed using a MOSFET model that is continuous from weak to strong inversion, showing that this condition always occurs from moderate to strong inversion in any CMOS process. The proposed topology was designed in a 180 nm process, operates with a supply voltage from 1.4V to 1.8 V and occupies around 0.010mm^2 of silicon area. From circuit simulations our reference showed a temperature coefficient (TC) of 15 ppm/°C from -40 to +85°C, and a fabrication process sensitivity of σ/μ = 4.5% for the current reference, including average process and local mismatch variability analysis. The simulated power supply sensitivity is estimated around 1%/V.

Index Terms: MOSFET ZTC Condition, Current Reference Source and Low Temperature Coefficient.

I. INTRODUCTION

Current references are essential building blocks for analog, mixed-signal and RF designs, often being used for biasing of analog subsystems inside the chip. The usual way to generate a current reference is through the implementation of a voltage reference [1], [7], [10], [16] and applying this voltage over a resistive device [2]. Another approach is using a device where a physical property or condition naturally establishes an operating current, which can be used as a reference [3]– [6], [8], [9], [14], [18].

Any kind of Direct Current (DC) reference, either a voltage or a current one, must offer appreciable thermal stability and power supply rejection, as its main characteristics. In addition, adequate fabrication repeatability ensures that the biasing operation point of the analog blocks is almost the same in every fabricated chip, and reveals how sensitive the current generator is with respect to fabrication process variations [19].

The main idea of this paper is to use the physical condition of MOSFETs called "zero temperature coefficient" (ZTC) to implement a circuit topology where the resulting current offers low sensitivity to temperature and process variations. This condition defines a biasing point where the drain current presents small temperature sensitivity, as can be seen in Fig. 1. The ZTC current condition occurs for every MOSFET in any technology, for N-Channel Metal-Oxide-Semiconductor (NMOS) and P-Channel Metal-Oxide-Semiconductor (PMOS) transistors, and it is the effect of mutual cancellation of the channel carrier mobility and the threshold voltage dependencies on temperature [4]. Remembering that the drain current increases when mobility increases and when threshold voltage decreases, and that mobility and threshold voltage both decrease when temperature increases, it can

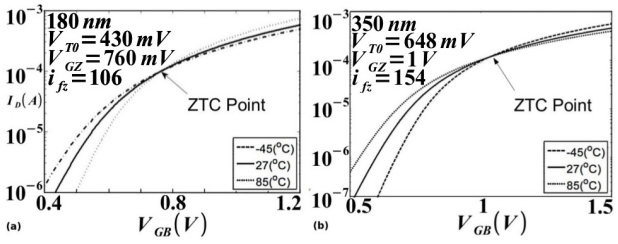

Figure 1. NMOS ZTC point for (a) 180 and (b) 350nm bulk-CMOS processes.

be proved that both effects can cancel each other at a certain bias point. Fig. 1 presents the drain current vs gate-source voltage of NMOS transistors under three temperatures for two different fabrication process, and in both figures a convergence point can be seen for the three I-V curves drawn.

The traditional analysis of this effect presented in literature is based on the strong inversion quadratic MOSFET model [4]. In this work we use a different analytical approach, based on a continuous MOSFET model that can predict its behavior from weak to strong inversion [11][21]. Based on this analysis, we verify that the ZTC point occurs from moderate to strong inversion for any CMOS process.

This paper is organized as follows. In Section II, an analytical formulation and the discussion about the ZTC operating point using an all-region CMOS compact model are presented. In Section III, simulation results from three fabrication processes are presented, regarding the ZTC operating point. After selecting a fabrication process for our design, in Section IV a self-biased CMOS current reference topology is proposed and described. The simulation results are presented in section V, followed by comparisons to other references proposed in literature. Finally, in section VI, the concluding remarks are drawn.

II. MOSFET ZTC CONDITION

MOSFET ZTC condition derives from mutual cancellation of mobility and threshold voltage dependencies on temperature [4]-[5], at a particular gate-to-bulk voltage bias. The drain current ZTC operating bias point was firstly defined in [4] and after in other correlated publications, always based on strong inversion quadratic MOSFET model. From [4], ZTC operating point is given by Eqs. (1) and (2).

$$V_{GZ}=V_{T0}(T_0)+nV_{SB}-\alpha_{V_{T0}}T_0 \tag{1}$$

$$I_{DZ} = \frac{\mu(T_0)T_0^2C'_{ox}}{2n}\left(\frac{W}{L}\right)\alpha_{V_{T0}}^2 \tag{2}$$

where T_0 is the room temperature, $V_{T0}(T0)$ is the threshold voltage at room temperature, n is the slope factor, V_{SB} is the source-bulk voltage, α_{VT0} is the thermal coefficient of the threshold voltage (a negative parameter, since V_{T0} decreases with temperature), $\mu(T_0)$ is the low field mobility at room temperature, C'_{ox} is the oxide capacitance per unit of area and (W/L) is the transistor aspect ratio. and are defined as gate-bulk and drain current ZTC bias point, respectively.

Fig. 1 (a) shows the drain current (in a log scale) as a function of gate-bulk voltage (V_{GB}) of a saturated long-channel NMOSFET, simulated under temperatures ranging from -45 to +85°C, for a 180 nm process. ZTC operation point can be seen around $V_{GB} \approx$ 760mV for a transistor with V_{T0} = 430mV, resulting that ZTC point occurs for an overdrive voltage around 330mV, meaning the transistor operates in strong inversion. Fig. 1 (b) shows the same for an NMOS transistor in a 350 nm CMOS process.

In a more general analysis, we can suppose that the ZTC condition can also happen in moderate inversion and a more complete MOSFET model must be used, such as one presented in [11], which describes continuously transistor behavior at any inversion level. The well-known Advanced Compact Model (ACM) is a design-oriented MOSFET model suitable for analog integrated-circuit design. From this model, Eqs (3) and (4) give the drain current of a long channel NMOSFET.

$$I_D = I_F - I_R = I_S\left(i_f - i_r\right) \tag{3}$$

$$I_S = \mu C'_{ox} n \frac{\phi_t^2}{2}\frac{W}{L} \tag{4}$$

where $I_{F(R)}$ is the forward (reverse) current, $i_{f(r)}$ is the forward (reverse) inversion coefficient, I_S is the normalization current, and ϕ_t is the thermal voltage.

Also from this model, Eqs. (5), (6) and (7) relate source and drain inversion coefficients (forward and reverse), i_f and i_r, with the three external voltages applied to transistor terminals, V_{GB}, V_{SB} and V_{DB}, using bulk terminal as reference.

$$V_P - V_{S(D)B} = \phi_t\left[\sqrt{1+i_{f(r)}} - 2 + ln\left(\sqrt{1+i_{f(r)}} - 1\right)\right] \tag{5}$$

$$V_P = \frac{V_{GB} - V_{T0}}{n} \tag{6}$$

$$V_{T0} = V_{FB} + 2\phi_F + \Upsilon\sqrt{2\phi_F} \tag{7}$$

where V_P is called the pinch-off voltage, Υ is the body effect coefficient, V_{FB} is the flat band voltage and ϕ_F is the Fermi potential at the bulk of semiconductor under transistor channel.

First order temperature dependence of V_{T0} can be given by Eqs. (8) and (9) [11].

$$V_{T0}(T) = V_{T0}(T_0) - |\alpha_{T0}|(T - T_0) \tag{8}$$

$$\left|\frac{\delta V_{T0}}{\delta T}\right|_{T=T_0} = |\alpha_{T0}| = \frac{1}{T_0}\left(1 + \frac{\Upsilon}{\sqrt{2\phi_F}}\right)\left(\frac{E_G}{2q} - \phi_F\right) \tag{9}$$

where q is the electron charge and E_G is the silicon band-gap energy. Fig. 2 presents expected values

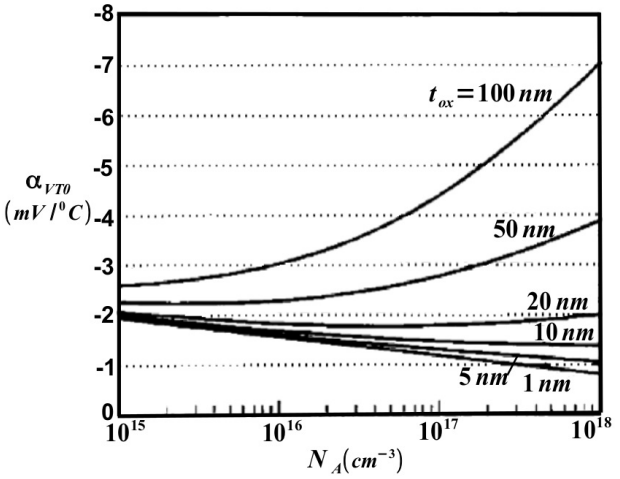

Figure 2. α_{VT0} vs N_A for different t_{ox} [13].

for α_{VT0} for wide ranges of doping concentration (N_A) and oxide thickness (t_{ox}) [13]. The target-technologies for this study are below 350 nm, which corresponds to α_{VT0} values between -3.5 and -0.5 mV/°C [13], that is the range used in the following analysis. In addition, Eq. (10) gives the thermal mobility dependence [13].

$$\mu(T) = \mu(T_0)\left(\frac{T}{T_0}\right)^{\alpha_\mu} \tag{10}$$

where α_μ is the temperature dependence power for mobility model. Since the carriers in inversion layer of transistors undergo several scattering mechanisms, α_μ is negative, and its value depends on prevalent scattering mechanisms (such as Coulombic, phonon, or interface scatterings - all of them interfering on carrier transport). Related to electron mobility and under room temperature this parameter varies in a range from -1.5 for high doping concentrations to – 2.4 for light doping concentrations [13].

If one derives the drain current expression for temperature in saturation region ($i_r << i_f$), the condition where its temperature dependence is negligible can be found, i.e., $\delta I_D/\delta T\big|_{T=T_0} \approx 0$. Using Eq. (3) and deriving it as a function of temperature.

$$\frac{\delta}{\delta T}\left(I_S i_f\right)\Big|_{T=T_0} = I_S \frac{\delta i_f}{\delta T}\Big|_{T=T_0} + i_f \frac{\delta I_S}{\delta T}\Big|_{T=T_0} \tag{11}$$

The $\frac{\delta i_f}{\delta T}\Big|_{T=T_0}$ can be found deriving Eqs. (5) and (6) with respect to temperature, to find that

$$\frac{\delta}{\delta T}\left(\frac{V_{GB}-V_{T0}}{n} - V_{SB}\right) = \frac{\delta}{\delta T}\left(\phi_t\left[\sqrt{1+i_f} - 2 + \ln\left(\sqrt{1+i_f}-1\right)\right]\right) \tag{12}$$

As V_{GB} and V_{SB} are temperature independent,

$$\frac{\delta}{\delta T}\left(\frac{-V_{T0}}{n}\right) = \frac{\delta\phi_t}{\delta T}\left[\sqrt{1+i_f} - 2 + \ln\left(\sqrt{1+i_f}-1\right)\right] + \phi_t \frac{\delta}{\delta T}\left(\sqrt{1+i_f} - 2 + \ln\left(\sqrt{1+i_f}-1\right)\right) \tag{13}$$

Assuming that $\frac{\delta\phi_t}{\delta T} = \frac{\phi_t}{T}$ and putting (8) in (13)

$$\frac{\delta}{\delta T}\left(\frac{|\alpha_{VT0}|}{n}\right) = \frac{\phi_t}{T}\left[\sqrt{1+i_f} - 2 + \ln\left(\sqrt{1+i_f}-1\right)\right] + \phi_t \frac{\delta}{\delta T}\left(\sqrt{1+i_f} - 2 + \ln\left(\sqrt{1+i_f}-1\right)\right) \tag{14}$$

Noting that the second term of the right branch of the Eq. (14) is equal to

$$\frac{\delta}{\delta T}\left(\sqrt{1+i_f} - 2 + \ln\left(\sqrt{1+i_f}-1\right)\right) = \left(\frac{1}{2\left(\sqrt{1+i_f}+1\right)}\right)\frac{\delta i_f}{\delta T} \tag{15}$$

And putting Eq. (15) in (14),

$$\frac{\delta}{\delta T}\left(\frac{|\alpha_{VT0}|}{n}\right) = \frac{\phi_t}{T}\left[\sqrt{1+i_f} - 2 + \ln\left(\sqrt{1+i_f}-1\right)\right] + \phi_t\left(\frac{1}{2\left(\sqrt{1+i_f}+1\right)}\right)\frac{\delta i_f}{\delta T} \tag{16}$$

Isolating the term $\frac{\delta i_f}{\delta T}$ from Eq. (16), we get

$$\frac{\delta i_f}{\delta T} = 2\left(\sqrt{1+i_f}+1\right)\left(\frac{|\alpha_{VT0}|}{n\phi_t} - \frac{1}{T}\left(\sqrt{1+i_f} - 2 + \ln\left(\sqrt{1+i_f}-1\right)\right)\right) \tag{17}$$

The derivative of normalization current regarding the absolute temperature can be found from Eq. (4) and Eq. (10).

$$\frac{\delta I_S}{\delta T} = \frac{1}{2}C'_{ox} n \frac{W}{L}\frac{\delta}{\delta T}\left(\phi_t^2 \mu\right) \tag{18}$$

where $\delta n/\delta T = 0$. After some algebra,

$$\frac{\delta I_S}{\delta T} = \frac{1}{2}C'_{ox} n \frac{W}{L}\left(\frac{\delta\mu}{\delta T}\phi_t^2 + \frac{\delta\phi_t^2}{\delta T}\mu\right) \tag{19}$$

Therefore, we can use $\frac{\delta\mu}{\delta T} = \frac{\alpha_\mu \mu}{T}$ and $\frac{\delta\phi_t^2}{\delta T} = \frac{2\phi_t}{T}$ in (19), we obtain

$$\frac{\delta I_S}{\delta T} = I_S\left(\frac{\alpha_\mu + 2}{T}\right) \tag{20}$$

Finally, applying Eqs. (20) and (17) in (11), and after isolating some terms one can find:

$$\frac{|\alpha_{VT0}|T}{n\phi_t} = \frac{|\alpha_{VT0}|q}{nk} = \left(\frac{\alpha_\mu + 2}{2}\right)\left(\frac{-i_{fz}}{\sqrt{1+i_{fz}}+1}\right) + \left[\sqrt{1+i_{fz}} - 2 + \ln\left(\sqrt{1+i_{fz}} - 1\right)\right] \quad (21)$$

where k is the Boltzmann constant and i_{fz} is defined as ZTC forward inversion level. Eq. (21) shows that if the transistor is biased such that the inversion level at source is i_{fz}, the drain current is insensitive to temperature.

Fig. 3 shows the ZTC forward inversion level surface (ZTCS), i.e., all possible solutions of Eq. (21) for ZTC bias condition as a function of values for α_μ and α_{VT0}. The ZTCS shows that the minimum ZTC forward inversion level is around 15.6 for α_μ = -2.5 and α_{VT0} = -0.5 mV/°C. Since inversion coefficient i_f = 3 means the condition where $V_{GB} = V_{T0}$ from Eqs. (5) and (6), one can conclude that ZTC bias condition always occurs for gate-bulk voltages larger than threshold voltage. Also, it is visible that ZTC inversion coefficient (i_{fz}) is only slightly dependent on α_μ, when compared to α_{VT0} dependence, justifying the usual choice $\alpha_\mu \approx$ -2 as a reasonable consideration for design purposes [4].

In order to see how far ZTC bias point is from threshold voltage (the overdrive voltage for ZTC bias point), for $V_S = 0$, the i_{fz} can be directly applied in Eq. (5) and (6),

$$V_{GZ} - V_{T0} = V_{OVZ} = n\phi_t f(i_{fz}) \quad (22)$$

where

$$f(i_f) = \sqrt{1+i_f} - 2 + \ln\left(\sqrt{1+i_f} - 1\right) \quad (23)$$

V_{OVZ} is defined as ZTC overdrive voltage. Fig. 4 shows all possible V_{OVZ} for any α_μ and α_{VT0} combination

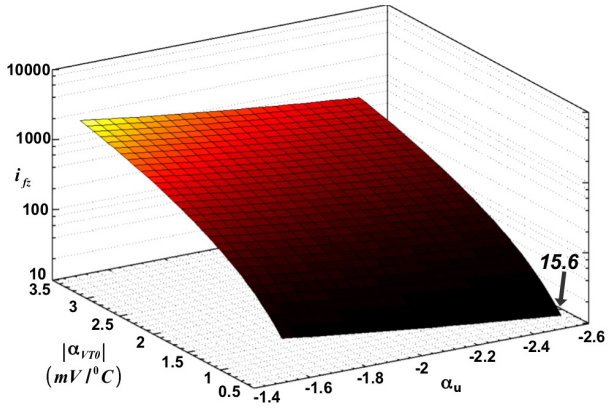

Figure 3. ZTC forward inversion level Surface (ZTCS).

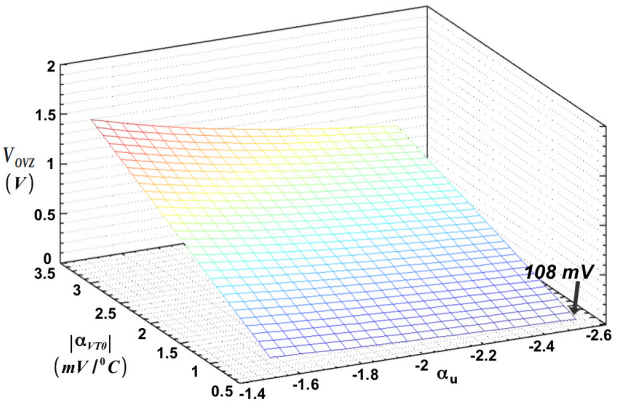

Figure 4. VOVZ - ZTC overdrive voltage.

in the same range that was used in Fig. 3. The minimum V_{OVZ} found is around 100 mV meaning that the ZTC bias point is always in moderate inversion condition or above.

Now using the assumption $\alpha_\mu \approx 2$ together with Eq. (21) and (5), a simple expression for ZTC gate-bulk voltage (V_{GZ} - related to i_{fz}) is found.

$$V_{GZ} = V_{T0}(T_0) + nV_{SB} - \alpha_{V_{T0}} T_0 \quad (24)$$

Eq. (24) presents the same result already derived from the strong inversion quadratic model in Eq. (1). ZTC drain current, related to i_{fz}, can be found using Eq. (3)

$$I_{DZ} = I_{FZ} = I_S(T_0) i_{fz} \quad (25)$$

III. MOSFET ZTC IN COMMERCIAL PROCESSES

ZTC condition of three commercial processes were evaluated through Spice simulations for these devices. Besides 180 and 350 nm already presented in Fig. 1, also the many-threshold transistors of a 130 nm process were verified. Table I shows some results for these transistors, including the threshold voltage (V_{T0}), the ZTC bias point (V_{GZ}, I_{DZ}) and corresponding inversion level (i_{fz}). For modern very short-channel nodes, some recent studies show that the ZTC condition still occurs [17].

Table I. ZTC Operating Point with W/L = 10µm/1 µm.

MOSFET	V_{T0} (V)	V_{GZ} (V)	I_{DZ} (µA)	i_{fz}
180 nm Regular	0.43	0.76	96.27	106
350 nm Regular	0.648	1.05	116.69	154
130 nm Regular	0.16	0.49	222.6	106
130 nm Low-Vt	0.1	0.44	274.8	112
130 nm Low-Power	0.6	0.87	128.1	74
130 nm Zero-Vt	0.063	0.23	97.7	32.5

IV. PROPOSED CURRENT REFERENCE

Main idea of this paper is to use ZTC vicinity of a NMOS transistor to compensate the thermal drift of a polysilicon resistor, resulting on an equilibrium bias point with small temperature dependence. This circuit topology naturally can be useful as a reference.

Fig. 5 shows proposed self-biased current reference. It is composed by ZTC NMOS transistor (M_{ZTC}) and a poly resistor (R_{poly}) inside a feed-back loop implemented with an Operational Transconductance Amplifier (OTA). PMOS mirror formed by M_1 - M_3 is for biasing and a start-up circuit is composed by M_4 - M_6 [20].

A. ZTC vicinity condition

Vicinity of ZTC condition can be analyzed using Eqs. (5) and (6),

$$V_{GB} = n\phi_t f(i_f) + V_{T0}(T) + nV_{SB} \tag{26}$$

Eq. (26) can be expanded in Taylor series around ZTC forward inversion level (i_{fz}). Therefore, the first order approximation is given by

$$V_{GB}(i_f) \approx V_{GZ} + \left.\frac{\delta V_{GB}}{\delta i_f}\right|_{i_f=i_{fz}} (i_f - i_{fz}) \tag{27}$$

where

$$\frac{\delta V_{GB}}{\delta i_f} = n\phi_t \frac{\delta f(i_f)}{\delta i_f} \tag{28}$$

After some analytical work, the following relation is obtained:

$$\frac{\delta f(i_f)}{\delta i_f} = \frac{1}{2(\sqrt{1+i_f}-1)} \tag{29}$$

Combining Eqs. (27), (28) and (29),

$$V_{GB}(i_f) \approx V_{GZ} + \frac{n\phi_t}{2(\sqrt{1+i_{fz}}-1)} (i_f - i_{fz}) \tag{30}$$

For $\alpha_\mu \approx -2$, the term $n\phi_t$ can be extracted from Eq. (21) and can be applied in Eq. (30). Then,

$$V_{GB}(T) \approx V_{GZ} - \frac{\alpha_{VT0}\Delta i_f}{2f(i_{fz})(\sqrt{1+i_{fz}}-1)} T \tag{31}$$

where

$$\Delta i_f = (i_f - i_{fz}) \tag{32}$$

Eq. (31) shows that V_{GB} presents a linear temperature dependence in vicinity of V_{GZ}, and that this dependence can be positive or negative, depending on chosen Δi_f.

Proposed circuit will be designed in next section for a 180 nm process, using a NMOS transistor where the ZTC bias point occurs in the strong inversion region (Section III). In this way, for design purposes both approximations $f(i_f) \approx \sqrt{i_{fz}}$ and $(\sqrt{i_{fz}+1}-1) \approx \sqrt{i_{fz}}$ can be adopted and applied in Eq. (31).

$$V_{GB}(T) \approx V_{GZ} - \frac{\alpha_{VT0}\Delta i_f}{2i_{fz}} T \tag{33}$$

As $i_f = I_D/I_S$ from Eq. (3), the dependency of V_{GB}(T) on temperature can be found such that:

$$V_{GB}(T) \approx V_{GZ} - \frac{\alpha_{VT0}\Delta I_D}{2iI_{DZ}} T \tag{34}$$

Fig. 6 illustrates the temperature dependence of Eq. (34), showing that if one chooses $\Delta I_D > 0$ (bias current "after" ZTC point), its derivative is positive, $\Delta I_D = 0$ is chosen (ZTC point), variation is zero, and if $\Delta I_D < 0$ (bias current "before" ZTC point), its derivative is negative. One can conclude that a MOSFET operating in vicinity of ZTC point presents a transconductance that can offer a positive or negative thermal dependence, the signal and magnitude of which can be adjusted by chosen bias current.

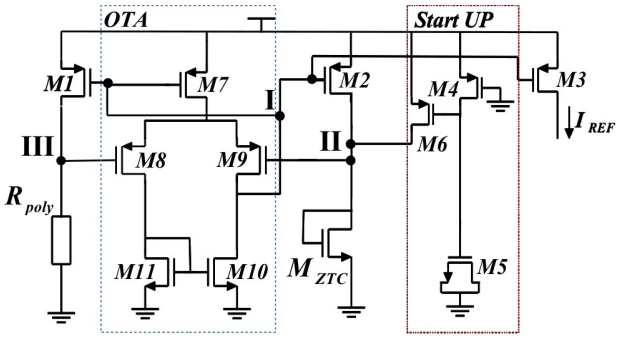

Figure 5. Self-biased CMOS Current Reference.

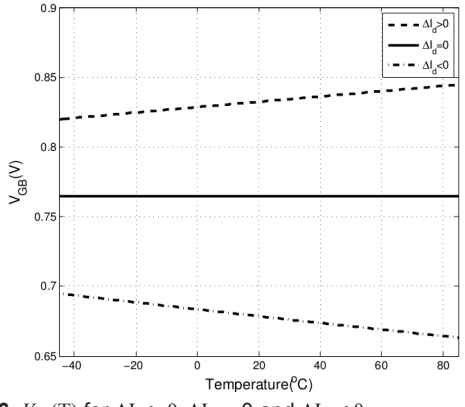

Figure 6. V_{GB}(T) for $\Delta I_D > 0$, $\Delta I_D = 0$ and $\Delta I_D < 0$.

B. Circuit Analysis

PMOS mirror formed by M1 - M3 is supposed to have an unitary gain in all branches for this analysis. Applying Kirchhoff's voltage law (KVL) over poly resistor, differential input of OTA and ZTC NMOS transistor, Eq. (35) is derived.

$$R(T) \approx R(T_0)(1 + \alpha_1(T - T_0)) \tag{35}$$

where V_{OS} is the amplifier offset voltage and I_{REF} is the desired output current. Poly resistor thermal dependence can be approximated as

$$R(T) \approx R(T_0)(1 + \alpha_1(T - T_0)) \tag{36}$$

Using (34), (36) and (35), one can derive

$$(1 - \alpha_1 T_0)R(T_0)I_{REF} + (R(T_0)\alpha_1 I_{REF})T = V_{OS} + V_{GZ} - \frac{\alpha_{VT0}(I_{REF} - I_{DZ})}{2I_{DZ}}T \tag{37}$$

Manipulating temperature dependent and independent parts, Eq. (38) and (39) are derived.

$$(1 - \alpha_1 T_0)R(T_0)I_{REF} = V_{OS} + V_{GZ} \tag{38}$$

$$R(T_0)\alpha_1 I_{REF} = \frac{\alpha_{VT0}(I_{REF} - I_{DZ})}{2I_{DZ}} \tag{39}$$

Now the terms $R(T_0)$ from (38) and I_{DZ} from (39) can be isolated

$$R(T_0) = \frac{V_{OS} + V_{GZ}}{I_{REF}(1 - \alpha_1 T_0)} \tag{40}$$

$$I_{DZ} = \frac{I_{REF}}{1 - \frac{2}{\alpha_{VT0}}R(T_0)\alpha_1 I_{REF}} \tag{41}$$

Expressions (40) and (41) show the dependence of parameters of devices, $R(T_0)$ and I_{DZ}, and the current I_{REF} , i.e., for a different I_{REF} , a new sizing for R_{poly} and M_{ZTC} is required.

Another consideration that must be taken into account is the sizing of PMOS mirror M_1 - M_2. One should consider the V_{GB} range, defined by Eq. (42).

$$\left|V_{GZ} + \frac{\alpha_{VT0}\Delta I_D T}{2I_{DZ}} + V_{T0_{P9}}\right| < |V_{GB_{1,2}}| < |V_{DD} - V_{DSAT_{10}}| \tag{42}$$

where $V_{DSAT_{10}}$ is the overdrive voltage of M_{10} and $V_{T0_{P9}}$ is the threshold voltage of M_9.

Regarding the stability of circuit, Eq. (43) describes the gain loop transfer function.

$$OL(s) = \frac{gm_{8,9}gm_{1,2}r_0(R(T_0) - r_{ztc})}{\left(\frac{s}{p_1} + 1\right)\left(\frac{s}{p_2} + 1\right)\left(\frac{s}{p_3} + 1\right)}$$
$$p_1 = (r_0 C_I)^{-1},$$
$$p_2 = (r_{ztc} C_{II})^{-1},$$
$$p_3 = (R(T_0) C_{III})^{-1}, \tag{43}$$

where $gm_{8,9}$ is the OTA transconductance, r_0 is the equivalent output resistance of OTA, r_{ztc} is equivalent resistance of ZTC transistor, $gm_{1,2}$ is the transconductance of PMOS mirror and C_I , C_{II} and C_{III} are the capacitance related to node I, II and III (Fig. 5).

C. Circuit Design

Circuit design was optimized through the Wicked™-MunEDA software [15] along with Cadence™ Tools. This tool is useful to improve yield, helping designers to spend less time in optimizing their design for yield, which is certainly an important market demand [12]. Design process was done using the methodology presented in Fig 7 [15]. This approach is composed by an initial analytical sizing, using design formulas described in this work, followed by electrical simulation, numerical sizing, layout and parasitic extraction. Unlike traditional analog design method, where simulation is used only as a verification tool, Wicked-MunEDA software modifies the device geometries iteratively based on simulation results, improving desired parameters. Main advantage of this process is to avoid intensive re-simulation time, which is a common burden in traditional analog design flow [15].

Analytical sizing was done using equations from subsection IV-B, along with the assumption that long channel MOS transistors were used and $\alpha_\mu \approx 2$. Process documentation and simulation were used to evaluate device parameters.

First step is the definition of I_{REF} and correspondent resistor $R(T_0)$ from Eq. (40). Considering $V_{SB} = 0$ and $V_{OS} = 0$,

$$R(T_0) \approx \frac{V_{T0}(T_0) - \alpha_{VT0}T_0}{I_{REF}(1 - \alpha_1 T_0)} \tag{44}$$

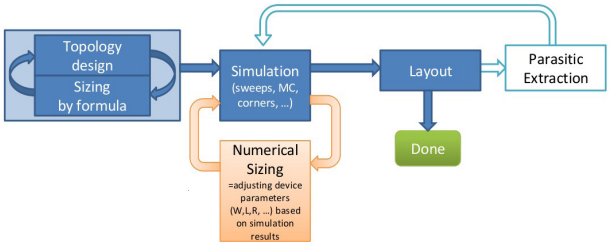

Figure 7. Numerical Sizing with Wicked™

Then, using (2) in (41), ZTC NMOS (M_{ZTC} in Fig.5) transistor can be sized.

$$\left(\frac{W}{L}\right)_{ZTC} = \frac{2n\left(\frac{-2}{\alpha_{VT0}}R(T_0)\alpha_1 + \frac{1}{I_{REF}}\right)^{-1}}{\mu(T_0)T_0^2 C'_{ox}\alpha_{VT0}^2} \quad (45)$$

PMOS mirror M_1-M_2 can also be sized by Eq. (46), taking care about the condition from Eq. (42).

$$\left(\frac{W}{L}\right)_{1,2} = \frac{2nI_{REF}}{\mu(T_0)C'_{ox}(V_{GB} + nV_{SB} - V_{T0P})^2} \quad (46)$$

Stability can be analytically checked using Eq. (43) or can be simulated.

After initial sizing, numerical size adjustment is done to improve the circuit yield, using "Feasibility Optimization" (FEA) followed by "Deterministic Nominal Optimization" (DNO). FEA enables the circuit designer to check all electrical/geometrical constraints and DNO improves circuit sizing by changing design parameters with unique gradient-based optimization algorithms, as "least-square algorithm" and "parameter distance algorithm". Finally, yield Optimization (YOP) analysis is done [15] in our design method.

D. Layout

The reference current layout is small, occupying only 0.01 mm², as shown in Fig. 8. The placement of devices was performed taking all precautions to minimize mismatch effects of global variations. In addition, PMOS mirror and ZTC NMOS were designed to occupy approximately 80% of total layout area, since the sizes of both are dominant factors in determining local mismatch effects.

Final transistor and resistor sizing, after all FEA and DNOS optimization steps, for all devices shown in the schematics of Fig. 5 are given in Table II.

Table II. Device sizing of proposed current reference (180 nm).

Device	Width (µm)	Length (µm)
R_{poly} (7108.2Ω)	2.62	17.65
M_{ZTC} (N=8)	35	10
M_1(N=4)	50.6	10
M_2(N=4)	50.6	10
M_3(N=4)	50.6	10
M_4	2.75	0.18
M_5(N=16)	5	5
M_6	2.75	0.18
M_7	2.75	2
M_8(N=2)	1.5	2
M_9(N=2)	1.5	2
M_{10}	1	2
M_{11}	1	2

*N is the multiplier number.

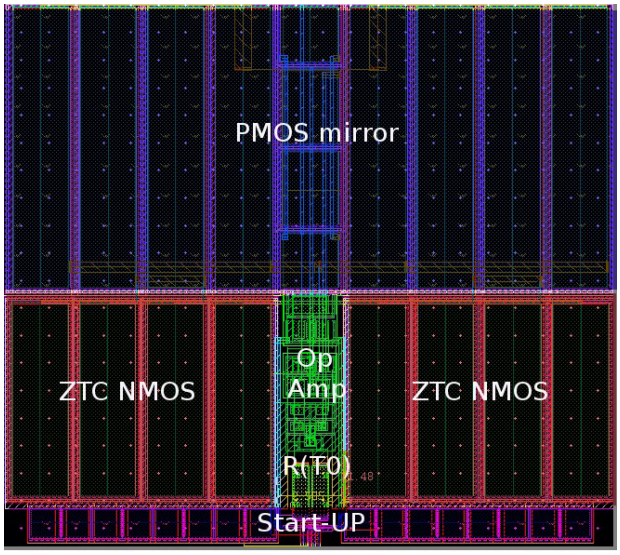

Figure 8. Layout - 100µm X 100µm – 180 nm CMOS Process

V. SIMULATIONS RESULTS

All results presented here were estimated using post-layout extracted parasitic. The circuit was designed to generate 5 μA, and presents a slight curvature due to the nonlinearity of mobility thermal dependence [4], as shown in Fig. 9. The good thermal stability of reference is evident from -45 to +85°C in this Figure. Effective temperature coefficient (TC_{eff}), as given by Eq. (47), is 15 ppm/°C, under V_{DD} = 1.8 V. Power supply sensitivity resulted around 1%/V for a V_{DD} range of 1.4 to 1.8 V, as shown in Fig. 10.

$$TC_{eff} = \frac{I_{REE_{MAX}} - I_{REE_{MIN}}}{I_{REF}(T_0)(T_{MAX} - T_{MIN})} \quad (47)$$

Since the impact of fabrication process is critical for performance repeatability of circuit, Monte Carlo

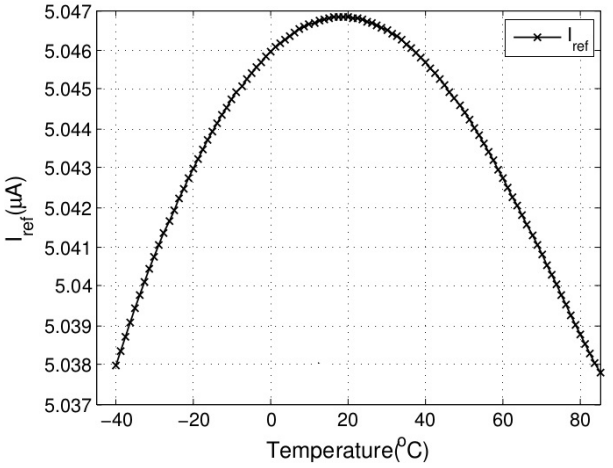

Figure 9. Current Reference vs. Temperature.

(MC) simulation was done separately only for local mismatch effects and for average process variations including mismatch, with 1000 runs each. For average process MC, all similar devices are changed in the same way for each run. For local mismatch MC, parameters of each transistor is changed individually for each run. Fig. 11 shows the reference current spread, with a σ/μ = 4.5% for mean process variation + mismatch, while only local mismatch is shown in Fig. 12, and yields σ/μ = 0.65%. From these simulations, one can conclude that average process variations (batch-to-batch) is the main yield reduction cause.

Fig. 13 presents the spread of effective temperature coefficient (TC_{eff}) for average process variations and mismatch, where 98 % of parts yields a TC_{eff} below 100 ppm/°C. Fig. 14 presents the same spread but only for local mismatch, where all parts have TC_{eff} < 60 ppm/°C. Clearly, the factors, which are the major contributors to spread, are average process variations (batch-to-batch).

Table III presents a comparison of recently published current references. Clearly main advantages of our new topology are competitive area and low temperature coefficient.

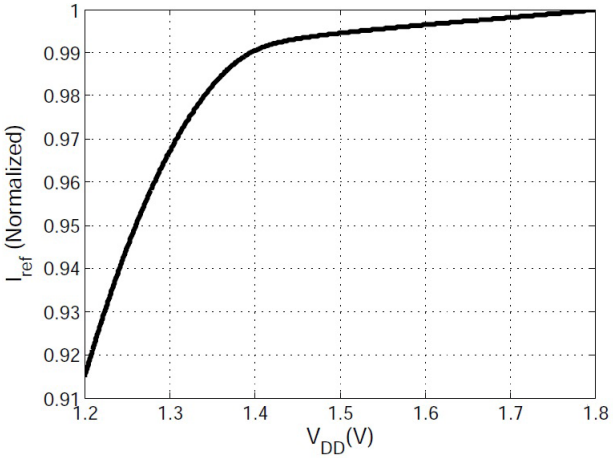

Figure 10. Normalized Power Supply Sensitivity. ($\frac{I_{REF}}{I_{REF@V_{DD}=1.8}}$)

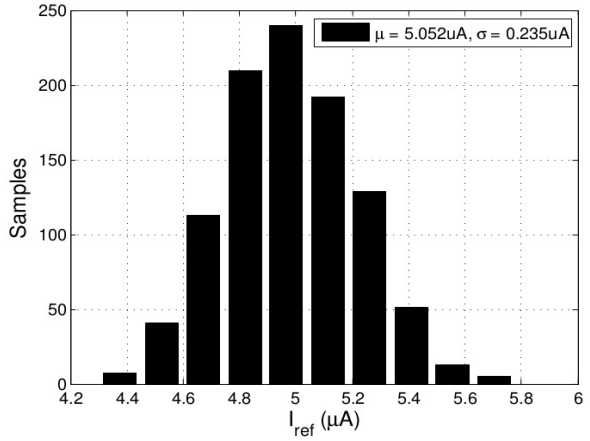

Figure 11. I_{REF} Monte Carlo simulation including process and mismatch.

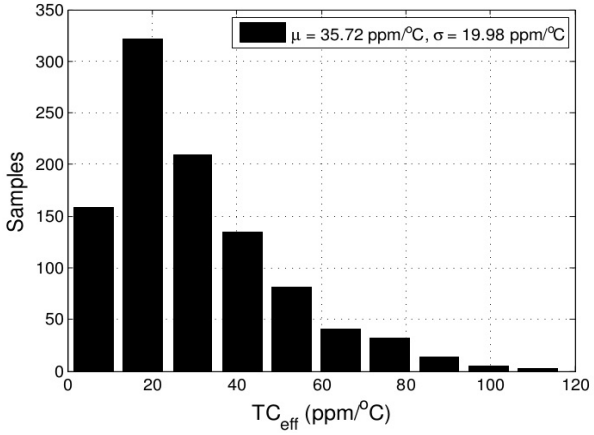

Figure 13. TC_{eff} Monte Carlo simulation including process and mismatch.

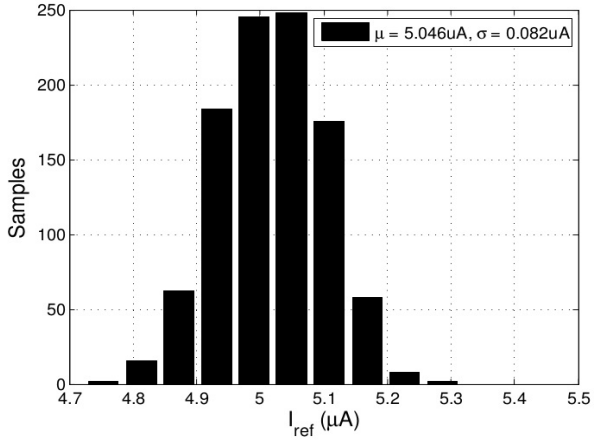

Figure 12. I_{REF} Monte Carlo simulation only for mismatch.

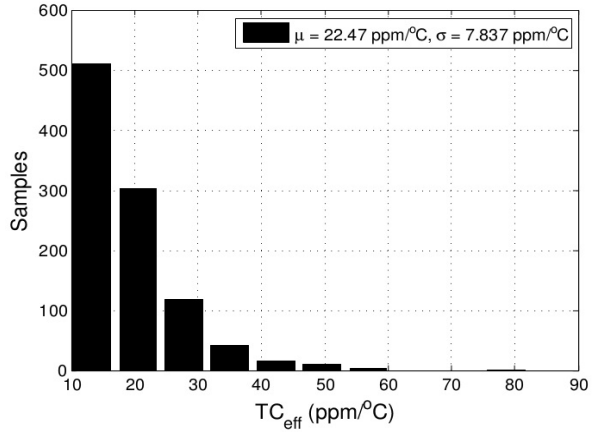

Figure 14. TC_{eff} Monte Carlo simulation only for mismatch.

Table III. Comparison of CMOS Current References

Specification	**This Work***	[6]* - I	[6]* - II	[2]**	[8]*	[9]*	[3]**	Unit
Technology	**0.18**	0.35	0.35	0.18	0.18	0.065	1.5	µm
Temperature	**-40 to 85**	-30 to 100	-30 to 100	0 to 100	-20 to 120	-40 to 125	-20 to 70	°C
Power Supply	**1.4 - 1.8**	N/A	N/A	1	2	3.3	1.2	V
I_{REF}	**5**	15.1	13.65	144	263.5	6.45	0.0004	µA
Temperature Coefficient	**15**	130	28	185	170	55	2500	ppm/°C
Power	**342**	N/A	N/A	227	80	155	0.002	µW
Area	**10000**	4200	4200	315000	N/A	N/A	45000	µm²

VI. CONCLUSION

A new analytical approach for ZTC MOSFET condition was presented using an all-region model, since this effect could occur from moderate to strong inversion levels, depending on process characteristics. Simulation data from different threshold MOSFETs from three commercial processes (350, 180 and 130 nm, from 3 different foundries) shows that ZTC bias point is located from moderate to strong inversion, as predicted analytically. A self-biased CMOS current reference topology was also proposed and designed herein, based on MOSFET ZTC, composed by MOSFETs and one poly-silicon resistor. Proposed circuit was designed in a 180 nm process, for an average current of 5 μA at room temperature under a power supply higher than 1.4 V. Post-layout simulation for typical device parameters resulted an effective temperature coefficient of 15 ppm/°C from -45 to +85°C, and a maximum of 100 ppm/°C for the same temperature range including process and mismatch variability effects. Monte Carlo simulations show a spread of σ/μ = 4.5 % for average process variation and mismatch σ/μ = 0.64 % only for local mismatch. Power consumption is 342μW and silicon area taken by our circuit is just 0.010 mm².

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