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A mixed-signal ASIC for time and charge measurements with GEM detectors

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Fabio Cossio
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Summary

A novel lightweight detector based on CGEM (Cylindrical Gas Electron Multiplier) technology has been developed to replace the aging inner tracker of the BESIII Spectrometer, an experiment carried out at the Beijing Electron Positron Collider in China. The CGEM-IT (CGEM Inner Tracker) consists of three independent layers of cylindrical GEM and, thanks to its fast response, low material budget, high rate capability and excellent radiation tolerance, will provide an improved spatial resolution along the beam axis and the required performance for the entire experiment lifetime. In order to face the unprecedented challenge of achieving high level tracking performance in a strong magnetic field (1 T) with a cylindrical GEM detector, an analogue readout, implementing charge centroid and μTPC (micro Time Projection Chamber) reconstruction algorithms, has been adopted. Compared to a binary readout, this approach allows to reduce the total number of channels to about 10000 which are readout by a dedicated Application Specific Integrated Circuit (ASIC) providing simultaneous measurement of the input signals time-of-arrival and deposited charge.

The chip comprises 64 independent channels, each of which featuring an analogue front-end for signal amplification and conditioning followed by a versatile back-end for the digitization of the event timestamp and input charge. The design of the analogue front-end has been driven by the requirements set by the detector. The ASIC is thus optimized for the readout of signals up to 50 fC, with a maximum event rate of 60kHz per channel and a noise below 2000 electrons r.m.s. for an input capacitance up to 100 pF. A dual-branch architecture, with different peaking time shapers, is employed in order to provide time and charge measurement with the required resolution. The event timestamp is digitized by low-power, quad-buffered TDCs, based on analogue interpolation, delivering a sub-50 ps time binning. In default operation mode, the charge information is extracted by a Sample-and-Hold (S&H) circuit, working as a digitally-controlled peak detector, that allows to capture the voltage peak at the output of the slower shaper. This value is then digitized by a 10-bit Wilkinson ADC which is shared with the TDCs.

In order to extend the input dynamic range and overcome the potential saturation of the measurement provided by the S&H circuit, the charge information can also be inferred from the Time-over-Threshold measurement. The ASIC has been fabricated in a cost-effective and well-established 110 nm CMOS technology node, which is largely adopted for radiation detection in particle physics. A first silicon iteration allowed to fully characterize the chip and correct some design weaknesses before the ASIC was submitted for the mass production. In view of the 2020 installation, integration tests with the CGEM-IT detector coupled with the full-chain readout electronics are now ongoing.

This thesis describes and discusses the design and characterization of a mixed-signal ASIC for the readout of the CGEM-IT and is organized as follows.

Chapter 1 reports a brief description about the BESIII experiment, discussing some details of the detector system and providing some motivations for the CGEM-IT upgrade. The main features and innovations of the CGEM-IT project are described. Moreover, an overview of the full-chain readout electronics is given.

The basic features of a typical front-end ASIC for a particle detector are described in Chapter 2. The main building blocks of the system are discussed, following the signal path: after its formation in the sensor, the signal is amplified and shaped by the analogue front-end and then, before being transmitted off-chip, discriminated and, eventually, digitized. In the last part of this chapter several readout architectures are illustrated, providing for some of them an example of practical implementation.

In Chapter 3 the design and functionality of each block of the ASIC described in this thesis, from the analogue front-end amplifier to the digital controller, are discussed in detail and supported by computer simulations results. Chapter 4 presents the results from the ASIC electrical characterization, showing its full functionality, and from two beam tests which have been carried out to confirm the suitability of this chip for the readout of GEM detectors.

Keywords: ASIC; Readout electronics; Mixed-signal design; Charge and time measurement; BESIII; GEM.

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Chapter 1

Introduction

1.1 The BESIII Experiment

The Beijing Spectrometer III (BESIII) is a multi-purpose detector running at the e^+e^- collider BEPCII (Beijing Electron and Positron Collider) of the Institute for High Energy Physics (IHEP) in the People's Republic of China (PRC). The collider operates in the τ-charm threshold energy region between 2 GeV and 4.6 GeV with a designed peak luminosity of $10^{33}\text{cm}^{-2}\text{s}^{-1}$ [1]. Electrons and positrons are injected in two storage rings (237.5 m in circumference) using a 202 m long LINAC, which accelerates electrons and positrons up to 1.89 GeV (see Figure 1.1).

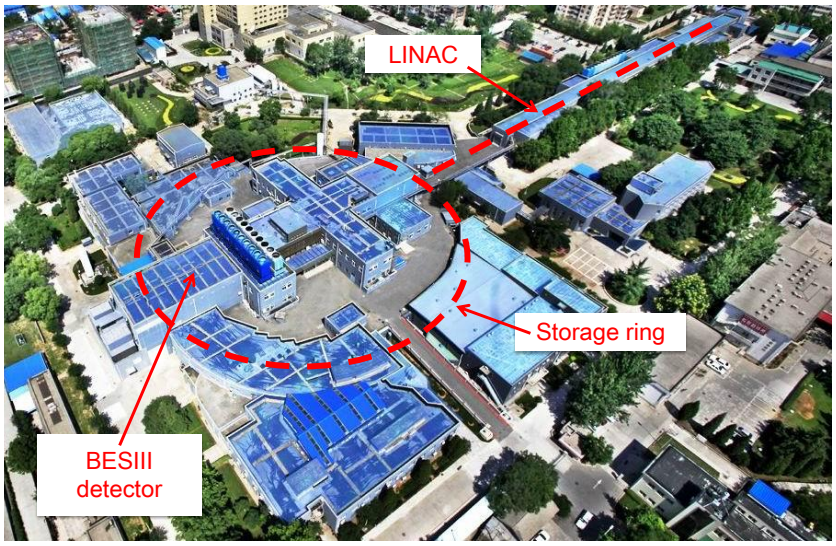


Figure 1.1: Aerial view of BEPCII and BESIII.

BESIII has been successfully running since 2008 and features a rich physics program studying strong, electromagnetic and weak interactions. The J/ψ high production rate in electron-positron collisions makes it suitable for studies on exotic hadrons composed of light quarks and gluons, which are the keys to understand the nature of the strong interaction [2].

1.1.1 BESIII detector

The BESIII detector, depicted in Figure 1.2, is located at the interaction point of the two pipe rings. It has a geometrical acceptance of 93% of the solid angle and can be divided in the following sub-detectors [3]:

- The **Multi-layer Drift Chamber** (MDC) is the tracking system of the detector and provides a spatial resolution of $\sigma_{r\phi} \approx 120$ µm and $\sigma_z \approx 2$ mm and a momentum resolution of $\sigma_p/p \approx 0.5\%$ at 1 GeV/c. The MDC is made of 43 sense wire layers, with the first 8 defining the inner MDC.

- The **Time-Of-Flight** (TOF) detector is composed by two layers of 88 scintillating bars in the barrel region. A recent upgrade of the TOF endcaps has been carried out featuring the installation of 36 overlapping trapezoidal-shaped Multi-gap Resistive Plate Chambers (MRPC) for each endcap [4]. The TOF detector allows to extract the time information of the crossing particles with a time resolution of about 80-90 ps.

- The **Electromagnetic Calorimeter** (EMC) consists of 6240 CsI(Tl) crystals arranged in a cylindrical shape and two endcaps. It provides the energy information with a resolution of 2.5% in the barrel and 5% in the endcaps at 1.0 GeV. This measurement, combined with the TOF system time information, allows for the particle identification (PID).

- A **solenoidal superconducting magnet** provides a uniform 1 Tesla magnetic field, thus allowing to measure the basic particles momentum. Its steel flux return yoke acts as a hadron absorber allowing for hadron-muon separation and provides as well the support for the spectrometer components.

- Outside the superconducting solenoid, several arrays of **Resistive Plate Chambers** (RPC) allow to identify muons and separate them from charged pions, other

hadrons and backgrounds. There are nine layers of RPCs in the barrel and eight in the endcaps.

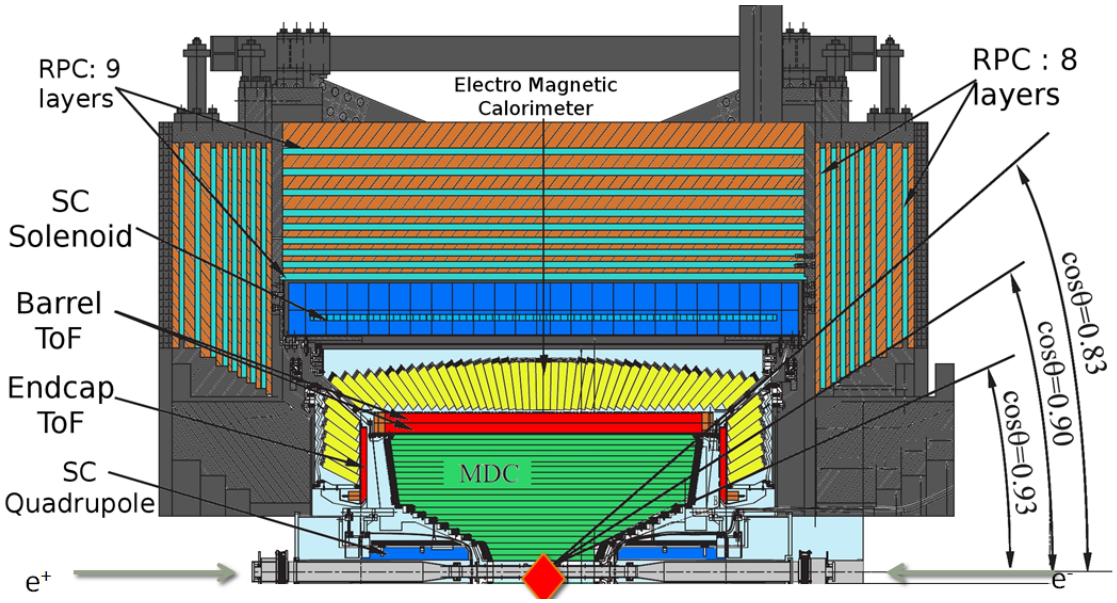


Figure 1.2: The BESIII detector [1].

1.1.2 BESIII trigger and DAQ systems

The trigger, data acquisition and online computing systems can accommodate multi-beam bunches separated by 8 ns. Fully-pipelined electronics allows to achieve an almost zero dead-time operation.

The trigger system diagram is shown in Figure 1.3. It comprises a hardware trigger level (L1) and a software trigger level (L3). The sub-detector signals used for the L1 trigger generation are first processed in the four sub-system modules and then transmitted, via optical links, to the L1 trigger crates where they are analyzed providing hit patterns, track segment finding, clusters and total energy. These sub-triggers are sent to the Global Trigger Logic for the generation of the final L1 trigger signal (see Figure 1.4). L1 signals, together with the system clock and other control commands, are transmitted to the Fast Control system in order to be distributed to the readout electronics crates of the sub-detectors via optical links.

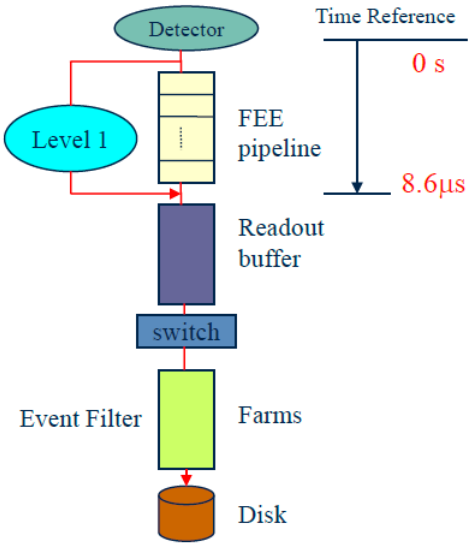


Figure 1.3: Data flow diagram of the L1 and L3 trigger.

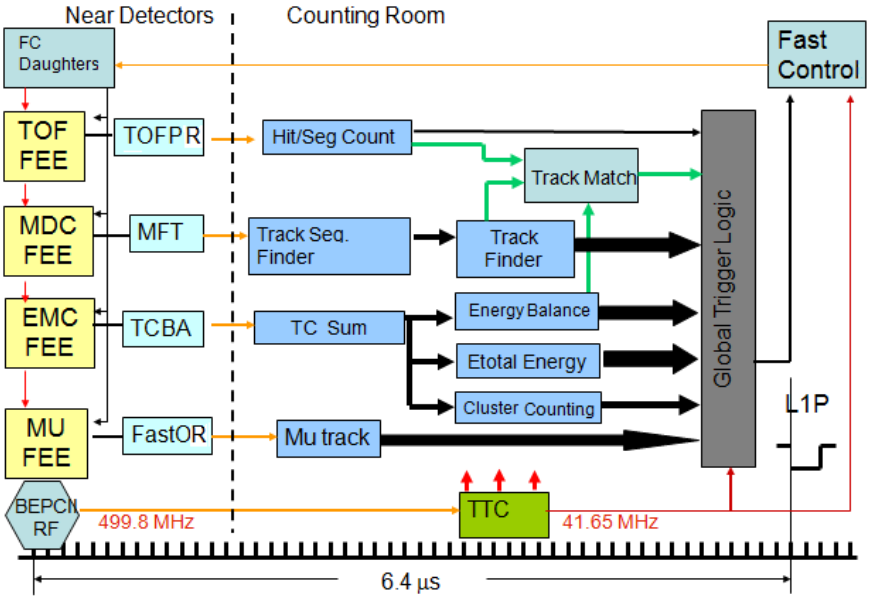


Figure 1.4: Block diagram of the L1 trigger system.

The trigger system and the sub-detectors readout electronics crates employ an 8-bit counter to count the L1 signals for event numbering and synchronization purposes. After the 256th L1 signal, the trigger system generates one CHK signal which is transmitted to the readout modules to check if the number of generated and received L1 signals is

the same. If the internal counter of each readout module is zero the data acquisition can continue, otherwise it needs to be stopped.

The L1 trigger allows to select good physics events with high efficiency while reducing the cosmic ray (2 kHz) and beam (20 MHz) related backgrounds to a level smaller than the 2 kHz physics event rate. This results in a designed L1 trigger maximum rate of 4 kHz.

The BESIII DAQ system is based on VME and online computer farm designed to read large amounts of data from the front-end electronics system and record valid data on permanent storage devices. At the reception of an L1 trigger, which is generated 8.6 μs after the collision, the DAQ system transfers the event data stored in the VME crates buffers to the online computer farm where the data are merged, forming complete events, and then filtered for background suppression (L3 trigger).

In addition, a detector control system (DCS) allows to monitor the environmental parameters of the system, such as temperature, humidity and radiation, as well as the performance of the spectrometer and accelerator itself, such as the status of the detector high voltage and gas systems, providing safety interlocking among sub-detectors and between the detector and the accelerator.

1.2 The CGEM-IT project

BESIII will run at least until the year 2024, and more likely until 2027. In order to guarantee optimal physics performance for the full experiment lifetime, the inner MDC needs to be replaced because of its aging induced by radiation damage [5]. Figure 1.5 shows the relative gain at which the MDC layers have been operated in the past years. In order to compensate the increment of sparks rate caused by the aging, the innermost layers are operated at lower relative gains and every year these effects become more relevant.

In 2014, an innovative solution featuring a lightweight tracker based on Cylindrical Gas Electron Multiplier (CGEM) technology was proposed by the Italian collaboration in BESIII and boosted by a INFN (Italian National Institute for Nuclear Physics) - IHEP (Chinese Institute of High Energy Physics) network. The project was funded by the European Commission within the H2020-RISE-MSCA-2014 framework and involved, apart from INFN and IHEP, also institutes from Mainz and Uppsala Universities.

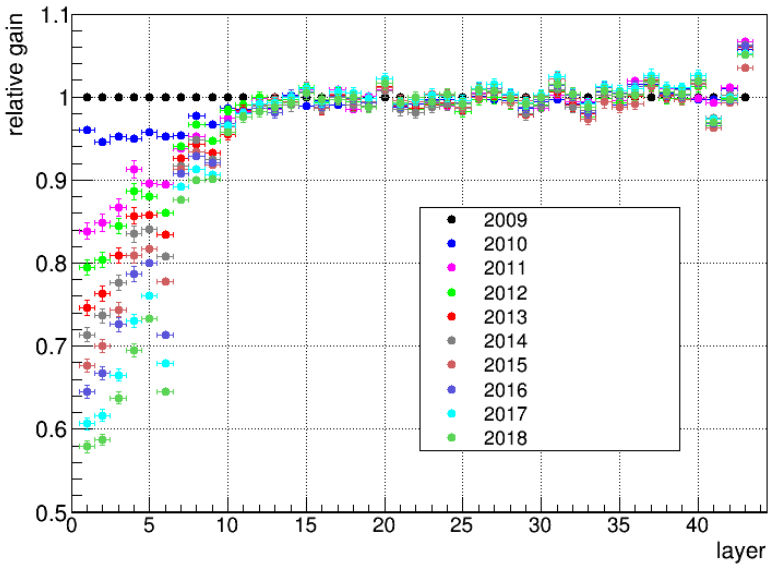


Figure 1.5: MDC gain loss in the 10-year BESIII operation.

1.2.1 Gas Electron Multiplier detectors

The Gas Electron Multiplier (GEM) is a gaseous detector invented in 1997 by F. Sauli [6]. A GEM foil is a metal coated polymer (typically 50 µm kapton + 3 µm copper), pierced with holes of ∼50 µm diameter (see Figure 1.6). A voltage of some hundreds of Volts is applied between the two copper layers to create an intense electric field (some tens of kV/cm) inside the holes. Electrons released by the primary ionization particle are attracted into the holes, where the charge multiplication occurs. The gas mixture typically is composed of Ar-CO_2 or Ar-iC_4H_{10} (Isobutane). Argon is the main gas (70-90%) enabling the ionization, while CO_2 and Isobutane serve as the quenching gases to lower the discharge risk.

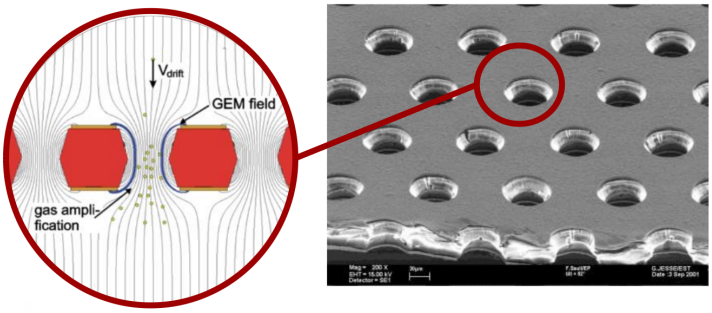


Figure 1.6: Details of a GEM foil.

Several GEM foils can be placed at short distances (typically 1–2 mm) distributing the gas amplification among several stages in order to increase the total gain while reducing the discharge probability. The triple-GEM configuration shown in Figure 1.7 (left) allows to reach gains up to some 10^4 and has been extensively adopted in High Energy Physics experiments. Its typical response is displayed in Figure 1.7 (right) where the current induced by an electron on one strip has been evaluated using Garfield++ [7] simulations. This toolkit allows for a detailed computational simulation of gaseous sensors, taking into account many phenomena that occur inside the detector, such as gas ionization, electrons diffusion (in the gas medium) and amplification (in the GEM holes) and signal induction.

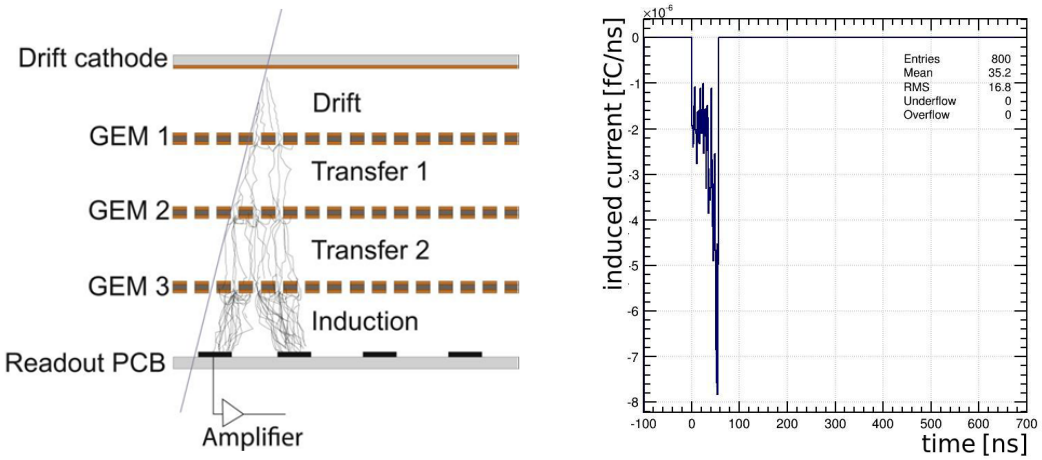


Figure 1.7: Schematic representation of the signal formation inside a triple-GEM (left) and Garfield++ simulation of the current induced by an electron on a strip as a function of the time (right) [8].

Compared to other drift devices, such as the currently operating MDC, this kind of detector offers better resistance to discharge and radiation damage. In addition, since the signal is produced only by electrons, and not from ion motion, higher operation rates can be achieved, without trading in terms of resolution. Therefore, thanks to their good spatial resolution, high particle flux, large area coverage, low material budget, favorable cost-effectiveness and high radiation tolerance GEM detectors are suitable for precise tracking in areas close to beam collisions.

1.2.2 The CGEM-IT detector

The CGEM-IT (Cylindrical Gas Electron Multiplier Inner Tracker) detector is the proposed upgrade of the BESIII inner tracker and is shown in Figure 1.8. The installation of the new detector is scheduled to take place in 2020. A detailed description of its design is given in [9].

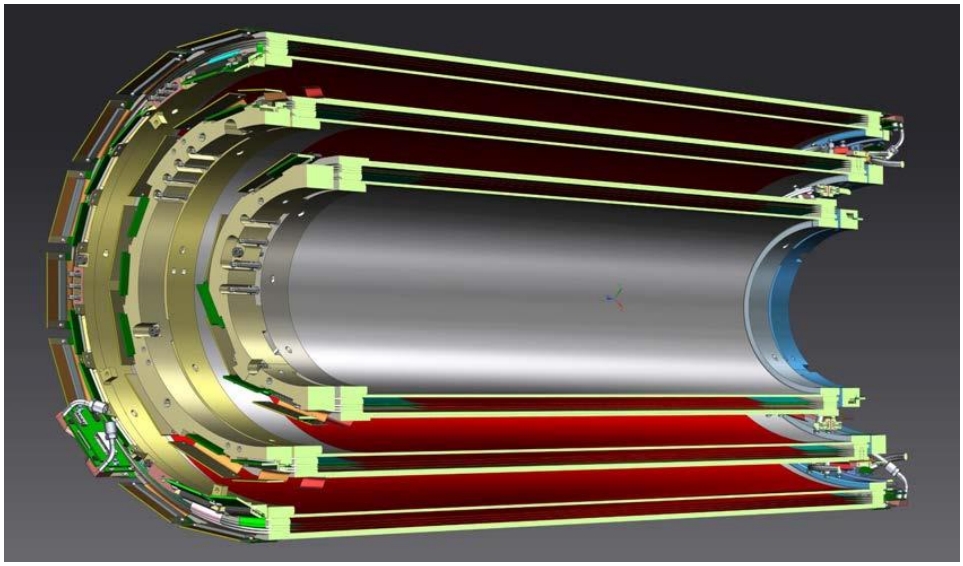


Figure 1.8: 3D view of the CGEM detector mechanical drawings.

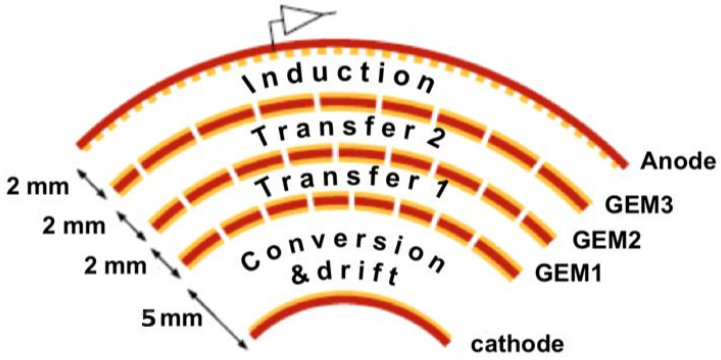


Figure 1.9: Schematic view of the BESIII Cylindrical triple-GEM.

The CGEM-IT comprises three independent concentric layers, covering 93% of the solid angle. Each layer is a Cylindrical triple-GEM detector and its configuration, shown in Figure 1.9, consists of a cathode, three GEM foils and a readout anode, where the

signal induced by the electron motion in the last gap is collected by bi-dimensional strips with a novel XV anode readout plane (see Figure 1.10). The X strips, parallel to the CGEM-IT axis and the beam pipe, provide the information of the $r\phi$ coordinates, while the V strips have a stereo angle between 33° and 43° with respect to the X strips and provide, together with the other view, the z coordinate.

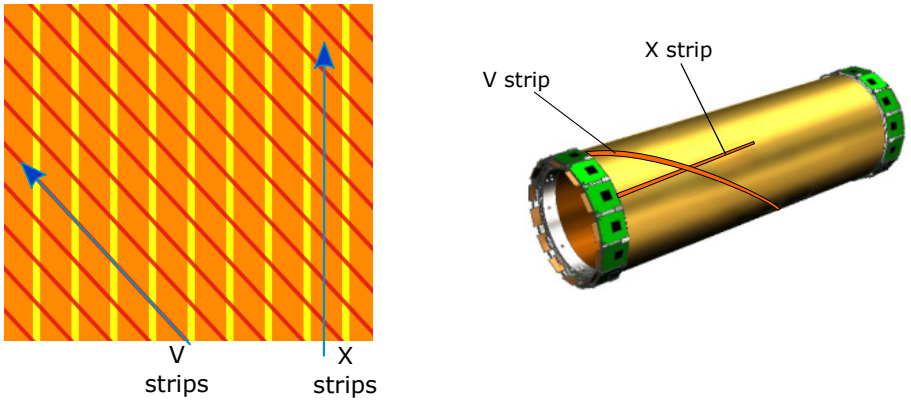


Figure 1.10: XV strips layout: the strips parallel to the cylinder axis (X-strips) are 570 µm wide, while the width of the V-strips is only 130 µm.

The design of the CGEM-IT took advantage from previous experience with cylindrical GEM employed as tracking system in KLOE-2 experiment [10], introducing several innovations in order to meet the requirements, from both mechanical and physics performance points of view, set by the BESIII Experiment, which are reported in Table 1.1.

Parameter	**Value**
Rate capability	10 kHz/cm^2
Efficiency	98%
$\sigma_{r\phi}$	130 µm
σ_z	1 mm
σ_{p_t}/p_t	0.5% at 1 GeV/c
Geometrical acceptance	93% 4π
Material budget	<1.5 X_0
Inner radius	78 mm
Outer radius	178 mm

Table 1.1: Design specifications for the CGEM-IT.

Compared to the KLOE-2 design, the CGEM-IT features the following innovations:

- In the KLOE-2 experiment the mechanical structure was realized with Honeycomb foils on the anode and cathode electrodes and a permaglass ring at the edges of the detector. For BESIII, the use of a very light mechanical structure based on Rohacell reduces the material budget of the detector [11]. In addition, the thickness of the GEM foils copper faces has been decreased from 5 to 3 μm, thus allowing to further reduce the detector radiation length to about 1% of X_0
- An analogue readout enabling charge centroid and μTPC reconstruction algorithms (refer to 1.2.2) has been chosen since it allows to achieve a better spatial resolution compared to the one provided by a digital readout, which is limited by the strips pitch dimensions. This choice relaxes the requirements concerning the number of channels to be readout: with a strip pitch of 650 μm the number of channels is reduced to ∼10000 [12].
- The drift gap has been increased from 3 mm to 5 mm in order to enhance the number of electrons from primary ionization, thus improving the performance of the position reconstruction algorithms: a larger gap provides more points for the μTPC technique and thus a better spatial resolution [8].

Thanks to the aforementioned innovations, the new detector will match the requirements for the momentum (σ_{p_t}/p_t) and radial ($\sigma_{r\phi}$) resolution and will improve by at least a factor of 2 the resolution along the beam axis (σ_z). This will enhance the performance of BESIII in reconstructing primary and secondary vertices, thus leading to a better background rejection and an improved efficiency for rare decays [13].

Reconstruction algorithms

The measurement of both the time and the charge information of the CGEM signal collected on the anode strips enables the use of two algorithms to reconstruct the position of the impinging particle: the Charge Centroid (CC) and the micro-Time Projection Chamber (μTPC) readout. The performance of the two methods depends strongly on the shape of the charge distribution on the readout plane.

The charge centroid method determines the position x of a charged track on the anode by means of the weighted average of the fired strip positions x_i:

$$x = \frac{\sum_i x_i q_i}{\sum_i q_i} \tag{1.1}$$

where the weights q_i correspond to the charge collected by each fired strip (see Figure 1.11).

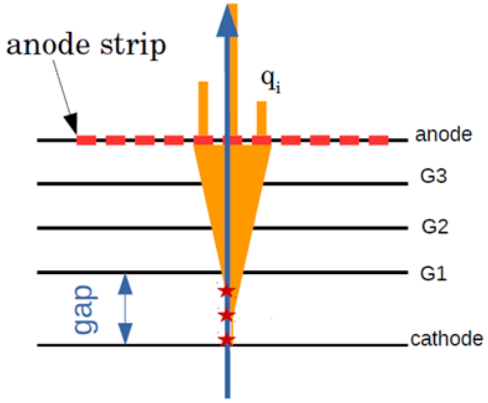


Figure 1.11: Representation of the charge centroid algorithm.

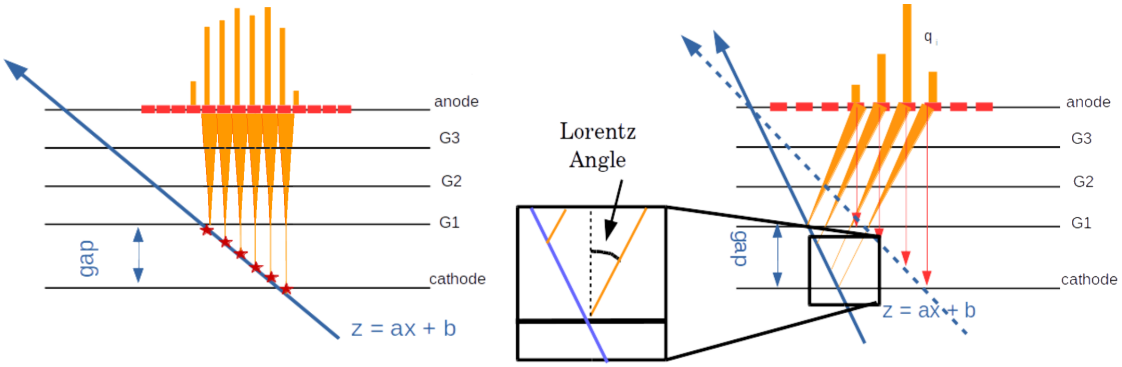


Figure 1.12: Representation of the μTPC algorithm for angled tracks without (left) and with (right) the presence of magnetic field.

The CC algorithm provides a good spatial resolution with orthogonal tracks producing a Gaussian-shaped charge distribution, while its performance degrades in presence of high magnetic fields or non-perpendicular tracks. To overcome this issue a new reconstruction algorithm, named μTPC, has been developed [14], [15]. Shown in Figure 1.12, this technique allows to reconstruct the 3-dimensional particle position as in a Time Projection Chamber but within the few millimeters of the drift gap. By measuring the time of arrival of the signal on each strip and by knowing the electron drift velocity in the gas mixture it is possible to calculate the direction of the incident particle and then extract the position of the primary ionization point.

In Figure 1.13 the drift time distribution is reported for an event in which eight strips are hit and for which the charge distribution on the anode is no more Gaussian, making the CC method totally unusable. Knowing the coordinate x_i of each strip, the position of each primary ionization z_i perpendicular to the strip plane is obtained from the time measurement using the electron drift velocity. The (x_i, z_i) points are then fitted with a linear function $z = ax + b$ and the position is extracted in the middle of the gap in order to minimize the errors [8] as:

$$x = \frac{\frac{gap}{2} - b}{a} \tag{1.2}$$

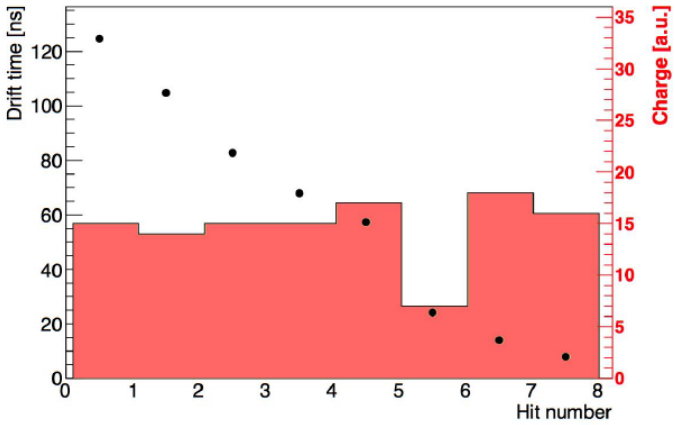


Figure 1.13: Drift time distribution as a function of hit strips (points). The histogram represents the charge distribution, which is no more Gaussian for this particular event [13].

The whole procedure is possible if the time resolution of the detector is good enough (<10 ns) to resolve the arrival times of the avalanches from different primary electrons, and with a highly segmented readout plane.

A merging algorithm to weight the contribution of these two anti-correlated methods has been developed in order to grant the required spatial resolution of 130 μm for the different angular regions (see Figure 1.14) and thus provide a unique measurement to track the particles with the triple-GEM detector inside the BESIII spectrometer [8].

For the CGEM analogue readout a dedicated multi-channel Application-Specific Integrated Circuit (ASIC) has been developed. The chip, named TIGER (Turin Integrated Gem Electronics for Readout), features 64 parallel channels that extract and digitize the amplitude and time-of-arrival of the input signals coming from the CGEM detector. The ASIC design and characterization will be described in detail in Chapter 3 and

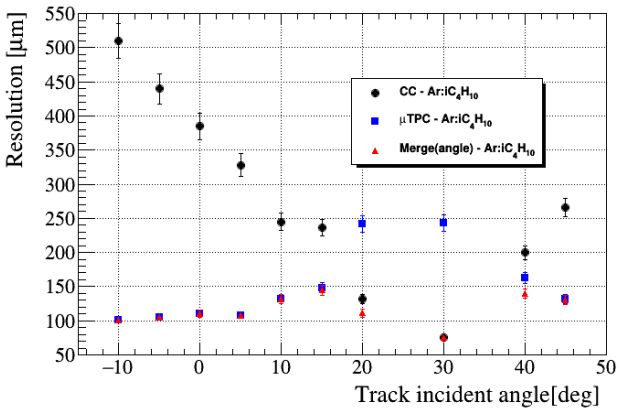


Figure 1.14: Spatial resolution for different incident angle in presence of magnetic field using the two reconstruction algorithms [8].

4, respectively. In the next section, an overview of the CGEM-IT readout electronics is given, discussing the main feature of each block composing the full-chain, from the on-detector front-end ASIC to the off-detector VME-based data collectors.

1.2.3 Overview of the CGEM-IT readout electronics

The general scheme of the CGEM-IT electronics is shown in Figure 1.15. The readout chain can be divided in 2 main blocks: the on-detector and the off-detector electronics.

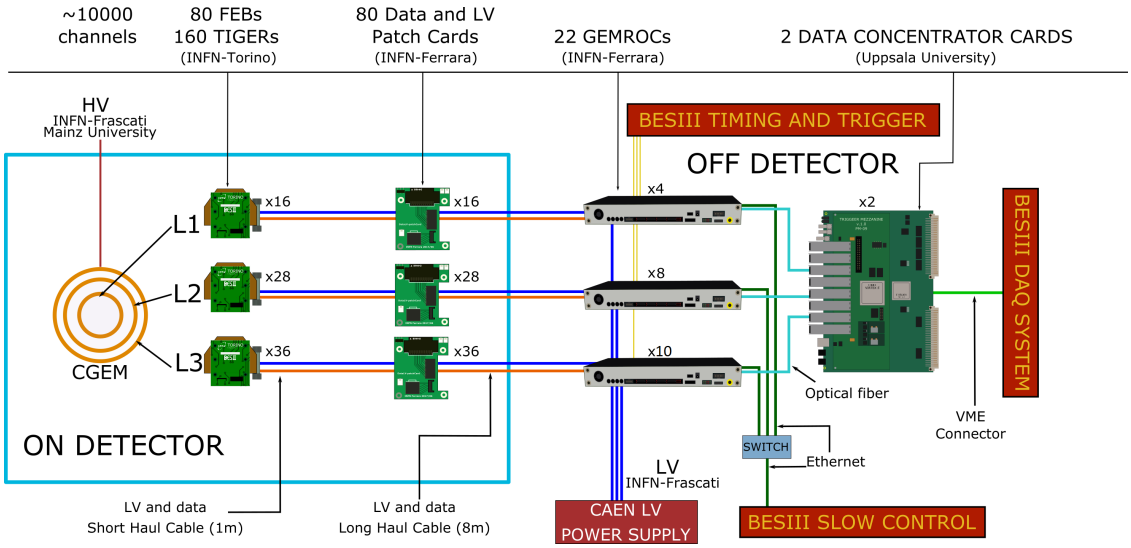


Figure 1.15: General scheme of CGEM-IT electronics.

On-detector electronics

The on-detector electronics includes the Front-End boards (FEBs) that host the TIGER custom ASICs. The limited space available in the inner part of the BESIII spectrometer called for a compact design of the boards [16]. Each FEB, shown in Figure 1.16, can accommodate two 64-channel chips and consists of a stack of two printed circuit boards (FE1 and FE2). The two ASICs are bonded on the analogue-most layer (FE1), where power regulators and SMD voltage divider circuits are used to properly bias the chips. Each channel input features an ESD protection network to prevent potential damage caused by the detector discharges. The interface towards the anode is provided by a Hirose FX10A-144S-SV connector. The digital-domain FE2 hosts the LVDS buffers and provides interface to the off-detector electronics for data (ERNI SMC-B26 connector) and power (MOLEX 504050-0691 connector). The two layers of the FEB are connected together through a HIROSE DF12-60DS-0.5V connector [17].

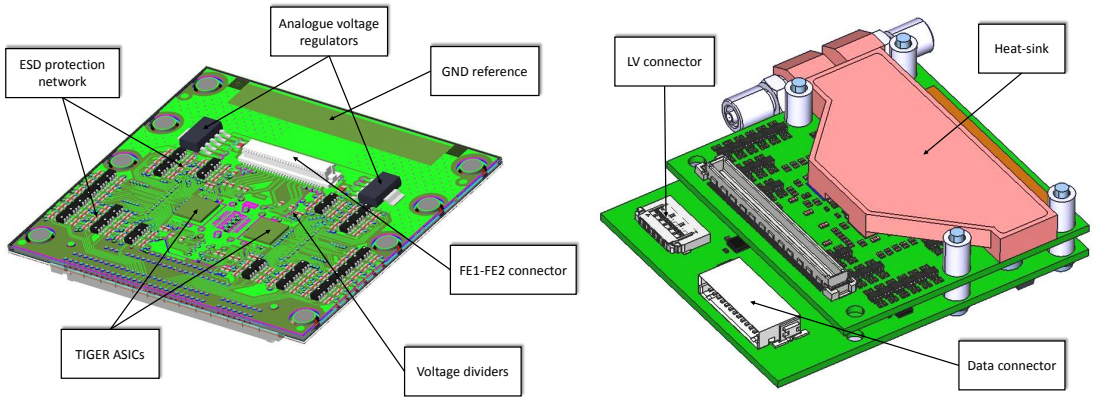


Figure 1.16: Front-End Board design for the CGEM-IT Layer 1: top-side routing on FE1 (left) and FE1/FE2 assembly with liquid cooling heat exchanger plate (right).

A copper heat-sink is mounted on the external side of FE1 to cool-down the electronics and keep the temperature stable by means of a closed circuit water-cooled system based on a SMC-HRS012 Thermo-chiller [18] and represented in Figure 1.17.

The different space available for the FEBs in the three layers of the CGEM-IT (see Figure 1.18) required a different and even more compact design for the L3 FEBs. The layout and routing have been completely revised in order to fit the same components in a smaller area. A size comparison of the FEBs for different layers is shown in Figure 1.19. This can be seen also in Figure 1.17 by observing the different geometry of the cooling system tubes.

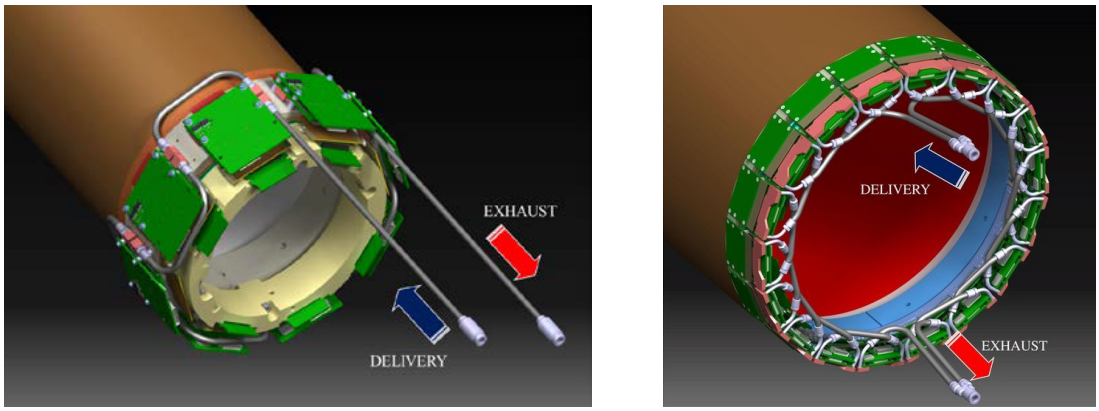


Figure 1.17: 3D view representation of the cooling system for the CGEM-IT Layer 1 (left) and 3 (right).

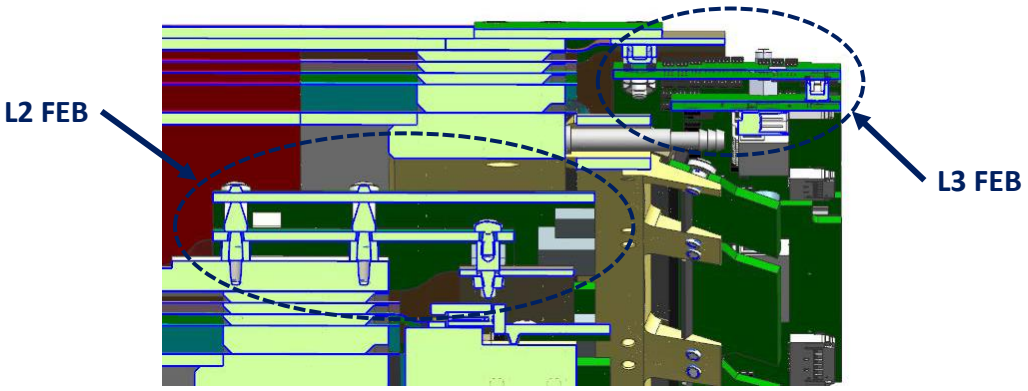


Figure 1.18: Detail of the CGEM mechanical drawing. The very limited space made available for the Layer 3 FEB can be observed in the top-right angle of the figure and compared to the space reserved to the Layer 2 FEB.

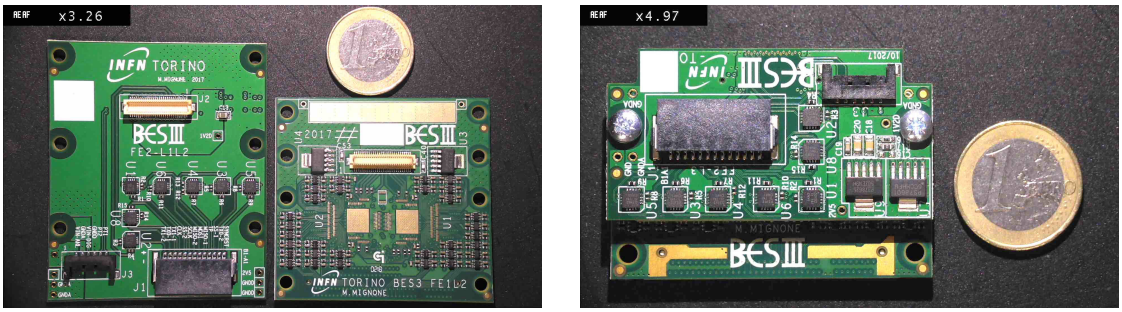


Figure 1.19: Size comparison of the Front-End-Boards for Layer 1 and 2 (left) and Layer 3 (right).

As shown in Figure 1.17, the FEBs are installed at both ends of the detector, with each side reading one half of it. To fully instrument the three layers of the CGEM-IT a total of 80 FEBs (160 TIGER chips) are needed and they are distributed as follows:

- Layer 1: 8 FEBs (16 TIGER) per side
- Layer 2: 14 FEBs (28 TIGER) per side
- Layer 3: 18 FEBs (36 TIGER) per side

The validation and calibration of the chips required to fully equip the detector will be discussed in Chapter 4. The self-triggered readout operation of TIGER implies that every signal above the selected threshold is digitized and sent off-chip to the off-detector electronics where the ASIC raw data are filtered using a time-tag approach based on the BESIII Experiment L1 trigger signal.

Off-detector electronics

The off-detector electronics is mainly composed by two data processing units: the GEM Read-Out Card (GEMROC) module and the GEM Data Collector (GEM-DC).

The GEMROC modules (see Figure 1.20) handle the interface with the on-detector electronics, providing data, configuration and monitoring through LVDS links. They also distribute the power supply coming from the Low-Voltage distribution system to the FEBs.

Each GEMROC module can handle up to four FEBs (8 chips, 512 channels) and is based on an ALTERA Arria V GX FPGA development board [19] coupled to a custom Interface Card (GEMROC_IFC) through an High-Speed Mezzanine Card (HSMC) high

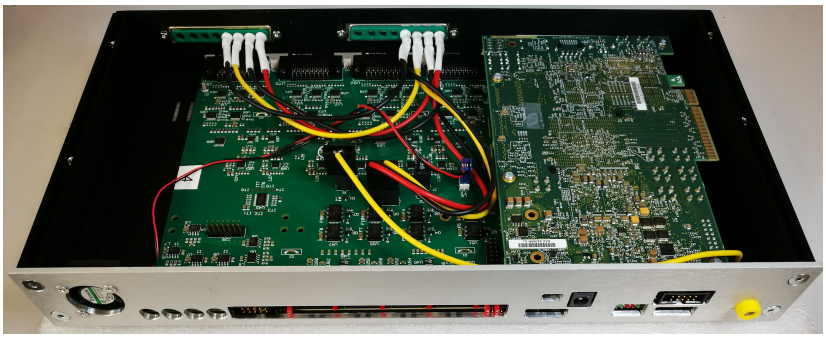


Figure 1.20: A GEMROC module assembled in its aluminum frame. The FPGA is the board mounted on the right.

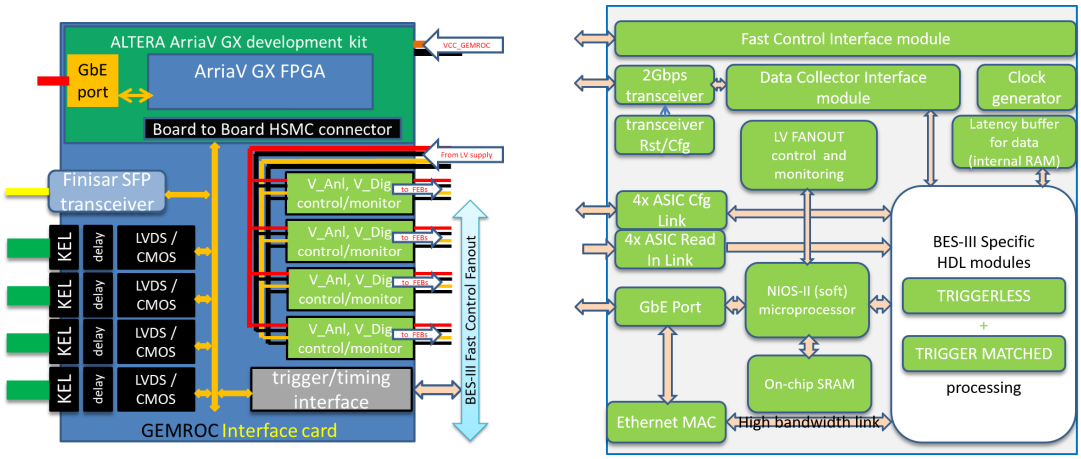


Figure 1.21: Block diagram of the GEMROC hardware (left) and schematic view of the FPGA firmware (right).

performance connector. The Interface Card manages the electrical and physical interfaces to the FEBs, to the GEM-DC and the BES-III Fast Control system (L1 trigger).

A schematic view of the GEMROC hardware is shown in Figure 1.21 (left). Each GEMROC employs four KEL-8822 connectors interfaced with LVDS/CMOS buffers for the communication with the FEBs, while a Finisar SFP transceiver mounted on the interface card handles the communication between the GEMROC and the GEM-DC via optical fiber. The interface card also implements a connector which is used to deliver and share clock and trigger signals between several GEMROCs. A block diagram of the FPGA firmware is displayed in Figure 1.21 (right). It features:

- Clock generation, synchronization (between different GEMROC modules) and distribution to the front-end electronics
- Read and write operations of the TIGER configuration registers
- LV fanout control and monitoring of the TIGER bias voltages and drained currents
- Readout of TIGER raw data
- TRIGGER-LESS and TRIGGER-MATCHED data processing
- Data collector interface to build packets to be sent through Ethernet (UDP communication) or optical connection
- Communication with the PC or BESIII slow control through a GbE port.

Two different readout modes, TRIGGER-LESS and TRIGGER-MATCHED, are implemented in the GEMROC firmware [20]:

- The **TRIGGER-LESS** mode is a standalone mode used for debug and configuration purposes, allowing to perform some scans to determine the optimal parameters for TIGER operation (e.g. threshold scan). The GEMROCs directly communicate with the PC running the acquisition. In this operation mode the device does not perform any data selection, all incoming data are collected from the input buffer and put into packets to be sent to the acquisition PC. A packet is sent after eight TIGER frame-words (8×204.8 µs = 1638.4 µs, refer to 3.3.1) or when the maximum packet size set for the GEMROCs communication (1440 bits) is reached. Data is sent without additional headers or trailers.
- The **TRIGGER-MATCHED** mode is used during physics acquisition runs. Hit data from ASICs are stored on a circular buffer waiting for the BESIII L1 trigger. The operation is shown in Figure 1.22. When a trigger signal is received, data is trigger-matched by reading a fixed number of words from the buffer which include the window of interest (8.6 µs latency, 1.5 µs window-centered), a formatted packet is created for each event with header and trailer words (8 bytes each) for event identification. The first received L1 trigger is used to sync-reset all the chips.

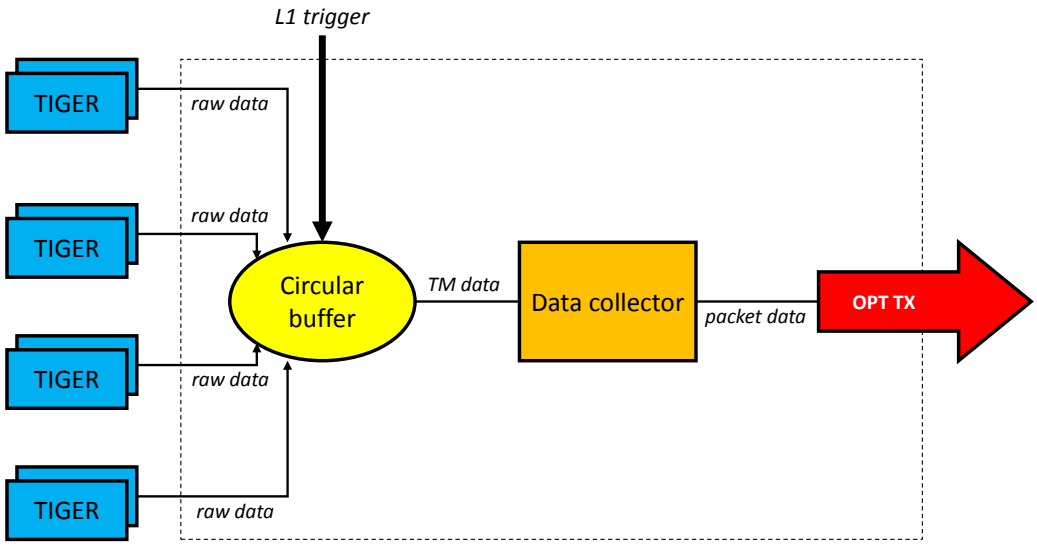


Figure 1.22: GEMROC Trigger-Matched data flow architecture.

Dedicated High-Voltage (HV) and Low-Voltage (LV) power distribution systems, mounted on CAEN SY4527LC and SY5527LC mainframes, are employed to supply the detector and electronics, respectively. The SY4527LC mainframe is equipped with two CAEN A1515CG boards and provides the HV bias to the CGEM detector. The SY5527LC mainframe hosts three CAEN A2519 cards (8 channels, 15V, 5A max) to supply the GEMROC modules and five CAEN A2517 cards (8 channels, 5V, 15A max) to supply the TIGER ASICs through the GEMROC LV power distribution section. The two systems can be controlled remotely via Ethernet and allow for single channel/board current/voltage monitoring and on/off capability.

80 "Data and LV Patch Cards" (DLVPC) are used to interconnect the "short haul" cables (about 1.5 m long) from the 80 TIGER FEBs to the "long haul" cables going to the GEMROC modules. Those boards are used to decouple the arrangement of long and short cables and can also serve as a common ground reference for the system.

To keep each detector layer and its electronics electrically floating with respect to the others a total of 22 GEMROC modules are needed:

- Layer 1: 2 GEMROC per side
- Layer 2: 4 GEMROC per side
- Layer 3: 5 GEMROC per side

The 22 GEMROCs send trigger-matched data to two GEM Data Collector (GEM-DC) modules through optical links running at 2 Gbit/s. These links are bidirectional communication channels and can also be used for ASIC configuration and monitoring. The GEM-DC are based on the VME Advanced Trigger Logic Board (ATLB, [21]), shown in Figure 1.23, and provide the interface between the CGEM-IT electronics and the BESIII Data Acquisition system.

Data coming from the GEMROCs are stored in buffers, events are time sorted and framed by an event builder module and then sent to an output buffer to be finally transmitted through the VME interface to the BESIII main DAQ.

One can estimate the raw data rate coming from one TIGER and, after that, the Trigger-Matched data rate sent by the GEMROCs to the GEM-DC modules. The maximum rate per channel is estimated to be 60 kHz. Each TIGER has 64 channels and

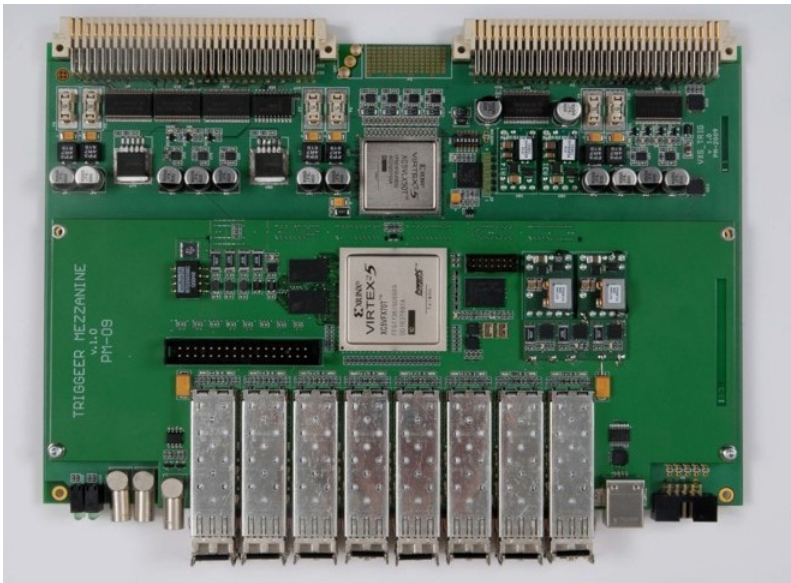


Figure 1.23: Advanced Trigger Logic Board.

generates event words of 64 bits each (80 bits after 8b/10b encoding) which are transmitted, in this application[1], via two Tx links working at 160 MHz in SDR (single data rate) mode. This implies that the maximum data throughput from one chip is expected at around 307.2 Mbit/s, hence two Tx links are barely enough. Nevertheless, the expected hit rate per channel should be lower than the maximum rate. A realistic value (physics + noise) can be set to 25 kHz/ch.

For a rate of 25 kHz/ch (1.6 MHz per chip) we obtain a data throughput of 102.4 Mbit/s from one chip. Considering a trigger-matching time window of 1.5 μs we can expect ∼2.4 hit/packet, where each packet contains also two 64-bit header and trailer words. Each GEMROC reads data coming from 8 TIGER and the maximum L1 trigger rate is designed to be 4 kHz. From these assumptions, the expected trigger-matched data rate at the GEMROC output is about 6 Mbit/s, which is much lower than the limit set by the 2 GHz optical links.

In Trigger-Less acquisition, 8 TIGER produce a data rate of 102.4 MB/s which need to be transmitted via a GbE interface (UDP protocol) for standalone readout. The maximum raw bandwidth of a GbE link is 125 MB/s which is barely compatible with the Trigger-Less acquisition mode requirements. However, it must be pointed out that this mode is a debug/standalone operating mode, in which usually only a subset of the ASICs are

[1]The ASIC has 4 Tx links which can work up to 200 MHz DDR.

selected to be monitored, thus relaxing the bandwidth requirements. Nevertheless, if all chips need to be readout at the same time, a multiplexed readout scheme could be implemented.

Finally, we can calculate the expected Trigger-Matched data bandwidth for the entire GEM detector. The full system comprises 160 TIGER, thus, with the same assumptions we made before, we obtain an event size of about 2-3 kB and thus a data rate of ∼8-12 MB/s.

Chapter 2

Readout ASICs for radiation sensors

The past two decades have witnessed rapid progress in the area of radiation detectors and their readout electronics. Nowadays, Application Specific Integrated Circuits (ASIC) are very common in high-energy physics applications and play a key role in every modern detector system. Different applications may require different readout electronics, nevertheless the IC design features some aspects common to all. Typically, the ASICs comprise an array of identical channels, allowing to readout highly segmented detectors. For each channel the radiation is converted by the detector into an electrical signal whose charge is proportional to the energy deposited inside the detector by the incident particle. After that, it is processed by the front-end electronics performing signal amplification and filtering, analogue-to-digital conversion and high-speed data transmission (see Figure 2.1). Modern front-ends are mixed-signal ASICs able to integrate complex analogue and digital circuits on the same silicon substrate.

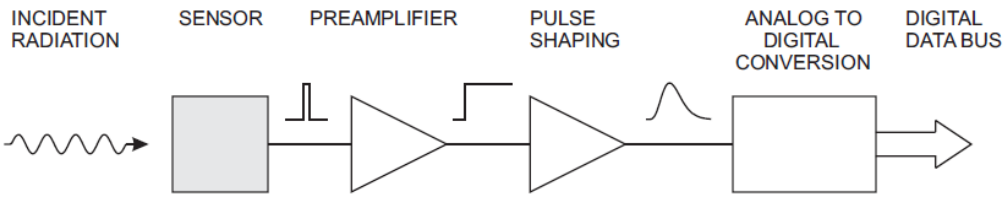


Figure 2.1: Main blocks of a radiation detection system [22].

In this chapter, a review of the components used in the signal processing chain will be provided. The main aspects in designing the front-end blocks performing signal amplification and conditioning are discussed, addressing the key design parameters related

to them. In the second part of the chapter, the most recurrent readout architectures are described, reporting the functionalities of the main building blocks and discussing some practical implementation that played a role in the development of the TIGER ASIC.

The information and topics discussed in this chapter, unless otherwise specified, are taken from [22]–[24].

2.1 Signal amplification and conditioning

The first amplification stage is usually referred as "pre-amplifier" and plays a crucial role in the design of front-ends electronics for radiation sensors. Its response has a great impact on the measurement quality provided by the full system, hence the factors that may limit its performance must be properly studied.

First, the application requirements and the sensor properties need to be carefully investigated and understood. Several parameters play an important role in the design of a front-end:

- the amount of charge released in the detector defines the impact of the signal deterioration due to the presence of front-end noise and external interference;
- the shape and the duration of the detector signal determine the time necessary to collect a suitable amount of charge in the signal integration;
- the rate of interactions defines the number of signals the system has to cope with and thus limits the time available to process the detector signal.

These parameters are used to generate an electrical circuit model which allows to simulate the sensor response with adequate detail. After that, based on the analysis of the circuit specifications and their trade-offs, a suitable front-end architecture is chosen and the design of the building blocks can start.

Some applications may require multi-stage architectures, where the signal processing is split into several stages: after the pre-amplifier input stage, one or more shaper stages are cascaded to improve the flexibility and performance of the front-end electronics.

2.1.1 Signal formation

An optimized readout requires an adequate knowledge of the sensor and of the physical measurement the system is intended for.

The working principle of a ionization chamber is depicted in Figure 2.2. Two conductive plates (electrodes) are kept at different potentials, thus creating an electric field inside the detecting volume. The sensing medium can be a gas, or a gas mixture, but also a semiconductor. For this discussion we will refer to a gas chamber but many aspects apply also for semiconductors.

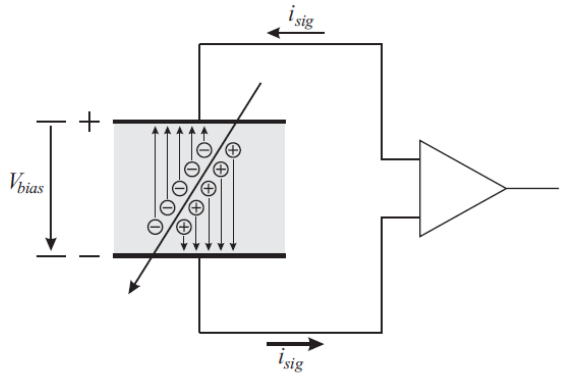


Figure 2.2: General scheme of an ionization chamber [22].

When a charged particle crosses the sensor, it ionizes the gas generating ion-electron pairs. The electric field applied to the sensor drifts the charge carriers towards the electrodes. For gas detectors, the charge generated in the primary ionization is typically too small to be efficiently detected, so it is first transferred to a region where a higher electric field starts the avalanche multiplication process. For instance, in a Gas Electron Multiplier (GEM) detector the avalanche multiplication occurs inside the holes. According to the Ramo Theorem [25], the electrical signal observed by the front-end electronics originates from the induction of the charge carriers that move towards the electrodes. By integrating the signal current it is possible to retrieve the signal charge, which is proportional to the energy released by the impinging particle.

It must be pointed out that in order to measure the total charge all carriers have to be collected. A front-end electronics with an integration time smaller than the detector charge collection time will hence incur in the so called ballistic deficit, where only a part of the charge is measured. The fraction of charge that is lost fluctuates, thus introducing a dispersion in the amplitude of the signal measured at the front-end output.

For instance, in gas detectors the ions low mobility, which can be three order of magnitude smaller than the one of electrons, produces very slow signal components. Some systems, like GEM detectors, address this issue by connecting the front-end electronics only to the electrode where the electrons are collected, so that the ions signals

are not readout.

Since it has an impact on the analogue front-end implementation, it is crucial to model the electrical behavior of the sensor. To draw the detector equivalent circuit one must consider that in real applications one electrode of the detector is connected to a high voltage supply, which is usually filtered to reduce noise, while the other is connected to the front-end amplifier input.

In the configuration shown in Figure 2.3, the negative HV power supply moves the electrons towards the upper electrode. As a consequence the negative charges on this electrode are forced to move towards the amplifier input, generating a negative signal at its input node. Electric circuits models represent a current as a flow of positive charges, hence the electrons flowing towards the amplifier input can be seen as positive charges moving in the opposite direction and they can be represented as a time-dependent current source, whose shape depends on several factors such as the position of charge deposition, the sensor material properties, the applied bias voltage and the detector geometry. The sensor can be thus modeled as a capacitor, with the sensing medium as the dielectric, and with a current source in parallel.

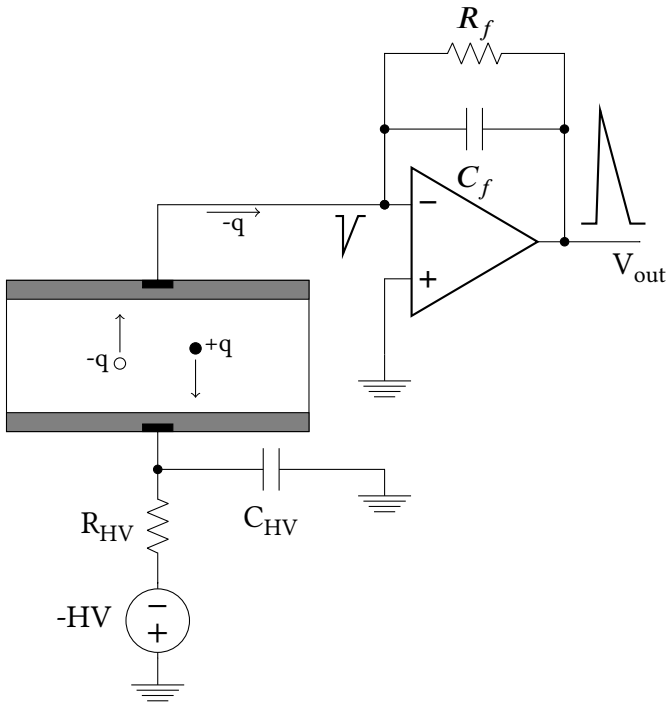


Figure 2.3: Signal collection with negative HV.

2.1.2 Input stage

The "pre-amplifier" provides the electronics interface to the sensor. It must convert the small current signal coming from the detector into a signal suitable for the next stage of the readout chain. It is typically located as close as possible to the detector to minimize the electronic noise introduced by the connection lines from the sensor to the amplifier input.

One of the most used configuration for sensor readout is the charge-sensitive amplifier (CSA), shown in Figure 2.4. It consists of an inverting high-gain voltage amplifier and a feedback capacitor, C_f, connected between the input and the output of the amplifier.

In order to write the transfer function of the pre-amplifier in Figure 2.4 some approximations can be done:

- The detector signal is modeled with a Dirac delta, as $I_{in}(t) = Q_{in}\delta(t)$. By doing this only the information about the total charge contained in the signal is kept.
- The core amplifier is assumed to be ideal, with infinite gain and bandwidth.
- The feedback resistance is chosen large enough so that it does not affect the signal processing. It only serves for establishing the correct DC bias point of the input transistor.

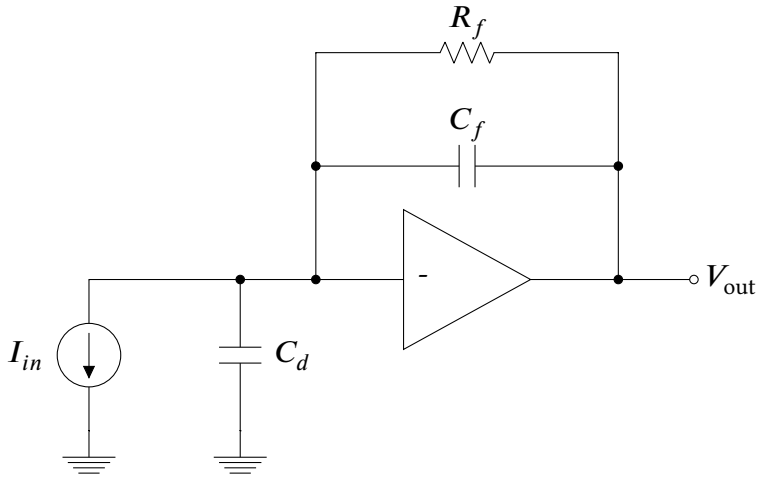


Figure 2.4: Charge Sensitive Amplifier (CSA) schematics.

Under these assumptions the pre-amplifier can be treated as an ideal integrator and

one can write:

$$V_{out}(t) = \frac{1}{C_f}\int I_{in}(t)dt = \frac{1}{C_f}\int Q_{in}\delta(t)dt = \frac{Q_{in}}{C_f}u(t) \tag{2.1}$$

where $u(t)$ is the Heaviside step function. The response of an ideal CSA is therefore a voltage step, whose amplitude is inversely proportional to the feedback capacitance.

An important aspect of the CSA can be observed from this relationship. The charge gain of a CSA depends only on the value of its feedback capacitor which can be thus designed according to the specifications for the intended application. Thanks to the "virtual ground" action of the high-gain core amplifier, the gain of the CSA does not depend on the value of the detector capacitance, C_d.

Applying the Laplace transform, Equation (2.1) in the frequency domain becomes:

$$V_{out}(s) = \frac{I_{in}(s)}{C_f}\frac{1}{s} \tag{2.2}$$

The CSA can be seen as a transimpedance amplifier since it converts the sensor current into a voltage signal. Therefore its gain is commonly expressed in mV/fC units.

However, realistic amplifiers have finite gain and bandwidth. If the amplifier has a finite gain, $A_0 = V_{out}/V_{in}$, the input node is not anymore a "virtual ground" and Equation (2.1) becomes:

$$V_{out}(s) = I_{in}(s)\frac{A_0}{s\left[C_d + C_f(1+A_0)\right]} \tag{2.3}$$

If $A_0 \gg 1$ and $(1+A_0)C_f \gg C_d$ we find again the ideal result of Equation (2.2).

The charge coming from the detector, Q_{in}, is shared between the sensor capacitance C_d and the dynamic input capacitance $C_{in} = (1+A_0)C_f$. The two terms can be written as:

$$\begin{cases} Q_f = V_{in}(1+A_0)C_f \\ Q_d = V_{in}C_d \end{cases} \tag{2.4}$$

where only Q_f is stored on C_f, thus contributing to the output signal, while Q_d is lost.

As a consequence, in order to readout a large fraction of the detector signal, the effective input capacitance of the CSA must be large compared to the sensor capacitance. In multi-channel systems, this issue can lead to cross-talk due to the fact that a fraction of the sensor capacitance comes from the coupling between one channel and its neighbors.

The finite bandwidth of a CSA affects the shape of the measured pulse, since it has not anymore a negligible rise time. This can be studied considering a simple amplifier made of an NMOS transistor with a load resistance R_L and an output capacitance C_L. The voltage gain of this inverting amplifier can be written as:

$$A_v = -g_m \frac{R_L}{1 + sR_L C_L} \tag{2.5}$$

where g_m is the transconductance of the input transistor and

$$Z_L = \left(\frac{1}{R_L} + sC_L \right)^{-1} = \frac{R_L}{1 + sR_L C_L} \tag{2.6}$$

is the load impedance given by the parallel combination of R_L and C_L. At low frequencies the second term is negligible and the gain is constant ($A_v = -g_m R_L$), while at high frequencies the second term dominates and the gain decreases linearly with the frequency.

The cutoff frequency is where the asymptotic low and high frequency responses intersect and is determined by the output time constant $\tau_L = R_L C_L$:

$$f_u = \frac{1}{2\pi\tau_L} \tag{2.7}$$

In the time domain, this implies that when a voltage step is applied to the input of the amplifier, the output does not respond instantaneously, as the output capacitance must first charge up. The amplifier response to a signal step of amplitude V_0 has therefore a finite rise time and can be expressed as:

$$v_{out}(t) = V_0 \left(1 - e^{-\frac{t}{\tau}} \right) \tag{2.8}$$

In a continuous time system, the charge coming from multiple signals is integrated on the feedback capacitor, C_f. In order to avoid the saturation of the CSA output voltage, the capacitor must be discharged through R_f. Therefore, although very high, R_f can not be infinite and its effect on the signal must be considered. The feedback impedance of the CSA is now given by the parallel between R_f and $1/(sC_f)$:

$$Z_f = \frac{R_f}{1 + sR_f C_f} \tag{2.9}$$

The transfer function of the circuit becomes:

$$\frac{V_{out}}{I_{in}} = \frac{R_f}{1 + sR_fC_f + s^2\frac{\zeta R_f}{g_{m1}}} \tag{2.10}$$

where g_{m1} is the transconductance of the input transistor of the amplifier, R_L and C_L are, respectively, the equivalent load resistance and capacitance and ζ is given by:

$$\zeta = C_TC_L + C_TC_f + C_LC_f \tag{2.11}$$

C_T is the total capacitance seen between the amplifier input and ground, in which the dominant contribution is usually given by the sensor.

Equation (2.10) can be approximated as:

$$\frac{V_{out}}{I_{in}} = \frac{R_f}{(1 + s\tau_f)(1 + s\tau_r)} \tag{2.12}$$

where:

$$\tau_r = \frac{\zeta}{g_{m1}C_f} << \tau_f = R_fC_f \tag{2.13}$$

The behavior of τ_r can be analyzed in two limiting cases:

1. When $C_f \gg C_L$ (and $C_T \gg C_L$)

$$\tau_r \approx \frac{C_T}{g_{m1}} \tag{2.14}$$

   Here the speed of the circuit is weakly sensitive to the value of the feedback capacitor and mainly depends on the ratio between the total input capacitance and the transconductance of the input transistor.

2. When $C_L \gg C_f$ (and $C_T \gg C_f$)

$$\tau_r \approx \frac{C_LC_T}{g_{m1}C_f} \tag{2.15}$$

   On the contrary, the speed of the circuit is also limited by the ratio between the sensor and the feedback capacitance.

In both cases, if the sensor capacitance is increased, also the transconductance of the input transistor must be augmented to preserve the CSA speed. Sensors with large capacitances thus require more power to maintain adequate speed and noise performance

in the front-end.

Finally, Equation (2.12) in the time domain becomes:

$$v_{out}(t) = \frac{Q_{in}}{C_f} \frac{\tau_f}{\tau_r - \tau_f} \left(e^{-\frac{t}{\tau_r}} - e^{-\frac{t}{\tau_f}} \right) \tag{2.16}$$

From Equation (2.16) it can be observed that small τ_f/τ_r ratios lead to a significant attenuation of the output voltage, thus reducing the overall circuit gain.

Figure 2.5 shows that high rates operation may cause the rising step of the next event to overlap with the exponential decay of the previous one, hence the CSA output does not return to the baseline and with a too high event rate the CSA may even reach its saturation point.

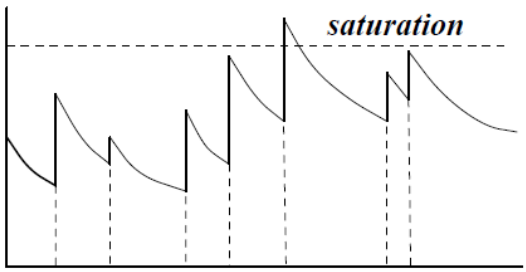


Figure 2.5: CSA pulses pile-up.

It must be taken into account that the pulses amplitudes carry the significant information, i.e. the charge deposited in the detector. Therefore, this issue can be addressed by shaping the pulses in such a way that their duration is reduced while their amplitude is not affected. Such signal filtering is typically carried out with a variety of RC shaper circuits.

2.1.3 Pulse shaping

Many applications require further signal conditioning which is implemented with a shaper stage connected at the pre-amplifier output. Its main task is to define the exact shape of the output signal in order to optimize the system performances in terms of signal-to-noise ratio and rate capability. The output signal shape should also be made insensitive to fluctuations in the input signal rise-time. In addition, it can provide a further signal amplification stage to optimize the front-end gain and match the input dynamic range requirements.

A simple pulse shaper connected at the output of the CSA is shown in Figure 2.6. Here a high-pass filter sets the duration of the pulse by introducing a decay time constant τ_d, while a low-pass filter increases the rise time to limit the noise bandwidth. The filters are isolated by a voltage buffer to decouple the two time constants.

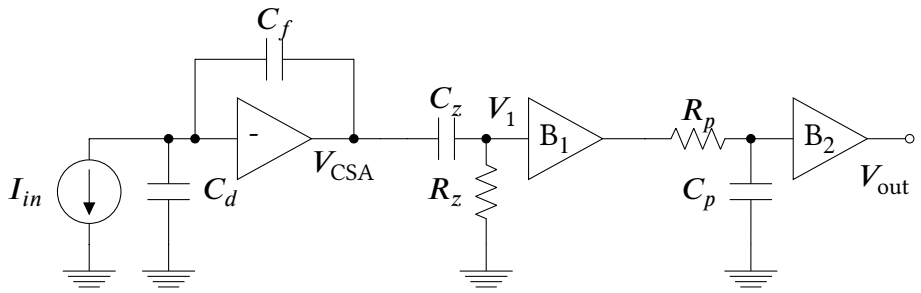


Figure 2.6: A simple CR-RC shaper using a CR "differentiator" as a high-pass filter and an RC "integrator" as a low-pass filter.

In the Laplace domain, the signal at the output of the high pass filter can be written as [23]:

$$V_1(s) = \frac{V_{CSA}}{s}\frac{sC_zR_z}{1+sC_zR_z} = \frac{Q_{in}}{C_f}\frac{\tau_z}{1+s\tau_z} \tag{2.17}$$

where $V_{CSA} = Q_{in}/C_f$ and $\tau_z = C_zR_z$. The pole in the origin introduced by the CSA is canceled by the zero due to the high pass filter. In the time domain the expression becomes:

$$V_1(t) = \frac{Q_{in}}{C_f}e^{-t/\tau_z} \tag{2.18}$$

The high pass filter cuts the constant or slow components, so that, when the input signal ends the output starts immediately to go back to the baseline before the next pulse arrives. Many applications requires to measure the charge released in the sensor, which can be extracted from the peak amplitude measurement. Since a signal with a smooth peak can be captured with better accuracy, the signal high frequency components are filtered-out with a low pass filter, which also plays an important role in signal-to-noise ratio optimization. The transfer function of the full chain can thus be written as:

$$V_{out}(s) = \frac{Q_{in}}{C_f}\frac{\tau_z}{1+s\tau_z}\frac{1}{1+s\tau_p} \tag{2.19}$$

where $\tau_p = R_pC_p$ is the low pass filter time constant.

For a given pulse duration, i.e. differentiation time, the CR-RC shaper yields the optimum signal-to-noise ratio when the two time constants are equal $\tau_p = \tau_d = \tau$ [23]. In this case we have:

$$V_{out}(s) = \frac{Q_{in}}{C_f} \frac{\tau}{(1+s\tau)^2} \tag{2.20}$$

which provides:

$$V_{out}(t) = \frac{Q_{in}}{C_f} \left(\frac{t}{\tau}\right) e^{-t/\tau} \tag{2.21}$$

where $\tau = \tau_p$ is the "peaking time" of the pulse shaper and corresponds to the time taken by the output signal to reach its maximum.

A more realistic implementation of a CR-RC shaper is shown in Figure 2.7. Here the decoupling buffers are replaced by low output impedance active stages that can provide also an additional gain.

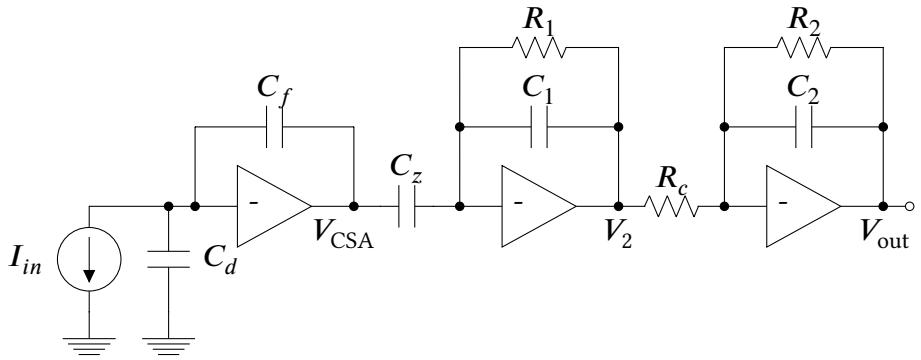


Figure 2.7: Implementation of a CR-RC shaper.

The transfer function of this circuit can be derived by studying the signal conversions which occur along the shaper building blocks. First, C_Z converts the CSA output voltage into a current, which is then converted back into a voltage, V_2, by a transimpedance amplifier:

$$V_2(s) = \frac{Q_{in}}{C_f} C_z \frac{R_1}{1+sR_1C_1} \tag{2.22}$$

Then V_2 is converted into a current by R_c and finally a second transimpedance amplifier provides at the shaper output a voltage as:

$$V_{out}(s) = \frac{Q_{in}}{C_f} C_z \frac{R_1}{1+sR_1C_1} \frac{1}{R_c} \frac{R_2}{1+sR_2C_2} \tag{2.23}$$

By imposing equal time constants, $\tau_1 = R_1C_1 = \tau_2 = R_2C_2 = \tau$, we obtain:

$$V_{out}(s) = Q_{in}\frac{C_z}{C_f}\frac{R_1R_2}{R_c}\frac{1}{(1+s\tau)^2} \tag{2.24}$$

In the time domain it corresponds to:

$$V_{out}(t) = \frac{Q_{in}}{C_f}\frac{C_z}{C_1}\frac{R_2}{R_c}\left(\frac{t}{\tau}\right)e^{-t/\tau} \tag{2.25}$$

The output of a simple CR-RC shaper returns to baseline rather slowly and this can be a critical issue for high-rate applications. The pulse can be made more symmetrical, thus with a faster return to baseline, by incorporating multiple integrators. These shapers are called "CR-RC^N shapers" or "Semi-Gaussian shapers" due to their response which is more similar to a Gaussian waveform. In time domain the resulting pulse shape is given by:

$$V_{out}(t) = \frac{Q_{in}}{C_f}\frac{C_z}{C_1}\frac{1}{n!}\left(\frac{t}{\tau}\right)^N e^{-t/\tau} \tag{2.26}$$

where N is the order of the shaper, defined by the number of integrators. In order to keep the same peaking time, the time constants must be scaled with the number of integrators.

CR-RC^N shapers are implemented cascading several active stages. This increases the requirements in terms of silicon area and power consumption and poses a limit on the shaper order. To further increase the symmetry of the impulse response without increasing the number of active stages, very sophisticated circuits, introducing complex conjugate poles in the transfer function, have been developed [26].

The design of a shaper stage must take into account several parameters, potentially conflicting with each other. On one hand, signal-to-noise ratio can be improved by limiting the bandwidth, thus filtering the noise frequencies without altering the signal. On the other hand a short pulse duration allows to measure consecutive signal pulses, avoiding pile-up, and may also provide better timing performance. Reducing the signal width increases the maximum sustained rate but also the noise. Usually, a trade-off between the two factors is found according to the specific requirements. For applications that require both energy and timing measurements a dual-branch architecture, integrating two independent shapers with different peaking times, can be the optimal solution.

2.1.4 Baseline stabilization

Detectors usually have a leakage current which is absorbed by the front-end amplifier and can affect the overall performance. Usually, the leakage current is removed by introducing AC coupling at a certain point of the chain. In Figure 2.7 the AC coupling is implemented between the pre-amplifier and the shaper with a series capacitor, C_z, which prevents the transmission of DC components. The input signals consist of a sequence of unipolar pulses, hence the baseline will drift to make the overall transmitted charge equal zero, as shown in Figure 2.8.

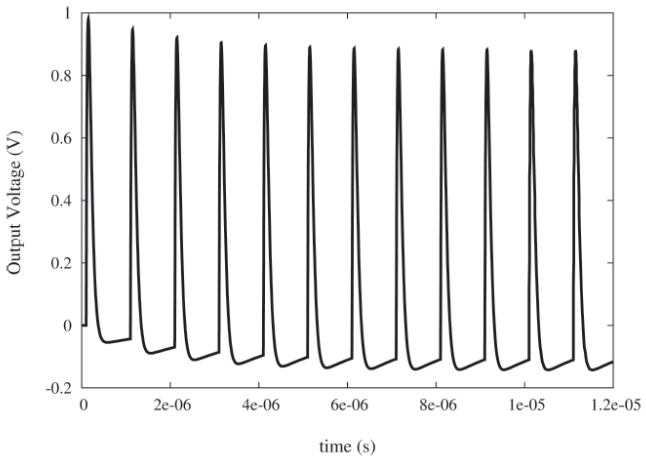


Figure 2.8: Baseline drift induced by a train of pulses occurring at regular intervals. In an AC coupled system a sequence of unipolar pulses will shift the baseline so that the net DC component is zero [23].

Here, regularly spaced pulses with fixed amplitude have been used, but in practical applications the events occur randomly in time and have different amplitudes, thus producing random variations of the baseline shift, which leads to an increased noise.

In addition, the input transistor of the shaper core amplifiers must be kept in the correct operating region, hence deviations from the optimal DC levels of the stages may also be an issue.

The baseline holder (BLH) is the circuit which allows to fix the shaper output DC voltage and to compensate the drift of the baseline caused by signals at high rates.

A typical BLH circuit is displayed in Figure 2.9. The circuit on the left allows to compensate a DC current entering into the stage, thanks to the feedback network formed by the differential amplifier A_2 and transistor M_1.

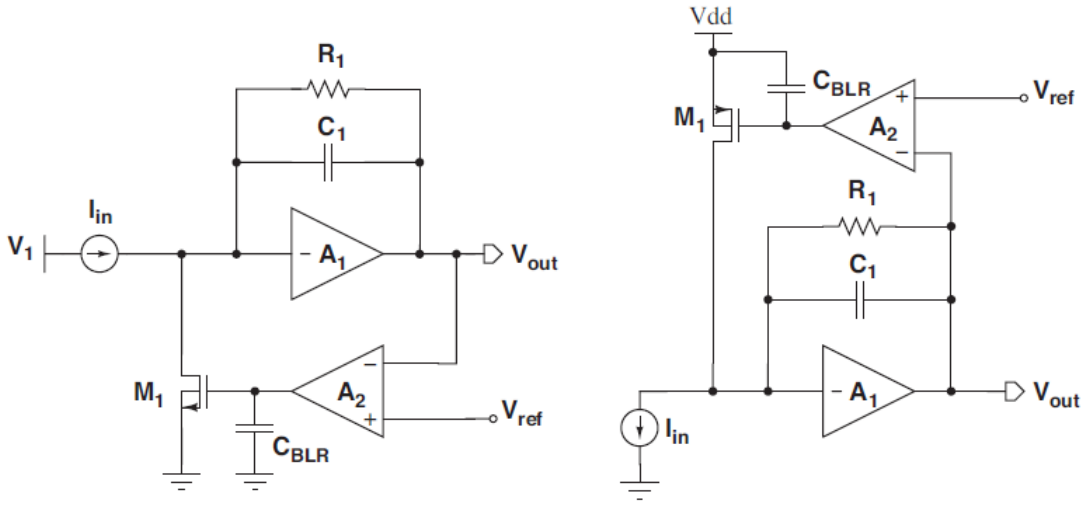


Figure 2.9: Baseline holder principle of operation [23].

Without the BLH circuit a current entering into the input node would flow in R_1, thus lowering the output voltage. The amplifier A_2 detects the difference between the shaper output, V_{out}, and an external reference voltage, V_{ref}. The voltage at the gate of M_1 is thus increased and the transistor sinks the input current, limiting the quantity that flows through R_1. This method locks the DC output voltage of the stage to the reference voltage, V_{ref}, allowing to optimize the dynamic range of the stage and the coupling to the following ones. The capacitor C_{BLR} and low bias currents allow to decrease the bandwidth of the differential stage so that only low-frequency signals are compensated by the feedback loop, without affecting real signals coming from the detector. The circuit on the right of Figure 2.9 works in the same way but it compensates a current sunk from the input.

2.1.5 Noise

Electronic noise sets the level of the minimum detectable signal and also establishes the ultimate limit of a measurement accuracy. Detectors signals usually are very small and, if not properly treated, they can be easily covered by the front-end electronic noise. It is therefore crucial to understand the main noise sources and study the techniques to minimize its effects.

Physically, noise can be explained by the finite number of charge carriers and the

finite speed at which they move inside a circuit. A variation in the number of carriers or in their speed will produce a perturbation in the currents or voltages inside the electronic system.

Different types of noise affect the response of an electronic circuit. In the following paragraphs, a brief description of the most commonly encountered types of noise is given.

Thermal noise

Thermal noise originates from the random motion due to thermal excitation of charge carriers inside a conductor. These erratic movements lead to temporary agglomeration of electrons that generate currents and voltages with mean value equal to zero, but producing instantaneous fluctuations of signals within a circuit [27]. At practical frequencies and temperatures thermal noise is independent of frequency, so its spectrum is "white" and its power spectral density can be expressed as:

$$v_n^2 = 4k_B T R \tag{2.27}$$

or equivalently:

$$i_n^2 = \frac{4k_B T}{R} \tag{2.28}$$

where k_B is Boltzmann constant, T the temperature (in Kelvins) and R the resistance of the material.

In MOS transistors, the channel can be treated as a variable conductance. Thermal noise is generated by random fluctuations of charge carriers in the channel, which can be represented as a current generator connected between the source and drain terminals. Its power spectral density can be expressed in terms of the transconductance g_m as:

$$i_n^2 = 4k_B T \gamma g_m \alpha_w \tag{2.29}$$

where γ is the inversion factor defined as:

$$\gamma = \frac{1}{2} + \frac{1}{6}\frac{I_c}{I_c + 1} \tag{2.30}$$

and α_w models the measured noise increase for short channel transistors.

Shot noise

With shot noise we indicate the time-dependent fluctuations in electrical current due to the quantization of the electron charge in solid-state devices [28]. This means that the current is not a continuous flow but the sum of discrete pulses in time, each corresponding to the transfer of an electron through the conductor. The individual events are independent of each other and described by Poisson statistics.

For instance, the sensor leakage current fluctuates due to shot noise. It can be modeled with a current noise generator in parallel with the detector whose spectral density is proportional to the average leakage current:

$$i_n^2 = 2qI_{det} \tag{2.31}$$

where q is the electron charge and I_{det} the detector leakage current.

The shot noise spectrum is white, at least up to the cut-off frequency given by the time for an electron crossing the conductor.

Flicker noise

Flicker noise is also commonly referred to as "1/f noise", since its noise power is inversely proportional to the frequency of the signal. It is the least understood of the noise phenomena. One hypothesis is that this kind of noise is originated by the interactions between the charge carriers in the MOSFET channel and the traps close to the Si-SiO_2 interface. The carriers, constituting the DC current flow, are held for some time period and then released, thus leading to fluctuations in the drain current. Flicker noise can be modeled with a voltage generator in series with the device gate, with a 1/f spectral density, which can be expressed as:

$$v_n^2 = \frac{k_f}{C_{ox}WL}\frac{1}{f} = \frac{A_f}{f} \tag{2.32}$$

where k_f is a technological process dependent constant, C_{ox} is the oxide capacitance in MOSFET devices, W and L are the channel width and length respectively.

The flicker noise of MOS transistors plays an important role in the performance of high resolution systems. Typically, PMOS transistors feature a lower 1/f noise than NMOS [29].

Equivalent noise charge

Noise performance of readout systems that measure signal charge can be expressed in terms of equivalent noise charge (ENC). ENC is the value of input charge which produces at the output a signal whose amplitude is equal to the output r.m.s. noise, i.e. the amount of charge that yields a signal-to-noise ratio of one:

$$ENC = \frac{Q_s}{S/N} \tag{2.33}$$

where Q_s is the input signal charge.

ENC is commonly expressed in fC or units of the electronic charge. In a continuous time front-end it can be expressed as:

$$ENC^2 = (C_d + C_{in})^2 \left(A_w v_n^2 \frac{1}{T_p} + A_F k_f \right) + A_p i_n^2 T_p \tag{2.34}$$

with v_n^2 and i_n^2 being respectively the input-referred voltage and current spectral noise density, C_d the sensor capacitance and C_{in} the sum of all the other capacitances appearing in parallel to the input (pre-amplifier input capacitance, stray capacitance). T_p is the front-end amplifier peaking time, while A_w, A_f and A_p are constant coefficients related to the front-end transfer function. From Equation (2.34), we can make some considerations:

- Series noise (both thermal and 1/f) is directly proportional to the input capacitance, therefore sensors with a small capacitance have a smaller noise.
- At small shaping times (large bandwidth) the ENC is dominated by voltage noise, while at long shaping times (large integration times) the current noise contributions prevail.
- The minimum ENC is where series and parallel noise contributions are equal. The time constant for minimum noise depends on the characteristics of the detector, the pre-amplifier and the shaper stage.
- The "1/f" noise contribution is independent of shaping time and flattens the noise minimum.

Peaking time plays a key role in a front-end design, defining its overall performance not only in terms of noise but also speed. For applications that require precise energy

measurements, in which it is important to optimize the ENC, the peaking time is typically set as long as permitted by rate and parallel noise considerations. In addition, it must be taken into account that the front-end is slowed down by increasing the value of the passive components building up the CR-RC network, hence the silicon area occupied by the circuit will increase as well.

Jitter and time-walk

ENC is not the only figure of merit to express the noise performance of a system. For timing measurements, where the determination of the time of occurrence needs to be optimized, the key parameter is not signal-to-noise, but slope-to-noise ratio. The time of arrival of an event is typically detected by a discriminator. In the basic leading-edge architecture, when the amplitude of the input pulse becomes larger than the threshold of the voltage comparator, the discriminator produces an output logic pulse, which carries the event time information.

Jitter and time walk are the two main effects that affect a time measurement, limiting the time resolution of a system.

Signals of same amplitude and rise time may trigger the discriminator at different times due to noise. The time of threshold crossing fluctuates around an average value and the sigma of this distribution defines the time jitter of the system, which is related to the noise affecting the signal fed to the discriminator by the following relationship:

$$\sigma_t = \frac{\sigma_V}{\frac{dV}{dt}} \propto \frac{1}{\sqrt{BW}} \tag{2.35}$$

where σ_V and dV/dt are, respectively, the noise and the slope of the signal fed to the discriminator. Typically, the leading edge of the signal is not linear, so the jitter is minimized when the threshold of the discriminator is set to the point of maximum slope.

In general, the noise is proportional to the square root of the bandwidth, while the signal slope is directly proportional to the bandwidth. As a consequence, jitter is inversely proportional to the square root of the bandwidth, hence faster systems have better timing performance. However, if the integration time of the front-end electronics is reduced below the charge collection time of the sensor a fraction of the input charge is not collected and this introduces an additional source of inaccuracy. Therefore, from a jitter optimization point of view, the peaking time of the system should match the detector charge collection time.

Unlike time jitter, time walk is not generated by noise but is due to the fact that signals with the same shape and peaking time but different amplitudes cross a given threshold at different times, as shown in Figure 2.10.

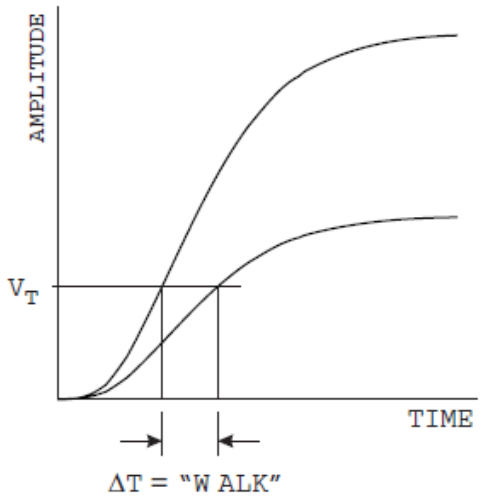


Figure 2.10: Time walk effect for signals of different amplitude [22].

Correction techniques both on-chip or off-chip can be implemented to compensate this effect. If the rise time is fixed and the amplitude of the signals is measured, time walk can be corrected offline inside the software event-by-event reconstruction. In hardware, time walk can be reduced by setting the threshold to the lowest practical level or implementing more complex discriminator architectures based on zero crossing or constant fraction timing [30], [31].

These results show that there is a trade-off between energy and time measurements. For this reason, many systems, in which both the time of arrival and the energy of the impinging particle is required, employ a dual-path topology. In this kind of architecture, the signal is split after the very input stage into two independent branches, with different shaping time constants, optimized either for timing or charge measurement.

2.2 Readout Architectures

Depending on the application requirements and constraints, different front-end readout architectures have been developed. Some applications, such as trackers for High Energy Physics experiments, may require only the position of the hit. The incident particle track is measured using multiple layers of sensors, which are typically immersed in a magnetic field to enable also the particle momentum measurement. Nuclear spectroscopy calls for high precision energy measurements, which can be provided by large dynamic range analogue circuits and Analogue to Digital Converters (ADC). For applications in which the determination of the time of occurrence of the interaction is the primary interest a common approach is to employ a fast response front-end coupled with a suitable Time to Digital Converter (TDC) in order to provide a good timing resolution.

2.2.1 Binary readout

A binary system is the simplest readout architecture. The analogue front-end is connected to a discriminator which detects if the front-end output goes above a preset threshold, generating a digital pulse. These systems require only a minimal digital circuitry to store the hit information, hence each channel occupies a small silicon area. Binary front-ends offer a good solution for applications where the primary information of interest is the hit position.

Since in a binary readout any signal crossing the threshold is processed as a good event, the number of hits due to noise must be minimized through a proper setting of the comparator threshold. The noise rate as a function of threshold-to-noise ratio [32] can be expressed as:

$$f_n = f_{n0} \cdot e^{-\frac{V_{th}^2}{2V_n^2}} \tag{2.36}$$

where f_n is the number of hits induced by noise per second, while V_{th} is the applied threshold voltage measured from the front-end amplifier baseline and V_n is the r.m.s. noise voltage measured at the front-end amplifier output. f_{n0} is the noise rate at zero threshold. For a CR-RC shaper it is given by:

$$f_{n0} = \frac{1}{4\sqrt{3}\tau} \tag{2.37}$$

where τ is the CR-RC shaper time constant. From Equation (2.36) one can calculate the required threshold-to-noise ratio for a fixed noise hit rate:

$$\frac{V_{th}}{V_n} = \sqrt{-2\ln(4\sqrt{3}f_n\tau)} \tag{2.38}$$

For a 60 ns time constant and a noise hit rate of $1 \cdot 10^{-5}$ hits/s we obtain a threshold-to-noise ratio of about 7.25. This implies that in a system with 10000 channels on average only one channel per second will fire due to noise. If we decrease the thresholds the efficiency on small signals will increase as well as the noise-induced hits.

The noise of a binary front-end can be measured using a threshold scan. An input signal of fixed amplitude is fed at the pre-amplifier input and the threshold of the discriminator is swept from low to high values, crossing the front-end output. For low threshold values all signals will be detected by the discriminator. When the threshold level is similar to the signal amplitude the efficiency decreases and becomes zero when the threshold is way higher than the signal. This transition, displayed in Figure 2.11, is broadened by electronic noise. The fit of the resulting "S-curve" provides an evaluation of the noise level and allows to find the optimum value for the threshold.

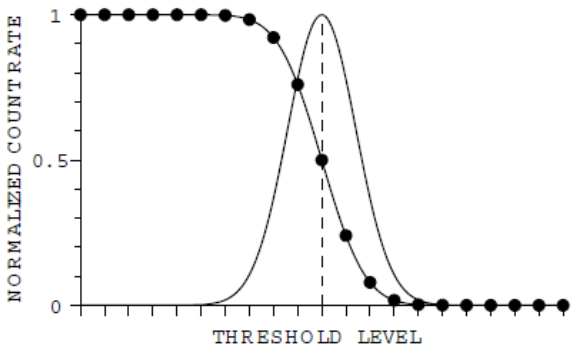


Figure 2.11: Typical S-curve produced by a threshold scan [22].

In multi-channel systems the discriminator offsets change the effective threshold applied to each channel, and this may affect the system performance in terms of noise rejection and efficiency. This effect can be studied by performing a threshold scan on several channels and observing that the transition of Figure 2.11 does not occur at the same point for all the channels.

In general, this offset can be reduced using very large transistors in the discriminator, but a very common approach is to compensate it using a a Digital to Analogue Converter (DAC) to fine tune the threshold setting for each channel. A threshold scan run using the discriminator DAC provides the correction code to the threshold of each comparator, thus equalizing the transition points of all channels.

GASTONE ASIC

GASTONE64 (Gem Amplifier Shaper Tracking ON Events, [33]) is a 64-channel ASIC developed to readout the signals coming from the cylindrical GEM inner tracker of the KLOE-2 experiment at the e^+e^- DAΦNE collider [34].

The ASIC architecture is depicted in Figure 2.12. Each channel comprises a charge sensitive amplifier, a shaper with a peaking time of 90 ns and a leading-edge discriminator with an internal DAC to fine tune the threshold on a channel-by-channel basis. The discriminator output is stretched by a monostable, with a programmable pulse width ranging between 200 ns and 1 µs, which allows to store the information and wait for the experiment trigger signal.

The small digital part includes a slow-control section providing an SPI interface, for read–write operations of the configuration registers, and a readout logic for the serialization of the digital output signals which are read-out using a 100 Mbit/s LVDS serial data link.

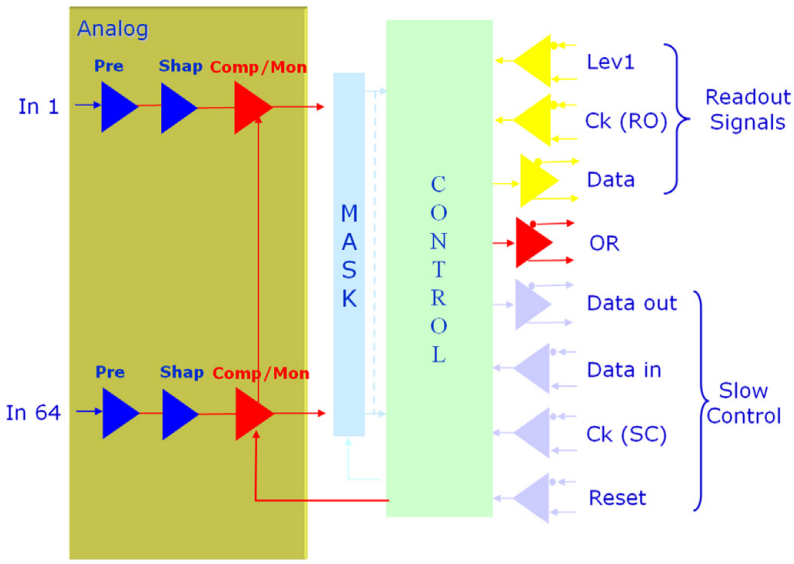


Figure 2.12: GASTONE architecture block diagram [33].

The ASIC has been designed in a CMOS 0.35 μm technology, for an input dynamic range between few fC and 40 fC, a charge gain of 16 mV/fC, with an equivalent input noise charge (ENC) of 800 e^- + 40 e^-/pF. The power consumption is about 6 mW/ch.

With GASTONE only the strips hit information is recorded, while the input signal charge is not measured, hence the system resolution is limited by the detector strip pitch (650 μm), which allows to achieve an overall spatial resolution of $\sigma_{r\phi} \approx 200$ μm. The BESIII CGEM-IT has the same strip pitch but a more demanding requirement in terms of spatial resolution ($\sigma_{r\phi} \approx 130$ μm), hence an analogue readout with charge and time measurement was preferred over the binary readout scheme described here.

2.2.2 Counting architectures

Adding a counter at the comparator output allows to record the number of events for a given time interval. This technique allows to measure the intensity of the impinging radiation, which is of particular interest in applications such as X-ray digital imaging or beam monitoring and control for particle therapy. The counters are typically implemented as Gray code counters such that two subsequent values differ in only one bit, thus allowing to reduce the number of simultaneous commutations. At the end of the time frame, the counters values are stored into output registers so that they can be cleared allowing to start a new cycle without dead time.

A counter can also be used to measure the duration of the comparator pulse. Since the time spent over threshold by the front-end output is proportional to the amplitude of the input signal, this method allows to extract the input charge information. Unlike peak sampling systems, this technique is not affected by the front-end saturation and allows to extend the charge measurement range beyond the limits imposed by the amplifier power supply.

2.2.3 Timing measurements

Applications seeking to optimize the determination of the time of occurrence may require the discriminator pulse to be captured with very good accuracy. A time resolution of 100 ps r.m.s. using the simple counter system described before would require clock frequencies in the range of GHz and it can become very unpractical to propagate such clock signal over a large number of channels.

Another way is to use a lower frequency reference clock and then measure the time elapsed between the discriminator output pulse and one clock edge with a TDC (Time

to Digital Converter) implementing digital or analogue interpolation techniques that allow to improve the time resolution beyond the system clock frequency.

In analogue interpolators, a capacitor is charged with a constant current source during the time interval to be measured and then the voltage across the capacitor is digitized usually with a Wilkinson ADC since its implementation requires little extra circuitry and allows for low power operation. Figure 2.13 shows the implementation of a time to amplitude converter coupled with a Wilkinson ADC.

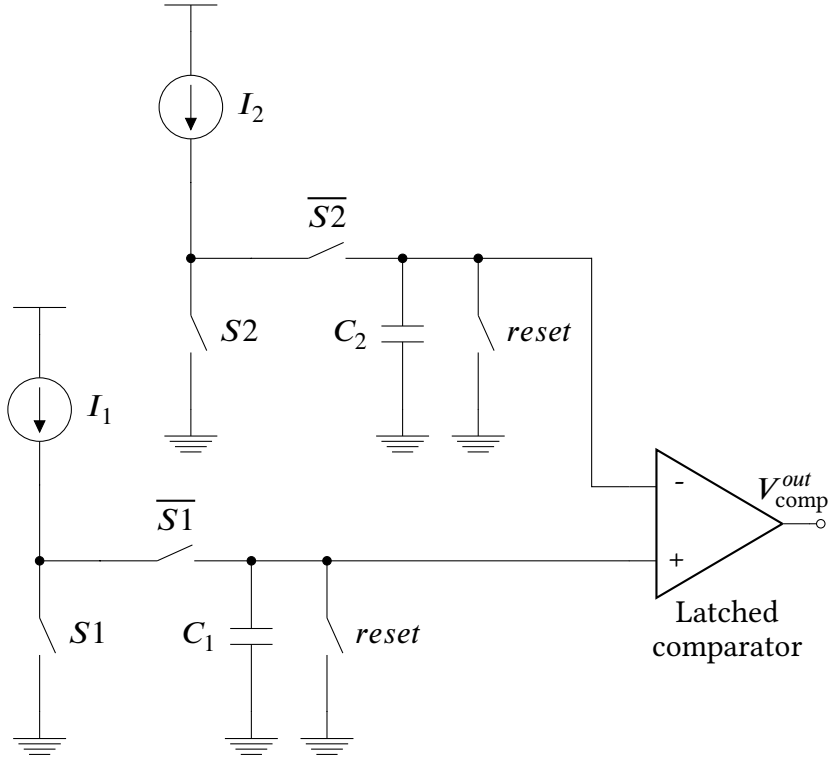


Figure 2.13: TDC based on analogue interpolation.

In idle mode, $S1$ is closed and $\overline{S1}$ is open and the current I_1 flows to ground. When the start signal arrives, $S1$ is open and $\overline{S1}$ is closed, steering the current from ground to the capacitor C_1. The voltage on C_1 rises linearly, and when the stop signal is asserted, the current is diverted back to ground and the capacitor is put in the hold mode. The final output voltage to be digitized is given by:

$$V_1 = \frac{I_1}{C_1}\Delta T \tag{2.39}$$

where $\Delta T = t_{stop} - t_{start}$ is the time interval to be measured. Typically, the stop signal

is given by the edge of a reference clock used to provide a coarse time base, thus making the TDC synchronous.

The voltage stored on C_1 is connected to one of the comparator inputs. The other input is connected to a second ramp generator composing the Wilkinson ADC. The capacitor C_2 is charged by a constant current I_2 until the voltage on C_2 is equal to the one stored on $C1$. The number of clock cycles required for this operation are counted and a fine time digital measurement (T_{fine}) is generated:

$$T_{\text{fine}} = \frac{C_2}{I_2} V_2 \tag{2.40}$$

where $V_2 = V_1$. From this value it is possible to extract the time difference between the unknown signal coming from the discriminator and the next edge of the system clock:

$$\Delta T = \frac{C_1}{I_1} V_1 = \frac{C_1}{I_1} \frac{I_2}{C_2} T_{\text{fine}} = \frac{C_1}{C_2} \frac{I_2}{I_1} T_{fine} = \frac{T_{\text{fine}}}{I.F.} \tag{2.41}$$

where $I.F.$ is the interpolation factor. For $C_2 = 4C_1$ and $I_1 = 32I_2$ an interpolation factor of 128 is achieved, thus providing for a 160 MHz clock frequency a time binning of about 50 ps.

The dead time due to the inherently high conversion time of the Wilkinson ADC can be addressed by employing more capacitors like C_1. In this multi-buffering scheme, if one capacitor is waiting for digitization, another one is ready to store a new event.

TOFPET ASIC

TOFPET (Time-Of-Flight Positron Emission Tomography) is a family of ASICs [35], [36] developed for the readout of Silicon Photo-multipliers (SiPMs), optimized for time-of-flight measurement in PET applications. The last version of this circuit (TOFPET2) is designed in a CMOS 110 nm technology and comprises 64 independent channels performing time and energy digitization of the input signals.

Each channel has two selectable pre-amplifiers for the readout of signals of either polarity. Three discriminators are deployed in order to reduce background events while keeping a good timing measurement accuracy. The first one is set to a very low threshold for precise timing measurement, the second one has a higher threshold for dark counts rejection, the third one is connected at the output of the integrator and allows to discard low energy events. Any signal that does not overcome all the three thresholds

is automatically discarded.

The signals from the discriminators are fed to a channel controller, running at 200 MHz clock frequency, that handles the operation of the TDC, ADC and charge integrator. The time of arrival information is digitized with a dual ramp TDC, composed by a set of four time to amplitude converters (TAC) and a Wilkinson ADC, providing a time resolution of 30 ps. The energy information can be extracted either from the charge integration of the signal or from the Time-over-Threshold measurement.

The ASIC is optimized for SiPMs with 320 pF total capacitance operating at gain of $1.25 \cdot 10^6$, providing a time resolution below 100 ps r.m.s. for a single photo-electron.

The TIGER ASIC inherited an upgraded version of the back-end controller of the TOFPET2 ASIC, hence the principle of operation of the ADC/TDC employed to encode the charge and time of arrival of the input signals is the same.

2.2.4 Sample-and-Hold and peak detectors

As discussed before, the signal amplitude can be derived from the measurement of time-over-threshold, but, except for specific architectures where the front-end output assumes a triangular shape, the ToT *vs* Q_{in} curve is intrinsically non-linear due to the response of a CR-RC^n shaper. This would require to build-up a calibration curve with many points.

Another way to measure the signal amplitude, and thus the input charge, is to sample the front-end output and capture its peak voltage that can be then digitized with a suitable ADC on-chip or off-chip. The basic scheme of a sample and hold (S&H) circuit to perform this task is shown in Figure 2.14.

During the sampling phase, the switch $S1$ is closed connecting the front-end output, V_{in}, to the hold capacitor, C_{hold}. $S1$ is closed at the detection of a peak, whose value is thus stored in C_{hold}. After that, $S2$ and $S3$ are closed so that the source follower acts as a buffer for the sampling capacitor and the stored voltage is made available for digitization or transmission. The critical point of S&H circuits is how the sampling time window is controlled.

In a continuous-time front-end, the highest SNR is obtained by sampling the peak of the output signal, hence the sampling time can be properly set according to the front-end peaking time. In this approach, the discriminator output is exploited to generate the start of the sampling time window whose duration is managed by a digital controller that counts a programmable number of clock cycles with the aim to capture the

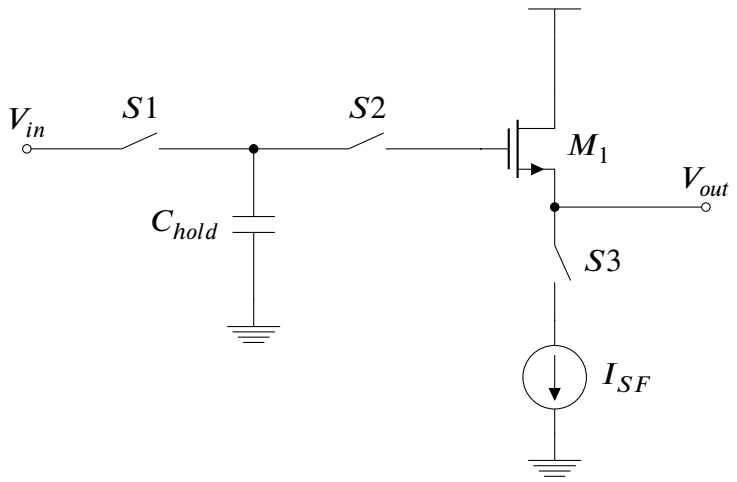


Figure 2.14: Principle of operation of a Sample-and-Hold circuit.

peak of the signal. The main issue of this method is that the jitter and time walk of the discriminator signal affect directly the sampling time.

A different solution requires the use of a fully-analogue peak detector [37] based on an operational amplifier which is configured as a voltage follower with a unidirectional element, usually a transistor, inserted in the feedback path. In this way, the output of the operational amplifier follows the input signal charging the hold capacitor. When the input reaches its maximum and starts to decrease the transistor in the feedback path is turned off and the peak voltage is thus stored on the capacitor and made available for the readout. This method offers a better accuracy at the cost of more hardware and power.

2.2.5 Analogue memories

Analogue memories feature an array of capacitors, ranging typically between 16 and 256 cells, to store the signal information and then make it available for the readout.

Two switches allow for write and read operations. The write switch connects the capacitor to the front-end output for a fixed amount of time. When the switch is re-opened the signal is sampled on that capacitor and the switch of the next cell is closed, in order to prepare the system for the next sampling. This operation is repeated for all the array capacitors. After that, a second switch is closed to read the stored value. The digitization of the sampled voltages can occur either on-chip or off-chip.

With analogue memories, the full front-end output waveform is recorded and can

be analyzed to detect undesirable effects, such as pile-up or baseline shifts. In this architecture only switches and capacitors are employed allowing for low power operation.

Capacitors are usually implemented using MOS transistor as they offer a larger density (>5 fF/μm^2) compared to the one of metal-metal capacitors (<1 fF/μm^2) and are thus more suitable when a high number of sampling cells is required. The circuit to control the sampling switches can employ a shift register driven by a clock signal that defines the sampling frequency or a digital delay line where the propagation delay of the logic gates, typically a couple of inverters, is exploited to achieve sampling frequencies in the order of GHz.

APV25

The APV chip series [38]–[40] was developed as a front-end amplifier for the CMS silicon strip tracker, but then it was also employed in many other GEM related applications [41], [42]. In the early stages of the CGEM-IT development, since the TIGER ASIC and its readout system were not ready yet, the first tests to study the performance of the GEM detector under development were carried out using the APV25. The results obtained from APV25 have been used as a reference and compared with the ones provided by TIGER.

The APV25 ASIC has been manufactured in a 0.25 μm sub-micron process[1] and includes a pre-amplifier, a shaper, an analogue pipeline and a deconvolution filter for each of its 128 channels (see Figure 2.15).

The pre-amplifier circuit consists of a single-ended folded cascode amplifier with a feedback capacitor of 150 fF. The requirements in terms of noise are met using a PMOS input transistor with an aspect ratio of $W/L = 2000/0.36$ (both width and length expressed in μm) and an input stage nominal bias current of 460 μA. A feedback resistor, realized with a transistor of variable conductance, avoids drifts and pileup effects.

A unity gain inverter is connected at the pre-amplifier output making the system compatible with signals of either polarity. The CR-RC shaper is coupled to the pre-amplifier output with a 1.4 pF capacitor. It is made of a single-ended non-folded cascode amplifier and has a time constant of $T_p = 50$ ns. The total front-end gain is 100 mV/mip (25000 electrons) with a non-linearity of less than 2% over a 5 mip range.

[1] The APV25 cannot be used in the final CGEM-IT application since it is based on IBM 250 nm technology, which is not exportable to China.

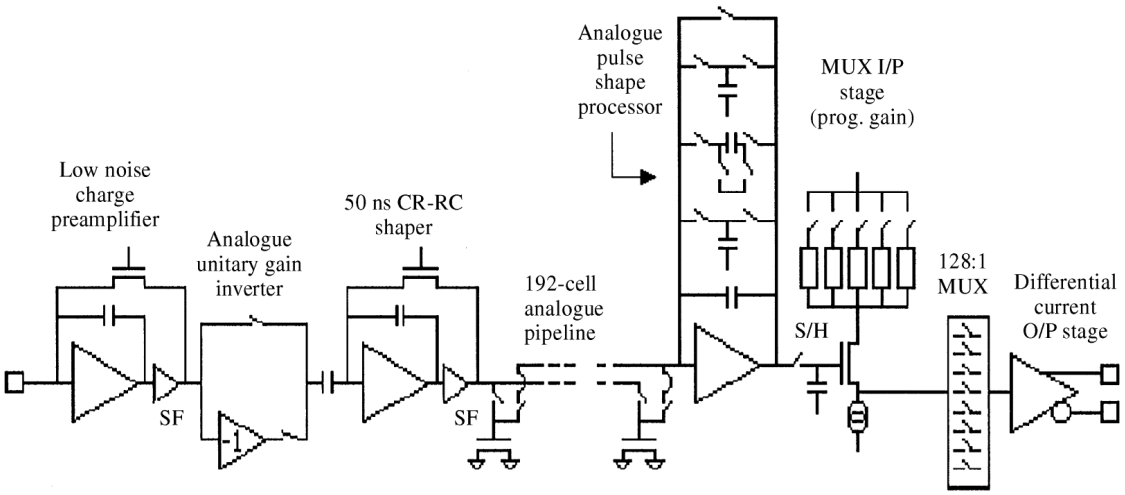


Figure 2.15: APV25 architecture block diagram [38].

The shaper output is sampled in steps of 25 ns, i.e. the bunch crossing frequency of LHC, and stored in an analogue pipeline, a ring buffer of 192 capacitor cells with cycling write and read pointers. Due to area constraints, the capacitors are realized using NMOS transistors operated in strong inversion to provide the best linearity. With a size of $W/L = 7/7$ (expressed in µm) a gate capacitance of 280 fF results.

On one hand, when data rates are sufficiently low and the effects of pile-up are negligible, the APV25 can operate in *Peak mode*, achieving the best performance in terms of signal-to-noise ratio and non-linearity. On the other hand, at higher rates of data, the chip is operated in *Deconvolution mode*, where a switched capacitor filter (Analogue Pulse Shape Processor) performs a three-weight deconvolution method that allows to distinguish between overlapped CR-RC shaped signals.

At the end of the pipeline, the signals are extracted upon a trigger request. The sampled outputs of the 128 channels are sent to a single output line, through a three-stage multiplexer, for optical transmission to the DAQ system.

Chapter 3

TIGER ASIC

The Torino Integrated GEM Electronics for Readout (TIGER) chip is a 64-channel mixed-signal ASIC developed for the readout of GEM detectors. The chip has been implemented in a 110 nm CMOS technology, occupies an area of 5×5 mm^2 and operates with a 1.2 V power supply.

In the first part of this chapter, a review of the specifications defined by the CGEM-IT detector requirements is presented. Different readout architectures are discussed as well as the motivations for the final design choices. After that, the architecture of one channel is presented with an in-depth description of the design of its building blocks. In the last part of the chapter, details about the ASIC architecture and its interface with the outside world are given. The expected performance of the ASIC are provided, supported by post-layout simulations.

3.1 Motivation and requirements

In this section the motivation and requirements that lead to the development of the TIGER ASIC are discussed. More details about the preliminary studies that contribute to the design of the full CGEM-IT detector can be found in the BESIII CGEM-IT Conceptual Design Report [9].

The very-front-end of TIGER has been designed to cope with the CGEM-IT requirements and it is optimized for input signals in the range 2-50 fC and targets a noise below 2000 electrons r.m.s. for a channel detector capacitance up to 100 pF. In this context, the different V-strips lengths and thus the wide spread of the input capacitance values does not allow for a fully optimization of the shaping stages in terms of noise reduction.

The innermost layer of the CGEM-IT will have to cope with a Total Ionizing Dose (TID) of 10 krad per year. The adopted 110 nm process technology has already been tested by another research group up to TID of 5 Mrad, with only minimal degradation effects [43]. This value is much higher than the maximum dose expected in BESIII. Nevertheless, the printed circuit board that hosts the chips has been irradiated to about 30 krad to test radiation damage on voltage regulators and passive components used to generate the ASIC bias voltages. A 0.7÷0.8% variation on voltage outputs has been observed, which is considered fully acceptable for this application.

As discussed before, the CGEM-IT will be the new inner tracker of the BESIII experiment and will be thus installed in the innermost part of the spectrometer. This poses several constraints in terms of rate capability, power consumption and readout operation.

The expected average rate per strip, extracted from the rates of the MDC innermost layer, is 14 kHz/strip. A ×4 safety factor has been introduced to take into account approximations in the detector description and digitization, systematic errors due to the angular distribution, high background running periods and luminosity increase. Therefore the maximum rate for the CGEM-IT is set to 60 kHz per channel.

Both binary and analogue readout architectures have been investigated. A binary readout front-end can be easily implemented as it manages only a single bit information per strip, while the analogue readout front-end requires the encoding of the collected charge and, as a consequence, a more complex readout chain. However, the binary readout chain has a not negligible drawback. Due to the constraint in spatial resolution requirement (∼130 μm) the strip pitch should be ∼300 μm, leading to a number of channels to fully readout the detector of about 25000. Considering the limited space available for the CGEM-IT inside the BESIII spectrometer, this can become very unpractical in terms of power consumption, number of cables and space required to host the on-detector electronics. The analogue readout chain, on the other hand, allows for a more relaxed strip pitch (650 μm), resulting in a more manageable number of channels (∼10000) and a maximum power consumption of about 12 mW/channel. Because of the strong constraints in terms of space, power consumption and spatial resolution, as well as noisy hit rejection capability, the analogue readout method has been chosen [12].

The charge and time information provided by the ASIC will be exploited to enable the charge centroid and μTPC reconstruction algorithms to improve the system spatial resolution compared to the one achieved with a simple binary readout. In this context, a time resolution below 5 ns is required in order to efficiently employ the μTPC algorithm.

One important aspect of the ASIC is the trigger-less (or data-push) readout architecture [44]. The chip produces output data regardless of the BESIII Experiment trigger: each signal above a given threshold is taken as a good event and digitized; data is then transmitted off-chip to the off-detector electronics (GEMROCs) where trigger-matching operations are performed, using the time information provided by the ASIC, and thus allowing to store only the data corresponding to the experiment L1 trigger signals, which are of interest for the experiment.

The relevant chip specifications are summarized in Table 3.1.

Parameters	**Value**
Input Charge	2-50 fC
Input Capacitance	Up to 100 pF
Data Rate	60 kHz/ch
Readout Mode	Trigger-less
Non-linearity	<1%
Charge Collection Time	60 ns
Time resolution	<5 ns
Power Consumption	<12 mW/ch
Technology	110 nm process

Table 3.1: Design specifications of the TIGER ASIC.

3.2 Channel architecture

The block diagram of one TIGER channel is reported in Figure 3.1. A charge sensitive amplifier (CSA) senses and amplifies the detector current. Its output is fed to two shapers optimized for timing and charge measurement.

The peaking time of the time-branch shaper has been set equal to the expected charge collection time (60 ns) allowing for low-jitter measurements. The shaper of the energy-branch has a slower peaking time (170 ns) for a better charge resolution and ENC optimization. Each shaper is coupled to a leading-edge discriminator with user-programmable threshold to correct potential offsets and mismatches between the 64 channels.

The discriminators output is fed to the channel controller, a digital logic unit running at a maximum frequency of 200 MHz, which generates the signals that handle

the operation of the mixed-signal back-end, where the time and charge information is extracted using two TDCs and a sample-and-hold (S&H) circuit.

Any relevant signal processing is performed on-chip in order to keep a good signal integrity and minimize interference noise. The ASIC communicates with the external environment using only digital LVDS links.

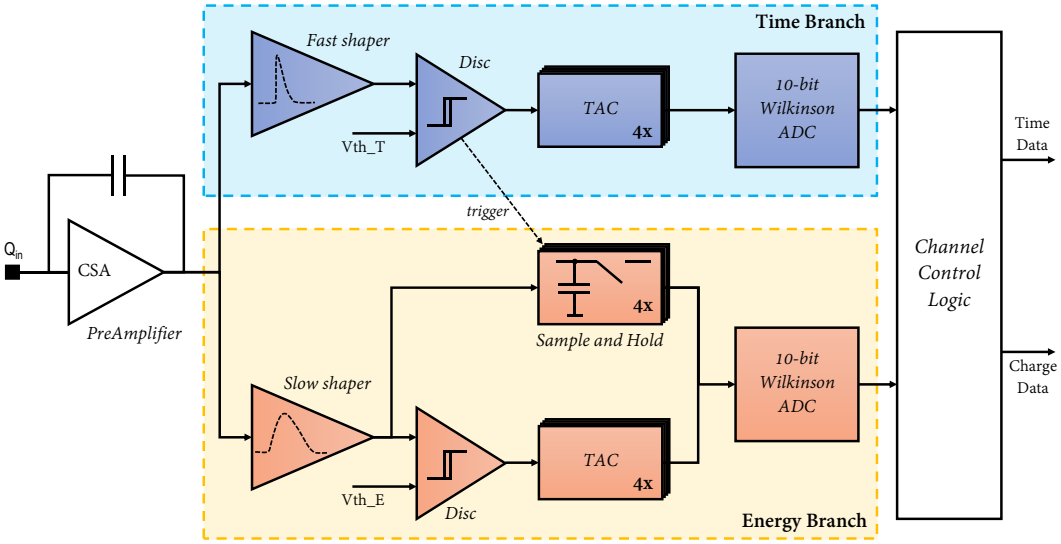


Figure 3.1: TIGER channel architecture scheme.

The two discriminators deployed in each channel enable a dual-threshold readout mode in which the time branch is set to a very low threshold for optimal timing performance while the better signal-to-noise ratio of the energy branch is used to discard the events induced only on the time branch due to noise.

An on-chip calibration circuit allows to inject test pulses of programmable amplitudes at the channels input to study the ASIC response for the full input dynamic range. A digital test pulse can be sent directly to the channel controller allowing to bypass the front-end part in case of malfunctioning and test and calibrate the TDCs as well as validate the digital back-end electronics.

The mixed-signal back-end is inherited from another ASIC developed for medical application [35], [36]. Due to the radiation environment in which TIGER is expected to operate, the digital logic has been SEU protected by Hamming encoding and Triple Modular Redundancy (TMR).

3.2.1 Measurement concept

The specifications set by the experiment demand TIGER to provide both time and charge measurements, with a fully digital output. In the next paragraphs, a brief description of the techniques implemented to perform these measurements as well as the different operating modes available inside the chip is given. A more in-depth description of each block will be provided in 3.2.5 and 3.2.6.

The time measurement is evaluated with two levels of accuracy. The coarse time information is provided by the chip master clock, running at a maximum frequency of 200 MHz and thus delivering a time binning of 5 ns. The fine time measurement is performed by a low-power TDC based on analogue interpolation. Here a set of four Time-to-Amplitude Converters (TACs) is used to measure the time elapsing between the hit triggered by the discriminator and the next clock rising edge (see Figure 3.2). The TAC analogue voltage is then digitized with a 10-bit Wilkinson ADC.

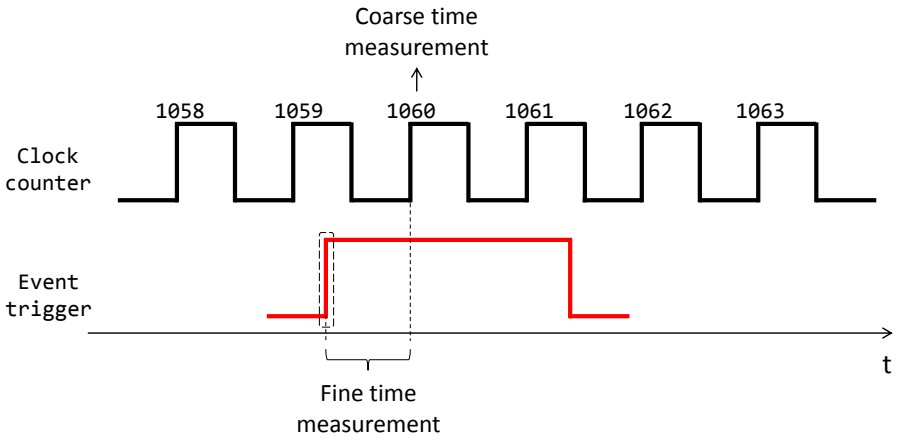


Figure 3.2: Time measurement concept: a clock counter provides the coarse time information of the event triggered by the discriminator; the system time resolution is enhanced by measuring the time elapsing between the asynchronous trigger signal and the next clock rising edge (fine time measurement).

The energy branch includes also an array of four Sample-and-Hold (S&H) circuits controlled by the digital logic to capture the peak voltage of the slow shaper output. This value is digitized by a second Wilkinson ADC, shared with the TDC.

The inherently high conversion time of this approach, i.e. the maximum digitization time can be up to 8 µs, is mitigated by the use of four derandomizing buffers, implemented both for the TACs and the S&H circuits, thus allowing for an event rate of at

least 100 kHz per channel with better than 99% efficiency.

The versatile back-end allows for different operating modes and charge measurement techniques. In *Time-over-Threshold mode* both branches are used for timing measurements, the S&H circuit is disabled and the two TDCs are employed to capture the leading and trailing edge of the discriminator and thus evaluate the pulse duration from which the charge information can be extracted (see Figure 3.3).

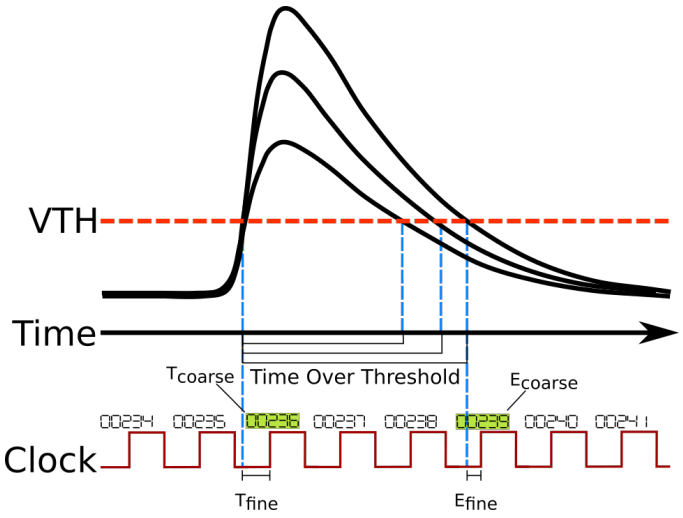


Figure 3.3: Charge measurement concept in ToT mode: both rising and falling edge time of the discriminator output are measured by the TDCs.

In *S&H mode* the charge measurement is performed by the S&H circuit capturing the peak voltage of the energy branch shaper output, which is then digitized by the Wilkinson ADC of the same branch. As a consequence, in this mode, the second branch does not produce a timing measurement, hence no ToT information is provided. As shown in Figure 3.4, the ADC performing the digitization works in reverse logic therefore the resulting ADC codes (Efine) will be high for small signals and low for large signals. If the signal to be digitized is higher than the ADC reference voltage (V_{ref}) the system saturates and the digitized output is fixed to a preset value (Efine = 1008).

Figure 3.5 shows an example of the chip response to different input charge signals for the two operation modes. These plots are obtained from measurements on silicon and show the charge measurement output (the ADC code for *S&H mode* and the time information for *ToT mode*) as a function of the input charge. On one hand, the response of the S&H is linear, but after the saturation point the digitized output value is not related anymore to the input signal. On the other hand, the ToT readout allows to extend the charge sensitivity beyond the saturation point of the front-end amplifier or the

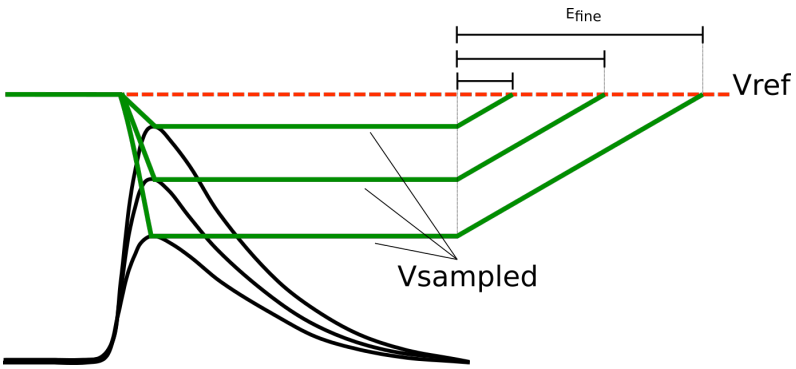


Figure 3.4: Charge measurement concept in S&H mode: the ADC of the energy branch is employed to digitize the slow shaper peak voltage.

S&H circuit. However, since the ToT response is not linear and strongly depends on the threshold setting, a calibration procedure is needed in order to translate the ToT measurement into a charge value and compensate channel-by-channel offsets and threshold variations. These two techniques will be analyzed more in detail in Chapter 4.

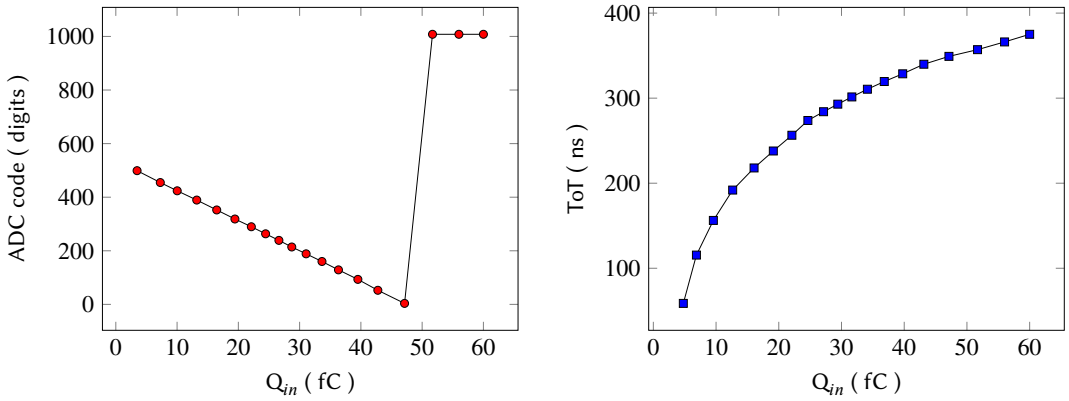


Figure 3.5: Charge measurement using the S&H circuit (left) and the ToT technique (right).

3.2.2 Input stage

The role of the input stage is to amplify the weak current delivered by the GEM anode while keeping the electronic noise as low as possible. A charge sensitive amplifier (CSA) has been chosen since it offers low noise, good stability and an output proportional to the total input charge, thus allowing to measure the energy deposited by the impinging particle with high precision.

Core pre-amplifier

Shown in Figure 3.6, the CSA core amplifier employs the two-stage cascode topology with rail-to-rail output proposed in [45]. The input stage is a dual cascode amplifier (M_1, M_2, M_4) with split current branch (M_3, R_3) and a common source stage with current mirror amplification (M_5, M_6, M_7) [46].

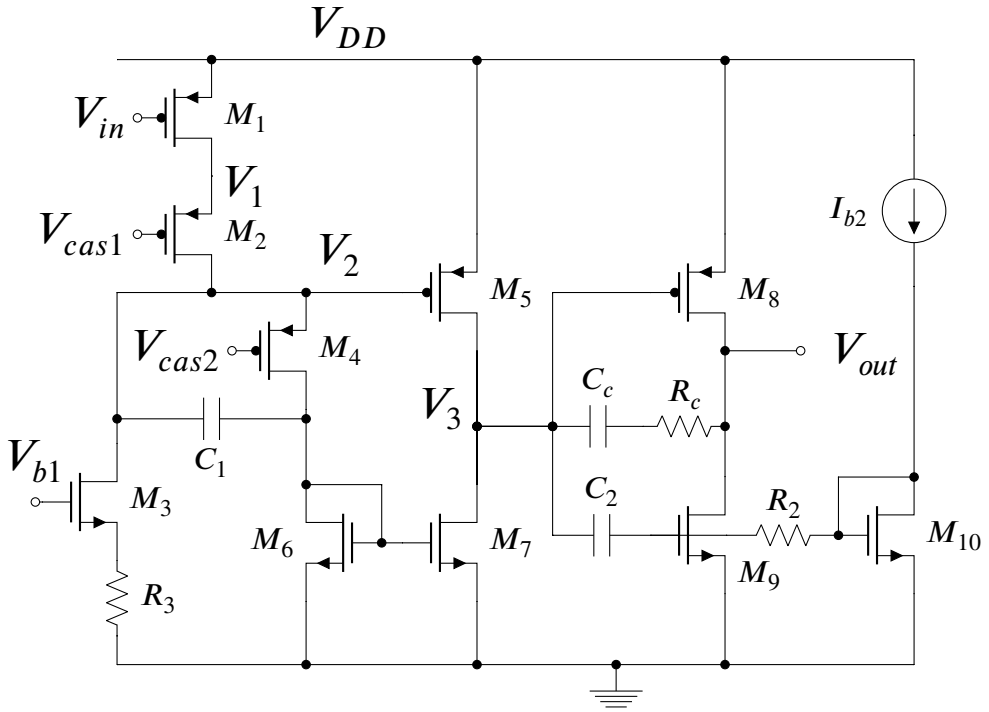


Figure 3.6: Schematic of the CSA core amplifier.

A PMOS input transistor has been chosen, because in the selected process it offers a smaller 1/f noise [29]. To satisfy the target ENC at the largest value of 100 pF input capacitance, a transconductance as high as 80 mS is required in the input transistor. This can be accomplished with an aspect ratio of $(W/L)_1$ = 9600/0.18 (width and length expressed in µm) and a bias current of 3.6 mA. The resulting gate capacitance is $C_g \approx 10$ pF and the device operates at the onset of moderate inversion (Inversion coefficient ≈ 0.4).

A 6-bit DAC generates the bias current of the input stage, providing an adjustable range from 1.5 mA to 4.5 mA. In this way, the current in the input transistor can be tuned to provide the required noise level for the given anode capacitance, optimizing the overall power dissipation of the system (see Figure 3.7).

The large bias current flowing through M_3 may have an impact on the overall noise

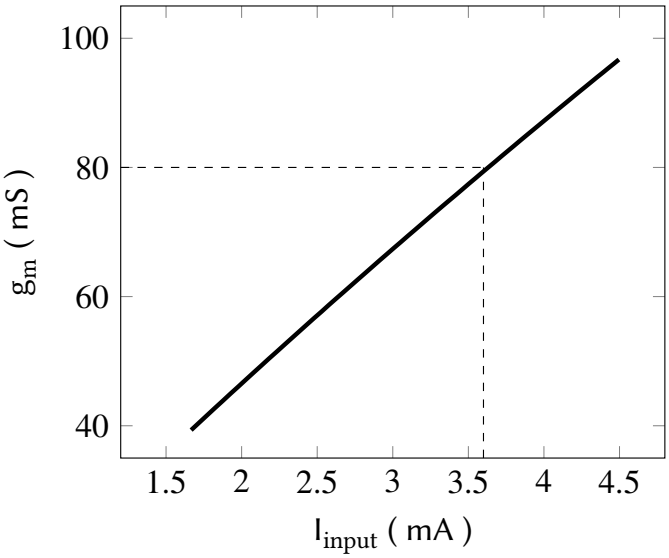


Figure 3.7: Computer simulation of the input transistor transconductance as a function of the bias current.

performance. In order to decrease the thermal noise injected by the bias circuit, g_{m3} is reduced thanks to the source degeneration resistor, R_3. The equivalent transconductance of the M_3-R_3 bias branch can be written as:

$$G_{m3} = \frac{g_{m3}}{1 + g_{m3}R_3} \tag{3.1}$$

As a result, the transconductance is reduced by a factor of $1/(1 + g_{m3}R_3)$. The total input referred voltage noise from the bias can be written as:

$$\overline{V_{bias}^2} = \frac{\overline{V_b^2}G_{m3}^2}{g_{m1}^2} + \frac{\overline{I_{R_3}^2}}{g_{m1}^2} \tag{3.2}$$

where $\overline{V_b^2}$ is the input referred spectral noise density of transistor M_3 and $\overline{I_{R_3}^2}$ is the spectral noise density of resistor R_3. The values of g_{m3} and R_3 can be estimated as follows. M_3 works in strong inversion, hence its transconductance is given by:

$$g_{m3} = \frac{2I_{DS}}{V_{OD}} \tag{3.3}$$

From this equation it can be seen that, for a given current I_{DS}, to reduce the transconductance of M_3 its overdrive voltage $V_{OD} = V_{GS} - V_{TH}$ should be set to a large value. However, a large overdrive voltage implies also a large saturation voltage, thus limiting the practical value of R_3. As a compromise, R_3 = 100 Ω and an aspect ratio $(W/L)_3$ = 600 µm / 4 µm have been chosen, leading to g_{m3} = 20 mS and G_{m3} = 10 mS. V_{OD} is set to 600 mV.

We can now study the signal path along the different stages of the pre-amplifier. As discussed before, the signals coming from the CGEM generate a negative pulse at the input of the CSA. When V_{in} is decreased, the current in M_1 increases and since this extra current can not be absorbed by M_3 it flows in M_4 rising V_2 up.

The current flowing in M_4 is mirrored by M_6, thus increasing the current in M_7. On the contrary, the current in M_5 decreases due to the increased V_2. As a result, V_3 is pulled down.

Despite the fact that in most of the time the chip will receive negative signals, occasionally there will also be positive input charge at the V_{in} node, due to sparks in the GEM detector or when a voltage step is injected as a test-pulse (refer to 3.3.2). If V_{in} rises, the current in M_4 is decreased. V_2 is pulled down, while V_3 is increased. It must be taken into account that when the current in M_4 decreases, V_2 can go low enough to switch M_4 off. To avoid the saturation of the amplifier, the bypass capacitor C_1 is added to create a feedforward path towards the gate of M_6. In this way, the circuit can handle both negative and positive input signals providing a symmetric response.

The output stage, formed by M_8 and M_9, is a class AB common-source amplifier providing an almost rail-to-rail output dynamic range [46]. The gate of M_8 is DC-coupled to the previous stage, while the gate of M_9 is AC-coupled through capacitor C_2. Resistor R_2 is made large enough, using two reversely biased PMOS transistors, so that the high pass filter formed by R_2 and C_2 has a sufficiently low cutoff frequency. Hence, in the frequency band of interest, the signals at node V_3 are transmitted through C_2 to the gate of M_9 without attenuation. M_8 and M_9 are thus driven in phase, providing class AB control of their bias current.

When V_3 is pulled down, the current in M_8 increases while the one in M_9 is decreased, thus the output node is charged. Therefore the output stage provides also a further signal inversion in order to make the overall amplifier suitable for negative feed-back.

The network composed by R_c and C_c grants an adequate frequency compensation to make the amplifier stable and will be discussed in the next pages.

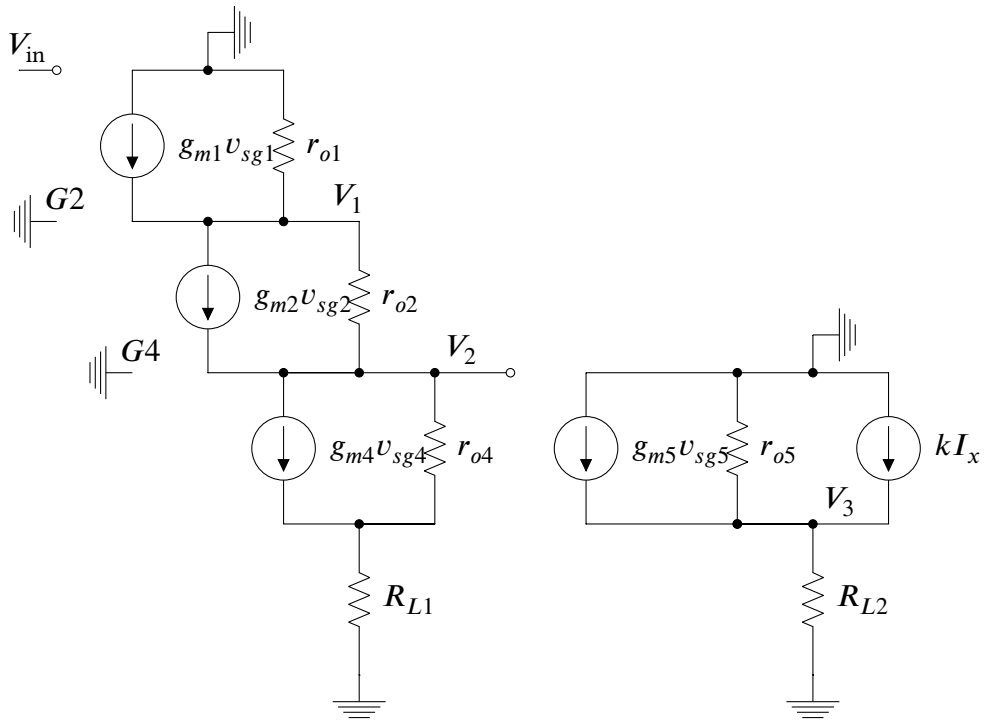


Figure 3.8: Small signal model of the first two stages of the core amplifier.

We can now calculate the amplifier open loop gain. The small signal model of the first two stages of the core amplifier is depicted in Figure 3.8. The output stage is not drawn and will be considered on a second phase, as well as the coupling capacitors. Writing down the node-voltage analysis equations we obtain:

$$\begin{cases} I_x = -g_{m1}V_{in} + \frac{V_1}{r_{o1}} \\ I_x = g_{m2}V_1 + \frac{V_1 - V_2}{r_{o2}} \\ I_x = g_{m4}V_2 + -\frac{V_2 - I_x R_{L1}}{r_{o4}} \\ \frac{V_3}{R_{L2}} = -g_{m5}V_2 - \frac{V_3}{r_{o5}} - kI_x \end{cases} \tag{3.4}$$

In the above expressions, $g_{m1} \div g_{m7}$ and $r_{01} \div r_{07}$ are respectively the transconductance and the output resistance of transistors $M_1 \div M_7$. The current mirror multiplication factor, k, is given by g_{m7}/g_{m6}. $R_{L1} = 1/g_{m6}$ and $R_{L2} = r_{o5} \parallel r_{o7}$ are the output impedances seen at the two ends of the current mirror branch.

The DC gain of the first and second stage can be written as:

$$\begin{cases} \frac{V_2}{V_{in}} = -\frac{g_{m1} r_{o1} g_{m2} r_{o2}}{1+g_{m4} r_{o2}(1+g_{m2} r_{o1})} \\ \frac{V_3}{V_2} = -(k g_{m4} + g_{m5}) R_{L2} \end{cases} \tag{3.5}$$

Therefore the DC gain from the input node V_{in} to V_3 is given by:

$$\frac{V_3}{V_{in}} = g_{m1}(r_{o5} \parallel r_{o7})\mathrm{B} \tag{3.6}$$

where the factor B is defined as:

$$\mathrm{B} = \frac{g_{m5}}{g_{m4}} + \frac{g_{m7}}{g_{m6}} \tag{3.7}$$

Compared with the gain of a standard common source amplifier, the amplification is thus multiplied by B.

For the last stage, at low frequencies the transconductance of M_9 is ignored due to the AC-coupling through C_2, hence the transfer function can be written as:

$$A_{out} = \frac{V_{out}}{V_3} = g_{m8}(r_{o8} \parallel r_{o9}) \tag{3.8}$$

The overall open loop DC gain of the core amplifier is given by:

$$\frac{V_{out}}{V_{in}} = \mathrm{B} g_{m1}(r_{o5} \parallel r_{o7}) g_{m8}(r_{o8} \parallel r_{o9}) \tag{3.9}$$

Table 3.2 lists some of the parameters and operating point values of the transistors of the CSA core amplifier, for a given setting of bias. Using the values of Table 3.2, from rough hand calculations, an open-loop gain of about 102 dB results. We can compare this result with an AC Spectre simulation. The core amplifier frequency response is shown in Figure 3.9.

The DC open-loop gain is about 100 dB and is in good agreement with the value obtained from hand calculations. The large open-loop gain of the amplifier should also guarantee low cross-talk between channels.

To enhance the amplifier stability, a Miller compensation capacitor, C_c = 500 fC is connected between the node V_3 and V_{out}. A compensation resistor R_c = 5 kΩ is inserted in series with C_c to shift the right-half-plane zero which could reduce the phase margin, compromising the system stability [47], [48].

Device	W/L [µm/µm]	g_m[mS]	r_o[kΩ]	C_g[fF]	C_{gs}[fF]	C_{gd}[fF]
M_1	9600/0.18	80.30	0.36	10577	5293	2957
M_2	2400/0.18	63.22	0.28	3701	2619	724
M_3	600/4	17.42	1.29	22170	21285	284
M_4	40/0.5	0.52	280.62	157	128	12
M_5	50/0.5	1.20	83.65	221	190	16
M_6	10/0.8	0.46	117.23	70	62	3
M_7	30/0.8	1.52	52.91	209	187	9
M_8	40/0.12	3.85	3.87	51	36	11
M_9	100/0.2	5.91	5.39	130	80	30
M_{10}	100/0.2	5.88	5.35	130	80	30

Table 3.2: Relevant operating point and parameters of the pre-amplifier.

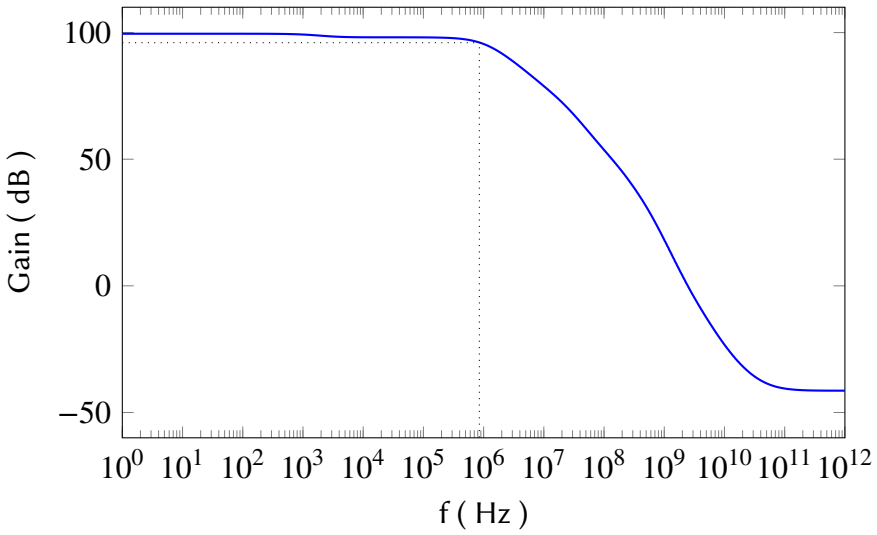


Figure 3.9: Frequency response of the open-loop amplifier. The dotted line indicates the cut-off frequency.

In order to evaluate the amplifier bandwidth, one can consider that the dominant pole of the amplifier is at the node V_3, since its load capacitance is increased by the Miller effect. The total capacitance and impedance at this node can be expressed as:

$$\begin{cases} C_{tot} = (1 + A_{out})C_c + C_{gd5} + C_{sd5} + C_{ds7} \approx 5\text{pF} \\ R_{tot} = R_{L2} = r_{o5} \parallel r_{o7} \approx 33\text{k}\Omega \end{cases} \tag{3.10}$$

where A_{out} is the output stage gain as defined in Equation (3.8). The resulting bandwidth of the core amplifier is given by:

$$f_T = \frac{1}{2\pi R_{tot} C_{tot}} \approx 960\text{kHz} \tag{3.11}$$

and is in good accordance with the simulation results shown in Figure 3.9.

Transconductance feedback

Figure 3.10 shows the CSA with its feedback network, which employs current mirrors combined with capacitors for pole-zero cancellation [49].

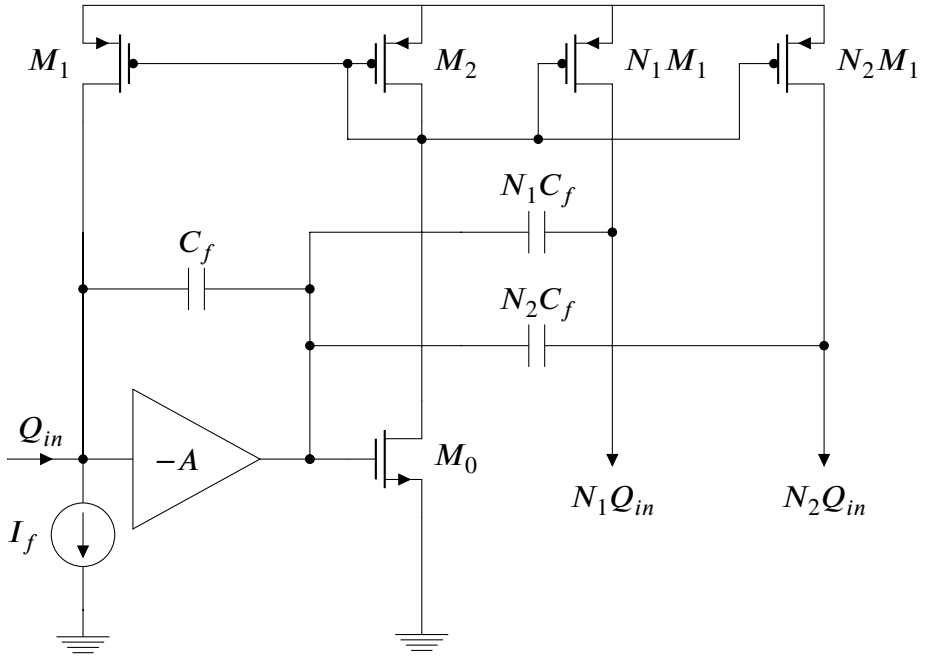


Figure 3.10: Pre-amplifier stage with transconductance feedback implemented with current mirrors.

The CSA output voltage is converted into a current by M_0, which is then mirrored towards the input, scaled by the aspect ratio between M_2 and M_1. The equivalent feedback resistance is given by:

$$R_f = \frac{1}{g_{m0}} \frac{\left(\frac{W}{L}\right)_2}{\left(\frac{W}{L}\right)_1} = \frac{k}{g_{m0}} \tag{3.12}$$

For a feedback current I_f = 10 nA and k = 100, we obtain g_{m0} = 10 µS which leads to a feedback resistance R_f= 10 MΩ. The feedback capacitor, C_f, is set to 150 fF, thus leading to a CSA gain of ∼6.7 mV/fC and a discharge time constant of 1.5 µs.

This architecture allows to split the signal into two identical branches providing additional charge amplifying given by the constants $N_1 = N_2 = N = 20$. The pole-zero cancellation is implemented by sizing the capacitors of the two branches with the same ratio of their respective transistors, hence the two capacitors necessary for the pole-zero cancellation are N times the feedback capacitor (NC_f = 3 pF).

The effect of cross-talk between two neighbor channels is shown in Figure 3.11. A capacitor C_M = 5 pF, is used to model the mutual capacitance coupling the input stages of the two channels. The input signal injected on the fired channel is set to the maximum value expected from the GEM detector (50 fC), inducing a 2.2 mV signal at the CSA output of the neighbor channel due to cross-talk. For a gain of 6.7 mV/fC, this variation corresponds to a 0.33 fC input signal.

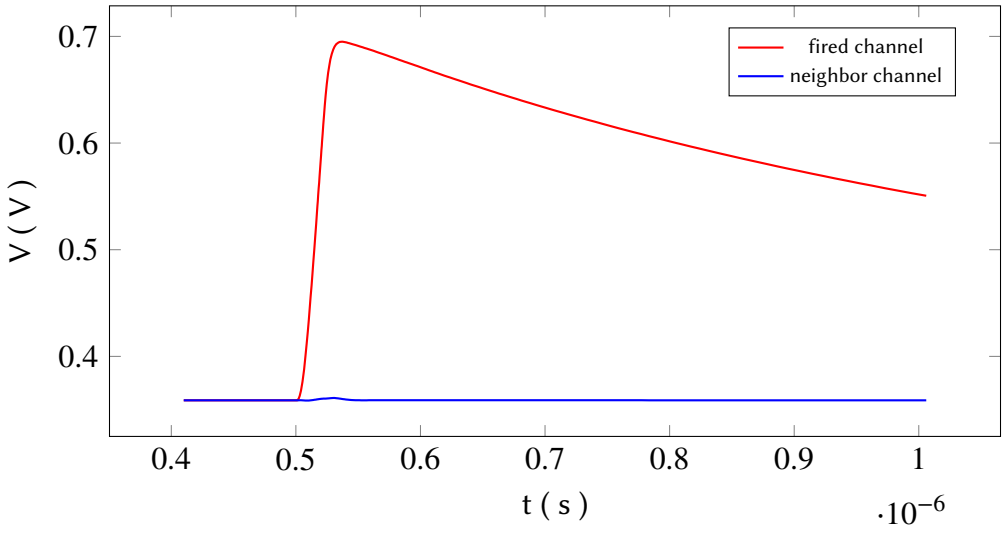


Figure 3.11: 2-channel simulation to study the cross-talk between the fired channel (50 fC input signal) and its neighbor. The channels coupling capacitance has been set to 5 pF.

3.2.3 Shaper stage

The input stage turns the input charge signal into a current output, which is split into two branches serving two shapers, optimized for timing and energy measurement.

Each shaper consists mainly of three blocks: the core amplifier, the high frequency feedback network and the Baseline Holder (BLH) circuit.

The main task of this stage is to define the shape of the signal making it more suitable for the next stages, i.e. discrimination and digitization. As discussed in the previous chapter, the front-end peaking time plays an important role in defining the system performance in terms of noise and rate capability. On one hand, for high precision energy measurement a longer peaking time is preferred since it offers a better ENC, on the other hand low-jitter time measurements require a fast rising signal and thus a shorter peaking time. Setting a sufficiently long peaking time allows to integrate a large fraction of the input current delivered by the detector, making the system almost insensitive to fluctuations of the input signal due to the charge collection time. Also the total width of the signal must be taken into account since it defines the maximum rate that the system can sustain. In addition, the baseline holder loop allows to set DC output voltage to optimize the front-end dynamic range and avoid baseline drifts.

Given the fact that TIGER is required to perform both energy and time measurements, a dual-branch architecture with different shaper topologies and different peaking times has been chosen.

All the core amplifiers implemented in the shapers employ the same topology adopted in the CSA. The class AB output stage provides an almost rail-to-rail output dynamic range thus allowing to accommodate the large output signals of the shaping core amplifiers. Transistor sizes and bias currents have been scaled down since the noise performance of these stages is less critical. A bias current of 100 µA is thus used in all the core amplifiers of both shapers. Further details about the shaper and BLH circuit design are provided in Appendix A.

Energy branch shaper

The shaper in the energy branch is shown in Figure 3.12. To optimize the signal-to-noise ratio a peaking time as long as permitted by rate considerations can be chosen. The expected maximum event rate per channel, including a safety factor of four, is 60 kHz. The time of arrivals of the events follows a Poisson distribution as:

$$P(n) = \mu^n \frac{e^{-\mu}}{n!} \tag{3.13}$$

where μ is average number of events in the time window of interest. If we set a total pulse width of 600 ns, for an event rate of 60 kHz, we obtain $\mu = 0.0375$. The probability

of not having pile-up is thus given by:

$$P(0) = e^{-\mu} = 96.3\% \tag{3.14}$$

The resulting pile-up probability of 3.7% is considered fully acceptable for this application.

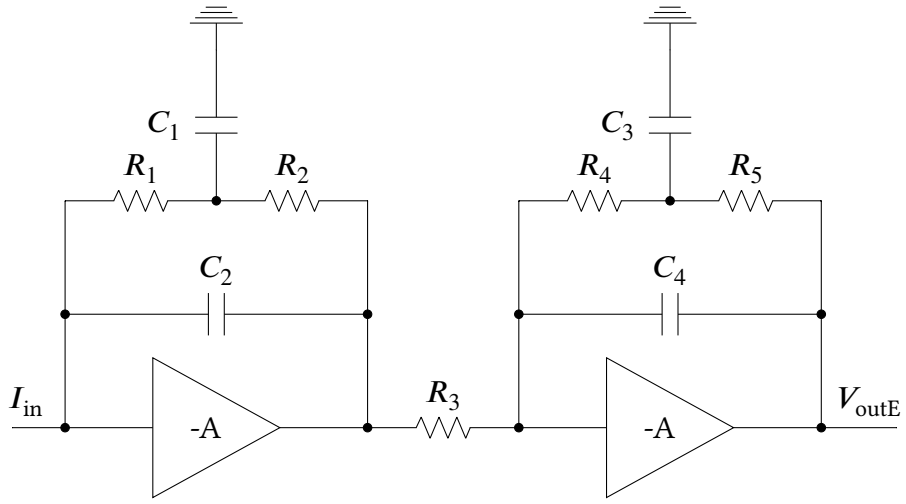


Figure 3.12: Shaper with four complex conjugate poles used in the energy branch.

To optimize the ratio between peaking time and total pulse width a topology with complex conjugate poles has been adopted [26], [50]. Two cells are cascaded to yield a system with four complex conjugate poles, in which the peaking time is about 30% of the total pulse width. The values of resistors and capacitors in the feedback network set a nominal peaking time of 170 ns and an overall gain of about 12 mV/fC.

Another factor which limited the peaking time was the available silicon area, since the full chip had to fit a 5×5 mm^2 in order to be produced in a Multi-Project Wafer (MPW) run. This posed a limit to the maximum size of resistors and capacitors implementing the feedback network, and thus their values.

Time branch shaper

The time branch shaper is shown in Figure 3.13. The peaking time is set to 60 ns, in order to match the typical charge collection time expected from the sensor. A simple CR-RC transfer function is implemented, since it offers a better slope and thus more favorable jitter performance. The pulse duration here is not very critical because the peaking time is shorter.

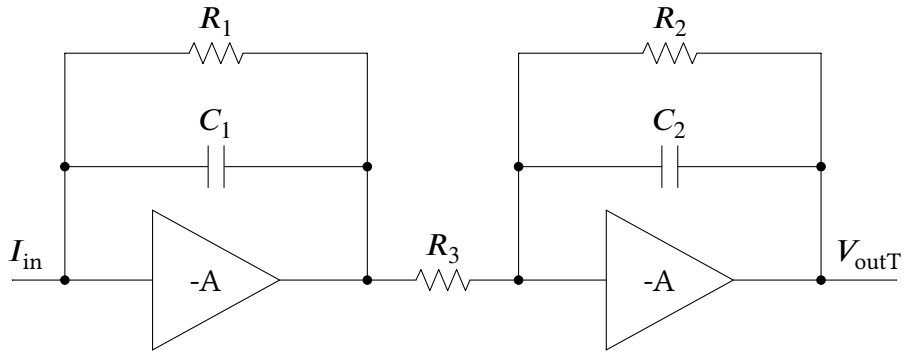


Figure 3.13: CR-RC shaper in the timing branch.

Baseline Holder

Each shaper is enclosed in a dedicated baseline holding (BLH) loop [51] to suppress any DC current coming from the preamplifier and lock the DC output voltage to an external reference voltage. For our application, this reference has a default value of ∼350 mV and can be adjusted off-chip through a dedicated pad.

A simplified block diagram of the baseline holder is shown in Figure 3.14. The voltage applied to the BLH input is first multiplied by the gain of the differential amplifier, then is converted into a current by M_1 and finally re-transformed into a voltage by the DC transimpedance gain of the shaper. A strong slew-rate limitation is introduced by current-starving the buffers B_1 and B_2 and by loading the internal buffers with capacitors C_1 and C_2. Fast signals are thus ignored by the BLH circuit, allowing to minimize rate-dependent baseline shifts.

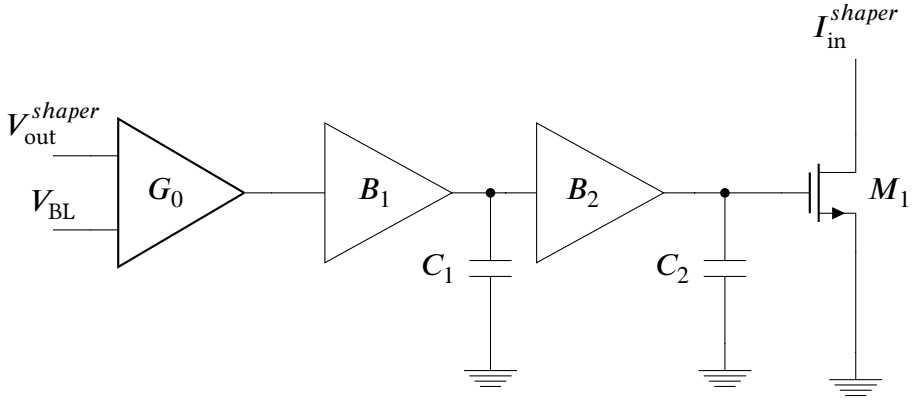


Figure 3.14: Block diagram of the baseline holder.

Figure 3.15 shows the implementation of the time branch full shaper stage. The values of the relevant components are reported in Table 3.3.

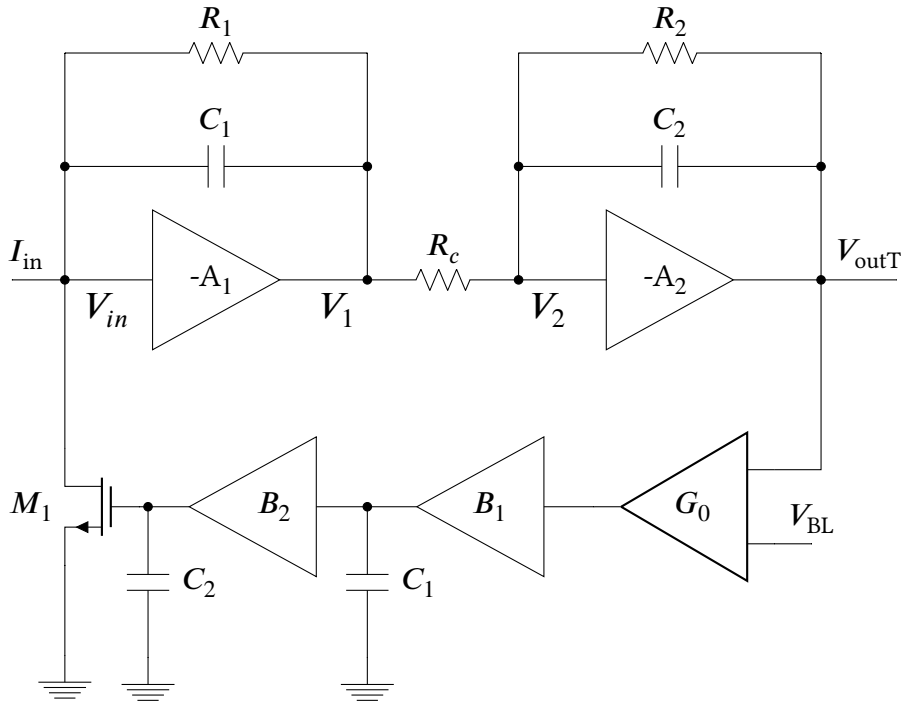


Figure 3.15: Time branch shaper with BLH.

Components	Values
R_1	100 kΩ
C_1	1 pF
R_2	20 kΩ
C_2	1 pF
R_c	20 kΩ

Table 3.3: Shaper stage design values.

We can now study the optimal setting of the DC levels to achieve an adequate dynamic range in each stage. The output of the second shaping stage is the global output and its DC point is given by V_{BL} which is set to 350 mV, reasonably close to ground. On the contrary the DC output of the first shaping block, where the signal is swinging downwards, must be as high as possible.

Since both core amplifiers, A_1 and A_2 are implemented with PMOS input transistor, we can assume that the DC point of their input is 700 mV for both stages. As a

consequence, the current flowing in the feedback resistor R_2 is given by:

$$I_{R_2} = \frac{V_{2,DC} - V_{out,DC}}{R_2} = 17.5\mu A \tag{3.15}$$

This current is provided by A_1 through the coupling resistor R_c, resulting in a voltage drop across R_c of 350 mV. The DC output of A_1 is thus given by:

$$V_{1,DC} = V_{2,DC} + \Delta V_{R_c} = 1.05V \tag{3.16}$$

which is barely sufficient to keep the output stage transistor of the shaper core amplifier in saturation.

The input DC voltage of A_1 is 700 mV, hence the current flowing in the feedback resistor R_1 is given by:

$$I_{R_1} = \frac{V_{1,DC} - V_{in,DC}}{R_1} = 3.5\mu A \tag{3.17}$$

This current must be provided by the baseline holder which works as follows. The input stage consists of a differential amplifier, G_0, to compare the baseline value with the reference voltage, V_{BL}. Since the DC input voltages are low, it is implemented with PMOS input transistors. Its output is fed to a couple of current-starved source followers in order to eliminate the contribution from fast signals and consider only potential baseline drifts.

The first source follower, B_1, is implemented with PMOS transistors and introduces a slew rate limitation when V_{out} rises, which is the typical situation that occurs with signals coming from the detector.

The second source follower, B_2, is implemented with NMOS transistors and allows to limit signals of "wrong" polarity, which may present at the front-end input when the on-chip pulser (refer to 3.3.2) is enabled injecting at the amplifier input a voltage step through a capacitor connected in series to the input.

Figure 3.16 shows the simulation results of the full analogue front-end electronics for an input signal of 7 fC. The baseline of both branches is kept at about 350 mV by the Baseline Holder circuit.

To check the functionality of the BLH and the stability of the circuit a simulation with a long time duration is needed. In this way potential large oscillations of the baseline become visible and can be properly addressed increasing the low-pass filtering time

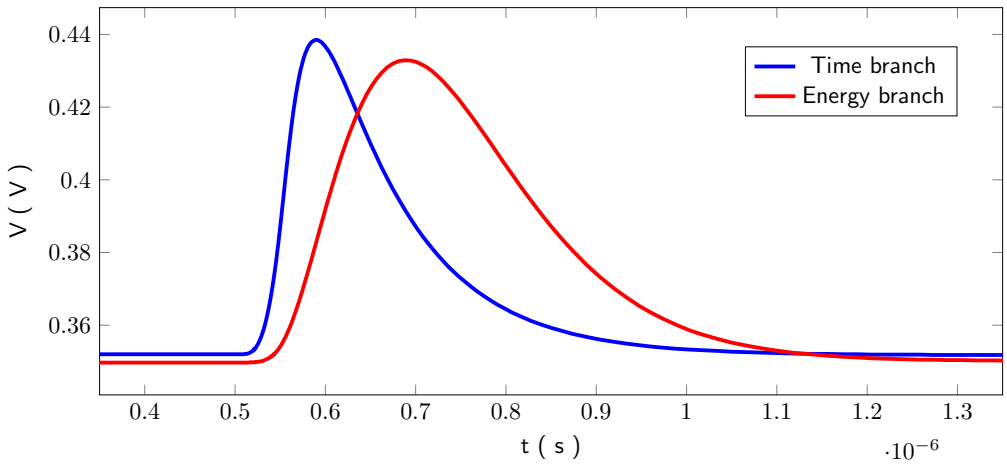


Figure 3.16: Simulation of the time and energy branch shapers output for a 7 fC input signal. The baseline was set to 350 mV.

constants introduced by the two buffers. Figure 3.17 reports the circuit response simulated for 2 ms time scale. No visible oscillations of the baseline are present.

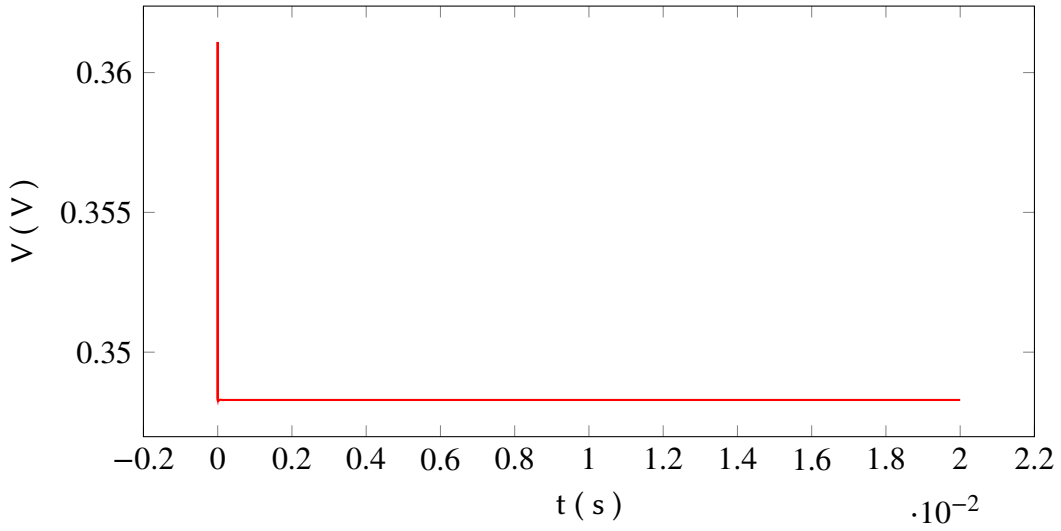


Figure 3.17: 20 ms simulation of the energy branch shaper output to assess the correct return to baseline.

In order to spot potential baseline drifts due to a high event rate, we must study the circuit response to a train of pulses, as reported in Figure 3.18. No significant baseline drift is observed. These results confirm the correct behavior of the BLH circuit.

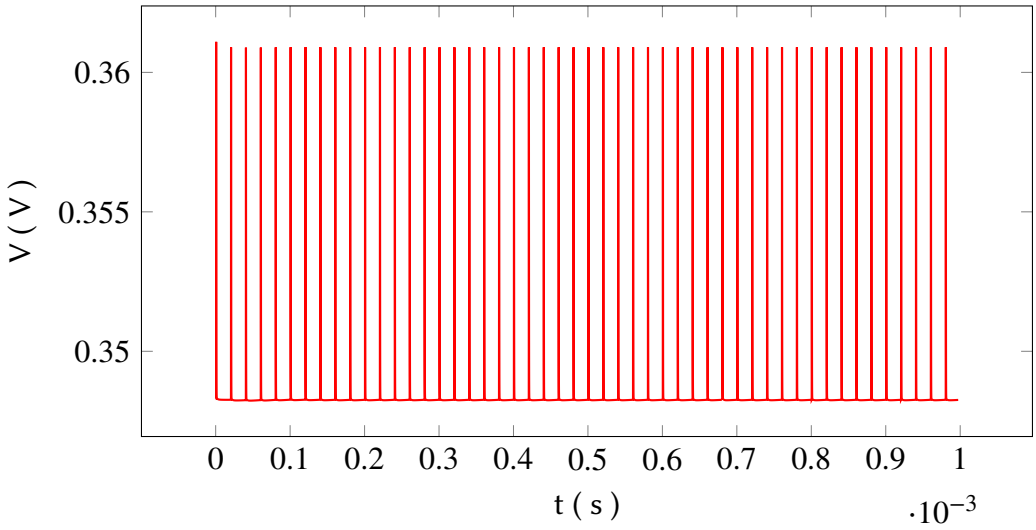


Figure 3.18: Energy branch shaper baseline drift simulation at 50 kHz event rate.

The layout of one channel analogue front-end is represented in Figure 3.19. It occupies and area of 69×1008 µm^2, the power consumption is about 5.5 mW, where the major contribution comes from the CSA (5 mW). The test pulse injection circuit will be described in 3.3.2. After the Charge Sensitive Amplifier, the two shapers are disposed in parallel and are followed by their Baseline Holder circuit. Due to its larger feedback network components the energy branch shaper occupies more area than the time branch shaper.

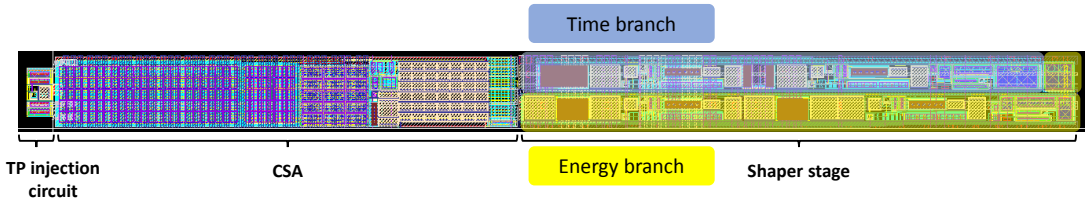


Figure 3.19: Layout of the analogue front-end.

Computer simulations of the full analogue front-end allow us to evaluate the system overall performance in terms of gain, linearity and noise. Figures 3.20 and 3.21 show the response of the analogue front-end chain for input signals ranging from 1 fC to 55 fC.

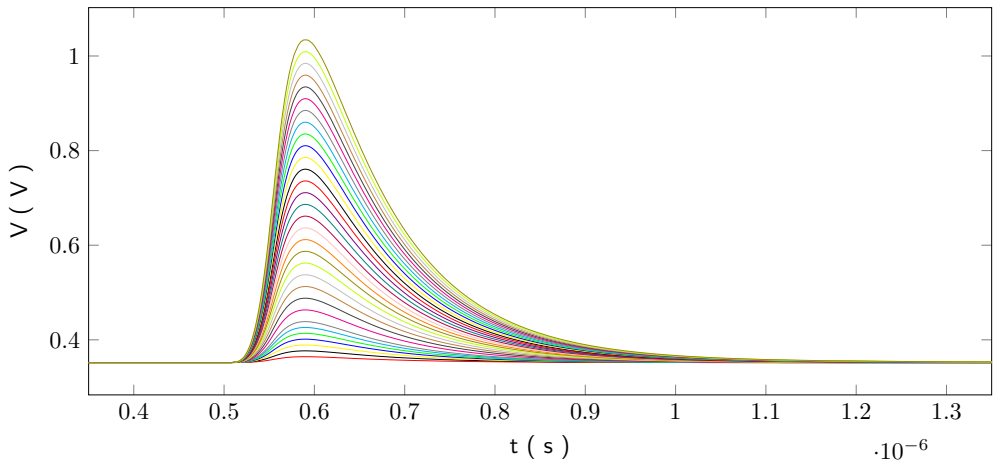


Figure 3.20: Time branch output for input signals from 1 fC to 55 fC.

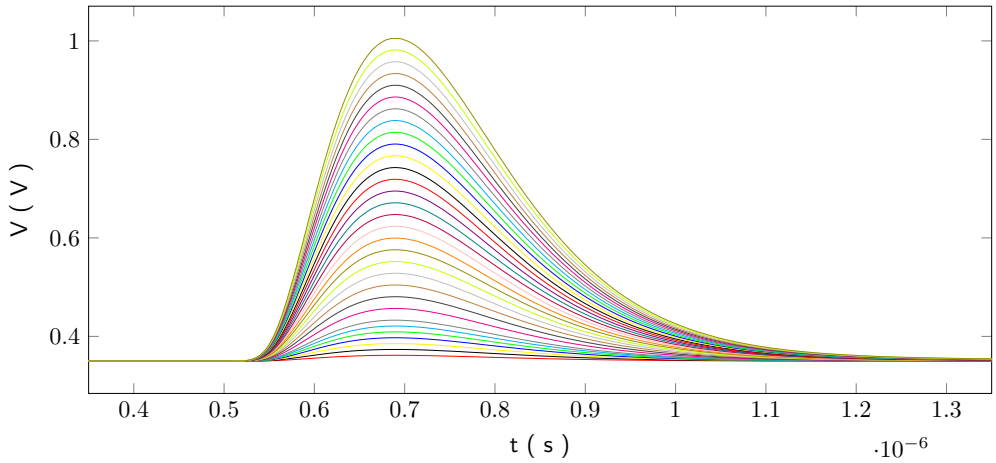


Figure 3.21: Energy branch output for input signals from 1 fC to 55 fC.

From these plots the gain and linearity of the two branches are extracted. The results are displayed in Figures 3.22 and 3.23. The residual non linearity has been evaluated as:

$$NL = \frac{A_n - A_{fit}}{A_{fit}} \tag{3.18}$$

where A_n is the pulse amplitude evaluated for the n point of the plot and A_{fit} is the value extracted from the linear fit.

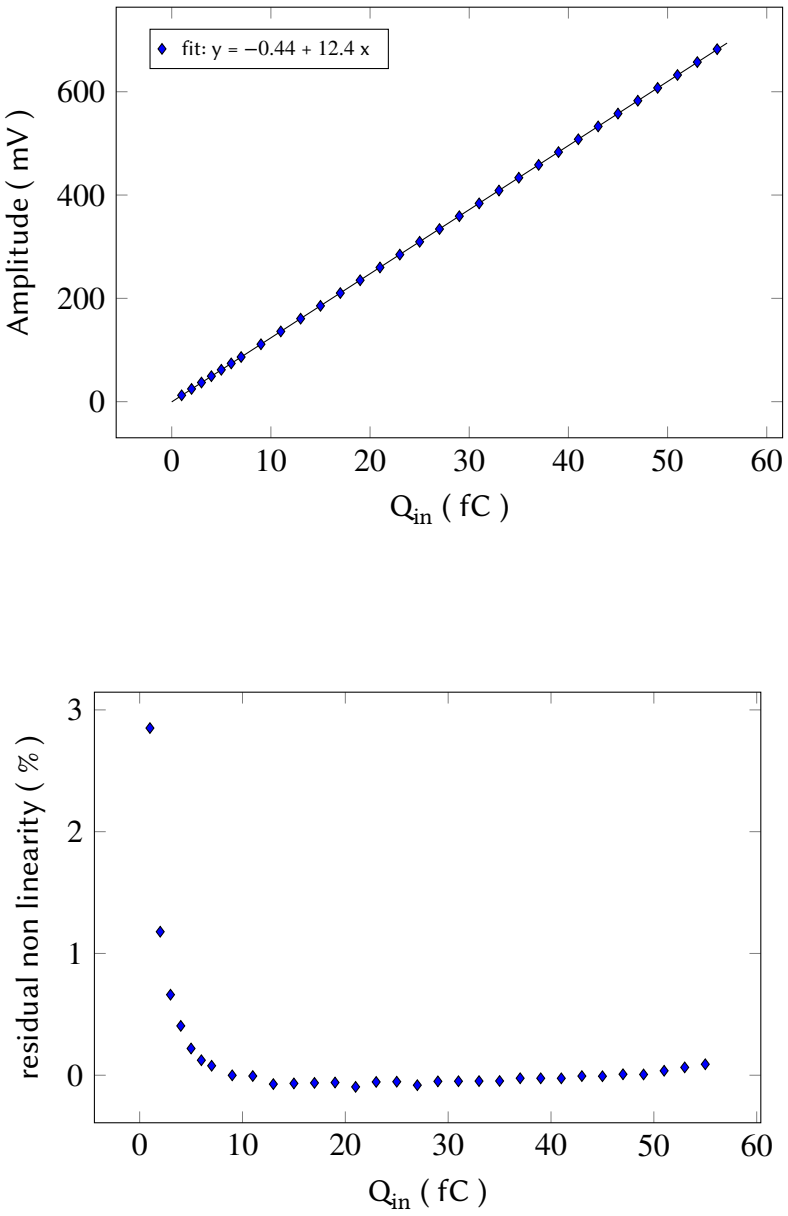


Figure 3.22: Time branch gain and linearity.

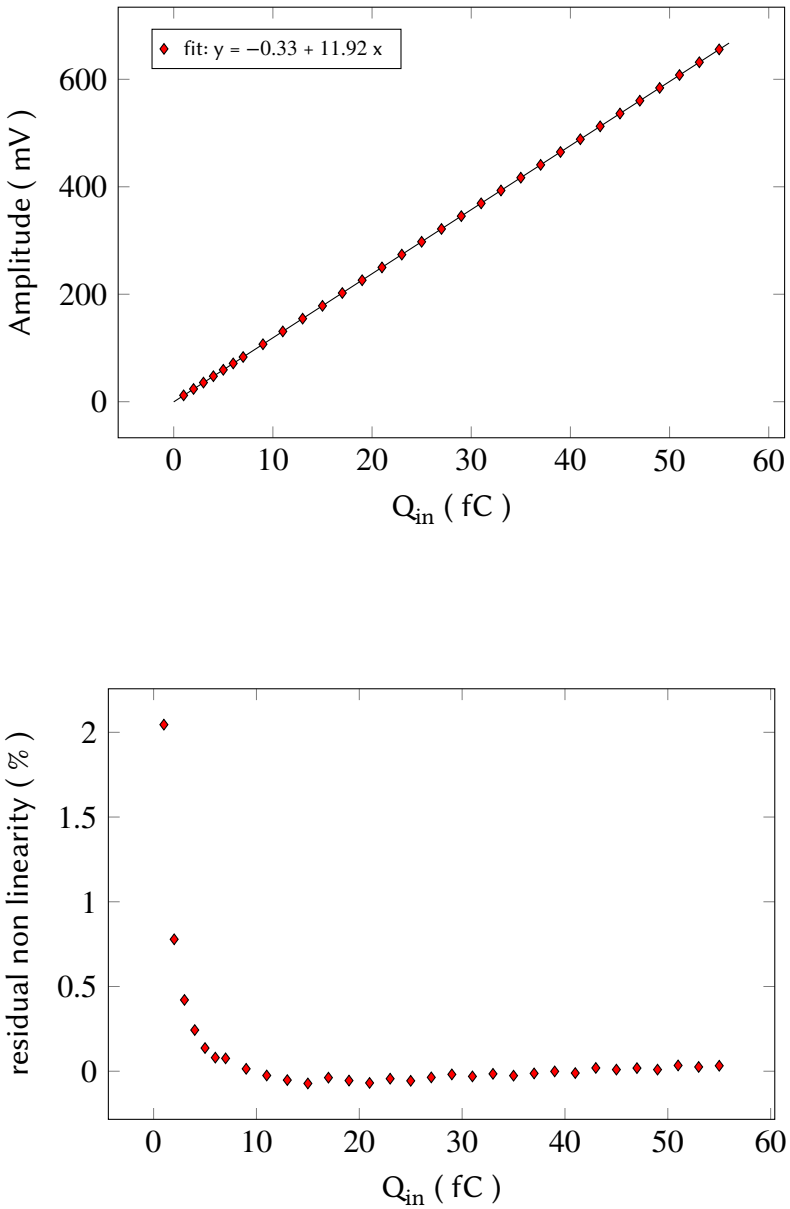


Figure 3.23: Energy branch gain and linearity.

The front-end response is linear for the full range of interest, with a gain of 12.4 mV/fC for the time branch and 11.9 mV/fC for the energy branch.

For what concerns noise, transient noise analyses allow to estimate the effect of the noise on the front-end output signal waveform. In transient noise analyses all noise sources in the circuit inject random noise signals into the simulation during each time step, hence a quite large number of repetitive simulations has to be performed in order to fully assess the system response.

The results of a transient noise simulation (20 iterations) for the output signal of the two branches, performed in the 1 Hz - 10 GHz frequency range for a 2.5 fC input charge, are reported in Figure 3.24 and 3.25. Further analyses about the noise performance of the ASIC will be provided at the end of this chapter.

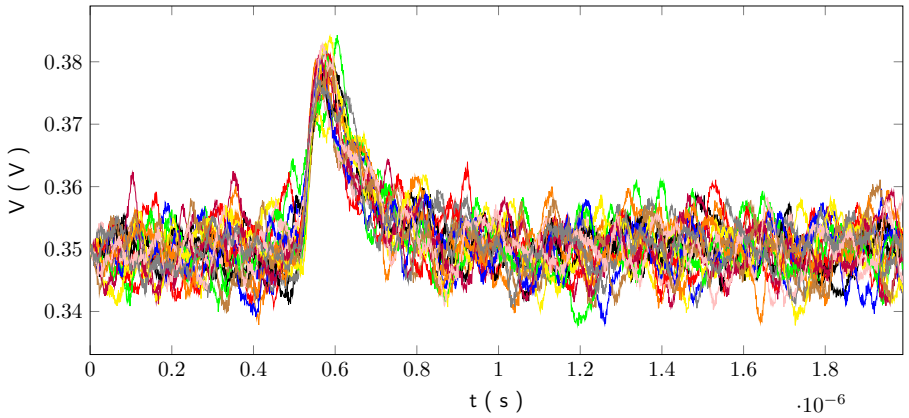


Figure 3.24: Time branch output for a 2.5 fC input signal (20 iterations).

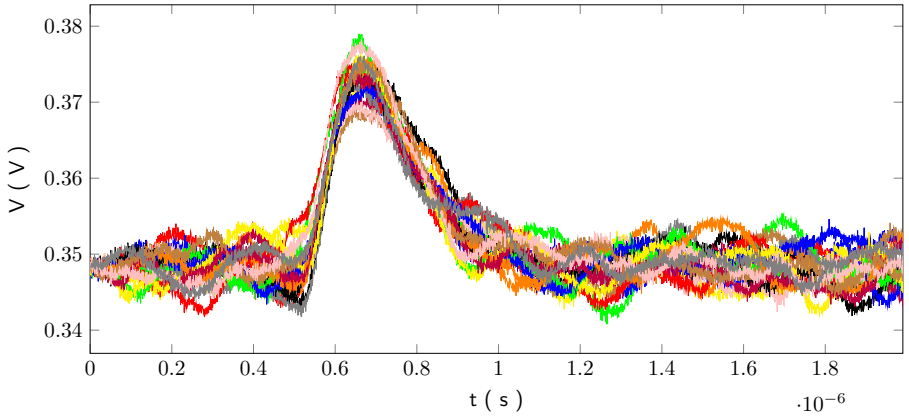


Figure 3.25: Energy branch output for a 2.5 fC input signal (20 iterations).

3.2.4 Discriminators

The two branches have a dedicated dual-stage cascoded leading edge discriminator. The first stage adopts the solution proposed in [52] and is shown in Figure 3.26. Two diode connected PMOS transistors are used to limit the maximum voltage swing for a fast recovery in case of large input signals. The passive load resistors offer a lower parasitic capacitance, improving the circuit speed with respect to the diode-connected loads configuration.

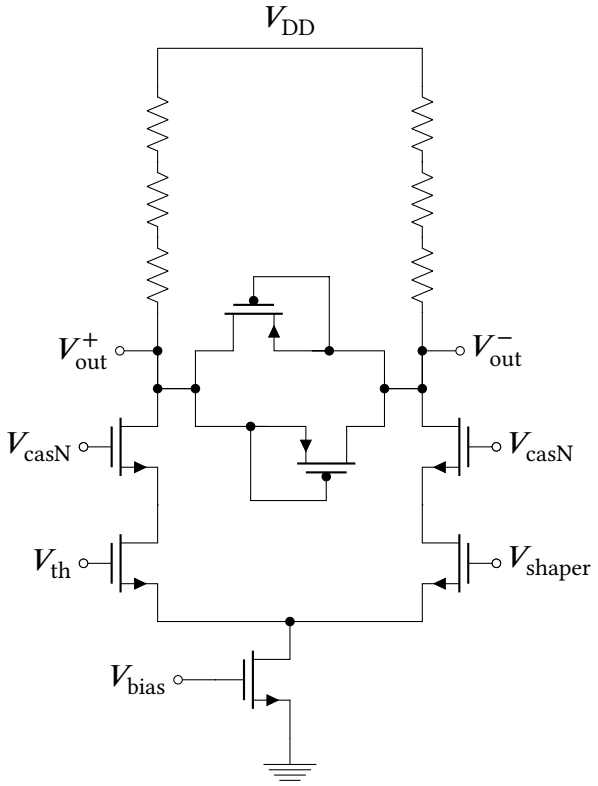


Figure 3.26: Discriminator first stage.

The threshold of each discriminator (Vth_T1 for the time branch, Vth_T2 for the energy branch) can be fine-tuned with a dedicated 6-bit DAC to correct channel-by-channel offsets. Their range (LSB) and DC offset can be controlled by three global configuration registers VcasP_VTH_T1, VcasP_VTH_T2 and I_postamp (refer to Appendix B). The linearity of the threshold DAC is displayed in Figure 3.27. With the default configuration settings an LSB of 5.25 mV results. By sweeping the values of this DAC, threshold scans can be performed, thus allowing to evaluate the noise and efficiency of the front-end.

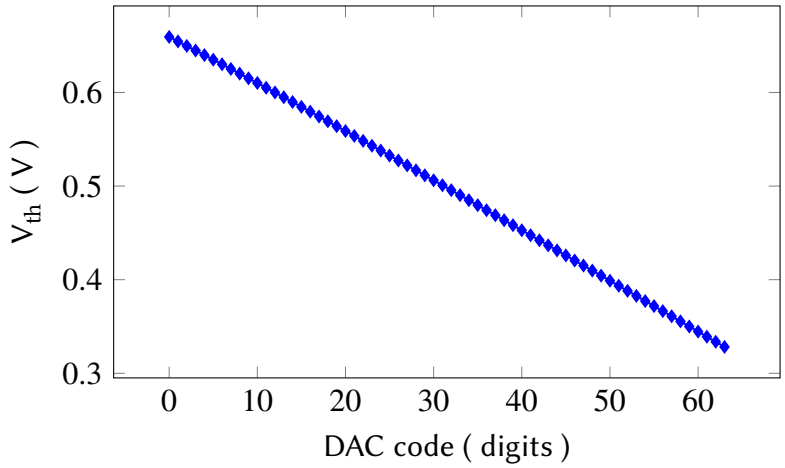


Figure 3.27: Linearity of the DAC used to generate the discriminator threshold.

In the discriminator second stage, shown in Figure 3.28, a 3-bit DAC programmable hysteresis can be enabled to reduce false triggers due to multiple commutations induced by the noise when the signals cross the threshold. The output stage is followed by two CMOS digital inverters in order to generate a well defined logic signal with adequate drive capability.

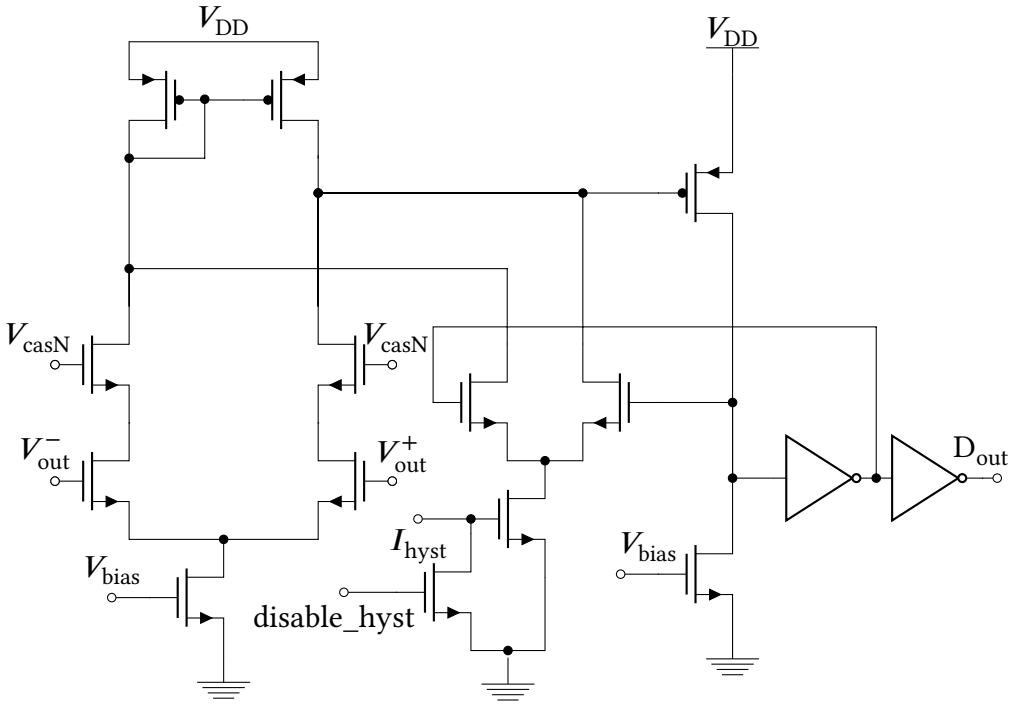


Figure 3.28: Discriminator second stage.

Delay line

The output of the time branch discriminator, before being sent to the channel controller for the trigger generation, is passed through a configurable delay line, shown in Figure 3.29. This line introduces a programmable delay ranging between 1 and 7 ns and allows, in the case of dual threshold readout, to use the time branch discriminator as the reference for the timing measurement, since it provides better timing performance.

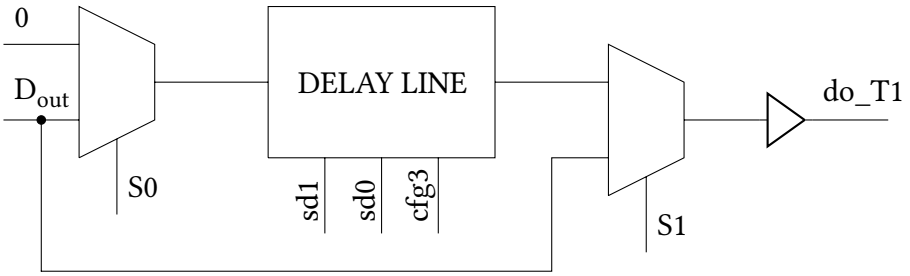


Figure 3.29: Delay line.

Trigger logic

The two discriminators outputs (DO_T1 for the time branch, DO_T2 for the energy branch) are sent to the digital channel controller. A trigger generator inside it handles the generation of the trigger logic signals that control the operation of the S&H circuit, the TDCs and the ADCs. Its operation is defined by four configuration registers, reported in Table 3.4, that can be set on a channel basis.

Register	Description
Trigger_T	time measurement
Trigger_E	event validation (and time measurement in ToT mode)
Trigger_Q	starts of S/H sampling window
Trigger_B	end-of-event (including integration termination)

Table 3.4: Trigger logic configuration registers.

- **Trigger_T** provides the start of the time measurement. The different available configurations are reported in Table 3.5. The delay line after the time branch discriminator implies that the time information is always measured in the fast branch. If Trigger_T is set to 0b01 the rising edge of Trigger_T will always be

given by the time of the rising edge of DO_T1 + DELAY, not by the rising edge of DO_T2.

- **Trigger_E** is used to validate the events and also provides the reference for the second time measurement when in *ToT mode*. The dual threshold readout mode can be enabled by setting Trigger_E = 0b011 (refer to Table 3.6). In this way, the less noisy energy branch is employed for the rejection of noise-induced events.
- **Trigger_Q** provides the start of the sampling window of the S/H circuit. Both discriminators can be used (see Table 3.7), in the default configuration the time branch discriminator is employed due to its lower jitter and time-walk. In *ToT mode* this register is ignored.
- **Trigger_B** indicates the end of an event. According to the values of the other trigger signals the event is validated, and sent to digitization, or discarded. As shown in Table 3.8, also for this register both discriminators can be used.

Value	Trigger_T
0b00	do_T1
0b01	do_T1 AND do_T2

Table 3.5: Trigger_T register.

Value	Trigger_Q
0b00	do_T1
0b01	do_T2
0b11	test pulse

Table 3.7: Trigger_Q register.

Value	Trigger_E
0b000	NOT(do_T1)
0b001	NOT(do_T2)
0b011	NOT(do_T1 AND do_T2)
0b101	do_T1
0b110	do_T2

Table 3.6: Trigger_E register.

Value	Trigger_B
0b000	do_T1
0b001	do_T2
0b011	do_T1 OR do_T2
0b110	test pulse

Table 3.8: Trigger_B register.

The trigger logic processes these signals as follows [53]. The rising edge of one of the trigger signals defines the arrival of a new event and then when **Trigger_B** comes back to zero the event is considered concluded and can be validated, if rising edges on all of **Trigger_T**, **Trigger_E** and **Trigger_Q** have been detected, or otherwise discarded. If the event has been validated it is sent for digitization and transmission. After validation or discard the logic is ready to process a new incoming event.

3.2.5 Analogue TDCs

The TDCs implemented in TIGER are based on clock counters with analogue interpolation to achieve a sub-clock resolution. The same architecture is described in [54] and features four TACs (time-to-analogue converter) and a Wilkinson ADC, common for the four buffers. The simplified TDC block diagram and its principle of operation are shown in Figure 3.30.

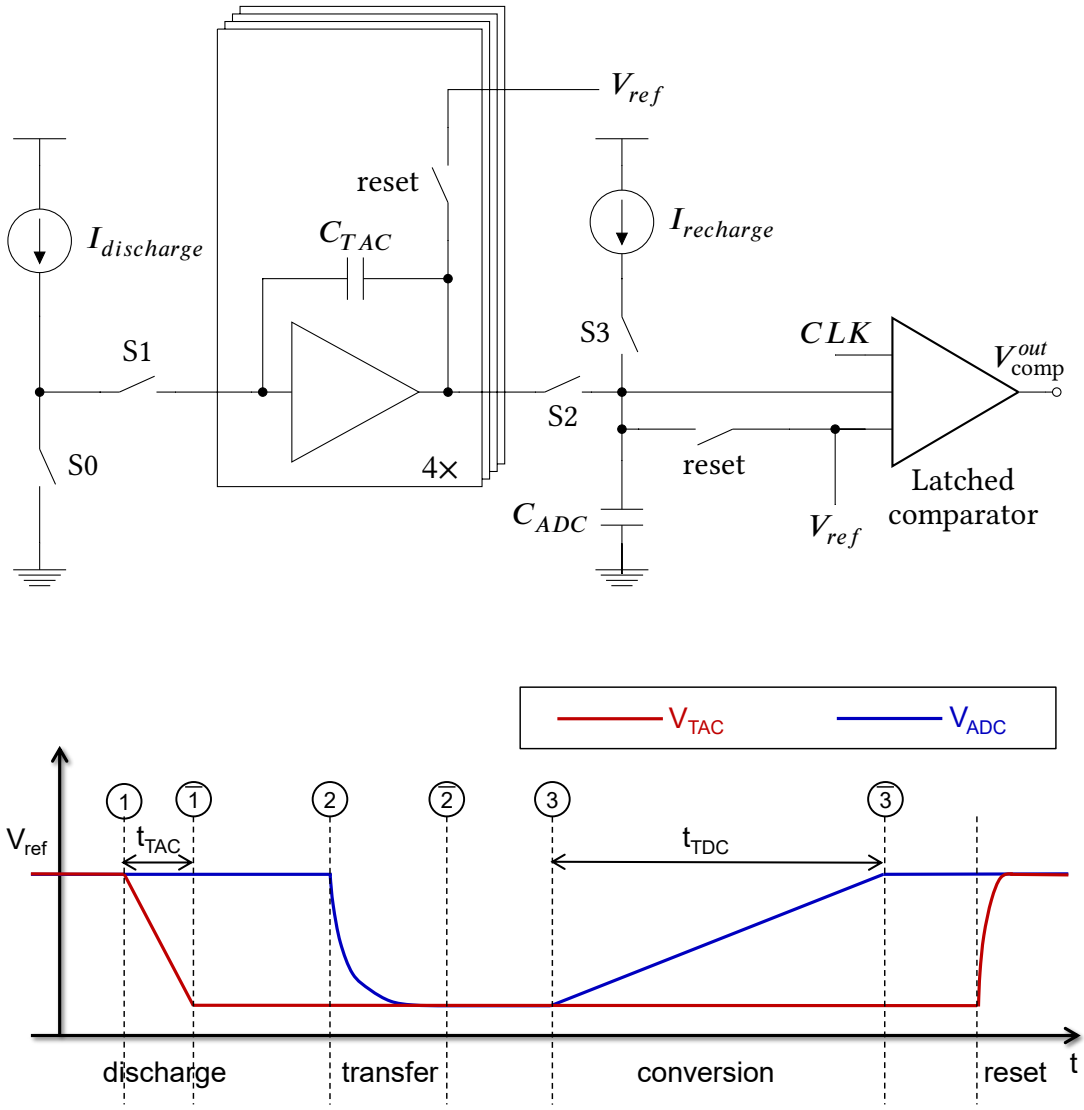


Figure 3.30: TDC block diagram and principle of operation.

In the idle state, the output of the analogue interpolators is preset to V_{ref}. When the discriminator is triggered by an event, the trigger logic generates a signal to open S0 and close the switch S1, so that the current $I_{discharge}$ is now connected to one of the TAC interpolators. Its output (V_{TAC}) is pulled down till to the first clock edge following the hit. After that, the voltage at the interpolator output is transferred into C_{TDC} by closing the switch S2. Finally, S3 is closed and V_{ADC} is recharged up to V_{ref} by $I_{recharge}$. The latched comparator stops the recharge phase when V_{ref} is reached and the clock cycles needed for the recharge process are counted to provide the digitized time information. This solution provides an interpolation factor of:

$$I.F. = \frac{I_{discharge}}{I_{recharge}} \cdot \frac{C_{TDC}}{C_{TAC}} \tag{3.19}$$

Table 3.9 reports the default design values for the TIGER chip. From Equation (3.19) an interpolation factor of 128 results.

Parameters	Values
C_{TAC}	500 fF
C_{TDC}	2 pF
$I_{discharge}$	25 µA
$I_{recharge}$	780 nA

Table 3.9: TDC design values.

This leads, for a 160 MHz clock frequency, to an overall TDC time binning of:

$$\text{time\_bin} = \frac{\tau}{I.F.} \approx 50\text{ps} \tag{3.20}$$

where τ = 6.25 ns is the clock period. As a consequence, the TDCs quantization error is negligible and the time resolution will be limited only by the sensor and the front-end amplifier performance. In order to grant the aforementioned good performance, the discharge and recharge currents must be kept constant during all the signal processing, otherwise a non-linearity will be introduced in the measurement. For this reason, the current sources are implemented using a double cascode which provides very high output impedance and thus very low sensitivity to the voltage variation occurring during the discharge and recharge phases [52]. A global 5-bit DAC (TDC_IREF_CS) generates a reference current which is distributed to all 128 TDCs of the ASIC. In each TDC, this current is mirrored generating the currents $I_{discharge}$ and $I_{recharge}$.

In addition, a 4-bit DAC, available in each TDC, allows to fine tune the discharge current (LSB = 500 nA) and thus to correct potential mismatches between channels, due to variations in the capacitors or currents employed in the conversion, allowing to equalize the time bin of the 64 channels. The remaining offsets between the 128 TDCs, as well as the mismatches between the four TACs of the same TDC, can be corrected offline by means of a look-up table. This method will be discussed in the next chapter.

In case of low event rate, the TAC nodes can be refreshed in order to avoid distortion due to leakage current discharging the active TAC capacitor. The refresh is enabled by the global configuration register TAC REFRESH ENABLE, with a configurable refresh time period (refer to Appendix B).

As mentioned before, the conversion ends when V_{ADC} equals V_{ref}. This information is given by a latched comparator, operating at the chip clock frequency of 160 MHz, which employs positive feedback to quickly regenerate the small voltage difference presented at its inputs to fully digital levels. The latched comparator is shown in Figure 3.31 and features a double regenerative loop delivering a very short response time [52].

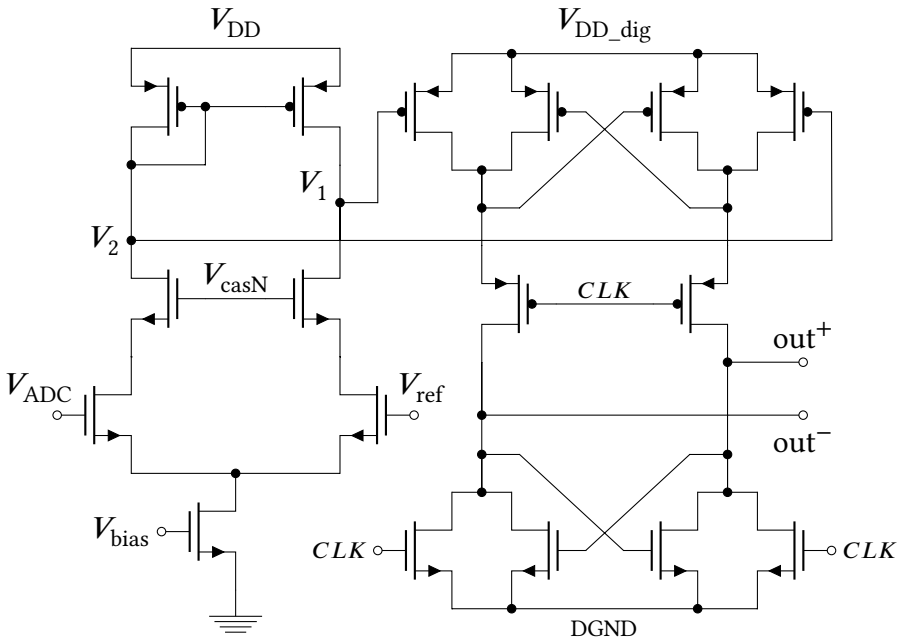


Figure 3.31: Latched comparator (simplified version).

The large conversion time is the major drawback of the Wilkinson ADC technique. With an interpolation factor of 128 and a clock frequency of 160 MHz, the conversion

can take up to 8 µs. In order to mitigate this issue, the analogue interpolators have a multiplicity of 4 to derandomize the arrival time distribution. With this solution, an event rate of 100 kHz per channel can be accommodated with better than 99% efficiency.

Thanks to the relative small area occupied by the TAC, two TDCs can be accommodated in each channel. In this way most of the digital operations are performed inside the channel, including the time to digital conversion and the multi event buffering.

3.2.6 Sample-and-Hold circuit

A Sample-and-Hold circuit (S&H), composed of an array of four sampling capacitors, is available to capture the peak voltage at the output of the slow shaper. The block diagram of the S&H is shown in Figure 3.32 and it works as follows.

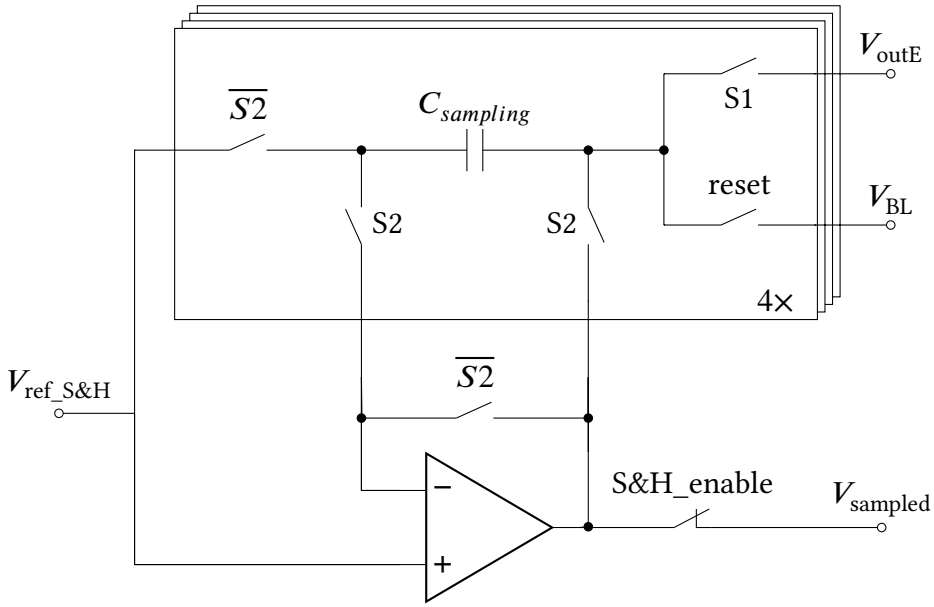


Figure 3.32: Block diagram of the S&H circuit.

In the idle state, the switches S1 and S2 are open and the sampling capacitors are reset to the external baseline reference voltage (V_{BL}). When an event is triggered, the switch S1 of one of the four buffers is closed so that the energy branch shaper output is sampled on $C_{sampling}$ (see Figure 3.33).

The start of sampling time window is given by the **Trigger_Q** signal generated by the channel controller and, in principle, can be provided by both discriminators. In default mode, it is generated by the discriminator connected to the fast shaper in order to reduce the effects of time walk and jitter on this measurement.

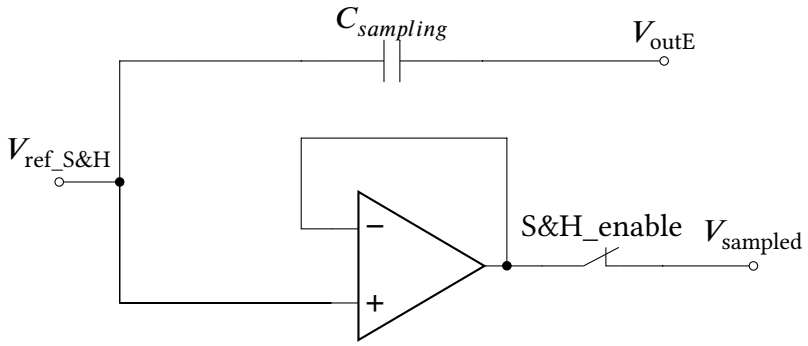


Figure 3.33: S&H circuit: sample phase.

The duration of the sampling time window can be programmed by the user through two channel configuration registers, MIN_INTG_TIME and MAX_INTG_TIME, which define in steps of four clock cycles the limits of the time window.

- If MIN_INTG_TIME = MAX_INTG_TIME the sampling window has a fixed duration set by the value of these two parameters. This is the default configuration that allows to capture the slow shaper output around its maximum.
- If MIN_INTG_TIME < MAX_INTG_TIME the sampling window has a variable duration between the two selected values and the sampling is stopped at the fall of **Trigger_B**. This configuration can be used for debug purposes.

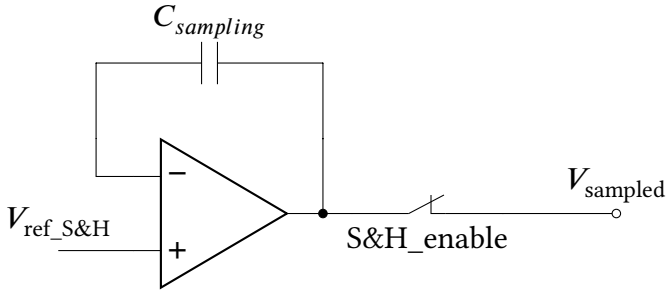


Figure 3.34: S&H circuit: hold phase.

At the end of the sampling time window, S1 is opened again, S2 is closed and the sampled voltage is stored on $C_{sampling}$ (see Figure 3.34).

The S&H_enable switch allows to connect the output of the S&H circuit to the Wilkinson ADC serving the E-branch TDC. Therefore, when in *S&H mode* the TDC of the E-branch is disabled and the charge information is extracted from the S&H circuit, while in *ToT mode* the S&H circuit is disconnected and both TDCs are employed to

provide the Time-over-Threshold information from which the input signal charge can be extracted.

Two factors may limit the performance of the S&H circuit. On one hand, the jitter and time walk of the discriminator affect directly the sampling time window leading to a difference between the shaper peak voltage and the sampled value. On the other hand, if the sampled signal is larger than the Wilkinson ADC voltage reference the conversion does not work properly and the digital output value is not related anymore to the input charge.

The first issue could be addressed employing a traditional, fully analogue peak detector [37], but this solution would require operational amplifiers with rail-to-rail input stage and thus more hardware and power. Figure 3.35 shows the results of a simulation in which the shaper peak voltage and the value captured by the S&H circuit are compared. The error is kept below 2% for the whole dynamic range, hence this approach is fully adequate for our purposes. In any case, an off-chip calibration can also help to correct the charge measuring error if needed.

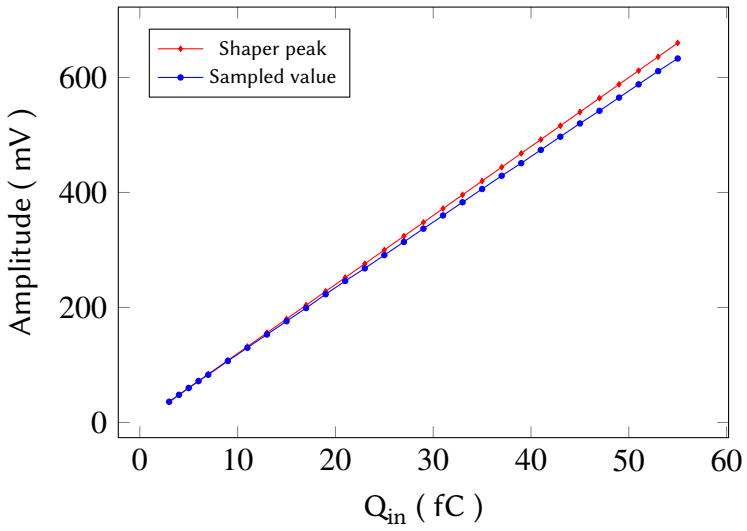


Figure 3.35: Simulation result of the difference between the peak of the shaper output and the sampled value.

The saturation of the Wilkinson ADC can be mitigated increasing the voltage reference used for the conversion, keeping in mind that the transistors of the current sources generating the discharge and recharge ramps must be kept in saturation. The effects of setting a too high voltage reference will be shown in 3.2.8. In this application, the ADC reference voltage has a default value of ~910 mV and can be adjusted off-chip.

3.2.7 Channel controller

A digital channel controller handles the channel configuration, generates the trigger and control signals to drive the S&H circuit, the TDCs and the Wilkinson ADCs and produces the digitized output of the time and charge measurements.

A channel configuration register (TRIGGER_MODE) allows to operate the channel in different modes, as reported in Table 3.10. In default mode, the channels work as described before, while in TDC mode the front-end is bypassed and the discriminators outputs are replaced by an external digital test pulse. In this way the test-pulse is directly injected at the TDCs input, thus allowing to test their response and calibrate them even in case of a malfunctioning of the analogue part. In inverse logic mode, all discriminators outputs are inverted, thus allowing, in principle, to read signals of inverted polarity, but it must be taken into account that some of the stages are optimized for negative polarity input signals. Finally, the last mode allows to mask the channel, turning off all data generation from that channels. This can be useful in case of noisy or disconnected channels.

Value	Description
0b00	default mode
0b01	TDC mode
0b10	inverse logic
0b11	disable channel

Table 3.10: Trigger mode register.

3.2.8 Full-channel simulations

In Figure 3.36 the simulation of an event recorded in *S&H mode* is displayed. In the upper part of the figure the analogue signals are shown: the output of the two shapers, the energy branch sampled peak voltage provided by the S&H circuit, the voltage ramps of the two Wilkinson ADCs, one for the timing measurement and the other for the digitization of the aforementioned sampled signal. In the lower part the digital signals controlling the channel operation are displayed: the discriminator output **DO_T1** generates the **w_coarse_T** signal to save the event coarse time information and the **wtac_T** signal to measure the correspondent fine time information. Moreover, it defines the start of the sampling window, indicated by **wqac_Q**. At the end of the sampling **w_coarse_E**

provides a second coarse time measurement from which the duration of the sampling window can be extracted. The **q_tx** signal transfers the voltages stored in the TAC and S&H capacitors to the Wilkinson ADCs for the conversion. The two latched comparators provide the end of conversion (**eoc**) and a new event, eventually already stored in the buffers, can be digitized. In *ToT mode*, the two branches operate in the same way, **wqac_Q** is replaced by **wtac_E** in order to provide a second fine time measurement which is digitized by the TDC of the energy branch.

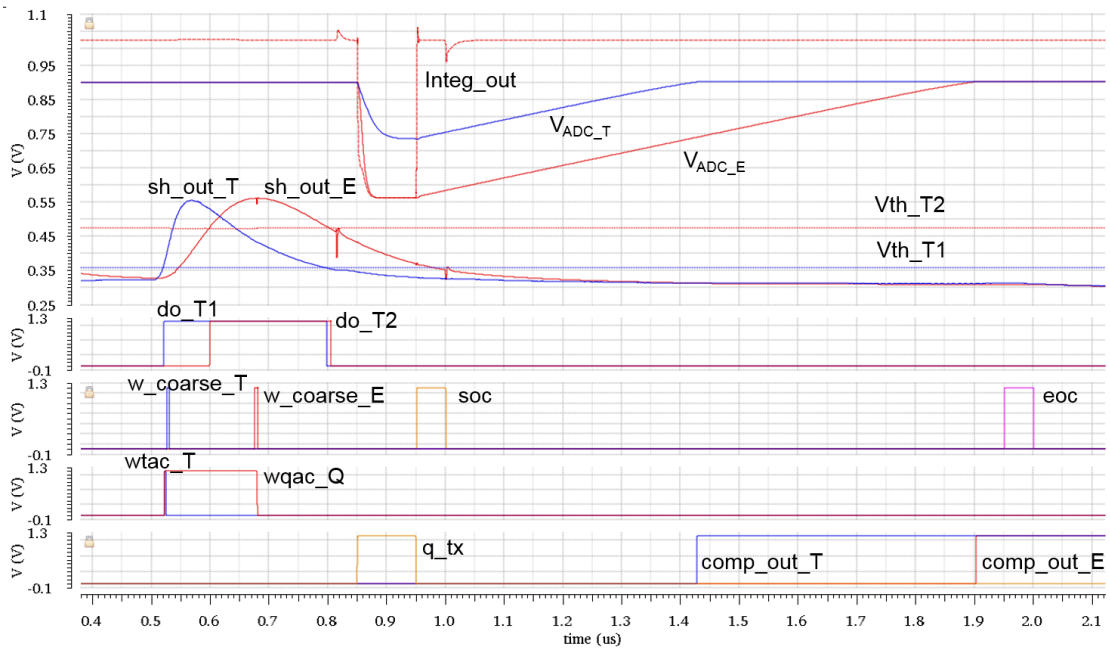


Figure 3.36: Simulation of one event in S&H mode.

We can now study the channel behavior to a high input rate and how the multi-buffering scheme allows to mitigate the issue of the long conversion time of the ADCs. The results from a simulation with an input pulse frequency of about 1 MHz are displayed in Figure 3.37. For simplicity, a single-threshold readout is employed, hence the discriminator output **DO_T1** generates the control signals both for TAC discharging (**wtac_T**) and peak sampling (**wqac_Q**). These two voltages are then digitized by the two Wilkinson ADCs ($\mathbf{V_{ADC\_T}}$ and $\mathbf{V_{ADC\_E}}$). The conversion time is marked by signals **soc** (start of conversion) and **eoc** (end of conversion). It can be observed that while the conversion of the first event is still ongoing a new event occurs. This second event is correctly detected by the control logic and its time and charge information stored in one of the four buffers waiting for conversion. Upon the receiving of the **eoc** signal of

the first event, the conversion of the second event is started. This scheme is repeated for the next events up to the 8th event when all the four buffers are full and therefore the control logic does not record the upcoming event which is discarded. Correct readout operation is recovered for the next event, when a buffer becomes available again. It must be pointed out that this event rate is much higher than the maximum event rate for which the chip has been designed (60 kHz).

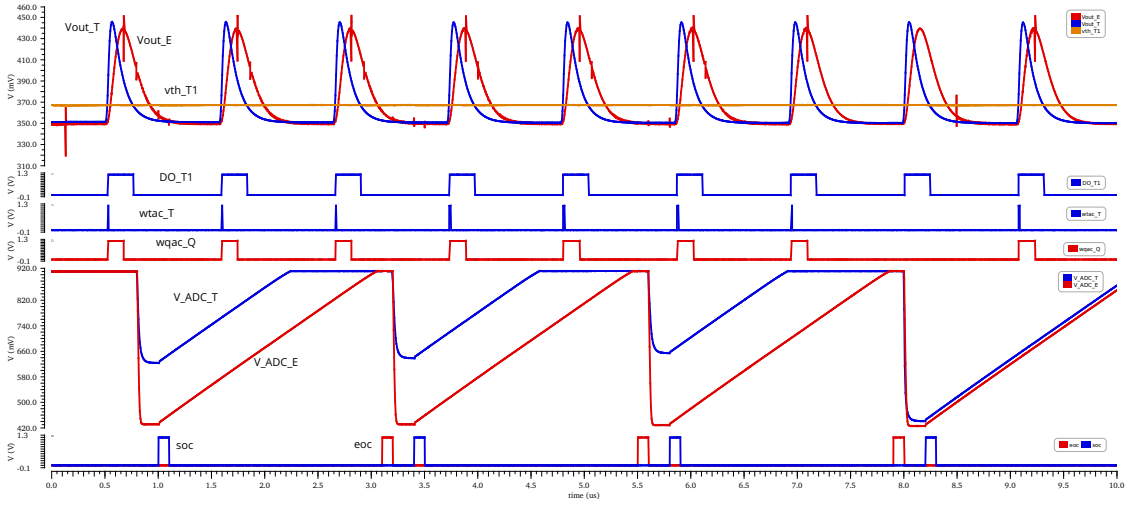


Figure 3.37: Simulation of the channel response to an event rate ∼1 MHz.

Another key point of the ADC design is the generation of the currents used to discharge and recharge the capacitors. These current must be kept constant and are therefore generated from a double cascode current mirror, in which the three transistors must be operated in saturation region for the whole recharge phase. Increasing the ADC voltage reference allows to increase the dynamic range of the charge measurement provided by the S&H circuit, but also decreases the voltage headroom of the current mirror transistors. When the voltage reference is risen too much these transistor are not in saturation and thus the current is not constant. This effect is shown in Figure 3.38, where a V_{ref} of 1.05 V is set (instead of the default value of 910 mV). It can be observed that when the ADC ramp approaches V_{ref} the current start to decrease, the linearity of the measurement is lost and the conversion may never reach its end. As a consequence, as soon as all the buffers are filled, the next events are lost and the channel becomes completely inefficient. This issue can be very critical since it affects all kind of signals, introducing a very high probability of losing a large fraction of the events.

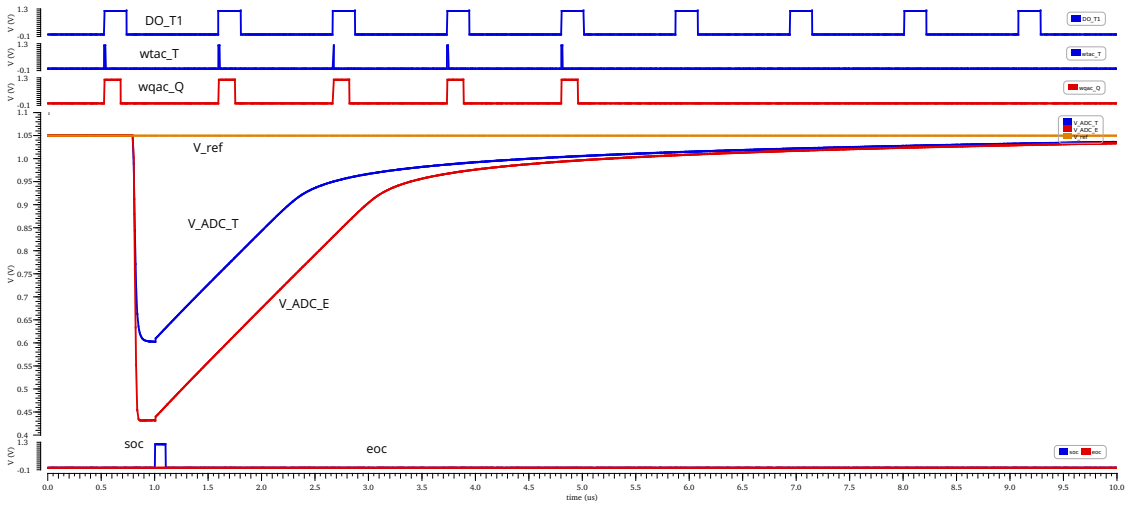


Figure 3.38: Channel simulation with V_{ref} = 1.05 V.

For this reason, the level at which the voltage reference (V_{ref}) is set becomes crucial. A too high value could completely jeopardize the channel response, therefore a trade-off between the channel overall stability and the S&H dynamic range must be found. This issue is intrinsically related to the chip readout architecture and can not be completely avoided. Nevertheless some studies have been carried out in order to implement, for a future version, a scheme which allows to mitigate this effect:

1. **Clock timer:** introducing a timer to stop the conversion after a given time would allow to avoid the loss of events due to the almost-infinite conversion time. Events without the correct digitized values would be stored with a pre-fixed ADC code in order to flag them. This approach does not allow to increase the dynamic range, but the additional information coming from the timer can be exploited to find the best value for V_{ref}.

2. **Level shifter:** in order to increase the S&H dynamic range one could shift downwards the sampled voltage before starting the ADC conversion. This could be accomplished using a source follower with programmable bias current and would allow to operate with a lower V_{ref} while keeping a high dynamic range. For instance, considering that the minimum signal to be converted is the baseline level, whose default value is 350 mV, this scheme allows to gain up to 350 mV of dynamic range.

The channel back-end layout is shown in Figure 3.39. It occupies an area of about 69×2880 μm^2 and consumes about 5 mW. Digital-to-Analogue buffers between the analogue TDCs and the digital controller are employed to transmit the channel configuration bits to the analogue blocks protecting them from the digital switching noise (refer to 3.3.5).

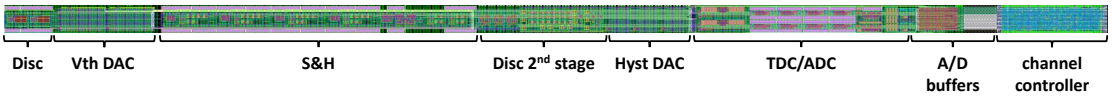


Figure 3.39: Layout of the mixed-signal backend of one TIGER channel.

3.3 Other structures

The core of the ASIC, consisting of the 64-channel block, is surrounded, as shown in Figure 3.40, by other structures providing the bias for the correct channels operation and the interface to the outside world.

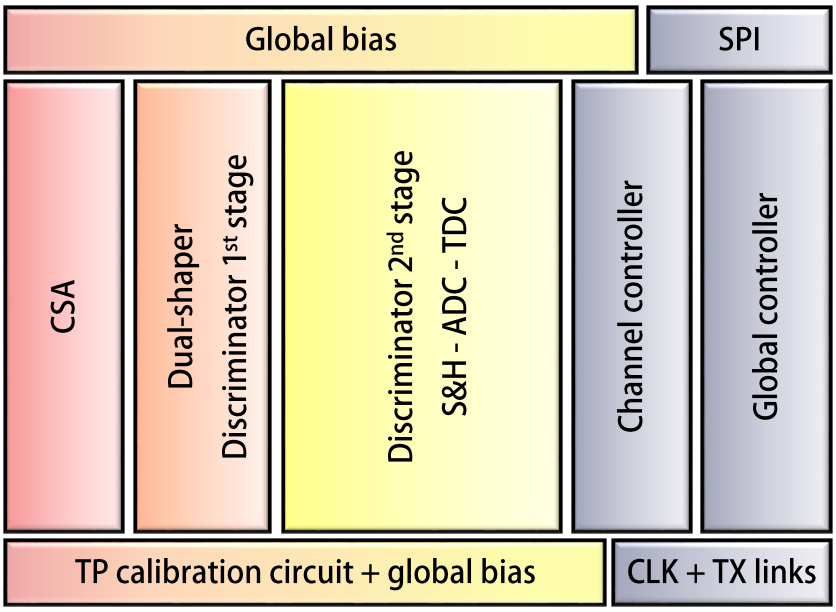


Figure 3.40: Block diagram representation of TIGER architecture. The different colors show the separation of the three analogue and one digital power domains (refer to 3.3.5).

3.3.1 Global controller

The global controller is a digital block that handles the ASIC configuration, the serialization of the digitized data coming from the 64 channel controllers and the off-chip data transmission. A simplified version of the global controller interface is depicted in Figure 3.41.

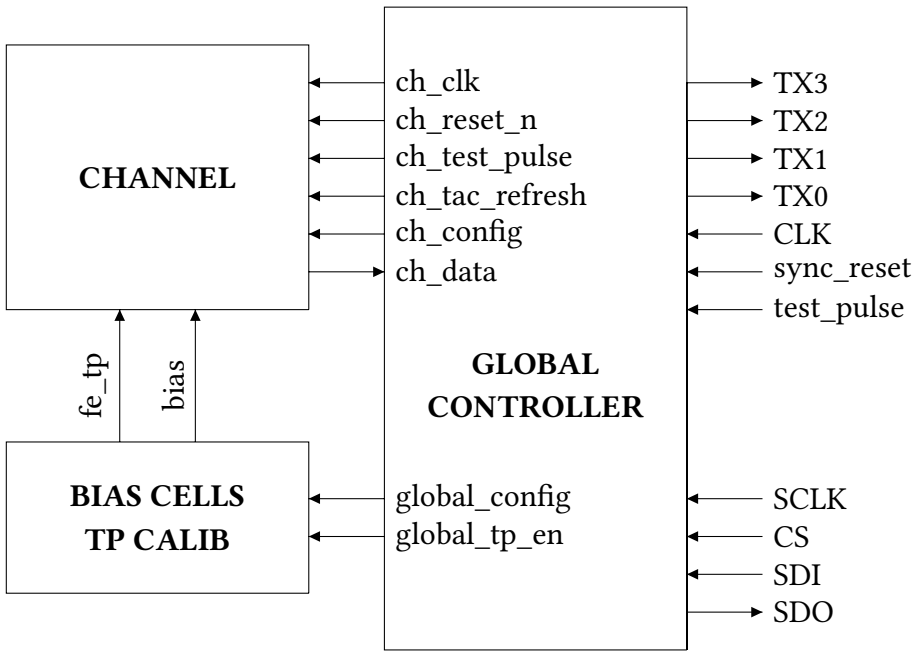


Figure 3.41: Global controller interface.

The digital logic can run with a master clock frequency up to 200 MHz. For system-related reasons, the ASIC will be however used in BESIII with a 160 MHz clock. It has been protected against Single Event Upsets (SEU) by using Triple Modular Redundancy (TMR) for finite-state machines and Hamming encoding for configuration payload. The ASIC configuration registers comprise a 169-bit global configuration vector and a 125-bit per channel configuration vector, that are read and written through an SPI-like interface at 10 MHz. When the ASIC is powered-on, a default global and channel configuration is loaded, allowing for a stable and easy start-up. The **sync_reset** signal can act as a dual purpose reset: a single clock active high strobe resets everything but the configuration registers, while a two or more clock strobe causes the entire ASIC to be reset.

A global counter is propagated to the 64 channels and is used to generate the digitized value of the time and charge measurement. For each valid hit, a 64-bit event-word,

is generated. Besides the event words, TIGER produces two other 64-bit word types, which are used as timing reference and to read several counters present inside the chip to monitor the acquisition status.

1. The **event-word**, identified by the sequence 0b10, contains the information about the digitized event which are reported in Table 3.11. The TAC_id refers to the TAC capacitor used in the time branch, but, since the four buffers of the two branches are kept synchronized by the channel controller, it applies also to the energy branch. The Tcoarse provides the global timestamps of the events and its 16-bit length allows to avoid counter rollover issues, while for the other three digitized words (Ecoarse, Tfine, Efine) a 10-bit resolution is already adequate for this application. The outputs of the energy branch (Ecoarse and Efine) provide different information when operating in ToT or S&H mode.

Bits	Parameter	Description
63:56	K28.1	Start of the 64-bit word identifier
55:54	0b10	Event word identifier
53:48	Channel_id	Channel identifier
47:46	TAC_id	TAC index
45:30	Tcoarse	Leading edge coarse time tag
29:20	Ecoarse	Falling edge coarse time tag (ToT mode) Sampling stop time tag (S&H mode)
19:10	Tfine	T-branch TDC fine time measurement
9:0	Efine	E-branch TDC fine time measurement (ToT mode) ADC charge value (S&H mode)

Table 3.11: Event word content

2. The **frame-word**, identified by the sequence 0x01, includes a progressive clock cycle counter (frame count) and the number of SEU events detected. The frame count allows to keep track of the rollover of the chip master clock counter used to generate the event timestamp (Tcoarse) and is used to match event data coming from different chips. A frame word is generated every 2^{15} clock cycles (half of the Tcoarse counter range) and transmitted off-chip with top-priority. With a 160 MHz clock frequency and a 16 bits coarse time information, the frame interval is:

$$2^{16-1} \cdot 6.25\text{ns} = 204.8\mu\text{s} \tag{3.21}$$

The frame count has itself 16 bits, so it will rollover every 13.42 s. In addition, the SEU count reports the number of Single-Event-Upsets detected by the digital logic during the correspondent frame interval.

3. The **count-word**, identified by the sequence 0x00, is enabled and configured through dedicated registers controlling the counting period (from 2^{18} to 2^{25} clock cycles) and the operation mode, according to Table 3.12. This feature allows to count the events bypassing the digitization and transmission phases that may introduce some limitation. The events to be counted can be selected at different stages inside the channel thus allowing to debug and characterize the behavior of the channel building blocks.

Counter mode	Description
0b0000	Never count
0b0001	Count all clock cycles
0b0010	Valid events
0b0011	Invalid events
0b1000	All events
0b1100	Number of trigger_B rising edges
0b1111	Number of cycles when trigger_B is active

Table 3.12: Counter modes.

A summary of the output words produced by TIGER is reported in Table 3.13.

Data is transmitted off-chip through a set of four LVDS links, working at 2.5 V. The 64-bit words are transmitted over one of the serial links in Single Data Rate (SDR) or Double Data Rate (DDR) mode, with 8b/10b encoding. Control symbol K28.1 (0x3C) marks the beginning of the 64-bit words, while control symbols K28.5 (0xBC) are transmitted during link idle times.

DDR operation at 160 MHz of clock frequency provides a total output bandwidth of 1.28 Gbit/s. This allows to transmit $1.6 \cdot 10^7$ events/s, which is equivalent to a frequency of 250 kHz/channel. The chip rate capability is thus limited by the front-end stage.

EVENT WORD

K28.1	0b10	ch_id 6 bits	TAC	Tcoarse 16 bits	Ecoarse 10 bits	Tfine 10 bits	Efine 10 bits

FRAME WORD

K28.1	0x00	reserved	frame count 16 bits	SEU count 15 bits

COUNT WORD

K28.1	0x01	reserved	ch_id 6 bits	counter value 24 bits

Table 3.13: TIGER output words

3.3.2 Test pulse calibration circuitry

A test-pulse calibration circuit is deployed on the chip periphery for test purposes. It allows to inject into the selected channels input a calibrated signal in order to assess its response even when the ASIC is not connected to the sensor.

The scheme for the test-pulse calibration and injection is displayed in Figure 3.42. Each channel is provided with a capacitor, C_{cal}, connected in series at the pre-amplifier input. A step voltage, V_{cal}, applied across the capacitor injects into the system a charge equal to $Q_{in} = V_{cal} \cdot C_{cal}$.

For each channel, a programmable switch (TP_dis) allows to connect the calibration line to ground, when it is not used, in order to avoid the pick-up of spurious signals. When connected to ground C_{cal} appears in parallel to the amplifier input, hence it may affect its noise performance. In order to make its impact negligible, a small value of C_{cal} = 200 fF has been chosen.

The voltage step, V_{cal}, is generated directly on chip by the periphery test-pulse calibration circuit. Its amplitude can be adjusted using three 5-bit DACs defining the voltage references and bias shown in Figure 3.42: $V_{\text{cal\_ref\_TP}}$, $I_{\text{bias\_TP}}$, $V_{\text{p\_source}}$, $V_{\text{n\_source}}$. An off-chip digital signal drives the switch TP_{ext}, allowing to inject the voltage step on C_{cal}.

The test pulse can be configured for either polarities, selected through the TP_INPUT_POL global configuration bit. If TP_INPUT_POL = 0 the NMOS transistor is turned off, while TP_INPUT_POL = 1 turns off the PMOS transistor.

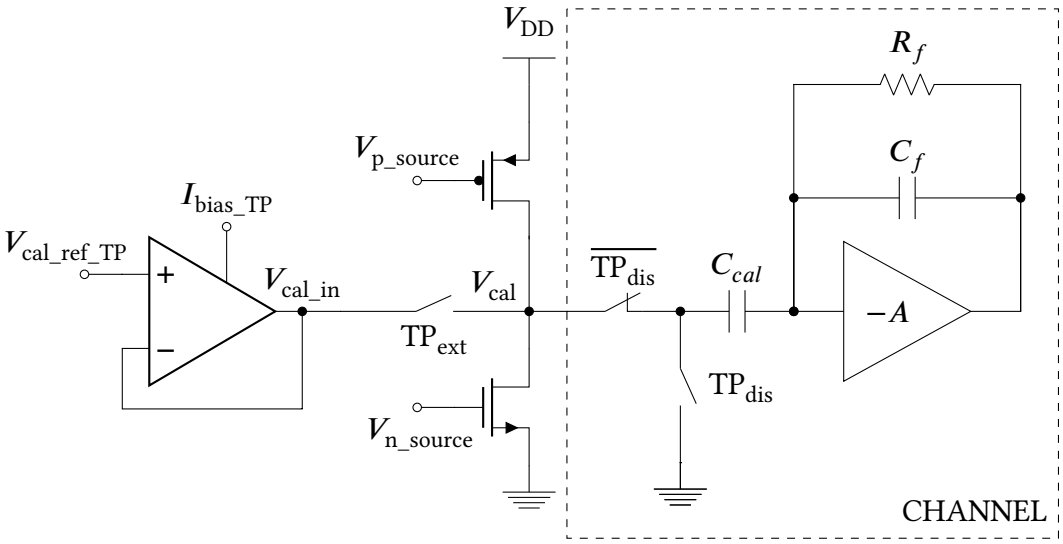


Figure 3.42: Test pulse calibration and injection circuit. On the left, the periphery calibration circuit used to generate a voltage step of programmable amplitude. Inside the dashed box, the channel injection circuit connected at the CSA input.

With TP_{ext} closed, V_{cal} is set to the value defined by V_{cal_in}. When TP_{ext} is opened, the node of the calibration line V_{cal} is abruptly shifted to V_{DD} (TP_INPUT_POL = 0) or to ground (TP_INPUT_POL = 1), thus allowing to generate a positive or negative voltage step which is injected at the the pre-amplifier input through C_{cal}. The current pulse fed to the amplifier is the derivative of the voltage step and can be approximated as a Dirac-delta.

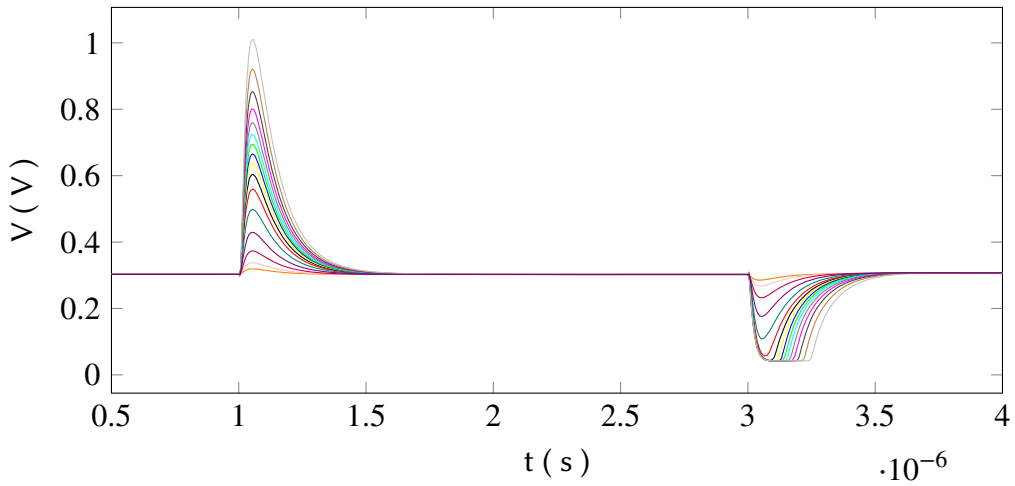


Figure 3.43: Simulation of the front-end response to test-pulses of different amplitude.

Figure 3.43 shows a simulation of the front-end response to a set of test-pulses with different amplitudes. In this simulation, in order to replicate the signals coming from a GEM detector, TP_INPUT_POL is set to 1, hence a negative step is injected at the input of the pre-amplifier and the resulting output is positive, as expected. The full dynamic range is explored by sweeping the values of $V_{\text{cal\_ref\_TP}}$ through its dedicated 5-bit DAC (refer to Appendix B). This simulation also shows the instant when the external digital test-pulse signal is released (t = 3 µs), producing a voltage step of opposite polarity.

3.3.3 ASIC Biasing

The global biasing of the TIGER ASIC features a voltage-to-current converter providing a current, which is weakly sensitive to V_{DD} variations, that defines the LSB of the DAC cells for the generation of all the channels bias. The global voltage reference, V_{bg}, is generated off-chip and driven to the ASIC through a dedicated pad. Its default value is 730 mV, but it can be tuned for performance *vs* power optimization. The circuit is represented in Figure 3.44.

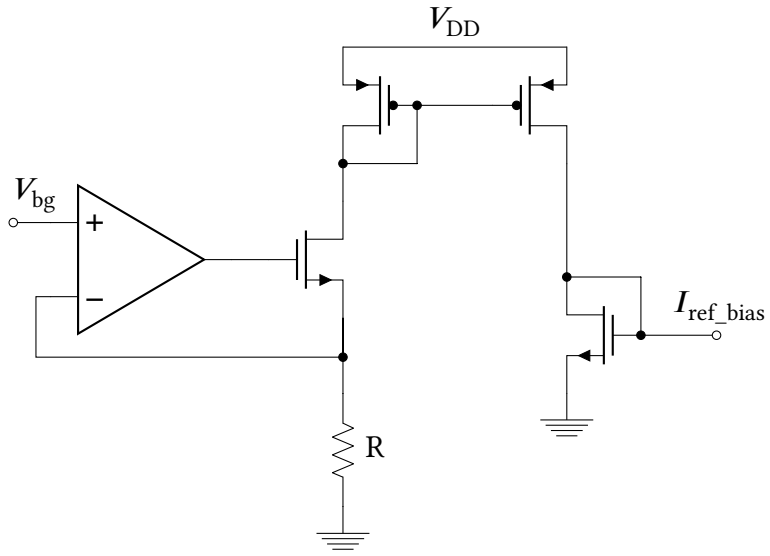


Figure 3.44: Bias reference generator.

Figure 3.45 shows the layout area assigned for the global bias generators and the test pulse calibration circuit. The bias cells share the same power domains of the core blocks to which they are connected. The power distribution partitioning is described in 3.3.5. The configuration bits associated to each DAC are listed in Appendix B.

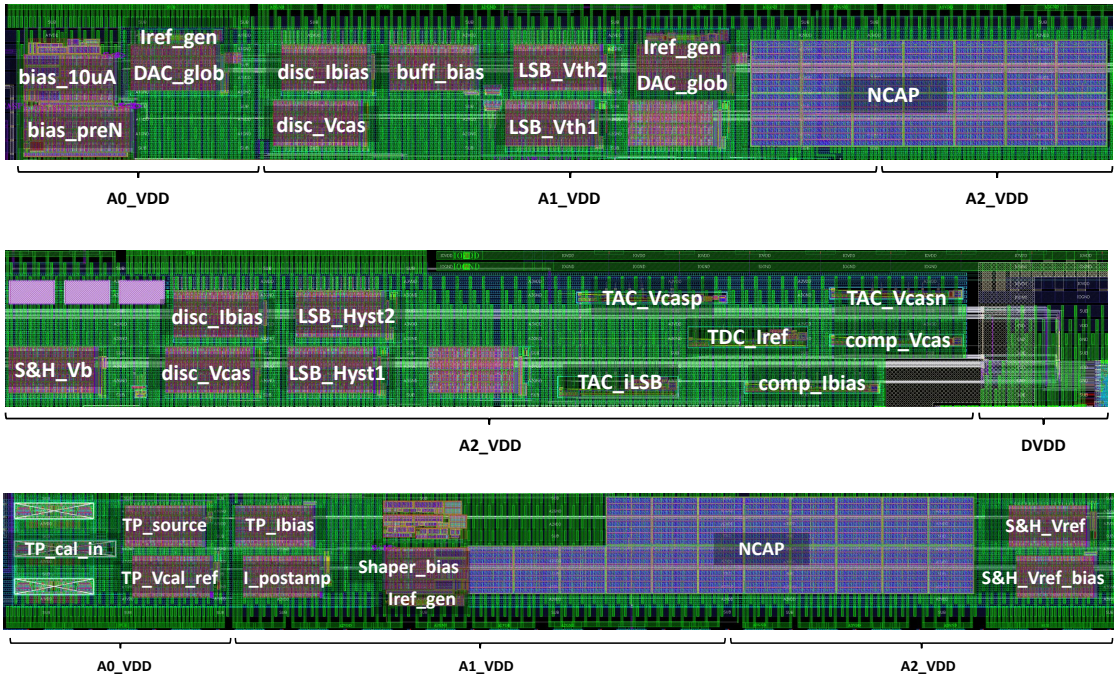


Figure 3.45: TIGER ASIC bias cells.

- **Iref_gen** is the circuit shown in Figure 3.44 to generate the reference current for all the bias cells. It is directly propagated to the TDC bias cells providing the value of the DACs LSB, while for the other cells its value can be adjusted through the DAC_glob cell.
- **DAC_glob** is a global 6-bit DAC which allows to increase or decrease the LSB defined by Iref_gen which is then propagated to all bias cells (TDC excluded). Iref_gen and DAC_glob are reapeated for each power domain.
- **bias_preN** defines the current bias of the CSA input transistor.
- **bias_10uA** defines the current bias of the CSA output stage and its feedback network.
- **disc_Ibias** defines the current bias of the discriminators input differential pair. Given the different power domains, this DAC cell is repeated for both discriminator stages but the configuration bits are the same.
- **disc_Vcas** defines the discriminators cascode voltage. Again, the DAC cell is repeated for both discriminator stages but the configuration bits are the same.

- **buff_bias** defines the current of the output buffers used to drive the two analogue debug outputs implemented in the chip (refer to 3.3.4).
- **LSB_Vth1** defines the LSB of the channel DAC for the time branch threshold fine tuning.
- **LSB_Vth2** defines the LSB of the channel DAC for the energy branch threshold fine tuning.
- **S&H_Vb** defines the current bias of the S&H folded cascode amplifier.
- **LSB_Hyst1** defines the LSB of the DAC to set the hysteresis in the second stage discriminator of the time branch. It shares the same configuration bits of LSB_Vth1.
- **LSB_Hyst2** defines the LSB of the DAC to set the hysteresis in the second stage discriminator of the energy branch. It shares the same configuration bits of LSB_Vth2.
- **TAC_iLSB** defines the LSB of the channel DAC used to correct the TAC discharge current.
- **TAC_Vcasp** defines the current bias of the TAC cascode amplifier.
- **TAC_Vcasn** defines the cascode voltage of the TAC cascode amplifier.
- **TDC_Iref** defines the reference current which is then mirrored to generate the TDC discharge and recharge currents.
- **comp_Ibias** defines the current bias of the Wilkinson ADC latched comparator input differential pair.
- **comp_Vcas** defines the Wilkinson ADC latched comparator cascode voltage.
- **TP_source** defines the bias voltage of the NMOS and PMOS transistors for the generation of the voltage step in the test pulse calibration circuit.
- **TP_Vcal_ref** defines the reference voltage from which the test-pulse voltage step is generated.
- **TP_Ibias** defines the current bias of the voltage buffer of TP_Vcal_ref.
- **TP_cal_in** comprises the circuit that generates the test-pulse voltage step.

- **I_postamp** defines the DC offset of the discriminators threshold.
- **Shaper_Ibias** defines the bias voltages for the shapers and Baseline Holder circuit.
- **S&H_Vref** defines the reference voltage of the S&H when in idle state.
- **S&H_Vref_bias** defines the current bias of the voltage buffer of S&H_Vref.

3.3.4 Debug outputs

For debug purposes, two dedicated pads of TIGER allow to probe the time branch shaper output (Vout_T) and discriminator threshold (Vth_T1) of channel 63. In order to limit the distortion on the observed Vout_T, the signal must be probed with a very low capacitance circuit, e.g. an oscilloscope active probe, and the observed signal may still be slower than the actual Vout_T.

In addition, for each channel, it is possible to use three of the four TX links to assess the response of the discriminator and the digital signals generated by the trigger logic. The different configurations available are reported in Table 3.14. Besides the discriminators output (do_T1 and do_T2) and the trigger signals (trigger_T, trigger_E and trigger_B), it is possible to observe the signals that control the TACs discharge for both branches (wtac_T_p and wtac_E_p) and the signal that defines the time window of the S&H circuit (wqac_Q_p).

These outputs are enabled by a global configuration register (GL_DEBUG_MODE) and the chip must be operated with only one TX link active for real data transmission.

ch_debug_mode	TX3	TX2	TX1
0b00	0	0	0
0b01	do_T1	do_T2	do_E[1]
0b10	wtac_T_p	wtac_E_p	wqac_Q_p
0b11	trigger_T	trigger_E	trigger_B

Table 3.14: Digital outputs for debug purposes.

[1] not present in TIGER, it was implemented for the TOFPET2 ASIC

3.3.5 Power distribution

The power supply is distributed through a power grid implemented using the top two thicker metal layers (M7-M8). In mixed-signal integrated circuits the switching noise of the digital circuitry can propagate to the analogue part through the power and grounding buses. Switching and sensitive circuits are thus separated by partitioning the power supply network in the following power domains:

- **A0_VDD**, **A0_GND**: front-end CSA amplifier, test-pulse calibration circuit
- **A1_VDD**, **A1_GND**: shaper and discriminator first stage
- **A2_VDD**, **A2_GND**: S&H circuit, discriminator second stage, TDC, ADC, digital to analogue buffers
- **DVDD**, **DGND**: channel controller, global controller

The chip area allocated for each power domain is displayed in Figure 3.46. Isolation between digital and analogue sectors and sub-partition of the analogue power domain allow to separate the sensitive input stage circuitry from the analogue/digital interface.

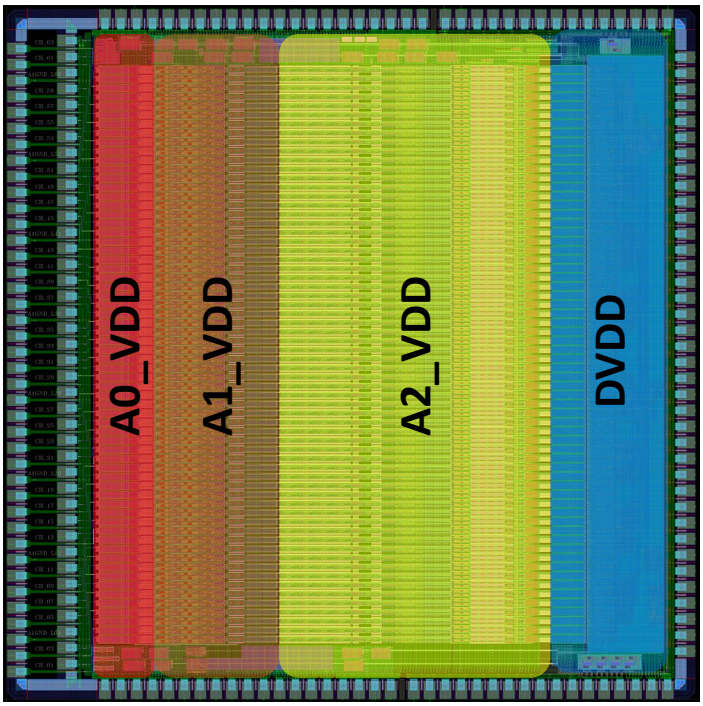


Figure 3.46: TIGER power domains partitioning.

However, the digital and analogue domains are unavoidably interconnected due to the transmission of discriminator signals (Analogue-to-Digital), trigger signals and configuration bits (Digital-to-Analogue). Every configuration bit is buffered in the analogue domain using two cascaded inverters that allow to protect the analogue part from the digital switching noise.

3.4 ASIC layout

The chip is organized as shown in Figure 3.47. The core is composed by 64 parallel channels, each of which comprises an analogue front-end, a mixed-signal back-end and a digital controller. The chip periphery includes bias cells to generate the references for the channels and a test pulse calibration circuit to test its response. A digital global controller handles the communication between the chip and the outside world.

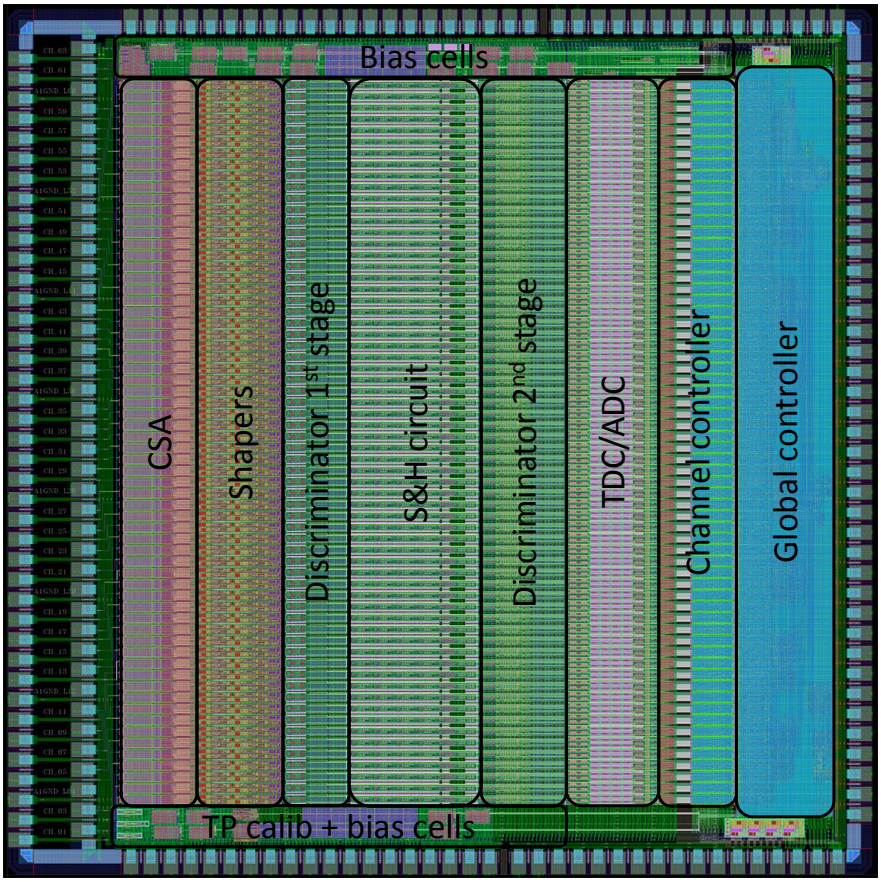


Figure 3.47: TIGER full ASIC layout.

The ASIC pinout is shown in Figure 3.48. The 192 pads are organized in the following way :

- 80 pads, arranged in two 40-pads columns, on the left side of the chip, hosting the 64-channel inputs and the analogue power domain for the Charge Sensitive Amplifier.
- 38 pads on the right side of the chip, hosting the ASIC digital power domain.
- 37 pads on the top side of the chip and 37 pads on the bottom side of the chip, hosting power domains for the shaper stage and the mixed-signal part, external voltage references, analogue debug outputs and digital I/Os.

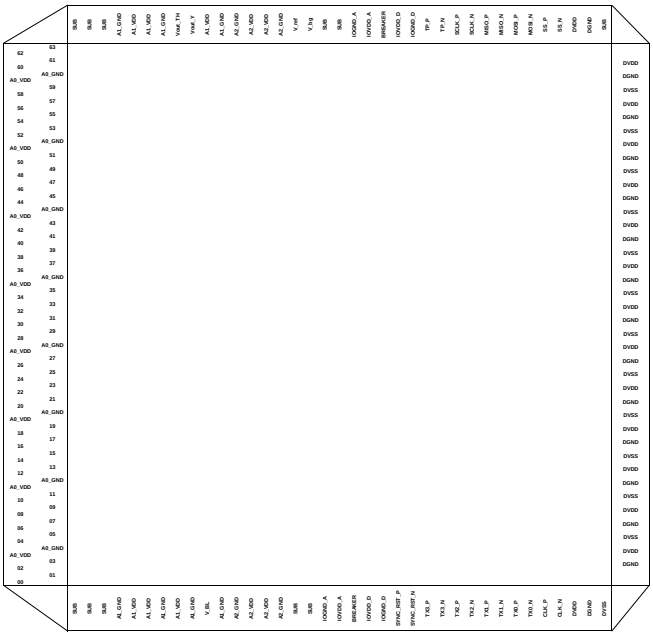


Figure 3.48: TIGER padring.

During the ASIC design phase it was assured that no critical analogue signal was routed close to a digital signal. The sensitive pre-amplifier inputs are on the left hand side of the die, while the fast LVDS IO signals are on the bottom-right and top-right hand side of the die, separated as much as possible.

3.5 Performance summary

This section provides a summary of TIGER performance and specifications. The results shown here are obtained from schematic and post-layout simulations and they will be compared to the measured performance in the next chapter.

3.5.1 Noise

The noise of both branches has been evaluated. Figure 3.49 shows the noise at the output of the time branch shaper as function of the input capacitance obtained from both schematic and post-layout simulations. For C_{in} = 100 pF a 3 mV noise results, with a 5% increment from schematic to post-layout values. The time branch performance will be further investigated in the next pages discussing the effects of jitter and time-walk on the system time resolution.

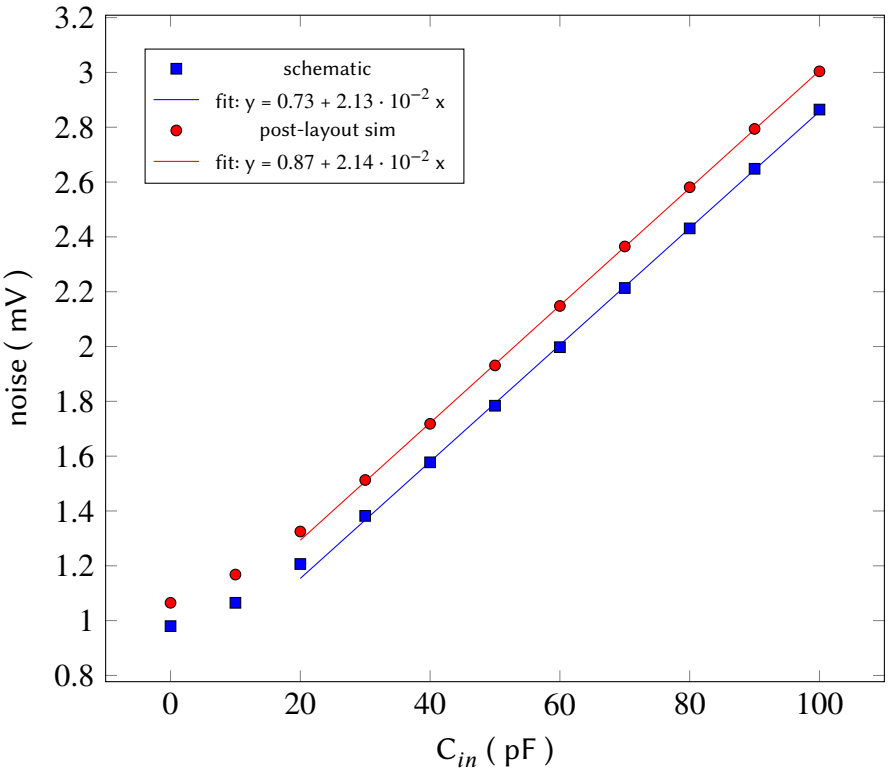


Figure 3.49: Time branch output noise.

The energy branch input-referred noise, expressed in Equivalent Noise Charge (ENC), as a function of the input capacitance is displayed in Figure 3.50, showing for C_{in} = 100 pF a ENC less than 1500 electrons. Here the increment from schematic to post-layout simulations is only 2%, mainly due to the higher shaper time constant that makes this branch less sensitive to parasitics introduced in the layout phase.

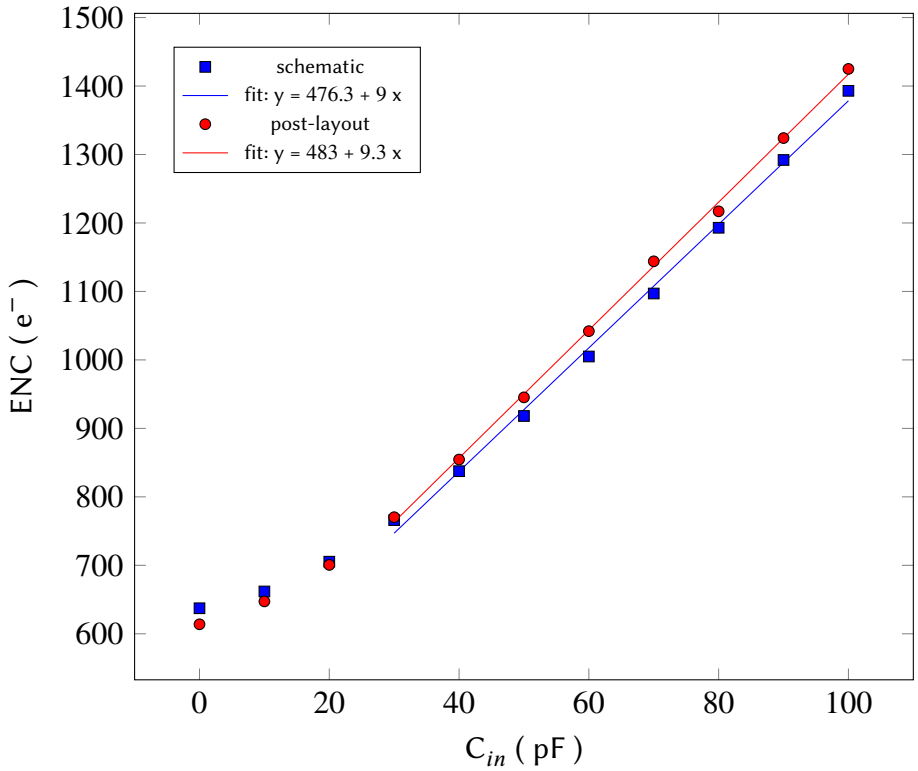


Figure 3.50: Energy branch equivalent noise charge.

One important aspect is the fact that in these simulations it is also included the protection circuit installed at the input of each channel on the board hosting the chip. A 22 Ω resistor connected in series to the channels input to protect them from the GEM discharges has a major contribution on the noise level.

3.5.2 Jitter

In principle, the overall time resolution is limited by the quadratic sum of the front-end time jitter (including also the discriminator response) and the TDC quantization error. Since the TDCs resolution is expected to be below 100 ps, we can affirm that the system time resolution will be affected only by the front-end performance.

In order to estimate the front-end jitter, simulations for different input capacitance and charge values have been carried out evaluating the timestamp provided by the discriminator. The results are depicted in Figure 3.51.

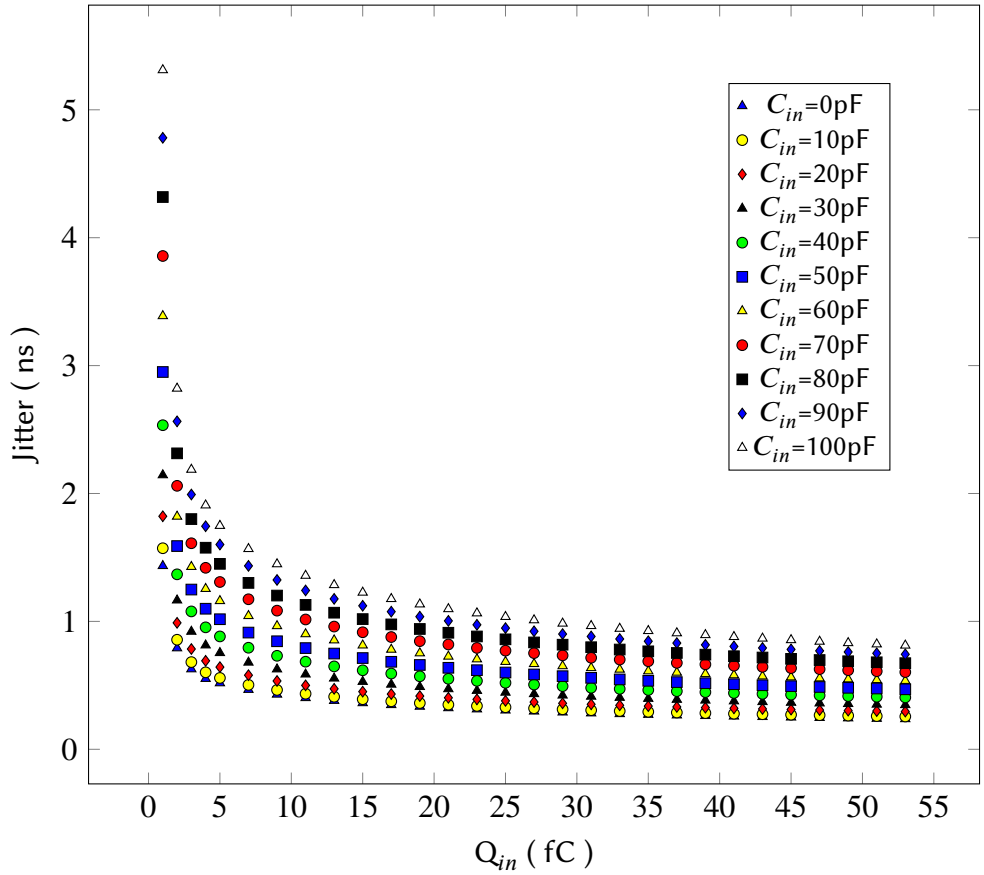


Figure 3.51: Time jitter as a function of input charge for different input capacitances.

3.5.3 Time Walk

The leading edge discriminators of TIGER are intrinsically affected by time-walk. Nevertheless, this effect can be studied and then corrected. In Figure 3.52 the time offset due to time-walk simulated for different input charge values and threshold settings is shown. Time walk depends on the signal amplitude, thus can be corrected using the charge measurement which is also provided by TIGER. It can be observed that, in order to meet the time resolution requirement, this correction is mandatory even with a low-threshold configuration.

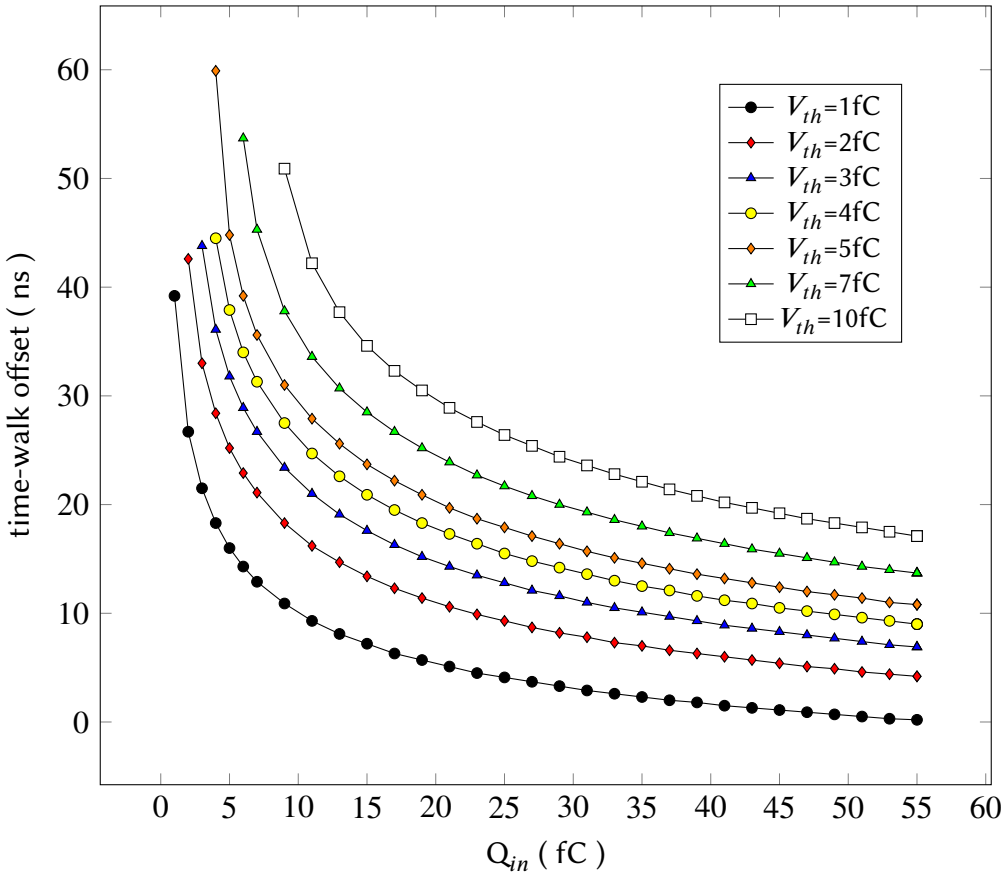


Figure 3.52: Time walk curve as a function of input charge for different threshold levels.

Finally, Table 3.15 lists the specifications of the TIGER ASIC.

Parameter	Value
Number of channels	64
Clock frequency	160-200 MHz
Input capacitance	up to 100 pF
Input dynamic range	2-50 fC
Front-end gain	12 mV/fC
Energy branch ENC	<1500 e^-
Time branch jitter	<5 ns
Time measurement	Leading edge discriminator + analogue TDC
TDC time binning	30-50 ps
Charge measurement	Peak sampling + ADC or Time-over-Threshold
Maximum event rate	60 kHz/channel
Readout Mode	Trigger-less
TX links	4, LVDS
Max. output data rate	1.6 Gb/s (200 MHz, DDR)
Configuration	10 MHz SPI-like
Power consumption	10-12 mW/channel
Process	CMOS 110 nm

Table 3.15: TIGER ASIC specifications.

Chapter 4

Test results

The ASIC has been fabricated in a 110 nm CMOS process with 8 metal layers. The die occupies an area of 5×5 mm^2. Figure 4.1 (left) shows the chip wire-bonded on the test printed circuit board, while on the right a microphotograph of the ASIC is displayed.

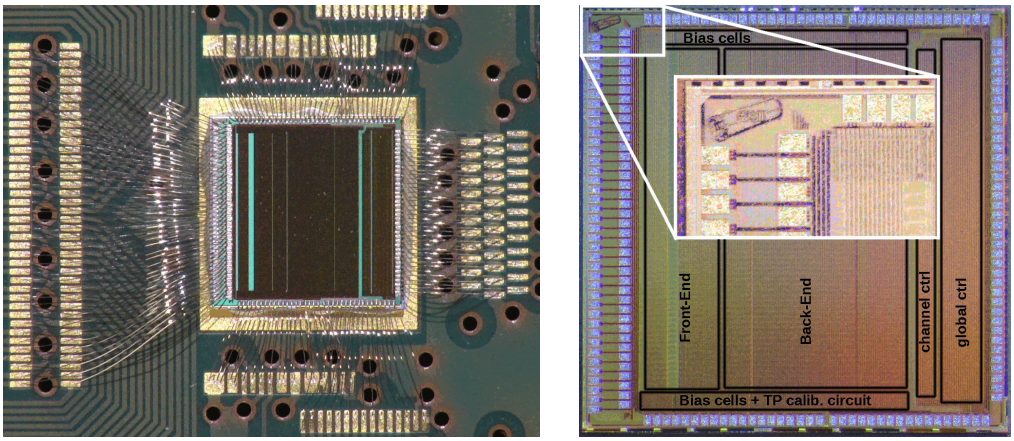


Figure 4.1: One TIGER ASIC wire-bonded on the test printed circuit board (left) and TIGER microphotograph (right).

A first prototype version, named TIGERv0 [55], was submitted to the foundry for fabrication on May 2016 in a cost-effective Multi-Project Wafer (MPW) run for the validation of the design. Due to a very strict schedule imposed by the collaboration, the prototype already included all the blocks foreseen in the final system, thus reducing the overall time of the design cycle.

The tests on the prototype started by the end of 2016 and a strong temperature-dependent baseline shift was observed at the shapers output. Besides this instability, the chip was successfully characterized delivering the required performance [56]–[58].

The baseline issue was thoroughly assessed and a new version (TIGERv1) was submitted in August 2017 for mass production in order to fully instrument the CGEM-IT detector.

The new version included an improved shaper-BLH stage and some minor changes in the TDC layout. TIGERv1 was tested during the first half of 2018 and was found completely bug-free. No baseline drifts were observed and, as a consequence, the input dynamic range was increased matching the value expected from simulation. The design revisions of TIGERv1 are discussed in Appendix A.

The results presented in this chapter, except where otherwise specified, are referred to the final TIGERv1 version.

4.1 Test setup

This section presents the experimental setup developed for the electrical characterization of the ASIC. A dedicated test board was designed in order to allow a thorough characterization of ASIC providing some trimming functionalities which are not present in the final Front-End Boards due to area constraints.

At that time, the off-detector electronics was not ready yet, hence a small DAQ system to efficiently readout the ASIC was developed within the Turin INFN Electronics Laboratory.

4.1.1 ASIC Test board

For the ASIC electrical characterization a custom test printed circuit board has been developed by the Turin INFN Electronics Laboratory [59]. The testboard, shown in Figure 4.2, hosts one chip and is equipped with six trimmers that allow to fine tune the external bias voltages of the ASIC:

1. **A0VDD** is the first analogue power supply, connected only to the CSA power domain.

2. **A1VDD** comprises both A1_VDD and A2_VDD power domains described in 3.3.5. In the final Front-End Boards all analogue power supply domains are provided by one voltage regulator, hence during the test phase they have been kept at the same value.

3. **DVDD** is the digital power supply used by the 64 channel controllers and the

global controller. A different voltage regulator is used to generate the fixed 2.5 V for the LVDS drivers.

4. $\mathbf{V}_{\mathrm{BL}}$ is the external reference voltage used by the Baseline Holder circuit (refer to 3.2.3) to lock the DC voltage at the output of the two shapers.

5. $\mathbf{V}_{\mathrm{bg}}$ is the external reference voltage to generate the current which defines the LSB of all bias DACs, as described in 3.3.3.

6. $\mathbf{V}_{\mathrm{ref}}$ is the Wilkinson ADC reference voltage (see 3.2.5).

In the final Front-End Boards these values are generated using surface mounting device (SMD) components and thus they cannot be easily changed. Therefore, in this phase of the tests their best values have been carefully investigated.

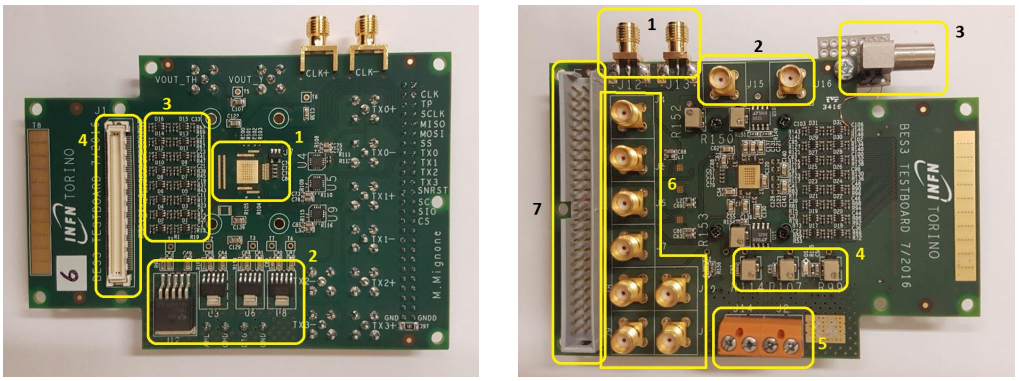


Figure 4.2: Close up of the TIGER testboard. In the left picture the bottom side of the test board: chip pads (1), voltage regulators (2), channels input protection circuits (3), GEM anode connector (4). In the picture on the right the top side of the test board: clock ports (1), analogue debug output ports (2), external TP injection and capacitance circuit (3), bias voltage trimmers (4), power supply ports (5), digital debug output ports (6), FPGA ribbon cable connector (7).

In addition, the test board features several ports to probe the ASIC debug outputs described in the previous chapter. In a very early phase of the ASIC electrical characterization, the digital debug outputs have been observed in order to assess the correct behavior of the control logic. The two analogue ports, probing the channel 63 time-branch shaper output and the threshold of the discriminator coupled to it, allowed to directly observe the front-end response and extract useful information about its gain and dynamic range as well as the LSB and linearity of the discriminator DAC.

An external injection circuit was installed on the testboard at the input of channel 63 in order to inject signals of well known charge. The circuit consists of a 1 pF capacitor, connected in series to the input of channel 63, and a 50 Ω termination resistor. In this way, it was possible to calibrate the test pulse generator embedded in the chip and then assess the response of the 64 channels.

Furthermore, the testboard was equipped with an additional external circuit that allowed to connect at the input of channel 62 capacitors of different values and thus evaluate the noise as a function of the input capacitance.

4.1.2 DAQ system

For the first electrical tests, since the full system with the GEMROC readout was not ready yet, a small readout setup (see Figure 4.3) has been developed. It is based on a Xilinx Virtex 6 FPGA Evaluation board (ML605 Evaluation kit, [60]), connected to the testboard with an FMC connector (one FPGA board can handle up to two testboards). The FPGA board manages the ASIC configuration and data reception and generates a test pulse with adjustable timing which is delivered to the ASIC for testing purposes.

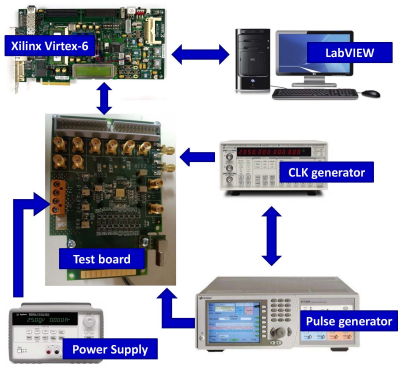


Figure 4.3: Main building blocks of the DAQ system.

An Ethernet cable connects the FPGA board to a PC where the data acquisition is managed through a LabVIEW program. Within the LabVIEW GUI, displayed in Figure 4.4, each ASIC configuration register can be programmed allowing to test the chip with different settings in order to find the optimal values for its operation. Data are analyzed online and displayed on a dedicated window and also saved on a text file.

The 160-200 MHz clock can be synthesized either by the FPGA board or with a low-jitter Stanford Research CG635 Clock Generator (up to 2.05 GHz square wave clocks, [61]).

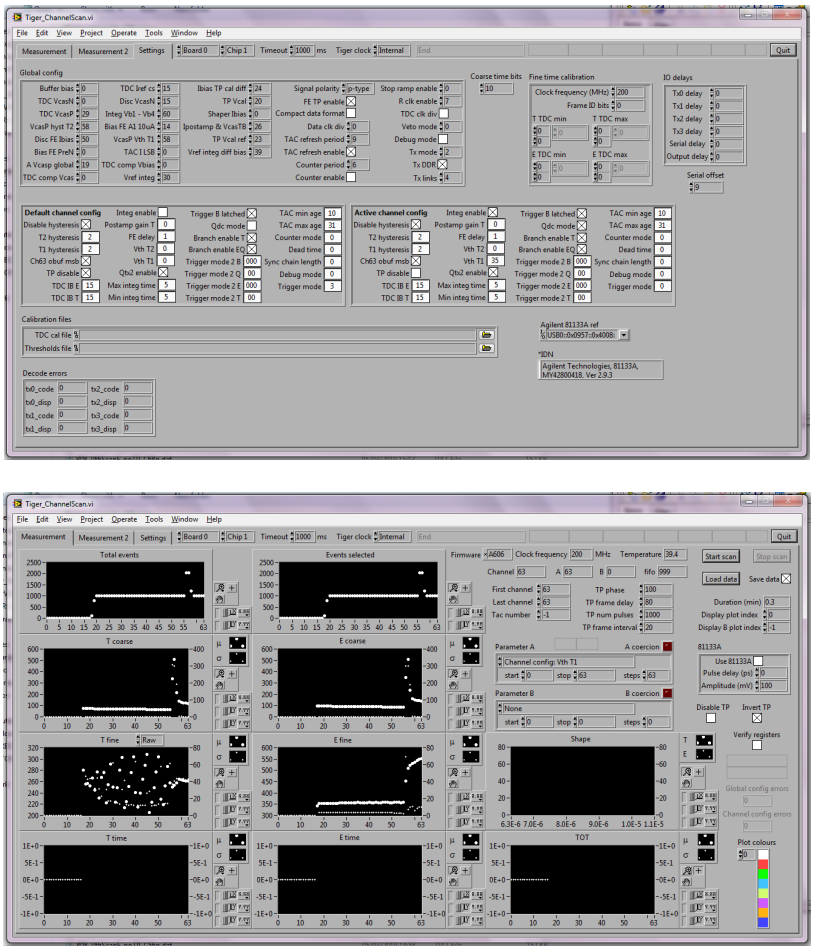


Figure 4.4: LabVIEW GUI. On the top the SETTING window that allows to set each parameter of the global and channel configuration registers. For the channel configuration it is possible to set different configurations for the active channel, i.e. the channel under test, and the other channels. The system allows to load threshold and TDC calibration files so that the acquisition is run with the selected channel-by-channel thresholds and the TDC output which is displayed online is already calibrated. On the bottom the MEASUREMENT window that allows to perform an acquisition on selected channels, scanning one or two parameters of the configuration registers. The results of the scan are displayed online during the acquisition allowing for a fast assessment of the ASIC response.

An Agilent 81133A Single Channel 3.35 GHz Pulse Pattern Generator [62] was used to inject a known charge at the input of channel 63 in order to calibrate the internal test pulse. Separated DC power supplies are used for the analog and the digital domains, using an Agilent E3631A 80W Triple Output Power Supply module [63].

4.1.3 Data analysis software

In order to perform more complex analysis and fully characterize the ASIC a dedicated software data analysis tool based on PyROOT [64] has been developed. This tool allows to read and process multiple files generated by the LabVIEW DAQ software and automatically generates the outputs (plots, histograms, tables, text) showing the measured performance in terms of gain, noise, jitter, linearity. Its functionality includes:

- **Noise measurement**: the threshold scans of the channel 62 obtained with different input capacitances are fitted with an s-curve from which the noise level is extracted and the plot noise *vs* C_{in} is created.
- **Threshold equalization**: the threshold scans of the 64 channels are fitted with an s-curve from which the effective baseline level is extracted. The thresholds are then equalized to a value set by the user and saved on a text file.
- **TDC quantization error and calibration**: the TDCs digitized outputs obtained from test-pulses with different delays are used to build a look-up-table containing the information about the time_bin and offset for each TAC of each TDC.
- **Jitter evaluation**: the measured timestamps from a repeated test-pulse (with fixed timing and amplitude) are collected in a histogram and the resulting Gaussian distribution is fitted providing the jitter measurement. The algorithm is automatically iterated for runs with different input capacitances and input signal amplitudes, thus yielding the jitter *vs* Q_{in} and jitter *vs* C_{in} curves.
- **Charge measurement calibration**: the charge digitized outputs (both S&H and ToT) obtained using the external pulse generator and the internal calibration circuit are compared and a conversion function is generated. This function is then applied to the 64 channels producing a look-up-table for the ADC code *vs* Q_{in} conversion. For the S&H measurement also its response linearity is evaluated.

4.2 Electrical characterization

4.2.1 Front-End response

Analogue probes

As a first measurement with TIGER, the output of channel 63 time branch shaper has been probed in order to assess the response of the analogue front-end. For this measurement, a test pulse has been injected at the input of channel 63 using the external pulse generator. The measured waveform is displayed in Figure 4.5.

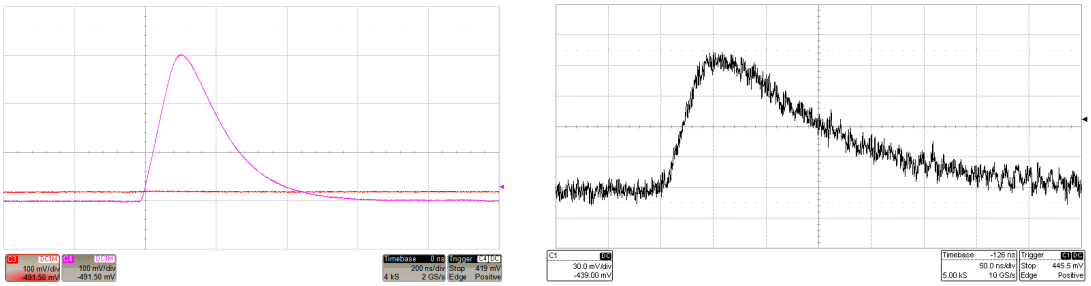


Figure 4.5: Preliminary measurements with TIGER probing its analogue debug output using a standard SMA cable (left) and an active probe (right). For details refer to the text.

The left figure shows the waveform generated from a 30 fC input signal and observed at the oscilloscope driving the signal through a standard SMA cable. The graph provides a first way to estimate the front-end characteristics in terms of gain and peaking time. A gain of ∼10 mV/fC and a peaking time of ∼ 100 ns are observed. These values do not perfectly match the ones from post-layout simulations (12.4 mV/fC gain, 60 ns peaking time). As mentioned before, this can be due to the limited drive strength of the output buffer used to transmit off-chip the front-end analogue output (refer to 3.3.4). Signal distortion and attenuation can be reduced by probing the signal with a very low capacitance circuit, such as an oscilloscope active probe. The figure on the right shows the resulting waveform from a 10 fC input signal observed using an active probe. Here the gain (∼12.3 mV/fC) and peaking time (∼60 ns) are compatible with the expected values.

Further measurements with different techniques, described in the following pages, will provide more accurate results about the front-end performance. Nevertheless, this very preliminary measurement proved the functionality of the analogue front-end part of the ASIC.

Front-end linearity and gain

The analogue debug IOs described before also provide a way to assess the front-end linearity. Test pulses of different amplitudes, scanning the full dynamic range, are fed at the channel 63 input and the output signal amplitude is measured at the scope. The results are displayed in Figure 4.6. The linearity is excellent up to 40-45 fC, whereas a large degradation is observed for signal above 50 fC. This is due to the front-end saturation and it is exactly as expected. The gain estimated from a linear fit of the measured points is about 12.4 mV/fC.

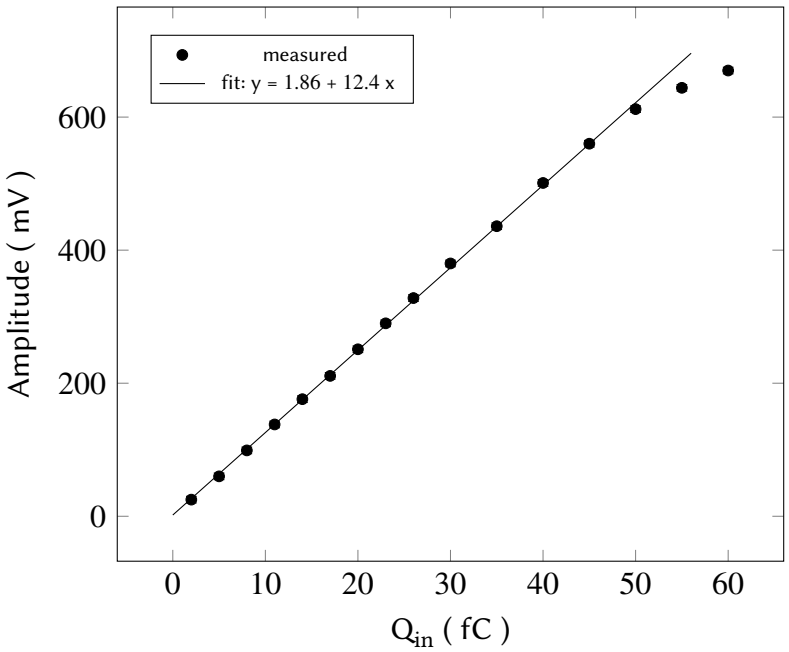


Figure 4.6: Gain measured on channel 63 probing the debug output.

S-curve measurements allow to improve the accuracy of this measure and assess also the other channels response. A threshold scan is performed by sweeping the discriminator threshold using its 6-bit DAC. For each step the DAQ system stores the number of registered event and the resulting plot is shown in Figure 4.7. The step size corresponds to the LSB of the DAC and its value is extracted from the second analogue debug output, which allows to probe the threshold of the channel 63 time branch discriminator.

The position of the signals baseline and peak are extracted by fitting the double S-curve, thus allowing to calculate the signal amplitude. The plot in Figure 4.8 is obtained by repeating this procedure for different input signals. The resulting average gain of 12.55 mV/fC matches very well the 12.4 mV/fC expected from post-layout simulations.

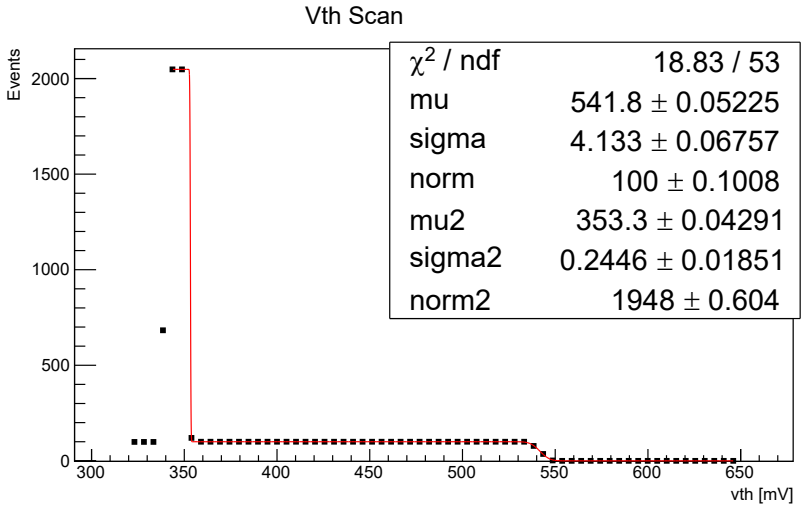


Figure 4.7: Double S-curve used to evaluate the signal amplitude: the peak around 350 mV is the position of the baseline, while the one at 550 mV is the signal peak.

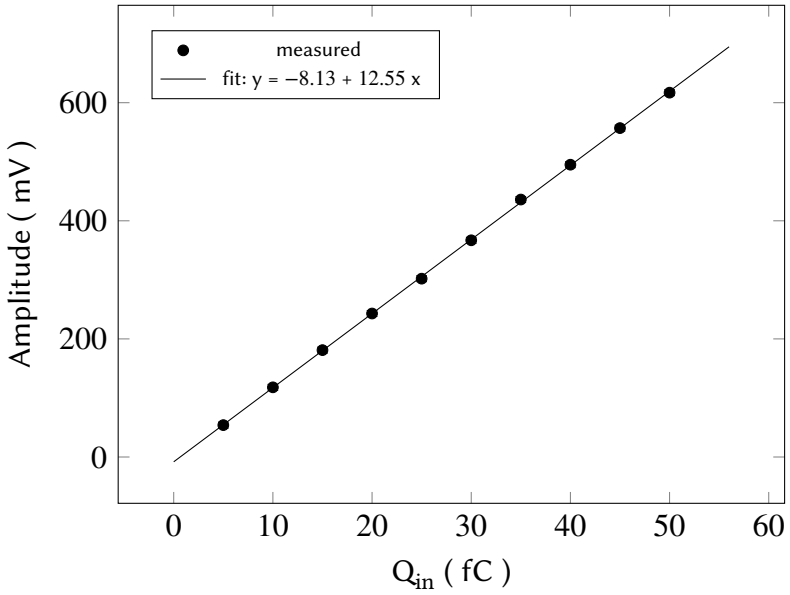


Figure 4.8: Signal amplitude measured with the double S-curve method for different input charge values.

The external pulse generator has been used to inject a well known input charge and calibrate the internal injection circuit that allowed to extend this measurement to all 64 channels. The gain distribution is shown in Figures 4.9 and 4.10. An average gain of 12.26 mV/fC with a 2% r.m.s. dispersion is found.

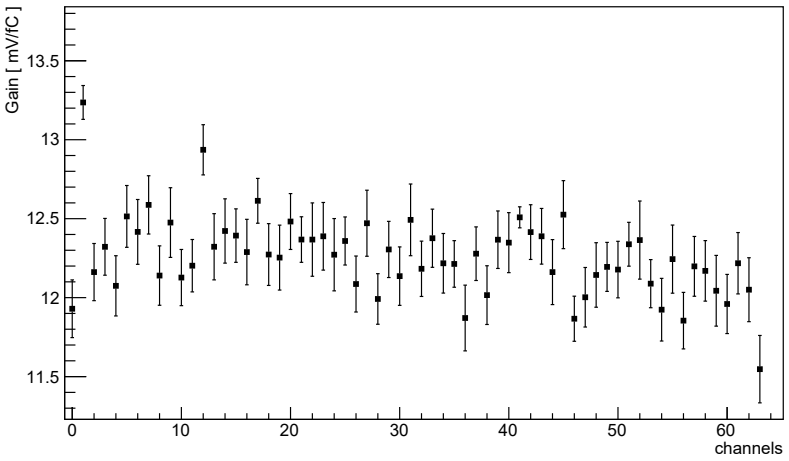


Figure 4.9: Time branch 64-channel gain distribution.

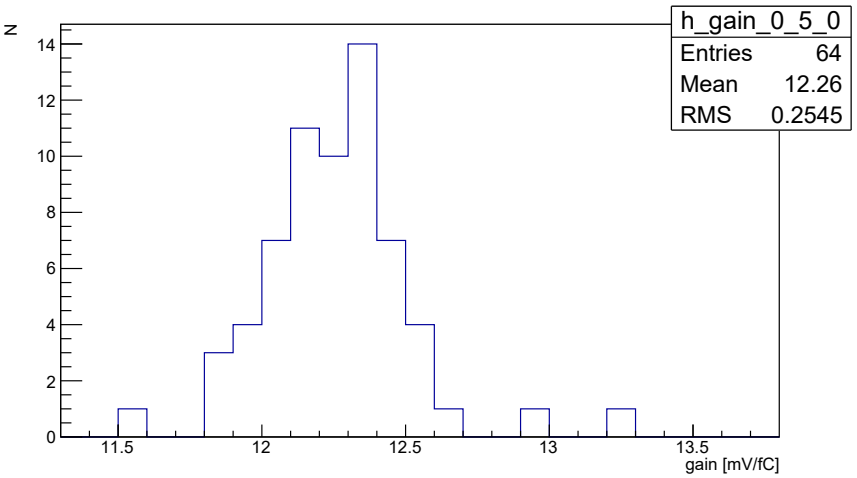


Figure 4.10: Time branch gain dispersion of the 64 channels of one ASIC.

The S-curve technique is employed in the same way to characterize also the response of the energy branch analogue front-end, which is not provided with a direct output debug port and whose performance are summarized in Figures 4.11, 4.12 and 4.13. An average gain of 11.56 mV/fC with a 2.3% r.m.s. dispersion results. This value is in good agreement with 11.92 mV/fC gain expected from post-layout simulations.

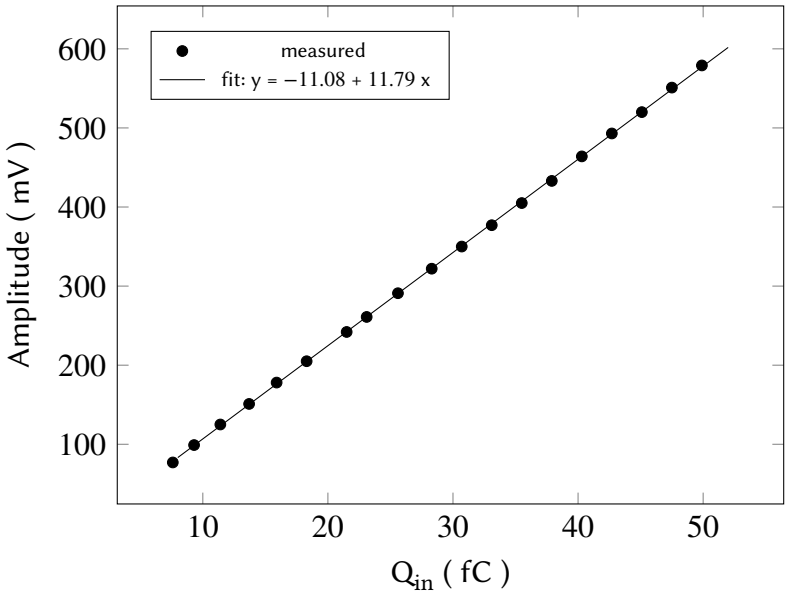


Figure 4.11: Energy branch linearity and gain measurement for one channel using the S-curve method.

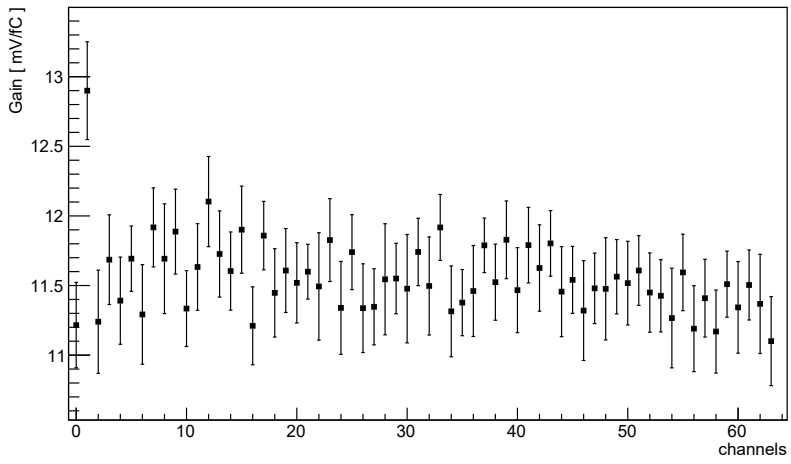


Figure 4.12: Energy branch 64-channel gain distribution.

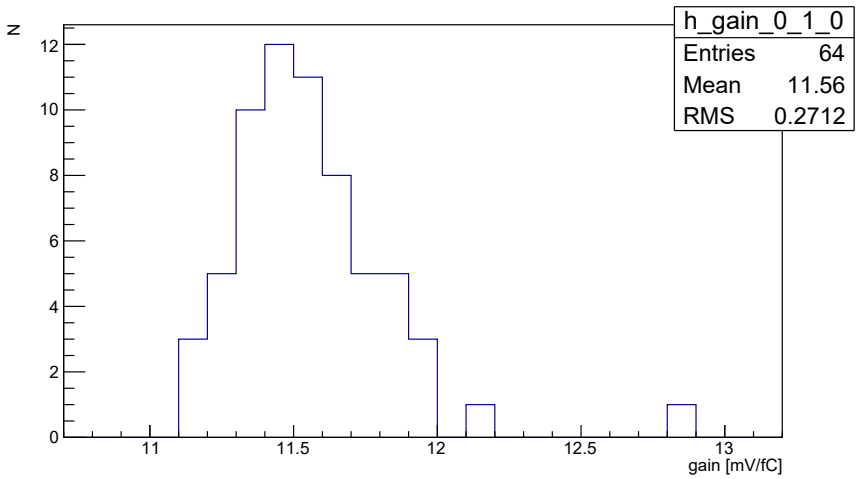


Figure 4.13: Energy branch gain dispersion of the 64 channels of one ASIC.

Noise performance

S-curve measurements provide also a way to evaluate the noise of the analogue front-end. A test pulse of fixed amplitude is sent at the channels input and a threshold scan is performed. The resulting S-curve is fitted with the Gaussian error function:

$$\mathrm{erf}(z) = \frac{2}{\sqrt{\pi}} \int_0^z e^{-t^2} dt \tag{4.1}$$

where $t = (x - \mu)/\sigma$ and σ provides a measurement of the noise level. For each input capacitance, the procedure is iterated many times in order to extract also an estimation of the error for this measurement.

The noise measured at the output of the time branch shaper for different input capacitances is shown in Figure 4.14. The noise is slightly higher compared to post-layout simulations (15% for C_{in} = 100 pF), at low input capacitance values a plateau is observed. The time branch noise performance mainly affect the time resolution of the system which will be analyzed in a dedicated section.

The energy branch input-referred noise, expressed in Equivalent Noise Charge (ENC), measured for different input capacitances is displayed in Figure 4.15. The results are similar to the one obtained from the time branch (20% noise increase at C_{in} = 100 pF, plateau at low input capacitances). The plateau seems to indicate that the measurement is affected by common-mode noise. Different test setup grounding and shielding have been

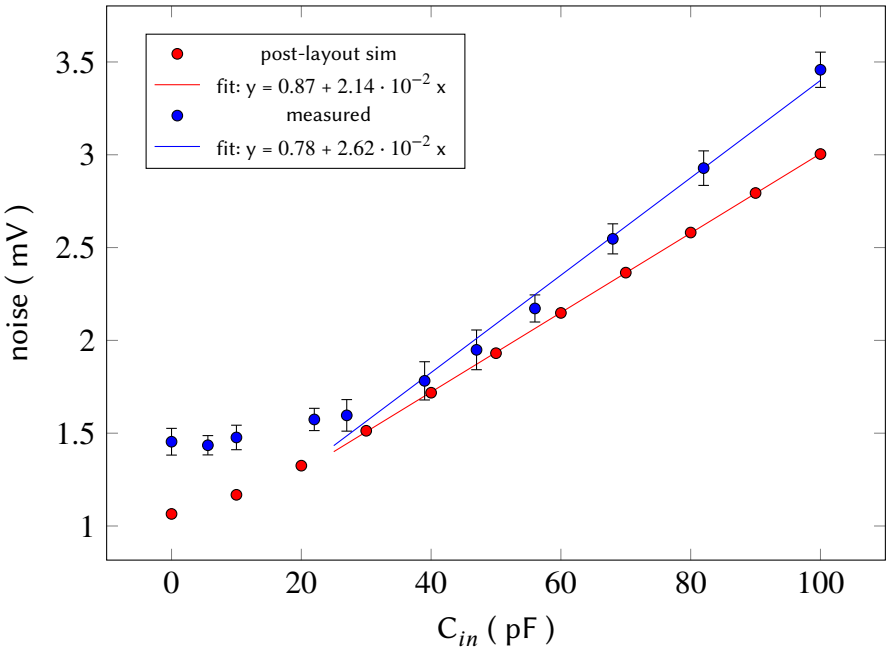


Figure 4.14: Time branch r.m.s. output noise as a function of the input capacitance.

investigated in order identify the root cause of this behavior, as well as studies on the power-supply rejection ratio (PSRR) of the front-end blocks. At the time of this writing the origin of this behavior is still not well understood, however the overall performance is already adequate for the final application.

The noise of the energy branch can also be evaluated exploiting the S&H circuit connected at the output of the shaper. In this test, repeated test pulses of fixed amplitude are sent to the front-end and the digitized output (Efine) provides a measurement of the signal peak amplitude.

Figure 4.16 shows the distribution of the digitized values for an input signal of 10 fC and an input capacitance of 100 pF. The distribution is fitted with a Gaussian function and the resulting noise of 0.29 fC (1812 electrons) is in good agreement with the value measured using the S-curve method shown before. The small increase could be due to the S&H circuit not capturing exactly the signal peak, i.e. the optimum point in terms of ENC optimization. However, this does not compromise the measurement provided by the S&H and the performance are still adequate for this application.

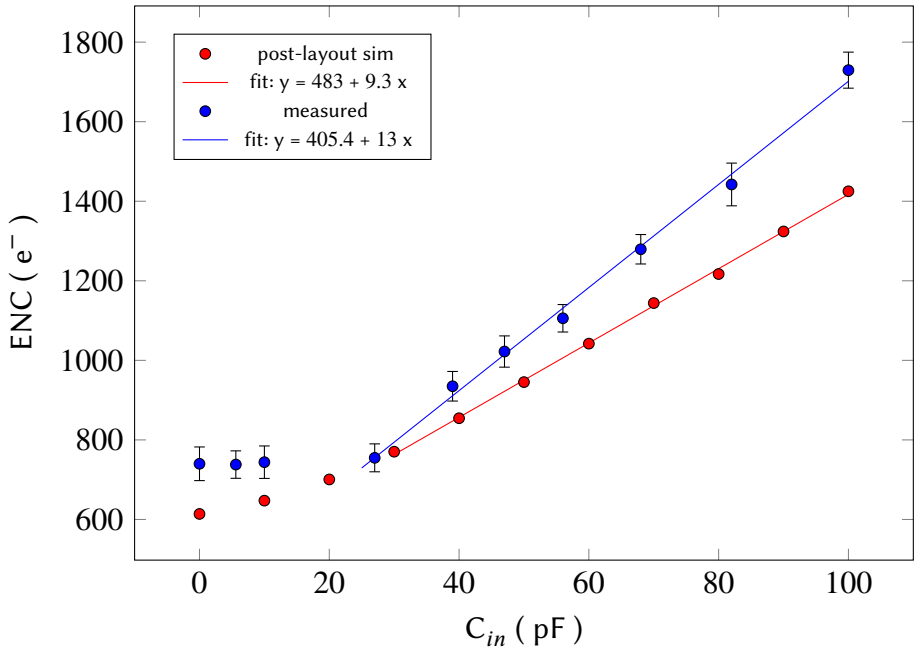


Figure 4.15: Energy branch ENC as a function of the input capacitance.

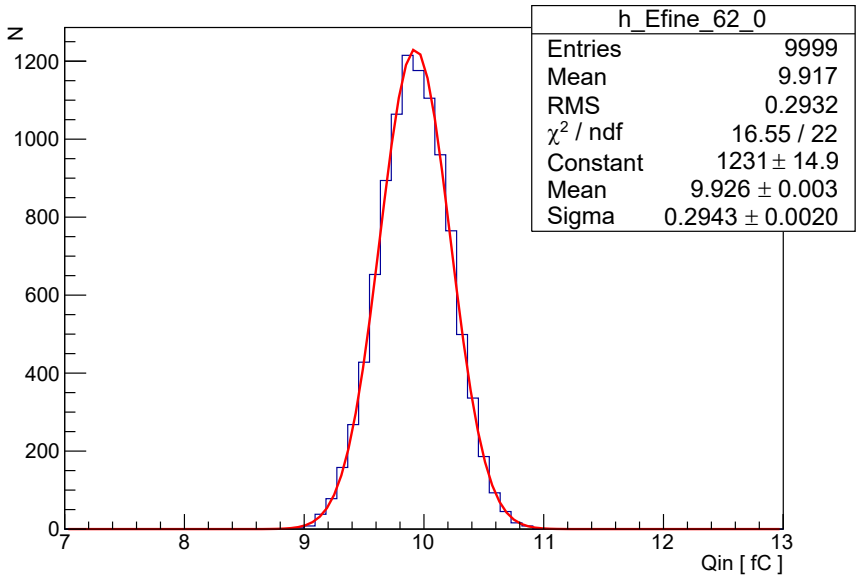


Figure 4.16: Noise measured with the S&H circuit using a repetition of test pulse of fixed charge (10 fC).

Thresholds equalization

Threshold scans offer a way to study and correct channel-to-channel baseline and threshold offsets. In principle a common threshold voltage is applied to all channels, therefore, in order to compensate potential channel-to-channel offsets, the threshold of each discriminator can be fine tuned with a 6-bit DAC.

The thresholds equalization is performed in two steps. First, the threshold non-uniformity is measured by performing a threshold scan for each of the 64 channels (Figure 4.17, left). Fitting the obtained S-curve provides the effective position of the baseline and allows to adjust the DAC of each channel to a value such that the effective thresholds of the 64 channels are set equally above the baseline (Figure 4.17, right).

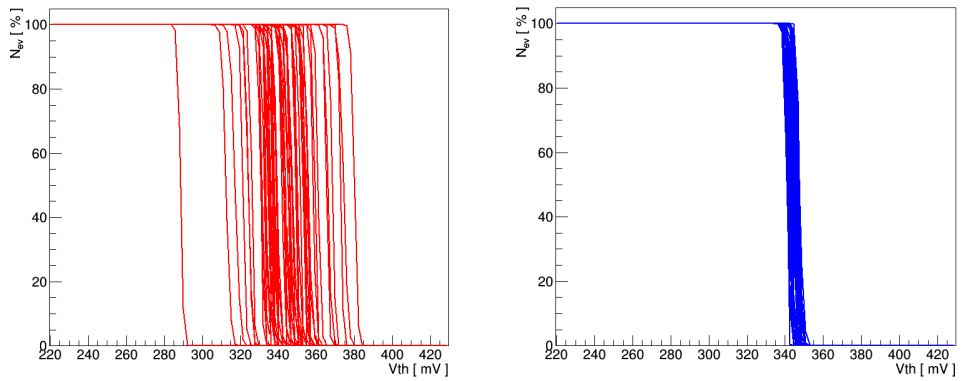


Figure 4.17: Baseline level of the 64 channels before (left) and after (right) thresholds equalization.

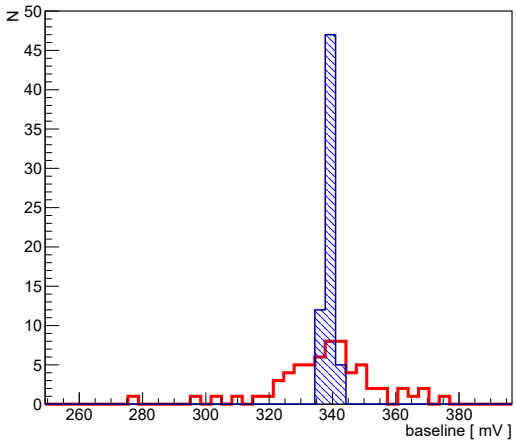


Figure 4.18: Threshold non-uniformity of the 64 channels in one chip before (red) and after (blue) the equalization.

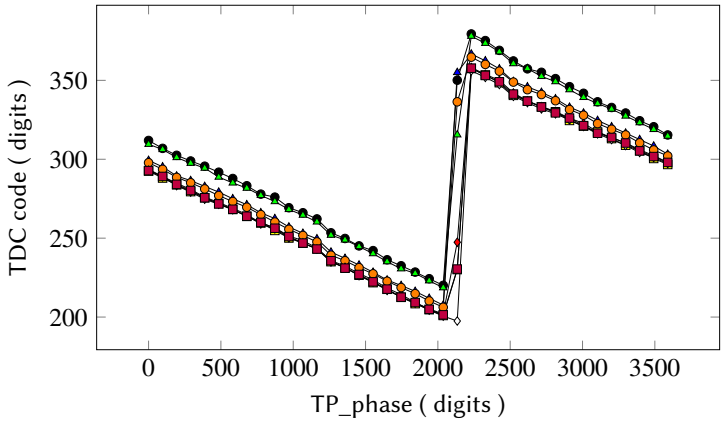
Figure 4.18 shows the 64 thresholds of one chip before and after the equalization. The original thresholds standard deviation was 16.7 mV, with a maximum difference of 99 mV. After adjusting the threshold of each channel, the standard deviation and maximum difference are reduced to 1.5 mV and 6 mV respectively.

4.2.2 Timing performance

In order to efficiently time-tag each hit, thus enabling the μTPC reconstruction algorithm, TIGER must meet the requirement of 5 ns time resolution. In principle, the timing performance of TIGER is affected by the front-end noise, the TDC quantization error and the discriminator time walk. In the following, these three contributions are analyzed.

TDC calibration and resolution

The TDC performance has been evaluated by feeding a digital TP at the input of the TDCs, using the dedicated TRIGGER_MODE = 1 operation, and scanning its phase along one clock cycle (Figure 4.19, left). These measurements allow to create an offline look-up table (LUT), in which the stored values are used for the offset and gain correction for the four TACs of the two TDC of each channel (Figure 4.19, right).



CH	TAC	MIN	MAX
0	T0	220.1	379.4
	E0	202.0	358.1
	T1	207.6	366.7
	E1	201.0	357.5
	T2	206.2	364.7
	E2	197.5	356.1
	T3	218.6	378.0
	E3	201.4	357.7

Figure 4.19: TDC response (1 channel, 8 TACs) to a test pulse phase scan (left) and look-up-table for offset and gain compensation (right).

The time bin is evaluated using the formula:

$$\text{time\_bin} = \frac{\tau}{\text{MAX} - \text{MIN}} \tag{4.2}$$

where τ = 6.25 ns is the clock period and MAX and MIN are respectively the maximum and minimum values measured by the TDC, both reported in the LUT and expressed in ADC codes. As an instance, the scan in Figure 4.19 (left) produces a TDC time bin of $\sim$ 40 ps.

The plots of Figure 4.20 show the TDC time resolution for the time and energy branch of the 64 channels after the calibration. The quantization error is less than 50 ps r.m.s., with good uniformity across the chip. This value is much lower than the required time resolution, therefore the timing performance of the channel will be only affected by the response of the analogue front-end. This test also proves the correct behavior of the back-end electronics.

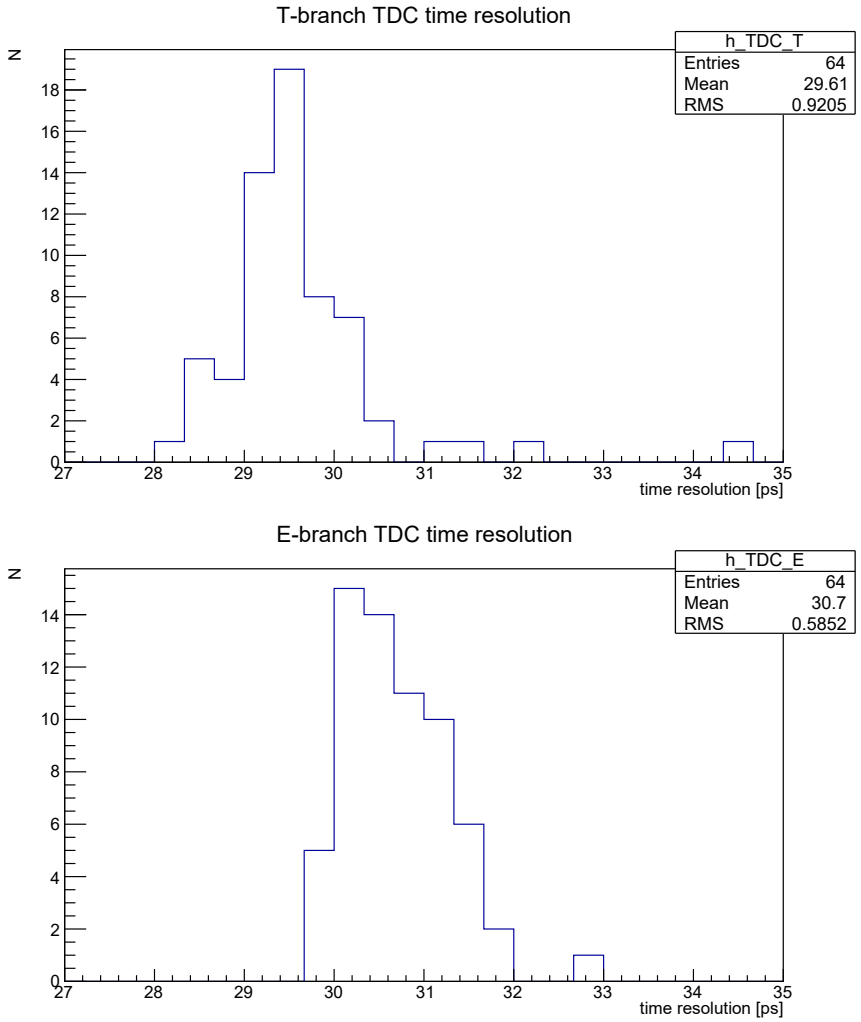


Figure 4.20: Time resolution of the TDC of the time (top) and energy (bottom) branch.

Time walk

The leading edge discriminators of TIGER are intrinsically affected by time walk, which can be corrected exploiting the charge information also provided by the chip. Figure 4.21 shows the time-offset measured for different threshold settings as a function of the input charge. For this measurement, the signals are produced at the same time but with variable amplitudes using the internal test pulse generator. The time walk *vs* amplitude relationship is non-linear; the longest time walk corresponds to small signals that barely cross the threshold and then reduces (with $\sim 1/Q_{in}$) as the signal amplitude increases. Even with a threshold of 1 fC the maximum offset is about 10-12 ns, hence time walk corrections are necessary to achieve the required time resolution for very small signals. The offset increases with the threshold making this correction even more mandatory.

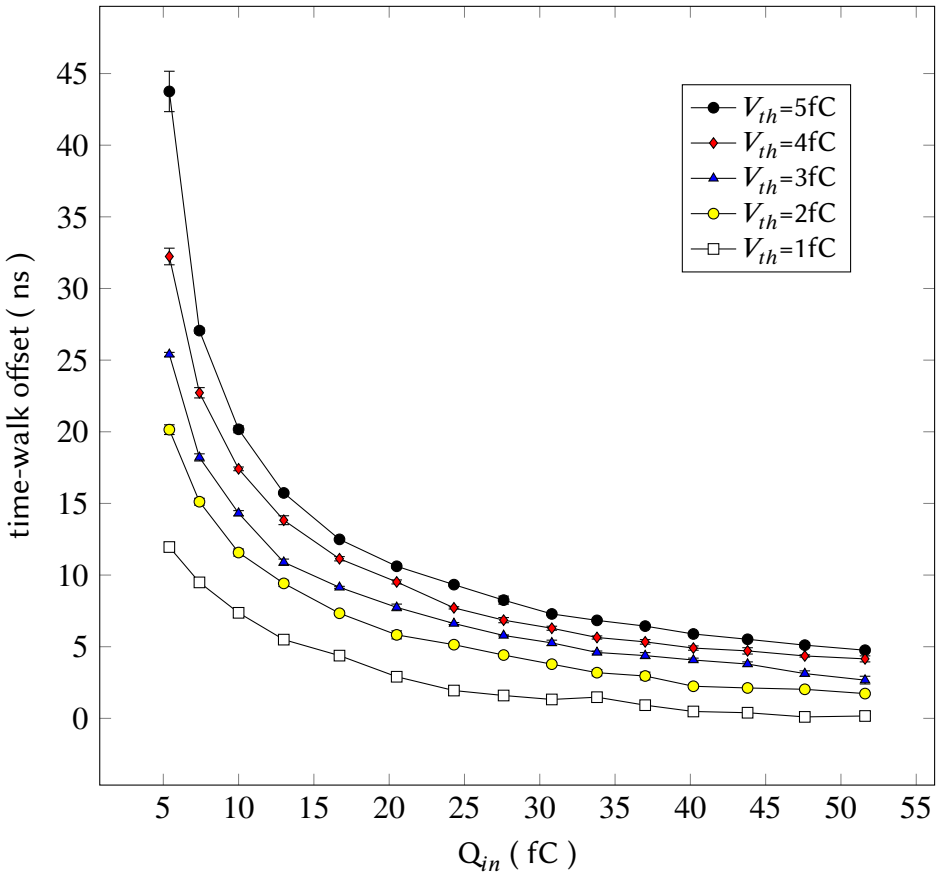


Figure 4.21: Time walk curve as a function of input charge for different threshold settings.

Jitter

The jitter of the time branch has been measured by sending at the pre-amplifier input repeated test pulses of fixed charge (from 2 fC to 50 fC) using the internal calibration circuitry. The resulting Gaussian distribution of the measured timestamps is fitted and the jitter r.m.s. corresponds to the sigma of the Gaussian function. As an instance, the measured time jitter for the worst-case scenario (C_{in} = 100 pF, Q_{in} = 2 fC) is displayed in Figure 4.22.

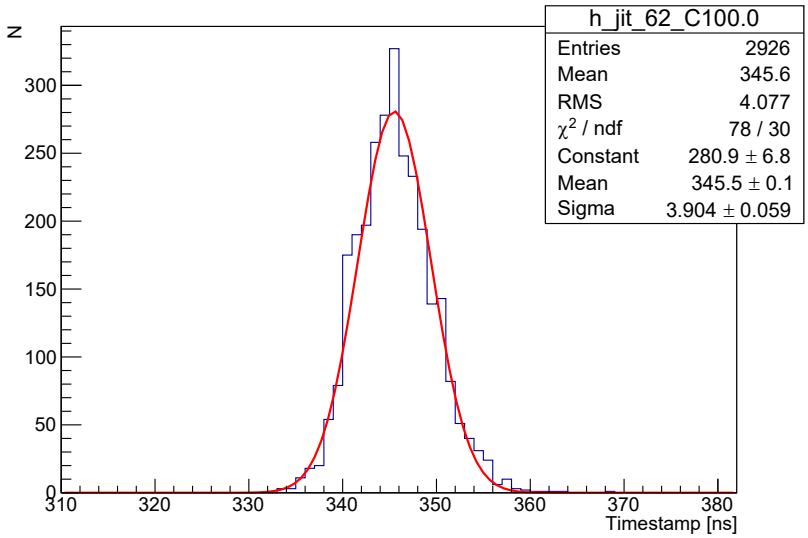


Figure 4.22: Time branch jitter for C_{in} = 100 pF and Q_{in} = 2 fC.

The procedure is iterated for different input capacitances and test pulse amplitudes. The jitter as a function of the input charge measured for different capacitances is shown in Figure 4.23. The jitter is kept below 5 ns r.m.s., thus enabling the use of the μTPC reconstruction algorithm.

4.2.3 Charge measurement

The charge information can be retrieved from two different measurements: in *S&H mode*, the digitized peak voltage of the energy branch shaper output is extracted using the S&H circuit - Wilkinson ADC chain, while in *ToT mode* the input charge is inferred from the measured pulse duration by enabling the TDCs of both branches. In the following section the results of both methods are depicted, showing their advantages and limitations.

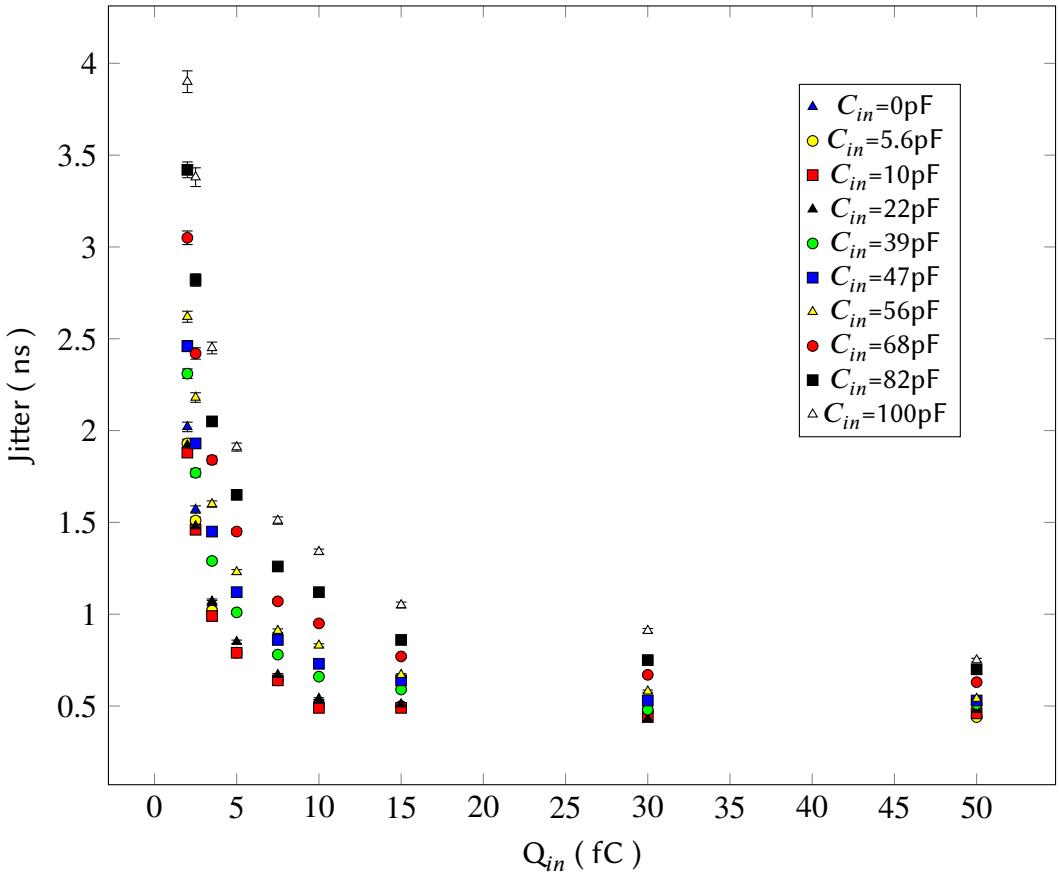


Figure 4.23: Time jitter as a function of input charge for different input capacitances.

S/H linearity and dynamic range

In order to study the linearity and dynamic range of the charge measurement, the external test pulse generator was used to injects signals of different well known amplitudes, providing a scan of the full dynamic range of interest with enough granularity. Figure 4.24 shows the charge measurement performed with the S&H circuit displaying the code of the Wilkinson ADC (Efine) that digitizes the S&H output as a function of the input charge. In this plot the negative slope of the line is due to the ADC reverse logic.

The linearity of the circuit can be studied by evaluating the residual non-linearity defined as:

$$NL = \frac{A_{fit} - A_{meas}}{A_{fit}} \tag{4.3}$$

where A_{fit} and A_{meas} are respectively the value extracted from the linear fit and the

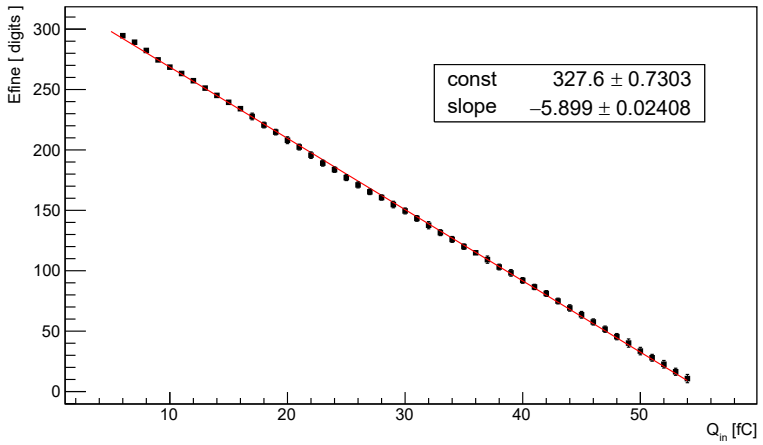


Figure 4.24: S&H charge measurement using the external pulse generator.

measured value, both expressed in ADC codes. The results are shown in Figure 4.25.

The good linearity of the circuit (less than 1% for the whole the dynamic range) proves that the discriminator time walk does not affect significantly the S&H circuit measurement.

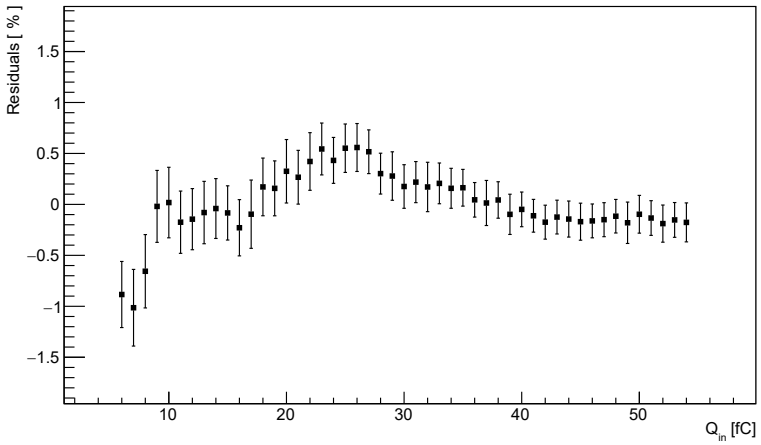


Figure 4.25: Residual non-linearity of the S&H charge measurement.

The measurement has been repeated using the internal pulse generator, thus assessing the response of all the 64 channels. The results are shown in Figure 4.26 and are similar to the ones obtained with the external pulser, proving that the on-chip test pulse generator provides a faster but still reliable way to test all the channels in the ASIC.

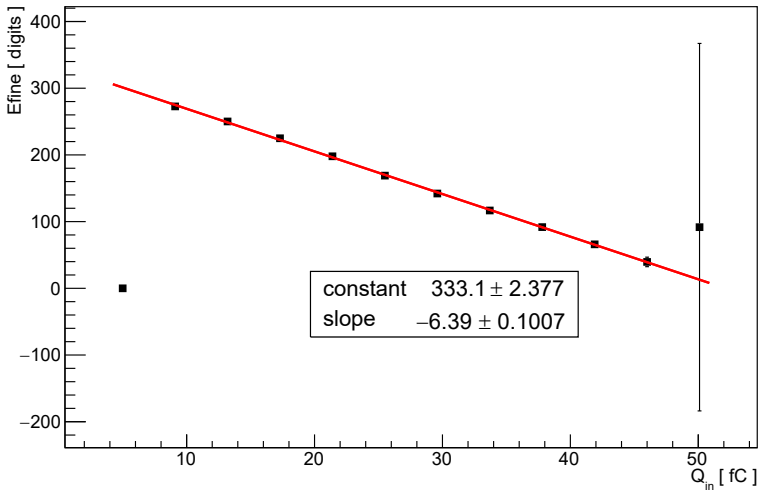


Figure 4.26: S&H charge measurement using the internal calibration circuit.

It can be observed that the internal pulse generator cannot be operated properly at both edges of the dynamic range (below 5 fC and above 45 fC) at the same time, because some transistors in the calibration circuit go outside their intended operating region, but some fine tuning of the configuration registers related to the test-pulse generation still allows to assess the whole dynamic range in dedicated runs.

The maximum signal measured by the S&H circuit is defined by the Wilkinson ADC reference voltage. If the sampled signal is higher than this voltage the conversion cannot work properly anymore and the output ADC code is a fixed number. The event is still transmitted but the charge information only indicates that the saturation point was reached. This poses the need to study the maximum input charge that can be correctly digitized and the potential impact of the presence of hits with no precise charge information on the reconstruction algorithms. This issue will be discussed in the section dedicated to the tests with the sensor itself since the effective input dynamic range is strictly related to the detector gain settings.

Time-over-Threshold

The plot in Figure 4.27 shows a typical charge measurement curve using the Time-over-Threshold (ToT) technique. The intrinsic non-linearity of the pulse duration of CR-RC^n-like shapers causes the non-linear behavior of this measurement. A precise ToT *vs* Q_{in} conversion, may need many calibration points due to its non-linearity and

the procedure can become cumbersome and time consuming when extended to hundreds of chips.

Owing the excellent performance of the S&H, it is not planned to use the *ToT mode* in the experiment. Nevertheless, the ToT mode offers a back-up solution and allows to extend the input dynamic range beyond the saturation point of the S&H mode.

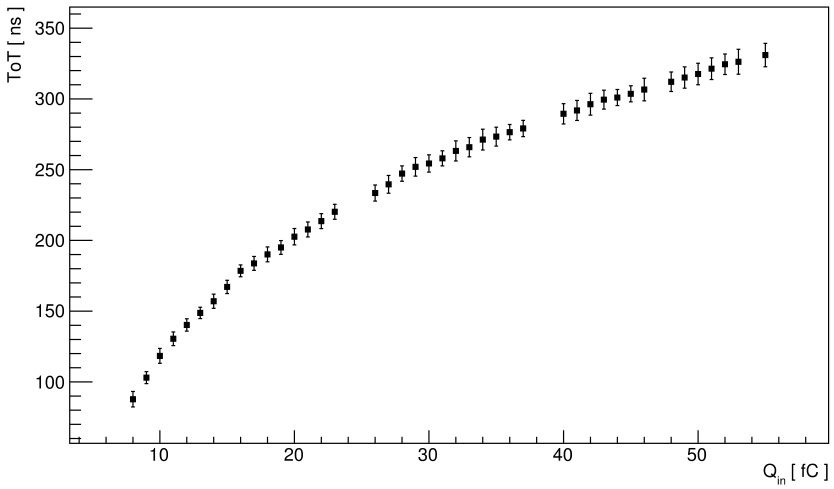


Figure 4.27: Time-over-Threshold as a function of the input charge.

4.2.4 Front-End-Boards validation

During the electrical characterization some Front-End-Boards (FEBs) were produced and tested in order to validate the PCB design and assess the ASIC response when mounted on these boards.

Each bias voltage provided off-chip was deeply investigated in order to find its optimal value. The baseline and Wilkinson ADC references voltages (V_{BL} and V_{ref}) define the dynamic range of the charge measurement using the S&H circuit. Lowering V_{BL} or raising V_{ref} allows to increase the dynamic range but at the cost of degrading the performance of some blocks of the readout chain. On one hand, a too low baseline may put the discriminator transistors out of saturation, making its response slower and less efficient. On the other hand, with a too high V_{ref} the current source used to recharge the ADC capacitor will work out of saturation and thus the current will not be a constant anymore.

Considering these constraints and the required input dynamic range the two parameters were set to V_{BL} = 350 mV and V_{ref} = 910 mV.

4.3 On-detector electronics assembly

After the successful electrical characterization of TIGERv1, the assembly of the required number of final Front-End-Boards started. Two ASICs were bonded on each FEB and they have been validated with a two-step procedure: first a TDC scan to assess the functioning of the ASIC back-end and then a threshold scan, with the test-pulse enabled, to test the front-end response. This procedure has been repeated before and after the heat-sink installation, thus testing the chips at different operating temperatures.

The FEBs passing the validation phase have been sent for calibration, the others have been investigated and the root causes of their malfunctioning identified. Issues in both the ASICs and the FEBs have been discovered. Due to a faulty FEB production batch, the FEBs for the detector Layer 2 and 3 presented several problems and non-compliance, such as wrong voltage divider values for the generation of the ASIC external bias, short-circuits on adjacent pins of the FEB connector, broken voltage regulators [65], [66]. Some of these faulty FEBs could be restored by the Turin INFN Electronics Laboratory, the others were discarded. The Layer 1 FEBs, which were produced by another firm, presented no issues and their validation was less cumbersome. For what concern the issues related to the ASIC itself, some of the chips presenting dead or noisy channels were recovered by changing the external bias voltages or internal configuration registers, the others were replaced with a new chip.

4.3.1 Charge and Time measurement calibration

Semiconductor manufacturing is intrinsically affected by process variations. Fluctuations during the fabrication phase, including equipment, material and processing, may cause deviation of the electrical properties of a semiconductor device, thus modifying the behavior of the circuit. For this reason, the development of complex mixed-signal ASICs can provide significant offsets in the response of different channels of the same chip, different chips of the same production batch or different production batches. Some techniques allow to reduce these effects but, as devices become smaller, they cannot be completely avoided.

A common approach is to calibrate the electronics response, i.e. to provide a tool which allows to link the ASIC digital output to some known physical quantities. For experiments with a high number of electronics channels the calibration procedure must be fast, reliable and repeatable.

For the CGEM-IT 160 TIGER chips ($\sim$ 10000 channels) are needed to fully instrument

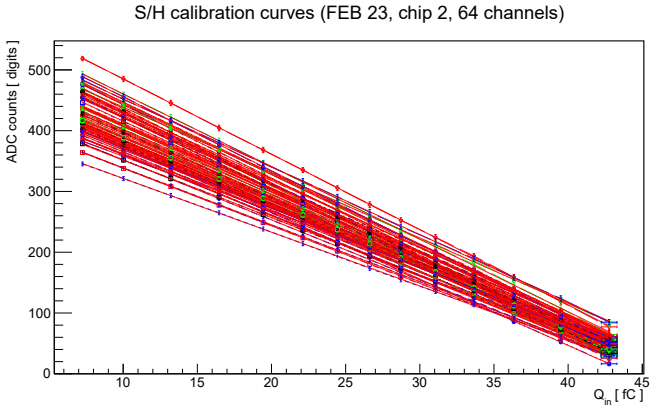
the detector. Taking into account also some spare chips, more than 12000 channels have to be calibrated for their charge and time response.

The TDC calibration has been already discussed in the previous sections. The FPGA allows to send at the TDCs input test-pulses with programmable delay with respect to the clock signal. The TDCs response is stored in look-up-tables containing the information for the gain and offset correction for each of the 512 TACs present in one chip.

The charge measurement calibration procedure is more complex since it requires to calibrate the internal analogue test pulse in order to generate input signals of well known amplitude scanning the full dynamic range of the 64 channels. The calibration procedure consists of the following steps:

1. Thresholds equalization by performing a threshold scan on the 64 channels
2. Internal TP calibration using a LabVIEW-controlled external pulse generator on one channel
3. Application of the same test-pulse configuration to the 64 channels
4. PyROOT script to generate LUTs (FEB_id, chip_id, channel_id, ADC code *vs* Q_{in})

Figure 4.28 shows the results of the charge measurement using the S&H circuit for the 64 channels in one ASIC. One can observe that, for a precise charge measurement, the channel-by-channel offsets must be taken into account, hence a calibration curve for each channel is needed.



CH	CONST	SLOPE
0	514.24	-10.74
1	483.28	-10.92
2	460.34	-9.99
3	506.53	-11.02
4	487.33	-10.32
5	450.71	-9.87
6	609.13	-12.40
7	563.24	-12.06
8	446.02	-9.45
9	496.37	-10.57

Figure 4.28: S&H charge measurement for the 64 channels in one ASIC (left) and the related LUT for the first 10 channels.

Each channel response is fitted with a linear function which can be expressed as:

$$\text{ADC\_code} = \text{const} + \text{slope} \cdot Q_{\text{in}} \tag{4.4}$$

The input charge can be thus retrieved using the formula:

$$Q_{\text{in}} = \frac{\text{ADC\_code} - \text{const}}{\text{slope}} \tag{4.5}$$

The calibration has been carried out with the final cooling system, thus operating the chips at the expected experiment temperature. Nevertheless, the internal test-pulse allows to periodically run again the charge measurement calibration procedure, if any big variation is observed.

From the first production batch a total of 166 TIGER chips have been validated and calibrated. 15 dead channels on a total of 10624 channels (0.14%) have been found [65]. Before the final installation some other FEBs will be prepared in order to replace the ones with dead channels and as a back-up solution in case some replacement is needed.

4.4 Testing of GEM detectors with TIGER

In this section the results obtained with TIGER connected to different GEM detectors are discussed. As a first step, some tests have been carried out using planar GEMs since they are easier to move and operate and require a smaller number of electronics channels to be readout. In this context, two beam tests allowed to prove the functionality of the system and validate the GEM readout using TIGER.

After that, the tests have been aimed towards the integration of the full-chain readout system (CGEM, on-detector and off-detector electronics). Some preliminary results are presented at the end of this section.

4.4.1 Test beam with planar GEMs

Two beam tests using TIGER and 10×10 cm^2 planar GEM chambers have been performed at two test beam facilities:

1. MAMI - MAinz MIcrotron [67] facility in Mainz with electron beam up to 855 MeV/c momentum (November 2017)

2. CERN - H4 beam line [68] with muon and pion beams up to 150 GeV/c momentum (April 2018)

Experimental setup

The CERN facility, shown in Figure 4.29 allows to test the system inside a magnetic field generated by Goliath [69], a large dipole magnet providing a magnetic field up to 1.5 T in both polarities which allows to recreate an environment similar to BESIII.

The setup is depicted in Figure 4.30. The planar chambers, featuring an XY readout with orthogonal strips, are placed inside Goliath and the beam direction is orthogonal to them. Two scintillator bars readout by photo-multiplier tubes are placed outside the magnet and provide a trigger signal for the acquisition. Some measurements have been performed rotating the planar GEMs around the vertical axis in order to characterize the chambers with inclined tracks.

Figure 4.29: CERN H4 beam line.

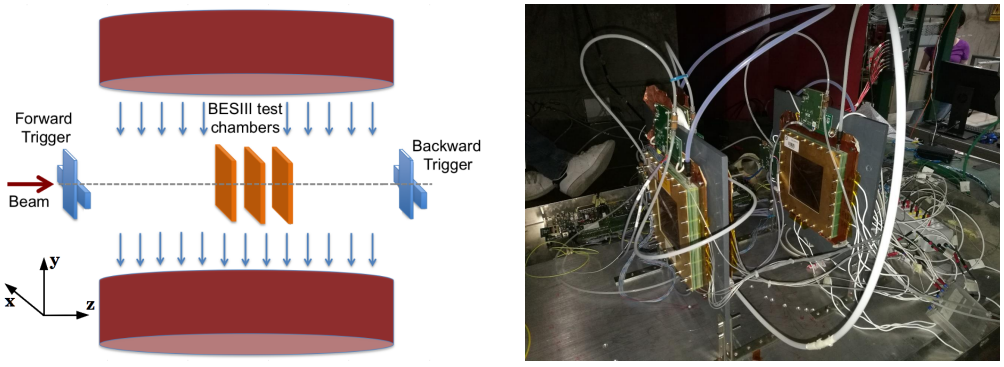


Figure 4.30: CERN test beam setup. In the picture on the right the two planar GEMs mounted on the left stand are readout with the FPGAs DAQ, while the one on the right stand is readout by the GEMROC module.

A similar setup has been used in the MAMI facility, where the magnet is not present. At the time of MAMI test beam only the prototype version of TIGER (TIGERv0) was available. As discussed before, this version suffered from a baseline instability due to the malfunctioning of the Baseline Holder circuit. Since the cooling system was still not available, temperature variations during the acquisition induced drifts in the baseline which prevented us from setting the thresholds properly close to the baseline. As a consequence, the operation at high thresholds (between 5 and 10 fC) did not allow for the optimization of the ASIC acquisition parameters.

Nevertheless, this test beam provided useful information about the integration of TIGER with a GEM detector, different grounding conditions were studied in order to find the best configuration in terms of noise. The DAQ system developed for this test beam was found fully functional and was re-used for the CERN test beam with only small improvements.

On the contrary, at the CERN test beam the final version of TIGER (TIGERv1) was available as well as a small cooling system that allowed to keep the FEBs temperature stable. Given the better operating conditions, the discussion will focus on the results obtained from the CERN test beam.

The DAQ system was already successfully employed in Mainz and is an upgrade of the test bench setup used during the ASIC electrical characterization. Each planar GEM is readout by two FEBs, one for the X-strips and one for the Y-strips. Two Xilinx Virtex 6 FPGAs allowed to handle 4 FEBs and thus two planar GEMs. The two FPGAs were synchronized by a third FPGA (Xilinx Spartan-6 FPGA SP605 Eval Kit, [70]), acting as a master, that distributed the clock and reset signals to the two slaves through a couple of Silicon Labs SI53301/4-EVB distribution boards [71].

The FEBs were connected to the planar GEMs using a transition board. The FEBs connector has been designed to be coupled directly to the CGEM anode, hence its pinout (refer to Appendix C) did not perfectly match the one of the planar GEMs transition board. As a consequence, some channels of the chips were disconnected or, even worse, they were connected to some protection circuit passive components. In order to avoid the collection of noise-induced data from these channels, they were disabled by setting their TRIGGER_MODE to 3.

In order to store the trigger time information, the signal provided by the scintillators was injected on one of the disconnected channels of each TIGER and was sent directly to the TDC by setting its TRIGGER_MODE to 1. In this way, the default TIGER trigger-less readout mode was turned into an offline trigger-matched operation using one channel

to measure the trigger time of arrival. With this approach, still all data were saved to disk, but during the offline analysis only the data corresponding to a trigger signal could be selected.

In addition, a third GEM chamber was readout by other two FEBs controlled by a GEMROC board, i.e. the readout module for the final application. At the time of this test beam the data acquisition using the GEMROC module was in its prototype phase and some of its functionalities still needed some debugging. In this context, the test beam allowed to perform some tests, e.g. data loss at high rates or trigger matching efficiency, and the results were used to improve the GEMROC firmware.

All the FEBs were already powered by the GEMROC modules, thus allowing to remotely power-on and power-off the chips and check their status in terms of power consumption and temperature.

Data with different GEM rotational angles and high voltage settings have been collected in order to study the performance for perpendicular and angled tracks with different gain configurations. From the ASIC point of view, the charge measurement was performed both in *S&H mode*, i.e. the intended mode for the final application, and *ToT mode*, as a backup solution in case the results from the S&H measurement were affected too much by saturation.

Data reconstruction and results

The data acquired with the FPGAs DAQ system have been analyzed in order to validate the GEM readout using TIGER chips and evaluate the performance of the system.

A specific software, named GRAAL (Gem Reconstruction And Analysis Library), has been developed for the reconstruction and analysis of data coming from GEM detectors [8]. The software exploits the trigger time information to build the events. In this case, the hits inside a (-300, +400) ns time window with respect to the trigger signal have been selected to form an event.

A cluster of strips is defined by contiguous hits in the same event. The clusterization algorithm can handle dead strips, building the cluster even if there is an empty strip between the good ones. The charge of the cluster is obtained by summing the charges of the hits inside the cluster. The charge and time information of each hit allow to reconstruct the overall hit position using the charge centroid and μTPC algorithms described in 1.2.2.

As a first step, the saturation percentage of the charge measurement provided by

the S&H circuit has been studied. The results for different HV settings and incident angles are shown in Figure 4.31. The left plot presents the CERN test beam conditions. The saturation ratio is kept very low even at very high gains and is considered fully acceptable for an efficient charge centroid reconstruction.

As a comparison, the situation during the Mainz test beam is reported in the plot on the right. Here the saturation ratio was too high to efficiently employ the S&H charge measurement mode. These two plots show the improvement provided by the new TIGER version (TIGERv1), where the baseline instability issues observed in TIGERv0 were completely solved.

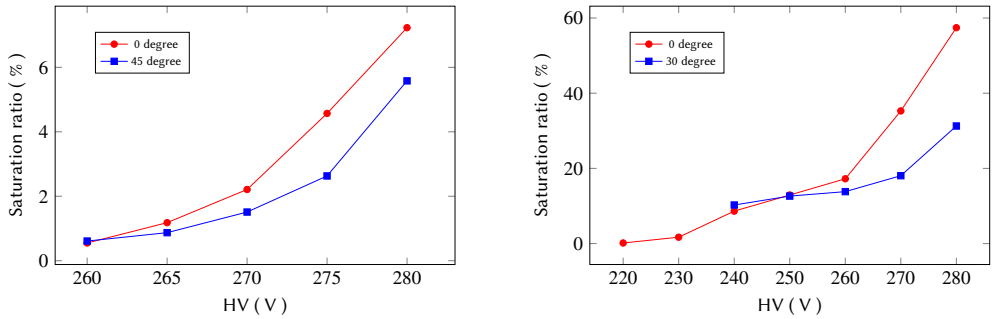


Figure 4.31: Charge measurement saturation ratio from CERN test beam using TIGERv1 (left) and Mainz test beam using TIGERv0 (right).

After the validation of the *S&H mode* for the extraction of fired strips charge information, the cluster charge and size have been evaluated by the clusterization software for the different detector HV settings. The results obtained for orthogonal and 45° tracks are shown in Figure 4.32. Rotating the GEM chamber more strips are hit by the beam and thus more charge is collected.

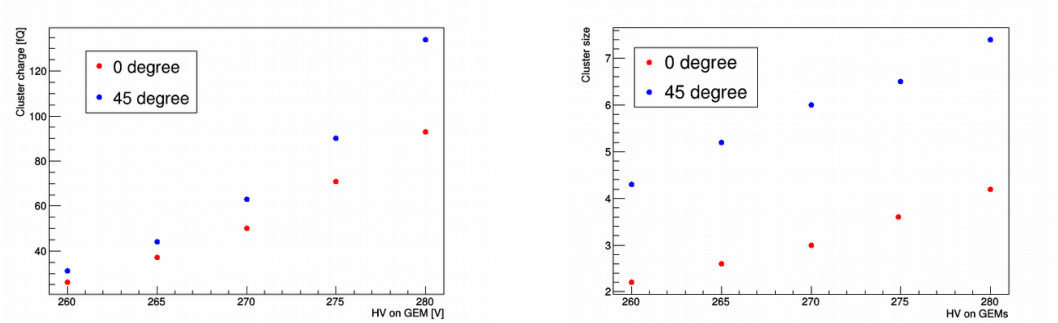


Figure 4.32: Cluster charge (left) and cluster size (right) as a function of the detector HV for different incident angles [72].

Finally, the spatial resolution of the hit reconstruction has been evaluated as a function of the detector gain and the mean cluster charge. The results are reported in Figure 4.33 and 4.34. The measured resolution is kept below the required 130 µm and is in good agreement with the one obtained from the APV25 ASIC, used to readout the GEM chambers in previous beam tests.

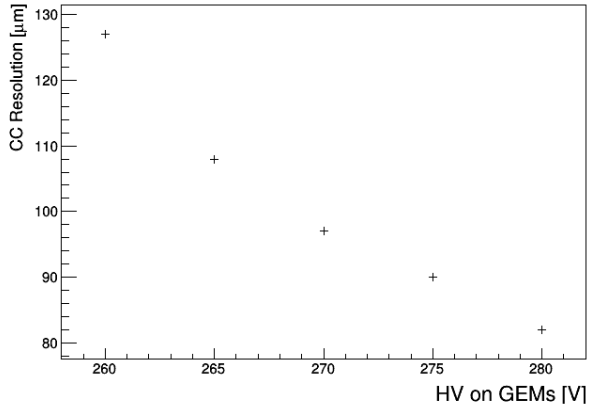


Figure 4.33: Charge centroid spatial resolution for different detector gain settings [72].

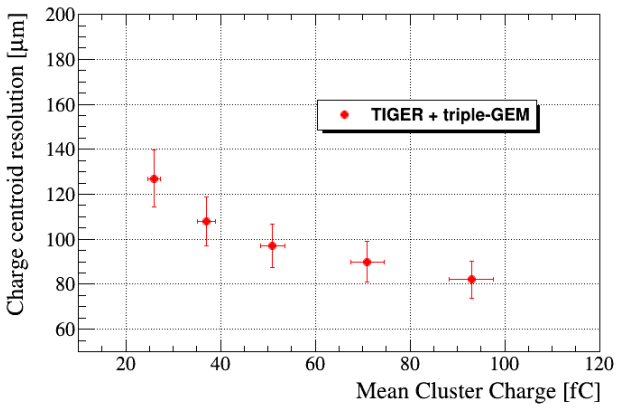


Figure 4.34: Spatial resolution as a function of the mean cluster charge obtained from the charge centroid algorithm using TIGER and planar GEMs [8].

These results prove that the data collected with TIGER can be efficiently reconstructed by the GRAAL clusterization software. However, only the spatial resolution measured with no magnetic field and 0° incident angle is shown. The software to include also angled tracks, which requires the µTPC algorithm, is currently being developed.

4.4.2 Readout of the CGEM-IT

In parallel to the validation with the planar GEMs, as soon as the different components of the CGEM-IT (CGEM detector layers, on-detector and off-detector electronics) were produced and individually validated, integration tests have been carried out in order to assess the functionality of the full system. Figure 4.35 shows the Layer 1 of the CGEM-IT assembled and fully instrumented at the INFN Laboratories of Ferrara, where the CGEM detectors have been developed and characterized.

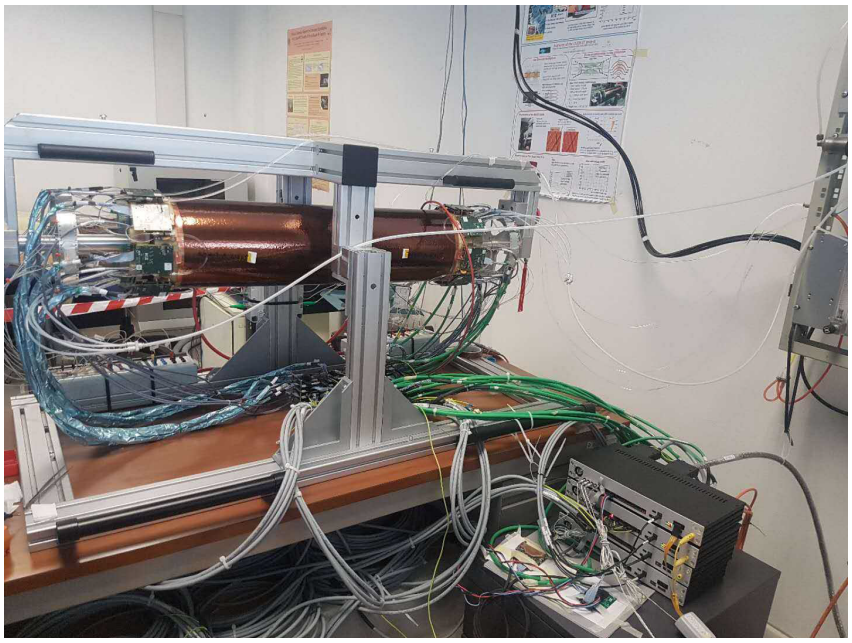


Figure 4.35: CGEM-IT Layer 1 fully instrumented at Ferrara INFN laboratories. The detector is readout by 16 Front-End Boards (32 TIGER) connected to 4 GEMROC (bottom right of the figure) through the LV-DATA Patch Cards (below the CGEM); in the top right corner a small part of the water-cooling system can be spotted.

Compared to the DAQ system used in the beam tests, here, due to the higher number of electronics channels to be managed, the TIGER chips are controlled and readout by the GEMROC modules. Still no GEM Data Collectors are employed, so the GEMROCs are directly readout by the PC running the acquisition through its Ethernet port (UDP communication).

Automatic tools to monitor the system status and configure the TIGER chips have been developed. The delays for the LVDS links TX and RX alignment are automatically set in the optimum point for bug-free data transmission. Custom Python scripts allow to perform threshold scans on every channel and set each threshold to a value specified

by the user. These settings can be then tested in a short acquisition to evaluate the noise occupancy on each channel and eventually fine tune the threshold of screamer channels [65]. For this purpose, a Graphical User Front-end Interface (GUFI, [73]) to select the configuration of the GEMROC modules and the TIGER chips and run and monitor the acquisition has been developed. This software will be later integrated in the BESIII CGEM slow control utility for the experiment run operations.

Figure 4.36 (left) shows the results of a threshold scan performed on the 64 channels of one chip. From this kind of scans the noise level for all the channels of the CGEM-IT Layer 1 has been evaluated. The results are displayed in Figure 4.36 (right). It can be observed the different distribution for X and V strips. The former have all the same length and thus the same capacitance, hence the noise level should be similar for all the strips, while the latter have very different lengths and thus a broader noise distribution. The longest V strips are similar to the X strips, as this measurement seems to confirm.

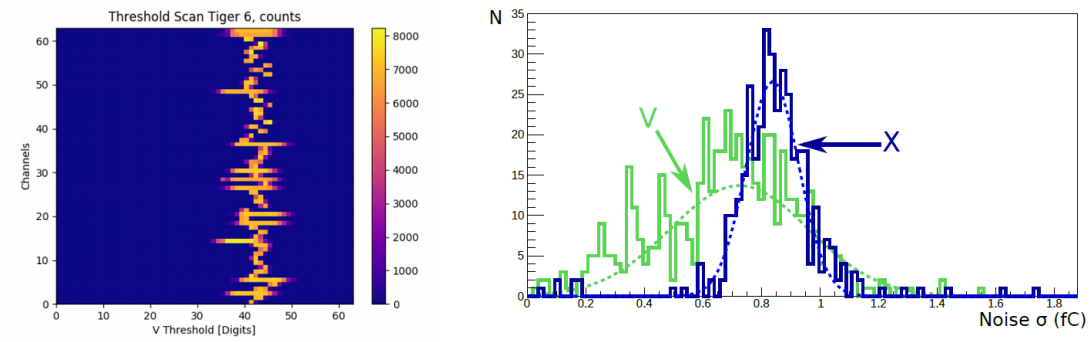


Figure 4.36: 64-channel threshold scan (left) and noise distribution measured on the CGEM-IT Layer 1 for X and V strips [73].

During this phase, also the synchronous operation of more than one GEMROC module was assessed. For this test, an external pulser was employed to generate the reset and trigger signals which were then propagated from the master GEMROC to the three slave GEMROCs.

In order to complete the readout chain validation, interconnection tests between the GEMROC and the GEM-DC have been carried out in February 2019. The setup is shown in Figure 4.37 and includes a FEB controlled by one GEMROC module, coupled to a GEM-DC installed on a VME crate together with a VME-USB Brigde CAEN V1718 board for the communication with the DAQ PC.

These tests proved the correct functionality of the bi-directional communication between the GEMROC module and GEM-DC over optical fiber link at 2 Gb/s. GEMROC

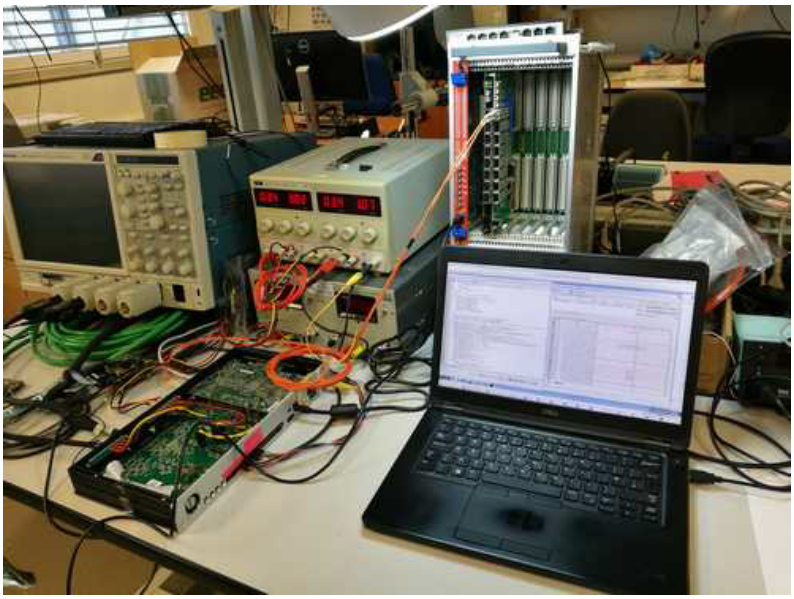


Figure 4.37: GEMROC-GEM DC interconnection test setup.

trigger-matched data packets are correctly transmitted to the GEM-DC and then sent to the PC through the VME. GEM-DC control signals allow to properly read and write the GEMROC configuration registers, while the TIGER configuration is handled through an Ethernet connection. Preliminary tests of the GEM-DC "event building" function have been carried out, some minor revisions to adjust this feature to the CGEM-IT data format are now ongoing.

Instrumentation of the full CGEM-IT detector

The three layers composing the CGEM-IT and all related electronics have been shipped to IHEP (Institute of High Energy Physics, Beijing) in the second half of 2018. The integration of the full system started in November 2018.

Figure 4.38 shows the IHEP laboratory in which the different CGEM layers are mounted, instrumented and tested. The three layers are firstly tested separately to assess their behavior after the shipment. GEM detectors, like most gaseous detectors, need some gas and HV conditioning in order to reach their nominal operation values. In parallel the connectivity of the detector HV and the on-detector electronics LV and data is validated. After that, they are assembled together for tracking measurements using cosmic rays and sources.

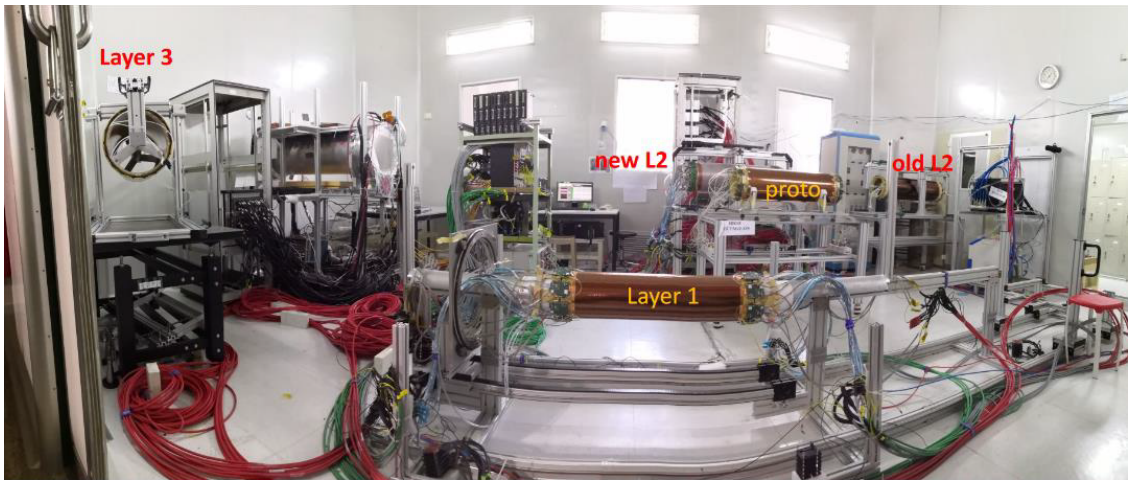


Figure 4.38: IHEP laboratory where the CGEM-IT is assembled. Layer 1 is mounted on the mechanical system used to insert L1 inside L2 and then inside L3. In this picture also two prototype CGEM layers built during the development of the CGEM-IT are present.

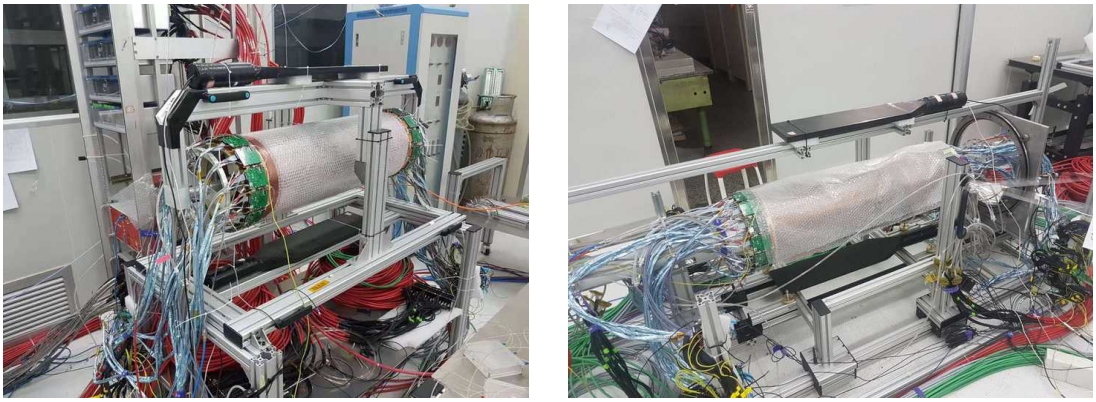


Figure 4.39: Test setups for Layer 2 stand-alone (left) and Layer 1 and 2 assembled together (right).

Figure 4.39 (left) shows the setup for the Layer 2 characterization, while the system incorporating the first two layers is displayed in Figure 4.39 (right). In both cases, the external trigger is provided by two scintillators placed above and below the detector. In order to simulate the BESIII L1 trigger latency, a 8.6 µs delay is applied to the scintillators coincidence signal before it is sent to the GEMROC modules which produce trigger-matched data inside a programmable 1.5 µs trigger time window. The trigger signal is also injected into one unused TIGER channel, set in TDC mode, to check the proper functioning of the GEMROC trigger-match operations and provide a global time reference.

Figures 4.40 and 4.41 show the noise level for the Layer 2 of the CGEM-IT. On one hand, the noise level of the X strips is flat along all the strips, except for some outliers, since they all have the same capacitance. On the other hand, the noise level of the V strips is not flat and follows the strips length profile. In general, V strips show a lower noise since their width is much smaller (130 µm *vs* 570 µm). The presence of groups of outliers implies that the system still needs to be optimized. The sectors showing this increased noise are currently being investigated from the point of view of the detector itself and its related electronics. Some improvements have already been observed by enhancing the grounding connection between the detector and the Front-End Boards.

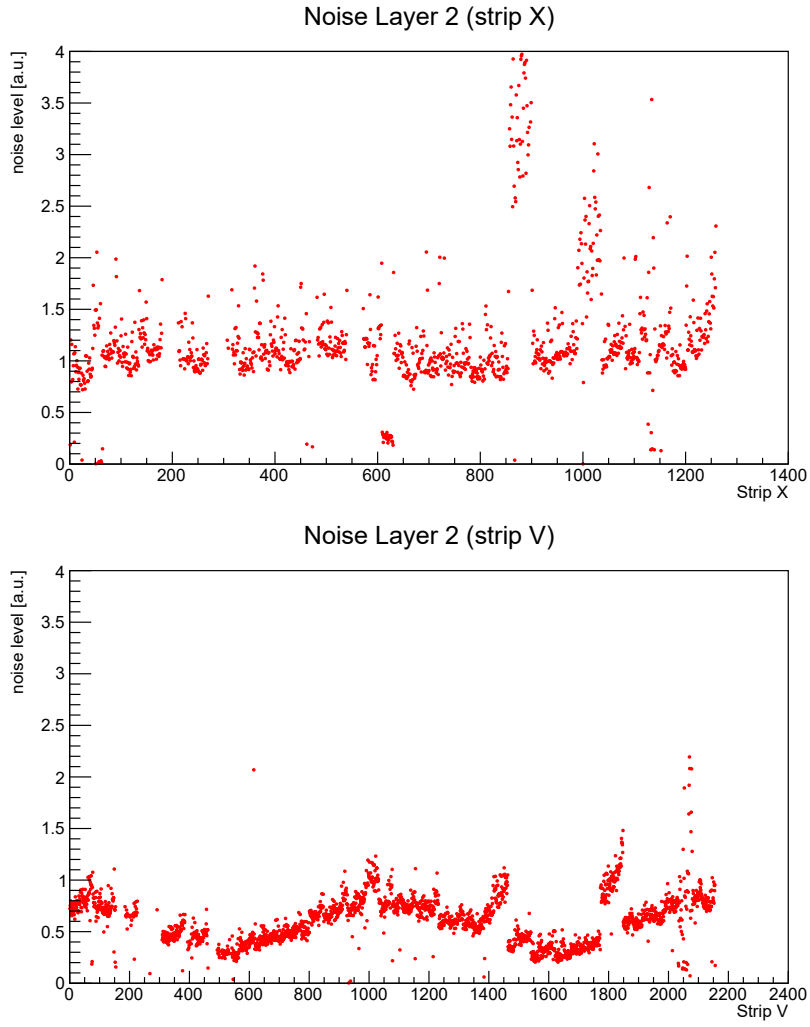


Figure 4.40: Layer 2 noise level profile for X (top) and V (bottom) strips.

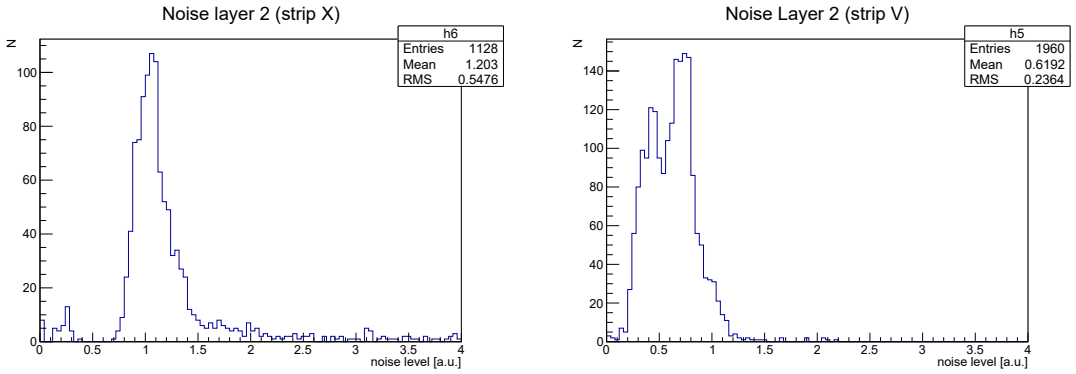


Figure 4.41: Layer 2 noise level distribution for X (left) and V (right) strips.

Cosmic rays data acquisition

At the time of this writing, the assembly of Layer 1 and Layer 2 has been completed and cosmic ray data acquisition is currently ongoing. Some very preliminary results provide a first evaluation of the quality of collected data.

The time information of each fired strip is used to reconstruct the particles track inside the GEMs 5 mm drift gap (refer to 1.2.2). In order to estimate the consistency of this time measurement, the difference between the timestamp of the fired strips and the trigger time reference, for a detector gain of 9000, is plotted in Figure 4.42.

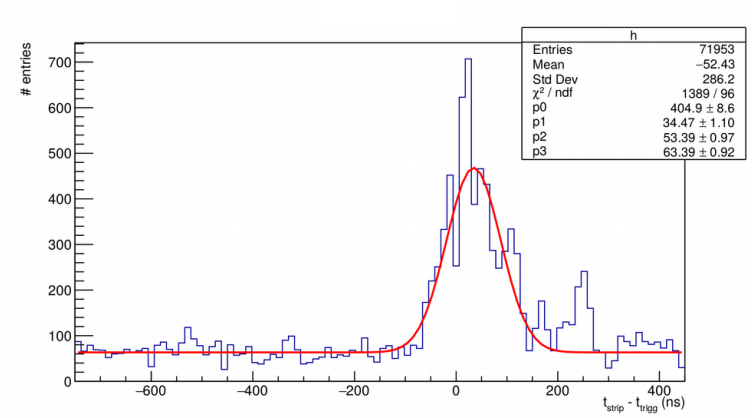


Figure 4.42: Strips time distribution around the trigger time for a gain of 9000.

The resulting distribution is fitted using a "Constant + Gaussian" probability density function, obtaining a FWHM of about 125 ns. Considering a drift velocity, v_d, of 45

μm/ns, it is possible to extract the width of the drift gap as:

$$d = \text{FWHM} \cdot v_d = 45\ \mu\text{m/ns} \cdot 125\ \text{ns} \approx 5.6\ \text{mm} \tag{4.6}$$

This value is in good agreement with the expected 5 mm drift gap width.

The same measurement is repeated with a different gain setting. The strips time distribution for a gain of 12000 is depicted in Figure 4.43.

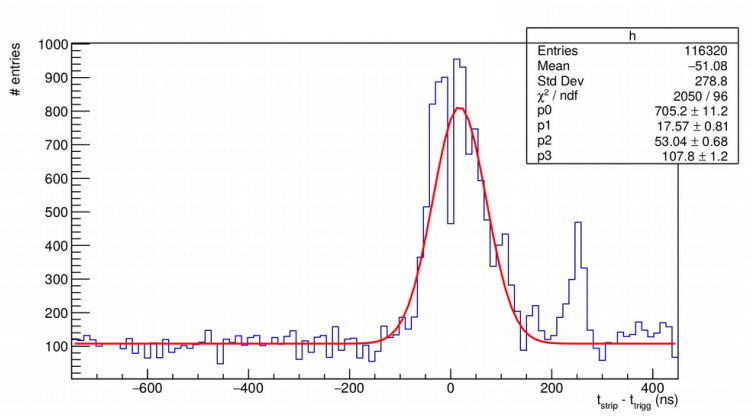


Figure 4.43: Strips time distribution around the trigger time for a gain of 12000.

Here we obtain a very similar result, proving that the drift time does not depend on the detector HV. The strips time distribution is constant for two different gain settings and compatible with the gap width. A more complete and precise measurement will be given by the clusterization algorithm which allows to extract and study the time information of each fired strip comprised in one cluster.

For what concerns cosmic rays tracking, the alignment of the two layers and the development of the software analysis tools for the events reconstruction are currently ongoing. In the next months, also Layer 3 will be included in the system and the integration of the full CGEM-IT detector will be completed.

Chapter 5

Summary and Outlook

For the upgrade of the BESIII inner tracker a novel lightweight detector, based on CGEM (Cylindrical Gas Electron Multiplier) technology has been developed. Once installed, the CGEM detector will be the first cylindrical GEM tracker with analogue readout inside a strong magnetic field.

In this context, the overall Ph.D. research activity has been focused on the design and characterization of a mixed-signal ASIC, named TIGER, suitable for the analogue readout of the CGEM-IT. The design of the ASIC analogue front-end was essentially driven by the CGEM-IT requirements, i.e. noise below 2000 electrons r.m.s. for input capacitance values up to 100 pF, input signals up to 50 fC and a maximum event rate of 60 kHz per channel. For each one of the 64 channels a dual-branch architecture, including shapers with different peaking times optimized for timing and energy measurement, has been adopted. The peaking time of the fast shaper has been set to 60 ns, in order to match the typical sensor charge collection time and thus provide a low-jitter time measurement. For the slower shaper a peaking time as long as permitted by rate considerations has been chosen in order to optimize the signal-to-noise ratio.

The ASIC is self-triggered and provides simultaneous measurement of input signals time of arrival and deposited charge, with a fully digital output. The input signal charge information is provided by peak detection with a S&H circuit or from the pulse duration measured with the Time-over-Threshold technique. The digitization is performed by a versatile mixed-signal back-end, comprising low-power Time to Digital Converters based on analogue interpolation and Wilkinson Analogue to Digital Converters.

The chip has been designed and fabricated in a cost-effective 110 nm CMOS technology. Given the very strict schedule imposed by the collaboration, the first version

prototype already included all the blocks foreseen in the final system. The digital logic and the analogue TDCs were inherited from the silicon-proven TOFPET2 ASIC, thus reducing the overall time for the design phase. The mixed-signal part of the ASIC was complemented by a novel S&H circuit providing linear charge measurement with low power consumption.

A comprehensive electrical characterization of TIGER first prototype allowed to discover and properly address a temperature-dependent baseline instability. The origin of this issue, which could limit the ASIC testability, has been investigated both on silicon and with computer simulations. A temporary remedy was adopted in order to complete the on-silicon ASIC characterization. Meanwhile, the shaper and baseline holder blocks were re-designed to correct this malfunctioning for the final version of the ASIC which has been produced in a dedicated engineering run towards the full instrumentation of the CGEM detector.

The ASIC final version has been found fully functional, all measured parameters match very well the design targets. The front-end provides a linear response for input signals up to 50-55 fC, with a gain of about 12 mV/fC. The input dynamic range is up to 50 fC in S&H mode and can be extended using the Time-over-Threshold mode. The low TDCs quantization error does not affect the system time resolution which only depends on the front-end noise performance. Here, a 15-20% higher noise level has been measured in both branches. The origin of this increase has been investigated, but at the moment of this writing a clear explanation is still to be found. However the performance are already adequate for the intended application. The power consumption is about 10-12 mW per channel, depending on the setting of the front-end amplifier.

In order to fully instrument the CGEM detector, more than 160 chips (10000 channels) have been validated and calibrated. For this phase, a fast and reliable procedure has been established. Two beam tests with 10×10 cm^2 planar GEM chambers have provided a validation of the ASIC with the sensor and confirmed the suitability of TIGER for the readout of this class of detectors. Integration tests with the CGEM detector and the full-chain readout electronics are now ongoing. The installation in the BESIII experiment is foreseen for mid 2020.

TIGER has been originally developed for GEM detectors, in particular the cylindrical GEM for the BESIII upgrade, but it can be adapted for a broad class of radiation detectors, including also silicon microstrip sensors. The use of the TIGER ASIC for the SPD detector at NICA (JINR, Dubna, Russia) is under discussion. Moreover, the COMPASS++/AMBER collaboration at the M2 beam line of the CERN SPS wants to replace

the existing ageing MWPC tracking station with large-area GEM or MicroMegas detectors. The first prototype is foreseen for 2021 and TIGER is one of the candidates for the readout electronics.

The versatile signal processing of TIGER mixed-mode back-end makes it suitable to be re-used for the development of new ASICs, where only the very front-end needs to be re-designed, according to the new application requirements, thus allowing for a significant reduction in the time required to develop the full readout system. In addition, some revisions aiming to improve the performance of the back-end are currently under study. More specifically, this upgrade may include an improved TDC architecture without the issue of the interpolators refresh as well as a revised readout scheme for the charge measurement with the S&H circuit in order to increase the dynamic range without introducing ADC non-linearity issues.

The CGEM-IT project significantly boosted the interaction between the European (Helmotz Institute Mainz in Germany, INFN in Italy, Uppsala University in Sweden) and Chinese (IHEP in P.R.C.) Institutions participating in BESIII. In this context, TIGER was the main deliverable of one the work packages (WP3) of the Project n.645664, funded by the European Commission in the call H2020-MSCA-RISE-2014.

Given the good results delivered by this project, the collaboration between INFN and IHEP is foreseen to continue with new proposals for future joint activities between the two institutes. From the IC design point of view, two test campaigns using TIGER for the readout of CZT detectors, developed by the Division of Nuclear Technology and Applications at IHEP, have been carried out and a revised version of the ASIC optimized for this class of detectors is currently under study. Additionally, TIGER will provide the baseline architecture for a first prototype of a Si-strip readout ASIC, featuring a dedicated low-noise very-front-end compatible with the HERD-STK detector, developed by the Astroparticle Physics Center at IHEP.

Appendix A

Optimization of the Shaper-Baseline Holder stage

The prototype version (TIGERv0) presented a drift on the baseline of the shapers output signal. The root cause of this issue was investigated both with silicon measurements and computer simulations.

Baseline instability in the prototype version

Experimental measurements

The baseline level was measured both by probing the analogue debug output of channel 63 and by performing threshold scans on the 64 channels. It was observed that the baseline was almost stuck around 600 mV and mostly insensitive to V_{BL}, the external reference voltage for the Baseline Holder circuit that allows to set the shapers DC output typically around 350 mV.

As a consequence, the front-end dynamic range was reduced by almost half, thus seriously compromising the charge measurement with the S&H circuit. The origin of this baseline offset was thoroughly investigated and the root cause was supposed to be a malfunctioning of the BLH circuit and, in particular, the small bias of the current-starved buffers.

The Baseline Holder circuit schematics is shown in Figure A.1. The BLH currents are designed to be very small and thus their V_{gs}. Due to the non-zero resistance of the power grid, IR drops along the path between the periphery bias cells and the core blocks

generate gradients on the effective VDD and GND seen by the different blocks inside the chip. We can thus define:

$$\begin{cases} \Delta V_{DD} = V_{DD,bias} - V_{DD,core} \\ \Delta GND = GND_{bias} - GND_{core} \end{cases} \tag{A.1}$$

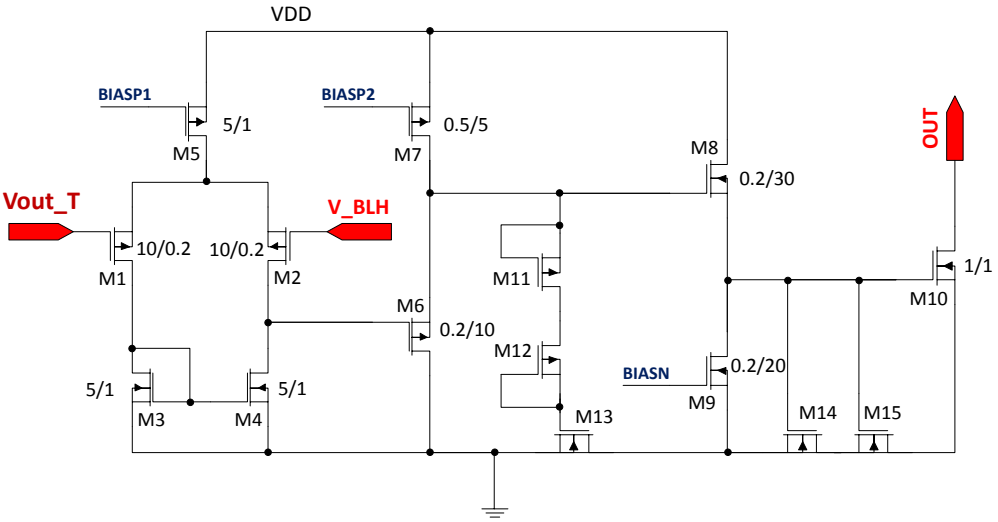


Figure A.1: Baseline Holder circuit schematics.

If ΔV_{DD} or ΔGND are too large then one of the bias transistors (M7 and M9) can be cut off, the loop is opened and the baseline level is defined only by the DC current in the shaper stages, leading to a value very close to the observed 600 mV.

The consistency of this hypothesis was firstly tested on silicon by heating up the chip. In fact, increasing the temperature allows to reduce the threshold voltage of the bias transistor which can be thus turned on again, restoring the functionality of the BLH circuit.

It was observed that as the temperature was increased the baseline level started to decrease approaching to the value imposed by V_{BL}, which was set to 350 mV. Figure A.2 shows the baseline measurement as a function of the temperature. A strong temperature dependence of the baseline can be observed. If the temperature is not kept stable by a suitable cooling system the baseline will drift every time the chip is powered-on, turned off, reset or re-configured.

At higher temperatures (T > 60℃) the baseline seems to stabilize around 380 mV. In principle, operating in this region should allow to keep a stable baseline with an almost

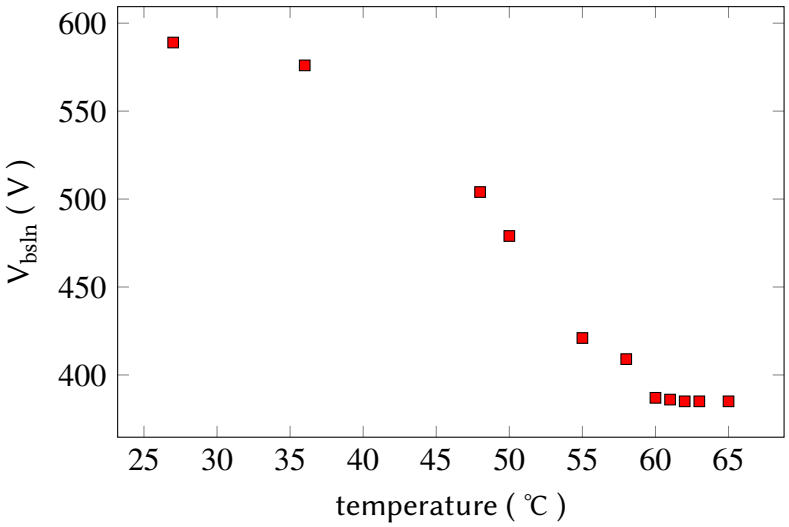


Figure A.2: Measured baseline level as a function of the operating temperature.

fully restored dynamic range. In practice, this solution can be adopted as a temporary remedy to test and characterize the other blocks of the ASIC, but it is not feasible for the final application due to constraints in both power consumption and operating temperature.

Computer simulations

Computer simulations have been performed in order to identify the faulty bias transistor and evaluate the correction needed to provide a more reliable design for the final version.

As a first step, a voltage gradient ΔV_{DD} between the BLH bias and core cells power supply has been applied and the resulting shaper DC output voltage has been evaluated. For these simulations, V_{BL} was set 300 mV in order to keep some safety margin. The results for the time and energy branches are depicted in Figures A.3 and A.4 respectively.

For the time branch, the simulation results show that the BLH circuit starts to fail when $V_{DD,bias} > V_{DD,core}$. For the energy branch the issue is less critical but still present.

The time branch shaper DC output voltage as a function of ΔV_{DD} for different $V_{DD,core}$ values, is displayed in Figure A.5, showing that the margin for the correct behavior of the BLH circuit is only 8 mV. This design weakness can certainly explain the malfunctioning of the BLH circuit and must be properly addressed.

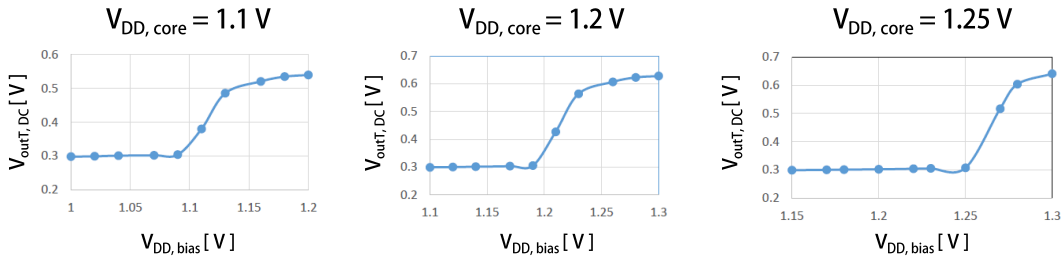


Figure A.3: Time branch shaper DC output voltage as a function of the bias cells power supply for different core cells power supply values.

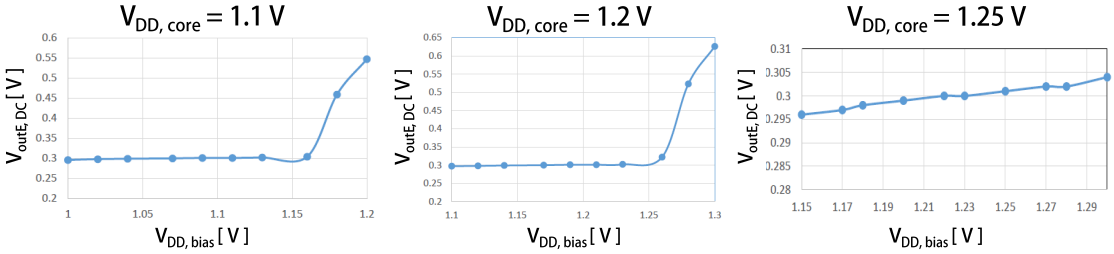


Figure A.4: Energy branch shaper DC output voltage as a function of the bias cells power supply for different core cells power supply values.

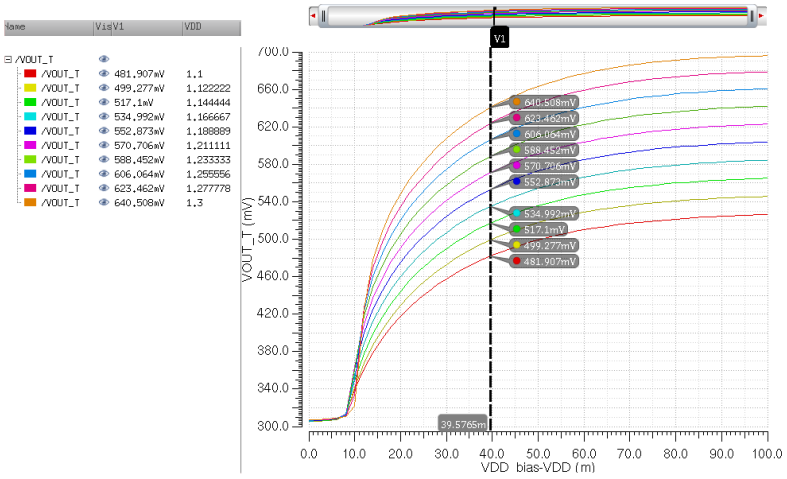


Figure A.5: Time branch shaper DC output voltage as a function of ΔV_{DD} for different $V_{DD,core}$ values.

For the sake of completeness, Figure A.6 shows the same plot for the energy branch. Here the margin is ∼55 mV. The analysis will be focused on the time branch behavior even though some corrections are needed also for the energy branch.

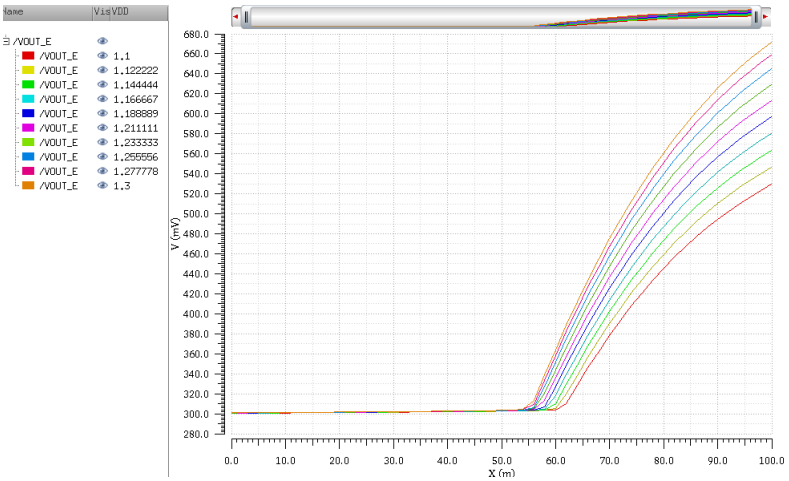


Figure A.6: Energy branch margin (X = ΔV_{DD}).

In order to reproduce the silicon results, a simulation to study the temperature-dependence has been performed. Figure A.7 shows the time branch shaper DC output voltage as a function of ΔV_{DD} for different temperature values. It can be observed that when the temperature is increased the BLH circuit has more margin to work properly, as expected.

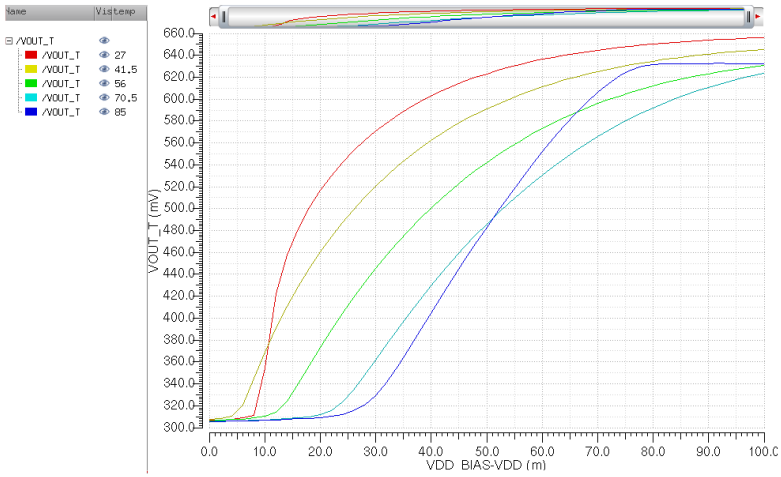


Figure A.7: ΔV_{DD} margin for different temperature values.

The same study with a voltage gradient applied on the GND power rail has been carried out, showing that also the margin ΔGND is too much small even though its impact on the shaper output DC level is less critical.

These results suggest that both bias transistors (M7 and M9 in Figure A.1) are operated with a too small gate-source voltage which cannot be properly propagated from the bias cell to the 64 channels due to IR drops in the correspondent power rail (VDD for M7 and GND for M9).

This is confirmed by the plot of Figure A.8, showing that the BLH circuit starts to fail when the gate voltage of M7 is $\sim$ 1.18 V and thus $V_{sg7} \approx 20$ mV. The circuit was designed to work with a nominal V_{sg7} of 25 mV but due to IR drops the effective value is reduced and the transistor is cut-off.

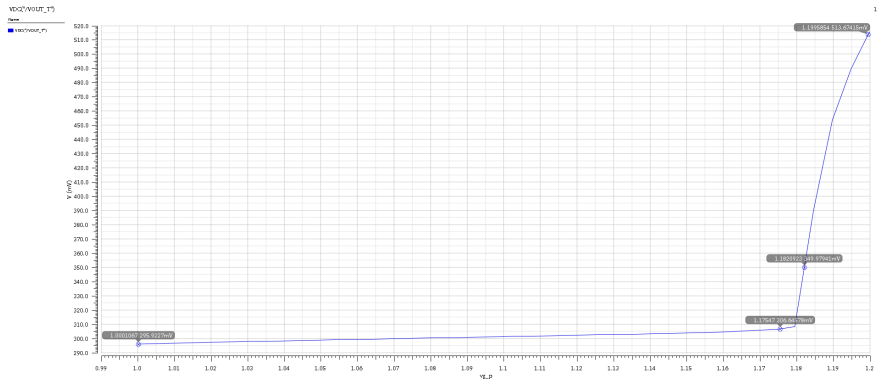


Figure A.8: Time branch shaper DC output as a function of the gate voltage of the PMOS bias transistor (V_{DD} = 1.2 V).

This analysis indicates that larger bias transistors gate voltages should guarantee the correct behavior of the BLH circuit. A re-design of the bias cells providing the gate voltage to M7 and M9 is thus needed in order to reduce the BLH circuit sensitivity to IR drops.

Design revisions for the engineering run version

The BLH circuit and its bias cells have been re-designed with the aim of having larger, and thus easier to propagate, bias voltages. In order to keep a safety margin for all PVT corners, a V_{sg7} of $\sim$150 mV and a V_{gs9} of $\sim$90 mV have been chosen.

The bias cells have been re-sized accordingly, providing nominal bias currents of 3 nA and 1 nA respectively. The maximum and minimum values obtained from PVT

corners simulations, reported in Table A.1, allow for a correct functioning of the BLH circuit.

Parameters	MIN	MAX
I_{M7}	765 pA	5.42 nA
I_{M9}	329 pA	5.26 nA

Table A.1: Maximum and minimum values of the BLH bias current obtained from PVT corners simulations (ΔV_{DD} and ΔGND up to 50 mV, T from 0℃ to 100℃).

In order to check the circuit stability, high-rate (200 kHz) and long-time (1 s) simulations have been carried out. No baseline drifts or oscillations have been observed.

In addition, since the BLH circuit must cope with the current of the shaper feedback network, some modifications have been made to the shaper core amplifier design.

A block diagram of the full shaper stage (core amplifiers, feedback network, BLH) is shown in Figure A.9, while the shaper core amplifier schematic representation is displayed in Figure A.10.

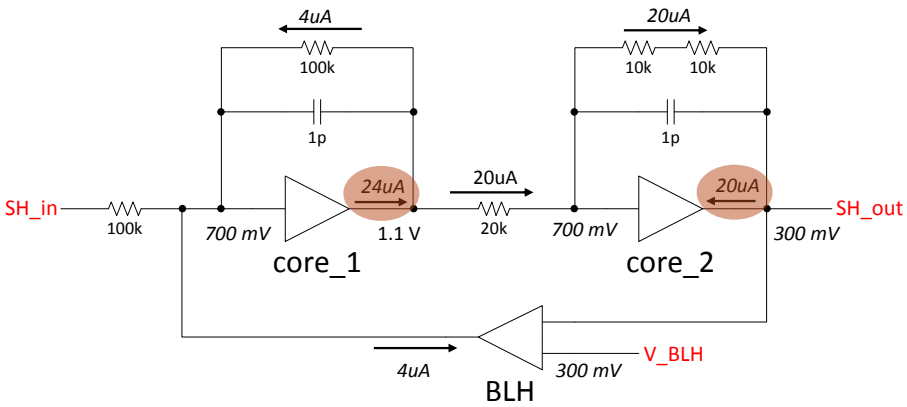


Figure A.9: Block diagram of the time branch shaper + BLH stage. The relevant DC operating points and the feedback network currents that must be provided by the two shaper cores and the BLH circuit are reported.

Minimum feature size transistors (M8, M9, M10) have been re-sized in order to reduce their sensitivity to process variations. Moreover, given the large voltage swing occurring at the shaper cores output, the bias current of the output stage (BIASP3) has been increased in order to provide more headroom to keep the transistors in saturation.

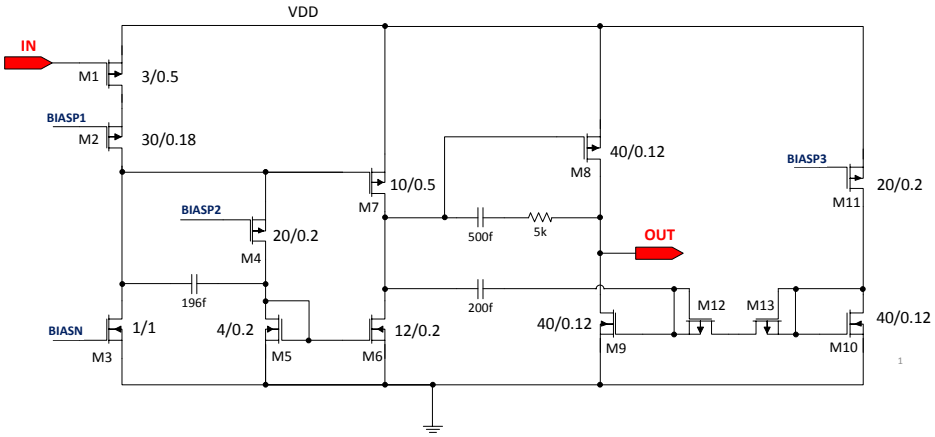


Figure A.10: Shaper core amplifier schematics: old design.

In order to validate the design after the aforementioned modifications, extensive post-layout simulations have been carried out. Process, Voltage (applying a voltage gradient between the bias and core cells to simulate IR drops) and Temperature (from 0℃ to 100℃) corners have been taken into account.

Figure A.11 shows the response of the two shapers. The DC voltage is correctly set around 300 mV with a dispersion of 10 and 8 mV for the time and energy branch, respectively.

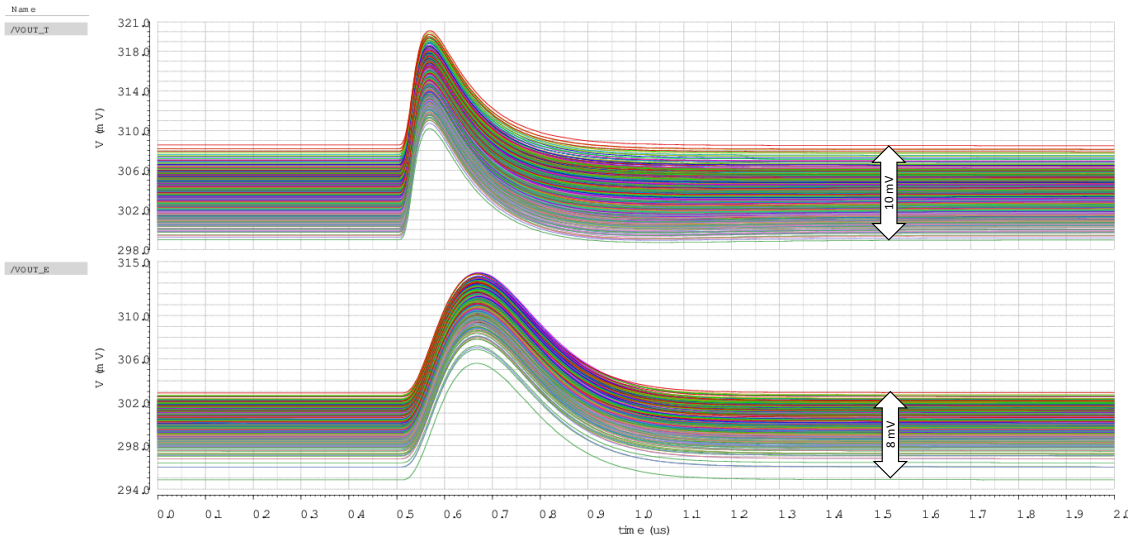


Figure A.11: PVT corners post-layout simulations of the time branch (top) and energy branch (bottom) outputs.

Appendix B

TIGER configuration registers

The ASIC configuration registers comprise a 169-bit global configuration vector and a 125-bit per channel configuration vector, that are read and written through an SPI-like interface at 10 MHz.

The global and channel configuration registers, and their default values, are reported in Tables B.1 and B.2. Fields in little-endian format are marked with *.

Global configuration register

g_config	Name	Value	Description
<168:167>	Buffer bias	3	current bias of the output buffers
<166:163>	TDC VcasN*	0	cascode voltage of the TAC core amplifier
<162:158>	TDC VcasP*	29	current bias of the TAC core amplifier
<157:152>	VcasP hyst T2*	55	LSB for Vth_T2 and hyst_T2
<151:146>	Disc FE Ibias*	50	discriminators current bias
<145:140>	Bias FE PreN	0	current bias of the CSA input stage
<139:135>	A Vcasp global*	19	global DAC for LSB adjustment
<133:130>	TDC comp Vcas*	0	latched comparator cascode voltage
<129:125>	TDC Iref cs*	15	reference current for discharging and recharging the TDC
<118:115>	Disc VcasN*	15	discriminators cascode voltage
<114:109>	Integ Vb1 - Vb4*	60	bias of the S&H folded cascode amplifier
<107:104>	Bias FE A1 10uA	14	current bias of the CSA output stage
<103:98>	VcasP Vth T1*	55	LSB for Vth_T1 and hyst_T1
<97:93>	TAC I LSB	0	LSB of the DAC current to discharge the TAC

<92:88>	TDC comp Vbias	0	current bias for the TDC latched comparator
<76:71>	Vref integ*	30	S&H reference voltage
<70:66>	Ibias TP cal diff*	26	current bias for the TP_Vcal_ref buffer
<65:61>	TP Vcal*	10	TP bias voltage
<60:57>	Shaper Ibias	0	shaper current bias
<55:51>	Ipostamp*	26	vth_T1 and vth_T2 DC offset
<50:46>	TP_Vcal_ref*	10	TP reference voltage
<45:40>	Vref_integ_diff_bias*	39	current bias for the v_ref_integ buffer
<33>	TP polarity	1	test-pulse polarity
<32>	FE TP enable	1	enable the TP generation for the FE
<30:29>	Data clk div	0	data clock divider (8 to 64)
<28:25>	TAC refresh period	9	set the refresh period (64 to 1024)
<24>	TAC refresh enable	1	enable the TAC buffer refresh
<23:21>	Counter period	6	set counter period
<20>	Counter enable	1	enable event counter
<19:18>	Stop ramp enable	0	TDC operation period
<15:13>	R clk enable	7	duration of control logic signals
<12>	TDC clk div	0	divide TDC clk by 2 (320-400 MHz)
<11:6>	Veto mode	0	enable triggering veto
<5>	Debug mode	0	enable TX1-TX3 for debug signals
<4:3>	Tx mode	2	data transmission mode (normal or training patterns)
<2>	Tx DDR	1	enable double data rate
<1:0>	Tx links	2	number of TX links enabled (1, 2, 4)

Table B.1: Global configuration register content.

Channel configuration register

c_config	Name	Value	Description
<124>	hyst dis	1	disable hysteresis
<120:118>	T2 hyst	7	set hysteresis for the E-branch
<117:115>	T1 hyst	7	set hysteresis for the T-branch
<110>	Ch63 obuf msb	1	MSB for the ch 63 output buffers bias
<108>	TP disable	1	disable the FE from receiving the TP signal
<107:104>	TDC IB E	15	E-TAC DAC discharge current adjustment
<103:100>	TDC IB T	15	T-TAC DAC discharge current adjustment

<95>	Integ enable	1	enable the S&H output
<90:89>	Postamp gain T	0	set vth_T1 and vth_T2 DC offset
<88:84>	FE delay	1	do_T1 delay line settings
<74:69>	Vth T2	0	threshold of the E-branch discriminator
<68:63>	Vth T1	0	threshold of the T-branch discriminator
<56>	Qtx2 enable	1	double duration of q_tx
<53:47>	Max integ time	5	set S&H sampling time duration
<46:40>	Min integ time	5	set S&H sampling time duration
<39>	Trigger B latched	0	define if Trigger_B is asynchronously latched
<38>	Qdc mode	1	select ToT or S&H mode
<37>	Branch enable T	1	enable the Time-branch
<36>	Branch enable EQ	1	enable the Energy-branch
<35:33>	Trigger mode 2 B	3	set trigger B
<32:31>	Trigger mode 2 Q	0	set trigger Q
<30:28>	Trigger mode 2 E	3	set trigger E
<27:26>	Trigger mode 2 T	0	set trigger T
<25:21>	TAC min age	10	define the TAC settling time after reset (in clocks)
<20:16>	TAC max age	31	define the TAC max idle time (in refresh strobes)
<15:12>	Counter mode	0	define the counting mode
<11:6>	Dead time	0	set additional dead-time after an event (in clocks)
<5:4>	Sync chain length	0	define the length of metastability synchronization chain
<3:2>	Debug mode	0	select the output debug signals
<1:0>	Trigger mode	0	set the trigger logic

Table B.2: Channel configuration register content.

Configuration modes

Different operation modes can be enabled by setting the proper configuration registers.

S&H and ToT mode

In the default configuration, the charge measurement is provided by the S&H circuit, whose sampling time window must be set accordingly to the clock frequency. In general with a 160 MHz clock frequency Max integ time and Min integ time are set to 5, while for a 200 MHz clock frequency they are set to 7. Switching to *ToT mode* requires to set Integ enable = 0 and Qdc mode = 0.

Threshold settings

The threshold values (Vth T1 and Vth T2) must be set individually on a per-channel basis after performing a threshold scan. The single-threshold readout mode can be enabled by setting Trigger mode 2 B = 0 and Trigger mode 2 E = 0. In this way the trigger signals are generated only by the time branch discriminator.

TDC mode

The TDC calibration requires to bypass the analogue front-end and send the external test-pulse directly to the TDCs, which can be thus calibrated by sweeping the test-pulse phase with respect to the chip clock. This can be done by setting Trigger mode = 1.

It must be pointed out that FE TP enable and TP disable must be kept at their default values (0 and 1, respectively) since they are related only to the generation of the analogue test-pulse signal for the front-end.

This operation mode can also be exploited to use one channel to store the time information of an external trigger, which can then be retrieved back to match the data of the other channels to the trigger signal.

Front-End TP mode

This mode is used to test the front-end response when the chip is not connected to any sensor. The generation of the test-pulse is enabled by setting FE TP enable = 1. This only enables the periphery calibration circuit to produce a voltage step whose polarity

and amplitude are defined by TP POLARITY, TP VCAL, TP_VCAL_REF and IBIAS TP CAL DIFF (refer to 3.3.2).

In order to enable one channel to receive this test-pulse the channel configuration register TP DISABLE must be set to 0, thus allowing to select only one channel to be the target of the test-pulse. If two or more channels are enabled for the test-pulse injection at the same time the voltage step generated by the periphery calibration circuit is shared between the channels, thus resulting in a smaller input charge.

Debug output mode

In order to probe the two analogue debug ports the output buffers must be properly biased by setting CH63 OBUF MSB = 0 and BUFFER BIAS = 0.

The digital debug outputs are enabled by setting the global configuration register DEBUG MODE to 1 and then selecting the required signal with the channel configuration register DEBUG MODE (refer to 3.3.4). This mode requires also to set TX LINKS = 0, i.e. only one TX link for real data transmission, since the other 3 TX links are employed for the transmission of the digital debug signals.

Appendix C

Front-End Board pinout

Due to the different anode geometry of the three layers of the CGEM-IT, the connector of the Front-End Boards has a different pinout. For the same reason, some channels are not used in FEBs for L2 and L3:

- Layer 1: all channels connected;
- Layer 2: channels 61, 62 and 63 disconnected;
- Layer 3: channels 62 and 63 disconnected.

In the following pages the anode connector pinout of the three different layers FEB is shown with the notation as follows:

- *P<n>* is the connector pin number
- *<chip>_<channel>* indicates the chip and the channel number

2_3	P1	P2	2_45
2_11	P3	P4	2_47
2_22	P5	P6	2_54
2_4	P7	P8	2_41
2_12	P9	P10	2_43
2_23	P11	P12	2_33
2_19	P13	P14	2_39
2_15	P15	P16	2_37
2_14	P17	P18	2_6
2_61	P19	P20	2_9
2_0	P21	P22	2_25
2_26	P23	P24	2_29
2_49	P25	P26	2_7
2_63	P27	P28	2_1
2_62	P29	P30	2_27
2_20	P31	P32	2_13
2_51	P33	P34	2_31
2_28	P35	P36	2_35
2_16	P37	P38	2_57
2_56	P39	P40	2_53
2_59	P41	P42	2_2
2_52	P43	P44	2_17
2_60	P45	P46	2_21
2_40	P47	P48	2_8
2_55	P49	P50	2_10
2_58	P51	P52	2_5
2_50	P53	P54	2_24
2_46	P55	P56	2_18
2_44	P57	P58	2_30
2_48	P59	P60	2_32
2_36	P61	P62	1_58
2_42	P63	P64	1_13
2_38	P65	P66	1_40
2_34	P67	P68	1_7
1_36	P69	P70	1_3
1_62	P71	P72	1_32
1_48	P73	P74	1_34
1_26	P75	P76	1_46
1_22	P77	P78	1_44
1_28	P79	P80	1_50
1_24	P81	P82	1_43
1_20	P83	P84	1_59
1_14	P85	P86	1_56
1_61	P87	P88	1_53
1_9	P89	P90	1_17
1_63	P91	P92	1_37
1_5	P93	P94	1_51
1_30	P95	P96	1_60
1_2	P97	P98	1_11
1_18	P99	P100	1_52
1_16	P101	P102	1_27
1_38	P103	P104	1_54
1_0	P105	P106	1_49
1_42	P107	P108	1_55
R	P109	P110	1_39
R	P111	P112	1_19
R	P113	P114	1_15
R	P115	P116	1_25
R	P117	P118	1_31
R	P119	P120	1_29
R	P121	P122	1_1
R	P123	P124	1_35
R	P125	P126	1_41
R	P127	P128	1_33
R	P129	P130	1_6
R	P131	P132	1_12
R	P133	P134	1_4
R	P135	P136	1_23
R	P137	P138	1_10
R	P139	P140	1_47
1_45	P141	P142	1_21
1_57	P143	P144	1_8

CHIP 1

ch	PIN
0	105
1	122
2	97
3	70
4	134
5	93
6	130
7	68
8	144
9	89
10	138
11	98
12	132
13	64
14	85
15	114
16	101
17	90
18	99
19	112
20	83
21	142
22	77
23	136
24	81
25	116
26	75
27	102
28	79
29	120
30	95
31	118
32	72
33	128
34	74
35	124
36	69
37	92
38	103
39	110
40	66
41	126
42	107
43	82
44	78
45	141
46	76
47	140
48	73
49	106
50	80
51	94
52	100
53	88
54	104
55	108
56	86
57	143
58	62
59	84
60	96
61	87
62	71
63	91

CHIP 2

ch	PIN
0	21
1	28
2	42
3	1
4	7
5	52
6	18
7	26
8	48
9	20
10	50
11	3
12	9
13	32
14	17
15	15
16	37
17	44
18	56
19	13
20	31
21	46
22	5
23	11
24	54
25	22
26	23
27	30
28	35
29	24
30	58
31	34
32	60
33	12
34	67
35	36
36	61
37	16
38	65
39	14
40	47
41	8
42	63
43	10
44	57
45	2
46	55
47	4
48	59
49	25
50	53
51	33
52	43
53	40
54	6
55	49
56	39
57	38
58	51
59	41
60	45
61	19
62	29
63	27

Figure C.1: Layer 1 FEB pinout.

2_3	P1	P2	2_45
2_11	P3	P4	2_47
2_22	P5	P6	2_54
2_4	P7	P8	2_41
2_12	P9	P10	2_43
2_23	P11	P12	2_33
2_19	P13	P14	2_39
2_15	P15	P16	2_37
2_14	P17	P18	2_6
2_60	P19	P20	2_9
2_0	P21	P22	2_25
2_26	P23	P24	2_29
2_49	P25	P26	2_7
2_55	P27	P28	2_1
2_51	P29	P30	2_27
2_20	P31	P32	2_13
2_16	P33	P34	2_31
2_28	P35	P36	2_35
2_59	P37	P38	2_57
2_56	P39	P40	2_53
2_50	P41	P42	2_2
2_52	P43	P44	2_17
2_58	P45	P46	2_21
2_46	P47	P48	2_8
2_40	P49	P50	2_10
2_48	P51	P52	2_5
2_44	P53	P54	2_24
2_42	P55	P56	2_18
2_36	P57	P58	2_30
2_34	P59	P60	2_32
2_38	P61	P62	1_5
1_26	P63	P64	1_42
1_28	P65	P66	1_9
1_20	P67	P68	1_58
1_24	P69	P70	1_13
1_22	P71	P72	1_7
1_2	P73	P74	1_3
1_48	P75	P76	1_32
1_0	P77	P78	1_34
1_36	P79	P80	1_46
1_16	P81	P82	1_44
1_18	P83	P84	1_56
1_38	P85	P86	1_43
1_30	P87	P88	1_59
1_14	P89	P90	1_54
R	P91	P92	1_53
R	P93	P94	1_17
R	P95	P96	1_37
R	P97	P98	1_11
R	P99	P100	1_51
R	P101	P102	1_27
R	P103	P104	1_60
R	P105	P106	1_25
R	P107	P108	1_55
R	P109	P110	1_39
R	P111	P112	1_19
R	P113	P114	1_15
R	P115	P116	1_49
R	P117	P118	1_31
R	P119	P120	1_29
R	P121	P122	1_1
R	P123	P124	1_35
R	P125	P126	1_41
R	P127	P128	1_33
R	P129	P130	1_6
R	P131	P132	1_12
R	P133	P134	1_4
1_40	P135	P136	1_23
1_52	P137	P138	1_10
1_50	P139	P140	1_47
1_45	P141	P142	1_21
1_57	P143	P144	1_8

CHIP 1

ch	PIN
0	77
1	122
2	73
3	74
4	134
5	62
6	130
7	72
8	144
9	66
10	138
11	98
12	132
13	70
14	89
15	114
16	81
17	94
18	83
19	112
20	67
21	142
22	71
23	136
24	69
25	106
26	63
27	102
28	65
29	120
30	87
31	118
32	76
33	128
34	78
35	124
36	79
37	96
38	85
39	110
40	135
41	126
42	64
43	86
44	82
45	141
46	80
47	140
48	75
49	116
50	139
51	100
52	137
53	92
54	90
55	108
56	84
57	143
58	68
59	88
60	104

CHIP 2

ch	PIN
0	21
1	28
2	42
3	1
4	7
5	52
6	18
7	26
8	48
9	20
10	50
11	3
12	9
13	32
14	17
15	15
16	33
17	44
18	56
19	13
20	31
21	46
22	5
23	11
24	54
25	22
26	23
27	30
28	35
29	24
30	58
31	34
32	60
33	12
34	59
35	36
36	57
37	16
38	61
39	14
40	49
41	8
42	55
43	10
44	53
45	2
46	47
47	4
48	51
49	25
50	41
51	29
52	43
53	40
54	6
55	27
56	39
57	38
58	45
59	37
60	19

Figure C.2: Layer 2 FEB pinout.

2_3	P1	P2	2_45
2_11	P3	P4	2_47
2_22	P5	P6	2_54
2_4	P7	P8	2_41
2_12	P9	P10	2_43
2_23	P11	P12	2_33
2_19	P13	P14	2_39
2_15	P15	P16	2_37
2_14	P17	P18	2_6
2_60	P19	P20	2_9
2_0	P21	P22	2_25
2_26	P23	P24	2_29
2_49	P25	P26	2_7
2_55	P27	P28	2_1
2_51	P29	P30	2_27
2_20	P31	P32	2_13
2_16	P33	P34	2_31
2_28	P35	P36	2_35
2_59	P37	P38	2_57
2_56	P39	P40	2_53
2_50	P41	P42	2_2
2_52	P43	P44	2_17
2_58	P45	P46	2_21
2_46	P47	P48	2_8
2_40	P49	P50	2_10
2_48	P51	P52	2_5
2_44	P53	P54	2_24
2_42	P55	P56	2_18
2_36	P57	P58	2_30
2_34	P59	P60	2_32
2_38	P61	P62	1_5
1_26	P63	P64	1_42
1_28	P65	P66	1_9
1_20	P67	P68	1_58
1_24	P69	P70	1_13
1_22	P71	P72	1_7
1_2	P73	P74	1_3
1_48	P75	P76	1_32
1_0	P77	P78	1_34
1_36	P79	P80	1_46
1_16	P81	P82	1_44
1_18	P83	P84	1_56
1_38	P85	P86	1_43
1_30	P87	P88	1_59
1_14	P89	P90	1_54
2_61	P91	P92	1_53
R	P93	P94	1_17
R	P95	P96	1_37
R	P97	P98	1_11
R	P99	P100	1_51
R	P101	P102	1_27
R	P103	P104	1_60
R	P105	P106	1_25
R	P107	P108	1_55
R	P109	P110	1_39
R	P111	P112	1_19
R	P113	P114	1_15
R	P115	P116	1_49
R	P117	P118	1_31
R	P119	P120	1_29
R	P121	P122	1_1
R	P123	P124	1_35
R	P125	P126	1_41
R	P127	P128	1_33
R	P129	P130	1_6
R	P131	P132	1_12
1_61	P133	P134	1_4
1_40	P135	P136	1_23
1_52	P137	P138	1_10
1_50	P139	P140	1_47
1_45	P141	P142	1_21
1_57	P143	P144	1_8

CHIP 1		**CHIP 2**	
ch	PIN	ch	PIN
0	77	0	21
1	122	1	28
2	73	2	42
3	74	3	1
4	134	4	7
5	62	5	52
6	130	6	18
7	72	7	26
8	144	8	48
9	66	9	20
10	138	10	50
11	98	11	3
12	132	12	9
13	70	13	32
14	89	14	17
15	114	15	15
16	81	16	33
17	94	17	44
18	83	18	56
19	112	19	13
20	67	20	31
21	142	21	46
22	71	22	5
23	136	23	11
24	69	24	54
25	106	25	22
26	63	26	23
27	102	27	30
28	65	28	35
29	120	29	24
30	87	30	58
31	118	31	34
32	76	32	60
33	128	33	12
34	78	34	59
35	124	35	36
36	79	36	57
37	96	37	16
38	85	38	61
39	110	39	14
40	135	40	49
41	126	41	8
42	64	42	55
43	86	43	10
44	82	44	53
45	141	45	2
46	80	46	47
47	140	47	4
48	75	48	51
49	116	49	25
50	139	50	41
51	100	51	29
52	137	52	43
53	92	53	40
54	90	54	6
55	108	55	27
56	84	56	39
57	143	57	38
58	68	58	45
59	88	59	37
60	104	60	19
61	133	61	91

Figure C.3: Layer 3 FEB pinout.

Glossary

ADC	Analogue to Digital Converter
APV	Analogue Pipeline Voltage mode
ASIC	Application-Specific Integrated Circuit
ATLB	Advanced Trigger Logic Board
BEPCII	BEijing Electron and Positron Collider II
BESIII	BEijing Spectrometer III
BLH	Baseline Holder
BW	Bandwidth
CC	Charge Centroid
CFD	Constant Fraction Discriminator
CGEM-IT	Cylindrical Gas Electron Multiplier Inner Tracker
CMOS	Complementary Metal-Oxide-Semiconductor
CSA	Charge-Sensitive Amplifier
DAC	Digital to Analogue Converter
DAQ	Data Acquisition
DDR	Double Data Rate
DLVPC	Data and Low Voltage Patch Card
EMC	Electromagnetic Calorimeter
ENC	Equivalent Noise Charge
ESD	Electrostatic Discharge

FEB	Front-End Board
FMC	FPGA Mezzanine Card
FPGA	Field Programmable Gate Array
GASTONE	Gem Amplifier Shaper Tracking ON Events
GbE	Gigabit Ethernet
GEM-DC	GEM Data Collector
GEM	Gas Electron Multiplier
GEMROC	GEM Read-Out Card
GRAAL	Gem Reconstruction And Analysis Library
GUFI	Graphical User Front-end Interface
IC	Integrated Circuit
IHEP	Institute for High Energy Physics
KLOE	K^0_L LOng Experiment
LSB	Least Significant Bit
LUT	Look-Up Table
LVDS	Low-Voltage Differential Signaling
MAMI	Mainz Microtron
MDC	Multi-layer Drift Chamber
µTPC	micro Time Projection Chamber
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
MPW	Multi-Project Wafer
PCB	Printed Circuit Board
PET	Positron Emission Tomography
PSRR	Power Supply Rejection Ratio
PVT	Process, Voltage and Temperature

RMS	Root Mean Square
RPC	Resistive Plate Chamber
S&H	Sample-and-Hold
SDR	Single Data Rate
SEU	Single-Event Upset
SiPM	Silicon Photo-multiplier
SMA	Sub-Miniature type A
SMD	Surface-Mount Device
SNR	Signal-to-Noise Ratio
SPI	Serial Peripheral Interface
TAC	Time to Amplitude Converter
TDC	Time to Digital Converter
TID	Total Ionizing Dose
TIGER	Turin Integrated Gem Electronics for Readout
TMR	Triple Modular Redundancy
TOF	Time-Of-Flight
TOFPET	Time-Of-Flight Positron Emission Tomography
ToT	Time-over-Threshold
UDP	User Datagram Protocol
VME	VERSABUS Module Eurocard

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