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Capacitive coupled RFID tag using a new dielectric droplet encapsulation approach

By

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Declaration

I hereby declare that, the contents and organization of this dissertation constitute my own original work and does not compromise in any way the rights of third parties, including those relating to the security of personal data.

Lorenzo Pirrami
2018

* This dissertation is presented in partial fulfillment of the requirements for **Ph.D. degree** in the Graduate School of Politecnico di Torino (ScuDo).

I would like to dedicate this thesis to my loving family

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Abstract

Radio frequency identification (RFID) is a well-known and fast-growing technology used to identify people, animals and products. RFID tags are used to replace bar codes in a wide range of applications, to mention just a few, retail, transportation, logistics and healthcare.

The two main driving aspects for most of research and development projects concerning RFID tags are the reduction of assembly costs and the downsizing of microchips. In that respect and considering an Industry 4.0 scenario, the study of a new assembly approach for passive and high frequency RFID tags has been proposed and studied in this thesis.

In this new approach, which is based on the inkjet printing technology, a specifically designed radio frequency integrated circuit (RFIC) will be delivered, inside a liquid dielectric droplet, onto the antenna and no longer placed and oriented precisely as it happens nowadays with pick-and-place and flip chip machines. After a landing phase, the liquid droplet (with the encapsulated chip) will self-aligns with respect to the contact thanks to capillary forces driven by specifically designed wetting conditions on the substrate of the antenna. Finally, with few additional steps, the complete RFID tag is created.

This research project brings to light a considerable simplification and a very high potential of parallelization, compatible with large volume manufacturing methods, in comparison to nowadays existing technologies. This may substantially drive down the fabrication costs. An in-depth analysis of electrical performances have been carefully undertaken and compliance with the ISO/IEC 144443 standard has been verified. Mathematical models have been developed showing fundamental limits for the maximum tag reading range and power requirements of the RFID reader.

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Nomenclature

Acronyms / Abbreviations

$3L$	Triple Line
ACA	Anisotropic Conductive Adhesive
ACF	Anisotropic Conductive Films
ACP	Anisotropic Conductive Pastes
$C4$	Controlled Collapse Chip Connection
CA	Contact Angle
CCD	Charged Coupled Device
$CMOS$	Complementary Metal-Oxide-Semiconductor
CSA	Capillary Self-Alignment
DOD	Drop-On-Demand
$DS-RFIC$	Double-Surface Radio Frequency Integrated Circuit
$FCBGA$	Flip Chip Ball Grid Array
FSA	Fluidic Self-Assembly
HF	High Frequency
ICA	Isotropic Conductive Adhesives
KCL	Kirchoff's Current Law

LF	Low Frequency
LSI	Large Scale Integrated
LV	Liquid-Vapor
MEMS	Micro-Electro-Mechanical Systems
PARC	Palo Alto Research Center
R2R	Roll-to-Roll
RF	Radio Frequency
RFIC	Radio Frequency Integrated Circuit
RFID	Radio Frequency Identification
ROM	Read Only Memory
SE	Surface Evolver
SL	Solid-Liquid
SOI	Silicon-On Insulator
SV	Solid-Vapor
TAB	Tape Automated Bonding
UBM	Under-Bump Metallization
UHF	Ultra-High Frequency
UPH	Unit Per Hour
UV	Ultraviolet

Chapter 1

Introduction

1.1 Introduction

RFID tags, also called transponders, are based on a well-established and widespread technology with a market of billions pieces fabricated every year. The RFID is part of a range of technologies (such as barcodes, optical card readers, magnetic stripe, etc.) used to collect, store, manage and interpret data. As shown in Fig.1.1, tags are part of RFID systems which consist of two additional components, readers (interrogators) and host computers, or a network, which support user interfaces for specific data processing (backend IT system).

A reader establishes the wireless communication using an integrated antenna (or connected with a cable) for transmitting signals and energy which are both received by the tag. The latter, by means of an integrated antenna, retransmits signals with additional information.

Most tags incorporate an integrated circuit (IC), also called radio frequency integrated circuit (RFIC), which contains an identification (ID), stored in a silicon memory, and performs the processing required for the communication. Depending on the application in which the tag is involved, it may contain sensors (e.g. temperature, humidity, etc.) and associated interfaces.

The applications of the RFID tags span from retail [16], to transportation, logistics & supply chain [17, 18], food [19], healthcare [20], pharmaceuticals, security, interactive marketing, etc. The reason behind the constantly increasing interest in

RFID system is twofold: first, the availability of low-cost RFID tags and second, the global spreading of wireless connectivity and robust network services to complement RFID tags.

To appreciate the range and depth of such a technology, one only has to look at recent announcement of Macy's (one of the largest U.S. retail store) which stated that *"by the beginning of 2017, more than 60 percent of all items in most of its stores will be RFID-tagged and to have 100 percent of all items in all stores tagged by the end of the year"* [21]. The Macy's example is not the only one, in fact, already in 2003 Wal-Mart (another U.S. retail store) adopted RFID tags for improving the supply chain efficiency saving billions of dollars. Many other retailers worldwide are currently using RFID tags across their supply chains.

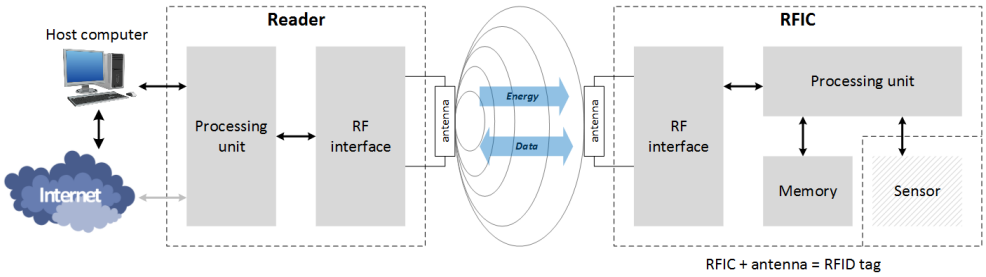


Fig. 1.1 Conceptual view of a simplified RFID system. User - reader interactions are performed between host computers (or directly through the network and specific interfaces and processing unit inside the reader). The reader establishes the communication using an antenna transmitting data and energy to the tag which receives and resends information (e.g. a specific ID) back to the reader after data processing. Some RFID tags have embedded sensors (integrated into the RFIC or as external components) depending on the application in which they are used.

The retail industry will undoubtedly be the highest adopter of RFID tags. According to the analysts at IDTechEx, this sector alone was responsible for the demand of 4.6 billion RFID tags in 2016 and is expected to reach 8.1 billion in 2024 [22]. The benefits from RFID implementation in the retail industry are multiple, to mention just a few: verify the authenticity of products, improve the visibility of products (asset management, tracking shopping behavior, inventory, etc.). Moreover, in a post-sale prospective, RFID tags offer information such as replacement parts, warranty, proper recycling, measuring the environmental conditions in which the products reside, etc.

The RFID technology will play a leading role in manufacturing applications. As part of Industry 4.0, RFID tags allow flexibility, efficiency and individualization in mass-production environments, in fact, products will be able to communicate with

machines and tell what is needed at a given fabrication step (e.g. answer specific customer needs). Moreover, RFID systems reduce the need of human intervention, by providing a high degree of automation [23–26].

Another well-known and large-scale application of RFID tags is the metropolitan public transport ticketing system which is used worldwide in numerous cities. In this case, RFID tags are normally embedded in reusable tickets (size of credit cards), which store either a seasonal pass or credit that can be used against travel [27]. According to IDTechEx, this market was responsible for the demand of 800 million RFID tags in 2016 [22].

The costs of passive RFID tags depend on the amount of memory, the packaging type and the sale volumes. However, generally speaking, more than 50 percent of the final costs are dominated by the RFIC and the antenna. The remainder are costs related to the assembly which are strongly dominated by the flip-chip step [28].

Reducing the fabrication costs of RFID tags is, of course, of a great interest for the large-scale adoption. The optimization of existing technologies is undoubtedly useful for this purpose, however, to push the market to the next level, new brilliant solutions need to be found and for doing this, why not use digital printing technologies?

1.2 State-of-the-art

Microassembly is nowadays a well-known technology to build highly integrated micro and nanosystems. The key point of this technology is the precise positioning of the microparts (e.g. integrated circuits and MEMS devices) which consists in aligning them with specific features such as edges and surfaces.

Conventional industrial microassembly lines for passive RFID tags are based on mature technologies that allow low investment risks and high-yield operations. To give an example, today the assembly yield of RFID tags is 98% and it can be more than 99% by optimizing all the processes and material parameters [29].

The continuous downsizing of microparts due to the constantly evolving market demand for reduced dimensions and costs, causes serious problems in microassembly processes. In fact, in dry environments, micro-parts are negatively affected by adhesive forces arising from electrostatic, Van der Waals and surface tension attractions. All of them are more dominant than inertial and gravity forces in the

micro-scale (scaling laws) [30]. This causes micro-parts to either stick together, creating aggregated structures or fly apart affecting the precision and the efficiency of assembly processes.

The rest of this section describes the assembly methods used nowadays in industry with a focus for RFID tags and more in general for microparts. After that, a review of the most relevant research activities is presented.

1.2.1 Industrial assembly technologies

Four interconnection techniques are available nowadays in an industrial level: wire bonding, flip chip bonding, beam lead, and TAB (Tape Automated Bonding) where the most widely used is the flip chip bonding process. A thorough discussion on these technologies can be found in [31].

The flip chip bonding process, also known as Controlled Collapse Chip Connection (C4) process, has been developed at IBM in the early 1960s with the main purpose of miniaturize electronics packages. A decade later, General Motors developed their own version for automotive electronics. Starting from the early 1990s, flip chips has been used in the high volume production for desktop PCs, TV displays, smartphones and many others including lower volume applications such as medical, cars, military and aerospace.

According to BCC Research (a market research reports and forecasts company), in 2015 the global market for the flip chip technology was $24.9 billion and it is expected to reach $41.4 billion in 2021 [32]. The smartphone sector alone is expected to have a market share of 20% [33].

In the flip chip technique, the bonding process can be performed in several ways among which the most used are i) reflow soldering and ii) thermocompression [31]. In both cases, microchips are prepared with conductive bumps deposited on the pads (or contacts) on the top side of the wafer. Before the attachment, as shown in the example of Fig.1.2, the microchip is flipped (upside down) twice in order to have the bumps, aligned and facing the underlying substrate. In a successive step, the pick-and-place robot moves and places itself in order to be aligned with respect to the contact of the antenna.

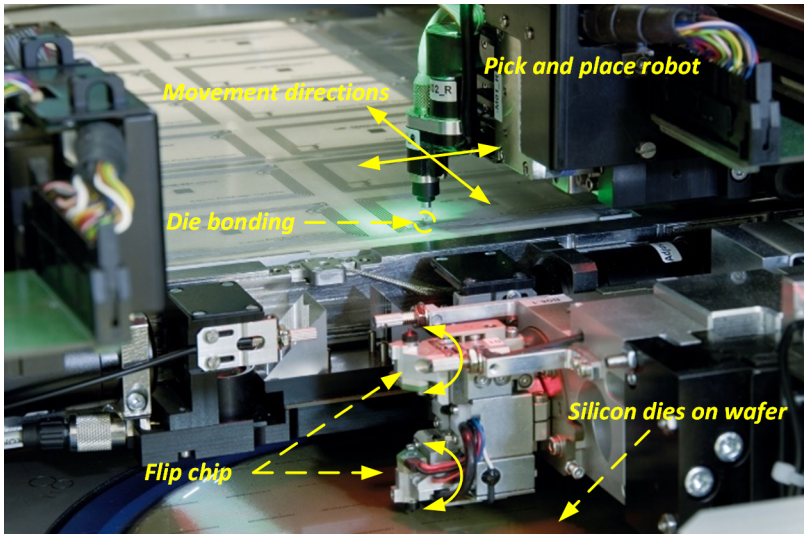


Fig. 1.2 Example of a robotic pick-and-place machines with the most relevant units. Image taken and modified from muehlbauer.de

Reflow soldering

The reflow soldering is a well characterized and highly reliable process in which lead-tin (SnPb) and more recently lead-free (Pb-Free) solder bumps act as interconnections between chips and substrates (e.g. antenna for RFID tags).

For fine pitch applications such as high-density packages (FCBGA -> Flip Chip Ball Grid Array) or ultra-small chips, the copper (Cu) pillars technology is more adapted. As shown in Fig.1.3 (a), the next-generation technology will feature micro-pillars down to 10 to 30μm.

The reflow process is usually carried out under controlled atmosphere and it consists of four main steps with specific thermal profiles: preheat, thermal soak, reflow, and cooling [34].

Each pad of the chip needs a specific preparation, called Under-Bump Metallization (UBM), which consists in the deposition of a thin layer of a material for providing i) an electrical connection from the pad of the chip to the solder bump, ii) a barrier to avoid unwanted diffusion from the bump to the silicon die and iii) a mechanical interconnection [35]. For the Cu pillars technology the preparation is more complex. In fact, as shown in Fig.1.3 (b), the Cu pillar is electroplated over a Cu seed layer with a photoresist scaffold defining the diameter of the pillar. A nickel

diffusion barrier between the Cu pillar and the solder cap is used to avoid reliability concerns.

Normally, an epoxy is employed to fill the space between the chip and the substrate (underfill) protecting the solder bumps against corrosion and mechanical stresses (thermal expansion mismatches or external loads) [34].

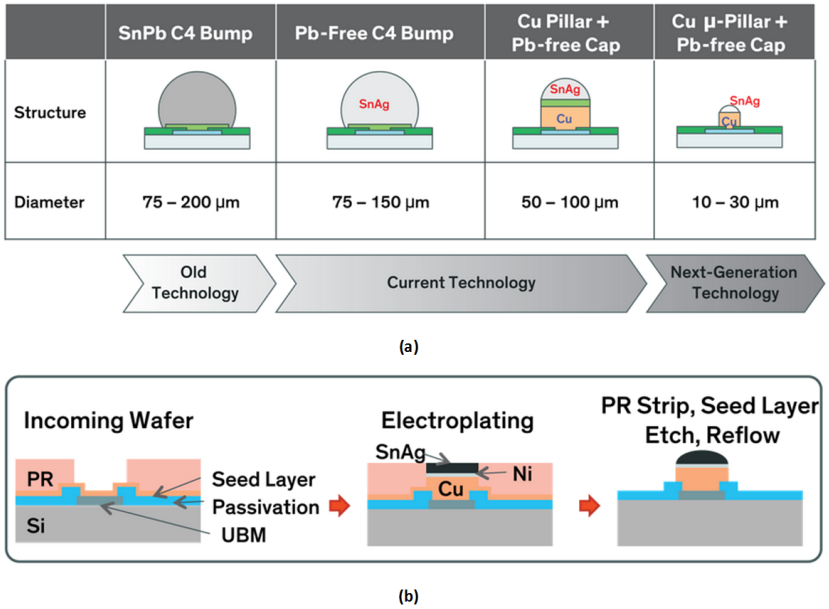


Fig. 1.3 (a) Bumping technology generations and (b) illustration of the copper pillar plating process. Images adapted from [1]

Thermocompression

The thermocompression bonding can be used in both wire and flip chip bonding processes. In the latter, solder bumps are replaced by materials with high diffusion rates and good ductile properties (e.g. copper or aluminum, but most of the time gold). Under relatively high temperatures and forces, the conductive bumps of microchips and substrates are attached together by diffusion [36].

In this technique, UBM as well as a controlled atmosphere is not required. In addition, since gold bumps are not prone to corrosion, the underfill step is not a necessary unless the chip is not protected against external mechanical loads.

Electrically conductive adhesives

Environmental concerns and substrate materials incompatible with high soldering temperatures increase the interest in electrically conductive adhesives. In fact the latter are environmentally friendly (lead-free) and they can be cured at relatively low temperatures [37].

Electrically conductive adhesives are composed of polymer binder (insulator) and conductive particles. Two types of electrically conductive adhesives exist:

- **Isotropic conductive adhesives (ICA)**: They may be used to replace solders since they have a high concentration of the particles that transform the insulating polymer matrix into a conductor. The concentration of conductive particles needs to be sufficiently high to provide good conductivity without sacrificing the mechanical properties. The critical amount of particles, at which the resistivity drops substantially, is called percolation threshold [38]. The electrical conduction is allowed in all directions giving rise to the isotropic term.

  Common volume fractions of the conductive particles are 25 to 30 percent. If the concentration is too high (above percolation threshold), the mechanical interconnection furnished by the polymer matrix may be seriously deteriorated and the resistivity does not decrease significantly [39].

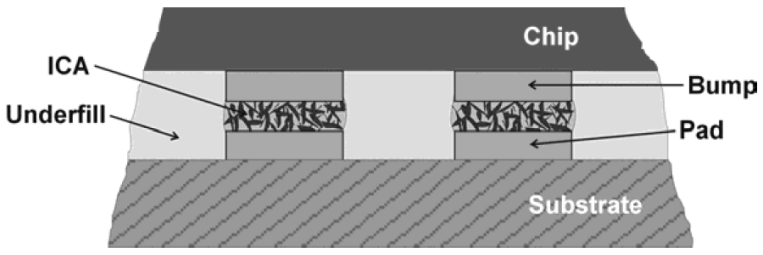


Fig. 1.4 Schematic illustration of the isotropic conductive adhesives (ICA) with flip chip and underfill. Source [2].

  As for the solder reflow method, a separate underfilling step is required for improving the reliability of the joints. A typical cross section of an ICA flip chip interconnection is shown in Fig.1.4.

- **Anisotropic conductive adhesive (ACA)**: The anisotropic conductive adhesives (films and pastes- ACA/ACF/ACP) are also made up of a polymer matrix

with dispersed conductive particles. However, in contrast to the ICA, the concentration is much lower. As shown in the sequence from a) to d) of Fig.1.5, the interconnection is established in four steps: i) the ACA is deposited over the substrate (in correspondence of the contacts), ii) low pressure and low temperature are applied simultaneously (as for the thermocompression process), iii) alignment of the chip with respect to the bonding contacts, iv) relatively high pressures and high temperatures are applied to perform the final bonding.

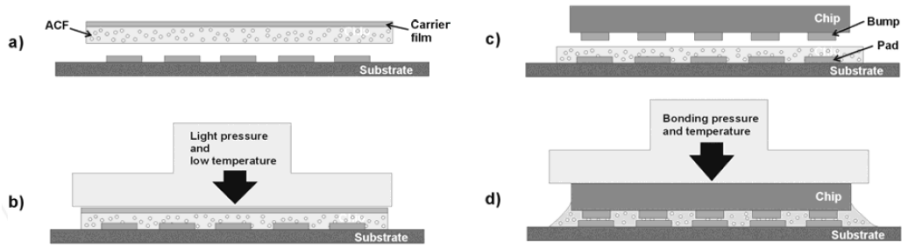


Fig. 1.5 a) Deposition of the anisotropic conductive adhesive (ACA) over the substrate. b) Pre-bonding. c) Chip alignment with respect to the bonding contacts. d) Final bonding. Adapted from [2].

In this case, a separate underfilling step is not required since the adhesive matrix is transformed into a liquid due to the applied heat [40]. In fact, the excess adhesive flows from the joints and fill the spaces around the contacts. This forms a mechanical connection between chips and substrates.

As shown in Fig.1.5 d), the electrical conduction is limited to the z-direction which is insured by the deformed and trapped conductive particles between the contacts of the chip and the substrate (bonding contact). In x-y directions the insulating property is maintained.

Flip chip assembly system

To give concrete examples, the high-end FCM 10000 (from Mühlbauer High Tech International) flip chip assembly system can assemble up to 9'500 UPH (Units Per Hour) achieving a placement accuracy of ± 20 μm with an assembly yield of 99.7%. The Datacon 8800 Chameo advanced system (from BE Semiconductor) can assemble 7'000 UPH but achieving a better placement accuracy of ± 3 μm. The FC 300R (from Smart Equipment Technology SET) pushes the placement accuracy down to ± 0.5 μm but at the expense of a throughput of only approximately 250 UPH.

Summary

The full assembly process of passive RFID tags can be summarized by the following steps:

1. the wafer is "bumped" to leave conductive bumps on the top of each pad,
2. the wafer is diced (separate each chip on the wafer),
3. the bumped dies are loaded onto a reel or waffle pack for assembly,
4. the micro-assembly is done using a pick-and-place and a flip-chip robot that positions the bumped dies directly on the package substrate (with the antenna),
5. the chip and the antenna are attached (cured or soldered) together to complete the interconnection. This step is also known as die bonding and it can be further described, for instance, as shown Fig.1.5,
6. and depending on the attachment method, an under-fill epoxy layer is normally used between the die and the substrate for protection the chip and the interconnection.

1.2.2 Self-assembly processes for microparts

A considerable effort has been undertaken to reduce the overall costs and increase the assembly rate of micro-components, in fact, several technologies can be found in literature. The most promising techniques are based on the self-assembly. The latter is a *"process by which disordered parts build an ordered structure through only local interaction."* [41]. In order to allow this process to take place at the micro-scale, local interactions have to be designed for energy minimization in order to drive micro-components toward desired locations. Several technologies have been proposed based on mechanical shape recognition in combination with gravity or vibration [42–44], electrostatic force [45], magnetic force [46, 47] and surface tension forces (also called capillary self-alignment) combined with robotic micro-manipulations, also called hybrid processes [48–55, 4, 7, 56, 57]. A recent review summarizes these technologies [58].

An interesting example has been reported by S-C. Park *et al*. in [3, 59] where they demonstrate the first implementation of a fluidic self-assembly machine, based

on the surface tension directed self-assembly. This implementation is capable of placing 15'000 UPH with an assembly yield exceeding 99% and using a 2.5 cm wide assembly region. As shown in Fig.1.6 (A) and (B), the microparts fall down due to the gravity in a funnel-like container filled with a liquid (e.g. water). The latter is continuously flowing through a circulation circuit and the same happen for the unbounded microparts in a parallel circuit driven by a pump-jet. The microparts adhere to the molten solder over each receptor site and precise positioning is performed by the minimization of the surface-free energy of the liquid solder eventually leading to an electrical connection.

The authors claimed that using this technology it would be possible to scale up the fabrication rate to 150'000 UPH simply by using a 25 cm web. This would be almost 20 times faster than the FCM 10000 flip chip assembly system.

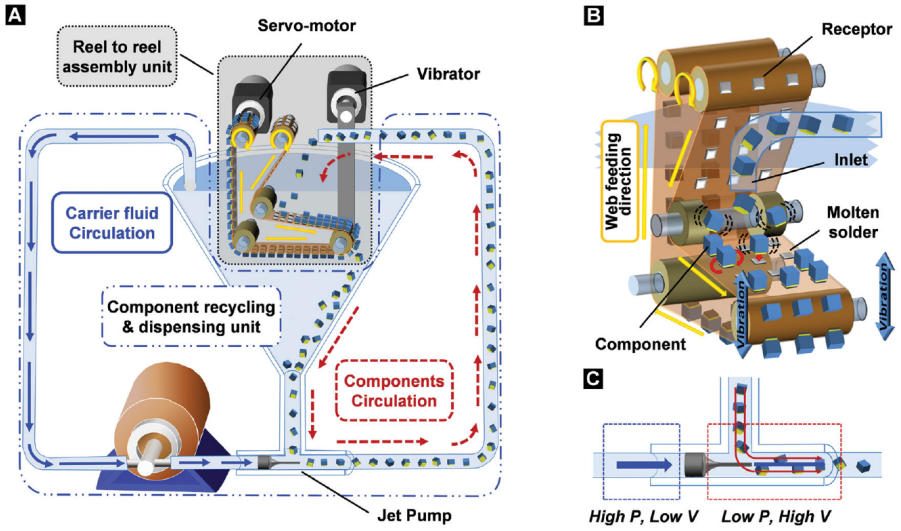


Fig. 1.6 (A) Automated RTR fluidic self-assembly scheme showing the transportation of the components towards the empty sites (receptors) using a liquid flow and gravity while the web is continuously advancing. (B) The self-assembly process takes place on the basis of surface tension directed self-assembly using molten-solder-bump. (C) Detail of the jet pump used to achieve recirculation of the chips. Source [3]. © 2014 IEEE.

Other examples of hybrid self-assembly processes where the chips (or more in general microparts) are deposited over a droplet of liquid as shown in Fig.1.7 a, are reported in [60–64, 54]. All these processes can be commonly characterized by a spontaneous self-alignment in which: i) three forces act on the chip keeping it in contact with the liquid droplet, ii) the evaporation of the liquid droplet eventually

leads to contact of the chip on the receptor site as shown in the sequence b, c and d of Fig.1.7.

The three forces just mentioned can be described as follows:

- F_s: surface tension force along the triple line, that is the solid-liquid-vapor interface between the chip and the liquid. This force can be expressed as $F_s = \gamma\, l$ where l is the lateral size of the chip, and γ is the surface tension of the liquid.
- F_l: surface tension force attributed to the Laplace pressure. It can be determined as $F_l = \Delta P\, A$, where ΔP is the pressure difference due to the surface tension of the liquid-air interface, and A is the surface of the chip.
- G: gravitational force. The latter is almost negligible at the micro-scale. In fact F_s and F_l may overstep G by a factor of 10^2-10^5 or more depending on the size of the micro-parts [65].

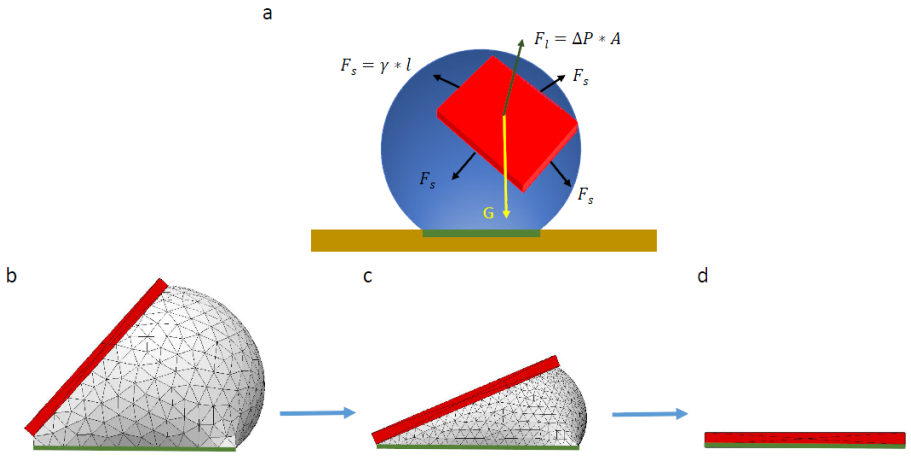


Fig. 1.7 (a) Forces acting on the chip floating on a droplet of liquid. (b) The chip is tilted and floating on a droplet. (c) The droplet gradually evaporates driving the chip toward the final position. (d) Alignment between the chip and the receptor size (or contact pad). Source [4].

The capillary self-alignment (CSA) has always been reported for cases in which the initial overlap between microparts and receptor sites was sufficient to allow the self-assembly to take place. Bo Chang *et al*. [5] interestingly demonstrate the feasibility of a capillary self-transport technique where microparts are initially

placed outside the high wettability region as shown in Fig.1.8 (a). Using a rain of microdroplets in correspondence of the assembly region, a meniscus is formed between the micropart and the receptor site. The surface energy minimization of this meniscus drives the micropart towards its final position as shown in the sequence from (b) to (f) of Fig.1.8. They demonstrated that using a droplet with a volume of 6 nl, the allowed initial distance of microparts from receptor sizes was 100 μm and felt down to 25 μm with 1 nl of volume. This shows the volume as a potential source of failure in the CSA process.

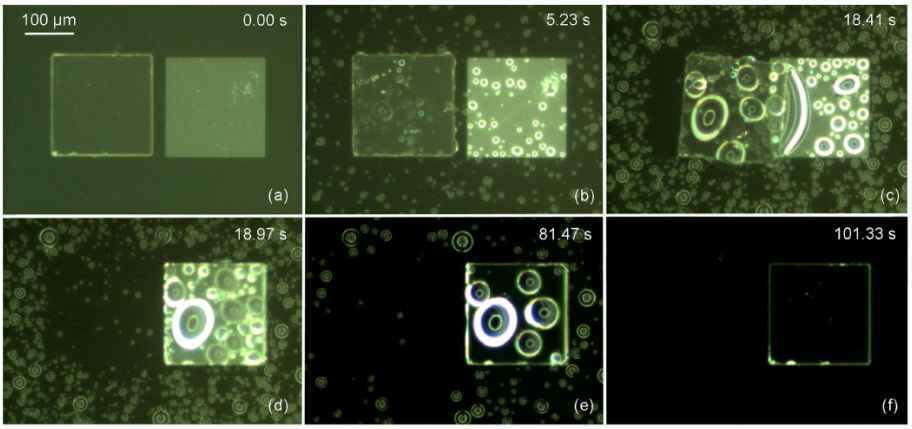


Fig. 1.8 Self-transport of a SU-8 chip with dimensions of 200 μm x 200 μm x 30 μm. (a) Chip placed at 25 μm from the receptor site. (b) Microscopic rain is delivered. (c) A liquid meniscus is formed between the receptor site and the chip. (d) The chip aligns with the receptor site due to the capillary force; (e) droplets evaporate; (f) Dry surface with chip aligned with respect to the receptor site. Source [5].

If the wetting contrast between the receptor site and its surroundings is too small, the self-alignment most likely cannot take place due to i) the friction force on the surroundings of the receptor site increases and ii) the energy curve becomes flat leading to low restoring forces. For this reason, a large wetting contrast is a key factor for performing a precise self-alignment [5].

However, a large wetting contrast alone is not sufficient for preventing the CSA to fail. If the contact angle of the surrounding substrate is too low (e.g. 100$\mathring{A}$) despite a large wetting contrast, the restoring force is counterbalanced by the friction force to which the micropart is subjected on the surrounding substrate. This is a major concern since most of liquid adhesives used in CSA processes present low contact angle on most surfaces because of their low surface tensions.

To cope this challenging situation, Ali Shah *et al*. [6] developed a low wettability nano-structured black silicon substrate coated with fluoropolymer and a high wettability gold surface acting as receptor site. They demonstrate a CSA process of microchips with water and a UV-curing adhesive.

The mechanisms of the self-alignment have been analyzed in [66]. In order to define the accuracy of the alignment after evaporation, they interestingly defined an initial stable configuration in which the chip is aligned with the receptor site at a distance depending on the volume of the droplet. Subsequently, they introduced a position perturbation destabilizing the system. The accuracy has been defined checking if the chip returned to its stable position, that is, aligned with respect to the receptor site.

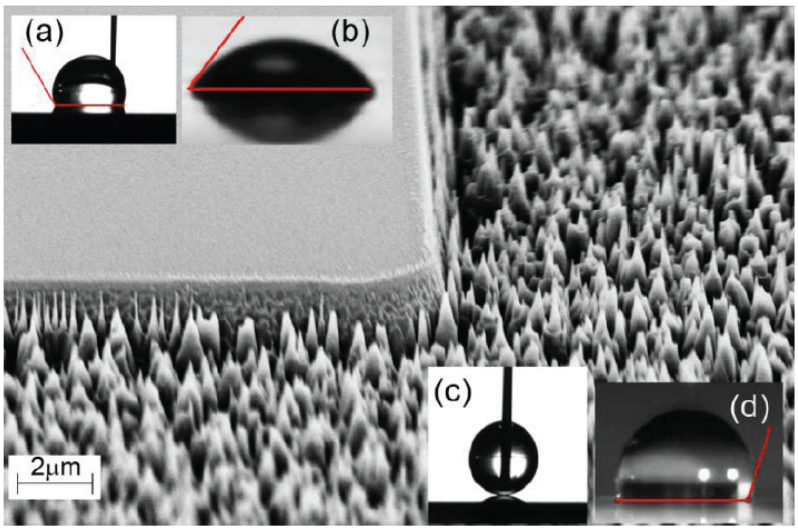


Fig. 1.9 SEM image showing the gold patterned high wettability region with contact angles for both water and adhesive droplets. The same for the low wettability porous fluoropolymer coated black silicon substrate. Source [6]. © 2013 IEEE.

As shown in Fig.1.10, four perturbation modes have been analyzed: lift, twist, shift and tilt. For the first three modes, misalignments are compensated by capillary forces, in fact the chip returned to its initial position. In the other hand, the tilt mode has been defined as slightly unstable because it turns out that the final alignment depends on the weight of the chip and on the volume of the droplet. The latter point is of a great importance since it can push the liquid to overflows on the low wettability region, finally leading to misalignment after evaporation.

Local chemical and geometric defects present on the high wettability surface are potential causes of misalignment. In fact, if the defects are sufficiently important in size and number, they may be responsible for modified contact angles, deviation of the motion of droplets or a complete arrest of them. The latter phenomenon is called pinning [67].

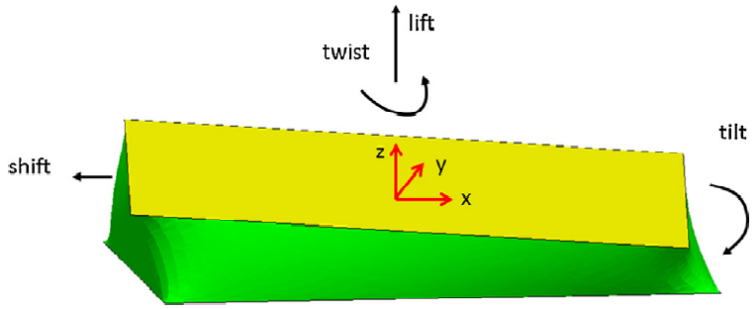


Fig. 1.10 The four different perturbation modes of the chip: lift, twist, shift and tilt. Source [7].

For very small microparts (in the range of 50 to 200μm), random agitation is normally sufficient to cope with this instability of the tilt mode. However, it is not effective for larger microparts. In fact, the authors of [68], proposed mechanical precautions such as stops and hinges for guiding microparts during the assembly process. Nevertheless, these techniques are complicated and not always compatible with the requirements of the microelectronics (e.g. RFID).

Berthier *et al*. [7] proposed an elegant way to stabilize the tilt mode by incorporating specific lyophilic (wetting) bands on the substrate. As shown in Fig.1.11, these bands are perpendicular to the fixed pad. If the wetting contrast is sufficient, the droplet does not overflow out of the bands and the unstable tilt mode turns into a stable mode. The effectiveness of this approach depends on the weight of the chips (not too large to succeed) and on system parameters, such as the width of the bands and the value of the contact angles.

Industrial scale self-assembly

An interesting industrial scale shape driven Fluidic Self-Assembly (FSA) process has been proposed by Yeh and Smith [42]. In this process, a slurry of special shaped RFID chips are rinsed over a substrate with corresponding 3D holes (351) as shown in Fig.1.12 (a). The chip is made up of a silicon block (355) combined with the

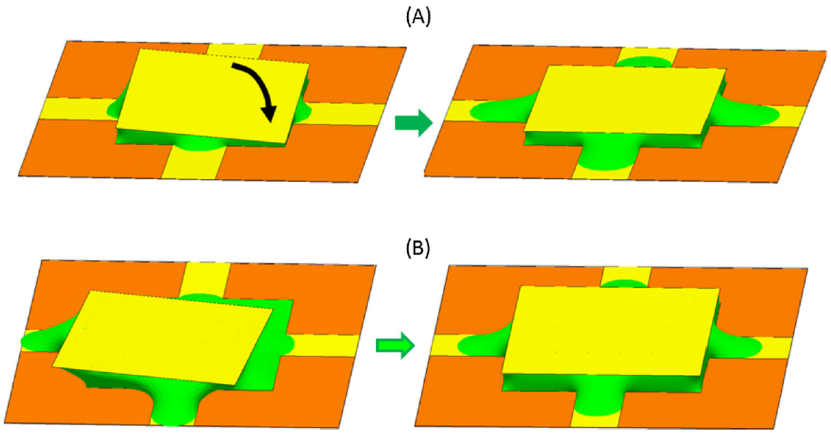


Fig. 1.11 (A) Square chip realigned after a tilt perturbation. (B) Square chip realigned after shift, twist and tilt motion. Chip dimensions 5x5mm, chip weight 0.07g. Source [7].

CMOS circuitry (353). As shown in the sequence from (b) to (d) of Fig.1.12, once the holes are filled, an adhesive layer (356) is applied with a doctor blade for i) mechanically fixing the chips and ii) take away the ones that are misaligned. After that, contact lines (357) are realized using a standard lithography technology.

The company Alien Technologies has several patents some of which are based on the above-mentioned FSA process [69–73, 8] with which they were able to produce 11'000 UPH with a fabrication yield of 99.99% and an alignment accuracy of $\pm$ 1μm.

Researchers at the Palo Alto Research Center (PARC), developed a xerographic printing-based process, called MicroAssembly Printer, in which they use a dynamic electric field-driven assembly of microparts. The latter are assembled into well-defined locations and orientations. This process allows high volume productions of complex heterogeneous systems exhibiting a huge potential as a parallel and high performance digital manufacturing tool [9].

In comparison with standard xerographic printing systems where the input is the ink (e.g. colored toner particles) and the output is an image, using the MicroAssembly Printer, the ink is made up of electronics chips (e.g. amplifiers, memory, sensors, etc.) and the output image is a functional electronic system.

As shown in Fig.1.13, the process of PARC can be explained in four fundamental steps: i) encoding microparts with charge patterns. This step can be interpreted as the ink preparation. ii) Microparts are assembled (image development) to pre-defined

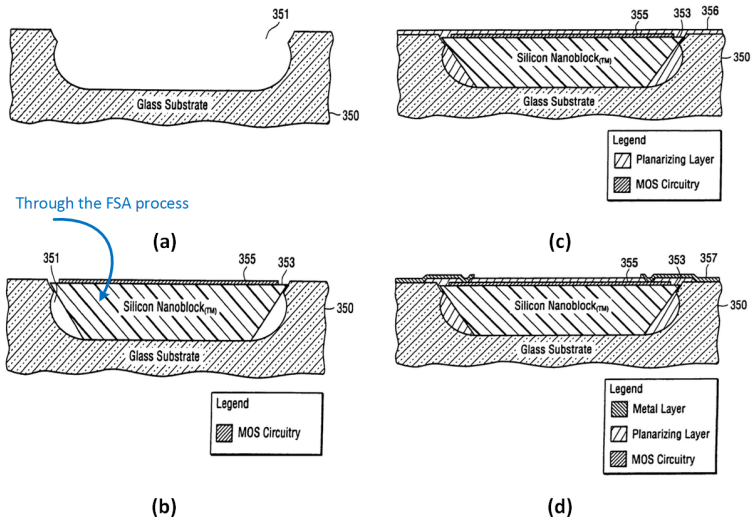


Fig. 1.12 Extract of the patent US 7531218 B2 explaining the FSA process of Alien Technologies. (a) hole initially empty. (b) Hole filled with a RFID chip through FSA process. (c) Application of the planarizing layer. (d) Deposition of the conductive interconnections. Images taken and modified from [8].

locations using a dynamic electric field-driven assembly process. iii) The microparts are transferred to the substrate through an intermediate roller. iv) Microparts are interconnected using photolithography or inkjet printing [9].

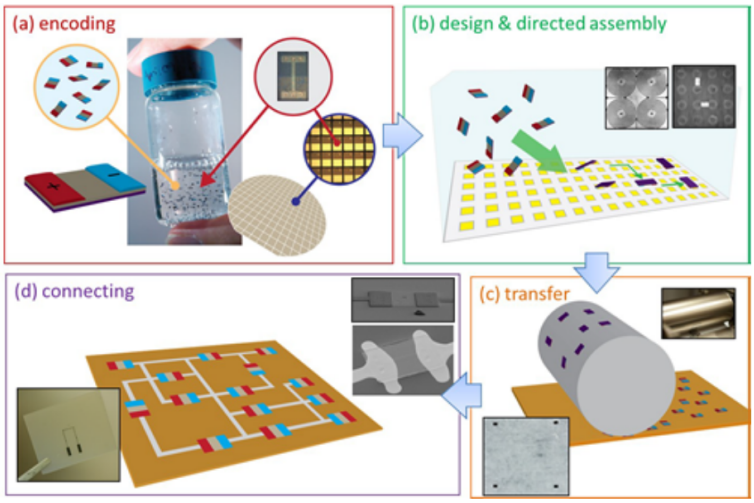


Fig. 1.13 MicroAssembly Printer process step: (a) encoding microparts, ii) microparts assembly (image development), iii) microparts transfer and iv) microparts interconnections. Source [9].

1.2.3 RFIC with stacked structure

Hitachi, a well-known company operating in several business segments, one of which is the Electronic Systems & Equipment, designs the smallest RFID chips in the world. One of them, called "$\mu - Chip$" was successfully used for the 2005 World Exposition in Aichi, Japan. In fact, all the passes incorporated a tiny chip containing a unique 128 bits identification number which was reflected back to the scanner of entrance gates [74].

The smallest chip (0.05x0.05mm^2 and 5um thick) has been officially called "Powder LSI chip" where "LSI" stands for Large Scale Integrated. It has been designed with a Silicon-On Insulator (SOI) 90nm CMOS technology followed by a series of post-CMOS processes. The peculiarity of the chip is that it shows two contact surfaces, one on the top of the chip and the second instead of the bulk [75, 10, 76]. Such a technology allows producing ultra-small chips connected to the antenna using a sandwich structure. It also allows to completely isolate the sensible circuitry from the RF input signal thanks to the insulating oxide. According to Usami [77], the use of this SOI technology is of a great advantage for preventing latch-up conditions. In fact, latch-up protection structures such as the two- or three-way guard rings of conventional devices are not necessary.

The post-CMOS fabrication steps are shown in Fig.1.14 and summarized in the following way:

- **Step 1**: The first "top" contact electrode is formed at the surface of the wafer by means of a gold plating or a sputtering technique.
- **Step 2**: The wafer is placed upside-down and the thickness of the Si substrate is reduced using the backgrinding technique followed by back-dry or wet etching. The buried oxide layer is used as an etch stop.
- **Step 3**: The second "back" contact electrode is formed on the surface of step 2. The connection of the second electrode to the front-end electronics is made by making a via hole through the buried oxide layer. In addition, narrow patterns are etched on this new surface in order to be used as an etching mask during the separation step.
- **Step 4**: The chip separation is accomplished by dry etching.

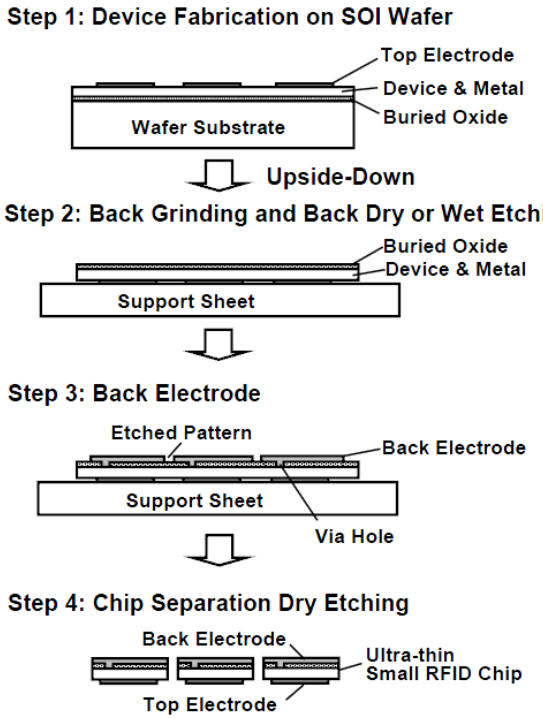


Fig. 1.14 Ultra-thin powder LSI chip fabrication process and sandwich-like structure (cross section). Source [10]. © 2006 IEEE.

The powder LSI chip has been designed with a minimum capability. It contains a rectifier circuit to generate a constant voltage from the received carrier frequency at 2.45GHz. This voltage is used for powering up the Read Only Memory (ROM) and its control logic. It also contains a clock recovering circuit for synchronizing with the reader. Anti-collision functions have not been implemented, allowing Hitachi to drastically reduce the size of the chip.

A similar approach has been implemented by Pachler *et al*. [11] in which the RFIC uses a large metal surface on the top of the chip as shown in Fig.1.15 (b). Nevertheless, in contrast to the Hitachi case in which a direct contact between the antenna and the large metal surface is used, the OC3 uses a non-resonant capacitive coupling mechanism working at multiple frequencies (HF and UHF bands). In fact, as shown in Fig.1.15 (d), the $1mm^2$ top metal surface acts as an electrode of a capacitor. The second electrode of the OC3 tag is realized by the silicon substrate and connected to the ground.

In Fig.1.15 (c) is shown the analog front-end of the OC3 which implements a voltage rectifier circuit with diode-connected transistors and threshold voltage

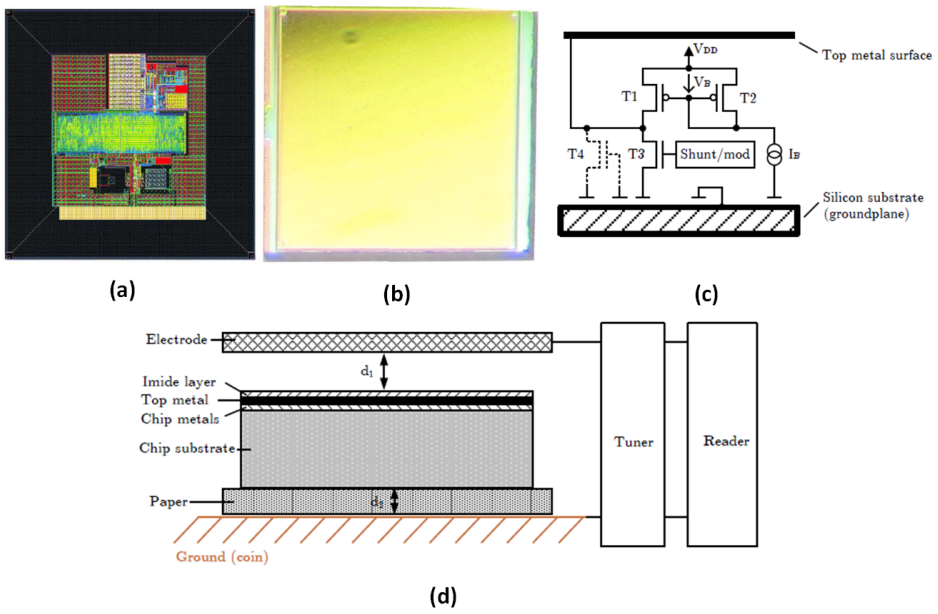


Fig. 1.15 Layout (a), microphotograph (b) and analog front-end schematic (c) of the one square millimeter OC3 RFID tag. Capacitive coupling and system overview (d). Adapted from [11]. © 2014 IEEE.

cancellation ($T1$ and $T2$). Transistor $T3$ is used both for the rectification path as well as for the load modulation. According to the authors, the capacitive coupling was successfully tested up to $100\mu m$ in air. For improving the reading distance, a booster antenna coil capacitively coupled to the OC3 has been used reaching a distance of 30 cm with an injected power of 1W in the reader side.

1.2.4 Hybrid assembly processes

Hitachi introduces [78] an automated technique which combines the fast and relatively precise robotic micro-handling and the advantages of the sandwich structure of $\mu - chips$. They develop the so-called handling ultra-small $\mu - chips$ apparatus (UH) which consists of four main parts: i) a reservoir unit which contains $\mu - chips$ suspended into liquid solutions such as water, organic solvent and aqueous surfactants. ii) A micropipette manipulator, controlled by robotic actuators, is operated by an aspirator (for capturing $\mu - chips$) and compressed air (releasing it). iii) A Charged Coupled Device (CCD) camera for detecting whether the chip is actually on the micropipette or not. iv) An antenna take-up roller over which thin antenna

films are placed. The authors claimed to be able to manipulate 100 chips in 44 min (26.4 s / chip) with a mounting pitch of 0.7 mm.

Based on this method, Hitachi, in a successive work [12], proposes a new process, shown in Fig.1.16 and called Liquid Droplet Self-aligned Positioning (LDSA). This process can be explained as it follows: i) a micro-liter liquid droplet (e.g. water) is deposited onto a hydrophilic / hydrophobic patterned surface on the antenna film. ii) A $\mu - chips$ is released onto the droplet which is several times larger than the chip. The latter is kept floating on the liquid / air interface of the droplet as already explained and depicted in Fig.1.7.

The positioning of the chip is performed by the evaporation of the droplet that gradually shrinks eventually leading to a precise self-alignment of the $\mu - chips$ with respect to the hydrophilic surface domain (an electrode).

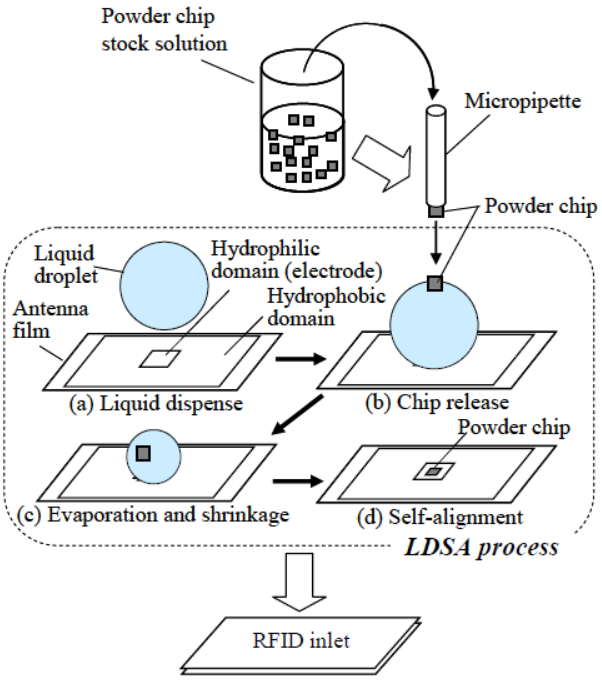


Fig. 1.16 Schematic illustration of RFID inlet fabrication flow using the LDSA process. Source [12]. © 2011 IEEE.

1.3 Motivation and project goals

The self-assembly processes mentioned in the section 1.2.2 proved their competitiveness against the traditional fabrication processes, in terms of efficiency and production rate, nevertheless most of them have been demonstrated in favorable cases. In fact, they have been applied in cases in which the density of the receptor sites are very high and the spacing between them and the size of the components are of the same magnitude [48]. This, of course, does not reflect the real case of an assembly of RFID tags where the size of the antenna coil can be several centimeters and the size of one RFID die is only few hundreds of micrometers. Such a difference in scale can reduce the efficiency of assembly processes and to achieve a good filling rate, it requires either a huge number of components or a very long time.

To cope with these limitations and deal with standard RFID tags, hybrid techniques which combine the two major branches of micro-handling have been developed. As reported in the section 1.2.2, these techniques used the high speed and low-cost robotic micro-manipulation for coarse positioning of chips near the binding sites and droplet self-alignment for fine positioning. However, these techniques still suffer from the serial behavior of the micropipette handling.

The sandwich-structured chips introduced above are clearly an elegant way with which the precise positioning onto the antenna terminals becomes a less critical aspect. This is possible because there is only one connection on each surface. Moreover, the chip orientation can be arbitrary so long as one of the two contacts faces the landing pad eliminating any concern about positioning. Another advantage of having a two-surface connection is that each connection area is designed to be as large as the chip surface to reduce connection resistance. These approach will lead to an increased fabrication rate as well as to a simplified assembly process.

Nevertheless, the 90*nm* SOI technology of Hitachi is not low cost and the post-CMOS processes used for the fabrication of the second electrode are relatively complicated and they add extra costs, therefore, even if these chips allow an easier assembly process in comparison to traditional pick-and-place machines, the whole process will be less cost effective.

Based on these considerations, the goal of this thesis is to present a concept study of a new fabrication process enabling the production of ultra low-cost RFID tags using an inkjet-like printing approach.

1.4 Thesis organization

This thesis is organized as it follows:

Chapter 2 gives the theoretical background and the fundamental concept of RFID system with a specific emphasis on the modeling of each element of an RFID tag and an in-depth analysis of the inductive coupling.

Chapter 3 introduces a novel concept of an inkjet-based fabrication process for producing ultra-low cost and high frequency RFID tags. The peculiarity of this process is the use of a dielectric ink droplet containing a specifically designed radio frequency integrated circuit (RFIC). A theoretical background is given in order to understand the ink - substrate interaction and the modeling behind droplets formation over specifically treated surfaces.

Chapter 4 is dedicated to an in-depth analysis of the capacitive coupling, created between the antenna coil of the RFID tag and the RFIC encapsulated inside the dielectric droplet over the substrate. A complete model will be developed and analyzed in order to determine RF performances, read range and compliance with ISO/IEC standards.

Chapter 5 describes a first high voltage implementation of an unconventional structured RFIC. In this chapter a new design methodology is developed for optimizing the voltage rectifier circuit based on the parabolic approximation of the voltage rectifier input current.

Chapter 6 concludes the presented research along with discussion on future work.

Chapter 2

Fundamental concept of RFID systems

2.1 Introduction

RFID systems have been assigned, during technology's early days, to the ISM (Industrial Scientific and Medical) frequency range in which, the most intensely used and known frequencies are 13.56MHz and 2.45GHz. The worldwide availability of these frequencies and the possibility to use tags and readers internationally without modifications, play a major role in the global adoption of RFID systems [79].

These operating frequencies are normally categorized into four bands as shown in Table.2.1 which summarizes the main characteristics as well as the associated standards of RFID systems [15].

The choice of a frequency band leads to specific physical characteristics of antennas and RF performances. For a fixed current of the reader antenna, the low frequency (e.g. 125kHz) require large coils with a relatively high number of turns (e.g. from 10 to 100 turns) whereas the high frequency (e.g. 13.56MHz), need smaller coils and a reduced number of turns. At ultra high frequency and microwave, tags normally use dipole antennas. The latter have dimensions which are typically about half the wavelength [79].

Table 2.1 RFID frequency characteristics, application and standard. Adapted from [15]

Band	**LF** (Low Frequency)	**HF** (High Frequency)	**UHF** (Ultra High Frequency)	**Microwave**
Frequency range	30 - 300KHz	3 - 30MHz	300MHz - 3GHz	2 - 30GHz
Specific RFID range	125 - 134KHz	13.56MHz	433MHz (UHF_1) 860 - 960MHz (UHF_2)	2.45GHz
Read range	< 0.5m	$\leq$ 1.5m	$\leq$ 100m (UHF_1) $\approx$ 0.5 - 5m (UHF_2)	$\leq$ 10m
Data transfer rate	< 1kbit/s	$\approx$ 25kbit/s	$\approx$ 30kbit/s	$\leq$ 100kbit/s
Characteristics	Short range Low data range Penetrate water but not metal	Mid range Reasonable data rate Penetrate water but not metal	Long range High data rate Cannot penetrate water or metal	Long range High data rate Cannot penetrate water or metal
Standard	ISO/IEC 11784/5 ISO/IEC 14223 ISO/IEC 18000-2 ISO/IEC 24631	ISO/IEC 14443 ISO/IEC 15693 ISO/IEC 18000-3 ISO/IEC 10373 ISO/IEC 18092 (NFC) ISO/IEC 13157 EPC class 1	ISO/IEC 18000-6/7 EPC Class 0/1 EPC GEN II	ISO/IEC 18000-4

The frequency band also affects the interaction of electromagnetic fields with materials such as metallic objects, body tissues and water. This point will be further investigated later in this chapter.

The signal detection accuracy, which is related to the frequency modulation scheme, and communication protocols also depend on the frequency band. These latter points are not further described since out of the scope of this thesis. However, a thorough discussion on these topics can be found in [79].

RFID systems can also be categorized based on the energy delivery methods to the transponder. Depending on whether a dedicated power source is present or not, RFID tags are classified in three groups: i) passive , ii) semi-passive and iii) active.

Passive tags harvest the required energy by converting the input RF signal (of any frequency bands) to a DC voltage which is further stabilized by a regulator and delivered to the rest of the circuitry.

The input information is extracted from the RF signal by performing an envelope detection and to send information back to the reader, they modulate the impedance of the antenna with respect to the data bits. This is performed by switching terminals of the antenna between open and short circuit. The reader is able to detect the impedance modulation through the mutual inductance (see next section).

The absence of a battery and a simple front-end RF circuitry support the low cost implementation. However, both simplicity and low cost come at the expense of a short read range (e.g. from 2 to 20m) and limited computational capabilities.

Semi-passive tags use batteries only to power the circuitry and the backscattering method (UHF) or the load modulation method (LF and HF) to retransmitting data back to the reader. The embedded power source allows the integration of some specialized RF front-end blocks (e.g. RF amplifiers) that leads to a longer read range (e.g. from 10 to 100m). Nevertheless, these type of tags have higher manufacturing cost compared to passive tags.

Active tags use a battery to power the entire tag circuitry. These type of tags can be considered as complete radios able to realize advanced modulation schemes and operate over long read range (e.g. 100m and more) operating in the UHF or Microwave frequency bands. In comparison to passive tags, the active counterparts have higher manufacturing cost, larger size and maintenance requirements.

2.2 Inductive link

Wireless power transfer has a broad meaning, in fact the term "wireless" indicates the absence of any wired connection. Following this definition, not only electric connection can be taken into account but also for example acoustic links. In this work, wireless power transfer refers to electric power and the nature of this transmission is electromagnetic. An electromagnetic wave is constituted of a magnetic field and an electric field coupled together. This relationship has been mathematically formulated, by James Clerk Maxwell, into the Maxwell's equations [80].

Depending on the wavelength λ, the size of the antenna and the distance between the reader and the tag, the transmission can be defined to be nonradiative and acting in the near-field region ($r < \lambda/2\pi$) or, to be radiating and acting in the far field ($r >> \lambda/2\pi$).

In the far field, the electric field is predominant and reduces when the distance increases according to $1/r$. This type of transmission will not be discussed further since out of the scope of this thesis.

In the near field, the electric field is used for creating a capacitive coupling, for example between two closely coupled parallel plates. The magnetic field instead can be used to establish an inductive coupling between two coils of different shape and size. Both fields reduce when the distance increase according to $1/r^3$.

2.2.1 Magnetic field strength H and magnetic induction B

Moving charges, such as electrons in wires, produce magnetic fields in the surrounding space. The magnitude of these fields is described by the magnetic field strength $\vec{H}$, independently of the material properties of the space.

The magnetic field strength is usually introduced using the example shown in Fig.2.1 (a) which consists in a single turn coil where $\vec{H}$ can be calculated at any target point using the Biot-Savart law:

$$\vec{H} = \frac{I}{4\,\pi} \int\limits_{wire} \frac{d\vec{l} \times \hat{\mathbf{r}}}{r^2} \tag{2.1}$$

In this expression, I is the current flowing into the coil, $d\vec{l}$ is an arc length and $\hat{\mathbf{r}}$ is the unit vector representing the direction of a point P in space relative to any point on the mean radius of the coil. The latter, in Cartesian coordinates, is:

$$\vec{r}' = a\big[cos(\theta)\hat{\mathbf{i}} + sin(\theta)\hat{\mathbf{j}}\big] \tag{2.2}$$

where a is the mean radius of the coil.

The relative unit vector $\hat{\mathbf{r}}$ can be expressed by:

$$\hat{\mathbf{r}} = \frac{\vec{r}' - \vec{r}_P}{|\vec{r}' - \vec{r}_P|} = \frac{\big[a\,cos(\theta) - x_P\big]\hat{\mathbf{i}} + \big[a\,sin(\theta) - y_P\big]\hat{\mathbf{j}} - z_P\hat{\mathbf{k}}}{\sqrt{\big[a\,cos(\theta) - x_P\big]^2 + \big[a\,sin(\theta) - y_P\big]^2 + (-z_P)^2}} \tag{2.3}$$

The arc length $d\vec{l}$ can be expressed, using a first order approximation, in the following way:

$$d\vec{l} = \frac{d\vec{r}'}{d\theta}d\theta = a\,d\theta\,\big[-sin(\theta)\hat{\mathbf{i}} + cos(\theta)\hat{\mathbf{j}}\big] \tag{2.4}$$

The cross product of Eq.2.1 can be simplified using Eq.2.4 and the numerator of 2.3 as it follows:

$$\begin{aligned} d\vec{l} \times \big(\vec{r}_P - \vec{r}'\big) &= a\,d\theta\,\big[-sin(\theta)\hat{\mathbf{i}} + cos(\theta)\hat{\mathbf{j}}\big] \times \Big\{\big[a\,cos(\theta) - x_P\big]\hat{\mathbf{i}} \\ &\quad + \big[a\,sin(\theta) - y_P\big]\hat{\mathbf{j}} - z_P\,\hat{\mathbf{k}}\Big\} \\ &= \Big\{\big[z_P\,cos(\theta)\big]\hat{\mathbf{i}} + \big[z_P\,sin(\theta)\big]\hat{\mathbf{j}} + \big[a - x_P\,cos(\theta) \\ &\quad - y_P\,sin(\theta)\big]\hat{\mathbf{k}}\Big\}\,a\,d\theta \end{aligned} \tag{2.5}$$

Using the results here above, the magnetic field strength at any point P is:

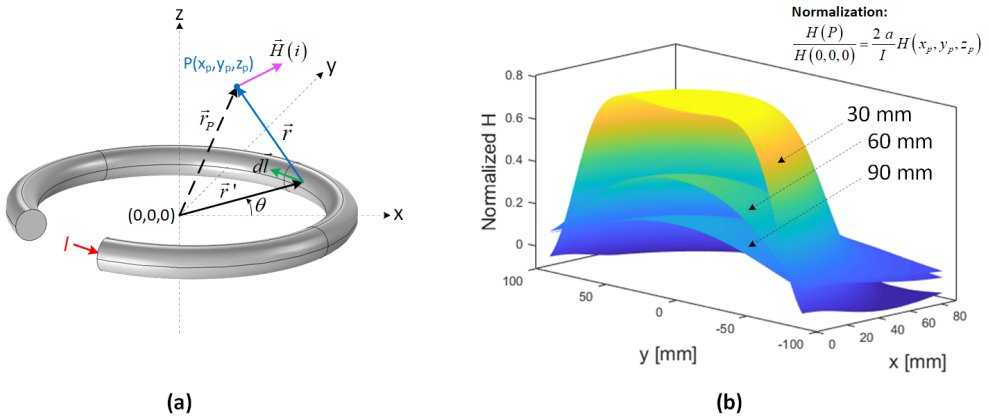


Fig. 2.1 (a) Single turn antenna coil with geometric parameters for magnetic field analysis using the Biot-Savart law. (b) Magnetic field strength H around the antenna coil for three axial distances.

$$\vec{H} = \frac{I\,a}{4\,\pi} \int_0^{2\pi} \frac{\left[z_P\,cos(\theta)\right]\hat{\mathbf{i}} + \left[z_P\,sin(\theta)\right]\hat{\mathbf{j}} + \left[a - x_P\,cos(\theta) - y_P\,sin(\theta)\right]\hat{\mathbf{k}}}{\left\{\left[a\cdot cos(\theta) - x_P\right]^2 + \left[a\cdot sin(\theta) - y_P\right]^2 + (-z_P)^2\right\}^{3/2}} d\theta \quad (2.6)$$

A numerical integration of this equation has been reported in fig.2.1 (b) where it can be observed that the magnetic field strength is higher for axial and proximity positions. At $z_P = 30\ mm$, the shape of $\vec{H}$ inside the coil is almost uniform whereas it rapidly reduces outside the diameter of the coil.

The total number of magnetic field lines passing through a surface S is defined as the magnetic flux ϕ which can be determined using the magnetic flux density $\vec{B}$ in the following way:

$$\phi = \iint_S \vec{B}\,d\vec{S} \quad (2.7)$$

The magnetic field strength $\vec{H}$ and magnetic flux density $\vec{B}$ are related through the material equation:

$$\vec{B} = \mu_0\,\mu_r\,\vec{H} \quad (2.8)$$

where μ_0 is the permeability of free space ($4\,\pi\,\cdot\,10^{-7}$ H / m) and μ_r is the relative permeability of the surrounding space.

2.2.2 Self-inductance

The inductance is defined as the magnetic flux ϕ divided by the current i flowing through that inductance. This is shown in Fig.2.2 (a) and can be mathematically defined as it follows:

$$L = \frac{\phi}{I} = \frac{\iint_S \vec{B}\, d\vec{S}}{I} = \frac{\iint_S \mu_0\, \mu_r\, \vec{H}\, d\vec{S}}{I} \tag{2.9}$$

where $d\vec{S}$ is an infinitesimal area vector pointing towards the normal direction of the plane defined by the area.

This expression cannot always be directly used due to the complexity of the geometry. In fact, most of the time, numerical approximations (e.g. using Comsol Multiphysics) or measurements are performed.

In the numerical case, very often, the surface integral is transformed into a line integral thanks to both the magnetic vector potential $\vec{A}$:

$$\vec{B} = \nabla \times \vec{A} \tag{2.10}$$

and the Stokes' theorem. The latter states that a surface integral of the curl of a vector field is equal the closed line integral over the boundary of the surface, therefore the inductance can be rewritten in the following way:

$$L = \frac{\iint_S \nabla \times \vec{A}\, d\vec{S}}{I} = \frac{\oint_{\partial S} \vec{A}\, d\vec{l}}{I} \tag{2.11}$$

2.2.3 Mutual inductance M and coupling coefficient k

Let's consider the example shown in Fig.2.2 (b) in which an inductance L_2 is located in proximity of L_1. In this situation, part of the magnetic flux density $\vec{B}_1$ pass through

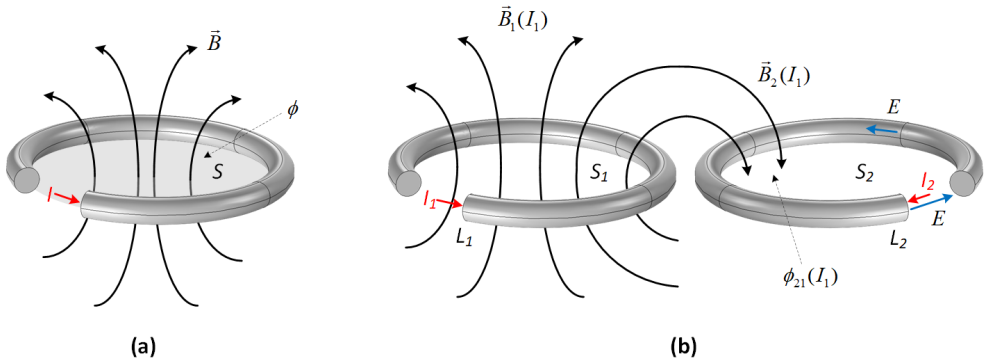


Fig. 2.2 (a) Magnetic flux and magnetic flux density for a single turn inductance. (b) Inductive coupling between two single turn inductances.

the area of the second inductance leading to ϕ_{12}. Following that, the two inductances are coupled together through ϕ_{21} which depends on the geometric configuration of L_1 and L_2 (in terms of dimensions and distance).

At this point, the mutual inductance can be defined rewriting Eq.2.9 in the following way:

$$M_{21} = \frac{\phi_{21}(I_1)}{I_1} = \frac{\iint_{S_2} \vec{B}_2(I_1)\, d\vec{S}_2}{I_1} \tag{2.12}$$

Based on the same principle, there is also a mutual inductance M_{12}. In this case, the current I_2 determines the magnetic flux ϕ_{12} re-coupling together the two inductances leading to the following relationship:

$$M = M_{21} = M_{12} \tag{2.13}$$

In RFID systems, the mutual inductance is used to quantitatively describe the coupling between the reader and the transponder by means of the magnetic field, whereas the coupling coefficient k, which is a geometric parameter, is used to make a qualitative description of the inductive coupling independently on electrical characteristics and geometric dimensions of the reader - transponder system:

$$k = \frac{M}{\sqrt{L_1\, L_2}} \tag{2.14}$$

where k varies between two extreme values: $0 \geq k \leq 1$. If $k = 0$, both L_1 and L_2 are completely decoupled due to a very large distance between them. if $k = 1$, the two inductances are perfectly coupled and they are subject to the same magnetic flux. Between these two extreme values, the coupling depends on the geometric configuration of L_1 and L_2.

2.2.4 Induction's law and Maxwell–Faraday equation

Considering again the inductive coupling of Fig.2.2 (b), it can be stated that any change in the magnetic flux ϕ_{21}, induced by the current of L_1, generates electric fields E in any infinitesimal boundary path $d\vec{l}$ of L_2.

All these electric fields together (electric field circulation) form a closed loop and since the material of L_2 is conductive, an electromotive force u_{2i} is provided and drives free charge carriers (electric current) around the conductive loop.

This can be mathematically stated using the integral form of the Maxwell–Faraday equation:

$$V_{2i} = \oint_{C2} \vec{E}\, d\vec{l} = -\frac{\partial}{\partial t} \iint_{S_2} \vec{B}_2\, d\vec{S}_2 = -\frac{\partial \phi_{21}}{\partial t} \tag{2.15}$$

where S_2 is the open surface representing the loop, C_2 is the boundary of this surface and the negative sign indicates that u_{2i} opposes the change in magnetic flux (Lenz's law), that is, it tends to maintain the existing ϕ_{21}.

Using again the Stokes's theorem on the left side of Eq.2.15, the latter can be rewritten in the following way:

$$\iint_{S_2} \nabla \times \vec{E}\, d\vec{S}_2 = -\iint_{S_2} \frac{\partial \vec{B}_2}{\partial t}\, d\vec{S}_2 \tag{2.16}$$

which simplifies and becomes the differential version of the Maxwell–Faraday equation:

$$\nabla \times \vec{E} = -\frac{\partial \vec{B}_2}{\partial t} = j\, \omega\, \vec{B}_2 \tag{2.17}$$

Combining equations 2.12 and 2.17 and considering sinusoidal currents and linear and time-invariant media, the induced voltage u_{2i} can be expressed in the following way:

$$V_{2i} \;=\; j\,\omega\,M\,I_1 \;=\; j\,\omega\,k\,\sqrt{L_1\,L_2}\,I_1 \tag{2.18}$$

where $\omega = 2\,\pi\,f$ is the angular frequency of the current I_1. This shows that the voltage induced on L_2 is proportional to the operating frequency.

2.3 Planar antenna coil modeling

In the high frequency range (e.g. 13.56MHz), antenna coils of RFID tags are mainly planar multi-turn inductances with rectangular cross-section as shown in Fig.2.3 (a) and (b). In order to allow interoperability, layout characteristics of inductances are specified by ISO/IEC standards such as the 14443 for proximity cards [81].

Rectangular shape

For a rectangular antenna coil, the total inductance can be calculated using a low-frequency approximation (without proximity effects) in which the self-inductance L_0 is summed to mutual inductances M_+ (positive) and M_- (negative) due to the coupling between adjacent segments [82]:

$$\begin{aligned} L &= L_0 + M_+ - M_- \\ &= \sum_{i=1}^{N_{seg}} L_{0_i} + \sum_{j=1}^{N_{seg}(N_{turns}-1)} M_{+_j} - \sum_{k=1}^{N_{seg}N_{turns}} M_{-_k} \end{aligned} \tag{2.19}$$

where N_{seg} is the total number of segments, N_{turns} is the number turns which constitute the antenna coil and L_{0_i} is the self-inductance of each segment. The latter can be calculated as it follows:

$$L_{0_i} \;=\; 2\,l_i\left[ln\Big(\frac{2\,l_i}{w\,+\,t}\Big) \;+\; 0.50049 \;+\; \frac{w\,+\,t}{3\,l_i}\right] \tag{2.20}$$

For each segment, w is the width, t is the thickness and l_i is the length as shown in Fig.2.3 (d). These three dimensional parameters are in *cm* and the self-inductance is in nH.

The mutual inductance between two segments is positive when currents are in the same direction. Consequently, the negative mutual inductance takes place when currents are in opposite directions. In the latter case, magnetic fields counteract each other. As shown in Fig.2.3 (d), the mutual inductance between two segments depends on both the length of each segment and the geometric mean distance between them. If the lengths are the same, as for example between segment m and n, the value of $M_{m,n}$ (which is positive in this case) can be calculated by:

$$M_{m,n} \;=\; 2\, l_1\, F(l_1,\, d_{mn}) \tag{2.21}$$

where d is the mean distance between adjacent segment (in this case between segments m and n) and $F(l,d)$ is the mutual inductance parameter which is calculated as it follows:

$$F(l,\, d) \;=\; ln\left(\frac{l}{d} + \sqrt{1 + \left(\frac{l}{d}\right)^2}\right) - \sqrt{1 + \left(\frac{l}{d}\right)^2} + \frac{d}{l} \tag{2.22}$$

On the other hand, if the lengths are different, as it happens in multi-turns coils and shown in Fig.2.3 (d) between segment m and o, the mutual inductance (which is negative in this case) is calculated by:

$$M_{m,\,o} \;=\; \frac{1}{2}\Big(M_m \;+\; M_o \;-\; M_p \;-\; M_q\Big) \tag{2.23}$$

where:

$$\begin{aligned} M_m &= 2\, l_1\, F(l_1,\, d_{mo}) \\ M_o &= 2\, l_2\, F(l_2,\, d_{mo}) \\ M_p &= 2\, l_p\, F(l_p,\, d_{mo}) \\ M_q &= 2\, l_q\, F(l_q,\, d_{mo}) \end{aligned} \tag{2.24}$$

As for the case of the self-inductance, the dimensional parameters are in *cm* and the mutual inductances are in *nH*.

Circular shape

As for the rectangular case, antenna coils with circular shape can be approximated using low frequency analytical expressions. As reported in [83], the accuracy of such expressions is lower than the rectangular case and it reduces as the number of turns increase.

In this thesis, the reader will be considered as a single turn coil as specified in the ISO/IEC 10373 standard [84]. Following that, the more accurate analytical expression found in literature is [85]:

$$L = \mu_0 \, a \left[ln\left(\frac{8\,a}{d}\right) - 3 \right] N^2 \tag{2.25}$$

where a is the radius of the circular antenna coil and d is the equivalent radius of the wire as shown in Fig.2.3 (e).

Series resistances and inter-winding capacitances

The frequency response of an antenna coil strongly depends on its physical layout. In fact, as shown in Fig.2.3 (a), for each segment, the total inductance, the inter-winding capacitance and the series resistance need to be taken into account using distributed models. The latter can be used to determine the self-resonant frequency (SRF) at which the reactive part of the impedance cancel out. The antenna coil change its behavior from inductive to capacitive based on whether is working below or above the SRF.

For a given working frequency, the lumped model of Fig.2.3 (f) is normally used and depending on the dimensional characteristics of the antenna coil, the parallel capacitor is sometimes not taken into account or merged with external tuning capacitors.

The real part of the impedance is the resistance which can be defined, for DC currents, by:

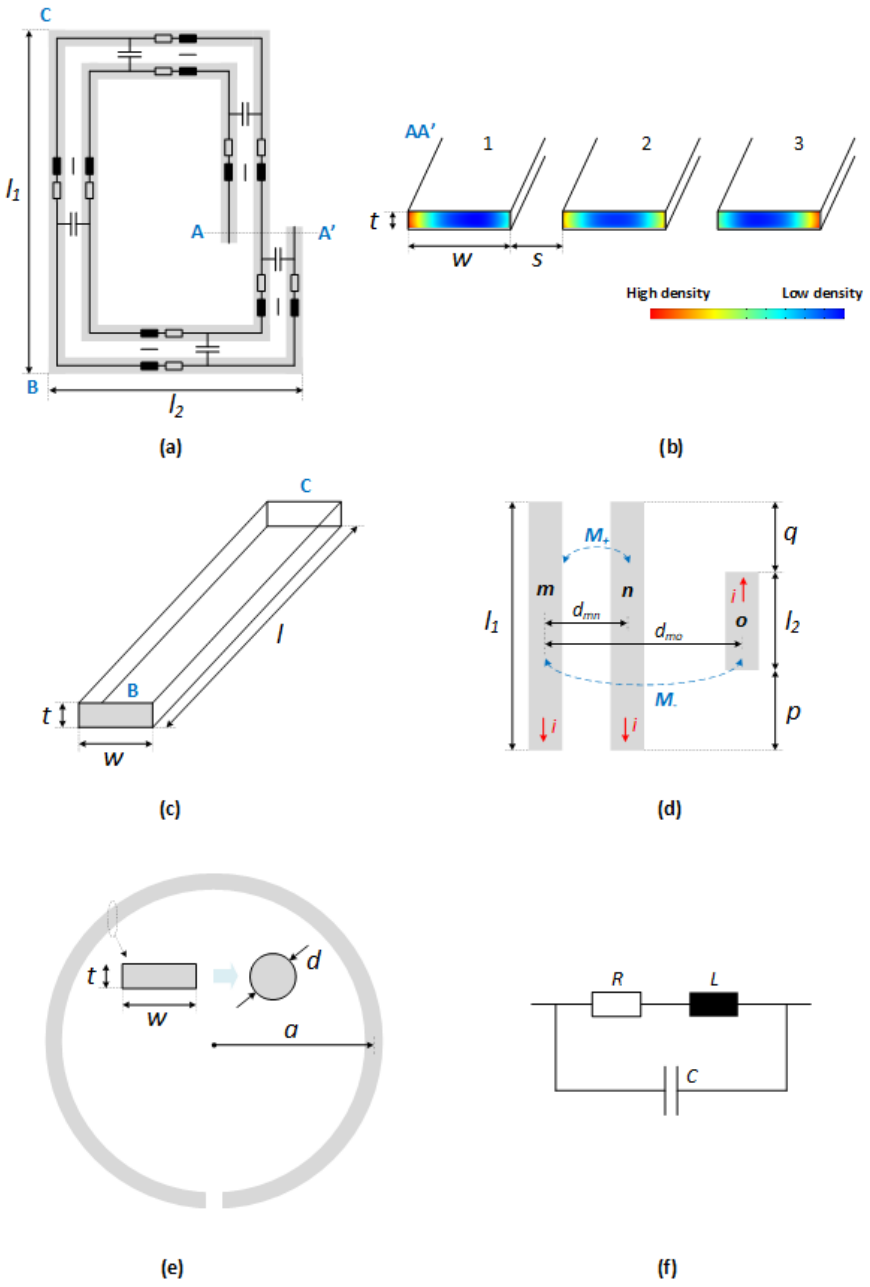


Fig. 2.3 (a) Distributed model of a rectangular antenna coil. (b) Skin and proximity effect on the current distribution in adjacent segments. (c) Dimensional characteristic of a conductive segment. (d) Positive and negative mutual inductance between segments in multi-turns coils. (e) Single turn circular antenna coil. (f) Lamped equivalent model at a specific frequency.

$$R_{DC} = \frac{l}{\sigma S} \tag{2.26}$$

where l is the conductor length, S is the cross-sectional area and σ the conductivity of the material.

As shown in Fig.2.3 (b), for AC currents at high frequency, the skin effect influences the effective area of the cross section. In fact, the current density decreases in the middle and increases near the edge leading to a higher resistance. The skin depth of a single wire with a circular cross-section can be defined by:

$$\delta = \sqrt{\frac{2}{\omega \mu \sigma}} \tag{2.27}$$

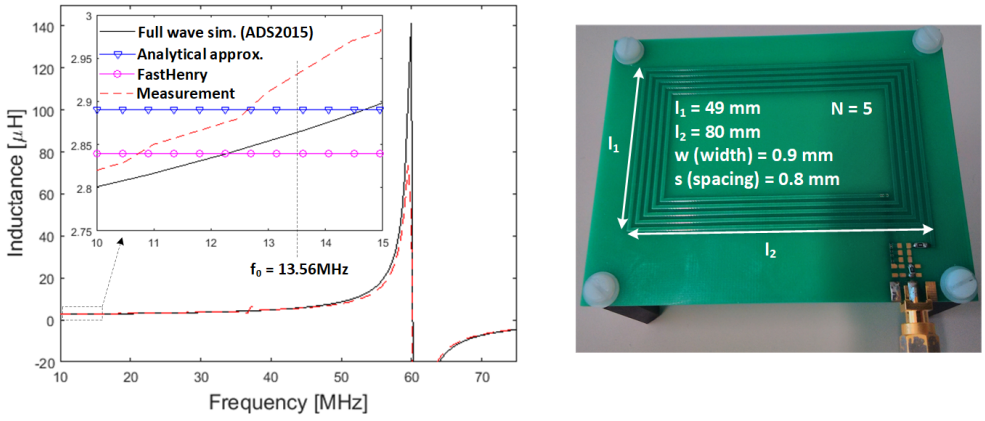
where $\mu = \mu_0 \cdot \mu_r$ is the permeability of the conductor material. In order to compute the effective AC resistance, it can be assumed that the entire current flows in the conductor skin whose thickness is determined by the skin depth.

$$\begin{aligned} R_{AC} &= \frac{l}{\sigma S_{active}} \\ &\approx \frac{l}{2a}\sqrt{\frac{f \mu}{\pi \sigma}} \\ &\approx R_{DC}\frac{a}{2\delta} \end{aligned} \tag{2.28}$$

where a is the radius of the wire.

The expression reported in Eq.2.28 does not apply for complex shape and conductors with rectangular cross-sections. In this case, current distributions are further influenced by proximity effects, caused by the magnetic field of the adjacent windings. In fact, by closely looking at Fig.2.3 (b), it can be seen that current densities are different based on whether the conductor is symmetrically surrounded by adjacent segments or is placed in the innermost or outermost turn of the antenna coil.

Approximations of series resistances can be computed using numerical tools such as FastHenry [86–88] or Comsol Multiphysics.



(a) (b)

Fig. 2.4 (a) Comparison of rectangular antenna coil inductance values between low frequency approximation, FastHenry, Advanced Design system full-wave simulation and measurements. (b) Test HF antenna coil with dimension complying with the ISO/IEC 14443 standard.

If the total inductance and the associated parasitic resistance of the antenna are the only characteristics of interest, in general quasi-static magnetic field (QSMF) approximations are sufficient (e.g. as described in [89]). However, if the parasitic inter-winding capacitance is required in order to define the frequency response of the antenna coil, full wave [90, 91] or hybrid [92] analyses are normally carried out. The latter takes into account electric and magnetic characteristics of the antenna within one simulation.

In this thesis, total inductances have been first approximated using the above reported expressions and subsequently verified using FastHenry and a full-wave analysis (using Advanced Design System). Finally, measurements have been carried out for validating the model.

As shown in Fig.2.4 (a), the analytical approximation (low frequency value) and the numerical solution of FastHenry differ of less than 2 %, whereas the difference between measurement values and the full wave analysis is less than 4 %.

The SRF occurs at approximately 60 MHz which is well above the intended working frequency, that is 13.56 MHz.

2.4 Electrical model of passive RFID tags

RFID systems are normally modeled using the equivalent electrical circuit presented in Fig.2.5 (b). The antenna coil of the reader can be driven either by a constant current or constant voltage and to deliver maximum power to the antenna, a matching network is usually introduced between the source and the antenna. This point will be further investigated in chapter 3.

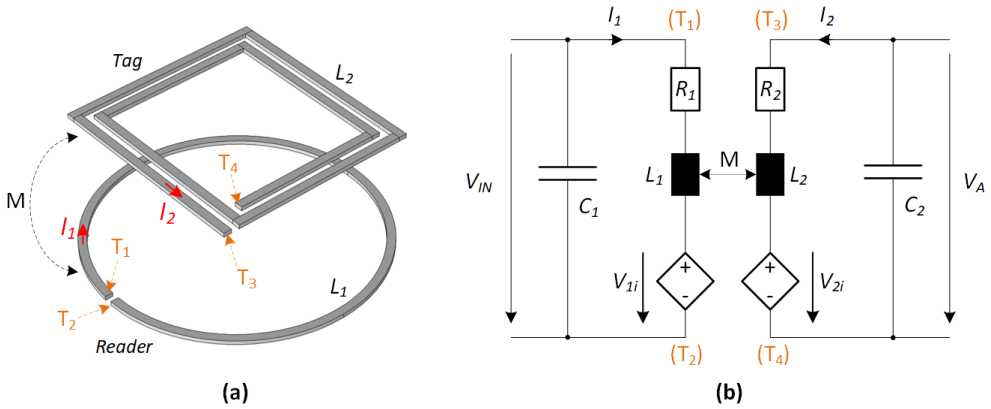


Fig. 2.5 (a) Inductive coupling of a reader-tag system with (b) simplified electrical model.

The RFIC impedance is modeled by a resistor R_L, which essentially represents the average power consumption of the chip, and a capacitor C_L. To significantly improve the power efficiency and the read/write range between the reader and the tag, the antenna of the latter is tuned to the resonance frequency (well below the SRF) of the reader by means of a parallel or a series capacitor C_2.

2.4.1 Inductive coupling and parallel resonance

In the analysis here following, the inter-winding capacitances have been left out of the model since they will be either merged into the resonant capacitor (parallel configuration) or neglected introducing an acceptable error (series configuration).

The parallel resonance is made up of a capacitor C_2 in parallel with the equivalent RFIC impedance as shown in Fig.2.6. For a series RLC circuit, the value of C_2 is calculated using the following equation:

$$C_2 = \frac{1}{(2\,\pi\,f_0)^2\,L_2} = \frac{1}{\omega_0^2\,L_2} \tag{2.29}$$

where f_0 is the carrier frequency of the reader. However, in the parallel case, both C_2 and C_L need to be merged together forming a new capacitor C_{PAR}.

$$C_{PAR} = C_2 + C_L \tag{2.30}$$

Successively, the parallel combination of C_{PAR} and R_L need to be converted in a series combination. This is carried out using the following two equations [93]:

$$C_{ser} = \frac{1 + (\omega\,R_L\,C_{PAR})^2}{\omega^2\,R_L^2\,C_{PAR}} \tag{2.31}$$

$$R_{ser} = \frac{R_L}{1 + (\omega\,R_L\,C_{PAR})^2} \tag{2.32}$$

Substitution of C_2 in Eq.2.29 with 2.31 yields the condition for the resonance of the transponder:

$$\omega_0 = \sqrt{\frac{1}{C_{PAR}\,L_2} - \frac{1}{C_{PAR}^2\,R_L^2}} \tag{2.33}$$

Using Eq.2.30, the value of C_2 can be expressed for a given resonant frequency:

$$C_2 = \frac{1}{2\,\omega_0^2\,L_2}\left(1 + \sqrt{1 - \frac{4\,\omega_0^2\,L_2^2}{R_L^2}}\right) - C_L \tag{2.34}$$

The voltage V_L available on the input of the RFIC can be expressed using Eq.2.18 and considering the total tag impedance:

$$
\begin{aligned}
V_A = V_L &= \frac{V_{2i}\, X_{C_{PAR}} \,//\, R_L}{X_{L2} + R_2 + (X_{C_{PAR}} \,//\, R_L)} \\
&= \frac{j\,\omega\, M\, I_1 \,\frac{1}{C_{PAR}\, L_2}}{(j\,\omega)^2 + j\,\omega\,(\frac{1}{R_L\, C_{PAR}} + \frac{R_2}{L2}) + (\frac{R_2}{R_L} + 1)\frac{1}{C_{PAR}\, L_2}}
\end{aligned}
\tag{2.35}
$$

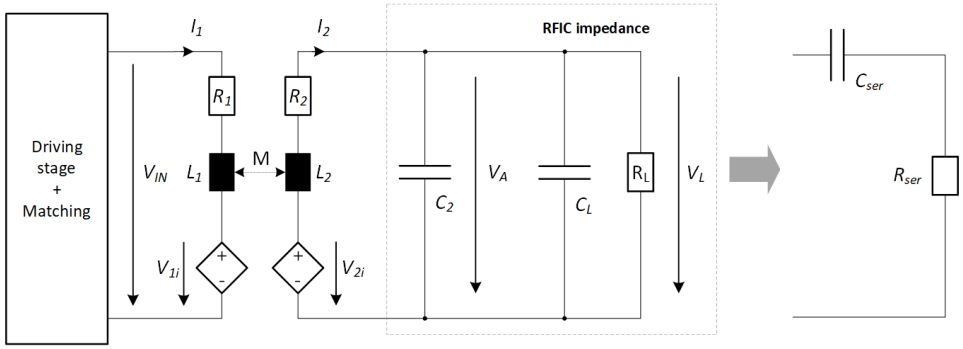


Fig. 2.6 Complete model with reader driving stage, reader antenna coil, transponder antenna coil with parallel resonance and RFIC impedance.

The quality factor of the transponder Q_{2L} affects the maximum achievable bit rate during communication. Indeed, the bandwidth needs to be at least capable of carrying all the frequency contained into the spectrum of the signal which modulates the carrier.

The value of Q_{2L} can be determined considering the circuit as a series combination of the real inductor (composed by L_2 and R_2) and the real equivalent capacitor (composed by C_{ser} and R_{ser}). This means that Q_{2L} is calculated considering the individual quality factor of the unloaded antenna coil Q_2 and of the equivalent capacitor Q_{ser}:

$$
Q_2 = \frac{X_{L2}}{R_2} \tag{2.36}
$$

$$Q_{ser} = \frac{X_{ser}}{R_{ser}} \tag{2.37}$$

$$Q_{2L} = \frac{1}{\frac{1}{Q_2} + \frac{1}{Q_{ser}}} = \frac{1}{\frac{R_2}{\omega_0 L_2} + \frac{1}{\omega_0 C_{PAR} R_L}} \tag{2.38}$$

In Fig.2.7 is clearly shown the voltage step-up of u_L due to the parallel resonance of L_2 and C_{PAR} at f_0 = 13.56MHz according to Eq.2.35. The value of the inductance L_2 has been defined as the mean value between the full-wave simulation and the measurements reported in Fig.2.4 (a).

The solid line shows the resonance for $R_2 = 1\Omega$ which is a very low value reachable only with an electro-deposition step during the antenna coil fabrication. In this case, the thickness of the coil can be up to 100 - 150μm. The small dashed line shows the resonance for $R_2 = 40\Omega$ which is a reasonable value for printed coils (without any extra plating process) considering skin and proximity effects. In this case, the thickness of the coil is between 5 and 10μm. The large dashed line shows the inducing voltage on the antenna coil u_{2i} according to Eq.2.18.

The self-resonant frequency has not been taken into account since as reported in Fig.2.4 (a) the latter is well above the working frequency.

Equivalent transponder impedance and transmitted power

Up to this point the inductively coupled system has been primarily analyzed from the point of view of the transponder. In order to study in more detail the interaction between the transponder and the reader, the equivalent transponder impedance Z_{EQ}, seen by the reader side, is introduced [79, 93].

The V_{IN} - I_1 relationship in the reader side is:

$$V_{IN} = I_1(R_1 + j\omega L_1 + Z_{EQ}) \tag{2.39}$$

where Z_{EQ} is expressed by:

$$Z_{EQ} = \frac{V_{1i}}{I_1} = \frac{j\,\omega\,M\,I_2}{I_1} = \frac{(\omega\,M)^2}{j\,\omega\,L_2 + \dfrac{1}{j\,\omega\,C_{ser}} + R_2 + R_{ser}} \tag{2.40}$$

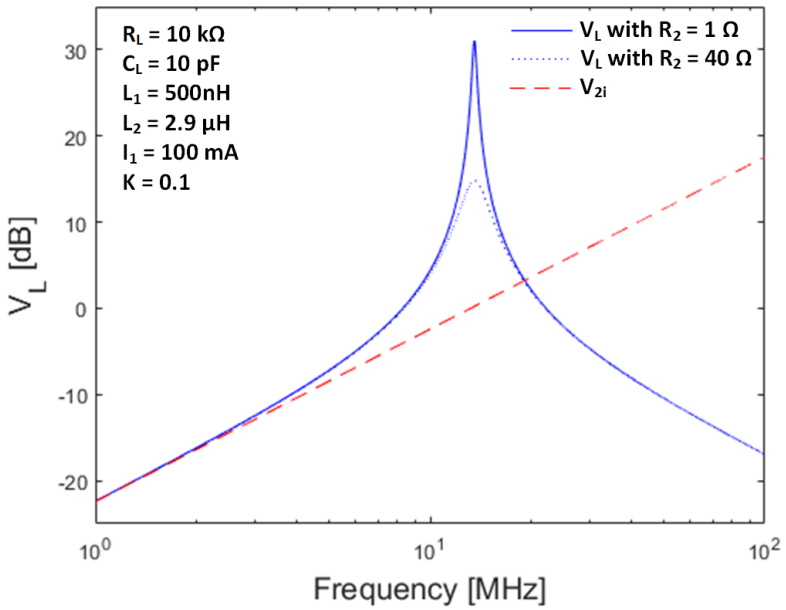


Fig. 2.7 Plot of the induced voltage on the antenna coil according to equation 2.18 (large dashed lines). Voltage step-up due to the parallel resonance of L_2 and C_{PAR} according to equation 2.35 for $R_2 = 1\Omega$ (solid line) and $R_2 = 40\Omega$ (small dashed lines).

For better understanding the maximum power transfer, it is interesting to consider the real part of the equivalent transponder impedance Z_{EQ}. The latter can be extracted using the process of rationalization leading to the following equation:

$$Re\left(Z_{EQ}\right) = \frac{M^2\,\omega^4\,C_{ser}^2\,(R_2 + R_{ser})}{\omega^2\,C_{ser}^2\,(R_2 + R_{ser})^2 + (\omega^2\,C_{ser}\,L_2 - 1)^2} \tag{2.41}$$

The tag is assumed to be tuned into resonance, therefore, using Eq.2.33 into Eq.2.31 and 2.32, both can be rewritten and become:

$$C_{ser,\omega_0} = \frac{C_{PAR}^2\,R_L^2}{C_{PAR}\,R_L^2 - L_2} \tag{2.42}$$

$$R_{ser,\omega_0} = \frac{L_2}{C_{PAR}\, R_L} \tag{2.43}$$

The use of Eq.2.33, 2.42 and 2.43 into Eq.2.41 leads to the following equivalent resistance:

$$R_{EQ,\omega_0} = \frac{M^2\,(C_{PAR}\, R_L^2\, -\, L_2)}{C_{PAR}\, L_2\, R_L\,(L_2\, +\, C_{PAR}\, R_2\, R_L)} \tag{2.44}$$

Finally, the amount of power transmitted to the transponder and dissipated into R_L is:

$$P_{RL,\omega_0} = \frac{I_1^2\, M^2\,(C_{PAR}\, R_L^2\, -\, L_2)}{2\, C_{PAR}\, R_L\,(L_2\, +\, C_{PAR}\, R_2\, R_L)^2} \tag{2.45}$$

where I_1 is the pick value of the current in the reader side.

Maximum power transfer can be achieved by matching the resistor R_2 with the equivalent resistor R_{ser}. However, R_2 depends on the geometric characteristics of the antenna coil as well as for the value of L_2. This means that the matching of R_2 is somehow counter-compensated by the change of L_2. Furthermore, skin and proximity effects between adjacent traces cause R_2 not to increase linearly with the number of turns N. The optimization of R_2 will lead to maximum power transfer only if the above-mentioned consideration are neglected as explained in [93] and [89].

Link efficiency

A maximum power transfer does not necessarily correspond to a maximum link efficiency. In fact as explained in [93], to calculate the overall efficiency η of the inductive link, one need to calculate two distinct efficiency η_1 and η_2. The first one is the power dissipated into the transponder circuit, by means of the equivalent

resistance R_{EQ} divided by the total power dissipated:

$$\begin{aligned} \eta_{1,\omega_0} &= \frac{R_{EQ}}{R_{EQ} + R_1} \\ &= \frac{M^2 \left(C_{PAR} R_L^2 - L_2\right)}{M^2 \left(C_{PAR} R_L^2 - L_2\right) + R_1 \left(C_{PAR} L_2^2 R_L + C_{PAR}^2 L_2 R_2 R_L^2\right)} \end{aligned} \tag{2.46}$$

The second one is the power dissipated into R_{ser} divided by the total power dissipated in the transponder side only:

$$\eta_{2,\omega_0} = \frac{R_{ser}}{R_{ser} + R_2} = \frac{L_2}{L_2 + C_{PAR} R_2 R_L} \tag{2.47}$$

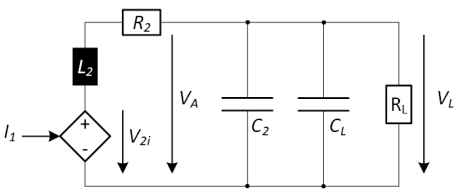
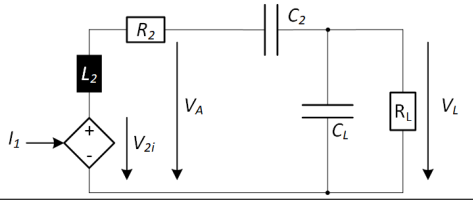
The total efficiency is finally calculated by the following expression:

$$\begin{aligned} \eta_{\omega_0} &= \eta_{1,\omega_0} \eta_{2,\omega_0} \\ &= \frac{M^2 L_2 \left(C_{PAR} R_L^2 - L_2\right)}{\left[M^2 \left(C_{PAR} R_L^2 - L_2\right) + R_1 \left(C_{PAR} L_2^2 R_L + C_{PAR}^2 L_2 R_2 R_L^2\right)\right]} \\ &\quad \cdot \frac{1}{\left[L_2 + C_{PAR} R_2 R_L\right]} \end{aligned} \tag{2.48}$$

2.4.2 Inductive coupling and series resonance

In the series resonance, instead of connecting the capacitor C_2 in parallel with the RFIC impedance, it is placed in series. The analysis of such a circuit is very similar to the one performed for the parallel resonant case. Table.2.2 summarizes the equations of the inductive link for both the parallel and the series resonant case.

Table 2.2 Inductive link equations with transponders in resonance for both series and parallel configuration.

Variables		
ω_0	$\sqrt{\frac{1}{C_{PAR}L_2}-\frac{1}{C_{PAR}^2R_L^2}}$	$\sqrt{\frac{1}{2C_L^2R_L^2}\left(\frac{R_L^2C_L-L_2}{L_2}+(\ldots)\right)+\frac{1}{2L_2C_2}}$
	$C_{PAR}=C_2+C_L$	$(\ldots)=\sqrt{\frac{C_L^4R_L^4+C_2^2(L_2-C_LR_L^2)^2+2C_2C_L^2R_L^2(L_2+C_LR_L^2)}{C_2^2L_2^2}}$
C_{ser}	$\frac{1+(\omega R_LC_{PAR})^2}{\omega^2R_L^2C_{PAR}}$	$\frac{C_2(1+\omega^2R_L^2C_L^2)}{1+\omega^2R_L^2(C_2C_L+C_L^2)}$
R_{ser}	$\frac{R_L}{1+(\omega R_LC_{PAR})^2}$	$\frac{R_L}{1+\omega^2R_L^2C_L^2}$
Q_{2L}	$\frac{1}{\frac{R_2}{\omega L_2}+\frac{1}{\omega C_{PAR}R_L}}$	$\frac{1}{\frac{R2}{L_2\omega}+C_{ser}R_{ser}\omega}$
$Re(R_{EQ})$	$\frac{M^2\omega^4C_{ser}^2(R_2+R_{ser})}{\omega^2C_{ser}^2(R_2+R_{ser})^2+(\omega^2C_{ser}L_2-1)^2}$	$\frac{M^2\omega^4C_{ser}^2(R_2+R_{ser})}{\omega^2C_{ser}^2(R_2+R_{ser})^2+(\omega^2C_{ser}L_2-1)^2}$
P_{RL}	$\frac{I_1^2\omega^2M^2R_LL_2C_{PAR}}{2(L_2+C_{PAR}R_2R_L)^2}$	$\frac{I_1^2\omega^4M^2C_{ser}^2R_{ser}}{2-4C_{SER}L_2\omega^2+2C_{SER}^2\omega^2(L_2^2\omega^2+(R_2+R_{SER})^2)}$
η	$\frac{M^2R_L\omega^2}{M^2\omega^2(R_2+R_L+C_{PAR}^2R_2R_L^2\omega^2)+R_1(\ldots)}$	$\frac{Cser^2M^2R_L(R_2+R_{ser})\omega^4}{(R_2+R_L+C_L^2R_2R_L^2\omega^2)(\ldots)}$
	$(\ldots)=2R_2R_L+L_2^2\omega^2+R_L^2(C_{PAR}L_2\omega^2-1)^2+R_2^2(1+C_{PAR}^2R_L^2\omega^2)$	$(\ldots)=R_1-2C_{ser}L_2R_1\omega^2+C_{ser}^2M^2(R_2+R_{ser})\omega^4+C_{ser}^2R_1\omega^2(R_2^2+2R_2R_{ser}+R_{ser}^2+L_2^2\omega^2)$

Chapter 3

New dielectric droplet encapsulation approach for RFID chip

3.1 Introduction

In this chapter, a new concept-level inkjet-based single chip liquid encapsulated delivering system is first presented. Subsequently, static fluid simulations and experimental tests have been undertaken for proving the feasibility of the chip liquid encapsulation onto the antenna substrate.

Three main aspects have been taken into account during the conceptual definition of the delivering system, that is the removal (or simplification) of: i) the wafer level die preparation such as UBM and copper pillars; ii) the conductive bump or film deposition; iii) the complex attachment of the chip with temperatures, forces and the high precision positioning requirements.

The concept is inspired from the inkjet printing due to its digital (Drop-On-Demand -> DOD) nature which fit very well with passive RFID tags in which large antenna and small chips are used. In addition, thanks to the high potential of parallelization (e.g. a multi-printheads), the process will be compatible with standard roll-to-roll (R2R) printing processes enabling the production of RFID tags only with printing steps.

3.2 Single chip delivery concept

The proposed assembly approach is shown in Fig.3.1 and it can be described as it follows: a container is filled with RFICs suspended in a liquid environment where they are randomly distributed to avoid agglomeration that would lead to the clogging of the input channel of the encapsulation system. The latter takes RFICs one-by-one encapsulating them in order to create a pipeline of droplets where each one encapsulates one RFIC. Once the droplets are into the printhead (e.g. an inkjet-like printhead), they are delivered in correspondence of the RFID antenna.

Considering the nature of the proposed process, a precise orientation of the RFIC inside the droplet during the encapsulation would be a complex task that would counterbalance the simple and low-cost approach. In fact, the chip may be shifted, tilted or turned upside down at the input of encapsulation system. In order to get rid of this orientation dependence (required by currently used industrial technologies), the RFIC has been designed using the sandwich structure proposed by Hitachi which consists in having a large metal layer on the top of chip acting as one contact for connecting the antenna. The second contact is the bulk of the silicon chip. However, compared to the Hitachi solution, in this work, a standard and low-cost CMOS technology will be employed and the RFIC will be called: double-surface RFIC (DS-RFIC).

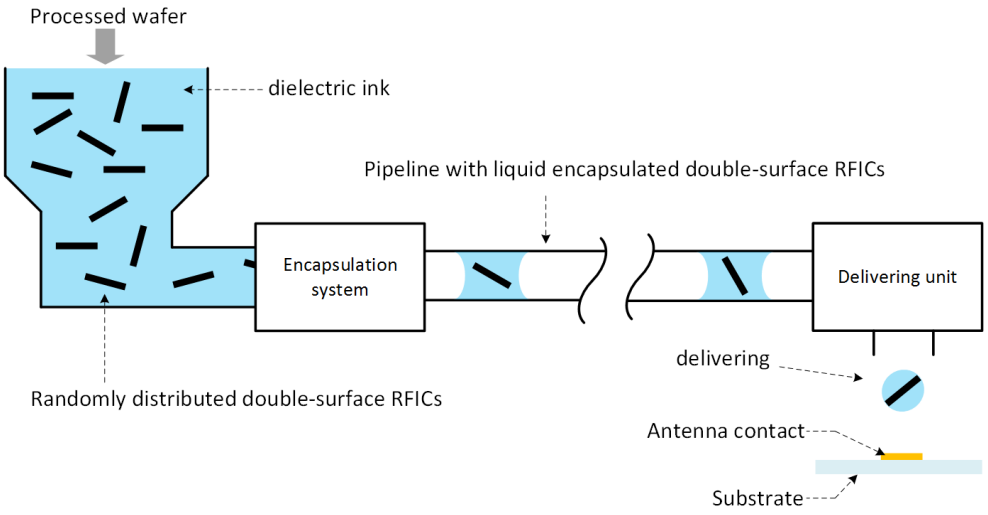


Fig. 3.1 Conceptual view of the Inkjet-based fabrication approach with: i) randomly distributed double-surface RFICs; ii) the single chip, liquid encapsulation system; iii) the delivering pipeline; iv) the inkjet-like printhead for single droplet delivering.

The encapsulation system itself is used along with a focalization unit which as the name implies, it deals with the focalization of DS-RFICs enabling the extraction and encapsulation of them on-by-one. As shown in Fig.3.2, a high frequency communication test is performed before the encapsulation to separate working DS-RFICs from the non-working ones. The latter leave the system through a waste channel.

The single chip detection is performed using a CCD camera pointed towards a specific region of interest (ROI). The latter will be defined based on both the liquid flow speed and the encapsulation latency. Thanks to the information of the CCD camera, an embedded control system drives: i) the encapsulation if the single chip detection succeed and ii) the rejection if the single chip detection fails due to the proximity of two or more DS-RFICs. During the rejection they are guided back to the encapsulation unit thanks to a recycling channel. In this way DS-RFICs are reused without passing again through the wall system.

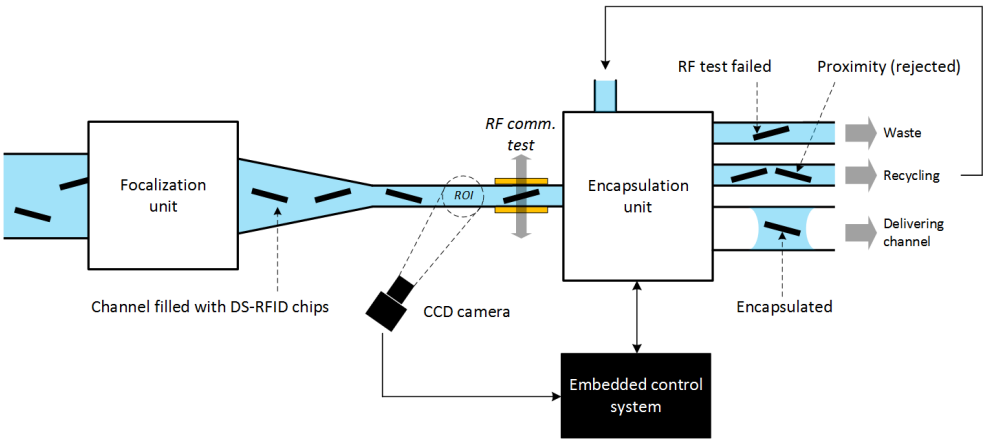


Fig. 3.2 Conceptual view of the encapsulation system with: i) the chip focalization unit; ii) RF communication test with single chip detection through CCD camera; iii) the encapsulation unit with waste, rejection and encapsulation capability.

Taking inspiration from the multi-printheads industrial inkjet printers and based on the concept of Fig.3.1, a fabrication process with a multistage configuration has been proposed. The latter can be used and integrated into R2R processes. It consists in adding N delivering stages where each one encompasses the encapsulation system as well as the inkjet-like printhead as shown in Fig.3.3.

The length of the delivering pipeline and the number of droplets can be adapted based on multiple attributes such as throughput, latency, RF communication and

encapsulation failure rates. All of them are required to meet specific fabrication requirements.

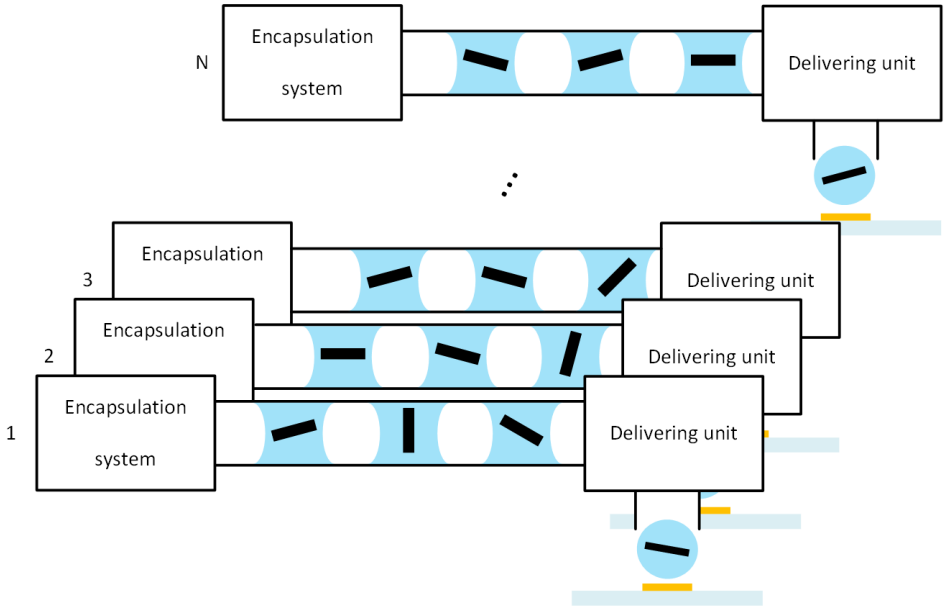


Fig. 3.3 Conceptual view of the multistage fabrication approach.

As shown in Fig.3.4, after the delivering phase (step 1), each droplet lands on the substrate with a relatively high precision with respect to the contacts of the antenna (pads). Thanks to specifically designed wetting contrasts between the contact of the antenna and its surroundings, a self-assembly process takes place where the droplet is spontaneously aligned over the high wettability pad. The chip is transported by the droplet through this self-assembly process.

The peculiarity of this process consists in having a dielectric ink that acts as liquid environment. On the basis of this, a curing phase (step 2) is performed in order to "fix" the dielectric droplet with the encapsulated RFIC. In this way, the bonding step (e.g. solder reflow or themocopression) has been removed from the process since the large top metal layer and the silicon substrate of the chip act as the plates of two capacitors. Using them in conjunction with the contacts of the antenna and the dielectric ink will result in a chip capacitively coupled to the antenna. This structure allows having the contacts of the antenna as large as the chip strongly relaxing the alignment requirements and reducing reliability concerns due to bad contacts. In addition to electrical connections, this method furnishes a mechanical shell to protect the chip from physical damage and external contaminants.

Finally (step 3), the top contact is printed with a conductive ink to close the loop of the antenna. It is important to note that this step will not be performed by the proposed inkjet-like printhead but rather in a subsequent stage in which standard printing technologies, compatible with R2R processes, will be used.

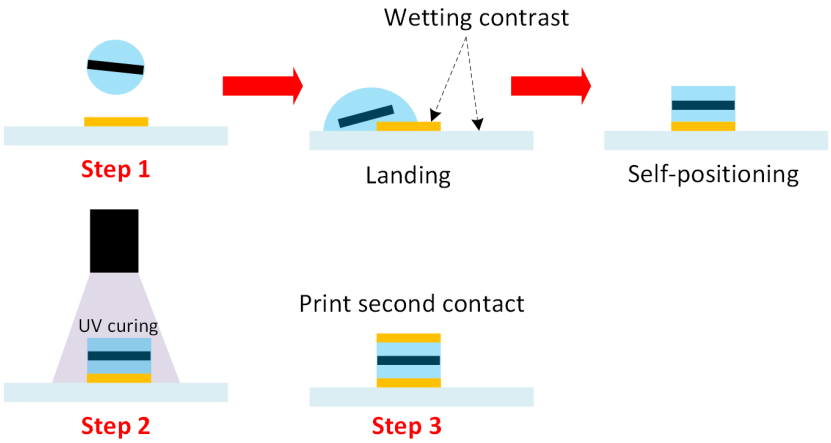


Fig. 3.4 Conceptual view of the self-assembly process: step 1) the RFIC is delivered inside a dielectric droplet and after the landing on the substrate, a self-assembly takes place enabling a precise positioning of the chip with respect to the contact of the antenna; step 2) the dielectric droplet is cured by UV exposure; step 3) the top contact of the antenna is printed for closing the loop of the antenna.

Fig.3.5 shows a conceptual cross-section of the stacked structure with the DS-RFIC encapsulated inside the dielectric ink after the spontaneous alignment over the contact of a high frequency antenna coil. The capacitive coupling has been identified in the following way:

- C_{Aa}: is the capacitor between the top contact of the antenna and one contact of the chip which is, in this case, the top side. This capacitor needs to be maximized since it belongs to the conduction path from the antenna to the circuitry of the transponder. For a given relative permittivity and surface of the chip, the capacitance mainly depends on the distance d_{Aa} between the two plates of the capacitor, therefore, the self-assembly process needs to be optimized in order to achieving this.

- C_{Ab}: is the capacitor between the top contact of the antenna and the opposite side of the chip. In this case, its value needs to be minimized since it is a conduction path that does not contribute to the functionality of the transponder.

For a given relative permittivity and a lateral cross-sectional area of the chip, the capacitance mainly depends on the orientation of the chip inside the droplet.

- C_{FT}: is the capacitor that couples the top and the bottom contacts of the antenna. As for the case of C_{Ab}, its value needs to be minimized since signals passing through it, will be lost and do not contribute to the functionality of the transponder. In this case, the capacitance manly depends on dimensional variations (e.g. ΔL) as well as on the lateral shifts (e.g. d_x).

- C_{Bb}: as for C_{Aa}, this capacitor is in the useful conduction path, hence it needs to be maximized.

- C_{Ba}: as for C_{Ab}, this capacitor needs to be minimized.

For the rest of this document, C_{Aa} and C_{Bb} will be called coupling capacitors whereas C_{Ab}, C_{Ba} and C_{FT}) will be called cross-coupling capacitors.

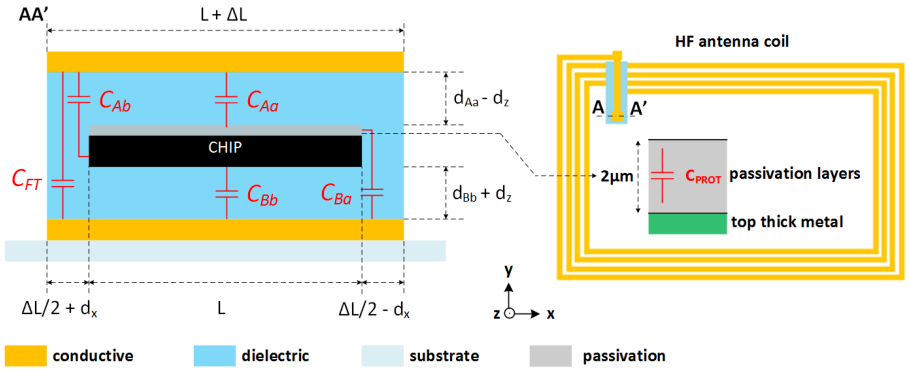


Fig. 3.5 Conceptual view of the DS-RFIC inside the sandwich structure after self-assembly over the contact of a high frequency antenna coil.

The top surface of an integrated circuit is normally entirely protected with one or multiple passivation layers, except for bond pads that need to be open to allow electrical connections. As shown in Fig.3.5 and reported by the process parameters document [94] of the foundry with which a first version of the DS-RFIC has been fabricated, the two passivation layers have a total thickness of $2\mu m$ creating a large capacitor C_{PROT} which results in a series combination with the coupling capacitor C_{Aa}.

Considering the nature of the proposed assembly process, a first approximation lets assume that the following condition will take place: $C_{PROT} \gg C_{Aa}$. This point

will be investigated later taking into account more realistic shape of the dielectric droplet with respect to the conceptual one shown in Fig.3.5.

3.3 Surface tension-driven self-alignment

The surface tension-driven self-alignment, also called capillary self-alignment (CSA) is a promising technique for the proposed inkjet-based fabrication process depicted in Fig.3.4. Simulations have been carried out in order to investigate and understand final shapes of the dielectric layers constituting the capacitive coupling.

The movement of the droplet, along with the encapsulated DS-RFIC, relies on a large wetting contrast between the pad of the antenna and its surroundings. For this reason, investigation on the required wetting conditions is an essential step to provide guarantees of a precise self-alignment. Volumes, sizes of the chip and contact angles are analyzed and simulated using the publicly available Surface Evolver (SE) software developed by Brakke [95, 96]. In addition, equilibrium shapes (after self-assembly) are imported into Comsol Multiphysics for extracting coupling and cross-coupling capacitor values and evaluating electrical performances.

3.4 Theoretical background and droplet modeling

3.4.1 Interfaces and surface tension

The boundary between two immiscible fluids depends on their molecular interactions and on Brownian diffusion (thermal agitation). In a microscopic level, the interface between two fluids can be represented as shown in Fig.3.6 (b). However, in an engineering level, it is more interesting to consider the macroscopic behaviur of the interface. In this case, as shown in Fig.3.6 (a), the interface has no thickness, is completely smooth and characterized by the angle θ formed between the substrate plane and the tangent of the liquid-air interface at the triple contact line (3L).

In the bulk of the liquid, each molecule is subject to interactions with neighboring molecules. These interactions are manly hydrogen bonds for polar liquid (e.g. water) and van der Waals attractions for organic liquids [97].

As schematically shown in Fig.3.6 (c), the air has a lower density in comparison to the liquid droplet, therefore, air molecules exhibit fewer interactions and less attractions. Following that, at the liquid - air interface there is an asymmetry, in terms of interactions, which results in an excess of surface energy. The latter, in a macroscopic scale, is characterized by the surface tension, usually denoted by γ, that takes into account this molecular effect. The dimension of the surface tension is the energy per unit area ($dyn\ cm^{-1} = mN\ m^{-1}$). According to this definition, the energy of a homogeneous interface, of surface area S, can be expressed as it follows:

$$E = \gamma S \tag{3.1}$$

The same principle applies to the solid - liquid interface. In fact, liquid molecules are attracted towards the interface due to van der Waals forces. If the attraction is strong, the SL interface has a negative energy and the solid is qualified as lyophilic (hydrophilic for water). On the other hand, if attractions are weak, the SL interface has a positive energy and the solid is qualified as lyophobic (hydrophobic for water).

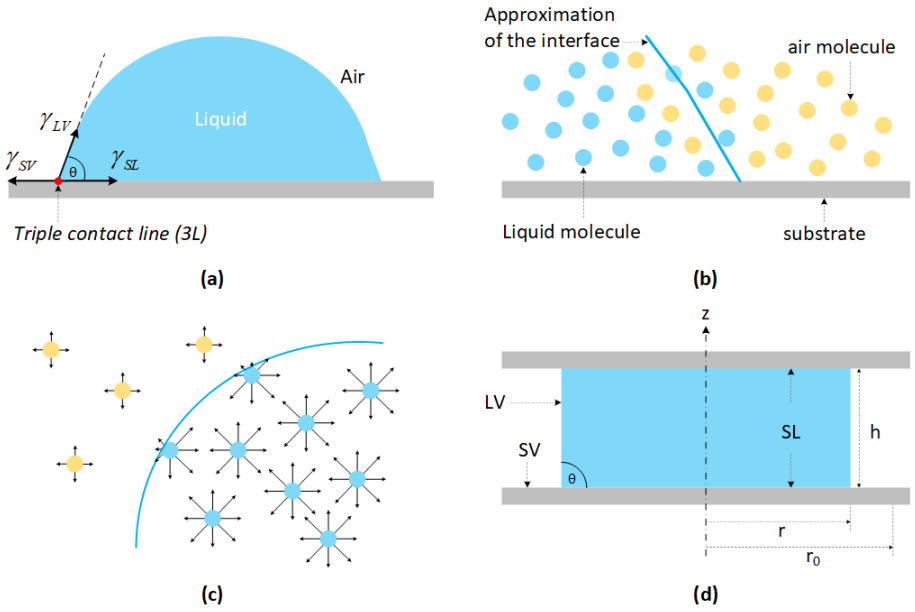


Fig. 3.6 (a) Example of a droplet over a solid substrate. The triple contact line, also called three-phase contact line, is characterized by a schematic of three forces per unit length that balanced out at equilibrium. (b) Example of a LV interface at the microscopic scale. (c) Molecular interaction with asymmetry at the LV interface. (d) An example of a liquid, of radius r, confined between two parallel surfaces (see text for explanation). The radius $r_0 \gg r$ is an arbitrary constant for defining the SV interface.

As an introduction, let's assume the case explained in [98] and represented in Fig.3.6 (d). In this example a liquid is confined between two solid surfaces creating a system with three phases: S (solid), L (liquid), V (vapor) and three interfaces: LV (liquid - vapor), SL (solid - liquid), SV (solid - vapor) with a total energy equal to:

$$E = E_{SL} + E_{SV} + E_{LV} = \gamma_{SL} S_{SL} + \gamma_{SV} S_{SV} + \gamma_{LV} S_{LV} \tag{3.2}$$

The energy of each interface can be expressed in the following way:

$$E_{SL} = 2\gamma_{SL}\pi r^2 \tag{3.3}$$

$$E_{SV} = 2\gamma_{SV}(\pi r_0^2 - \pi r^2) \tag{3.4}$$

$$E_{LV} = \gamma_{LV} 2\pi r h \tag{3.5}$$

where the radius $r_0 \gg r$ is an arbitrary constant for defining the SV interface.

By combining the last three equations into Eq.3.2, the total energy can be rewritten as:

$$\begin{aligned} E &= 2\gamma_{SL}\pi r^2 + 2\gamma_{SV}(\pi r_0^2 - \pi r^2) + \gamma_{LV} 2\pi r h \\ &= 2\gamma_{SV}\pi r_0^2 - 2\pi r^2(\gamma_{SV} - \gamma_{SL}) + \gamma_{LV} 2\pi r h \\ &= constant - \underbrace{S_{SL}(\gamma_{SV} - \gamma_{SL})}_{\text{M}} + \underbrace{\gamma_{LV} 2\pi r h}_{\text{N}} \end{aligned} \tag{3.6}$$

where the term M is characterized by the Young's law:

$$\gamma_{LV}\, cos(\theta) = \gamma_{SV} - \gamma_{SL} \tag{3.7}$$

This relation is very useful for understanding the behavior of droplets on surfaces and it comes from the fact that at equilibrium, the projection of the "forces" of the 3L on the x-axis must be zero. The contact angle between the liquid and the solid surface can therefore be defined as:

$$\theta = arcos\left(\frac{\gamma_{SV} - \gamma_{SL}}{\gamma_{LV}}\right) \tag{3.8}$$

The term M can be rewritten taking into account the Young's law:

$$M = S_{SL}\ \gamma_{LV}\ cos(\theta) \tag{3.9}$$

Simulations have been performed using Surface Evolver. The latter processes an evolution script containing geometry coordinates, various parameters (e.g. surface tension and contact angles) and constraints (volume, level-set and triple-line) in order to evolve the LV (in this case ink - air) interface toward an energy minimum.

3.4.2 Droplet geometries

The geometries of droplets are defined by four elements which can be described as it follows:

- **Vertices**: A vertex is characterized by a point with three coordinates in space (x, y and z) and one identification number. In Fig.3.7 (b), the vertices are numbered from 1 to 16 defining an initial rectangular shape. During the surface evolution (computational iterations) the coordinates of each vertex are changed. The vertices carry energy if they are on a 3L constraint.
- **Edges**: Edges are one-dimensional geometric elements. Using a linear model, an edge is an oriented segment between two vertices. As shown in Fig.3.7 (b), edge 1 is defined as the segment between vertex 1 and 2. Using higher order models, edges are defined by interpolating end vertices with intermediate points. Edges carry energy if they are on a 3L constraint.
- **Facets**: A facet is an oriented triangle defined by three edges. Using a linear model, triangles are flat surfaces whereas in a quadratic model, they are curved defined by quadratic interpolation between three vertices and three midpoints. In the example of Fig.3.7 (b), the facets are not yet triangulated. This step is performed once the evolution script is loaded into SE. Facets carry surface tension energy depending on their area.
- **Bodies**: A body is a 3D region of space made up of all the boundary facets together (triangular 2D facets). The body is not triangulated (meshed) but only its facets that are used for calculating the body volume and the gravitational energy. In Fig.3.7 (b), the body is defined by nine facets.

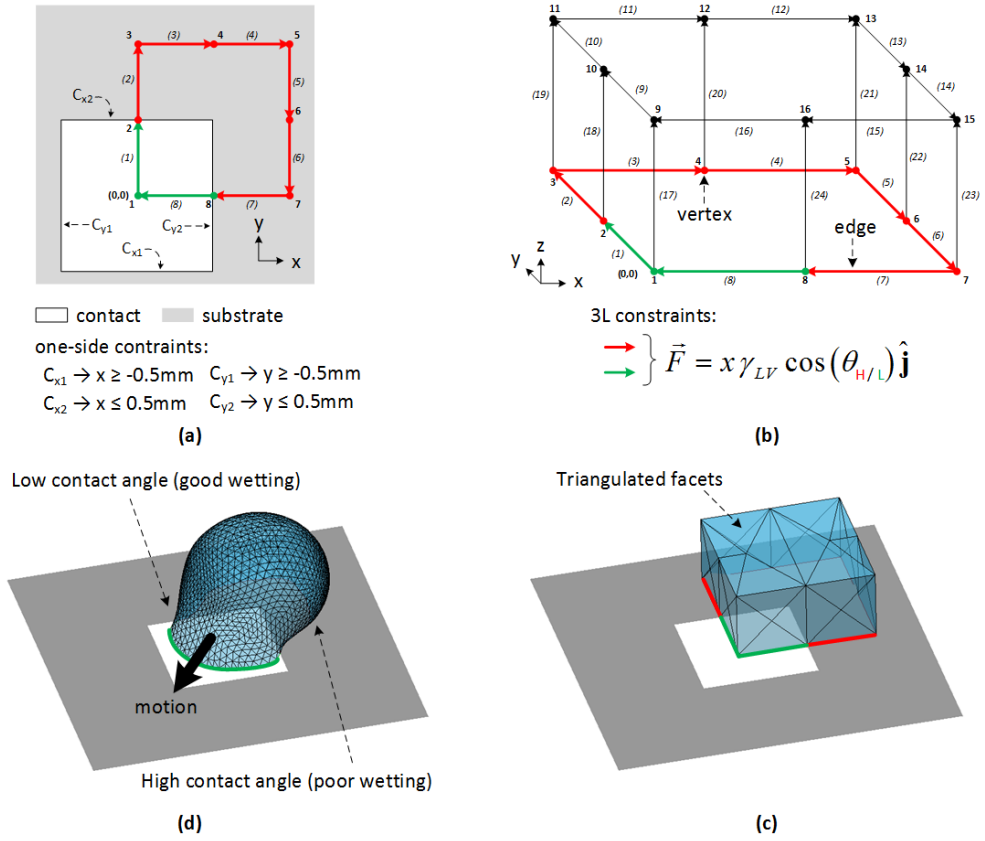


Fig. 3.7 (a) Triple line (3L) and one-sided constraints defined on both vertices and edges on the *x*-*y* plane at *z*=0. (b) Droplet initially defined as a parallelepiped with vertices (defined by 3D coordinates), edges and facets. (c) Droplet with triangulated facets after loading of the evolution script into SE. (d) Capillary self-alignment (CSA) of the droplet toward the low contact angle surface (good wetting) after some computational iterations. The iterations proceed until convergence of the energy penalty function. Refinements are performed for a better approximation of the curved surface and help convergence.

3.4.3 Triple-line constraint

In Surface Evolver, normally, only the LV interface is meshed and not the SL. However, in order to compute the energetic content of the non-meshed interface, 3L constraints can be defined into the evolution script. This can be seen in Fig.3.7 (a) where the SL interface is considered as one-dimensional boundary elements (red and green arrows) with associated energy specified by a vector field $\vec{F}$.

In the Cartesian coordinate system, the SL interface energy can be defined as it follows:

$$\vec{E}_{SL} \;=\; \gamma_{LV}\, cos(\theta) \iint_{S} \hat{\mathbf{k}} \cdot d\vec{S} \tag{3.10}$$

This equation implies that the energy is in the *x*-*y* plane where $\hat{\mathbf{k}}$ is a unit vector parallel to the local vertical direction of the frame of reference. At this point, $\vec{F}$, can be defined using the Stokes's theorem which states, as already explained in chapter 2, that:

$$\iint_{S} \nabla \times \vec{F} \cdot d\vec{S} \;=\; \oint_{\partial S} \vec{F} \cdot d\vec{l} \tag{3.11}$$

where the curl operator is:

$$\nabla \times \vec{F} \;=\; \left(\frac{\partial F_z}{\partial y} - \frac{\partial F_y}{\partial z}\right)\hat{\mathbf{i}} + \left(\frac{\partial F_x}{\partial z} - \frac{\partial F_z}{\partial x}\right)\hat{\mathbf{j}} + \left(\frac{\partial F_y}{\partial x} - \frac{\partial F_x}{\partial y}\right)\hat{\mathbf{k}} \tag{3.12}$$

From Eq.3.11, it follows that the vector field $\vec{F}$ needs to be found in order to satisfy the following relation:

$$\nabla \times \vec{F} \;=\; \gamma_{LV}\, cos(\theta)\, \hat{\mathbf{k}} \tag{3.13}$$

leading to these two possible solutions:

$$\vec{F} \;=\; x\, \gamma_{LV}\, cos(\theta)\, \hat{\mathbf{j}} \quad or \quad \vec{F} \;=\; -y\, \gamma_{LV}\, cos(\theta)\, \hat{\mathbf{i}} \tag{3.14}$$

Therefore, a 3L can be defined with both vectors fields finally leading to the same result.

3.4.4 Level-set constraint

Level-set constraints are planar equations which are used to restrict the SL (in this case substrate - ink) interface to lie on one or multiple planes. Let's assume the case shown in Fig.3.7 in which the droplet needs to be confined on a specific region (white square-shaped surface) located on a wider substrate (grey). In this situation, both vertices and edges of the 3L on the substrate will be on one level-set constraint (red arrows) whereas the vertices and edges belonging to the 3L on the white surface

will be on four one-sided constraints (green arrows) to keep it within this surface. The one-sided constraint is defined with the form $x \geq$ - 0.5 or $y \leq 0.5$ as shown in Fig.3.7 (a).

The evolution script has been written in order to detect when vertices and edges, on the triple-lines, hit a one-sided constraint. If this happens, both vertices and edges are transferred to another level-set constraint removing one degree of freedom from them. This finally allows the constrained motion of droplets towards desired locations as shown in Fig.3.7 (d).

Gravitational energy and volume constraint

Energy minimization takes place considering both level-set and triple-line constraints. In the case of this work, the total energy E, which represents the energy contribution of each facet of the meshed LV interface, has been defined as a combination of the surface tension and the gravitational energy as it follows:

$$E = \gamma_{LV} \iint_S dS + \rho g \iiint_V z \, dV \tag{3.15}$$

where ρ is the density of the dielectric ink, g is the gravitational acceleration (9.81 ms^{-2}), S is the area of a facet and z is its height.

If the gravitational energy can be ignored for droplets in the micrometer range, it is not necessarily the case for millimeter-sized droplets. In this case, the density of the liquid play an important role.

Surface Evolver cannot perform volume integrals, however, the latter can be converted to a surface integral by means of the Divergence Theorem which states that:

$$\iiint_V \nabla \cdot \vec{W} \, dV = \iint_{\partial V} \vec{W} \, d\vec{S} \tag{3.16}$$

where the divergence operator is:

$$\nabla \cdot \vec{W} = \frac{\partial Wx}{\partial x} + \frac{\partial Wy}{\partial y} + \frac{\partial Wz}{\partial z} \tag{3.17}$$

Therefore, the following relation can be used:

$$\nabla \cdot \vec{W} = z \tag{3.18}$$

which leads to:

$$\vec{W} = \frac{z^2}{2}\hat{\mathbf{k}} \tag{3.19}$$

At this point, the gravitational energy can be rewritten, in terms of surface integral, as it follows:

$$\rho g \iiint_V z dV = \rho g \iint_{\partial V} \frac{z^2}{2}\hat{\mathbf{k}}\, d\vec{S} \tag{3.20}$$

If evaporation does not take place during the self-assembly process, a built-in function in SE can be used to define a volume constraint. The volume is calculated at each iteration in order to keep it constant and equal to the constrained value. As for the gravitational energy, the volume can be calculated using the Divergence Theorem leading to the following expression:

$$\iiint_V dV = \iint_{\partial V} z\,\hat{\mathbf{k}}\, d\vec{S} \tag{3.21}$$

Each oriented facet of the surface forms, with respect to the *x*-*y* plane at $z = 0$, a volume which is characterized by a prism. The contribution of all facets constitutes the total volume of the droplet. This implies that certain types of facet, such as horizontal facets at $z = 0$ and vertical facets (90° with respect to the *x*-*y* plane at $z = 0$), do not contribute to the volume calculation. Indeed, the surface integral of the facet corresponding to the SL interface, may obviously be omitted for the calculation of both the volume and the gravitational energy.

3.4.5 Total energy and convergence

Surface Evolver performs several iteration steps in which the force at each vertex is determined using the negative gradient of the total energy as a function of the position of that vertex. This is basically the gradient descent method of minimization.

Following that, at each iteration, the surface is evolved by moving vertices in the direction of calculated forces. In addition, as can be seen in Fig.3.7 (d), the surface is progressively refined in order to have a better approximation of the curved surface.

The iterations proceed until convergence of an energy penalty function which in the most straightforward form can be expressed in the following way:

$$\Delta E \; = \; |E_1 \; - E_2| \; < \; \varepsilon |E_1| \tag{3.22}$$

In this case, the total energy difference after each iteration is compared and when the difference is smaller than a given value (defined by ε), convergence is achieved. However, this method may oscillate when a surface is near equilibrium, hence a more convenient convergence test is necessary.

SE has a built-in function that examines the standard deviation of the total energy about its average value:

$$\Delta E \; = \; \sqrt{\frac{\sum_{i=1}^{N} \left(E_i \; - \; \bar{E} \right)}{N \; - \; 1}} \; < \; \varepsilon |\bar{E}| \tag{3.23}$$

where the total average energy value is:

$$\bar{E} \; = \; \frac{\sum_{i=1}^{N} E_i}{N} \tag{3.24}$$

3.4.6 Capillary length and Bond number

Microscopic droplets are governed only by surface tension and they have spherical shapes as shown in Fig.3.8 (a). In the other hand, large droplets (millimeter range) result from a balance between gravity and surface tension. Their shape is flattened as shown in Fig.3.8 (b). The transition between these two definitions is given by the capillary length. The latter can be calculated using the following expression:

$$L_C \; = \; \sqrt{\frac{\gamma}{\Delta \rho \; g}} \tag{3.25}$$

where γ is the surface tension of the liquid and $\Delta \rho$ is the difference between the density of the liquid and the surrounding fluid.

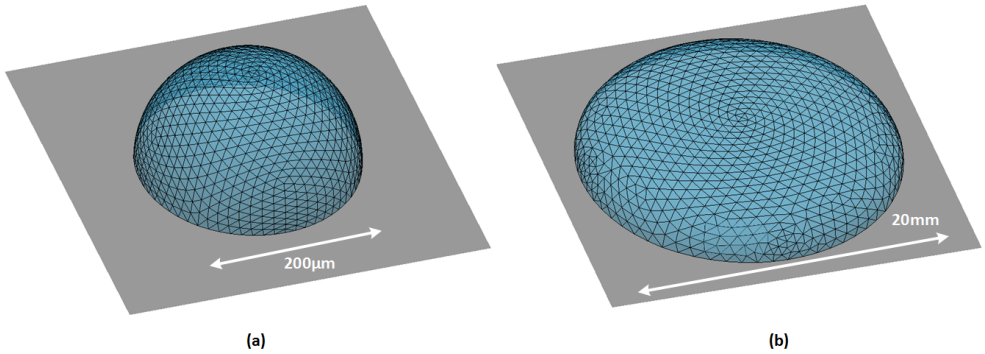


Fig. 3.8 Surface Evolver simulation of a microscopic droplet with spherical shape (a) and a large droplet governed by gravity and surface tension (b) . Images not to scale.

A similar meaning is given by the dimensionless number called Bond number (Bo). For Bo « 1 the droplet has a spherical shape, whereas for Bo » 1 it has a flattened shape due to the gravitational force. The Bond number is derived by Eq.3.25 and is expressed by:

$$Bo = \frac{\Delta\rho\ g\ R^2}{\gamma} \tag{3.26}$$

where R is the characteristic dimension, normally defined by the radius or the height (apex) of the droplet.

3.5 Antenna - substrate wetting contrast analysis

A first set of simulations has been carried out in order to study the behavior of the dielectric droplet after landing on the substrate. The wetting characteristics of the dielectric ink are reported in the experimental section 3.7.

The numerical model has been defined with the 3L entirely and uniformly outside the lyophilic region as shown in Fig.3.9. The energy content of the 3L is defined as it follows:

$$\vec{E_{NW}} = -y\ \gamma_{LV}\ cos(\alpha_{NW})\ \hat{\mathbf{i}} \tag{3.27}$$

where α_{NW} is the contact angle of the lyophobic substrate.

As shown in Fig.3.10 (a), the initial shape of the droplet is a parallelepiped with a volume corresponding to the minimum required for perfectly encapsulating the chip

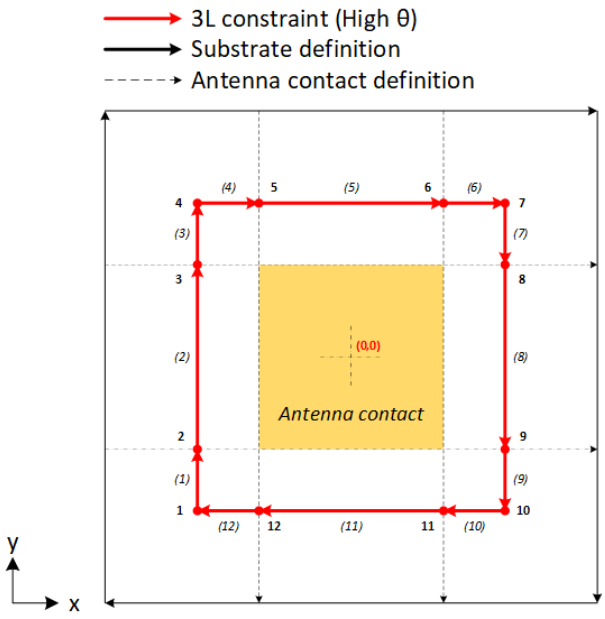


Fig. 3.9 Graphical representation of the SE model in the plane *x*-*y* where the 3L is entirely and uniformly outside the high wettability region (contact).

with a sphere. In these simulations, the chip has not been integrated in the model since the minimum volume is initially considered to be large enough to avoid the dewetting of the chip (e.g. region left uncovered creating new triple lines on the walls of the chip). Therefore, the surface of the droplet is minimized regardless of whether the chip is considered in the model or not.

Considering L as the lateral dimensions of a chip with a square surface and h_{CHIP} its thickness, the minimum volume of the ink can be calculated in the following way:

$$V_{MIN} = V_{SPHERE} - V_{CHIP} \approx \frac{\pi}{6}\left(2L^2 + h_{CHIP}^2\right)^{3/2} - h_{CHIP}\,L^2 \tag{3.28}$$

In order to perform analysis, a volume increase factor has been defined:

$$\delta = \frac{V_{DROP}}{V_{MIN}} \tag{3.29}$$

In Fig.3.10 (b) the contact angle α_{NW} on the substrate is too low for completely driving the droplet over the pad. In fact, it spreads outwards reducing its height and relaxing the surface curvature. At the same time, the diameter of the 3L increases

potentially leading to misalignments of the chip as highlighted by the tilted black shaded square (representing the DS-RFIC) in Fig.3.10 (c).

On the other hand, in Fig.3.10 (d), the droplet is perfectly confined over the pad due to a very high value of α_{NW}. In this case, the droplet spreads inwards until reaching the pad of the antenna. At this point the contact angle is supposed to change and become α_W which is much smaller. However, as well known for these type of applications, the contact angle depends on the volume of the droplet and since the pad is relatively small for the amount of liquid, a bulge morphology arises [67].

For both high and low values of α_{NW}, the triple line of the droplet moves inwards or outwards symmetrically in all directions on the *x*-*y* plane (perfectly flat and uniform substrate) as shown in Fig.3.10 (c).

3.5.1 Complete dewetting of the substrate

As reported in the state-of-the-art, the complete dewetting of the substrate is a proven condition for reliable self-assembly processes based on capillary forces. However, in the case of this work, there are three main issues:

- **Extreme non-wetting contact angle** (α_{NW}): As reported in section 1.2.2, the large wetting contrast alone is not sufficient to completely confine the droplet over the pad. Indeed, in the simulation of Fig.3.10 (d), a complete dewetting of the substrate takes place only for $\alpha_{NW} > 120°$ where for lower values, the contrast is already large. Such a high contact angles are extremely challenging for oil-like liquid with surface tension of only ≈20 to 30 mN/m.

- **Droplet height**: The droplet has an almost spherical shape which results in an excessive amount of dielectric ink between the contacts of the antenna and the chip. The superficial polymerization of the dielectric ink may shadow (reduce the radiative transfer) the deepest part of it from UV light leading to an incomplete curing which in turn may lead to additional signal attenuation as well as poor adhesions and low hardness of the dielectric shell.

- **Droplet folded shape**: As shown in Fig.3.10 (e), the printing of the electrical connection of the top side contact of the antenna is not possible without an extra fabrication steps such as the printing of additional dielectric layers for compensating the shape curved inwards (folded) near the triple-line.

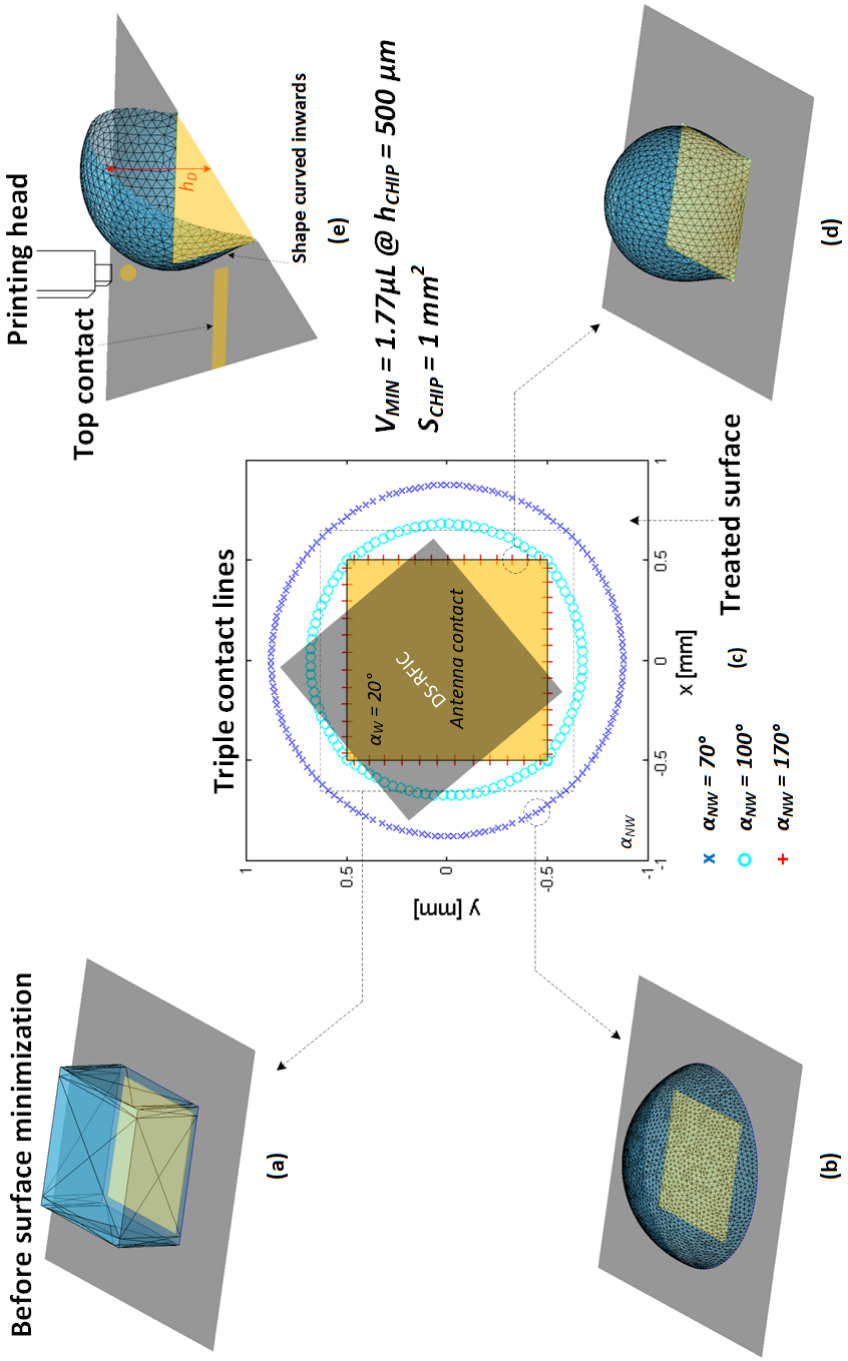


Fig. 3.10 (a) The dielectric droplet is initially modeled as a parallelepiped. Surface minimization start from this point. (b) Low contact angles on the substrate allow the spreading of droplets over it. This can potentially result in misalignments of the chip. (c) Plot showing the triple lines corresponding to each contact angle α_{NW}. (d) Perfect confinement of the droplet with a very high value of α_{NW}.

As a result of these considerations, the perfect confinement of the droplet over the pad of the antenna is not the preferred solution for this new assembly approach. In fact, most of the self-assembly processes found in literature evaporate the liquid droplet (e.g. water) leading to a perfect positioning. However, in this new approach, the droplet is part of the final electrical and mechanical coupling between the chip and the antenna.

3.5.2 Partial dewetting of the substrate

The partial dewetting is more interesting since, in comparison to the previous case, it allows a lower amount of dielectric ink above the chip and therefore better electrical performances.

In Fig.3.11 (a) are shown three droplet profiles where each one corresponds to a specific contact angle α_{NW} and in order to investigate the suitability of the partial dewetting, a square shape representing the DS-RFIC has been added under the profiles.

For the highest value ($\alpha_{NW} = 90°$) the lateral profile is relatively close to the pad of the antenna. At the same time, the upper level profile (above the chip) shows that the amount of dielectric ink is large leading to a low capacitor value and hence to a high-coupling impedance.

For the lowest value ($\alpha_{NW} = 70°$), the surface curvature is more relaxed, indeed the lateral profile is larger and the top of the droplet is closer to the surface of the chip.

It is important to note that the lowest the value of α_{NW}, the higher the probability to have a dewetting of the chip near its edges. In fact, as experimentally demonstrated in Fig.3.17 (e), this would let small parts of the chip (e.g. the silicon substrate) unexposed and potentially prone to short circuit when printing the conductive layer for closing the antenna loop (step 3 in Fig.3.4). In addition, the shape of the minimized surface is not reliable and the model needs to be changed including the chip.

As shown in Fig.3.11 (b), in order to avoid the dewetting of the chip with the lower value of α_{NW}, the volume of the droplet has been increased. This leads to larger lateral profile and therefore to a higher potential of misalignment, indeed the

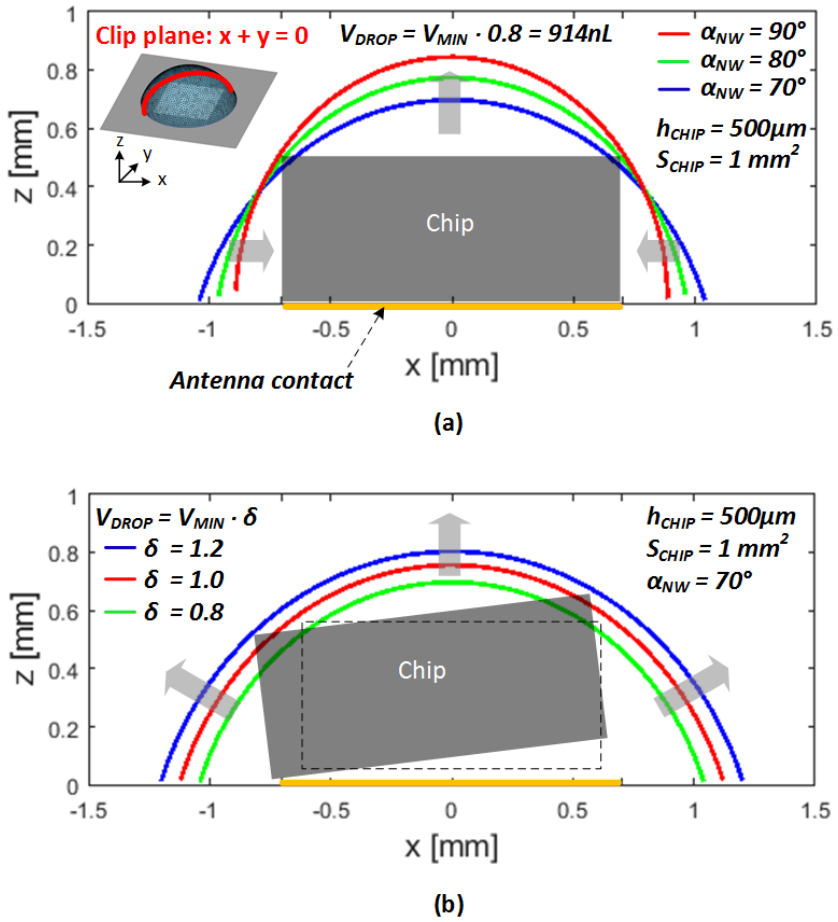


Fig. 3.11 (a) Cross-sectional view of the droplet for three contact angles on the substrate and using a volume slightly less the minimum one according to Eq.3.28. Potentially uncovered regions of the chip may lead to short-circuit when printing the top electrode of the antenna. (b) Cross-sectional view of the droplet for three larger volumes. Chip misalignments depend on the volume.

DS-RFIC may be tilted, shifted or both reducing the coupling capacitors and creating cross-coupling capacitors.

Nevertheless, thanks to the double-surface approach, the contacts of the antenna are as large as the chip and some misalignment can be tolerated without severe signal attenuation. Furthermore, the cross-coupling capacitors may have a limited impact on the signal attenuation. Following this, the partial dewetting is a promising solution that will be analyzed more in detail in section 4.3.

A working map considering the drop volume V_{DROP} and the contact angle has been performed in order to have an overview. Results are reported in Fig.3.13 for

three thicknesses of the RFIC. The latters have been defined with three typical values: 250μm (b), 500μm (c) and 750μm (d). All of them are used (without extra post-CMOS processes) in standard technologies such as for instance the AMS 0.35μm. The chip surface instead, has been defined as $1mm^2$ in order to ensure a minimum aspect ratio for the alignment of the double electrode structure with the pads of the antenna.

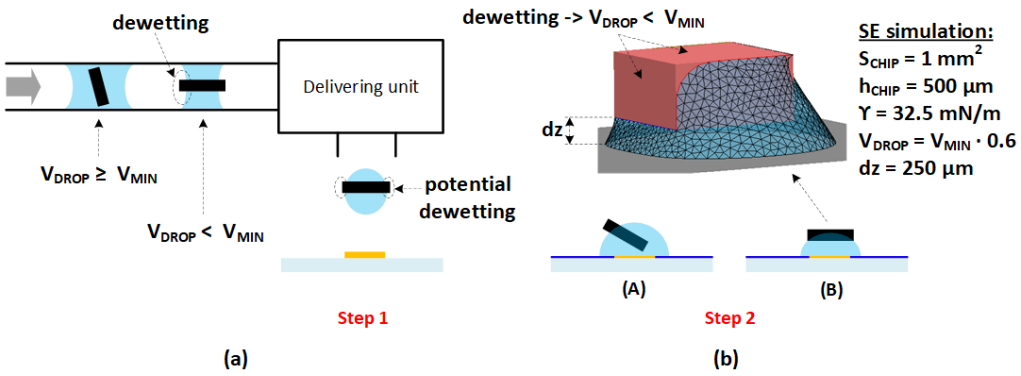


Fig. 3.12 (a) Delivering unit with chip partially dewetted inside the delivering channel and during the flight time. (b) Dewetting of the chip after self-alignment.

The volume starts from 0.6 times the minimum one according to Eq.3.28 and it is afterwards increased by the factor δ. The latter has been increased with step of 0.2. The second x axis (bottom one) defines the ratio between the droplet and the chip volume.

The red lines show the boundaries between the chip dewetting and the complete wetting. In the latter case, the surfaces of the droplet and the chip do not intersect considering the chip with zero offset in the z direction as shown in Fig.3.13 (a). Starting from this volume and above, the surface minimization of the droplet is considered to be equal regardless the chip is inside or not. For the dewetting case, an intersection has been observed. In this case, the corners of the chip are uncovered due to the interaction between the dielectric and silicon surface. Therefore, the shape of the droplet is modified and the model is not reliable any more.

It can be seen that for a thickness of 250 μm, a complete wetting of chip is guaranteed over the entire analysis range. As shown in Fig.3.12 (a) for volumes below the minimum one according to Eq.3.28, some parts of the chip may be unexposed during the transportation into the delivering channel (see Fig.3.1). The same may happen during the delivering, in fact as shown in Fig.3.12 (b), a part of

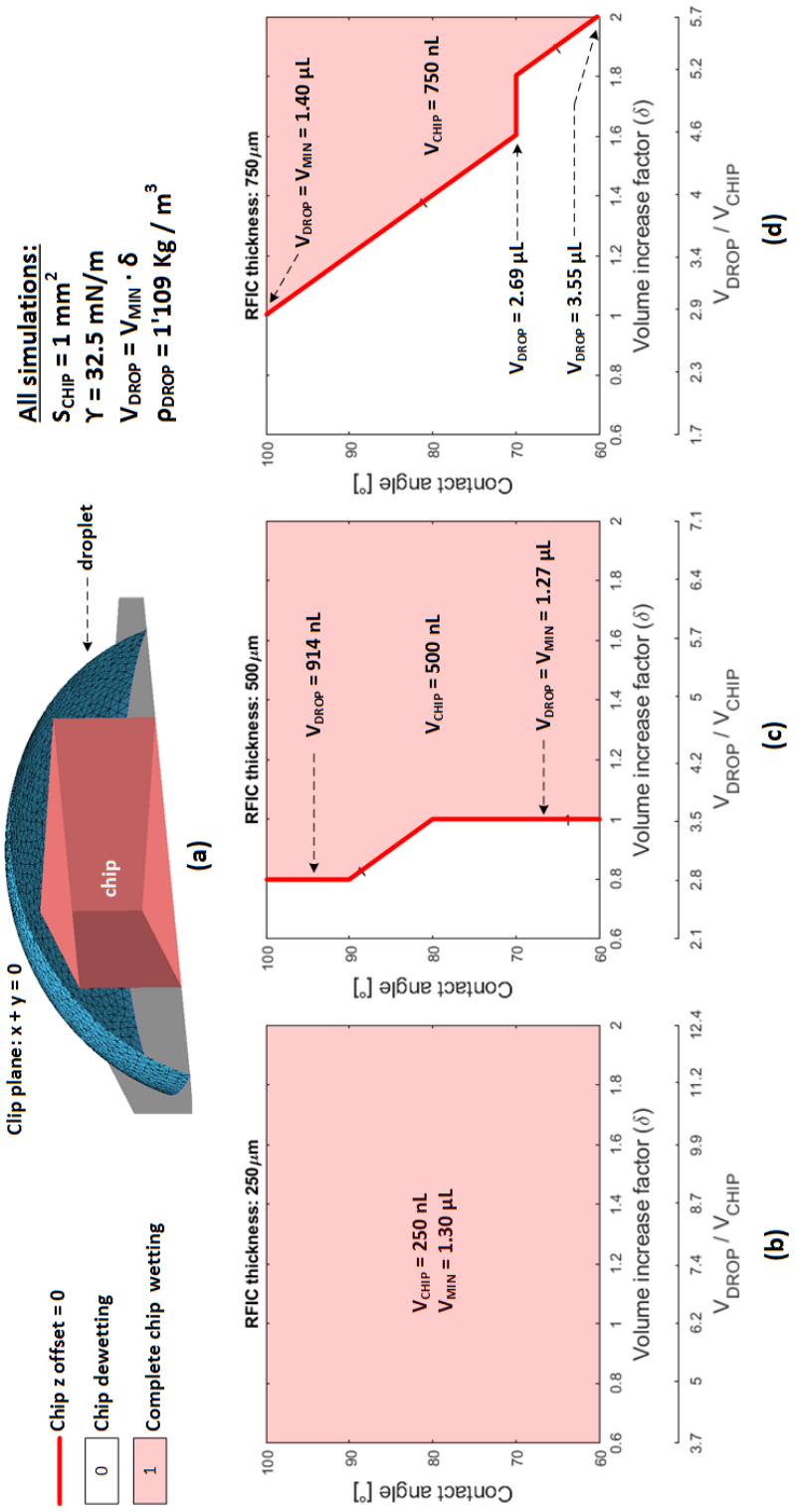


Fig. 3.13 (a) Cross-sectional view of the SE simulation after surface minimisation. Working map considering the drop volume V_{DROP} and the contact angle for a chip thickness of: 250 μm (b), 500 μm (c) and 750 μm (d).

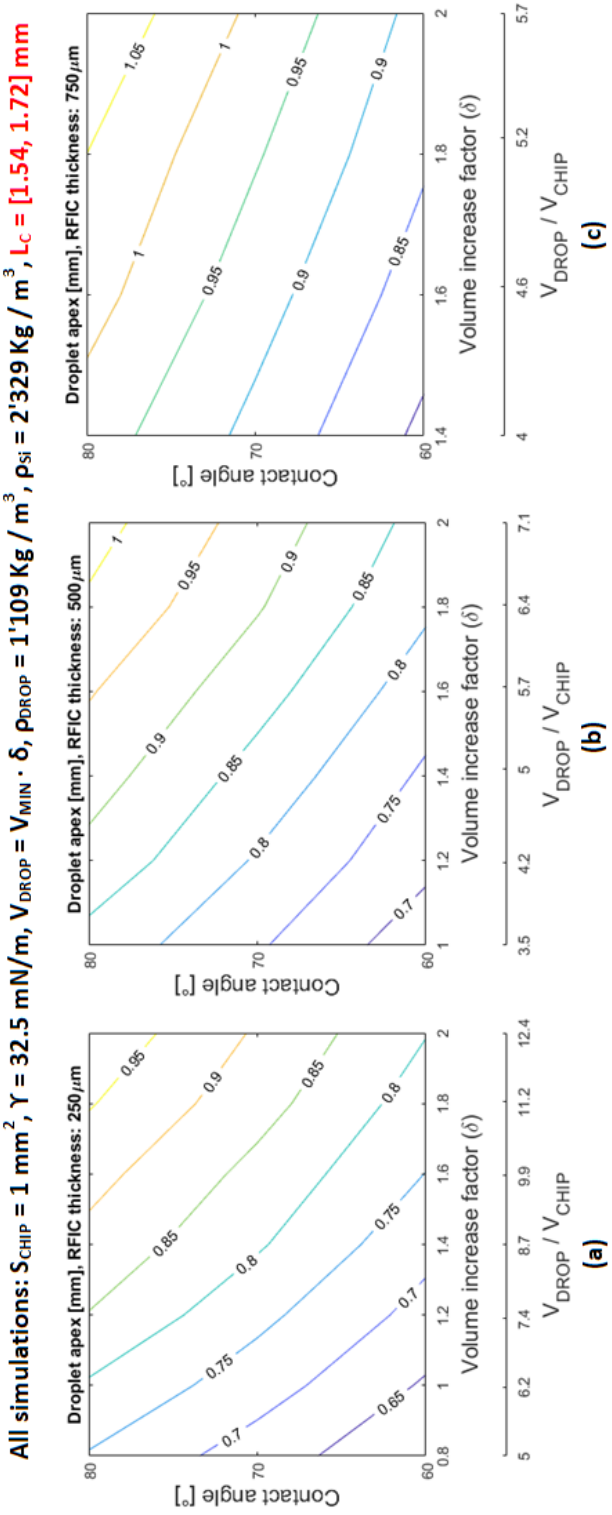


Fig. 3.14 (a) Apex (characteristic) length of dielectric droplets without chip. Simulation performed for a thickness of: 250μm (a), 500μm (b) and 750μm (c).

the chip may be left unexposed after the self-positioning process. Following that, the minimum volume should be guaranteed in any case. However, a large amount of volume means high coupling impedances and hence low electrical performances. This point will be further investigated in chapter 4.

For a thickness of $500\mu m$, volumes starting from the minimum one are sufficient in the range of CAs spanning from 60 to 80°. Above these values, both the surface treatment and the printing of the top contact of the antenna are considered too complicated, therefore, the cases from 80 to 100° will not further investigated.

For a thickness of $750\mu m$, a larger amount of ink is required in order to avoid any dewetting of the chip. As shown in Fig.3.13 (d), in the range of CAs spanning from 60 to 80°, the increase volume factor varies from 1.4 to 2.0, which means from 4 to 5.7 times the minimum volume.

Considering the relatively large volumes involved in the working ranges, the characteristic lengths (apex in this case) of dielectric droplets have been compared to the capillary length of the dielectric ink in order to verify if whether the gravitational force has an impact or not on the final shape of droplets.

Results are shown in Fig.3.14. Considering that the droplet volume is more than six times the volume of the chip for all thicknesses, the density of the liquid will dominate. Using an average density, the capillary length varies between 1.54 and 1.72 mm. These values are above the apex simulated in SE for the three thicknesses considering only the liquid, that is without chip. Therefore, gravitational effects can be neglected.

3.6 Droplet landing position analysis

A new set of simulations has been carried out for investigating the impact of the landing position (initial position of the droplet on the substrate) on the final shape of the droplet considering the case of a partial dewetting ($\alpha_{NW} = 70°$) as well as three different thicknesses of the chip with corresponding minimum volume.

As shown in Fig.3.15 (a), each droplet completely covers the high wettability region (pad of the antenna) while at the same time, it spreads on the substrate creating an asymmetric 3L. For chips with higher thicknesses, the 3L spreads largely on the substrate leading to a huge misalignment. In fact, considering a thickness of $h_{CHIP} =$

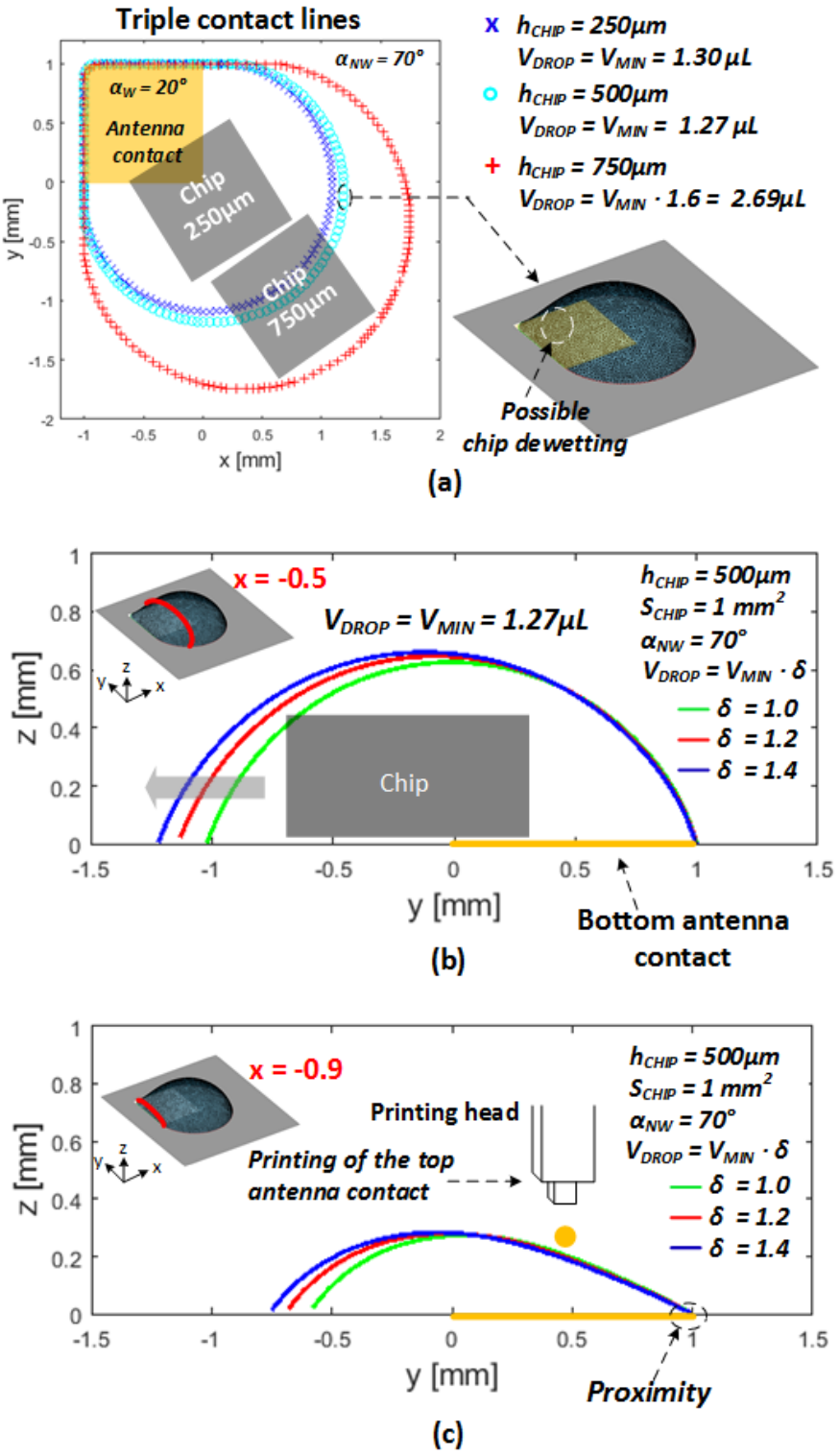


Fig. 3.15 (a) Left side: simulation results showing the triple lines of three droplets with minimum volume based on three different chip sizes. Smaller volumes allow better chip alignments. Right side: final shape of a droplet with asymmetric cross-sectional profile. (b) Cross-sectional view of the droplet in the middle of the antenna pad for three volumes larger than V_{MIN}. (c) Cross-sectional view of the droplet near the antenna pad edge.

$750\mu m$, the misalignment may be so large to completely impede any alignment between the DS-RFIC and the pad of the antenna. For $h_{CHIP} = 500 and 250\mu m$, the alignment is still not acceptable and a large chip dewetting may happen near the pad.

In Fig.3.15 (b) are shown the droplet profiles for three different amount of volume and a thickness of $h_{CHIP} = 500\mu m$. A larger volume of the droplet is important to avoid unexposed parts of the chip, however, more than 50% of lateral misalignment may occur. Indeed, on the surrounding of the pad, the lateral profile is shifted outwards while on the pad side, it is slightly pushed down.

The printing of the top contact of the antenna is a critical point in this case since as shown in Fig.3.15 (c), the asymmetric shape of the droplet leads to a small distance between the top and the bottom contacts. This may introduce a large feed-through capacitor C_{FT} that would strongly attenuate the electrical signal. In addition, a short-circuit may occur if the dielectric ink does not cover the bottom pad completely (e.g. proximity at y = $1mm$).

Following this analysis, it is clear that droplets have to be delivered as close as possible to the center of the pad. At this stage of the research and considering positioning accuracies of approximately $\pm$ 20 μm of nowadays mechatronics systems, the landing position will not be further investigated.

3.7 Experimental

3.7.1 Dielectric ink characterization

The dielectric ink is the InkA-I220 from Politronica. It is based on silica nanoparticles dispersed in an epoxy matrix. The low frequency dielectric constant is 5 and the surface tension is between 30 and 35 mN/m. An average value of 32.5 mN/m has been used for all the simulations previously presented.

The density of the ink has been measured using the densimeter Anton Paar DMA 4100 M. Measurements have been carried out at 30°C and 45° of inclination. The average density value, out of four values, is $1.109 kg/m^3$.

Wetting conditions have been measured using the GH11 Drop Shape Analysis System of Krüss GmbH for three different substrates: i) the untreated polyethylene

naphthalate (PEN) Teonex Q83 from DuPont Teijin Films), ii) the Printed Electronics Limited (PEL) 60 with micro-porous surface treatment and iii) silicon wafer.

Dispersive and polar components measurements

The Owens, Wendt, Rabel and Kaelble (OWRK) method, based on Young's equation (see Eq.3.7) was used to evaluate the surface free energy of each substrate. It uses the following equation:

$$\gamma_{LV}\left[1 + cos(\theta)\right] = 2\left(\sqrt{\gamma_{SV}^{d}\,\gamma_{LV}^{d}} + \sqrt{\gamma_{SV}^{p}\,\gamma_{LV}^{p}}\right) \tag{3.30}$$

where the exponent d means disperse and p means polar.

For the measurements of contact angles, two known liquids, that is, distilled water, and diiodomethane have been used. The specifications of their surface tension and components can be found in [99] and have been reported in Table 3.1.

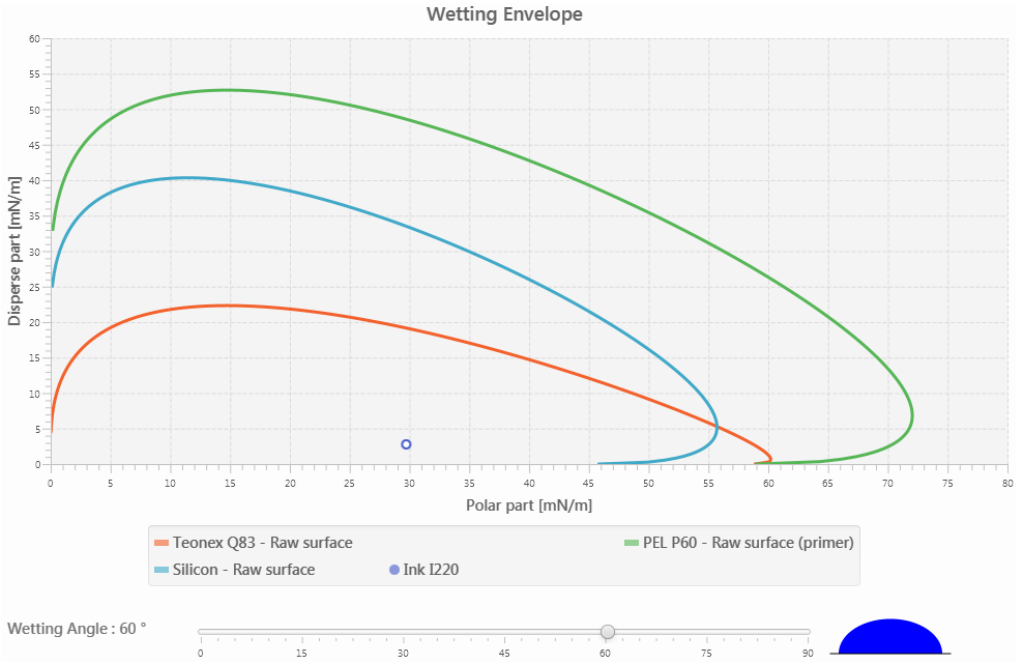


Fig. 3.16 Wetting envelope for three different substrates: i) the Teonex Q83 PEN, ii) the PEL 60 and iii) a silicon wafer.

Results are reported in Fig.3.16 for all substrates. Dispersive components are plotted along the y-axis against polar components along the x-axis. The envelope is

Table 3.1 Measured, calculated and reported (from [99]) surface tensions and components of the test liquids and the dielectric ink.

Material	Surface tension [mN/m]		
	γ_{LV}	γ^p_{LV}	γ^d_{LV}
Dielectric ink InkA-I220	32.5	29.73	2.77
Distilled water	72.8	51.0	21.8
Diiodomethane	50.8	0	50.8

Table 3.2 Measured and calculated surface tensions and components of the three substrates.

Material	Surface tension [mN/m]		
	γ_{SV}	γ^p_{SV}	γ^d_{SV}
PEL 60 coated foil	64.51 ± 2.25	20.04 ± 1.52	44.12 ± 0.73
PEN Q83 uncoated foil	44.04 ± 0.66	1.93 ± 0.17	42.11 ± 0.48
Silicon wafer	49.72 ± 4.40	15.44 ± 2.04	34.27 ± 2.36

defined using the OWRK method solved for the case of a contact angle of 60°, which is the minimum analysed with Surface Evolver. The area bounded by the *x*-*y* axes and the three curves is less than 60° and that outside this boundary is greater than 60°. It can be seen that the dielectric ink InkA-I220 perfectly wets all the tested substrates with a CA well below 60°. All the measured and calculated surface tensions have been reported in Table.3.1 and 3.2.

3.7.2 Printing of the HF antenna coil

The HF antenna coil shown in Fig.3.17 (d), has been inkjet-printed on the Teonex Q83 PEN substrate with 125 μm of thickness. The latter has been cleaned by immersion in isopropanol and deionized water and subsequently dried in an oven at 150 °C for 1 h. After that, the PEN foil has been plasma treated in order to modify its surface, resulting in an improvement of wettability for the conductive ink onto the substrate.

The conductive ink (Sicrys I30EG-1 from PVNanoCell) is based on single-crystal silver nanoparticles (30% by weight) in ethylene glycol (EG). A custom printer with a RICOH MH5440 printhead with 7pL drop volume and native resolution of 150 dpi has been used. Two rows out of four were used to print the conductive layer in order to have a resolution of 300 dpi.

Printing was performed with a custom multipass algorithm (original image unraveled in four random images that recreate the original one when superposed) for improving layer homogeneity avoiding coalescence effects between drops. The multipass algorithm randomizes the nozzles to be used in order to minimize the effects of malfunctioning nozzles.

Intermediate thermal curing of 1 minute have been performed in order to improve the multilayer printing and avoid the spilling of the ink. A detail of the antenna coil is shown in the bottom side of Fig.3.17 (d) where layers are made up of small droplets characteristic of the inkjet printing. A final thermal curing has been performed in a oven at 180°C for 30 minutes.

The contact angle of the lyophilic conductive structure has been measured with the GH11 Drop Shape Analysis System of Krüss GmbH. Measured values, performed under ambient conditions (temperature of 20°C) span from 19 to 21° as shown in Fig.3.17 (c). An average value of 20° has been used for all simulations performed with Surface Evolver.

3.7.3 Chip dewetting and encapsulation

The chip dewetting test has been performed by drawn 10 μL of dielectric ink along with the chip (2.25 mm^2) using an adjustable microliter syringe. After that, the syringe has been agitated for encapsulating as much as possible the chip into the dielectric ink. Subsequently, the droplet has been delivered onto an untreated PEN substrate (Teonex Q83) leading to the situation shown in Fig.3.17 (e) in which the dielectric ink spreads largely over the substrate as one may expect according to the wetting envelope of Fig.3.16.

This test demonstrated the need of a substrate coating in order to increase the contact angle to at least 60 to 70°. For this purpose, the FluoroPel PFC1601V ink from Cytonix Corporation has been used. This ink is a one percent fluoropolymer solution in a fluorosolvent.

As for the printing of the antenna coil, the Q83 PEN substrate has been cleaned by immersion in isopropanol and deionized water and subsequently dried in an oven at 150 °C for 1 h. After that, the PEN foil has been plasma treated in order to modify its surface. Subsequently, the FluoroPel PFC1601V ink has been spin coated with a specific speed profile where the maximum one was 1600 rpm. The entire cycle lasts

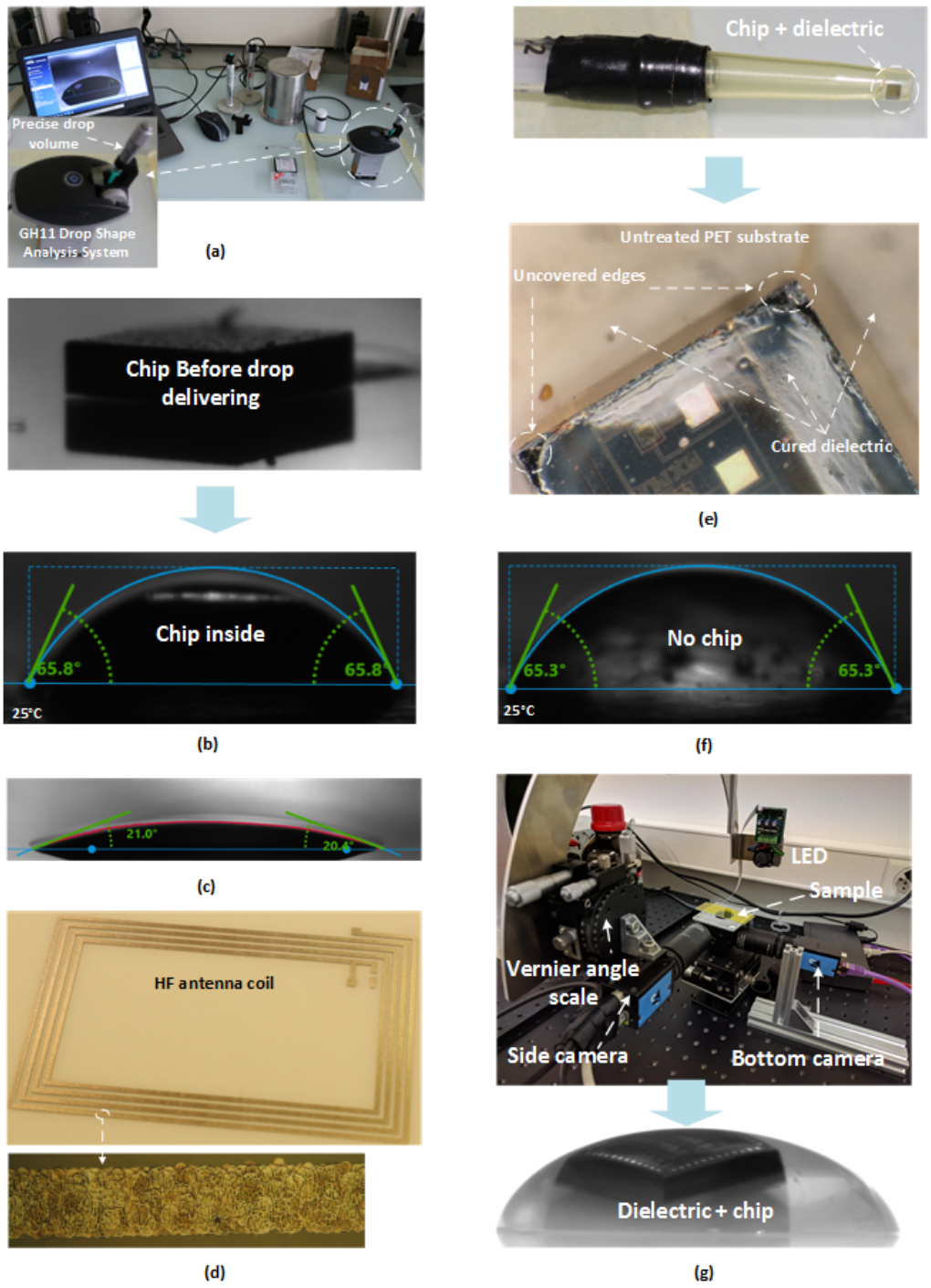


Fig. 3.17 (a) Measurement setup with PC, GH11 Drop Shape Analysisi system, distilled water and diiodomethane. (b) Chip (before) and chip + dielectric (after delivering) interaction onto the coated Q83 PEN substrate. (d) Printed HF antenna coil with Ag-based conductive ink and detail of the inkjet printed structure. (e) Photomicrograph of a test IC with dielectric ink after the curing step. Contact angle measurement of the dielectric ink over: the Ag antenna contact (c) and the coated Q83 PEN substrate (f). Droplet shape image acquisition system with chip encapsulated into a dielectric droplet.

30 seconds. After that, the coated substrate has been heated in a oven at 180°C for 30 minutes.

Contact angle measurements have been performed once again with the GH11 Drop Shape Analysis System. Results show an increased CA between 65 and 66° which is in the expected range according to the supplier specification. Measurements have been performed with and without the chip leading to approximately the same value, that is 65.8 and 65.3° as shown in Fig.3.17 (b) and (f).

The test chip has been deposited over the coated substrate and subsequently a drop of dielectric has been delivered completely covering the chip and spreading on the surrounding substrate until equilibrium. The CAs measurement have been performed using the height and width method. The droplet shape at equilibrium is a spherical cap as expected and predicted during the numerical analysis. The complete wetting of the chip was also expected according to the wetting envelope of the silicon substrate shown in Fig.3.16.

Using again the adjustable microliter syringe, droplets of dielectric with the encapsulated chip have been deposited over the coated substrate. After that, using a specific setup, shown in Fig.3.17 (g), for acquiring droplet shape images has been used. A CCD camera mounted on a vernier angle scale faces a controllable (in timing) LED, with the droplet placed in between. The camera and LED are trigerred by a FPGA, allowing for fine tuning of the lighting conditions. A bottom camera can be used for the analysis of the alignment of the chip with respect to the pad of the antenna.

In the bottom side of Fig.3.17 (g), a test chip encapsulated into the droplet can be clearly seen. The size of the chip is 2.25 mm^2 with a droplet volume of approximately 10 μL. Some samples have been subsequently cured using an UV treatment with 150 mJ/cm2 and a wavelength between 280 and 320nm.

3.8 Summary

In this chapter the droplet shape after surface minimization has been investigated. Simulation results show that the amount of volume plays an important role for the self-positioning of the DS-RFIC. Large quantity of the dielectric ink are required to

avoid the chip dewetting (at the corner). However, the larger the volume, the more important is the misalignment.

The wetting contrast between the pad of the antenna and the surrounding substrate is a fundamental parameter. Simulation results show that a perfect confinement (very high contact angle on the substrate) leads to subsequent complex printing step for closing the antenna loop. On the other hand, a lower contact angle allows the spreading of the droplet over the substrate relaxing the curvature.

A working map of CA and ink volume has been defined showing that at least two times the minimum volume is required for completely encapsulating the chip on the substrate. However, high-coupling impedance mainly due to the relatively large thickness of the dielectric material are expected, therefore electrical performances need to be evaluated.

Experimental tests show that at equilibrium, droplets have a spherical cap shape as initially predicted. This is of a great importance for validating the Surface Evolver simulations.

The partial dewetting has been selected for further investigation (next chapter).

Chapter 4

Capacitive coupling and dielectric stacked structure

4.1 Introduction

The capacitive coupling is mainly known as an alternative technique to the inductive wireless power transfer. The main driving factors for the development of this technology are: the reduced implementation costs, lower radiated EMI (Electromagnetic Interference), lower power losses, ability to transfer power across metal barriers and high density interconnection capability (IC 3D integration) [100].

A capacitive coupling is established through the electrostatic induction (varying electric field) which is done, in most common applications, between metallic plates forming a parallel plate capacitor. Using this method, the wireless power transfer (WPT) has the same limitations under which regular capacitors are subjected, that is, smaller plates area and greater distances between them lead to lower capacitances and thus higher impedances. For this reason, to have better efficiencies, distances between parallel plates is normally lower than a millimeter.

Many applications involving the capacitive power transfer (CPT) exists today, to mention just a few: biomedical devices [101], electric vehicle charging applications [102], inter-chip communication [103, 104], and wireless wafer-level testing for automatic test equipment (ATE) [105].

To optimize the amount of power transferred, an inductor is usually connected in series with the coupling capacitors [13, 102, 106]. In addition, the surfaces of plates, are normally covered (or coated) with dielectric materials in order to provide: i) electrical isolation and ii) increased capacitance by means of relative permittivity ε_r higher than 1.

In this chapter, an in-depth analysis of the capacitive coupling, created between the antenna coil and the DS-RFIC, is performed. The analysis has been carried out in three steps which can be summarized as it follows: i) mathematical modeling through an in-depth impedance analysis, ii) simulation of ideal cases for finding boundary behaviours and iii) simulations using the minimized surfaces (from chapter 3) through FEA analysis.

4.2 Capacitive coupling analysis

The transponder electrical model has been modified in order to consider the coupling as well as the cross-coupling capacitors created by the new fabrication approach. For the convenience of analysis, the circuit of Fig.3.5 has been redrawn as shown in Fig.4.1 (a).

For the detailed analysis of this model the voltage V_A and the current I_a are considered as independent variables. In this case, the circuit can be modeled using the inverse hybrid parameters, also called g-parameters as shown in Fig.4.2.

The g-equivalent two-port circuit is characterized by the following set of equations:

$$\begin{bmatrix} I_A \\ V_L \end{bmatrix} = \begin{bmatrix} g_{11} & g_{12} \\ g_{21} & g_{22} \end{bmatrix} \begin{bmatrix} V_A \\ I_a \end{bmatrix} \tag{4.1}$$

where the first parameter is g_{11} and it can be expressed by:

$$g_{11} = \frac{I_A}{V_A}\Big|_{I_a=0} \tag{4.2}$$

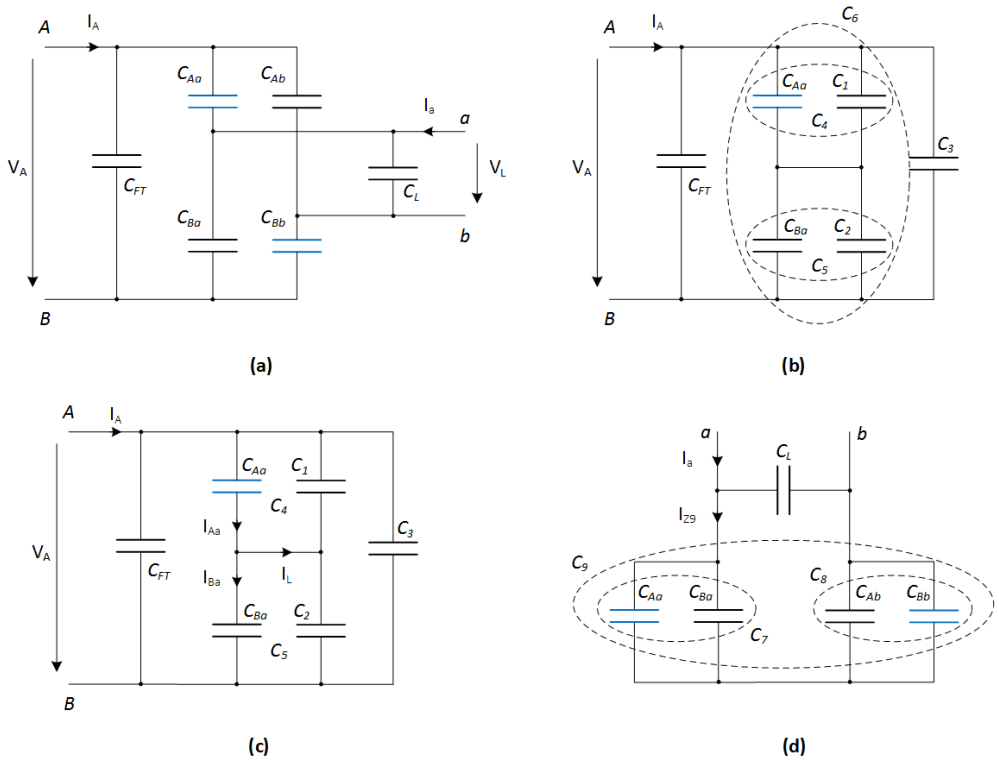


Fig. 4.1 (a) Electrical model of the capacitive coupling with main capacitors (C_{Aa} and C_{Bb}) and cross-coupling capacitors (C_{Ab} and C_{Ba}). (b) Modified electrical model for impedance analysis. The bridge network is modified using the $Y-\Delta$ transform. (c) Nodal analysis with KCL for determining g-parameters with input open-circuit conditions. (d) Modified electrical model for determining g-parameters with input short-circuit conditions.

The current I_A needs to be defined in terms of total impedance seen from the points $A-B$. As can be seen in Fig.4.1 (a), the coupling circuit is formed by a bridge network. The latter can be simplified using the $Y-\Delta$ transform leading to three new impedances connected in a more convenient way as shown in Fig.4.1 (b).

The values of these new impedances are expressed by:

$$Z_1 = \frac{Z_{Bb}\,Z_{Ab} + Z_{Ab}\,Z_L + Z_L Z_{Bb}}{Z_{Bb}} \tag{4.3}$$

$$Z_2 = \frac{Z_{Bb}\,Z_{Ab} + Z_{Ab}\,Z_L + Z_L Z_{Bb}}{Z_{Ab}} \tag{4.4}$$

$$Z_3 = \frac{Z_{Bb}\,Z_{Ab} + Z_{Ab}\,Z_L + Z_L Z_{Bb}}{Z_L} \tag{4.5}$$

At this point, the total impedance Z_{AB} can be expressed in the following way:

$$Z_{AB} = \frac{V_A}{I_A} = \frac{1}{\frac{1}{Z_6} + \frac{1}{F_{FT}} + \frac{1}{Z_3}} \tag{4.6}$$

where Z_6 is the impedance formed by $\left(C_{Aa}+C_1\right)//\left(C_{Ba}+C_2\right)$ as shown in Fig.4.1 (b) with dashed lines.

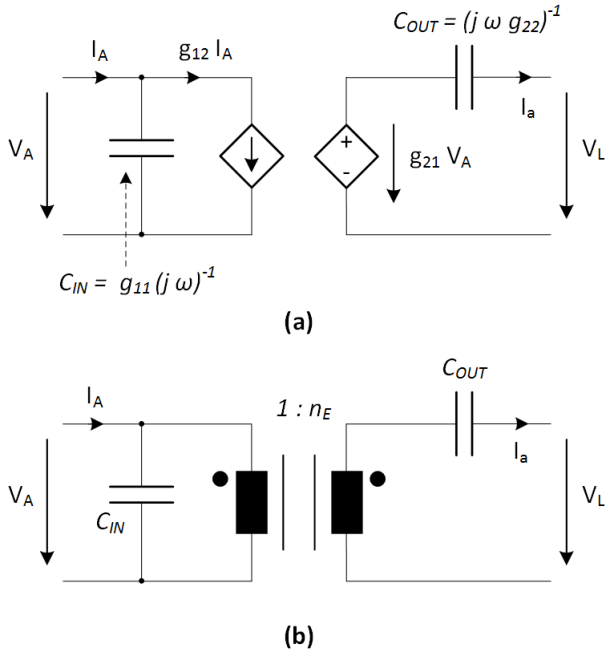


Fig. 4.2 Capacitive coupling two-ports equivalent circuit using g-parameters. The voltage V_A and current I_a are considered as independent variables whereas current I_A and voltage V_L are dependent variables (a). Equivalent model using a step-down transformer as proposed by [13] (b).

The parameter g_{11} can be defied using Eq. 4.6 and 4.2. However, is more interesting to directly express the input capacitance C_{IN}:

$$\begin{aligned} C_{IN} &= \frac{g_{11}}{j\,\omega} = \frac{1}{j\,\omega\,Z_{AB}} \\ &= \frac{\left[C_{FT}\,\left(C_{Bb}\,C_L + C_{Ba}\,(C_{Bb} + C_L)\right) + C_{Aa}\,(...) + C_{Ab}\,[...]\right]}{C_{Ba}(C_{Bb} + C_L) + C_{Bb}\,C_L + C_{Ab}\,(C_{Ba} + C_L) + C_{Aa}\,\{...\}} \end{aligned} \tag{4.7}$$

where:

$$(...) = C_{Bb}\,C_{FT} + C_{Ab}\,(C_{Ba} + C_{Bb} + C_{FT}) + C_L\,(C_{Bb} + C_{FT}) + C_{Ba}\,(C_{Bb} + C_L) \tag{4.8}$$

$$[...] = (C_{Bb} + C_{FT})\,C_L + C_{Ba}\,(C_{Bb} + C_{FT} + C_L) \tag{4.9}$$

$$\{...\} = C_{Ab} + C_{Bb} + C_L \tag{4.10}$$

The second parameter is g_{21} and is defined by:

$$g_{21} = \frac{V_L}{V_A}\Big|_{I_A=0} \tag{4.11}$$

In this case, the load voltage V_L needs to be defined in terms of the input voltage V_A. The latter is used to define the current flowing through Z_4 and Z_5. As shown in Fig.4.1 (c), these two currents are subtracted forming the current of Z_L (the reactance of the load capacitance) which can be finally used for determining the load voltage V_L and hence g_{21}:

$$\begin{aligned} g_{21} &= \frac{Z_L}{Z_6}\left(\frac{Z_4}{Z_{Aa}} - \frac{Z_5}{Z_{Ba}}\right) \\ &= \frac{C_{Aa}\,C_{Bb} - C_{Ab}\,C_{Ba}}{C_{Ab}\,(C_{Aa} + C_{Ba}) + C_{Bb}\,(C_{Aa} + C_{Ba}) + C_L\,(...)} \end{aligned} \tag{4.12}$$

where:

$$(...) = C_{Aa} + C_{Ab} + C_{Ba} + C_{Bb} \tag{4.13}$$

The third parameter is g_{12} and is defined by:

$$g_{12} = \frac{I_A}{I_a}\Big|_{V_A=0} \tag{4.14}$$

The short-circuit condition (V_A = 0) at the input leads to the simplified circuit shown in Fig.4.1 (d). The total impedance seen from the points $a-b$ is expressed by:

$$Z_{ab} = \left[(Z_{Aa} \,//\, Z_{Ba}) + (Z_{Ab} \,//\, Z_{Bb})\right] // Z_L \tag{4.15}$$

The current I_A can be expressed by performing the KCL at the node A taking into account the current I_{Aa} and I_{Ab}.

$$\begin{aligned} g_{12} &= \frac{Z_L}{Z_6}\left(\frac{Z_4}{Z_{Aa}} - \frac{Z_5}{Z_{Ba}}\right) \\ &= \frac{C_{Aa}\,C_{Bb} - C_{Ab}\,C_{Ba}}{C_{Ab}\,(C_{Aa} + C_{Ba}) + C_{Bb}\,(C_{Aa} + C_{Ba}) + C_L\,(...)} \end{aligned} \tag{4.16}$$

where:

$$(...) = C_{Aa} + C_{Ab} + C_{Ba} + C_{Bb} \tag{4.17}$$

From Eq.4.12 and 4.16 it turns out that $g_{12} = g_{21}$. In fact the coupling circuit is symmetric.

The last parameter is g_{22} and is defined by:

$$g_{22} = \frac{V_a}{I_a}\Big|_{V_A=0} \tag{4.18}$$

As for the parameter g_{11}, is more interesting to directly define the output capacitance C_{OUT}:

$$\begin{aligned} C_{OUT} &= \frac{1}{j\,\omega g_{22}} = \frac{Z_{ab}}{j\,\omega} \\ &= \frac{C_{Ab}\,(C_{Aa} + C_{Ba}) + C_{Bb}\,(C_{Aa} + C_{Ba}) + C_L\,(...)}{C_{Aa} + C_{Ab} + C_{Ba} + C_{Bb}} \end{aligned} \tag{4.19}$$

where:

$$(...) = C_{Aa} + C_{Ab} + C_{Ba} + C_{Bb} \tag{4.20}$$

All the equations reported here above have been developed using standard mathematical and circuit analysis methods. The results are relatively complicated to use and they are not circuit intuitive.

The authors of [13] introduced an elegant technique for analyzing circuits such as the one shown in Fig.4.1 (a). This technique consists in considering the coupling circuit as a capacitive step-down transformer as shown in Fig.4.2 (b) with a coupling coefficient defined by:

$$K_E = \frac{C_{Aa}}{C_{Aa} + C_{Ba}} - \frac{C_{Ab}}{C_{Ab} + C_{Bb}} \tag{4.21}$$

With a perfectly coupled system, cross-capacitors C_{Ab} and C_{Ba} disappear from Eq.4.21 leading to $K_E = 1$. If the cross-coupling capacitors are taken into account, the coupling coefficient will tend to: 0 if all capacitors are equal and -1 if the system is uncoupled and the signal completely passes through the cross-coupling capacitors instead to the main capacitors (C_{Aa} and C_{Bb}).

They also defined two new capacitors:

$$C_X = \frac{C_{Aa}\, C_{Ba}}{C_{Aa} + C_{Ba}} + \frac{C_{Ab}\, C_{Bb}}{C_{Ab} + C_{Bb}} \tag{4.22}$$

$$C_Y = \frac{1}{\dfrac{1}{C_{Aa} + C_{Ba}} + \dfrac{1}{C_{Ab} + C_{Bb}}} \tag{4.23}$$

and one parameter that couples the primary and secondary side of the capacitive transformer with a pseudo-turn ratio:

$$n_E = \frac{K_E\, C_Y}{C_L + C_Y} \tag{4.24}$$

Looking closely to these three equations it can be observed that C_Y corresponds to C_9 in Fig.4.1 (d). Capacitor C_X represents the total capacitance of the coupling system without C_{FT} and C_L. It does not have an equivalent in the g-parameter analysis, however it will be helpful. In fact, thanks to this new set of equations, the g-equivalent circuit of Fig.4.2 can be described in a more convenient way:

$$C_{IN} = \frac{g_{11}}{j\,\omega} = C_{FT} + C_X + \frac{C_L\, C_Y}{C_L + C_Y}\, K_E^2 \tag{4.25}$$

$$C_{OUT} = \frac{1}{j\,\omega\, g_{22}} = C_L + C_Y \tag{4.26}$$

$$n_E = g_{12} = g_{21} = \frac{K_E\, C_Y}{C_L + C_Y} \tag{4.27}$$

4.2.1 Parallel resonance analysis

The analysis of the parallel resonance configuration of the complete model shown in Fig.4.3 (a) requires some transformations to reduce the circuit to a second order system. The latter has been defined in Eq.2.35.

The first step consists in reflecting the impedance of the secondary side of the capacitive transformer to the primary side as shown in Fig.4.3 (b). This can be performed in the following way:

$$R_{L_p} = \frac{R_L}{n_E^2} \tag{4.28}$$

$$C_{OUT_p} = C_{OUT}\, n_E^2 \tag{4.29}$$

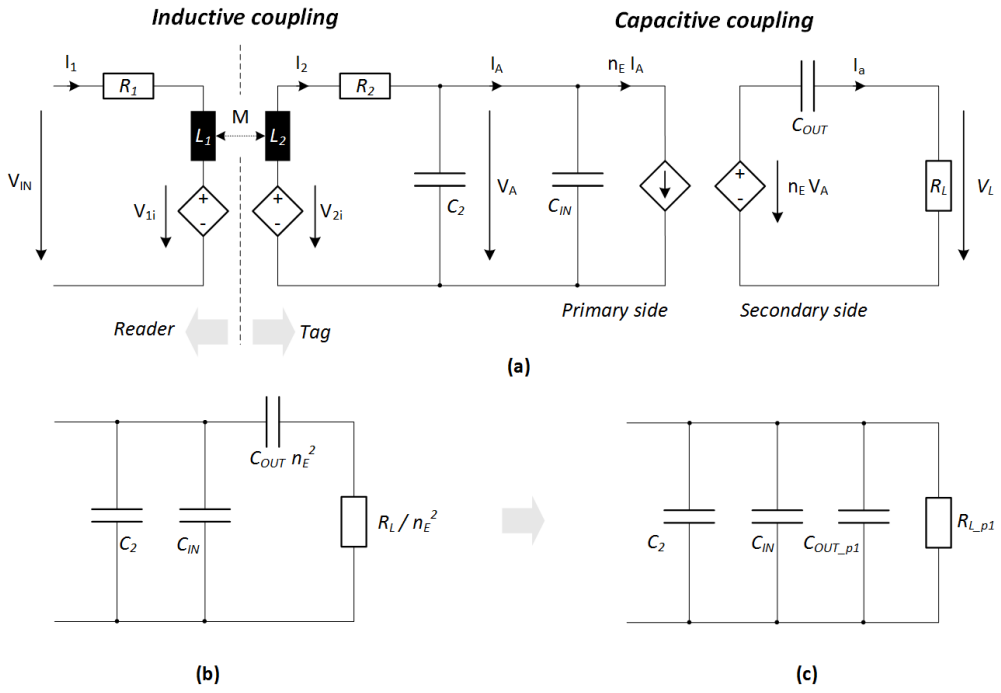


Fig. 4.3 Complete model with inductive (reader to tag) and capacitive coupling (a). Secondary side impedance of the capacitive transformer reflected to the primary side (b). Series to parallel transformation (c).

In the second step, a series to parallel impedance conversion is performed to merge all the capacitors together as shown in Fig.4.3 (c).

$$R_{L_{p1}} = \left(1 + Q_{sec}^2\right) \frac{R_L}{n_E^2} \tag{4.30}$$

$$C_{OUT_{p1}} = \frac{Q_{sec}^2}{1 + Q_{sec}^2} C_{OUT}\, n_E^2 \tag{4.31}$$

where Q_{sec} is the quality factor of the secondary side which is calculated as it follows:

$$Q_{sec} = \frac{1}{\omega_0\, R_L\, C_{OUT}} \tag{4.32}$$

At this point, the total parallel capacitance becomes:

$$C_{TOT_p} = C_2 + C_{IN} + C_{OUT_{p1}} \tag{4.33}$$

The value of C_2 needs to be calculated in order to tune the transponder at the resonance frequency. This can be done using Eq.2.34 where the load resistor R_L is replaced by the $R_{L_{p1}}$ and the capacitor C_L is replaced by $C_{IN} + C_{OUT_{p1}}$. The same for Eq.2.35 in which capacitor C_{PAR} is replaced by C_{TOT_p}.

$$C_2 = \frac{1}{2\,\omega_0^2\, L_2}\left(1 + \sqrt{1 - \frac{4\,\omega_0^2\, L_2^2}{R_{L_{p1}}^2}}\right) - \left(C_{IN} + C_{OUT_{p1}}\right) \tag{4.34}$$

$$V_A = \frac{j\,\omega\, M\, i_1 \frac{1}{C_{TOT_p}\, L_2}}{(j\,\omega)^2 + j\,\omega\left(\frac{1}{R_{L_{p1}}\, C_{TOT_p}} + \frac{R_2}{L_2}\right) + \left(\frac{R_2}{R_{L_{p1}}} + 1\right) \frac{1}{C_{TOT\,p}\, L_2}} \tag{4.35}$$

Considering again the complete model of Fig.4.3 (a), the load voltage V_L can be calculated in the following way:

$$V_L = V_A\, n_E \frac{R_L}{X_{COUT} + R_L} \tag{4.36}$$

Electrical performances have been evaluated based on a standard RFID system configuration which is made up of: i) a proximity coupling device (PCD) assembly 1 acting as a reader antenna coil according to the ISO/IEC 10373 standard [84] and ii) an RFID tags antenna coil complying with the ISO/IEC-14443 (proximity cards) class 1 standard [81], also called proximity integrated circuit card (PICC). This RFID system is shown in Fig.4.5 (a) and it has been characterized by carefully analyzing both the magnetic field strength and the mutual inductance.

Magnetic field strength

RFID tags should operate between minimum and maximum magnetic field strength specifications. According to the ISO/IEC 14443 standard, the H_{min} is defined to 1.5 A_{rms}/m and H_{max} to 7.5 A_{rms}/m. These limits are defined along the axial direction (in z) from the center of the PCD antenna coil.

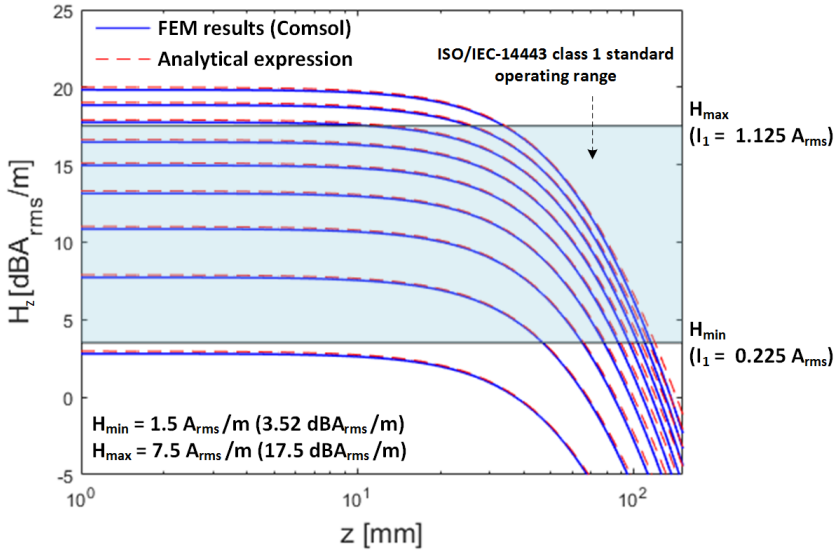


Fig. 4.4 Magnetic field strength $\vec{H}$ along the axial distance from the center of the PCD antenna coil for different current levels.

The magnetic field strength can be calculated, for a PCD assembly 1 antenna coil (single turn circular coil of 150 mm in diameter), using Eq.2.6 which can be rewritten setting $x_P = y_P = 0$:

$$\vec{H} = \frac{I\,a}{4\,\pi}\int_0^{2\pi}\frac{\left[z_P\,cos(\theta)\right]\hat{\mathbf{i}}+\left[z_P\,sin(\theta)\right]\hat{\mathbf{j}}+a\,\hat{\mathbf{k}}}{\left(a^2\,+\,z_P^2\right)^{3/2}}\,d\theta \tag{4.37}$$

Carrying out the integration, the x and y components are zero:

$$H_x = \frac{I\,a\,z_P}{4\,\pi\,\left(a^2\,+\,z_P^2\right)^{3/2}}\,sin(\theta)\Big|_0^{2\pi} = 0 \tag{4.38}$$

$$H_y = -\frac{I\,a\,z_P}{4\,\pi\,\left(a^2\,+\,z_P^2\right)^{3/2}}\,cos(\theta)\Big|_0^{2\pi} = 0 \tag{4.39}$$

and the z component is:

$$H_z = \frac{I\,a^2}{4\,\pi\,\left(a^2\,+\,z_P^2\right)^{3/2}}\,\theta\,\Big|_0^{2\pi} = \frac{I\,a^2}{2\,\left(a^2\,+\,z_P^2\right)^{3/2}} \tag{4.40}$$

Values of H_z are shown in Fig.4.4 for different current levels up to 150 mm of distance from the surface of the PCD antenna coil. These values have been compared with Comsol Multiphysics using a static magnetic field analysis. In this case, the following set of equations is considered:

$$\nabla\times\vec{H} = J_{ext} + j\omega\vec{D} \tag{4.41}$$

$$\vec{B} = \nabla\times\vec{A} \tag{4.42}$$

where $j\omega\vec{D}$ is the displacement current which contribution can be neglected in the near field with conductive media, J_{ext} is the external current density applied to the PCD antenna coil and the magnetic vector potential $\vec{A}$ is the unknown field quantity.

Very close to the PCD antenna coil, magnetic field strengths are almost constant but they fall rapidly as the distance increase. In free space, the decay of H_z is approximately 60dB per decade in the near field. It is worth noting that standard RFID tags should operate up to approximately 104 mm under H_{max} condition using the above mentioned PCD antenna coil.

Currents above 1.125 A_{rms} exceeds the standard operating range, therefore, the rest of simulations of this chapter has been performed with reader currents compiling with H_{max}.

Mutual inductance

In order to calculate the mutual inductance M of the RFID system and simplify the model, current density distributions inside conductive wires (skin effect) have been neglected. As shown in Fig.4.5 (a), both reader and transponder antenna coils have been modeled using 1D geometry elements forming closed loops in a 3D surrounding space (air environment).

Recalling Eq.2.12 and 2.11 from chapter 2, the mutual inductance M can be calculated as it follows:

$$M = \frac{\oint_{\partial S_2} A_{2x}t_x + A_{2y}t_y + A_{2z}t_z \, dl}{I_1} \tag{4.43}$$

where $\vec{t}$ is the unit tangent vector of 1D segments constituting the geometry of the transponder and dl is an infinitesimal line element.

Values of M are shown in Fig.4.5 (b) for distances from 1 to 100 mm. As already explained in chapter 2, M depends only on the geometric configuration between L_1 and L_2.

The simplified approach has been compared with FastHenry which model has been defined with a cross-sectional spatial discretization of 50 filaments. Results show relative deviations, between the two models, below 7%.

Reference configuration and voltage normalization

A reference RFID system configuration has been taken into account for simulations of this chapter. This configuration consists in placing the center of the antenna coil of the tag (without capacitive coupling) in the axial direction at 37.5 mm from the surface of the PCD antenna coil.

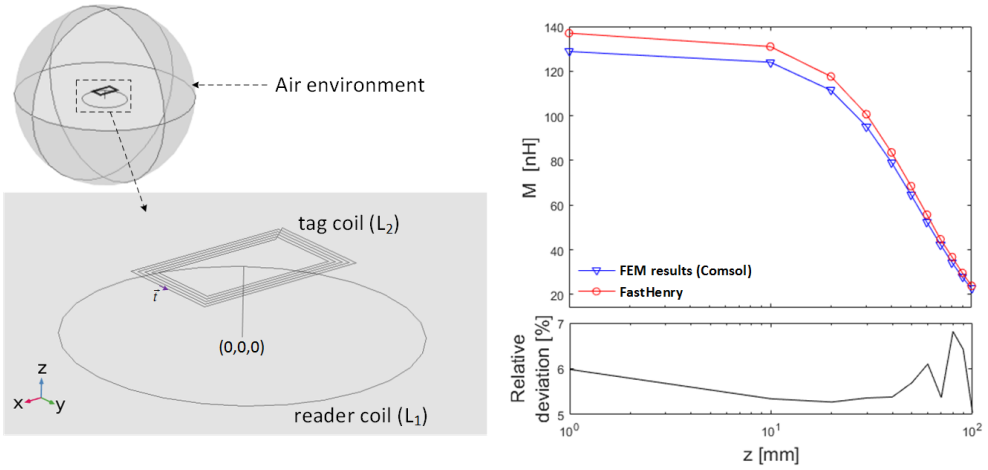


Fig. 4.5 (a) RFID system made up of a single turn, circular antenna coil complying with the ISO/IEC 10373 standard and a transponder complying with the ISO/IEC-14443 (proximity cards) class 1 standard. (b) Mutual inductance M in the proximity operating range for i) a simplified 1D model in Comsol Multiphysics and ii) a FastHenry 3D model with a cross-sectional spatial discretization of 50 filaments.

This particular case is interesting for two main reasons: i) in terms of distances, it is compatible with proximity applications such as public transport ticketing, access cards and contactless payment cards, ii) as shown in Fig.4.6, the magnetic field strength is almost constant over the entire surface of antenna coils complying with the ISO/IEC-14443 (proximity cards) class 1 standard. Following that, the integral of Eq.2.12 can be simplified and becomes:

$$M = \frac{\mu_0 \, \mu_r \, H_z \, A_{eff}}{I_1} \tag{4.44}$$

where, for a rectangular shape, the effective area A_{eff} of the transponder coil is:

$$A_{eff} \approx \sum_{i=1}^{N_{turns}} \prod_{j=1}^{2} \left[l_j - \frac{w}{2} - (i - 1) \, 2 \, d \right] \tag{4.45}$$

where w is the width of each segment and d is the mean distance between adjacent segments.

Simulations here following have been normalized considering this reference configuration. The current I_1 has been calculated in order to have minimum power

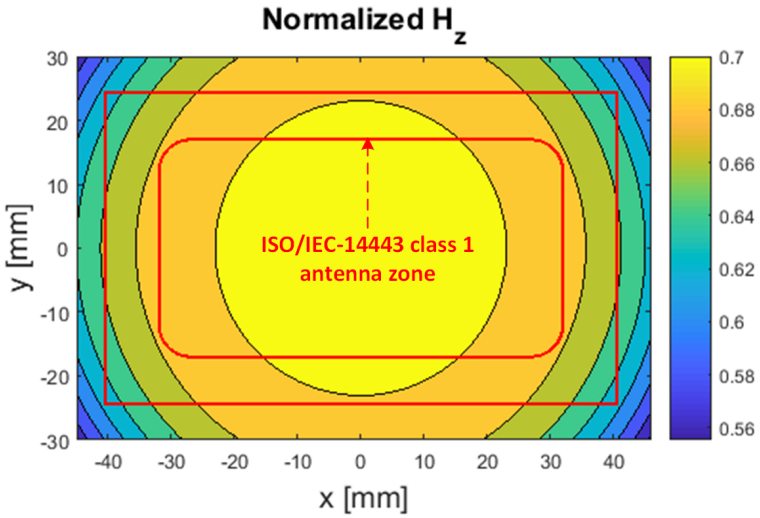


Fig. 4.6 Homogeneous magnetic field strength over the surface of antenna coils complying with the ISO/IEC-14443 (proximity cards) class 1 standard.

requirements in the reader antenna coil. This means that I_1 has been calculated to have H_{min} at $z_P = 37.5$ mm:

$$I_{min,rms} = \frac{2\,H_{min}\left(a^2 + z_p^2\right)}{a^2} \tag{4.46}$$

Frequency shift and voltage attenuation

Simulations of the capacitive coupling have been: i) performed using four perfectly uniform dielectric layers with thickness d_{Aa} and d_{Bb} equal to 1 mm, 100 μm, 10 μm and 1 μm where the last two values are considered to be very challenging considering the nature of the proposed fabrication process, ii) normalized according to the reference configuration explained here above.

At this point of the analysis, the cross-coupling capacitors C_{Ab}, C_{Ba} and C_{FT} have been not been taken into account.

As shown in Fig.4.7 (a), as $C_{Ab} = C_{Ba} = C_C$ decreases, the voltage (normalized according to the reference case) on terminals of the antenna coil of the transponder, is boosted around the resonant frequency. This, at first, seems to be a good point, however, as shown in Fig.4.7 (b) the voltage available at the load impedance is strongly attenuated (up to -48dB) because of the high-coupling impedance. In this

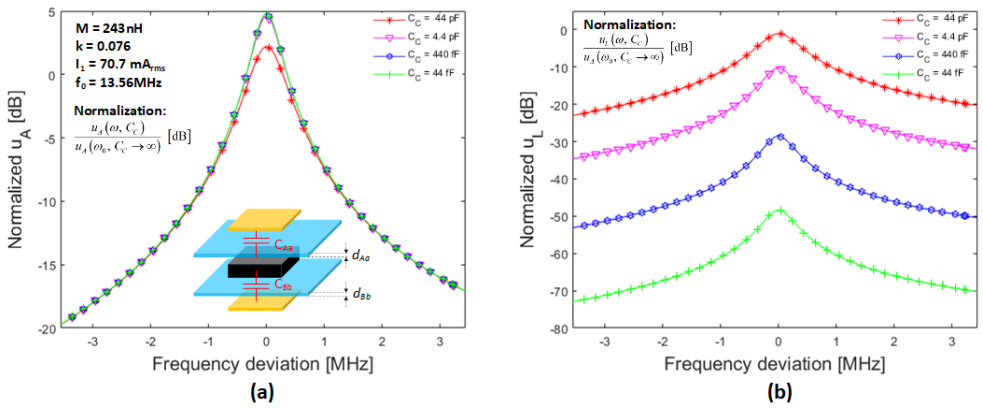


Fig. 4.7 (a) Antenna voltage V_A for three values of $C_{Aa} = C_{Bb} = C_C$ according to Eq.4.35. The value of C_2 is adapted for tuning the transponder at ω_0. (b) Low values of C_C create high attenuation of u_L. For much higher values of C_C, the coupling impedance is so small that can be considered as a short-circuit. Both V_A and V_L are normalized according to the reference case. Unless otherwise specified, numerical values of Table.4.1 have been used.

case, the parallel capacitor C_2 acts as a low impedance path and most of the current flows through it with the result of limiting the working range of the transponder.

For the simulations of Fig.4.7, the value of C_2 has been optimized for each different value of the coupling capacitor C_C leading to a perfectly tuned transponder.

As shown in Fig.4.8 (a), for small coupling capacitors, the optimum value of C_2 (normalized according to the reference case) tends to the value that would be used for a simple RLC circuit, that is, an unloaded transponder. For large coupling capacitors instead, C_2 tends to the value that would be used for a traditional transponder. In fact, the coupling impedance is so small that can be considered as a direct coupling (without capacitive coupling).

As one may expect, for small values of C_C, the load capacitor is isolated from the antenna due to the high-coupling impedance, hence, as shown in Fig.4.8 (b), C_L does not have any effect on the optimum value of C_2. On the other hand, for large values of C_C, the load capacitor affects C_2 according to Eq.2.34.

Nevertheless, considering the nature of the proposed fabrication process, one can expect variations of C_{Aa} and C_{Bb} within a certain range. For this reason, the tuning of the transponder would imply additional fabrication steps such as the measurement of C_{Aa} and C_{Bb} followed by the printing of C_2 or the addition of specific matching networks. This, of course, is not compatible with the ultra low-cost

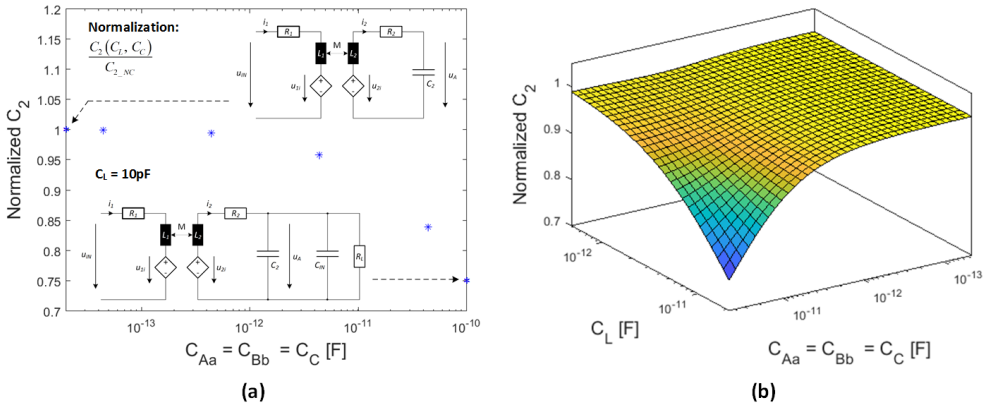


Fig. 4.8 Optimization of C_2 for keeping the transponder tuned to f_0. Small values of the latter move C_2 towards the value that would be used for a simple RLC circuit. Instead, large values of C_C moves C_2 towards the value that would be used in a conventional transponder (without capacitive coupling). Unless otherwise specified, numerical values of Table.4.1 have been used.

concept. In addition, changes in the capacitance of C_2 due to temperature variations or manufacturing tolerances would counterbalance the optimization of C_2.

In simulations of Fig.4.9, the value of C_2 has been kept constant for each value of C_C (without optimization of C_2) leading to the detuning of the transponder which is characterized by a positive or negative frequency shift with respect to f_0 depending on the value of C_2.

For the positive frequency shift case, C_2 has the value that would be used in a conventional transponder (defined as "*direct coupling*"). In fact, the higher the values of C_C, the lower the frequency shift and the voltage attenuation on the load.

For the negative frequency shift case, C_2 has the value that would be used for a "*unloaded*" antenna coil. As for the previous case, the voltage attenuation on the load is minimized for high value of C_C. However, the frequency shift is minimized for very low value of C_C due to their high impedances that almost isolate the chip from the antenna coil.

The load capacitor (C_L) forms a voltage divider along with capacitors C_{Aa} and C_{Bb}, therefore, better RF performances are expected for small values of C_L. In fact, as shown in both Fig.4.10 (b) and (d), the smaller the value of C_L, the lower the load voltage (V_L) attenuation at the resonant frequency. For large value of C_L instead, a low impedance path is created in parallel with R_L leading to strong attenuation.

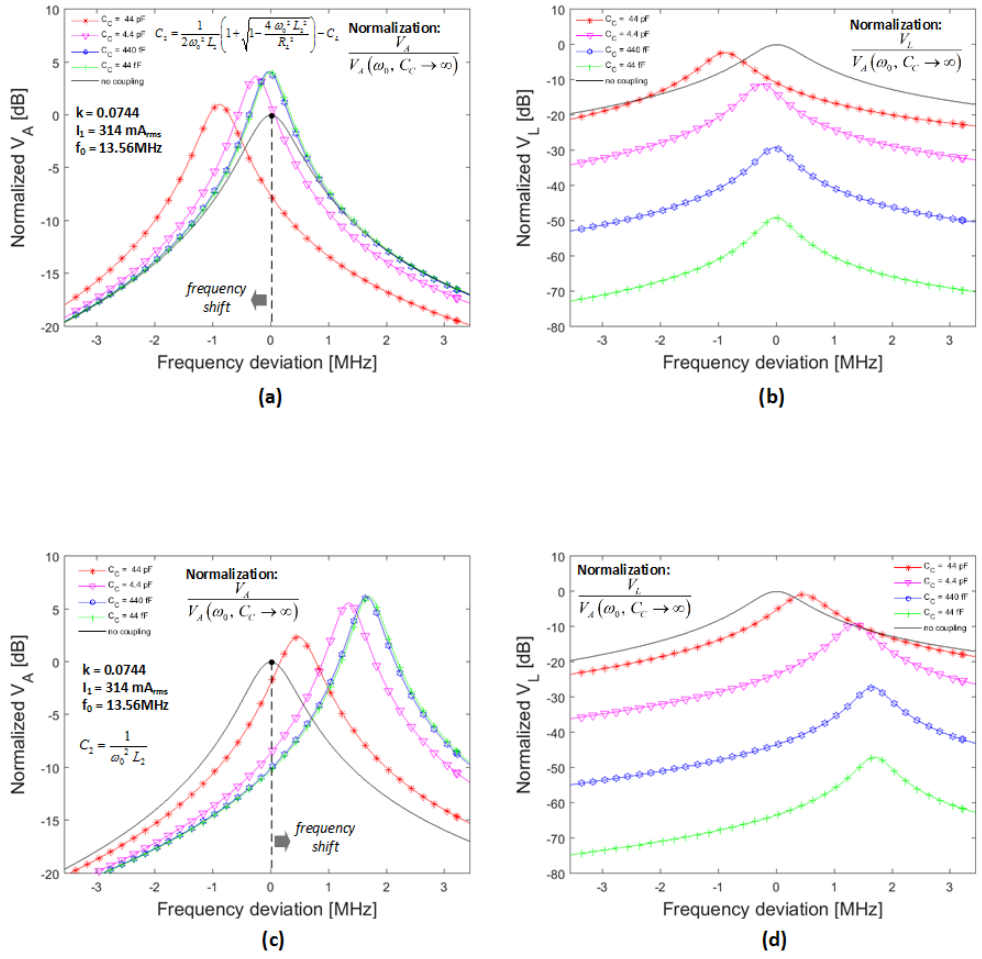


Fig. 4.9 (a) Antenna coil voltage and (b) load voltage. Both with a positive frequency shift. C_2 tuned to the value that would be used without coupling (direct contact).(c) Antenna coil voltage and (d) load voltage. Both with a negative frequency shift. C_2 tuned to the value that would be used in the case of an unloaded antenna. Unless otherwise specified, numerical values of Table.4.1 have been used.

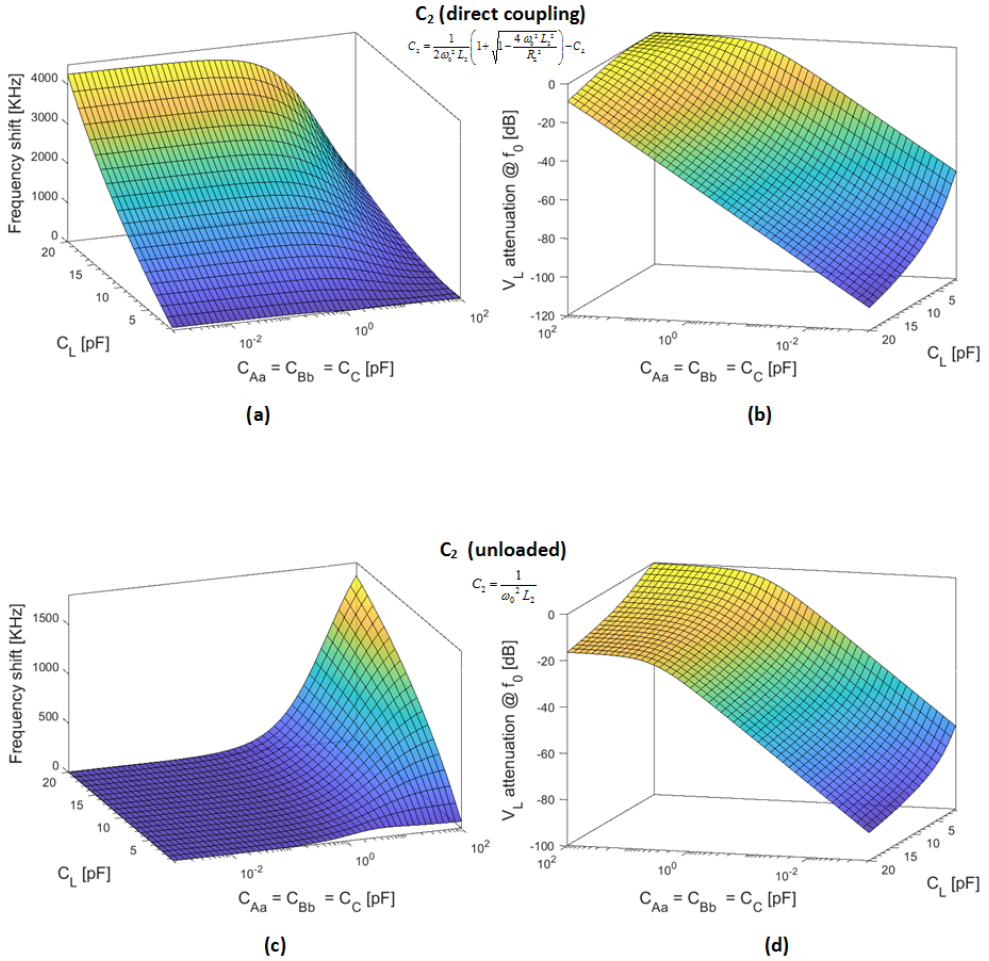


Fig. 4.10 (a) Absolute value of the frequency shift and (b) load voltage attenuation for different values of C_C and C_L and considering the direct contact case. (c) Absolute value of the frequency shift and (b) load voltage attenuation for different values of C_C and C_L and considering the unloaded antenna case. Unless otherwise specified, numerical values of Table.4.1 have been used.

Table 4.1 Numerical values for a typical RFID system complying with the ISO/IEC 14443 and 10373 standards)

Symbol	Description	Value	Unit
f_0	Resonant frequency	13.56	MHz
L_1	Reader (PCD) antenna coil	500	nH
L_2	Tag (PICC) antenna coil	2.9	μH
R_2	Series resistor of L_2	10	Ω
R_L	Load resistor	10	$k\Omega$
C_L	Load capacitor	10	pF
C_2	Parallel capacitor	47	pF
S_{CHIP}	Chip surface	1	mm^2
h_{CHIP}	Chip thickness	500	μm
ε_r	Relative permittivity (100KHz)	5	-

By carefully looking at very high coupling capacitors, the voltage attenuation for the "*unloaded*" case increases more rapidly than the "*direct coupling*" case. This can be explained by the fact that C_2 is larger creating a lower impedance path shunting the load resistor R_L, hence attenuating the voltage V_L.

As shown in Fig.4.10 (c), the frequency shift has a different behavior in comparison to the "*direct coupling*" case. In fact, it remains almost constant regardless of any variation of C_L when C_C is very small. This, as already explained, can be readily understood considering the high impedance of C_C which isolate the load, weakening the effect of C_L.

When the value of C_C reaches few pF, the frequency shift rapidly rump up with the increase of C_L. It can be seen that this rapid increase shows a pick form which can be explained by closely looking at Eq.4.31. In fact, the multiplication of the squared values of Q_{sec} and n_E give rise to this pick form and become important for large values of both C_C and C_L.

In the "*direct coupling*" case instead, the frequency shift is much more sensitive to C_L and it is maximized for very small value of C_C. In fact, when the latter increases, creating a low impedance path that acts as a short circuit, the frequency shift decreases.

Quality factor

Antenna coils of transponders have intrinsic quality factors (without loads) of hundreds or more. These values are mainly governed by the parasitic series resistance of the inductance which can be, as already explained in chapter 2, very low and even below 1Ω depending on the fabrication technology. However, communication protocols with specific numerical bit rates, anti-collision management procedures and signal with imposed standard (rise time, fall time, cutoff time, etc.) need fixed bandwidths reachable with quality factors Q_{2L} well below the intrinsic one. For traditional transponders, often external resistors are used to bring back the quality factor to values of ≈20 for NFC applications and up to ≈ 70 - 80 for ISO/IEC 14443 proximity applications [107].

In the case of this work, any extra component is not compatible with the ultra low-cost approach and thus the quality factor needs to be controlled only by printing steps. One way would be to control the thickness of the antenna coil acting on the value of the series resistance R_2.

As shown in Fig.4.11, the value of Q_{2L} is boosted by the addition of coupling capacitors, reaching values compatible with both NFC and proximity applications. Therefore, another way to control Q_{2L} would be to find a compromise between voltage attenuation and quality factor boost by means of coupling capacitors which could be controlled by increasing or decreasing the amount of the dielectric ink volume.

4.3 Capacitive coupling and dielectric droplet

According to the working map developed in chapter 3, the minimized surface corresponding to the parameters: $h_{CHIP} = 500\mu m$, $S_{CHIP} = 1mm^2$ and volume increase factor $\delta = 2.0$ (worse case), has been employed along with Comsol Multiphysics for extracting coupling and cross-coupling capacitors.

Simulation results are given under the common form of the Maxwell capacitance matrix. The latter describes the relation between the charge of the i^{th} terminal (or conductor) to the voltages of all terminals in the system.

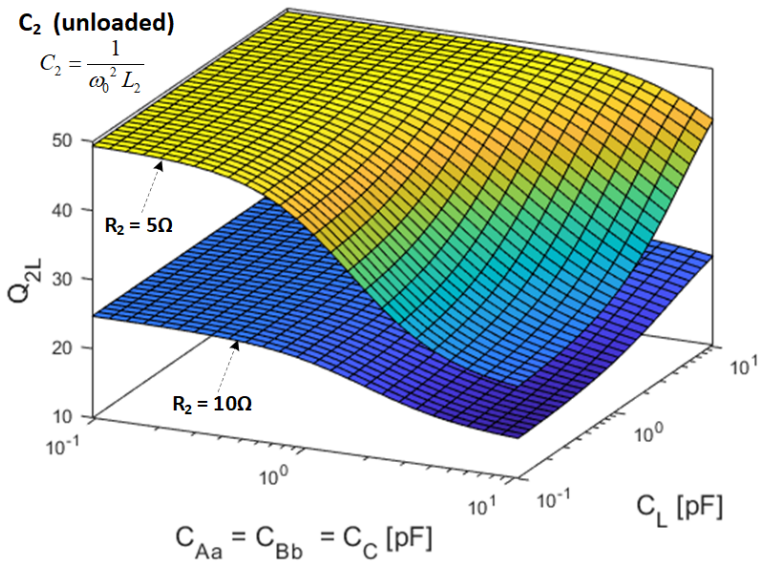


Fig. 4.11 Quality factor Q_{2L} for two values of R_2 with dependence on C_C and C_L. The value of Q_{2L} is boosted by additional low values of coupling capacitors.

$$\begin{bmatrix} Q_1 \\ Q_2 \\ \vdots \\ Q_N \end{bmatrix} = \begin{bmatrix} C_{11} & C_{12} & \cdots & C_{1N} \\ C_{21} & C_{22} & \cdots & C_{2N} \\ \vdots & \vdots & \ddots & \vdots \\ C_{N1} & C_{N2} & \cdots & C_{NN} \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \\ \vdots \\ V_N \end{bmatrix} \tag{4.47}$$

A more interesting way to determine the total charge on terminal 1 is to summing up all the contributions of the self and mutual capacitances. Considering $N = 3$ as an example, the charge Q_1 can be expressed by:

$$\begin{aligned} Q_1 &= C_{m,11}V_1 + C_{m,12}(V_1 - V_2) + C_{m,13}(V_1 - V_3) \\ &= (C_{m,11} + C_{m,12} + C_{m,13})V_1 - C_{m,12}V_2 - C_{m,13}V_3 \end{aligned} \tag{4.48}$$

where for example $C_{m,11}$ is the self-capacitance of terminal 1 and $C_{m,12}$ is the mutual capacitance between terminal 1 and 2. All the self and mutual capacitance can be expressed in a matrix form as it follows:

$$\begin{bmatrix} C_{m,11} & C_{m,12} & \cdots & C_{m,1N} \\ C_{m,21} & C_{m,22} & \cdots & C_{m,2N} \\ \vdots & \vdots & \ddots & \vdots \\ C_{m,N1} & C_{m,N2} & \cdots & C_{m,NN} \end{bmatrix} \tag{4.49}$$

As shown in Fig.4.12 (b), four terminals ($N = 4$) have been defined in order to take into account coupling and cross-coupling capacitors. The terminals can be defined as: terminal 1) the top contact of the antenna coil; terminal 2) the top contact of the DS-RFIC; terminal 3) the bottom contact of the DS-RFIC including the lateral walls of the silicon substrate; terminal 4) the bottom contact of the antenna coil.

Following this, the capacitors defined in the model of Fig.4.1 have been assigned to the coefficients of the mutual capacitance matrix as it follows:

$$\begin{aligned} C_{FT} &= C_{m,14} \\ C_{Aa} &= C_{m,12} \\ C_{Ab} &= C_{m,13} \\ C_{Bb} &= C_{m,43} \\ C_{Ba} &= C_{m,42} \end{aligned} \tag{4.50}$$

The self-capacitances are not taken into account since the ground is considered to be at infinity. In fact, the chip generates its own ground reference internally.

Case study 1: total dewetting

The first case investigated is shown in Fig.4.12 (a) where the minimized surface, which is made up of a set of coordinates representing each vertex of the surface, has been imported from Surface Evolver to Comsol Multiphysics. The droplet is perfectly confined onto the pad of the antenna thanks to the total dewetting of the substrate characterized by a very high contact angle.

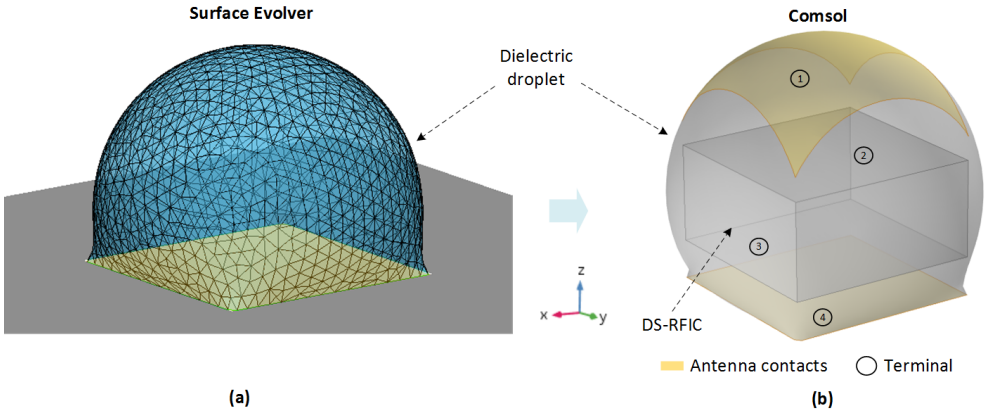


Fig. 4.12 (a) Geometry of the droplet in Surface Evolver representing the total dewetting of the substrate after energy minimization. (b) Geometry imported in Comsol Multiphysics for extracting the mutual capacitance matrix between terminals. The chip has been shifted in x, y and z directions as well as tilted or rotated around them.

This scenario has already been defined to be problematic for two main reasons: i) droplet height and ii) the folded shape of the droplet near the 3L.

For the sake of having a concrete idea of the range of capacitances involved in this case, the DS-RFIC has been integrated into the droplet where it has been shifted in all directions, with respect to an initial position which is shown in Fig.4.12 (b). In addition, the chip has also been tilted and rotated in order to take into account all the possible positions it may assume, along with the droplet, during: i) the self-assembly process (transition between the landing position and the final position over the antenna), ii) the encapsulation position.

By carefully observing the shape of the droplet, it turns out that its height is enough to potentially have the DS-RFIC placed at 90° with respect to the plane of the substrate (vertical position). This, as shown in the simulation results of Fig.4.13 (a), would lead to high-coupling capacitances (extreme values), hence low impedances between the bottom contact of the antenna and the silicon bulk.

It can be observed that, except for the vertical position, most of capacitance values in the first and third quartile are equally distributed around their median with minimum variations. In both cases, median values are in the same order of magnitude.

This is not sufficient to have good electrical performances, in fact as shown in Fig.4.13 (b), high values of C_{Bb} correspond to very low capacitances of C_{Aa} which

in turns lead to high impedances, hence high voltage drops. The same can be stated for C_{Aa}, nevertheless, the highest values of the latter capacitor are one order of magnitude lower than C_{Bb}.

Since the values of cross-coupling capacitors are much lower than the coupling ones, the total capacitance of the series combination of C_{Aa} and C_{Bb}, called C_{ser}, approximately corresponds to the capacitor C_y introduced in the capacitive coupling analysis. As shown in Fig.4.17 (b), C_{ser} is dominated by low values of C_{Aa}. As a consequence of this, the capacitor C_L needs to be kept as low as possible to have a capacitive voltage divider allowing maximum voltage on the load.

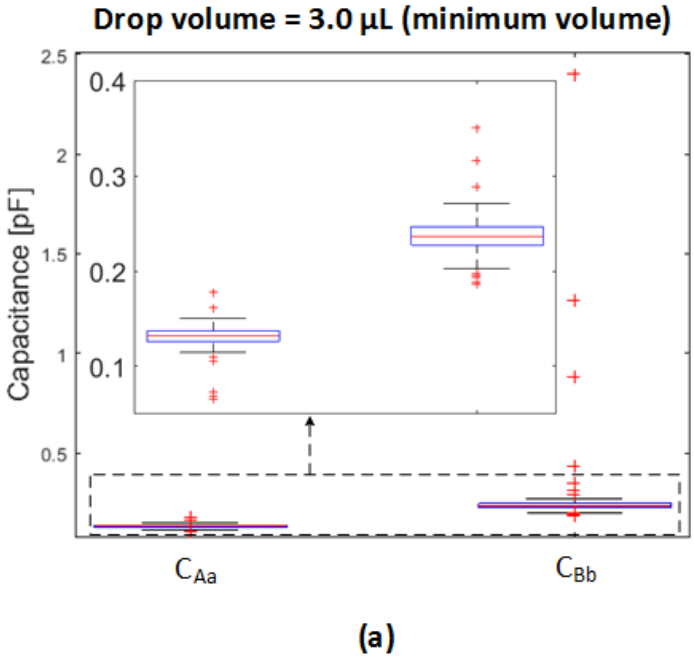
It can be seen that for the vertical position, the capacitor C_{ser} deviates from C_Y since the cross-coupling capacitors are more significant and begin to play a role attenuating further the RF signal.

The complete model of Fig.4.3 has been simulated considering the reference configuration, all extracted values of coupling and cross-coupling capacitances and a typical RFIC impedance. Results reported in Fig.4.14 (a), show a large voltage dispersion with minimum attenuation at the resonant frequency of ≈38 dB with minimum reader current and ≈27 dB with maximum reader current. Both currents are compliant with H_{min} and H_{max} and two values of the parallel capacitor C_2 has been used. In the first case (solid lines), the transponder is tuned to f_0 whereas in the second one (dashed lines), which is clearly not suitable, is completely detuned leading to additional attenuation.

In Fig.4.14 (b) the normalized load voltage, at f_0, has been computed increasing the geometric coupling coefficient k. At the reference distance (37.5 mm), with a maximum current injected into the reader antenna coil and considering upper bound coupling capacitor values, a load voltage amplitude of 2.26 V can be expected. The latter is potentially enough for powering up the circuitry, in standard CMOS technologies (e.g. AMS 0.35 μm), by using a full-wave voltage rectifier circuit.

For lower bound coupling capacitor values instead, the load voltage amplitude is only 814 mV. This requires a voltage rectifier circuit with multiple stages for voltage multiplication.

At closer position with respect to the reader antenna, higher voltages can be expected, reaching amplitudes of 3.68V at 1mm. However, such a distance is not realistic considering packages of both transponder and reader.



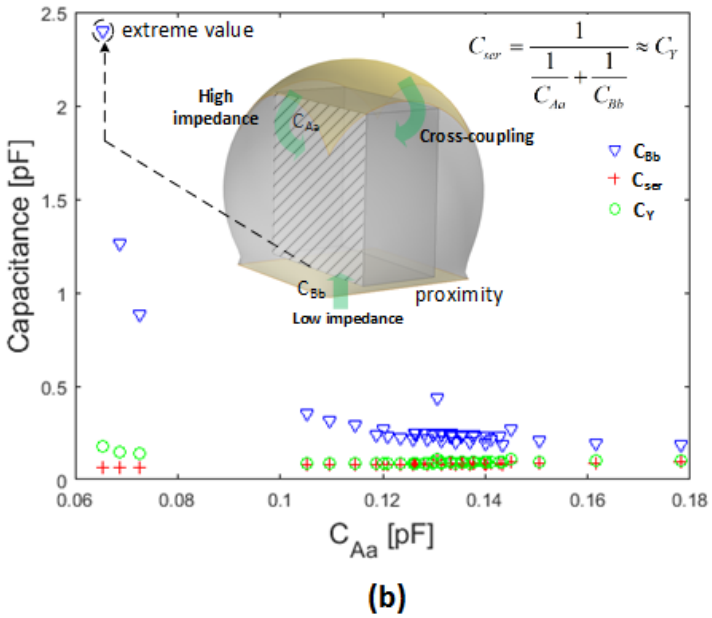


Fig. 4.13 (a) Boxplot showing the capacitance dispersion of C_{Aa} and C_{Bb} for the case of the total dewetting. Values extracted from model show very low coupling capacitances, except for C_{Bb} when the DS-RFIC has a vertical position inside the droplet. (b) Dependence of C_{Aa} and C_{Bb} as well as their series combination showing C_{Aa} as the dominant capacitor is the conduction path.

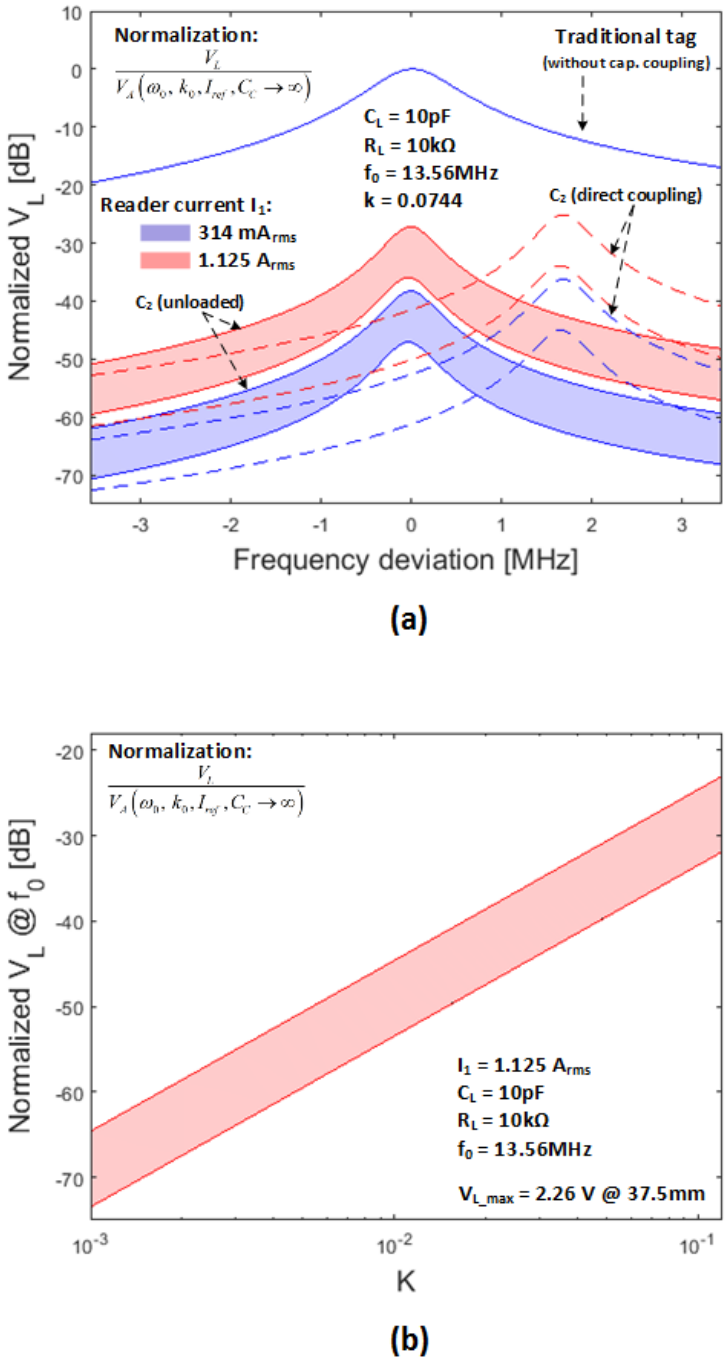


Fig. 4.14 (a) Comparison of a traditional transponder (without capacitive coupling) and the complete model including the extracted set of values of coupling and cross-coupling capacitors for the case of the total dewetting. (b) Load voltage increasing the geometric coupling coefficient k. All simulations normalized according to the reference configuration. Unless otherwise specified, numerical values of Table.4.1 have been used.

As previously mentioned, the capacitor C_L plays an important role, in fact, it creates, along with C_{Aa} and C_{Bb} a voltage divider that strongly affects the voltage available at the input of the DS-RFIC. Indeed, as shown in Fig.4.19 (a), high values of C_L attenuate the load voltage and make it insensitive to the load resistor R_L. In the other hand, lower values of C_L allow higher voltages which are more sensitive R_L, in fact, in this case, the total load impedance is dominated by R_L.

The reduction of C_L is undoubtedly an optimization parameter that strongly depends on i) the dimension of the DS-RFIC and ii) the analog front-end input capacitance.

Case study 2: centered landing position and low CA

The second case taken into account is shown in Fig.4.16 and it represents the droplet homogeneously distributed around the contact of the antenna with a 3L defined by a circle with a relatively low contact angle.

In order to simplify the model and performing parametric simulations, the surface of the droplet has been fitted using the ellipsoid equation which can be expressed, in the Cartesian coordinates system, as it follows:

$$\frac{x^2}{a^2} + \frac{y^2}{b^2} + \frac{z^2}{c^2} = 1 \tag{4.51}$$

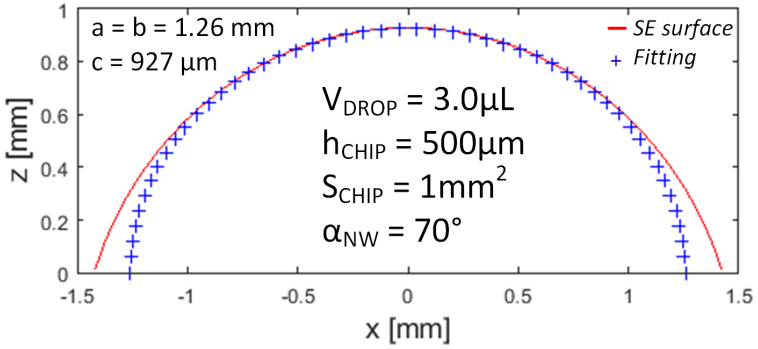


Fig. 4.15 Fitting of the SE surface with an ellipsoid having parameters a, b and c according to Eq.4.51. The cross-sectional view (plane z-x) is at $y = 0$.

As shown in Fig.4.15, the fitting is much better in the above half-section of the droplet while imprecise in the lower part near the 3L. This can be explained by the fact that the ellipsoid (in this specific case an oblate spheroid) does not take into

account the contact angle. A better fit in the above half-section of the droplet is considered to be more important for the extraction of the coupling and cross-coupling capacitors.

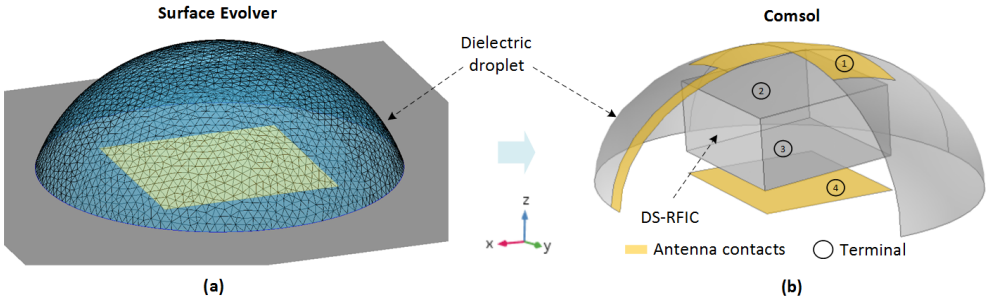


Fig. 4.16 (a) Geometry of the droplet in Surface Evolver representing the partial de-wetting of the substrate after energy minimization. (b) Geometry imported in Comsol Multiphysics for extracting the mutual capacitance matrix between terminals. The chip has been shifted in x, y and z directions as well as tilted or rotated around them.

Contrary to the previous case, capacitance values are not equally distributed around their median. In fact, as shown in simulation results of Fig.4.17 (a), capacitor C_{Aa} has a very limited dispersion with data points inside the first and third quartile. On the other hand, capacitor C_{Bb} shows a large data dispersion with values up to few pF. This can be explained by the fact that the curvature of the droplet is more relaxed compared to the total dewetting case. Therefore, as already explained in the section 3.3, the height of the droplet is much lower and the DS-RFIC is forced to stay closer to the bottom pad of the antenna.

In Fig.4.17 (b) is interesting to see that values of C_{Bb} in the third quartile are concentrated between 3.5 to 5 pF. This leads to a low impedance, hence low voltage drop on it. Nevertheless, as already explained in the previous case, capacitors C_{Aa} and C_{Bb} can be merged together into C_{ser} and since they are in a series combination, the smallest capacitance dominates. In fact, it can be observed that C_{ser} is dominated once again by the low values of C_{Aa}.

Using the same simulation parameters of the case study 1, the complete model of Fig.4.3 have been simulated taking into account the new extracted values of coupling and cross-coupling capacitances.

As shown in Fig.4.18 (a), the load voltage dispersion is strongly reduced and for maximum reader current, the attenuation at f_0 is $\approx$-21 dB, that is 6 dB better than the previous case. The frequency shift due to the capacitor C_2 is the same as the case

study 1, in fact, since coupling capacitors are very small, the detuning of the tag is dominated by the capacitor C_2.

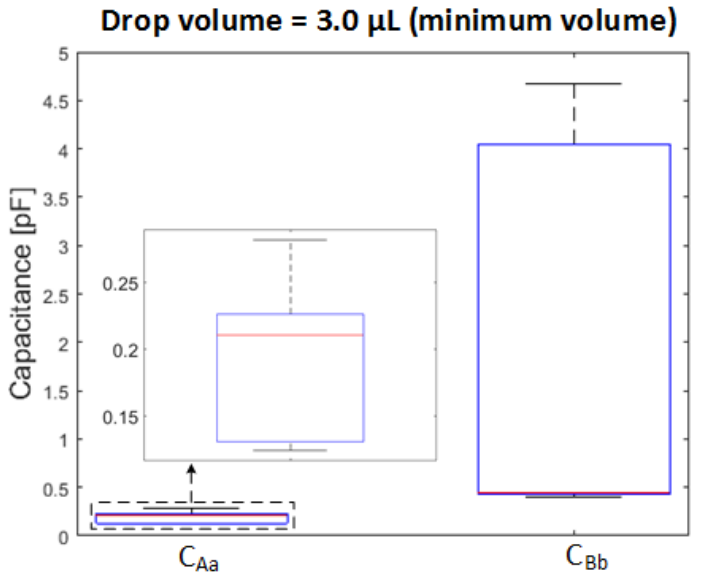
The dependence of V_L on the geometric coupling coefficient k and the chip impedance, shows the same behavior of the previous case study, nevertheless, better performances can be clearly expected. Indeed, at the reference distance of 37.5 mm, voltage amplitudes are higher enough to justify the design of simple RF to DC voltage converters (e.g. single wave voltage rectifier).

4.4 Summary

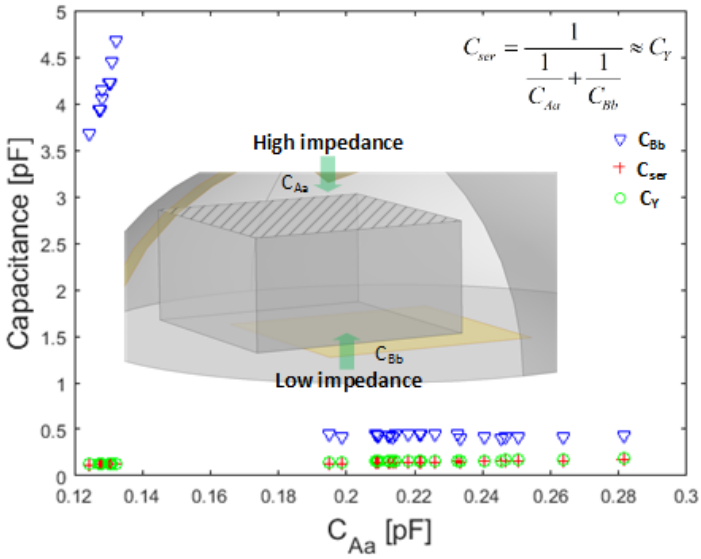
In this chapter an in-depth analysis of the capacitive coupling has been carried out and a complete electrical model (also taking into account the inductive coupling) has been developed.

A chip thickness of 500 μm has been reasonably selected for the analysis. The worse case, that is with a volume increase factor of 2.0 has been used. Simulation results show that coupling and cross-coupling capacitors exhibit a relatively large dispersion with values in the sub-pico farad range. These low values, which depend on the position of the DS-RFIC inside the dielectric droplet, suggest tuning the resonant parallel capacitor to the value that would be used for a simple RLC circuit (unloaded antenna coil).

Electrical performances have been verified according the ISO/IEC 14443 standard. The best performances have been obtained with the partial dewetting case in which the dielectric droplet spread homogeneously over the substrate leading to a spheroid shape that allows lower amount of dielectric in correspondence of the coupling pads.

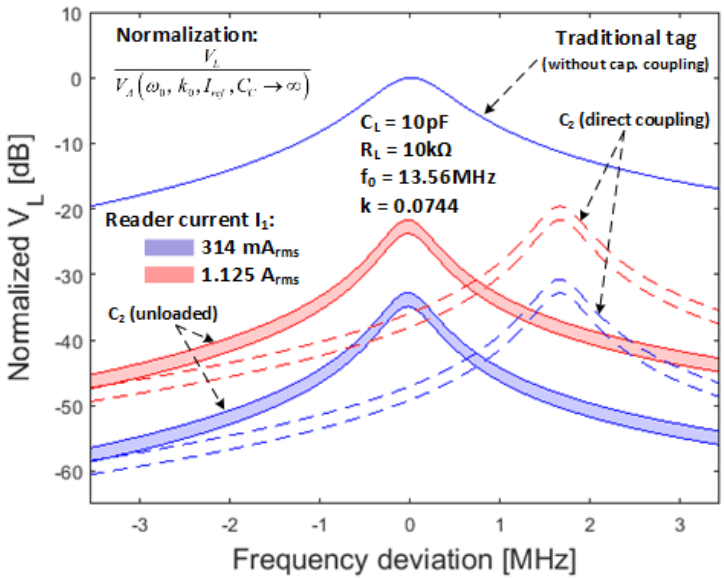


(a)

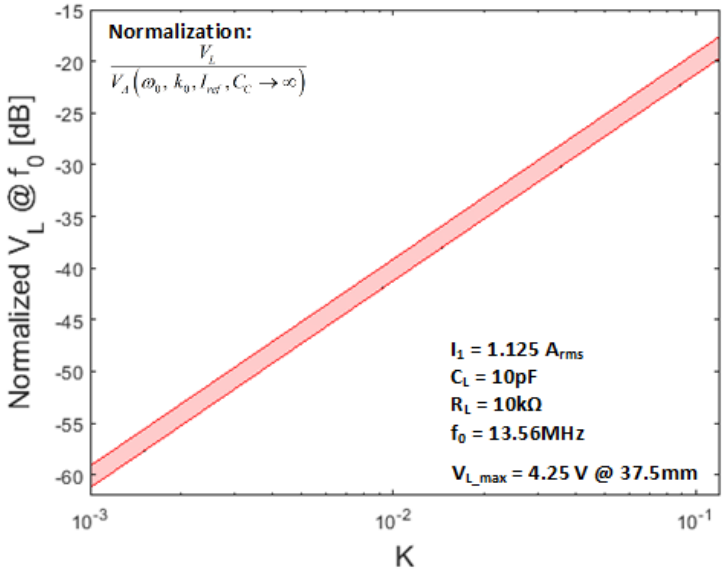


(b)

Fig. 4.17 (a) Boxplot showing the capacitance dispersion of C_{Aa} and C_{Bb} for the case of the partial dewetting. Values extracted from model show a large variation of C_{Bb} with values up to few pF. (b) Dependence of C_{Aa} and C_{Bb} as well as their series combination showing C_{Aa} as the dominant capacitor is the conduction path. The values of C_{Aa} are still low but higher than the previous two cases.



(a)



(b)

Fig. 4.18 (a) Comparison of a traditional transponder (without capacitive coupling) and the complete model including the extracted set of values of coupling and cross-coupling capacitors for the case of the partial dewetting. (b) Load voltage increasing the geometric coupling coefficient k. Better results can be observed in comparison to the previous case study. All simulations normalized according to the reference configuration. Unless otherwise specified, numerical values of Table.4.1 have been used.

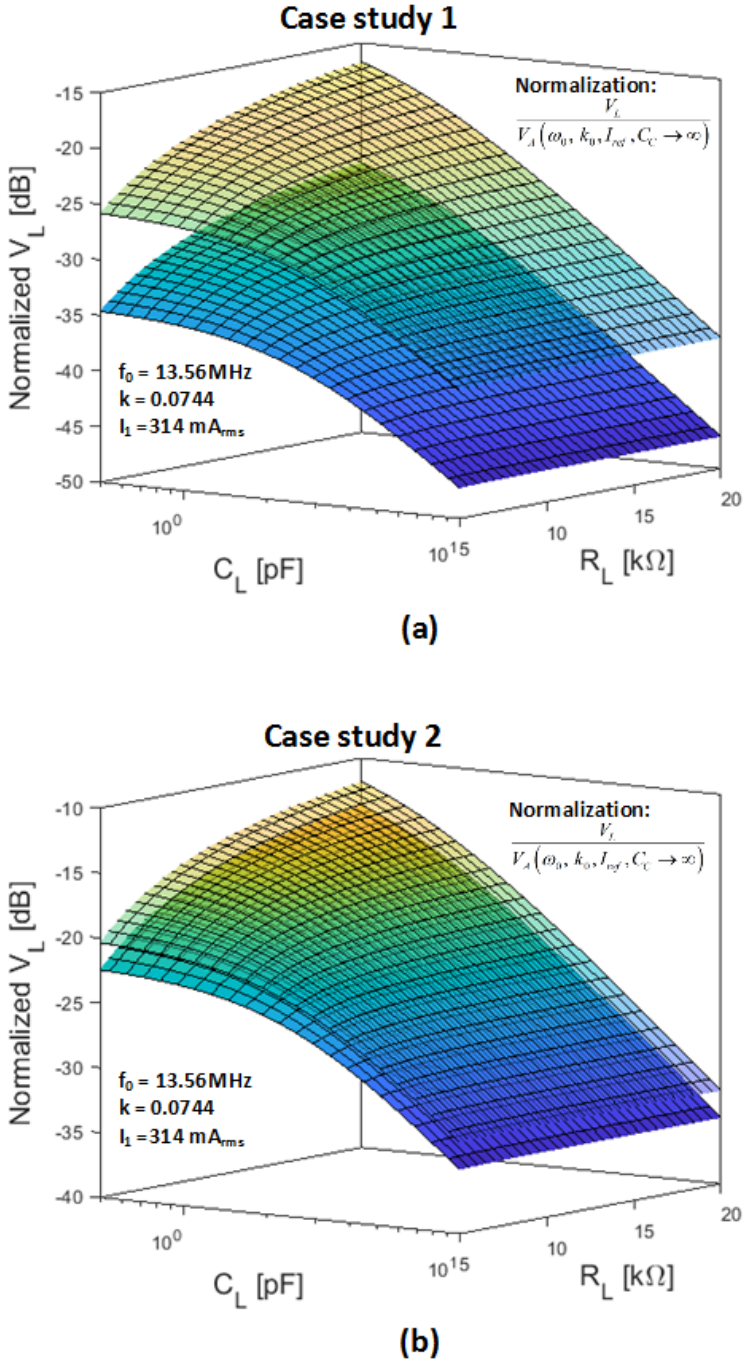


Fig. 4.19 Normalized V_L dependence on the load impedance for (a) the case study 1 and (b) the case study 2. For both cases, only upper and lower bound values (related to coupling and cross-coupling capacitors) have been plotted.

Chapter 5

Double-surface RFIC design

5.1 Introduction

The double-surface RFIC structure has already been introduced in section 3.2. The peculiarity of such a chip consists in having two contacts as large as the surface of the chip. One contact is implemented with the highest metal layer allowed by the technology whereas the other one is constituted by the silicon substrate. A concept view of this structure, with capacitive coupling, is shown in Fig.5.1 (a).

A first test implementation of the DS-RFIC has been fabricated using the high voltage (HV) AMS $0.35\mu m$ technology where a simplified cross-section is shown in Fig.5.1 (b) with the four characteristic layers that can be described as it follows: i) the top of the chip is covered with a passivation layer (e.g. silicon nitride Si_3N_4). In an electrical point of view, it represents a capacitor which is serially connected to the coupling capacitor C_{Aa} or C_{Bb} depending on the orientation of the chip during the encapsulating process; ii) the oxide layers between the metal connections is composed of silicon dioxide (SiO_2). Four layers of metal (e.g. aluminium Al) exists in the AMS $0.35\mu m$ technology; iii) the devices implanted into the silicon substrate are connected together (using the metal layers) forming the circuitry of the RFIC; iv) the silicon substrate which is essentially considered as a resistor in the high frequency range.

The analog front end (AFE) of this first test implementation is made up of a full-wave voltage rectifier with load modulation capability.

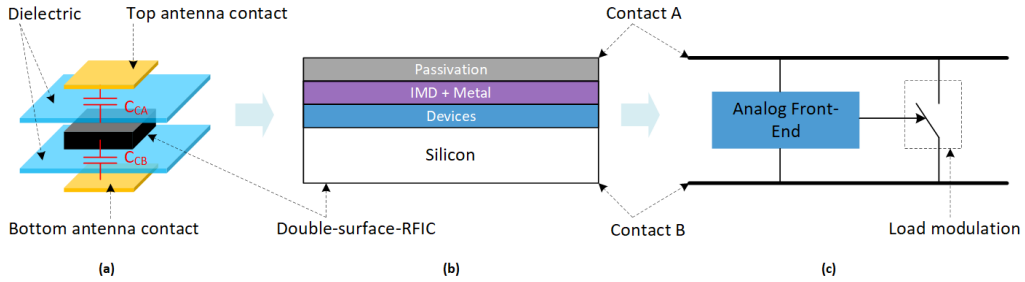


Fig. 5.1 (a) Exploded view of the DS-RFIC and the capacitive coupling. (b) Simplified DS-RFIC structure showing the material distribution along the cross-section and (c) simplified schematic of the analog front end with the load modulation.

5.2 Design methodology for voltage rectifier circuits

5.2.1 Introduction

Voltage rectifiers are normally built using diode bridges that allow the conversion a RF signal from the antenna to a DC output voltage. For low voltage circuits, the forward voltage drop of diodes is a critical point that affects the Power Conversion Efficiency (PCE). Indeed, if the RF input voltage is below the forward voltage, the rectifier circuit will not be able to produce DC output voltage. This region is known as the "dead zone" which leads to reduced read ranges for RFID transponder, or more in general wireless devices [108].

Schottky diodes with low forward voltage drops and low threshold voltage (low V_{th}) transistors could be used to enhance the efficiency. However, these solutions require additional masks and fabrication steps, hence the production costs are higher compared to a standard CMOS process.

One common way to enhance the PCE, is to use diode-connected MOS transistors using threshold voltage cancelling techniques which reduce the turn-on voltage [109] or using operational amplifier (active diodes) [110], demonstrating high PCE.

Nevertheless, these latter techniques normally require additional biasing circuits using on-board batteries (e.g. semi-passive transponder) the inclusion of which is prohibitive in many applications such as the one proposed in this thesis.

Multi-stages rectifier circuits are normally used to increase the output voltage [111, 108]. This technique consists in cascading N rectifier cells which behave as a charge pump voltage multiplier. An in-depth description of these techniques can be

found in [109]. The number of cells is a trade-off between the PCE and the parallel input resistance which value reduces increasing N. this is essentially because each cell adds in parallel.

As an example, a simplified electrical model of a single stage, full-wave VR diode-based circuit is shown in Fig.5.2 where during the positive half-wave, the conduction path, highlighted in (a), is given by the resistor R_T, the diode D_1, the load impedance Z_L and finally the diode D_4. For the negative half-wave, the conduction path, highlighted in (b), is given by D_2, Z_L, D_3 and R_T.

The output voltage of the VR circuit, shown in Fig.5.2 (c), is characterized by an initial transient period and a steady state in which V_{out} exhibits a voltage ripple. The latter is given by the charge and discharge of the capacitor C_{tank} and it depends on the current drawn by the load (I_{out}) as well as by the value of the capacitor. As shown in Fig.5.2 (e), during the transient period, the input current is much higher than the current in steady state since the C_{tank} si initially discharged.

5.2.2 Large signal VR circuit analysis

The voltage rectifiers have been analyzed and designed to maximize the PCE. The design method is based on a steady state time-constant equivalent model where the parameters are extracted thanks to a parabolic approximation of the pulsed input current. This approximation allows to reduce the complexity of the analytical equations. In addition, the complicated large signal modeling of AC currents induced by the parasitic capacitances of transistors (gate-to-source: C_{gs}, gate-to-drain: C_{gd}, drain-to-bulk: C_{db}, source-to-bulk: C_{sb} and gate-to-bulk: C_{gb}) during fast voltage transitions, is not required since the switching losses will be simply treated as a rms current to be minimized during the design phase.

The parabolic approximation model, characterized by the diode conduction angle, is valid for cases in which the total conduction path resistance R_T and the output capacitor C_{tank} fulfill the following condition ($\tau_1 = R_T C_{tank} >> T/m$). Considering the DS-RFIC structure, in which the bulk is part of the conduction path, larger R_T are expected than conventional voltage rectifier design, therefore, the parabolic approximation model is a well-suited design tool.

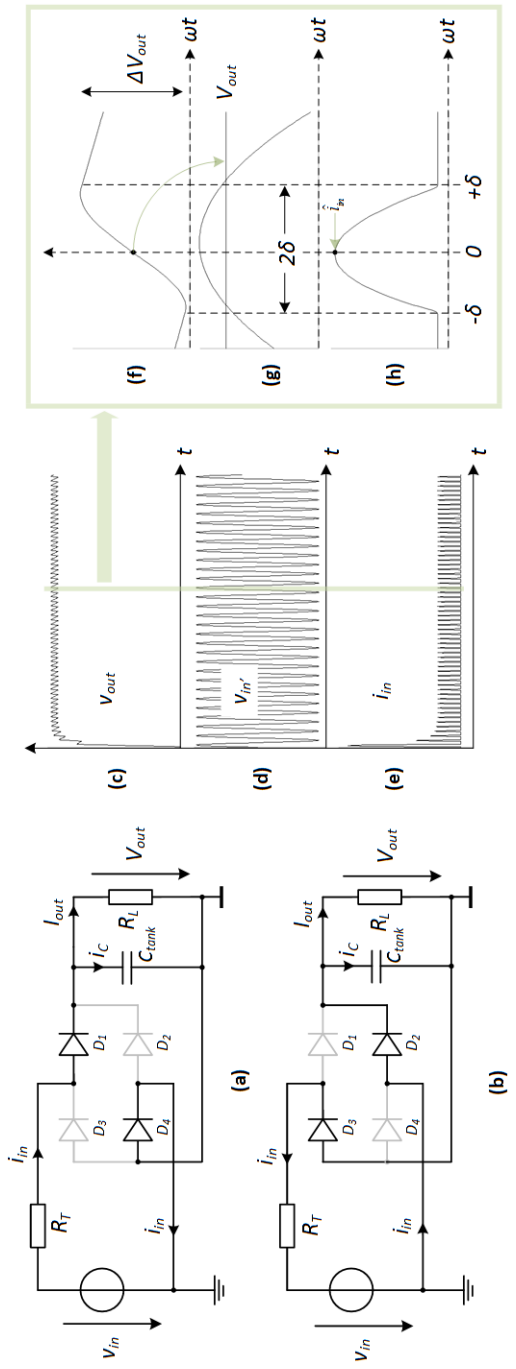


Fig. 5.2 Simplified electrical model of a full-wave voltage rectifier with the conduction path highlighted for the positive (a) and negative (b) half-wave. (c) Typical output voltage waveform with ripple. (d) Input voltage reduced of $2V_{Don}$. (e) Pulsed input current. (f) Detail of the output voltage ripple during the conduction period ($2\ \delta$). (g) Detail of the input voltage (reduced of $2V_{Don}$) and the average output voltage showing the conduction period and the limit of conduction. (h) Detail of the pulsed input current during the conduction period.

5.2.3 Conduction angle

The definition of the conduction angle δ of a voltage rectifier circuit allows the optimization of the VR itself and the tank capacitor C_{tank}. Moreover, it can be used for extracting the total resistance of the conduction path R_T during simulations and experimental measurements.

In steady state, with a voltage ripple sufficiently small, the output voltage can be considered to have a constant value given by V_{out}. This situation is illustrated in Fig.5.2 (g) along with the upper part (near the pick) of the sinusoidal voltage $v_{in'}$ which is given by:

$$v_{in'} = v_{in} - 2V_{Don} \tag{5.1}$$

where V_{Don} is the forward threshold voltage of the diodes.

As shown in Fig.5.2 (h), the conduction period which is given by 2δ, defines the duration during which the current can flow from the input of the VR to the load. This happens when the voltage $v_{in'}$ is above the average output voltage. Following that, δ can be calculated at the limit of conduction when the following condition occurs:

$$\begin{aligned} V_{out} &= v_{in'} \\ &= \widehat{v_{in}}\, cos(\delta) - 2V_{Don} \end{aligned} \tag{5.2}$$

Therefore, the conduction angle can be determined by:

$$\delta = arccos\left(\frac{V_{out} + 2V_{Don}}{\widehat{v_{in}}}\right) \tag{5.3}$$

It is important to note that in this analysis, the origins of the graphs, shown in Fig.5.2 (f) to (h), have been shifted in the middle of the pulsed input current.

At this point, the input pulsed current can be defined using δ:

$$\begin{aligned} i_{in} = \frac{u_{RT}}{R_T} &= \frac{u_{in} - \left(2V_{Don} + V_{out}\right)}{R_T} \\ &= \frac{\widehat{v_{in}}\, cos(\omega t) - \widehat{v_{in}}\, cos(\delta)}{R_T} \end{aligned} \tag{5.4}$$

The average of i_{in} can be calculated by integrating it within the conduction period 2δ. This average value corresponds to the DC current drawn by the load and can be expressed as it follows:

$$\begin{aligned} I_{out} = \frac{V_{out}}{R_L} = I_{in,avg} &= \frac{m}{2\pi} \int_{-\delta}^{\delta} i_{in}(\omega t)\, \mathrm{d}\omega t \\ &= \frac{m}{2\pi} \int_{-\delta}^{\delta} \frac{\widehat{v_{in}}\left[cos(\omega t) - cos(\delta)\right]}{R_T}\, \mathrm{d}\omega t \\ &= \underbrace{\frac{m\, \widehat{v_{in}}}{\pi\, R_T}}_{\mathrm{A}} \left[sin(\delta) - \delta cos(\delta)\right] \end{aligned} \tag{5.5}$$

where the resistor R_T represents the total resistance of the conduction path, m corresponds to: 1 for a single wave voltage rectifier and 2 for a full-wave voltage rectifier. The term A corresponds to the average load short-circuit current.

In order to simplify the analysis of the VR, a parabolic approximation of the input pulsed current is introduced [112]. As already explained, if the condition $\tau_1 >> T/m$ and the voltage ripple is sufficiently small to be neglected, the following approximation can be used:

$$i_{in,approx} = \widehat{i_{in}} \left[1 - \left(\frac{\omega t}{\delta}\right)^2\right] \tag{5.6}$$

where in this case δ acts as a compression term of the parabolic function. At this point, the average as well as the rms value of i_{in} can be easily defined using the following two expressions:

$$\begin{aligned} I_{out} = I_{in,avg} &= \frac{m}{2\pi}\int_{-\delta}^{\delta}\left[\widehat{i_{in}} - \widehat{i_{in}}\left(\frac{\omega t}{\delta}\right)^2\right] \mathrm{d}\omega t \\ &= \widehat{i_{in}}\,\frac{2\,m\,\delta}{3\,\pi} \end{aligned} \tag{5.7}$$

and

$$\begin{aligned} I_{in,rms} &= \sqrt{\frac{m}{2\pi}\int_{-\delta}^{\delta} i_{in,approx}(\omega t)^2\,\mathrm{d}\omega t} \\ &= \sqrt{\frac{m}{2\pi}\int_{-\delta}^{\delta}\left[\widehat{i_{in}} - \widehat{i_{in}}\left(\frac{\omega t}{\delta}\right)^2\right]^2 \mathrm{d}\omega t} \\ &= 2\,\widehat{i_{in}}\,\sqrt{\tfrac{2\,m\,\delta}{15\,\pi}} \end{aligned} \tag{5.8}$$

5.2.4 Output (tank) capacitor

In order to insure the maximal allowed voltage ripple (ΔV_{max}) at the output of the VR, the capacitors C_{tank} needs to be optimized. The voltage ripple is given by the discharge of the capacitor that takes place when the voltage $v_{in'}$ is below the average output voltage. In this case, the current i_{in} is zero (outside the conduction period 2δ) and the capacitor become the source that supply the voltage to load resistor (the internal circuitry), indeed, as for a simple *RC* circuit, the voltage decreases exponentially according to the following expression:

$$u_{out} = u_{out,max}\, exp\Big(-\frac{t}{R_L C_{tank}}\Big) \tag{5.9}$$

If the capacitor is well designed ($\tau_2 = R_L C_{tank} >> T/m$), the ripple is characterized by a small portion of the exponential decay which can be considered to be linear. Following that the voltage ripple can be expressed as:

$$\Delta V_{out} = \frac{I_{out} T_{decay}}{C_{tank}} \tag{5.10}$$

where T_{decay} can be expressed in terms of δ:

$$T_{decay} = T\left(\frac{1}{m} - \frac{\delta}{\pi}\right) \tag{5.11}$$

Therefore, the necessary value of C_{tank} that insure a voltage ripple lower than $\Delta V_{out,max}$ is:

$$C_{tank} \geq \frac{V_{out}}{R_L\, \Delta V_{out,max}} T\left(\frac{1}{m} - \frac{\delta}{\pi}\right) \tag{5.12}$$

5.2.5 Input resistor

It was shown, in the section 4.1, that the supply voltage on the transponder depends on its input impedance. The latter is defined by an imaginary part (called C_{in}) due to the parasitic capacitances and a real part (called R_{in}) that depends on the output current consumption.

The voltage rectifier is a non-linear circuit due to the presence of diodes and the input current has a pulsed form leading to a non-constant input impedance which in turn leads to a complex time and frequency domain analysis. Nevertheless, in the steady state, the voltage rectifier can be modeled using the time-constant equivalent circuit of Fig.5.3 where the reference point (GND) is internally generated by the voltage rectifier. This model enables the prediction of the power needed to supply a given load output current at a constant output voltage.

The resistor R_{in} represents the mean power that enters the rectifier circuit, more precisely, the input pulsed current is transformed into an equivalent sinusoidal current which enables the transfer of the same amount of power. In this case, the sinusoidal current can be defined as it follows:

$$i_{in,sin}(t) \;=\; \frac{v_{in}(t)}{R_{in}} \;=\; \frac{\widehat{v_{in}(t)}\; sin(\omega t)}{R_{in}} \tag{5.13}$$

Therefore, the mean power is expressed by:

$$\begin{aligned} \overline{P_{in}} \;&=\; \frac{1}{T}\int_0^T v_{in}(t)\; i_{in,sin}(t)\; \mathrm{d}t \\ &=\; \frac{1}{T\; R_{in}}\int_0^T \widehat{v_{in}}^2\; sin^2(\omega t)\; \mathrm{d}t \;=\; \frac{V_{in,rms}^2}{R_{in}} \end{aligned} \tag{5.14}$$

where T is the period of the input signal. With the measured (or simulated) value of $\overline{P_{in}}$, the equivalent time constant resistor R_{in} that satisfies the power equivalence can be calculated as it follows:

$$R_{in} \;=\; \frac{V_{in,rms}^2}{\overline{P_{in}}} \tag{5.15}$$

5.2.6 Output resistor and output voltage

In the model of Fig.5.3, the voltage $V_{out,0}$ of the voltage controlled voltage source (VCVS) depends on the pick input voltage $\widehat{v_{in}}$ and it is defined as an open circuit voltage (without load).

The output resistor R_{out} takes into account the average output voltage drops due to the resistor R_T in the conduction path. As shown in Fig.5.2 (f), the average output voltage V_{out} can be found in correspondence of the pick input current. For this reason, the output voltage drop can be defined as it follows:

$$V_{Rout} \;=\; R_T\; \widehat{i_{in}} \tag{5.16}$$

At this point, considering that the output current of the model is $I_{out} = I_{in,avg}$, the output resistor can be defined with the following expression:

$$R_{out} = \frac{V_{Rout}}{I_{out}} = R_T \frac{\widehat{i_{in}}}{I_{in,avg}} \tag{5.17}$$

It is more interesting in this case to express the pick input current in terms of $I_{in,avg}$. Thanks to the parabolic approximation, the ratio between the rms and the average input current of the voltage rectifier can be expressed as it follows:

$$\frac{I_{in,rms}}{I_{in,avg}} = \sqrt{\frac{6\,\pi}{5\,m\,\delta}} \tag{5.18}$$

Using this last equation in conjunction to Eq.5.8, the input pick current can be approximated in the following way:

$$\widehat{i_{in}} = I_{in,avg} \frac{3\,\pi}{2\,m\,\delta} \tag{5.19}$$

At this point, Eq.5.17 can be rewritten and becomes:

$$R_{out} = R_T \frac{3\,\pi}{2\,m\,\delta} \tag{5.20}$$

The average output voltage can finally be expressed using Eq.5.20:

$$V_{out} = \widehat{v_{in}} - mV_{Don} - R_{out}\,I_{out} \tag{5.21}$$

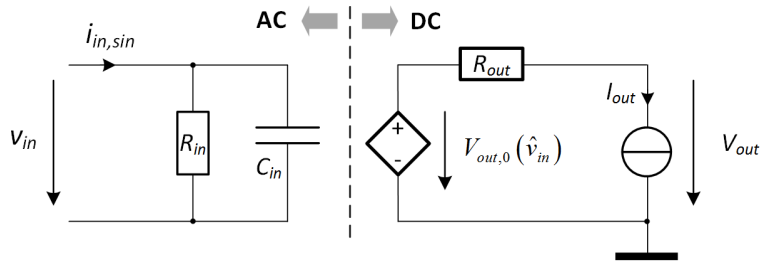


Fig. 5.3 Voltage rectifier time-constant equivalent circuit.

5.2.7 Power Conversion Efficiency (PCE)

The power conversion efficiency is a metric with which the conversion capability of the VR is quantified in terms of energy converted to the tag. This parameter is calculated by the equation below:

$$PCE = \frac{P_{load}}{P_{load} + P_{loss}} = \frac{V_{out}\, I_{out}}{V_{in,rms}\, I_{in,rms}} \tag{5.22}$$

Thanks to Eq.5.21 the PCE can be rewritten as it follows:

$$PCE = \frac{\left(\widehat{v_{in}} - mV_{Don} - R_{out}\, I_{out}\right) I_{out}}{V_{in,rms}\, I_{in,rms}} \tag{5.23}$$

This suggests that higher output resistances R_{out} and higher forward threshold voltages V_{Don} lead to lower PCE. Therefore, both R_{out} and V_{Don} needs to be kept as low as possible for improving the conversion efficiency.

5.3 High voltage full-wave VR circuit

Considering the nature of the DS-RFIC, voltages of some volts may be expected in the bulk, especially when the tag is working in proximity with respect to the reader. Following this, the high voltage technology is an obvious candidate for isolating the low voltage circuitry from the large input signal. Indeed, as shown in Fig.5.4, both PMOS and NMOS transistors are isolated inside a deep n-well region forming a diode with the intrinsic substrate (p-type) which is, in normal operations, reversely biased.

Voltage rectifier circuits are normally implemented in a multistage configuration (voltage multiplier) in order to increase both the output voltage and the efficiency. However, in this work, thanks to the high voltage transistors, a small, single stage and full-wave voltage rectifier has been designed using the NMOS gate cross-connected bridge structure shown in Fig. 5.6.

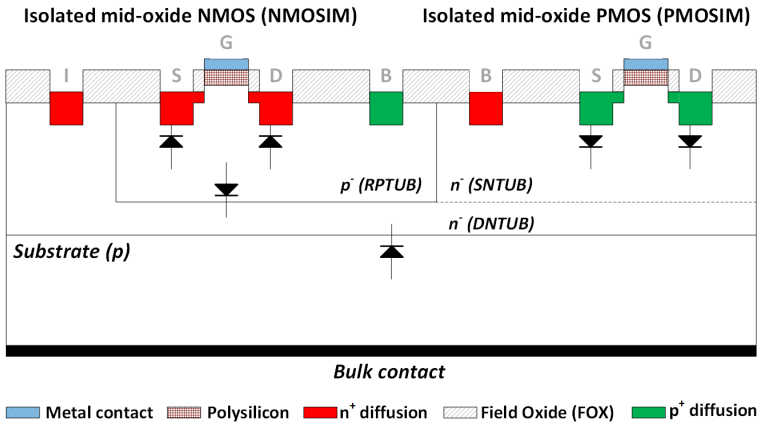


Fig. 5.4 Cross-sectional view of the isolated mid-oxide NMOS and PMOS transistors. The NMOS transistor is inside a p-type region (RPTUB) which is isolated from the intrinsic substrate by the deep n-well (DNTUB). The PMOS transistor is inside a shallow n-type region (SNTUB) which is isolated just like the NMOS transistor.

5.3.1 Single stage VR and PCD power requirement

The feasibility of using a single stage voltage rectifier has been first verified taking into account once again the complete model of Fig.4.3 and the reference RFID system configuration (z_P = 37.5mm) of the previous section.

The VR circuit has to be able to deliver a voltage sufficient to drive the internal circuitry of the transponder. In this work, a minimum DC voltage of 5V (see next section for detail) is considered taking into account the forwards voltage drop of diodes, substrate losses, the drop-out voltage of a regulator and the load modulation. This minimum DC output voltage implies a RF input voltage amplitude of 5V considering a single stage full-wave rectifier.

The current I_1, required in the reader side for having at least V_L = 5V, has been calculated based on Eq.4.44 and 4.36 and reported here following under the form of its module:

$$|I_1| = \frac{2\,V_{L,min}}{\mu_0\,\omega_0^2\,a^2\,A_{eff}\,n_E\,R_L\,R_{Lp1}}\sqrt{\left(a^2+z_P^2\right)^3\left\{\omega_0^2\left(\ldots\right)^2+\left[\ldots\right]^2\right\}} \tag{5.24}$$

where:

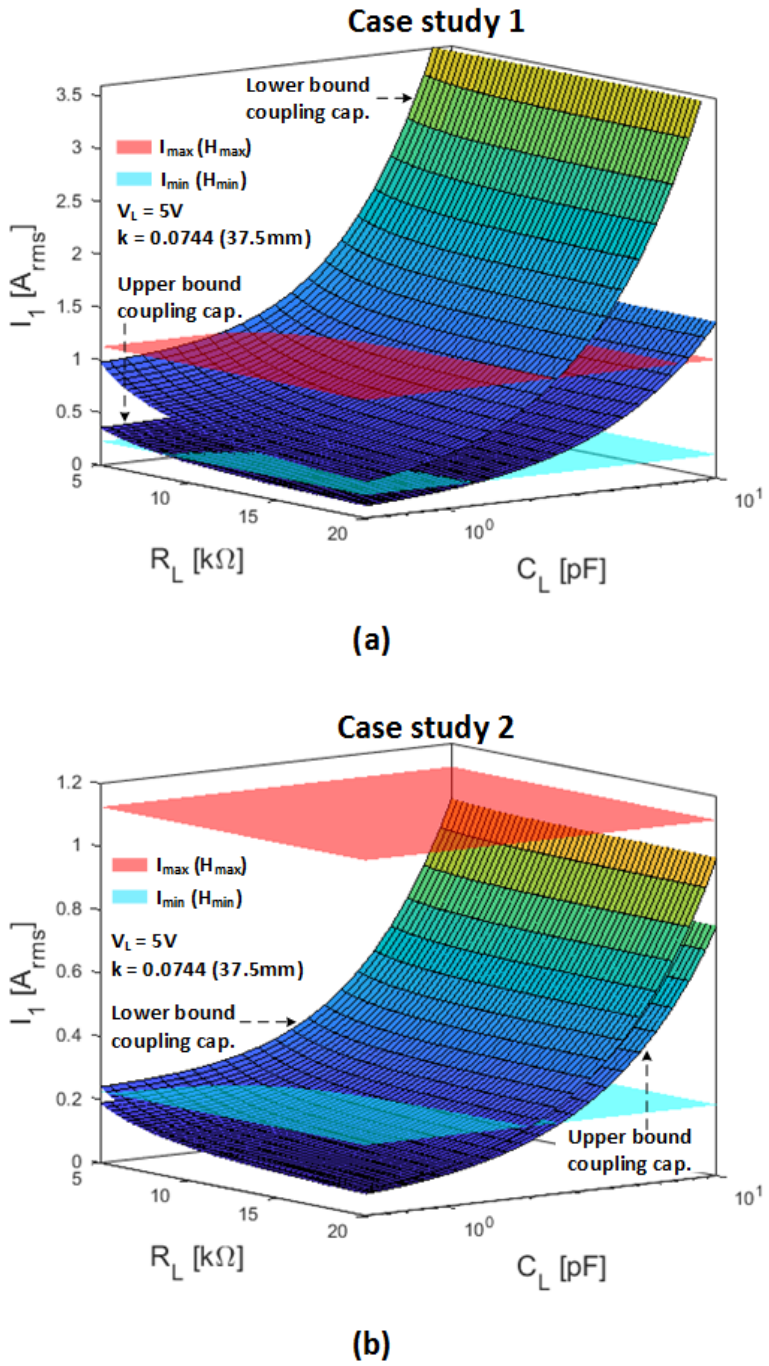


Fig. 5.5 Reader current required in order to have a load voltage amplitude of 5V for the case study 1 (a) and the case study 2 (b). In both cases, only upper and lower bound values of the coupling and cross-coupling capacitors are considered and the current I_1 is compared with the maximum and minimum values according to the ISO/IEC 10373 standard. The minimum power requirement is plotted in function of the load impedance.

$$\begin{aligned}(...) &= L_2 + C_{TOTp}\, R_2\, R_{Lp1} + C_{OUT}\, R_L\, (R_2 + R_{Lp1}) \\ &\quad - C_{OUT}\, C_{TOTp}\, L_2\, R_L\, R_{Lp1}\, \omega_0^2\end{aligned} \tag{5.25}$$

and

$$\begin{aligned}[...] &= C_{OUT}\, L_2\, R_L\, \omega_0^2 + R_{Lp1}\, (C_{TOTp}\, L_2\, \omega_0^2 - 1) \\ &\quad + R_2\, (C_{OUT}\, C_{TOTp}\, R_L\, R_{Lp1}\, \omega_0^2 - 1)\end{aligned} \tag{5.26}$$

For the case study 1, as shown in Fig.5.5 (a), considering load capacitors above 2.5pF and lower bound coupling and cross-coupling capacitors, the current required in the reader side for reaching V_L = 5V, exceeds largely the maximum value allowed by the ISO/IEC 14443 standard. On the other hand, for upper bound values, standard specifications are fulfilled with C_L up to ≈7.5pF.

The PCD antenna coil should be driven at least at I_{min} which means that for C_L lower than ≈1pF, the load voltage will be higher than 5V of amplitude.

For the case study 2 instead, the maximum current allowed in not exceeded, even for lower bound coupling and cross-coupling capacitors. It can be observed that the distance between upper and lower bound values is strongly reduced compared to the case study 1. This is in agreement with the results of the previous section.

5.3.2 NMOS gate cross-connected bridge

The implemented voltage rectifier, shown in Fig.5.6, can be explained as it follows: when V_{INA} has a high potential, M_2 is "open" and D_1 is forward biased charging up the capacitor C_{tank}. The latter smooth out the sinusoidal input voltage to a *DC* power supply. When V_{INB} is at a high level, M_1 is open and D_2 is forward biased charging up again the capacitor C_{tank}. In this way, not only the full-wave rectification is performed but the two cross-connected NMOS transistors M_1 and M_2 also generate

an internal reference potential (gnd) which is not directly connected to the bulk but distributed to the isolated circuitry.

The VR structure has been designed in order to have a symmetric behavior, in fact, transistors M_1 and M_2, as well as the diode D_1 and D_2 are identical. The bulk connection (V_{INB}) is modeled with a resistor R_B whereas the connection between the top metal layer (V_{INA}) is modeled with a resistor R_A. The latter has a much smaller value than R_B since implemented with a direct metal connection.

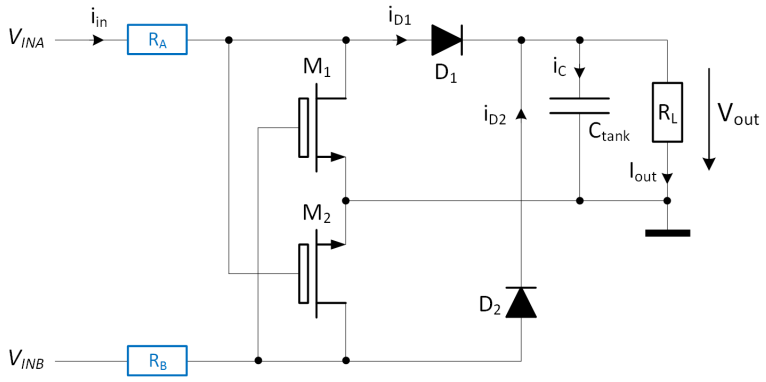


Fig. 5.6 Full-wave cross-connected bridge voltage rectifier with capacitor filter, high voltage transistors and parasitic resistors.

5.3.3 Substrate analysis

Accurate 3-D field solver numerical methods exist today for substrate capacitance, inductance and resistance extraction. An overview of these methods can be found in [113]. However, accurate closed-form expressions for calculating the substrate resistance are less frequent in literature.

In the case of this work, any frequency-dependent effects of the substrate have been ignored since in the high frequency range, the substrate conduction is dominated by its resistive nature. In fact, considering a homogeneous and isotropic silicon block with resistivity ρ, the admittance Y between the contact of the substrate (backside) and the contact of a diffusion, near the Si-SiO_2 interface, is given by:

$$Y = G + j\omega C \quad with \quad G = \sigma \frac{A}{t} \quad and \quad C = \varepsilon_0 \, \varepsilon_r \frac{A}{t} \tag{5.27}$$

where A is the surface of the contacts, t is the distance between them and $\sigma = \rho^{-1}$ is the conductivity of the substrate. Therefore, for $\sigma \ll \omega\varepsilon_0\varepsilon_r$, the substrate predominantly behaves resistively and can be modeled as a resistive network as shown in Fig.5.7 (a).

As reported in [114], the substrate resistance to the backplane has been extracted for both uniform and heavily doped substrates using the RCCG (Resistive and Capacitive Coupling exploiting Geometry constraints) method with sufficient accuracy. The same authors, also proposed an improved method, called SRG (Substrate Resistance computation based on Geometry constraints) which is based on a geometric formulation of the current streamlines between coupled structures. The correct geometric shape is determined as the one which exhibits the minimum resistance. The SRG method is more precise than the RCCG one (from 15% to 5% accuracy) especially for epi-taxial lightly doped substrates [115].

In this work, the substrate is supposed to have no resistivity variations in the x, y and z directions. In fact, in the vertical direction, the nonuniform doping profiles are not considered since not disclosed by the foundry. Furthermore, the high voltage technology has multiple wells for isolating the low voltage circuitry from the high voltage one. This further complicate the modeling of the substrate.

Using Comsol Multiphysics a lumped resistor has been extracted from the substrate. The validity of this method has been initially verified using the straightforward closed form expression developed by Terrill and Hu [14] with the purpose to have a design starting point. Subsequently, measurements results have been used in conjunction with the parabolic approximation model for extracting the total path resistance of the voltage rectifier circuit.

As explained in [14], the resistance between a square contact of side length L_{CONT} and the backside has been calculated by using an equivalent circular disk of the same area of the contact and assuming a homogeneous substrate. The resistance can be calculated as it follows:

$$R = \frac{\rho_{DIFF}}{2\pi a}\left\{\frac{\pi}{2} + 2\sum_{i=1}^{n} k^i \, sin^{-1}\left(\frac{2a}{\sqrt{(2a)^2 + (2\,i\,T_{DIFF})^2} + 2\,i\,T_{DIFF}}\right)\right\} \tag{5.28}$$

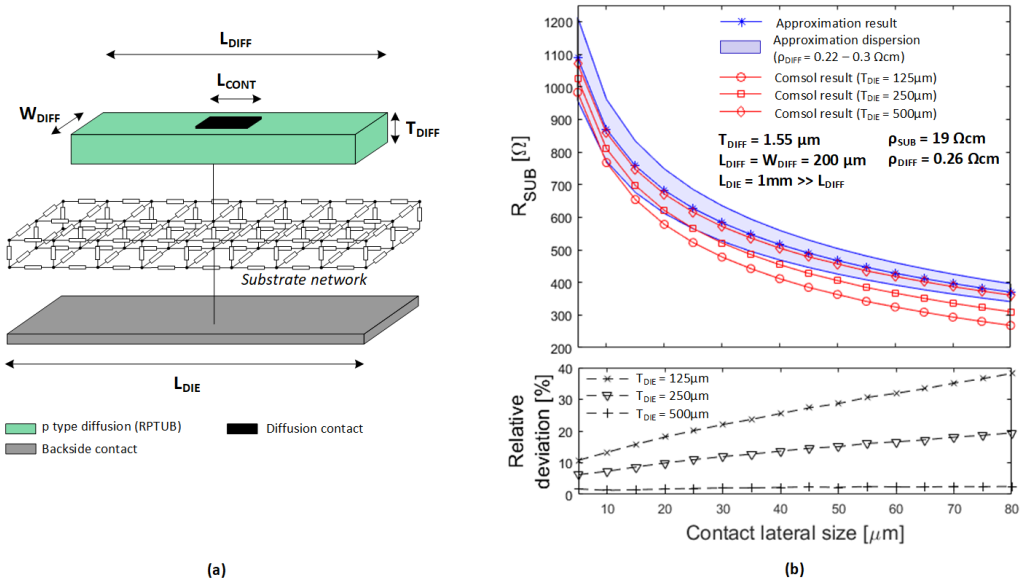


Fig. 5.7 (a) Exploded view of the backside contact with the resistive substrate network and a p-type diffusion. The size of the contact is smaller than the size of the diffusion itself. (b) Top: Comsol simulation results and results obtained using the equation of [14]. For substrates with $T_{DIE} \geq 500\mu m$ the results agree with a relative deviation < 3%. Bottom: relative deviation between Comsol results and the closed form expression for three T_{DIE} values.

with:

$$k = \frac{\rho_{SUB} - \rho_{DIFF}}{\rho_{SUB} + \rho_{DIFF}} \tag{5.29}$$

and

$$a = \sqrt{\frac{L_{CONT}^2}{\pi}} \tag{5.30}$$

In this expression, ρ_{SUB} is the substrate resistivity, ρ_{DIFF} is the resistivity of the diffusion region and T_{DIFF} is the depth of this region below the surface.

The first set of simulations of Fig.5.7 (b) show that for substrates with thickness $T_{DIE} \geq 500\mu m$ the agreement between the Comsol model (shown in Fig.5.8 (c)) and Eq.5.28 is less than 3% for contact lateral size between 5 to 80 μm, where the diffusion lateral size (equivalent to a square) is 200 μm. The relative deviation has been determined using typical values of ρ_{SUB} and ρ_{DIFF} whereas the lightly blue

shaded region shows the resistance dispersion considering maximum and minimum values of ρ_{DIFF}. The latter has been calculated based on the sheet resistance of the process parameters document of the foundry [94].

For $T_{DIE} < 500\mu m$, the relative deviation become much larger because Eq.5.28 has been developed considering both the lateral size of the diffusion and substrate to be infinitely large and thick respectively. This assumption becomes more and more unrealistic as the size of the contact increase, in comparison to the diffusion size and the bulk thickness decrease, finally leading to larger relative deviation.

As shown in Fig.5.8 (d), small chip dimensions increase the substrate resistance with an almost exponential behavior for thick chips. In a design point of view, the substrate resistance is a compromise between: i) the contact size and ii) the surface occupation of the VR circuit.

5.3.4 Diode-connected transistor optimization

Diodes D_1 and D_2 are both isolated mid-oxide diode-connected NMOS transistors with a channel length L = 0.5 μm (minimum allowed by the process) and the cross-section shown in Fig.5.8 (a). They allow gate-to-source V_{GS} and drain-to-source voltages V_{DS} up to 5.5V. These types of transistors have higher V_{th} than the low voltage counterparts.

The isolated structure is inside a p-type region (RPTUB) creating the parasitic diode ID_2 with the deep n-well (DNTUB). The latter region, as already explained, forms another parasitic diode ID_1 with the intrinsic substrate. In normal operation ID_1 should be reverse biased thanks to the terminal I tied to V_{out}, however, in the case of the DS-RFIC, substrate signals with amplitudes larger than V_{out} may put ID_1 in forward bias leading to an additional charging current flowing into C_{tank}.

As the voltage V_{out} increase due to the charging up of C_{tank}, the parasitic diode ID_2 is more and more reversely biased since the isolated bulk (terminal B) is connected to the reference potential which is generated by the bridge structure.

The values of the equivalent on-resistance, of both diodes D_1 and D_2, are shown in Fig.5.8 (e). They have been extracted using Matlab and the parabolic approximation procedure of Fig.5.9. The input voltage v_{in} and the input pulsed current i_{in} have been imported from Cadence and the value of $\widehat{i_{in}}$ is used to define the parabolic

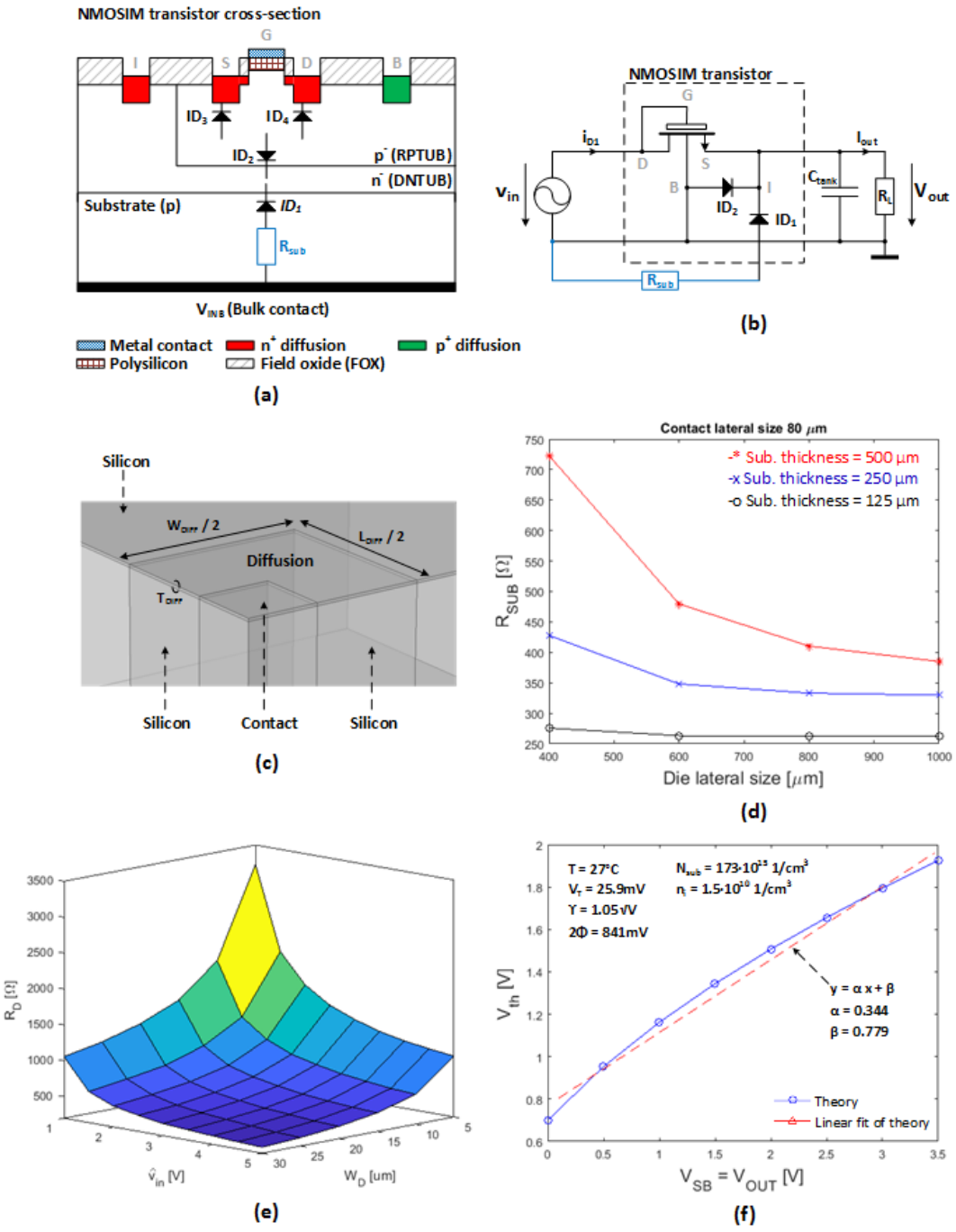


Fig. 5.8 (a) Isolated NMOS diode-connected transistor cross-sectional view with parasitic diodes and substrate network. (b) Simulated half-wave voltage rectifier circuit for the NMOS diode-connected transistor optimization using the parabolic approximation model. (c) One quarter of the model with substrate, contact and diffusion dimensions. (d) Substrate resistance from the backside up to the contact of $80\mu m$ of lateral size. (e) Equivalent diode on-resistance for different widths of the diode-connected transistor and input voltages. (f) Threshold voltage affected by the body effect. A linear fitting is used to define the equivalent diode turn-on voltage.

approximation current as specified by Eq.5.6. A set of conduction angles (δ) is defined and feed to the fitting function that finds the optimum value of δ for which the error between i_{in} and $i_{in,approx}$ is minimized. This error can be expressed as it follows:

$$err \;=\; \sum_{i=1}^{N} \left(i_{in,approx} \;-\; i_{in}\right)^2 \tag{5.31}$$

Using δ_{opt}, in conjunction with Eq.5.7 and 5.8, the average and the rms currents can be calculated. The average short-circuit current has been defined by the term A in Eq.5.5 which contains the total resistance of the conduction path (R_T). In the case of the test circuit of Fig.5.8 (b), the resistor R_T directly correspond to the average on-resistor (R_D) of the diode-connected transistor which can be calculated using the following expression:

$$R_D \;=\; \frac{\widehat{v_{in}}}{\pi\, I_{in,approx,avg}}\left[sin(\delta_{opt}) \;-\; \delta_{opt} cos(\delta_{opt})\right] \tag{5.32}$$

As shown in Fig.5.8 (b), the source of the isolated mid-oxide NMOS transistor is connected to the output capacitor whereas the bulk is connected to the internal reference potential. Following that, the source to bulk voltage (V_{SG}) increase along together with V_{out} due to the charging up of C_{tank}. In this condition, the threshold voltage (V_{th}) of the transistor is affected according to the body effect:

$$V_{th} \;=\; V_{th0} \;+\; \gamma\left(\sqrt{|2\phi_F \;+\; V_{SB}|} \;-\; \sqrt{|2\phi_F|}\right) \tag{5.33}$$

where V_{th0} is the threshold voltage without body effect ($V_{SB} = 0V$), γ is the body effect coefficient and ϕ_F is the bulk Fermi potential which ca be calculated as it follows:

$$\phi_F \;=\; 2V_T(T) ln\left[\frac{N_{sub}}{n_i(T)}\right] \tag{5.34}$$

where N_{sub} is the effective substrate doping, n_i is the intrinsic carrier concentration of the silicon bulk, T is the temperature and V_T is the thermal voltage. The latter can be expressed by:

$$V_T = \frac{K_B T}{q} \tag{5.35}$$

where K_B is the Boltzmann constant ($\approx 1.380 \cdot 10^{-23}\ JK^{-1}$) and q is the elementary charge ($\approx 1.602 \cdot 10^{-19} C$). A commonly used value of n_i at 300K is $1.5 \cdot 10^{10}\ cm^{-3}$ and V_{th0}, γ and N_{sub} can be found in the process parameters document of the foundry [94].

The values of the threshold voltage under body effect are plotted in Fig.5.8 (f) where a linear equation, defined by the parameters α and β, is used in conjunction with Eq.5.21 to find the output voltage (V_{out}). This equation can be rewritten in the following way:

$$V_{out} = \frac{\widehat{v_{in}} - m\beta - R_{out}\ I_{out}}{1 + m\alpha} \tag{5.36}$$

PMOS transistors have also been used for this type of voltage rectifier [116] mainly because the forward voltage drop can be minimized, however, reverse leakage currents would have a negative impact on the PCE and higher voltage ripples are inevitable. In addition, channel resistances are higher than the NMOS counterpart and thus for keeping a total path resistance low, large area occupations are required.

5.3.5 Full-wave voltage rectifier optimization

The two NMOS gate cross-connected devices M_1 and M_2 are both isolated mid-oxide transistors as for the case of D_1 and D_2. However, they are not affected by the body effect since the bulk and the source are connected together.

These type of transistors have higher channel resistances R_{ON} and gate charges Q_G which lead to higher power dissipations and high frequency switching losses.

The optimization of the voltage rectifier circuit is based on the tradeoff between the size and the parasitic capacitances of the transistors. Indeed, as shown in Fig.5.10 (a), small transistor geometries lead to small parasitic capacitances which in turn reduce the switching losses and increase the PCE. Despite this advantage, as shown in Fig.5.10 (b), small geometries have higher channel resistances and thus the total conduction path resistance R_T has higher values which deliver less current to the load.

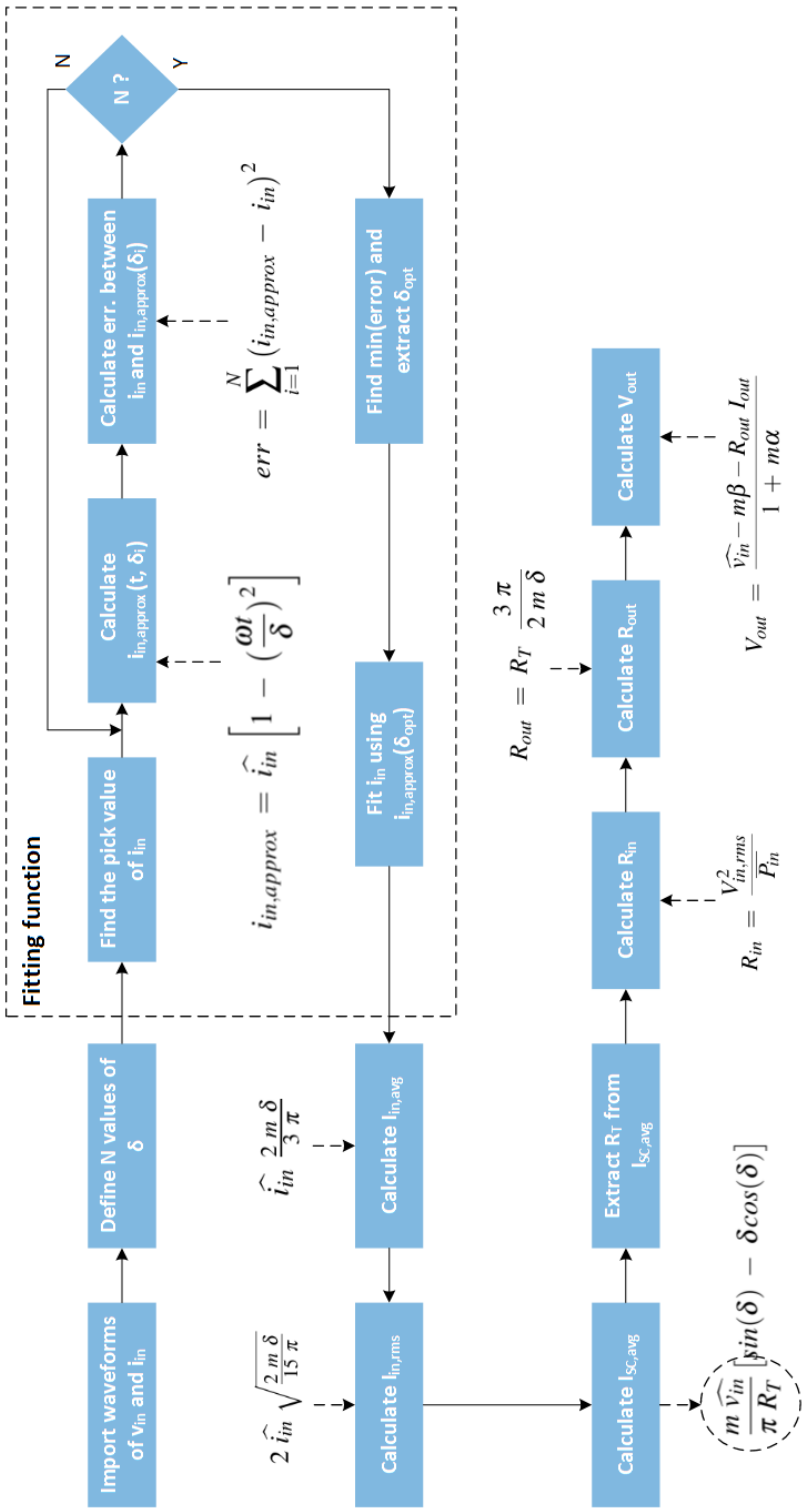


Fig. 5.9 Fitting procedure according to the parabolic approximation of the input current.

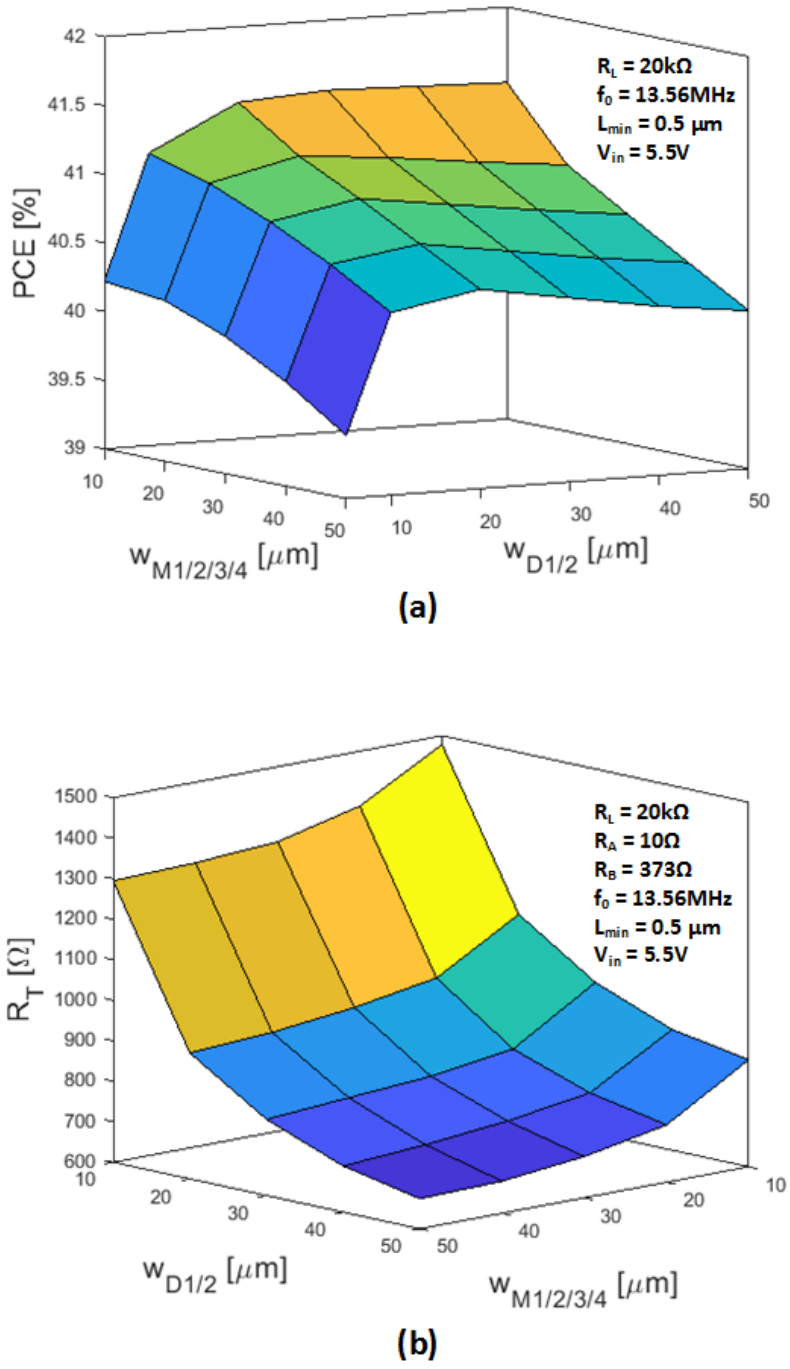


Fig. 5.10 (a) Power conversion efficiency (PCE) and (b) total conduction path resistance R_T. Both relative to the widths of the bridge and diodes transistors for an input voltage amplitude of 5V.

The values of R_T have been extracted using the parabolic approximation method explained above. It can be seen that R_T is mainly dominated by the channel resistance of the diode-connected transistors (D_1 and D_2) since, in steady state, their V_{GS} voltages are reduced because of the output voltage V_{out}. The bridge transistors M_1 and M_2 instead, have constant voltage swings between gate and source of approximately $\widehat{v_{in}}$ leading to lower channel resistances.

The PCE show optimum values when the width of D_1 and D_2 are approximately 20 μm. This may let thinking about a design optimization point, however, maximum and minimum PCE values are very close together and optimum PCE values do not necessarily lead to low R_T. For this reason, in this work, PCE is not the only figure of merit for the VR design but rather a tradeoff between PCE, load power requirement in conjunction with the total conduction path resistance R_T and the area occupation.

Switching losses

The analysis and the modeling of the switching behavior of the gate cross-connected bridge formed by M_1 and M_2 is a complex task mainly because of non-linear characteristics of parasitic capacitances.

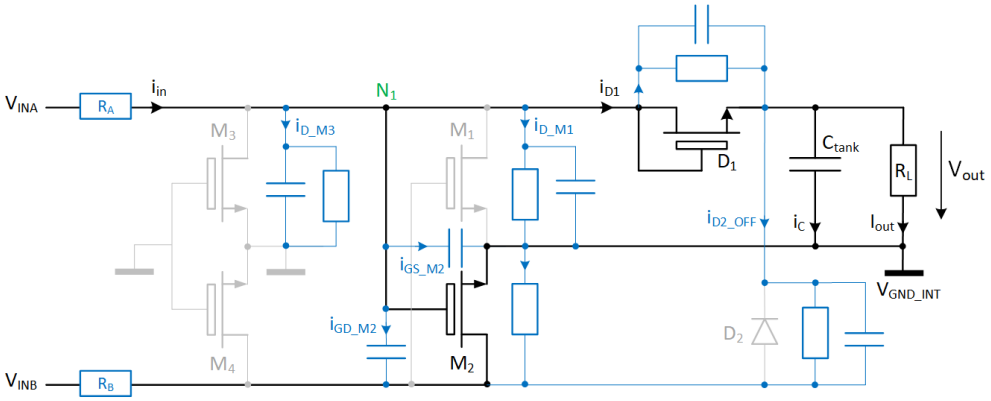


Fig. 5.11 Full-wave NMOS gate cross-connected bridge voltage rectifier circuit with parasitic elements for switching and conduction losses during positive half-wave.

As shown in the detailed schematic of Fig.5.11, during the positive half-wave, the input current i_{in} can be calculated summing currents at the node N_1:

$$i_{in} = i_{D\_M3} + i_{D\_M1} + i_{D_1} + i_{GD\_M2} + i_{GS\_M2} \tag{5.37}$$

where, as shown in Fig.5.13, i_{D_M3} is the drain current of the transistor M_3 (which is OFF and used for the load modulation with M_4), i_{D_M1} is the drain current of the transistor M_1 (which is OFF), i_{D_1} is the diode parabolic current that charges the output capacitor C_{tank} and the gate current, constituted by i_{GD_M2} and i_{GS_M2}, are the gate-to-drain and respectively the gate-to-source currents. For wide transistors, the latter two currents have the largest contribution to the switching losses. Indeed, they strongly depends on the parasitic capacitors C_{GD} and C_{GS} according to the following expression:

$$i_{G\_M2} = i_{GD\_M2} + i_{GS\_M2} = C_{GD}\frac{dV_{GS}}{dt} + C_{GS}\frac{dV_{GS}}{dt} \tag{5.38}$$

where in this case, the internal reference potential V_{GND_INT} is considered constant and thus both capacitors have the same AC voltage.

As already explained and shown in Fig.5.12, using the parabolic approximation method, switching losses are considered as the difference between *rms* values of the input current and the current extracted from the parabolic approximation according to Eq.5.8.

The fitting window is chosen in order to best fit the simulated (or measured) current inside the conduction period. The deviation between the approximation and the simulated charging current is reported in the lower part of Fig.5.12 for wide transistors. It can be seen that the largest deviation occurs in the right side (with respect to the 0 reference point) of the input current. This can be explained by the fact that the lower part of current shape is not perfectly parabolic but rather relaxed due to parasitic capacitors. In addition, the parabolic approximation is zero outside the conduction period leading to large deviation. Nevertheless, for the specified conditions, rms values only deviate of $\approx$ 1% which is more than acceptable for the purpose of this analysis.

If the total conduction path resistance (Fig.5.10 (b)) and the output current (Fig.5.14 (a)) are dominated by the R_{ON} of the diode-connected transistors, the conduction losses (Fig.5.14 (b)) are dominated by transistors M_1 and M_2 and to a lesser extent by the two load modulation transistors M_3 and M_4.

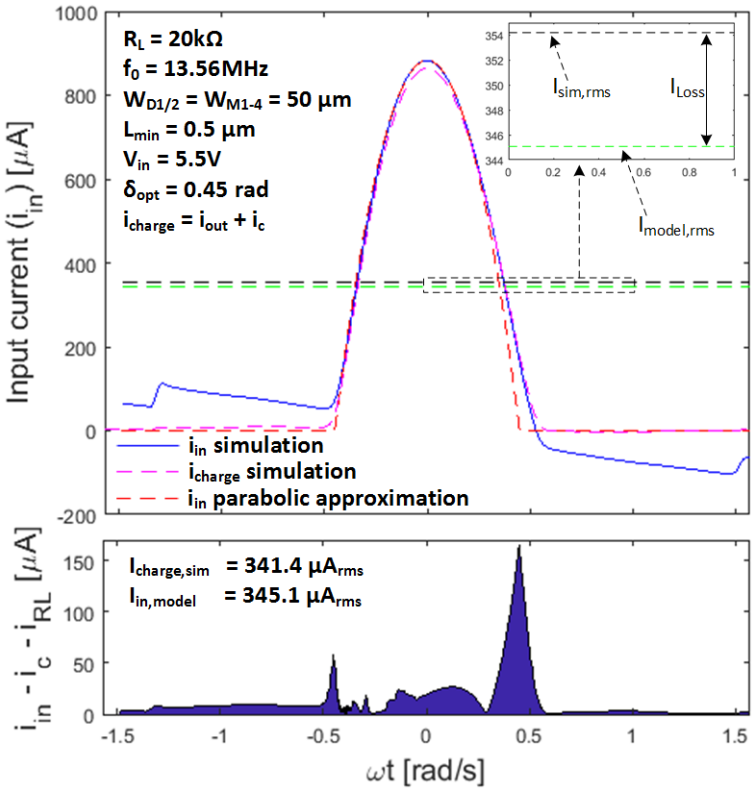


Fig. 5.12 Simulation input current and parabolic approximation fitting with rms current deviation from simulations to model.

At this point, combining simulation results together and the parabolic approximation, dimensions of each transistor can be optimized according to the following procedure:

1. define the load power requirement defining output voltage and average current,
2. define the maximum total conduction path resistance R_T complying with the load power requirement of point 1,
3. maximize the width of the diode-connected transistors according to area occupation constraints,
4. verify power conversion efficiency and switching losses,
5. and choose the width of M_1 to M_4 according to previous points.

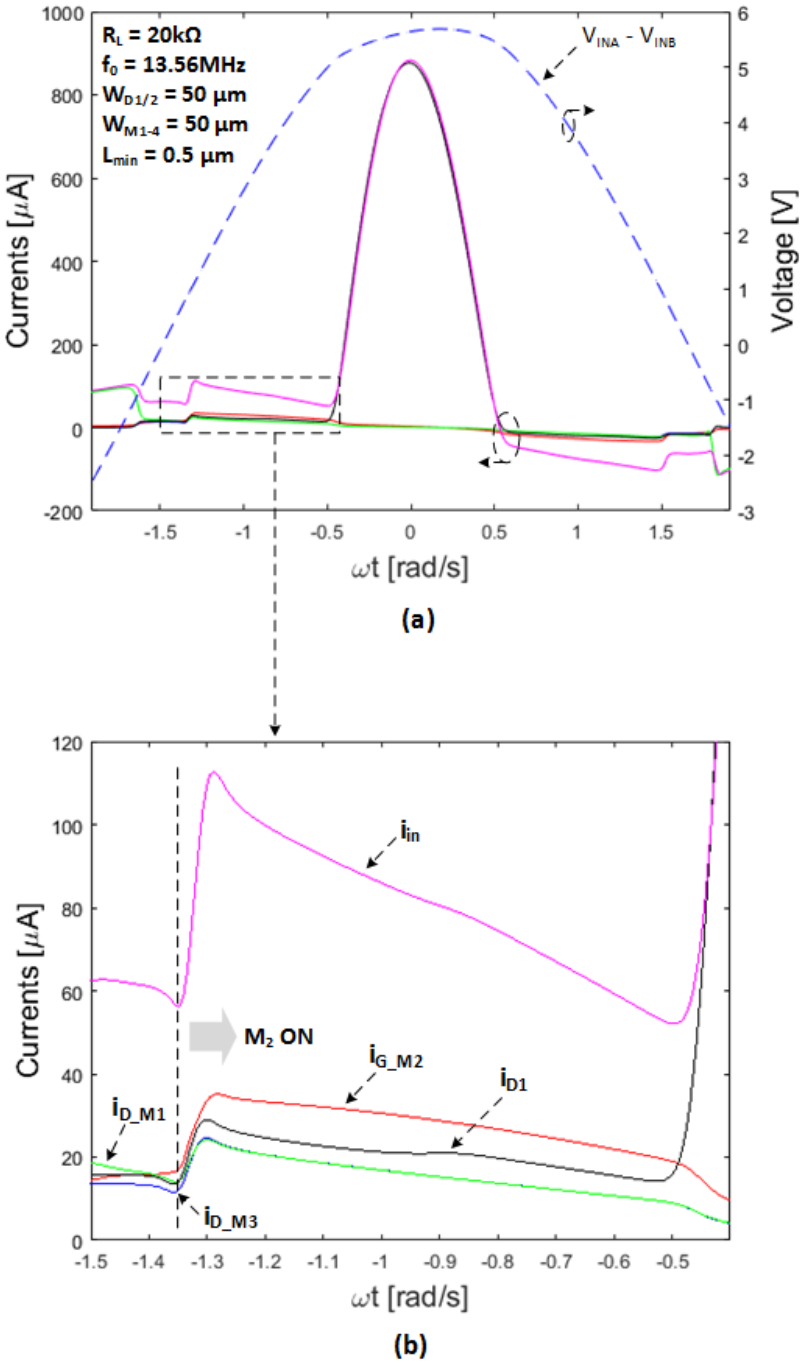


Fig. 5.13 (a) VR input voltage (right axis) and various currents showing the input parabolic current and switching losses due to wide transistors. (b) detail of point (a) showing gate and drain currents during the positive half-wave.

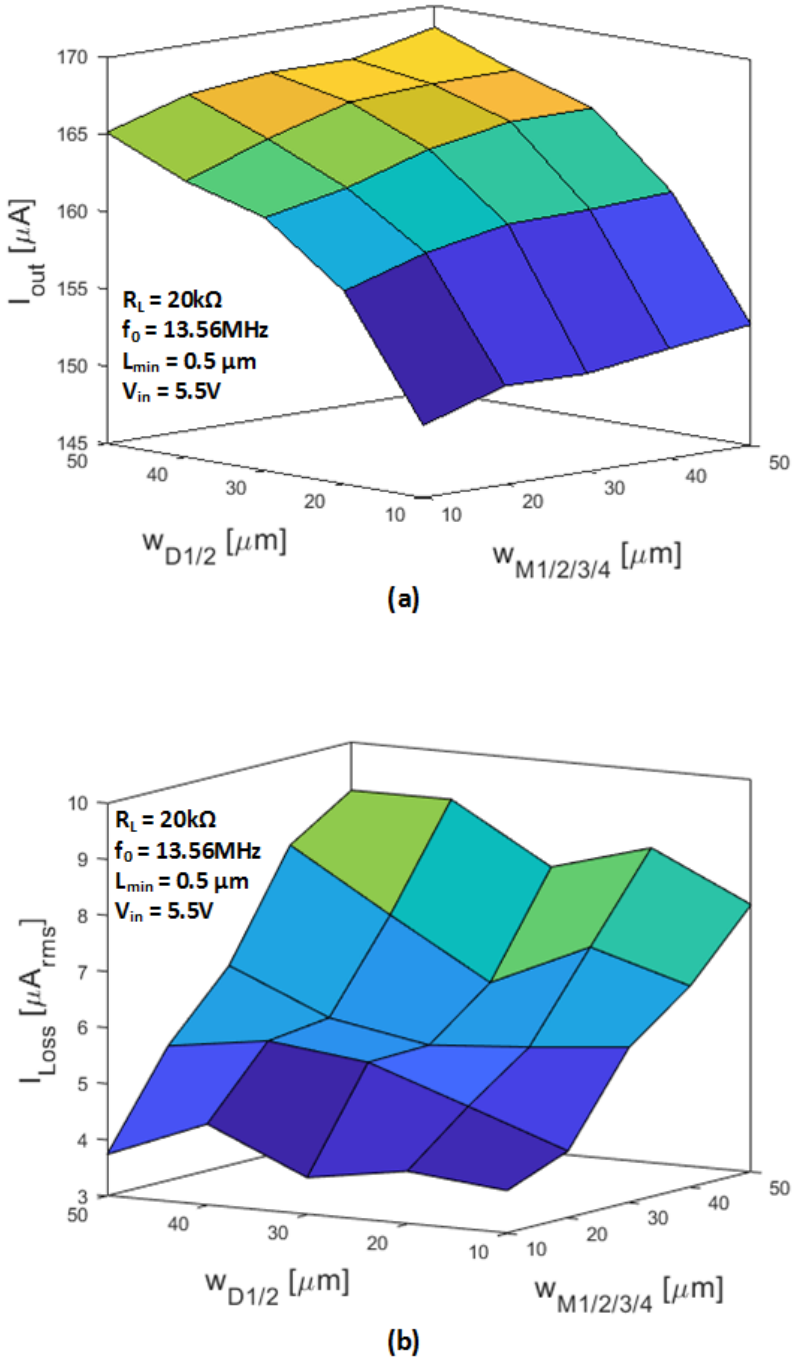


Fig. 5.14 (a) Average output current of the simulated VR circuit under specified conditions. (b) Simulated conduction and switching losses.

Layout considerations

During the layout phase, some considerations need to be taken in to account for reducing as much as possible feed-through parasitic currents capacitively coupled to the voltage rectifier structure. In Fig.5.15, layout induced parasitic capacitors (red dashed line) have been included into the gate cross-connected bridge circuit.

Reconsidering again the node N_1, three additional currents can be summed:

$$\begin{aligned} i_{RA} &= i_{D\_M3} + i_{FT\_3} + i_{FT\_4} + i_{D\_M1} + i_{FT\_5} \\ &\quad + i_{D_1} + i_{GD\_M2} + i_{GS\_M2} \end{aligned} \tag{5.39}$$

where i_{FT_3}, i_{FT_4} and i_{FT_5} are the feed-through parasitic currents which couple to: i) the output capacitor bank, ii) the substrate contact and iii) the internal voltage reference (internal gnd). Depending on their value, these capacitors lead to transient currents outside the conduction period.

The capacitor C_{FT_3} is represented in Fig.5.16 (b) between the highest metal layer (MET4) and the second polysilicon layer (POLY2) of the output capacitor bank. As shown in Fig.5.16 (c), the distribution of the power supply (VDD) increases the effective coupling area of the capacitor bank, leading to lower performances. This depends on the interconnection density, which in turn, is related to the complexity of the chip.

The transient current, shown in Fig.5.17 (b), generated by C_{FT_3}, contributes to the charging up of the tank capacitor slightly boosting the output voltage. Nevertheless, after the conduction period, negative transient currents discharge more rapidly the tank capacitor finally leading to lower average output voltages and thus lower PCE. Values of C_{FT_3} well below 1 pF, have a marginal effect.

The transient current generated by C_{FT_5} has the same behavior, however, as shown in Fig.5.17 (c), this current does not contribute to the charging up of C_{tank} but only to switching losses decreasing the PCE. In comparison to the previous case, the capacitor C_{FT_5} has a much lower coupling area, in fact, the first polysilicon layer (POLY1), connected to the internal ground, is covered by the POLY2. Therefore, the value of C_{FT_5} is mainly given by the ground distribution as shown in Fig.5.17 (d).

Considering the node N_2, the current flowing into the VR circuit can be defined as it follows:

$$i_{in} = i_{FT\_1} + i_{FT\_2} \tag{5.40}$$

where the feed-through parasitic current i_{FT_1} represents the coupling to the surface of the substrate. The capacitor responsible for this current is followed by a large resistor. The latter is not calculated using Eq.5.28 since not connected to a low resistivity diffusion.

The current i_{FT_2} instead flows directly to the substrate contact, which is, as shown in Fig.5.17 (b), large for reducing the substrate resistance and thus the total conduction path resistance. As shown in Fig.5.17 (a), large values of C_{FT_2} induce currents that contribute to the switching losses but does not charge up of the output capacitors.

5.4 Experimental

An experimental setup, shown in the lower part of Fig.5.20, has been designed to evaluate electrical performances and to verify the agreement between measurements, simulation results and the parabolic approximation model.

The chip has been wire-bonded directly on a test PCB and the silicon substrate has been attached onto a gold electrode using a conductive epoxy in order to allow the substrate conduction.

The intrinsic diodes of the high voltage isolated structures are connected between the output voltage and the deep NWELL (DNTUB). During the negative half-wave, when the output voltage is lower than the input, these diodes are in forward bias and depending on the DNTUB dimension, currents, in addition to the one of D_2, flow into the load. These currents are approximately comparable during the initial transient period, whereas in steady state, as shown in Fig.5.18 (a), currents flowing into the intrinsic diodes are more significant.

The parabolic procedure previously explained has been applied for extracting the total conduction path resistance from the measurements. An external capacitor

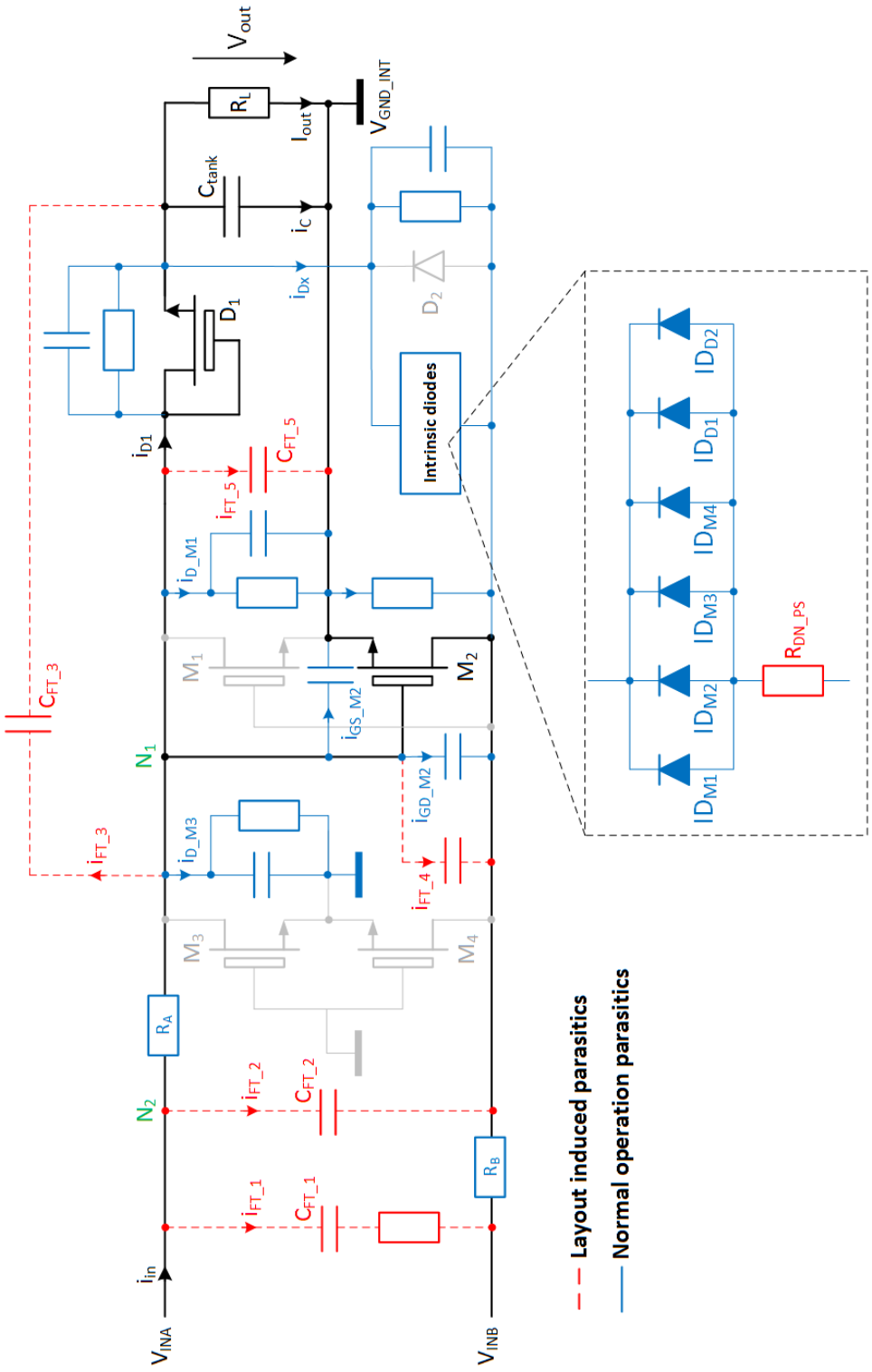


Fig. 5.15 Full-wave NMOS gate cross-connected bridge voltage rectifier circuit with layout induced and normal operation parasitic elements.

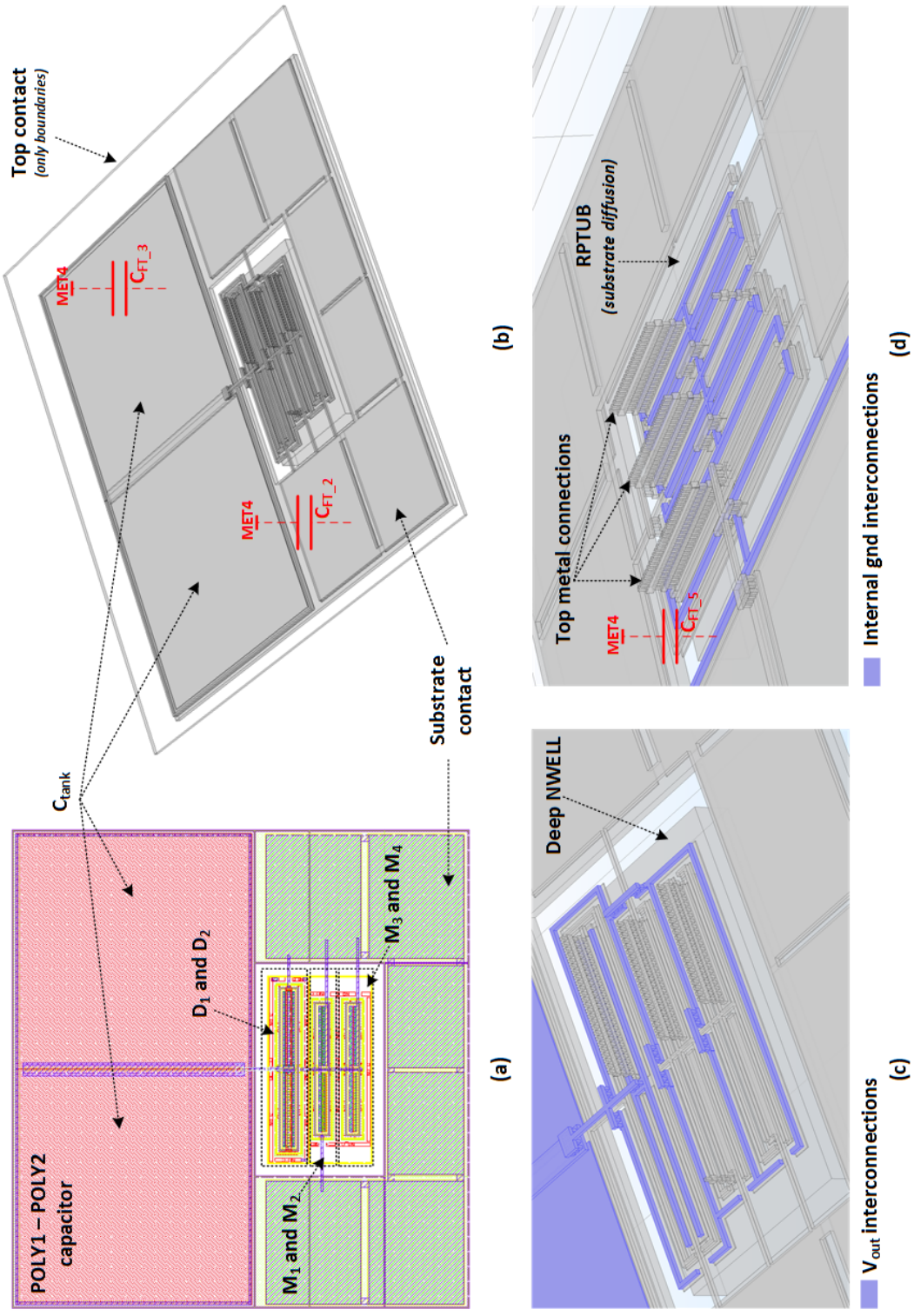


Fig. 5.16 (a) Layout 2D view of an implemented voltage rectifier circuit. (b) 3D view of the VR circuit of (a). Interconnections highlighted in order to extract the total feed-through capacitor for: (c) the output voltage and (d) the internal ground.

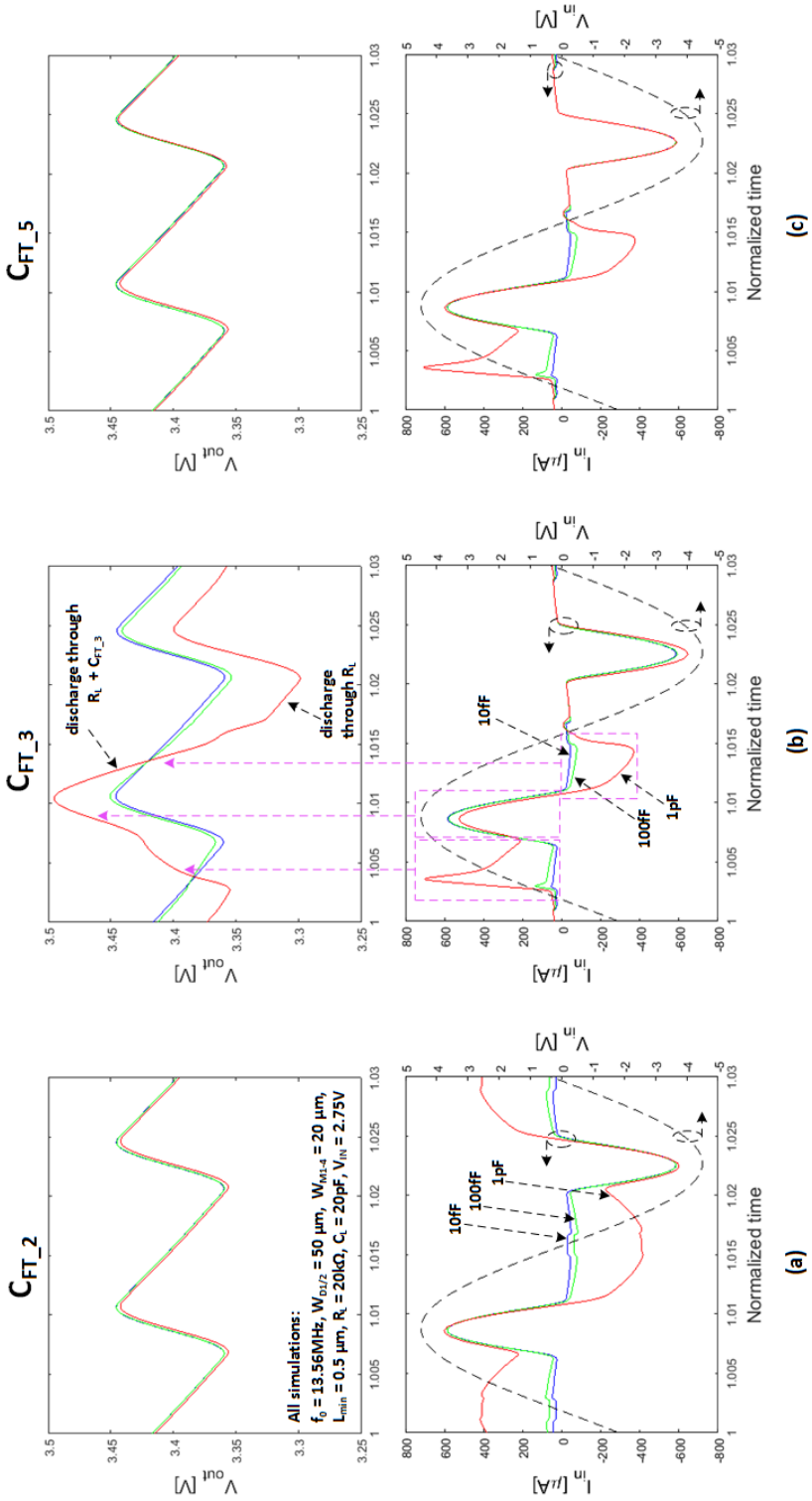


Fig. 5.17 Steady state analysis with: (a) switching losses induced by C_{FT_2}, (b) switching losses and output capacitor charging due to C_{FT_3} and (c) switching losses induced by C_{FT_5}.

of 40pF has been added in parallel to the load in order to reduce the output voltage ripple and thus have a better parabolic fitting. The input current has been processed for both the positive and negative half-wave. Results are reported in Fig.5.19.

In order to ensure a good fitting, data points around the pick current of the positive half-wave have been smoothed using a moving average filter. The extracted conduction path resistance is 1.12 kΩ whereas the simulated value is 974 Ω which represent approximately 13% of deviation. This deviation can be considered reasonable taking into account the accuracy (from 15% to 5% accuracy) reported in [14, 115].

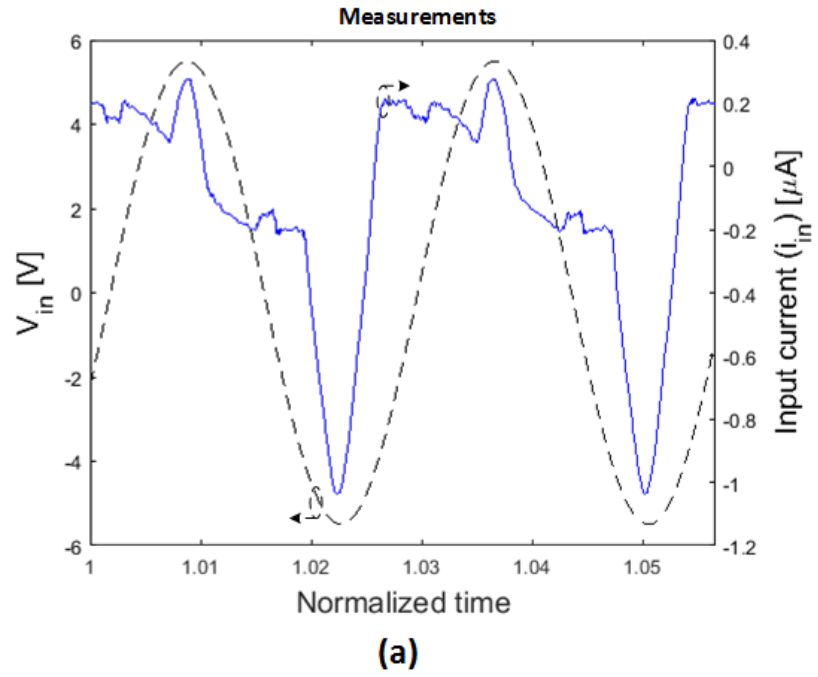
During the negative half-wave, the equivalent conduction path resistance is lower. In this case, most of the current flows into intrinsic diodes and the transistor M_1 which means that the channel resistance of the diode D_2 is considerably bypassed. The extracted value of R_T is, in this case, 867 Ω.

5.5 Summary

In this chapter a steady state analysis of the voltage rectifier circuit has been carried out. The input current has been analyzed by applying a parabolic approximation during the conduction period. This approach simplify considerably the large signal analysis and above all it allows the extraction of the total conduction path resistance. This is of great interest for this work since the silicon substrate is part of this conduction path and its resistance is not well-known because of the lack of knowledge about doping profiles with associated resistivity. The total resistance extracted from the measurements show a reasonable (< 15%) agreement with the Comsol model.

The layout induced parasitic capacitors have a marginal role for the small test structure implemented in this thesis, however, careful analysis needs to be undertaken for larger implementation with a high density interconnection and large output capacitor banks.

The maximum output voltage reached is slightly above 3.5 V. This is just enough for powering up the 3.3 V internal circuity, nevertheless, under load modulation conditions, this voltage is insufficient. For this reason, finer technologies (e.g. AMS 0.18 μm) with power supply voltages of 1.8V will be considered for future implementations.



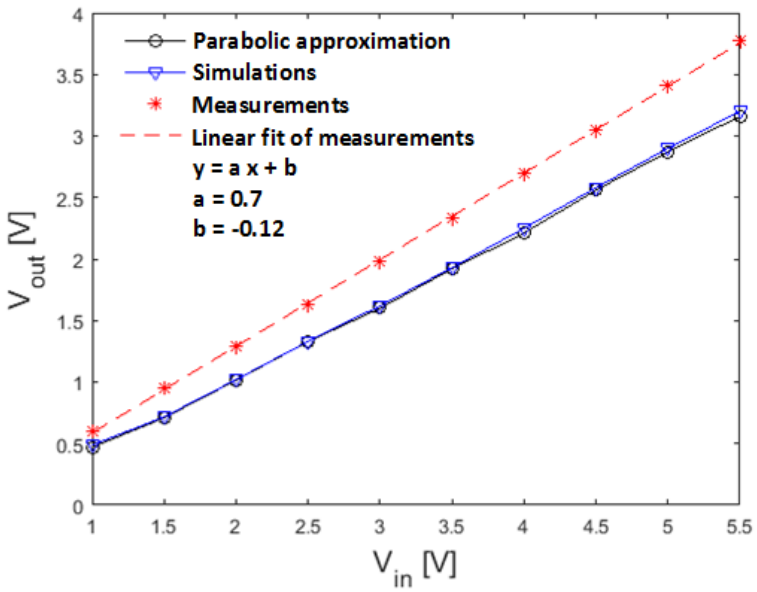


Fig. 5.18 (a) Measurement of the input current and voltage. (b) Measurements, simulations and parabolic fitting of the output characteristic of the voltage rectifier circuit.

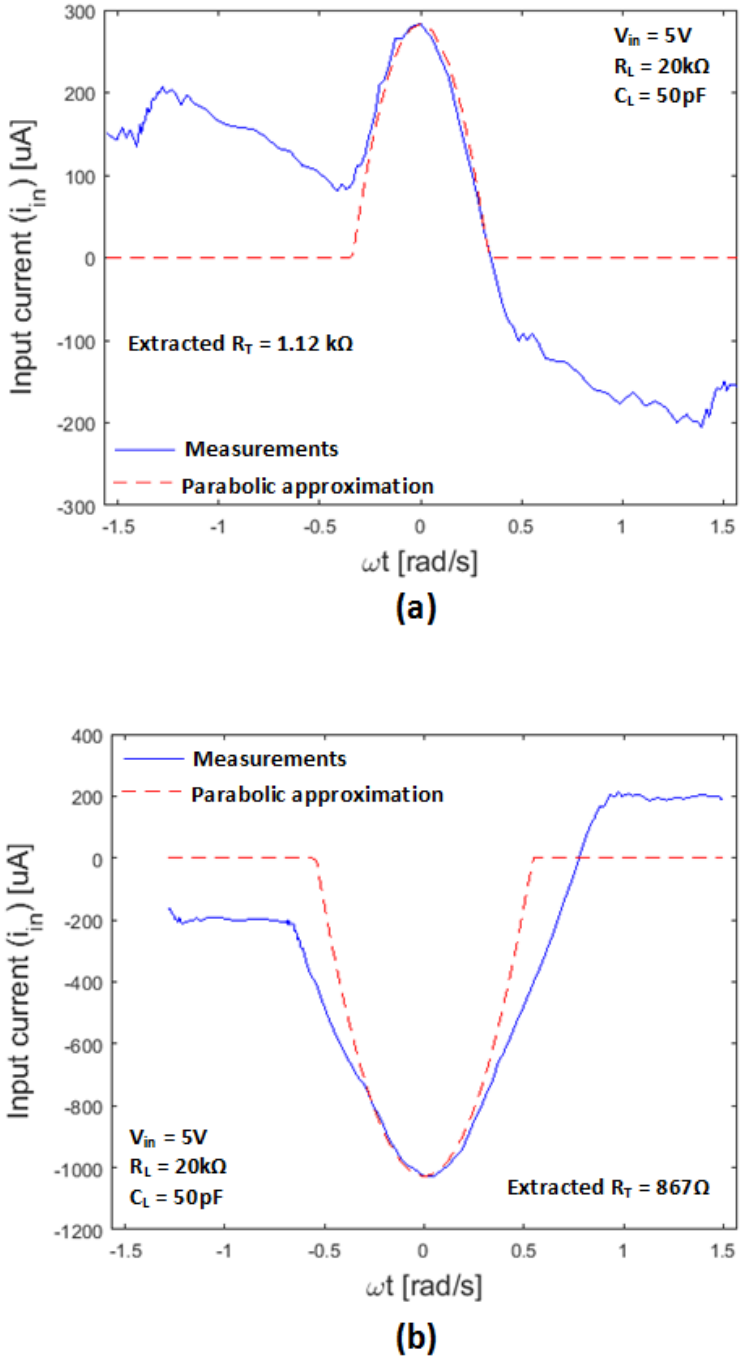


Fig. 5.19 Parabolic fitting of the input current during: (a) positive half-wave and (b) negative half-wave.

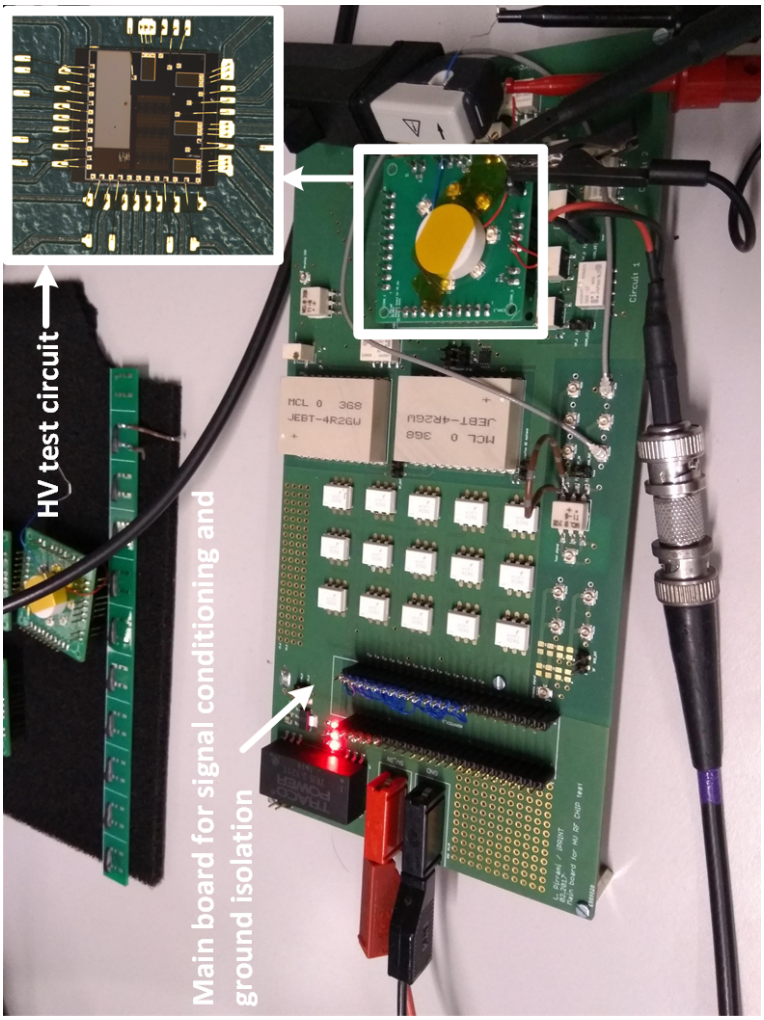


Fig. 5.20 Measurement setup including the test module with wire-bonded high voltage circuits and main board for signal conditioning and ground isolation. The latter board has mainly be developed for latch-up testing. However, this part has not been reported in this thesis since still under test.

Chapter 6

Conclusions

Traditional printing technologies, such as offset, screen and inkjet printing have caused a great industrial interest for reducing fabrication costs of RFID tags. These technologies in mass production environments are able to drive down antenna fabrication costs. However, RFID chip design and testing along with the assembly, still result in a costly manufacturing process.

The costs of RFID chips are essentially related to the silicon area, reason why several research centers, such as the MIT AutoID Center, have invested considerable effort to create RFID chips with less than 8,000 transistors leading to smaller die sizes and reduced power consumption. Nevertheless, in dry environment, such small chips negatively affect the micro handling posing new challenges.

In this thesis, taking inspiration from the digital nature of the inkjet printing technology, a novel fabrication approach for passive RFID tags has been introduced and carefully analyzed. Ideas developed during this thesis have been driven by the need of reducing i) global fabrication costs and ii) the complexity of currently used industrial assembly technologies.

The proposed assembly concept is based on a completely new and creative die-handling technology in which double-surface structured RFID chips are suspended and randomly distributed into a dielectric liquid. These chips consist in having one contact on the top of the chip and the second contact is established by the silicon bulk, as first developed by Hitachi in 2005.

A dedicated system will encapsulate RFID chips, into a microliter dielectric droplet, for the purpose of delivering them (in an inkjet like manner) in correspondence of the RFID antenna. The surfaces of the latter will be specifically treated allowing the spontaneous alignment of chips. Based on the latter point, the wetting contrast between the contact of the antenna (bonding site) and its surroundings has been carefully analyzed. Optimal design parameters have been simulated using the software Surface Evolver which computes static simulations evolving an initial surface towards its minimum. It has been demonstrated that very high contact angles on the substrate lead to the perfect confinement of droplets with respect to the bonding pads of the antenna. However, in this case, the printing of the second layer (closing the antenna loop) may lead to open circuits or to very low coupling capacitance values, hence strong signal attenuation.

To address this problem, it has been demonstrated that the assembly process is feasible without extreme contact angles (e.g. superhydrophobic conditions) on the substrate. In this case, the outwards spreading of the droplet potentially leads to larger chip misalignments. Nevertheless, simulation results show more limited signal attenuation in comparison to the perfect confinement case.

The coupling capacitors, created by the dielectric droplet due to its surface minimization has been analysed through an in-depth analytical model followed by FEM simulations for extracting concrete capacitance values. It turns out that for the perfect confinement case, capacitance values have a large dispersion and related load voltages are strongly attenuated. On the other hand, for more relaxed wetting conditions of the substrate, the capacitance dispersion is considerably reduced giving better electrical performances complying with the ISO/IEC 14443.

This work has also shown that it is possible to rely on standard CMOS technologies for harvesting the necessary energy without the need of expensive and complex post CMOS processes. It has been demonstrated that a compact, single stage and high voltage rectifier circuit is able to produce a sufficient output voltage of 3.3V with load down to 20 kΩ with 10pF of output capacitor. Nevertheless, future implementations will be developed using a finer technology with a power supply voltage of only 1.8 V allowing load modulations.

Experimental tests for evaluating possible latch-up triggering conditions in the silicon bulk need to be undertaken. Regarding this point, test structures, not reported in this thesis, have been fabricated and are currently under test.

In conclusion, the author would like to mention that optimizations of capacitive coupling is still in progress. In fact, specific geometric features, embedded on the substrate along with the contact of the antenna, are currently under investigation for minimizing the dielectric layers between the chips and the antenna, hence maximizing the power transfer efficiency.

In addition, the delivering system concept has recently benefited from a research grant. This dissertation is therefore only a modest first step towards the fabrication of ultra-low cost passive RFID tags.

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