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# SETA: A CAD tool for Single Event Transient Analysis and Mitigation on Flash-based FPGAs

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***Abstract*—Flash-based Field Programmable Gate Array (FPGA) devices are nowadays golden cores of many applications especially in space and avionic fields where reliability is becoming an important concern. In particular, for Flash-based FPGAs when adopted in those applications, the main concern is radiation-induced voltage glitched know as Single Event Transient (SET) in the combinational logic. In this work, a new CAD tool has been developed in order to evaluate the sensitivity of the implemented circuit regarding SET and to mitigate their effects. The proposed tool has been applied to an industrial design adopted by the EUCLID space mission including more than ten different modules. The experimental results demonstrated the feasibility and efficiency of proposed tool.**

***Key words*—Flash-based FPGAs, CAD tool, Single Event Transient.**

## I. Introduction

When Flash-based FPGA is used in mission critical application, dependability of such device is becoming an important issue. One of the most critical environmental aspects that could lead to the failure of these systems is radiation. Due to the charge deposition of particles striking the device, a voltage glitch known as Single Event Transient (SET) is induced. This voltage glitch can propagate through routing and logic resources of the circuit that it may reach and be captured by a sequential element, such as Flip-Flop (FF). The SET sampled by a FF may corrupt the values previously stored causing a bitflip which in turn can propagate to misbehavior of the target design [1].

Several studies have focused on the evaluation of SET propagation using electrical simulation [2]. Even though these methods are effective to analyze the propagation of SET pulses, they do not evaluate the broadening or filtering effect of the SET pulses traversing logics and routings resources knowing as Pulse Induced Propagation Broadening (PIPB) [3]. In addition, those approaches are time consuming, thus not efficient to be applied to an industrial design flow with enormous amount of resources.

Different mitigation solutions have been proposed in the past. Solutions based on gate filtering apply mainly on benchmark circuits without considering timing and resource overhead constraints [4].

The main contribution of the present work is the complete identification of the SET propagation scenario. Thanks to the developed CAD methodology, we are able to cover the possible pulse propagation cases and its relevant PIPB effects on industrial circuits implemented on Flash-based FPGAs [5].

In this work, we propose a new CAD tool, named SETA, able to interface with the commercial FPGA design flow. Within the proposed tool, SET Analyzer (SETA) part targets the SET propagation and its relevant PIPB effects on circuits implemented on Flash-based FPGAs, while Convergence-SET analyzer (C-SETA) part focuses on overlapping SET pulses scenarios when several SET pulses propagating through several logic paths unit at a convergence node. Also a mitigation algorithm has also been developed for improving reliability of target design based on the SET analysis performed by SETA and C-SETA.

The proposed tool has been applied to a SoC mapped on Microsemi ProASIC3 Flash-based FPGA within the framework of EUCLID space mission project for monitoring the dark space. The experimental results present an evaluation of SET phenomena affecting the circuit during its realistic operational lifetime with mitigation method applied, confirming the efficiency of our proposed CAD tool.

The paper is organized as follows: Section II describes the concept of SET provoked in circuits; Section III presents the developed tools for SET analysis and mitigation; Section IV presents the experimental results; Finally, conclusions are drawn in Section V.

## II. Single Event Transient In Circuits

When a highly charged particle strikes the silicon junction of the device, the produced free mobile carriers are concentrated within depletion region of a p-n junction in one of the sensitive transistor nodes causing a voltage glitch at the output of the transistor, known as Single Event Transient (SET).

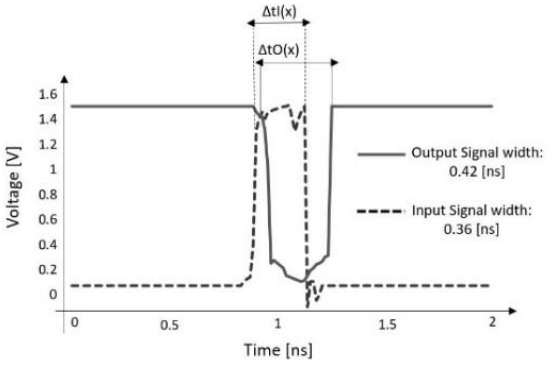


Fig 1. Examples of Transient pulse generation and propagation through Inverter gate.

The induced SET can propagate through several paths in the

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output cone, leading to several SET pulses, which may cause multiple upsets in the circuit if they reach and are sampled by memory storage elements. When the SET pulse traverses a logic gate, it can be modified in pulse width and amplitude, as the example illustrated in Figure 1, where the SET pulse at the input of an inverter is broadened from 0.36 ns to 0.42 ns.

When the SET pulses are traversing the logics and routing resources, it may undergo pulse width modulation known as PIPB effect which is due to delay unbalance at different circuit nodes. However, it can be more critical if during the lifetime of SET, the pulse reaches to a divergence node and propagates through two or more divergence-paths which merge at a convergence node further along the logic path, in which case two different types of phenomena could occur. The former happens when there is a large difference between the propagation delays of the divergence-paths, therefore the SET pulses reaching the convergence node are still regarded as separate pulses, presented in Fig. 2(A). On the other hand, if the delay difference is below certain threshold, it is possible to obtain a Convergence SET (C-SET) which has larger width as a result of two (or more) pulses overlapping, Fig. 2(B).

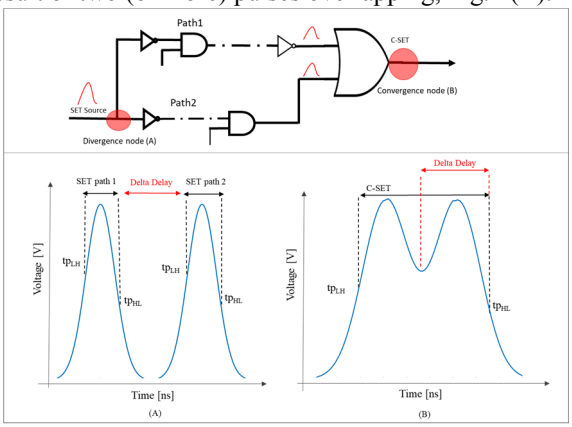


Fig 2. An example of SET propagation effects: multiple independent SETs or C-SET.

Considering the technology advances of Flash-based FPGA, the scaling of node size leads to the higher sensitivity against SET. Thus even the particle with low energy can induce SET when it strike the device [2]. On the other side, the increasing of clock frequency, along with more complex circuit design increase the probability of SETs being sampled [5]. Moreover, the increasing level of complexity of industrial designs such as microprocessors which usually contain thousands of logical gates and storage elements such as FFs connecting together makes it even worse regarding design reliability against SET induced by radiation effects.

## III. The Proposed Tool

The target of the proposed tool is to provide an effective methodology for the analysis of the SET sensitivity taking into account different SET propagation scenarios and for SET mitigation of the circuit designs to be implemented on Flash-based FPGA devices. The tool can be integrated with the standard FPGA design flow, which for our study case is the Microsemi Libero SoC software tool, as illustrated in Fig. 3.

Starting from the Hardware Description of the design, through netlist synthesize, mapping and place and route, the commercial design flow generates the post-layout netlist along with Physical Design Constraints (PDC) and timing information stored in Standard Delay Format (SDF) file. The proposed SETA tool starts from elaborating the post-layout netlist, PDC and SDF file together for building netlist timing graph for SET and C-SET analysis.

The SET analysis implemented by SETA tool takes into account the pulse propagation behavior through the routing and logic resources of the design, generates the SET sensitivity report for all the FFs in the design. Moreover, SETA reports all Gate-to-Gate PIPB coefficient during the propagations of SET pulses. Meanwhile, we extend this analysis to include different scenarios when a SET pulse propagates through divergent paths and when multiple SET pulse traverse a convergent node. The C-SET analysis method elaborates the Gate-to-Gate PIPB coefficient database along with SDF of the target circuit in order to evaluate the sensitivity of the design regarding C-SET phenomena and update the SET sensitivity of the design.

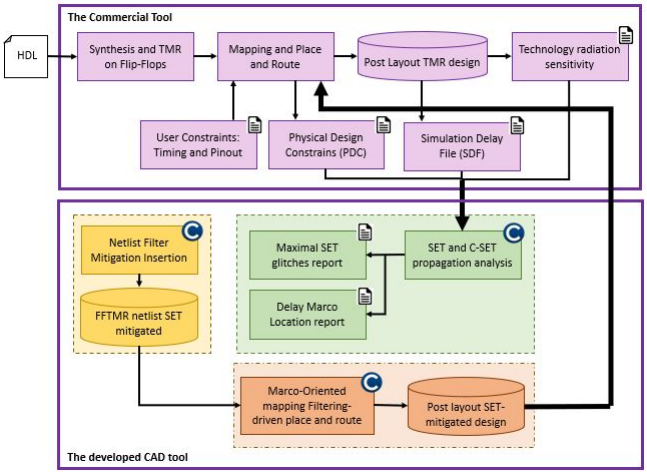


Fig 3. The developed analysis flow for the accurate evaluation of SET effects on SoC implemented on Flash-based FPGAs.

A typical SET mitigation method for Flash-based FPGA inserts Guard Gate (GG) structure at the input of each concerned FF in order to filter the SET pulse. In this case, any SET previously reaching at FF input and having SET width lower than the filtering capability of the inserted GG is nullified. The algorithm optimizes effective SET filtering capability while maintain or reduce the area and performance overhead by carefully selecting the netlist point where to insert the mitigation structure instead of inserting at the inputs of FFs.

### A. SET Analyzer

To evaluate the SET sensitivity of the target circuit design, SETA tool works in two phases: the first phase consists in generation of SET pulses and injecting the generated SET pulses in all the logic resources of the circuit. The SET generation phase provides a list of SET pulses based on the parameters set by user such as voltage amplitude and pulse width. Each pulse is described using 100,000 voltage sample points, allowing a precision of 1 ps.

The second phase elaborates the PDC file containing placement information of the logic resources used in the circuit. Together with logic information extracted from post-layout

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netlist, SETA generates a Physical Design Description (PDD) file for storing the elaborated circuit where I/O pins, FF, RAM or ROM ports are considered as *terminal nodes* and combinational logics as *intermediate nodes* connected through routing segments. There are four different types of routing segments: extra array long line, which contains the longest interconnections between logical nodes; intra array long lines allowing long connections through the whole device; medium lines and short lines for local routing resources [7].

The SET pulses generated in first phase are then injected at each single intermediate node of the design, propagated until a terminal node. During this propagation, based on the type of gates and routing interconnection stored in PDD file, PIPB coefficient is calculated. At the end, SETA tool reports the SET sensitivity for each terminal nodes, in terms of PIPB coefficient and probability of sampled SET causing bitflip.

### *B. Convergence SET (C-SET) Analyzer*

In order to analyze the target circuit regarding C-SET, SETA starts from PDD file and extracts all possible combination of divergent nodes and convergences nodes where C-SET could occur and all the paths between them to identify different C-SET scenarios. With the PIPB coefficient calculated in previous SET analysis and the delay information extracted from SDF file, all the paths are then categorized as whether C-SET will contribute to wider SET pulse and the previous PIPB coefficient information and SET sensitivity report are updated for later mitigation algorithm to optimize balance between SET filtering capability and resource and performance overhead.

The categorization is performed by comparing the total delay of the paths between the divergent node and the convergent node, which includes the delay of all the gates and interconnection/routing segments along the path extracted from SDF file. Considering two paths of A and B as two paths between a divergence and convergence nodes, if the different between the delay of these two paths is less than the duration of the expected SET pulse, one single SET will be observed at the convergence point. However, if the delay difference is close to the width of one of the two SET pulses along the divergence paths, then due to the overlapping of SET pulses, the duration of C-SET could as wide as the sum of widths of two SET pulses. Please note that, during propagation along path A and B separately, the two SET pulse may undergo filtering or broadening depending on the exact composition of the path itself. While if the delay difference is more than the duration of the SET pulse, two separated pulses could be observed at the convergent node.

### *C. SET Mitigation*

The SET mitigation is realized by modifying the original circuit netlist by inserting proper GG structure as illustrated in Fig. 4. Each GG structure is composed of a 3-inputs NAND gate, three 2-inputs NAND gate and parameterized number of inverters INVD gates determined by desired SET filtering capability.

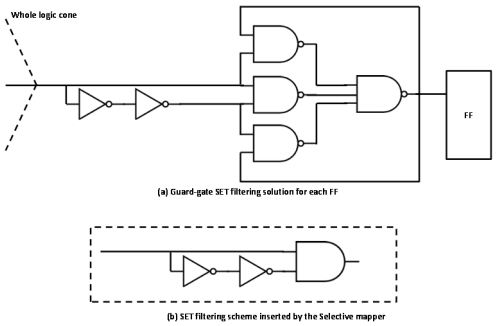


Fig 4. The GG schema for filtering SET at the input of a Flip-Flop (a) and in any position of the circuit (b).

The mitigation algorithm firstly calculates the maximal PIPB coefficient for each used resources according to the results generated by SET and C-SET analyzer. The broadening coefficient is computed for each logic gate as $\Delta B_{logicgate}$ and for each routing net as $\Delta B_{Routing}$. The final PIPB coefficient ($\Delta B_{path}$) of path reaching FF is the combination of all logic gates and routing segments coefficients as illustrated in Fig. 5. A positive value of coefficient corresponds to a broadening effect, while a negative value to filtering of the SET pulse.

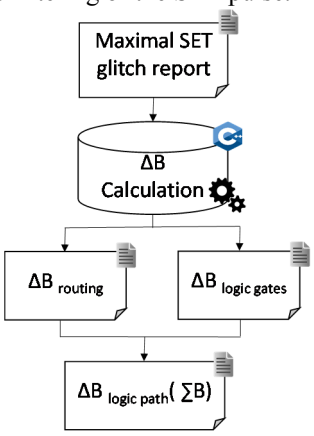


Fig 5. The automatized flow for the computation of the broadening coefficient for each logic path.

As an example, Fig. 6 shows the calculation of the ΔB for the gate G1 and G3 and for the routing segment R1. Based on the coefficients calculated, the tool inserts the GG structure with certain number of INVD determined by user desired filtering capability. The location for GG insertion is optimized for filtering capability while maintain or reduce overhead, thus not necessarily at the input of FF, as illustrated in Fig. 7.

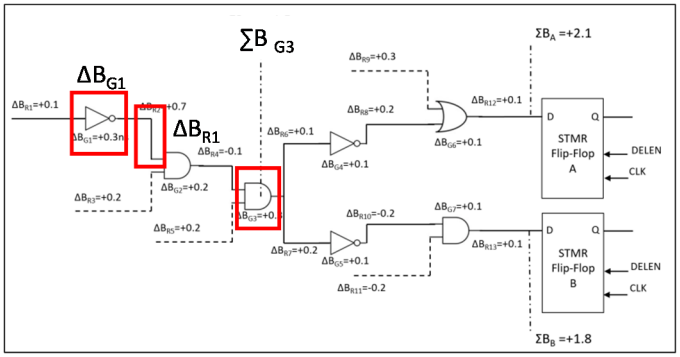


Fig 6. Identification of gate and routing considered for guard-gate insertion.

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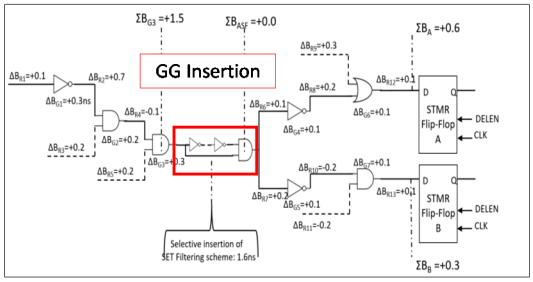


Fig 7. Insertion of SET filtering element within a circuit structure.

## IV. Demonstration and Results

The proposed methodology has been performed on a SoC embedded in EUCLID space mission designed for monitoring dark space. Microsemi ProASIC3 A3P3000 Flash-based FPGA device has been used for implementing EUCLID circuit while Microsemi Libero SoC 11.7 is used as the design tool in order to implement the EUCLID design and export the input files for SETA tool.

The Euclid space environment has been also characterized considering SET events and determining that longest SET is of maximum 0.9 ns. Therefore, we set the filtering capability to maximum of 0.9 ns. Please notice that the GG filtering capability is not necessarily set to 0.9 ns due to PIPB effects and the glitch rejection capability of the FFs. The characteristics of different implemented versions are described in Table I, including the plain unmitigated circuit, the Triple Modular Redundancy (TMR) applied and the TMR version with proposed tool applied. In Fig. 8, it is illustrated a demonstration of GG insertion within the Euclid design.

TABLE I. EUCLID DESIGNS USED RESOURCES

| Euclid Design | Sequential [#] | Logic Gates [#] |
|---|---|---|
| Plain | 5,907 | 27,826 |
| Euclid TMR | 17,719 | 31,782 |
| Euclid TMR + GG | 17,719 | 48,625 |

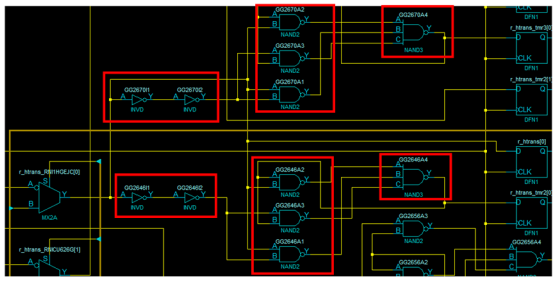

Fig 8. An example of Guard-Gate automatic insertion on a portion of the Euclid Design.

The performance overhead introduced by the proposed tool, reported in Table II, is maintained that the previous timing constraints are still satisfied. It is interesting to notice that our approach is not affecting high frequency domains. In fact, the performance remains almost identical to the plain (original) implementation. Please note that the frequency drop of the clock domain at 60 MHz (CLK60) for the Euclid TMR implementation is due to the inefficient placement rules that were not being applied to that implementation. Vice versa, the Euclid TMR + GG includes placement constraints to force the timing characteristic of each guard-gate structure and thus maintaining the timing property almost identical to the plain design.

TABLE II. EUCLID DESIGNS WORKING FREQUENCIES

| Euclid Design | CLK60 [MHz] | CLK_30 [MHz] | CLK_70 [MHz] | CLK_20 [MHz] |
|---|---|---|---|---|
| Plain | 81.4 | 35.4 | 79.4 | 39.4 |
| Euclid TMR | 66.4 | 30.3 | 71.5 | 34.8 |
| Euclid TMR + GG | 81.9 | 30.3 | 78.8 | 33.4 |

The CRÈME96 and our SETA tool have been used to evaluate the Euclid circuit SET sensitivity in terms of error cross-section for the two most resilient versions: our approach and the previous state-of-the-art solution with TMR and SET filtering. In details, we analyzed the integral fluence expected for the nominal duration of the mission, which is 6.25 years. In order to perform the SET error estimation, we normalized the CRÈME96 data for each single ProASIC3 Versatile and routing segment. The SET normalized cross-section coefficients have been elaborated with the SET tool applied to the post-layout netlist of the target design. For the unmitigated version, we obtained a normalized transient error cross-section of 1.77E-4, while for the mitigated version (TMR+GG) we achieved a normalized transient error cross-section of 2.42E-7. Please notice that for EUCLID design which is occupying 70% of ProASIC3 A3P3000 FPGA, the CPU time for the analysis of one SET has been measured in 23 hours.

## V. Conclusions

In this work, we presented a new CAD tool for improving design reliability regarding SET for circuits implemented on Flash-based FPGAs. The developed tool has been evaluated on a realistic SoC design for the ESA EUCLID space mission for monitoring the dark space. Experimental results demonstrated a reduction of three order of magnitude of the overall SET sensitivity, while all narrow SETs were completely filtered.

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