On-line Junction Temperature Estimation of SiC Power MOSFETs through On-state Voltage Mapping

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***Abstract*—This paper deals with real-time estimation of the junction temperature of SiC power MOSFETs. The junction temperature of one device of a 4-switch module is real-time estimated by measuring its current and on-state voltage V_{ON} at each switching period and entering the temperature look-up table of the device. The temperature model is preliminarily obtained in a dedicated commissioning session, where the V_{ON} is measured at different temperature and current conditions. The results show the feasibility of on-line temperature monitoring and even active limitation of the junction temperature of the tested SiC power MOSFET modules, accurately and with an instantaneous dynamic response. Different modules with die from different manufacturers were tested in a H-bridge demonstrator power converter, emulating the operating conditions of real converters such as voltage source DC/AC or DC/DC conversion structures. The commissioning procedure is meant to be performed directly on the final application for each converter. The proposed temperature estimation technique is validated against a thermal camera and compared to direct measurement of the die temperature with a thermistor, showing high accuracy and high feasibility.**

Index Terms*— *SiC power MOSFET, Junction temperature monitoring, On-state resistance, On-state voltage, TSEP.

I. Introduction

The failure rate of power semiconductors is closely related to their junction temperature during operation, which in many cases is known very approximatively through a temperature sensor placed into the power module. Despite the efforts of the scientific community and power module manufacturers, the measurement of the junction temperature of power semiconductor devices is still a challenge. Over the years the problem has become more important due to the further increased power density of the new devices such as Silicon Carbide (SiC) power MOSFETs [1], [2] and [3].

According to [4], the methods currently used to evaluate the temperature of power semiconductors devices are divided into optical methods, physical contact methods and electrical methods. Each approach has its own strengths and weaknesses. The methods of the first class are based on the detection of optical proprieties of the semiconductor, which are temperature dependent, or more simply on the acquisition of the thermal image of the semiconductor die through an infrared camera. This class of techniques can achieve a high level of accuracy and provide a thermal map of the semiconductor die, from which the points of maximum temperature and the gradient of temperature across the die are easily determined. However, all such methods need visual access to the chip, the removal of the dielectric gel and extra computing resources to process the thermal image. Physical contact methods put the die in direct contact with a thermo-sensitive material (e.g. thermocouples or thermistors). This approach requires mechanical access to the die inside the module and has a limited accuracy and dynamic response, as also confirmed by the results of this paper. Electrical methods are based on the detection of thermo-sensitive electrical parameters (TSEP). The most significant techniques in this field are based on the evaluation of switching times or on the threshold voltage of the body diode [4] and [5]. Other techniques rely on a thermal-electrical model of the component [6]. Most of the TSEP techniques require complex calibration, and this makes their application to commercial converters impractical. Furthermore, all the techniques based on the evaluation of the switching times are hardly implementable on SiC devices, where the commutations are extremely fast and data acquisition noisy. Nevertheless, the knowledge of the junction temperature during operation is a powerful source of information for many purposes, including protection, diagnostics and full exploitation of the device safe operating area.

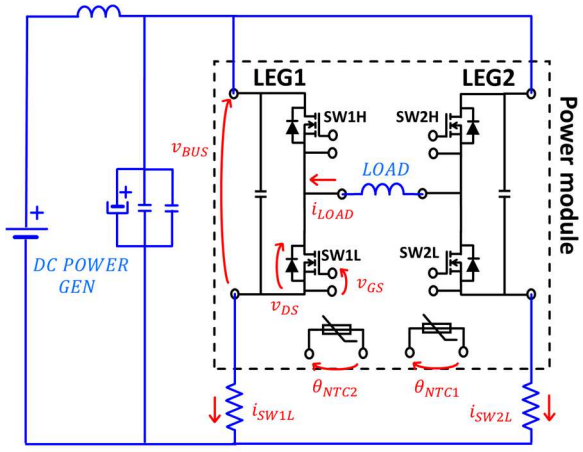


Fig. 1. Schematic diagram of the proposed setup: red quantities are measured online.

This paper presents a technique for the estimation of the junction temperature of a SiC power MOSFET, with high

accuracy and dynamics, applicable to all types of switching converters, either DC/AC or DC/DC. This work is the extended and reviewed version of [7]. The schematic of the setup used for this proof of concept study is shown in Fig. 1. It consists of an H-bridge power converter made with a custom Emipak 2B module, courtesy of Vishay Semiconductor Italiana, equipped with additional sensors for the measurement of the on-state current and voltage of one of the four power devices of the module. The junction temperature model is built via the initial commissioning of the on-state voltage of the monitored power switch, whose output is a look-up-table defining the on voltage as a function of the junction temperature and conducted current. The look-up table is then used for on-line determination of the junction temperature.

The strengths of the proposed method deal with its simplicity and accuracy. In turn:

- The converter commissioning does not need dedicated equipment like a curve tracer: it can be performed directly on the final application.
- Temperature detection does not affect the converter operation with either noise injection or additional parasitics.
- Temperature detection has a fast-dynamic response.
- No complex computation is involved.
- Hardware modifications are minor and non-costly.

TABLE I - RATINGS OF THE EXPERIMENTAL SETUP

Maximum RMS Load current	40 A
Maximum DC Voltage	1000 V
Maximum Switching frequency	500 kHz
Electrolytic capacitors (total)	1120 µF
Film capacitors	10 µF
Ceramic capacitors (SMD)	300 nF
Inductive load	22 to 176 µH
Microcontroller	STM32F429ZI
12-bit A/D channels of the MCU	3
12-bit A/D converters on the power board	5
On-board SDRAM memory	64 Mbit
Adjustable plate temperature	30°-150°C
V_{GS}	-5/+20 V
Power Module, type #1 (from datasheet)	
Rated current (Tsink=80°C)	19 A
Breakdown voltage	1200 V
R_{ON} @ 25°C, 20A	78 mΩ
$C_{internal}$	2 x 47 nF
Max Junction Temperature	175°C

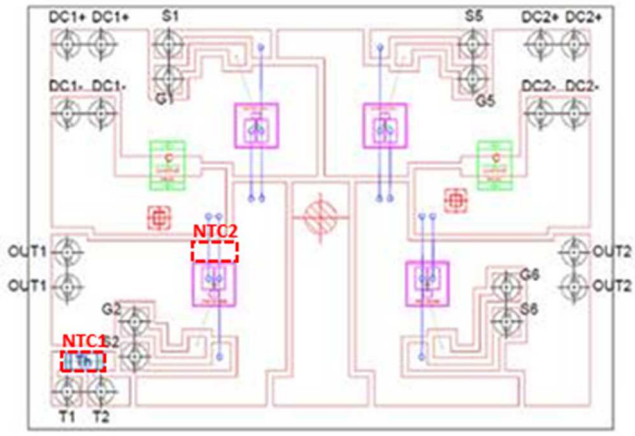
II. TEST SETUP

Fig. 1 reports the schematics of the power section. As said, the custom Emipak 2B power module of Fig. 2-a is connected in H-bridge configuration, and supplies a purely inductive load. This mimics real operating conditions while absorbing a fraction of the converted power from the input DC source. The load current is closed-loop controlled by one leg of the module (LEG2), while the other leg (LEG1) is open loop controlled at a fixed duty-cycle, to mimic a constant voltage load. Details can be found in [8]. The power module is monitored electrically and thermally, as detailed in the next paragraphs.

A. Custom Power Module

Fig. 2-b shows the internal layout of the power module. Two capacitors are embedded into the module (green rectangles), to minimize the stray inductance of the power loop. The standard embedded thermistor NTC1 indicated in the figure is the one used for measurement of DBC substrate temperature, also called the “case temperature” in the text.

a)



b)

Fig. 2. a) Power module package. b) Internal layout of the power module (courtesy of Vishay Semiconductor Italiana). Green: Internal capacitors. Magenta: SiC MOSFET dies.

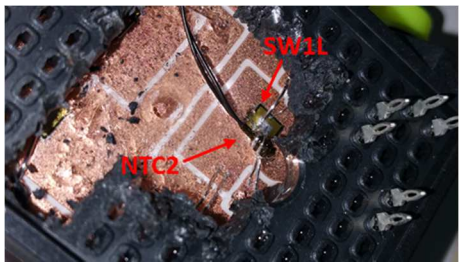


Fig. 3. Placement of NTC2 thermistor.

Moreover, one additional thermistor (NTC2) was later put in direct contact with the die of the MOSFET under monitoring, as depicted in Fig. 3. Both NTC1 and NTC2 have a full scale of 145°C.

Different modules with die from different manufacturers where tested. For simplicity, this paper refers to **one manufacturer (called type #1) and one size only**. Datasheet

values, referred to in Table I, where provided by Vishay Semiconductor Italiana.

B. Power Converter Description

The prototype converter built to validate the proposed method is depicted in Fig. 4, from top to bottom we find: the control board, the gate-driver boards and the power board. The heatsink, partially visible in the low part of the picture, has two fans for ventilation and four resistors for pre-heating the power module and impose the case temperature during the commissioning stage. The control board was designed for easy plug-in of one STM32F429 Discovery demo board, used for real-time control and data collection purposes. The Discovery board embeds the ARM Cortex-M4 microcontroller unit STM32F429ZI, and was chosen for its onboard 64 Mbit SDRAM memory, used for PC communication during the debug phase. The control board includes one LEM current transducer used for closed loop control of the load current, and a resonant high frequency power generator which provides insulated power distribution to the gate drivers and additional A/D converters placed on the power board.

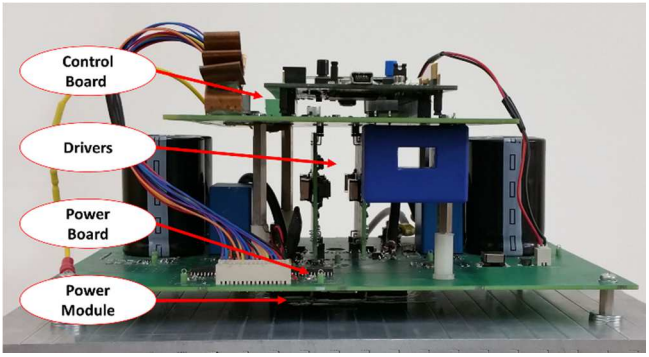


Fig. 4. Picture of the experimental setup.

The gate-driver boards, one per module leg, are sandwich-connected between the upper control board and the lower power board. Such 3-dimensional arrangement permits to minimize the distance between the drivers and the power module and therefore to minimize the parasitic inductance of the gate driver circuit. The gate-driver boards are based on the intelligent driver STGAP1S, that offers programmable fault check and hardware protection thresholds.

The power board houses the DC link electrolytic capacitors visible in Fig. 4 and five additional A/D converters. These sample the electrical quantities v_{GS}, v_{DC}, v_{DS}, i_{SW1L}, i_{SW2L} indicated in red in Fig. 1. The trigger of A/D synchronization is provided by the MCU. Each A/D converter communicates with the MCU through a dedicated opto-isolated SPI connection.

C. Measurement of the on-state drain-source voltage

Special attention was paid to the measurement of the on-state voltage drop V_{ON} of the monitored switch SW1L. The schematics of the signal conditioning circuit is reported in Fig. 5. Diode D8 protects the signal circuit from the DC-link voltage when the MOSFET SW1L is OFF while the diode D9 is used to compensate the voltage drop of the diode D8.

When the SW1L is in ON state, the diodes are forward-biased by injection of a constant current and the drain-source voltage V_{ON} turns into the output signal ADC, to be sampled by the dedicated A/D unit. For guaranteeing that the forward voltage drops of the diodes are identical, the bias currents are obtained from a current mirror. Moreover, the diodes are placed close to each other on the board (see Fig. 6), so that temperature variations might affect their voltage drop to the same extent. The operational amplifier U15 is an OPA 357 with an output voltage slew-rate of 150 V/µs, for fast transition between saturated and linear states at every commutation of the power component.

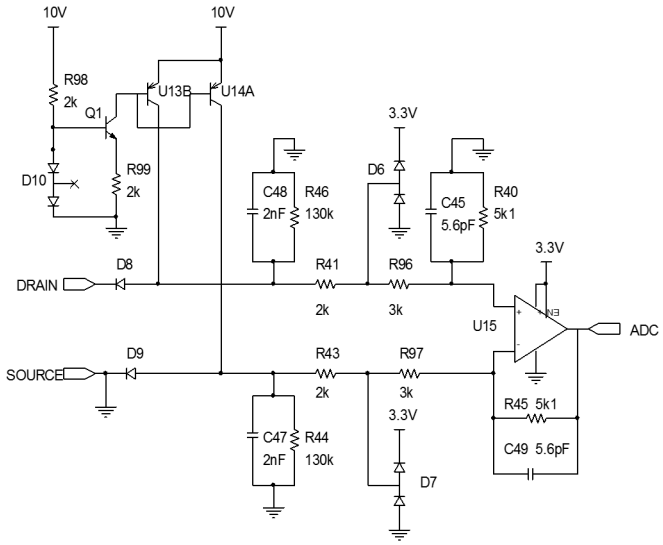


Fig. 5. Schematic of the analog conditioning stage dedicated to the V_{ON} measurement.

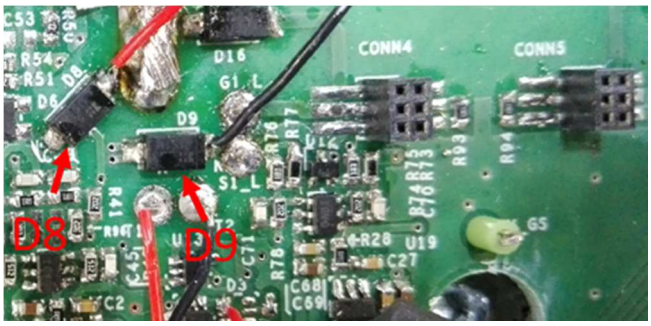


Fig. 6. Detail of the PCB board with the two diodes very close to eachother.

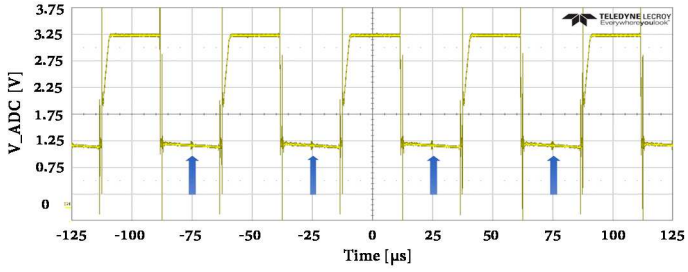


Fig. 7. ADC output of the op-amp in Fig. 5 (25µs/div, 500 mV/div). The switch SW1L is commanded at 50% duty-cycle. Arrows indicate the sampling time.

Fig. 7 shows the conditioned V_{ON} voltage (label ADC in Fig. 5) during operation, with a duty cycle around 50% and i_{DS}>0. When the switch SW1L is OFF the ADC voltage is clamped to the upper rail voltage of the op-amp, equal to 3.3 V. The blue arrows indicate when the V_{ON} is sampled by the A/D converter.

In this setup, the voltage conditioning circuit was off-line calibrated for producing precise identification curves for the modules under test. **However, if the proposed commissioning methodology were applied to a commercial converter, this would not require precise calibration of the drain-source voltage.** Other solutions for measuring the V_{ON} are feasible, like the one presented in [9].

D. Current sensing

The current sensing circuit consists of a shunt resistor, with a signal conditioning circuit that is very similar to the one used for the V_{ON} sampling (another operational amplifier in differential configuration that measures the voltage across the shunt resistor). Other types of current transducers can be used, provided that their bandwidth guarantees that the current and V_{ON} measurement are perfectly synchronized and not distorted.

III. Commissioning and Temperature Estimation

First, the on-state voltage drop of the MOSFET under test SW1L is characterized as a function of junction temperature and on-state current. The obtained model, in the form $V_{ON}(I_{DS}, \theta_J)$ is then used for real-time estimation of the junction temperature during operation. A similar concept of temperature monitoring was proposed in [10] for CoolMOS devices, but without addressing the dependency of R_{ON} (same as V_{ON}) from the drain current, and using calibration data either using the datasheet of the component or a curve tracer. The proposed setup uses the V_{ON} probe on-board of the converter both for the commissioning of the model and for the online temperature estimation.

A. Description of the Commissioning Process

The characterization of V_{ON} versus the junction temperature θ_J and drain current i_{DS} is done by imposing a series of current pulses of short duration to the switch under test. The sequence is repeated for different values of the DBC (Direct Bonded Copper) temperature of the module. The DBC temperature is measured via the embedded NTC1 thermistor.

The commissioning process can be schematized as follows:

1. The heatsink is preliminarily heated using four external resistors, until the NTC1 embedded thermistor outputs 145°C. Therefore, the resistors are turned off and the heatsink starts cooling slowly and the identification sequence begins.
2. A set of twenty-eight current pulses of 100 µs duration each is imposed to the load and thus to the monitored MOSFET, from 1 A to 28 A as showed in Fig. 8. This takes 3 seconds altogether.
3. Every time that the NTC1 temperature drops by 5°C a new set of current pulses is imposed. The wait time between one temperature level to the next one is in the order of the minutes.
4. The test stops when the heatsink reaches the room temperature is (25°C in this case). The total commissioning time for this prototype is around 20 minutes.

B. Timing of the Pulse Sequence

The short duration of the current pulses (100 µs per pulse) ensures that the junction temperature equals the NTC1 reading, i.e. **the junction and the DBC temperatures are equal.** This is confirmed by the thermal impedance of this module, reported in Fig. 9. The transient thermal impedance of this module for a DC pulse of duration 100 µs is 0.03°C/W, to say that the junction to DBC temperature difference during one current pulse is $\Delta\theta_J$ < 3.06°C, in worst case conditions (V_{ON} = 3.64 V, i_{DS}=28 A, θ_J=145°C, P_{ON} = 102 W). This temperature spread is small enough to assume that the junction and DBC temperatures are equal when V_{ON} and i_{DS} are sampled and stored at each pulse.

Moreover, the time lag of 100 ms (1000 times the pulse duration) between the current pulses cancels any residual temperature perturbation, ensuring that the junction temperature returns to the current DBC temperature value, before the next pulse occurs

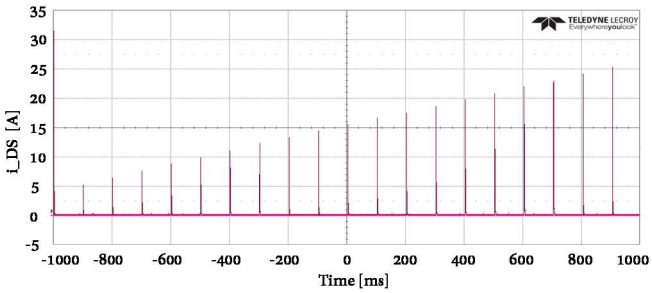


Fig. 8. Example of current pulses used for commissioning of $V_{ON}(I_{DS}, \theta_J)$. Scale of i_{SW1L} is 5 A/div, time scale is 200 ms/div.

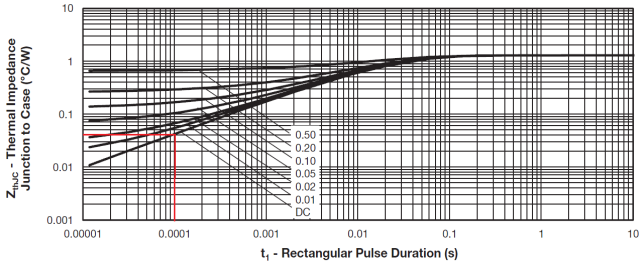


Fig. 9. Maximum thermal impedance Junction-to-Case Characteristic (courtesy of Vishay Semiconductor Italiana).

C. Results: V_{ON} look-up table

Fig. 10 shows the results obtained from the current pulse test at different temperature. Fig. 11 shows the corresponding V_{ON} surface of the power module under test. The V_{ON} voltage as function of current and junction temperature. For the sake of clarity, Fig. 12 and Fig. 13 report the same results in the form of R_{ON} parametric curves, as a function of temperature and current, respectively, with the other quantity used as a

parameter. According to Fig. 12, the R_{ON} sensitivity to junction temperature is significant. For example, the resistance increases by 84% when passing from 25°C to 145°C. Conversely, the sensitivity to the load current is less pronounced, as shown in Fig. 13. As depicted in Fig. 12 the R_{ON} values from the datasheet are higher than the measured ones. This is expected because the datasheet refers to typical values of a series of devices, with some margin on the safe side. The datasheet does not give any indication about the sensitivity of R_{ON} to the current. Other die from different producers were tested, still within custom EMIPAK-2B modules, proving the consistency of the proposed setup and methodology [8].

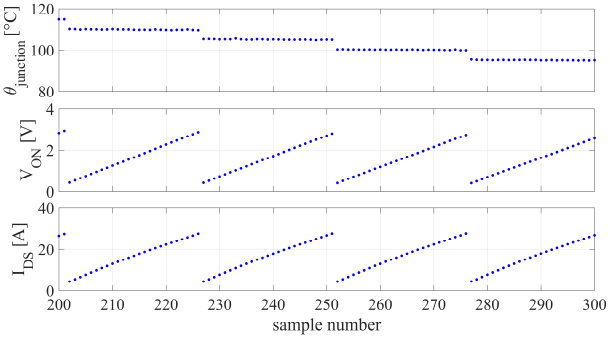


Fig. 10. Results of the commissioning: 28 current and voltage values per temperature value.

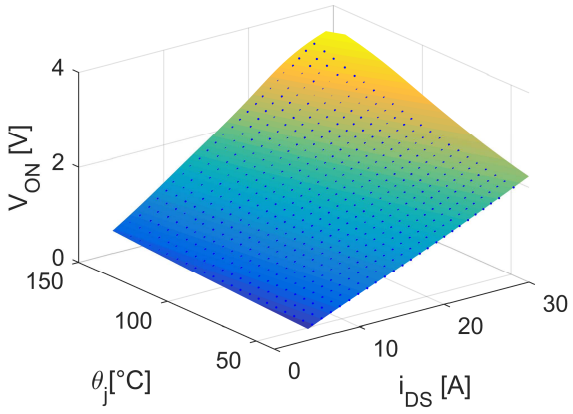


Fig. 11. Measured *Von* as a function of junction temperature and current.

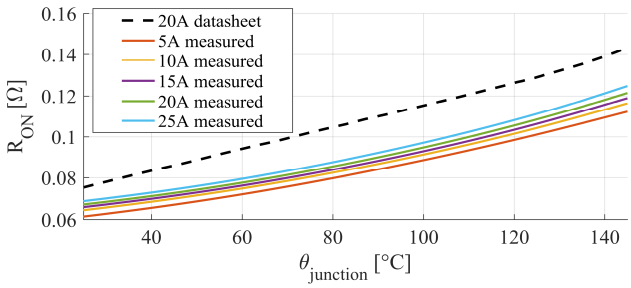


Fig. 12. *Ron* as a function of junction temperature.

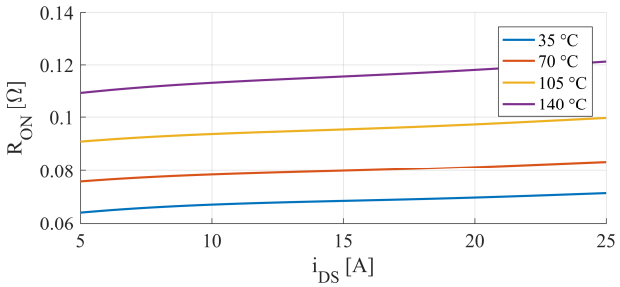


Fig. 13. *Ron* as a function of current.

D. Data Manipulation

The data obtained from the commissioning test must be manipulated before being used for temperature estimation. In its final form, the model will have the current and voltage samples as inputs, and the estimated junction temperature as the output. For building such a look up table it is necessary to reorganize the experimental data according to regularly spaced vectors in the input domain I_{DS}, V_{ON}. Fig. 14 shows the experimental data reorganized in the forms $\theta_J(i_{DS}, V_{ON})$ and $\theta_J(i_{DS}, R_{ON})$, respectively. The second representation is arguably easier to interpolate on a square, regular domain of the inputs i_{DS}, $R_{ON,}$ and will be utilized in the following. The experimental data are therefore interpolated in the form $\theta_J(i_{DS}, R_{ON})$ using a polynomial function of the second degree, ending up with the regular LUT used later for temperature estimation.

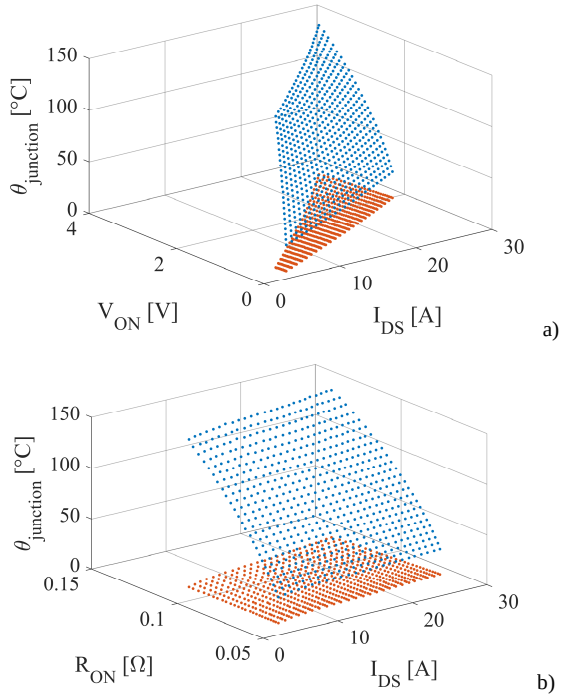


Fig. 14. Experimental data reorganized for having θ_J on the z axis. a) θ_J (V_{ON},I_{DS}). b) θ_J (R_{ON},I_{DS}).

E. Online Monitoring of Junction Temperature

The block diagram of the temperature monitoring scheme is represented in Fig. 15. The on-state current and voltage of the device are measured at each PWM period, and the temperature is estimated accordingly. The index (k) in Fig. 15 indicates the current time sample t_k of the digital controller.

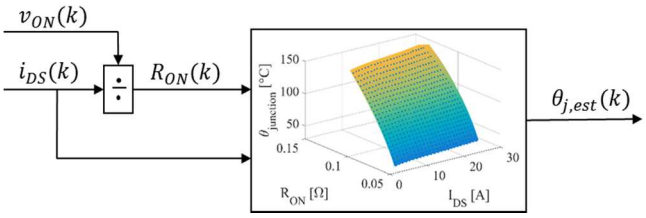


Fig. 15. Block diagram of the proposed on-line temperature monitoring.

IV. RESULTS

The temperature estimate method is tested in different operating conditions, referring to different waveforms of the load current. Closed-loop temperature limitation is also presented, using the temperature estimate as feedback for load current limitation. Additionally, the results coming from the embedded thermistor NTC1 and the local thermistor NTC2 are compared and commented, showing the insensitivity of the commissioning method to the position of the thermistor in the module. Finally, the method is validated against a thermal camera, showing good matching both in steady state and transient conditions.

A. Load Current Step Response

Fig. 16 reports the response of the junction temperature estimate to a square-wave load current. The results show that the DBC temperature during the test is constant (dashed blue line) and the junction temperature responds to the load with a time constant of some tenth of second. The junction to DBC temperature difference reaches 60°C within one second.

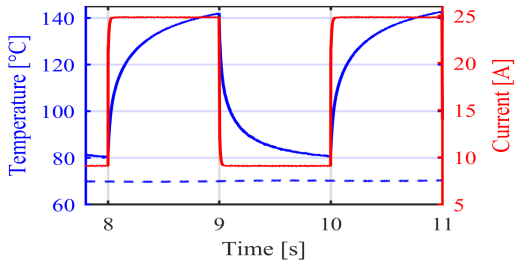


Fig. 16. On-line estimated junction temperature of SW1L (blue continuous), under squarewave load current (red) conditions. The dashed blue line is the DBC temperature, measured from NTC1.

B. Direct Temperature Measurement via NTC2

Besides the standard DBC thermistor NTC1, an additional sensor named NTC2 was later included for direct measurement of the die temperature of SW1L (Fig. 3). NTC2 is placed as close as possible to the die, right under the bonding wires. The direct die measurement NTC2 was compared to the proposed temperature measurement in different operating conditions.

Fig. 17 reports the temperature response to a 25 A load step, showing that the reading from NTC2 gives a bad estimate of the junction temperature, both in terms of steady-state values (steady-state underestimate is around 45°C in this test) and dynamic response (time response of NTC2 is slower than estimation).

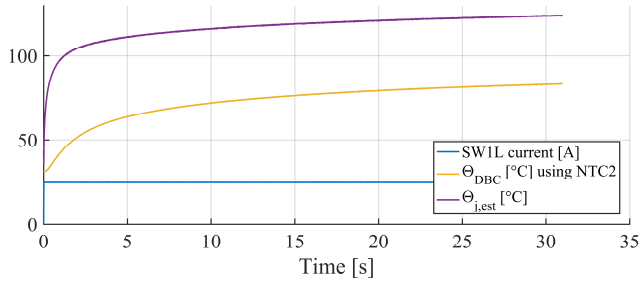


Fig. 17. Current step of 25A. Comparison between junction tmeperature estimate and direct-contact measurement with NTC2.

Similar conclusions can be drawn after the DC + AC load current test of Fig. 18. A 5 A peak current component at 0.1 Hz is superimposed to the 20 A direct current of previous test. Also in this case, the NTC2 output is underestimated both in average and peak values, and delayed respect to the junction temperature estimate. Such underestimate and delay have to do with the thermal impedance between the thermistor and the junction of the device. Although the thermistor is in direct contact with the die, it is not able to capture the intimate junction temperature due to the non-negligible thermal impedance between the surface of the die and the thermistor itself. This result is consistent with the literature [1].

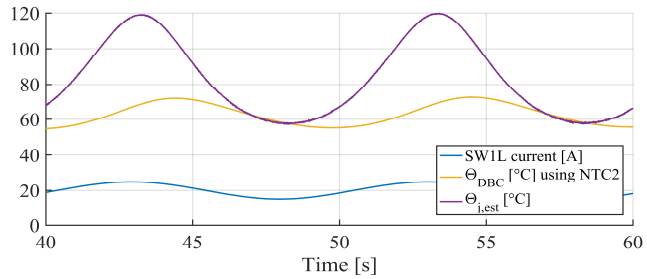


Fig. 18. AC current at 0.1 Hz superimposed to 20 A DC. Comparison between junction temperature estimate and direct-contact measurement with NTC2.

C. Insensitivity to the Placement of the Thermistor

As NTC2 cannot be considered for direct measurement of the device temperature, it has been used as another DBC thermistor, placed very close to the device. The characterization of the module has been repeated using NTC2 resistor instead of NTC1, producing a second V_{ON} look-up table. The look-up table is identical to the one obtained using NTC1, shown in Fig. 11. The load tests of Fig. 17 and Fig. 18 where repeated running the temperature estimates coming from the two tables in parallel, for the sake of comparison.

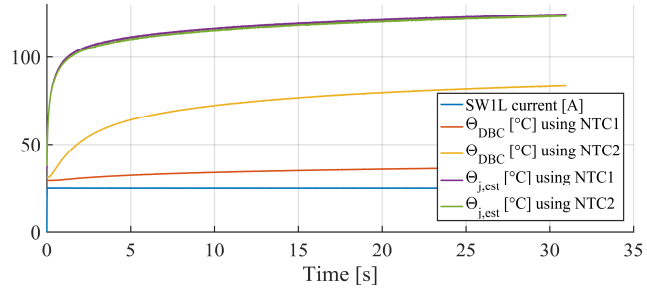


Fig. 19. Junction temperature estimation during a current step of 25A

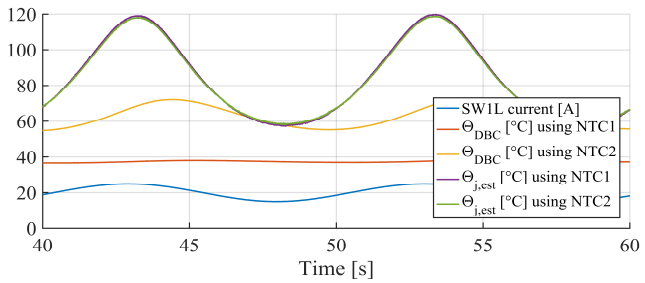


Fig. 20. Junction temperature estimation with sinusoidal current reference

The results of Fig. 19 and Fig. 20 show that the two table-based estimates are superimposed, the one coming from the former look-up table obtained with NTC1 and the new one using the look-up table obtained with NTC2.

The results show that the characterization of the module is insensitive to the placement of the NTC sensor within the power module. In other words, the positioning of the thermistor within the module, and its distance from the monitored switch are not critical for the proposed commissioning and temperature estimation method. Power modules already equipped with internal thermistors do not require hardware modifications.

D. Closed Loop Limitation of the Junction Temperature

The on-line estimation of θ_J is used here for closed-loop limitation of the junction temperature during operation at variable load conditions. A PI regulator was used to saturate the load current reference when the estimated temperature reaches a predefined maximum value. This is not intended as the final use of the proposed monitoring technique, but it is considered a valid stress test for demonstrating the potential and high dynamic response of the proposed estimation technique. The modulation frequency is 10 kHz, so that switching losses are not significant.

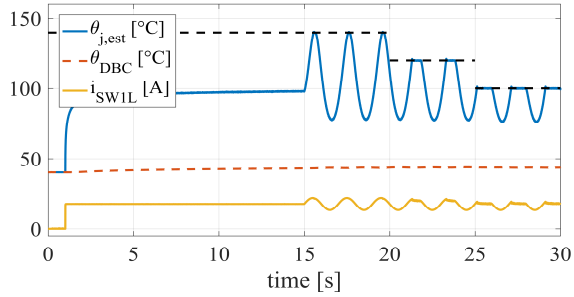


Fig. 21. Online junction temperature estimation, average duty-cycle is 0% (SW1L always close). a) AC current frequency 0.5Hz

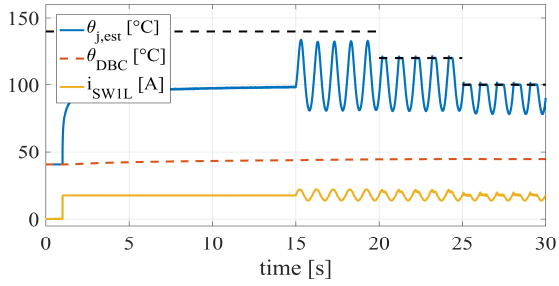


Fig. 22. Online junction temperature estimation, average duty-cycle LEG1 0% (SW1L always close). AC current frequency 1Hz

In the tests described in Fig. 21 to Fig. 24 the junction temperature limit is initially set to 140°C and then lowered to 120°C and finally to 100°C. Maximum allowed temperature is indicated with a black horizontal dashed line. The load current (yellow line) is equal to 18A in the first 15 seconds of the test. After 15 s, a sinusoidal current component is superimposed to the direct current, either at 0.5 Hz (Fig. 21 and Fig. 23) or at 1.0 Hz (Fig. 22 and Fig. 24). In Fig. 21 and Fig. 22 the duty-cycle of LEG1 is imposed to 0%, to say that SW1L is in continuous conduction, whereas in Fig. 23 and Fig. 24 the same test is repeated at 50% duty-cycle (SW1L in conduction half the time). LEG1 is the leg of the H-bridge that works open-loop. Load current is controlled by LEG2 [8].

Concerning the first two tests (Fig. 21 and Fig. 22), the estimated temperature has a peak value of 140°C in the 0.5 Hz case and circa 130°C when 1 Hz is used. The AC frequency expectedly lowers the amplitude of the temperature swing. In both Fig. 21 and Fig. 22, the current is real-time clamped during the periods where the temperature threshold is 120°C and 100°C. Accordingly, the temperature instantaneously respects the corresponding threshold value.

In Fig. 23 and Fig. 24 the two tests are repeated with the same load current and duty-cycle of the switch equal to 50%. In this case the switch SW1L shares conduction losses with the upper switch of LEG1 and it is less stressed thermal wise. The estimated temperature never touches the upper threshold, neither for the 110°C case.

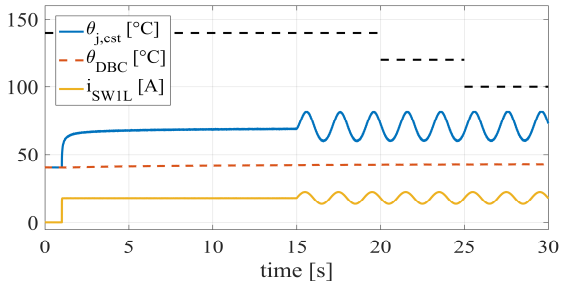


Fig. 23. Online junction temperature estimation, average duty-cycle LEG1 50% (SW1L close for 50% of the period). AC current frequency 0.5Hz

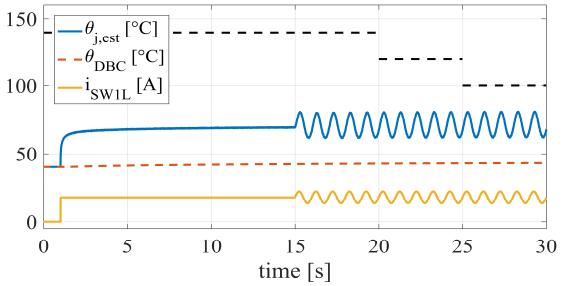


Fig. 24. Online junction temperature estimation, average duty-cycle LEG1 50% (SW1L close for 50% of the period). AC current frequency 1Hz

E. Validation against a Thermal Camera

The proposed methodology has been validated using a thermal camera. The layout of the test rig has been modified to permit visual access to the die. The module gel filling has been removed. In Fig. 25 the estimated temperature is compared to the temperature measured using a thermal camera

(Cedip Titanium 560MB IR, Courtesy of the University of Nottingham), with a sampling frequency of 20 Hz.

As the temperature gradient across the die is not negligible, two thermal camera outputs are reported: maximum and average temperature. The results show that the maximum temperature of the die is, expectedly, higher than the estimated temperature. Time wise, the blue curve (hot spot by the thermal camera) has an unexpectedly slow tail when passing from the high level to the low level at the step down of the load current. This is related to the automatic interpretation of the thermal image from the camera.

Dealing with the average temperature from the thermal camera, this matches the estimate well. In conclusion, the proposed methodology can estimate the average temperature of the die very accurately, and come as close as possible to the peak temperature within the die. This result is hard to beat, unless a complete thermal image of the die is available within the power converter.

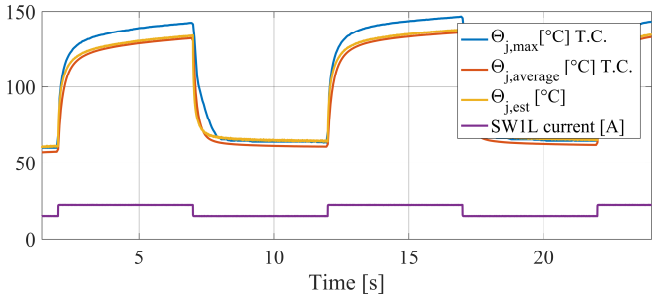


Fig. 25. Current square wave 15A-22.5A. Comparision between the estimated temperature and the measured temperature using the thermal camera.

V. DISCUSSION

A. Minimum Set of Measured Quantities

Not all the sampled quantities indicated in Fig. 1 are necessary for implementing the proposed online temperature estimation. The minimum set of dedicated measurements required by the proposed technique consists of:

- Drain-source voltage in on-state: this is the most critical measurement, as discussed in section II.C.
- Switch current in on-state, measured here via a shunt resistor in series with the switch. Current transducers of other type are also viable. Current controlled converters may use the same transducer used for current feedback.
- Case temperature: one thermistor embedded in the module, measuring the DBC temperature.

The monitoring of V_{GS} during the ON state was made available in the demonstrator for checking that the gate driver commands were appropriately at constant voltage. This would be unnecessary in a commercial converter.

B. Applicability to Different Converter Structures

One key assumption behind the proposed methodology is that the monitored switch is representative of the entire module's behavior. This is surely true for H-bridge structures operated in DC/AC configuration, as well as for 3-phase or n-phase 2-level voltage source inverters. All the mentioned DC/AC converter structures have in common the fact that all power devices, high side and low side, any leg, see the same duty-cycle and current over one period of the AC side. This guarantees that their peak temperature will be the same and that monitoring one switch will protect the entire converter.

For other structures, where the switches are loaded unevenly, the monitoring should be repeated for many significant switches. For example, if the H-bridge is used as a 4-quadrant DC/DC converter, monitoring the two switches of one leg is representative of the whole converter, because the two legs behave symmetrically. Other structures require to be evaluated case by case.

C. Aging of the Component and Prognostics

The R_{ON} tends to increase with the aging of the component. According to [11] the on-state resistance can increase by 10%-17% before the component fails. This would lead the proposed technique to overestimate the device temperature, and eventually to over-limit the device current according to the detected extra-resistance. Therefore, without recalibration of the look-up table, the method tends to accelerate the detection of the component aging, through the temperature misestimate. In this sense, the temperature monitoring is also a tool for on-line prognostics, like what done off-line in [12] and [13]. If the maximum allowable current is actively limited using the estimated temperature as feedback, the current limitation tends to trigger more frequently with the age of the component, leading the converter to underperform and warn the user. In this case, a new self-commissioning session can put in evidence the increased R_{ON} and the aging effect. Future investigation will be needed to evaluate the increment of the R_{ON} before the failure of the component especially in SiC devices.

D. Active thermal control

Thermal cycling magnitude strongly influences semiconductors' lifetime [14] and [15]. Experimental data showing the closed loop limitation of the junction temperature have been presented. However thanks to the high level of dynamic of the proposed method, it is possible to implement more sophisticated techniques like the one presented in [16] - [18], that actively reduce the temperature swing of the component and permits to extend the lifetime of the semiconductor.

E. Limitations and future improvements

Due to limitations of the current prototypal hardware, the temperature of the switch SW1L can be monitored only for positive values of the drain-source current, because the V_{ON} conditioning circuit does not cover the negative range. This choice was initially made to maintain a high level of accuracy of this measurement. After a certain number of tests, it is clear now that the 12 bit A/D converter used for sampling the V_{ON} is accurate enough to measure a wider range of voltages, and the input range of the circuit will be extended to cover negative currents soon.

Another singular condition is when i_{DS} is very low. In this case V_{ON} is in the low range of the measurement span and the measurement accuracy diminishes. However, this situation is

normally associated to low conduction loss, i.e. it is non-critical in terms of junction temperature

When the conduction time of the switch SW1L decreases to the order of few microseconds, the V_{ON} measurement can become problematic. If the duty cycle is close to 100%, the switch SW1L is in conduction for a limited amount of time. The same is true when the switching frequency is high, e.g. >100 kHz, which might be reasonable with SiC devices. The proposed current measurement system was tested with success up to 80 kHz, with duty cycle = 50%, corresponding to a minimum settling time of 3 µs circa. Also in this case work is in progress to push the switching frequency limit up to 200 kHz, i.e. the settling time below 1 µs.

In a real-world converter, the measurement system might be integrated in the drivers, considering that most of the drivers already integrate desaturation protections based on V_{ON} inspection.

In a future version, the MOSFETs itself will be used for heating the heatsink with the goal of running the commissioning test at a reduced temperature and to extrapolate the rest of the characteristic.

Finally, the proposed solution provides the average temperature of the die, though the temperature gradient across the die is not always negligible. Nevertheless, in the authors' opinion this apparent limitation does not harm the applicability of the proposed method, which is considered a strong step ahead towards on-line integrated temperature estimation.

VI. CONCLUSIONS

The paper demonstrates that inserting the V_{ON} measurement on board of a power converter permits a good and high-dynamic estimation of the junction temperature of one of the power devices. The method is promising for application to standard and special converters, with little impact in terms of additional components and cost. The measurement system can be integrated into the gate driver circuit. Through the knowledge of the junction temperature it is possible exploit completely the SOA of the component while maintaining high reliability levels. It is expected that this innovation might reduce the cost of the final application.

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