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An Analytical Approach for the Design of Class-E Resonant DC-DC Converters

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***Abstract*—We present a new approach to design resonant dc-dc converters, that allows to achieve both a more accurate implementation and a simpler architecture, by reducing the number of required passive components. The approach is applied to a class-E topology, and it is based on the analytic solution of the system of differential equations regulating the converter evolution. Our technique is also capable of taking into account the most important circuit non-idealities. This represents an important breakthrough with respect to the state-of-the-art, where class-E circuit analysis is based on strong simplifying assumptions, and the final circuit design is achieved by means of numerical simulations after many time-consuming parametric sweeps. The developed methodology is dimensionless, and the achieved design curves can be de-normalized to easily get the desired circuit design. Measurements on two different prototypes confirm an extremely high adherence to the developed mathematical approach.**

***Index Terms*—Resonant dc-dc converters, Class-E converters.**

I. Introduction

ONE of the most important recent trends in the design of dc-dc switching power converters is the increase in their operating frequency, which has nowadays reached the VHF range (30-300 MHz) [1]–[4]. There are, in fact, several advantages connected to a very high switching frequency. Two of them are noteworthy: first, better transient performance and bandwidth can be achieved; second, constraints on the values of passive reactive elements are relaxed and, in general, smaller and less expensive components are required. This allows to increase the converter power density and supports the ultimate goal of adopting air-core magnetic components small enough to be embedded into a fully integrated solution.

Unfortunately, the design of a VHF switching power converter poses several challenges. In particular, the main issue is the converter efficiency, since switching losses are increasing with the switching frequency [1]. To solve the impasse, resonant class-E dc-dc converters were introduced [5], [6], exploiting the so-called *soft switching* technique.

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Roughly speaking, they embed a resonant circuit that shapes the voltage across the semiconductor switching device in such a way that it naturally reaches zero immediately before the instant in which the switch is turned on [7], allowing current to start flowing. Additionally, it is possible to impose that the voltage goes to zero smoothly, *i.e.*, with zero time derivative.

These two conditions are known respectively as zero voltage switching (ZVS) and zero voltage derivative switching (ZVDS), and satisfying them produces a reduction of the voltage-current product of the switching device at turn on instants, lowering (ideally, down to zero) the energy-loss-per-cycle, with beneficial effects also in terms of electromagnetic interference (EMI) mitigation and stress reduction on switching devices.

While the classical procedure for resonant converter design relies on heavy simplifying assumptions, here we propose a novel approach where the exact dynamics of the system is taken into consideration. By solving the system of ordinary differential equations (ODE) regulating the converter behavior, and by considering the converter operating at steady state condition as in [8]–[10], we develop a mathematical framework which makes possible a fast and accurate circuit design.

In addition to the obvious advantage of achieving a less approximate design without resorting to circuit-level simulations, the ability of considering non-simplified dynamics allows to eliminate circuit elements, such as bulky RF choke inductors, high-Q filters or tuned matching network conventionally introduced to justify model simplifications. This has a tremendous impact on circuit size and complexity and allows us to apply our approach to an extremely lightweight class-E architecture that can be configured either as an isolated or non-isolated topology.

Some preliminary results, limited to the case of ideal circuit components, were reported in [11], where we presented an initial study of the ODE-based approach. A first dc-dc converter prototype has been designed and described in [12]. Here, with respect to [11], [12], we present three additional steps:

- we include the most important circuit non-idealities and parasitic elements in the model. This allows us to obtain an almost perfect match between the expected circuit behavior and the actual measurements, and to make this procedure extremely useful for circuit designers;
- we introduce a suitable normalization that makes the circuit design independent of the values of voltages, currents and switching frequency. We also provide general design curves that allow any designer to immediately solve the

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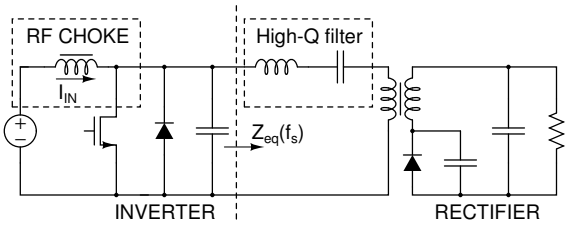

Fig. 1. Classical isolated class-E dc-dc converter design taken from [13], where we highlighted the RF choke inductor and the LC high-Q filter connecting the inverter and the rectifier stages.

converter design problem by simply de-normalizing the general solution;

- we validate the improved methodology by implementing two new circuit prototypes. The almost perfect match between theoretical and measured waveforms in both circuits confirm the validity of the design tool and opens new optimization possibilities in class E dc-dc converter design.

The paper is organized as follows. Section II reviews the state-of-the-art design methodology of class-E dc-dc converters and introduces the resonant topology considered in this paper. In Section III we develop the framework for the exact circuit analysis. Then, in Section IV our design approach is explained, and used for achieving general design curves in Section V. The implementation of the two prototypes is presented in Section VI and, finally, we draw the conclusion.

II. Class-E dc-dc converters

Class-E dc-dc converters were first introduced in the early 80s to take advantage of the radio frequency (RF) design techniques in high-frequency dc-dc power conversion, aiming to move from the common single power source scenario to low power, small size, distributed power modules [5], [6], [13]. The key point was to increase efficiency at high speed of operation by moving from rectangular pulse waveforms to sinusoidal-like ones.

A. Conventional class-E converter design approach

All class-E dc-dc converter topologies are based on two fundamental building blocks, a class-E inverter [7], [14] and a rectifying stage [15]–[18], usually connected together by means of an LC filter that acts as impedance matching network. A very common topology used for isolated converters is represented in Fig. 1 (taken from [13]).

The inverter stage is basically a class-E amplifier working at frequency f_s, and loaded with a non-resistive network designed to properly shape the voltage across the transistor and achieve optimal operation, *i.e.*, ZVS and (possibly) ZVDS conditions. More specifically, the inverter design is achieved by assuming the equivalent input impedance $Z_{eq}(f_s)$ of the rectifier as load. The resonant rectifier (*i.e.*, a rectifier properly connected with reactive elements) makes the final ac/dc conversion. Its design is achieved by *approximating the input voltage as a sinusoidal tone* at the converter working frequency f_s. To ensure both the aforementioned assumptions,

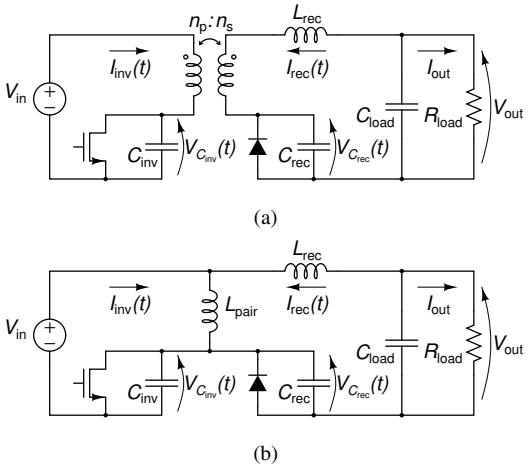

Fig. 2. Schematic of the considered converter. (a): isolated topology; (b): non-isolated topology.

allowing the actual circuit behavior to match the approximated one, the inverter and rectifier are connected by means of a high-Q LC filter, ensuring both an impedance matching (from the inverter point of view) and harmonics filtering (from the rectifier point of view). A large RF choke inductor is also commonly employed to ensure that the simplifying assumption of a constant current power source is actually satisfied.

In this way, the whole converter design can be readily obtained taking advantage of well-known RF techniques [13].

In recent years, research efforts have been focused on the investigation of different inverter and rectifier topologies [19]–[24] to increase efficiency or reduce device stress. As an example, the ϕ_2 converter [19] was introduced to decrease the peak level of the MOS switch drain-source voltage. A few contributions also tried a mathematical formalization of the converter analysis aiming to reduce the circuit complexity by removing unnecessary reactive elements such as the RF choke inductor [25]. However, the achieved accuracy is always limited by the aforementioned sinusoidal approximation, that makes necessary the presence of the LC filter, and causes appreciable differences between the theoretical circuit evolution and the actual one. Consequently, a simulation-based tuning of circuit parameters is needed to identify the optimal operating point.

B. Proposed circuit description

The schematic of the circuit we consider is shown in its isolated and non-isolated configuration in Fig. 2(a) and 2(b), respectively. In both cases, we indicate the input voltage with $V_{\rm in}$, the output voltage with $V_{\rm out}$, and we assume a resistive load $R_{\rm load}$, with load current given by $I_{\rm out} = V_{\rm out}/R_{\rm load}$. Like any class-E dc-dc converter, the circuit can be separated into an inverter and a rectifying stage, connected together either by a coupling transformer or by a pairing inductance $L_{\rm pair}$.

Note that the two schematics of Fig. 2 represent only the "core" of a class-E dc-dc converter. Actually, two sub-circuits required to obtain the complete scheme used in practice are not considered.

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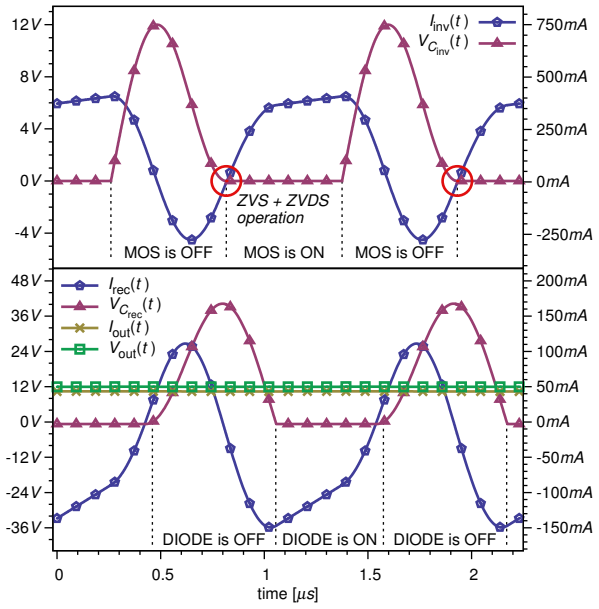

Fig. 3. Example of current and voltage signals waveforms for the inverter, featuring ZVS and ZVDS (top plot), and for the rectifier (bottom plot) in an isolated converter topology example.

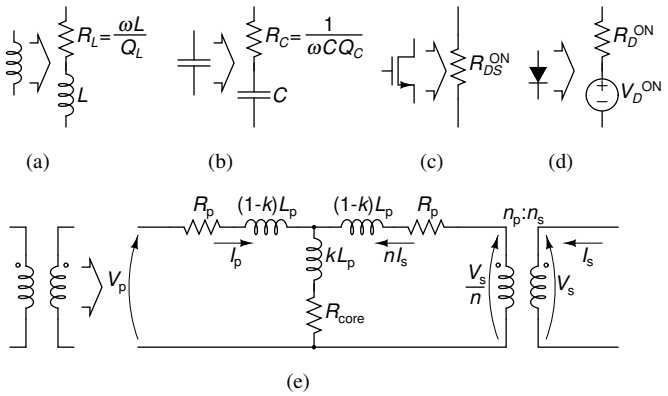

Fig. 4. Equivalent circuits used to model real devices. (a): inductors; (b): capacitors; (c): MOS switch (ON state); (d): diode (ON state); (e): transformer. MOS switch and diode in the OFF state are modeled as open circuits.

The first one is a gate driver circuit for the MOS switch. With respect to this, it is worth noticing that in practical cases the most common approach is to embed a self-resonant gate driver circuit with the aim of improving energy efficiency [26]. In this paper, to maintain focus on the main contribution, we decided to simply assume that the oscillation frequency is regulated by an external clock generator, which turns ON and OFF the MOS switch at frequency f_s with duty-cycle D.

The second sub-circuit is the load regulator. In class-E dc-dc converters, ZVS and ZVDS are achieved only for a specific optimal operating point, i.e., for a given $R_{\rm load}$ or equivalently a given output power. To preserve ZVS and ZVDS with a variable load, an on-off control [25], [27] is typically employed. Without entering into details, this approach allows the converter only to be in an off state (where the output voltage is maintained constant by $C_{\rm load}$) or to work in the optimal operating point. Under this assumption, the converter design is achieved considering the maximum output power, i.e., the minimum $R_{\rm load}$, and the ratio between the actual output power and the maximum one is set by the ON/OFF ratio. Again, to maintain our paper focused on its main contribution and simplifying the presentation as much as possible, in this paper we do not consider the on-off control, and we design the circuit according to the maximum output deliverable power.

An example of the typical circuit waveforms of the dc-dc converter of Fig. 2(a), designed accordingly to the proposed methodology, can be observed in the SPICE simulation waveforms of Fig 3. The picture includes the voltage $V_{C_{\rm inv}}(t)$ and the current $I_{\rm inv}(t)$ at the inverter side, and the voltage $V_{C_{\rm rec}}(t)$ and the current $I_{\rm rec}(t)$ at the rectifier side. The (almost constant due to $C_{\rm load}$) output voltage $V_{\rm out}$ and output current $I_{\rm out}$ are also shown; note that, accordingly to the schematic of Fig. 2, and considering a zero average current flowing through the output capacitor in steady-state condition, $I_{\rm out}$ can be expressed as a function of the mean value of $I_{\rm rec}(t)$ as:

$$I_{\rm out} = -\left\langle I_{\rm rec}(t) \right\rangle \tag{1}$$

It is worth stressing that the desired ZVS and ZVDS operation conditions have been perfectly ensured, as $V_{C_{\rm inv}}(t)$ smoothly crosses the zero level at the MOS turn-ON instant.

III. ODE-based Circuit Analysis

A. Non-idealities modeling

To develop an accurate mathematical model for the dc-dc converters of Fig. 2, for every device (with the exception of $C_{\rm load}$) we consider a very simple equivalent circuit that includes non-idealities and parasitic effects as summarized in Fig. 4.

More specifically, for inductors and capacitors we use the classical equivalent circuit for lossy reactive components operating at angular frequency $\omega_s = 2\pi f_s$ of Fig. 4(a) and 4(b) respectively. The value of the series resistances is linked to the quality factors Q_L and Q_C by

$$Q_L = \frac{\omega_s L}{R_L}, \quad Q_C = \frac{1}{\omega_s C R_C} \tag{2}$$

Conversely, $C_{\rm load}$ is not part of a resonating circuit, but its role is just to limit oscillations in the output voltage $V_{\rm out}$ as much as possible. Therefore, we will adopt in the following a common assumption for all dc-dc switching converters and replace the $R_{\rm load}$ and $C_{\rm load}$ network with an ideal dc voltage source $V_{\rm out}$.

Active devices (*i.e.*, the MOS switch and the rectifying diode) are modeled as switches that can be either in a completely ON or OFF state. When ON, the MOS switch is replaced by a reasonably small $R_{DS}^{\rm ON}$ resistance as shown in Fig. 4(c), and by an open circuit while OFF. When the diode is ON, we observe a forward voltage drop that has a weak dependence on the diode current. To model this effect, we replace the diode with an ideal voltage source $V_D^{\rm ON}$ and a (small) series resistance $R_D^{\rm ON}$ as in Fig. 4(d). When in the OFF state, we assume that the diode is equivalent to an open circuit. Note that parasitic capacitances on both the MOS switch and the diode, that may be relevant in particular in their OFF state,

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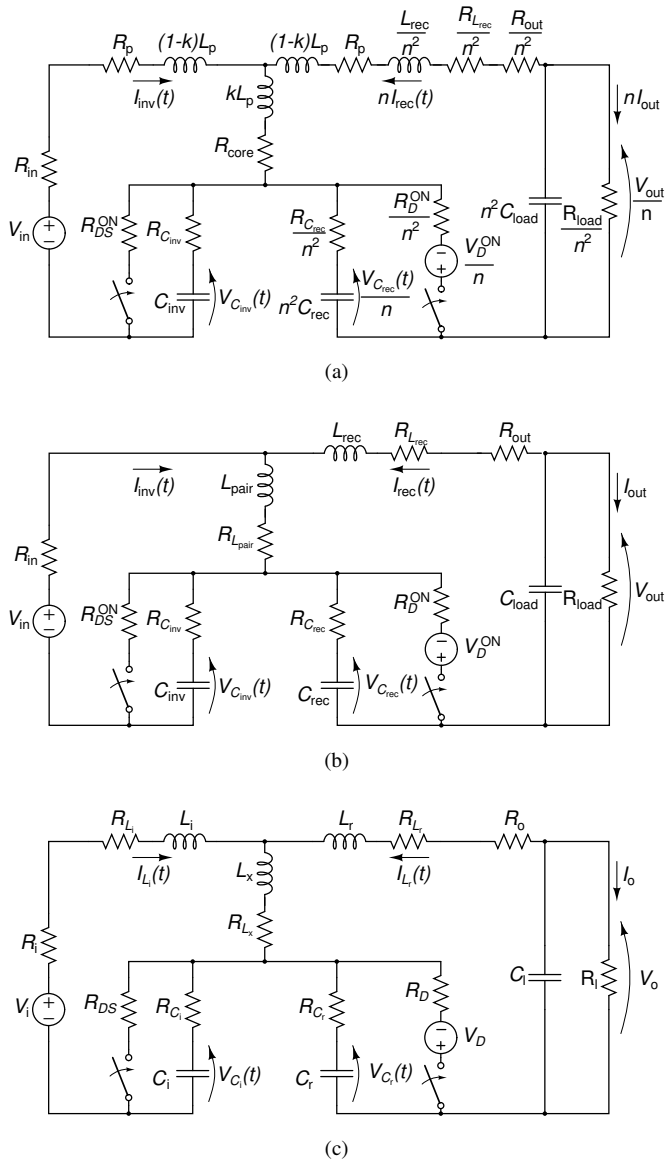

Fig. 5. Equivalent schematic circuits of the converter topologies of Fig. 2, including parasitic device modeling. (a): isolated topology, referring all elements at the secondary side of the transformer to the primary side; (b): non-isolated topology; (c): schematic and notation used to analyze both topologies.

have not been explicitly modeled. In fact, for typical values of the external capacitors $C_{\rm inv}$ and $C_{\rm rec}$ these parasitic effects can be considered as masked or conveniently absorbed by them; this is a very common assumption in almost all class-E design approaches, and we adopted it here as well.

Finally, the transformer is modeled with the standard equivalent circuit of Fig. 4(e) [28], where all the elements are referred to the primary side and an ideal transformer with turns ratio $n = n_{\rm s}/n_{\rm p}$ couples the secondary side. The total inductance $L_{\rm p}$ seen at the primary side is split into a magnetizing inductance $kL_{\rm p}$ and two leakage inductances $(1-k)L_{\rm p}$ by means of the coupling coefficient k. The equivalent circuit also includes a resistance $R_{\rm core}$ mainly modeling energy loss in the magnetic core, and two resistances $R_{\rm p}$ modeling wire turns losses.

When replacing all devices of Fig. 2 with the equivalent of Fig. 4, we get the two schematics of Fig. 5(a) and Fig. 5(b). In the figure we have also included two additional resistances $R_{\rm in}$ and $R_{\rm out}$ to model other possible circuit losses (*e.g.*, current sensing resistors, a non-ideal voltage source, *etc.*) and, in the isolated topology, we have replaced all elements at the secondary side of the transformer (*i.e.*, $L_{\rm rec}$, $C_{\rm rec}$, $C_{\rm load}$, $R_{\rm load}$, $R_{\rm out}$ and the rectifying diode) with the corresponding equivalent ones at the primary side.

The differences between the circuits of Fig. 5(a) and Fig. 5(b) are very limited. Since the aim of this paper is to analyze both converter topologies, the most convenient approach is to introduce the schematic of Fig. 5(c). The notation of the new circuit is simplified with respect both to that of Fig. 5(b) and of Fig. 5(a) to allow an easier mathematical analysis, and a few elements have been removed by considering series connections. More formally, the new notation is achieved by setting

$$V_{\rm o}=\begin{cases}V_{\rm out}/n\\ V_{\rm out}\end{cases},\ C_{\rm l}=\begin{cases}n^2C_{\rm load}\\ C_{\rm load}\end{cases},\ R_{\rm l}=\begin{cases}R_{\rm load}/n^2\\ R_{\rm load}\end{cases},$$

$$I_{\rm o}=\begin{cases}nI_{\rm out}\\ I_{\rm out}\end{cases},\ I_{L_{\rm r}}(t)=\begin{cases}nI_{\rm rec}(t)\\ I_{\rm rec}(t)\end{cases},\ R_{\rm o}=\begin{cases}R_{\rm out}/n^2\\ R_{\rm out}\end{cases},$$

$$L_{\rm r}=\begin{cases}(1-k)L_p+L_{\rm rec}/n^2\\ L_{\rm rec}\end{cases},\ R_{L_{\rm r}}=\begin{cases}R_p+R_{L_{\rm rec}}/n^2\\ R_{L_{\rm rec}}\end{cases},$$

$$V_{C_{\rm r}}(t)=\begin{cases}V_{C_{\rm rec}}(t)/n\\ V_{C_{\rm rec}}(t)\end{cases},\ C_{\rm r}=\begin{cases}n^2C_{\rm rec}\\ C_{\rm rec}\end{cases},\ R_{C_{\rm r}}=\begin{cases}R_{C_{\rm rec}}/n^2\\ R_{C_{\rm rec}}\end{cases},$$

$$V_{\rm D}=\begin{cases}V_D^{\rm ON}/n\\ V_D^{\rm ON}\end{cases},\ R_D=\begin{cases}R_D^{\rm ON}/n^2\\ R_D^{\rm ON}\end{cases},\ L_{\rm x}=\begin{cases}kL_{\rm p}\\ L_{\rm pair}\end{cases},$$

$$R_{L_{\rm x}}=\begin{cases}R_{\rm core}\\ R_{L_{\rm pair}}\end{cases},\ L_{\rm i}=\begin{cases}(1-k)L_{\rm p}\\ 0\end{cases},\ R_{L_{\rm i}}=\begin{cases}R_{\rm p}\\ 0\end{cases}$$

where the first line refers to Fig. 5(a), and the second one to Fig. 5(b), and by defining for both cases $V_{\rm i}=V_{\rm in}$, $R_{\rm i}=R_{\rm in}$, $R_{DS}=R_{DS}^{\rm ON}$, $C_{\rm i}=C_{\rm inv}$, $R_{C_{\rm i}}=R_{C_{\rm inv}}$, $I_{L_{\rm i}}(t)=I_{\rm inv}(t)$ and $V_{C_{\rm i}}(t)=V_{C_{\rm inv}}(t)$.

B. Converter analysis

By modeling the MOS switch and the rectifying diode as devices that can be only in an ON or an OFF state, the analysis of the circuit of Fig. 5(c) can be achieved by considering separately the four different configurations determined by the possible ON/OFF combinations of the state of the two devices. We denote them as *zones*, referred to with Z_j, $j=1,\ldots,4$. The schematic associated to each zone is depicted in Fig. 6.

The four circuits of Fig. 6 have been obtained as follows. The MOS switch is OFF in Z_1 and Z_2, where it is modeled as an open circuit. In Z_3 and Z_4 it is ON and replaced by R_{DS}, that it is assumed very small. Therefore, $V_{C_{\rm i}}(t)$ is vanishing, and the current $I_{L_{\rm i}}(t)$ is all flowing through the MOS, so that C_i has almost no effect and is not considered. Conversely, the rectifying diode is OFF in Z_2 and Z_3 and ON in Z_1 and Z_4 where, since R_D is small, we have $V_{C_{\rm r}}(t)\approx -V_D$ so that C_r can be assumed to have no influence on the circuit.

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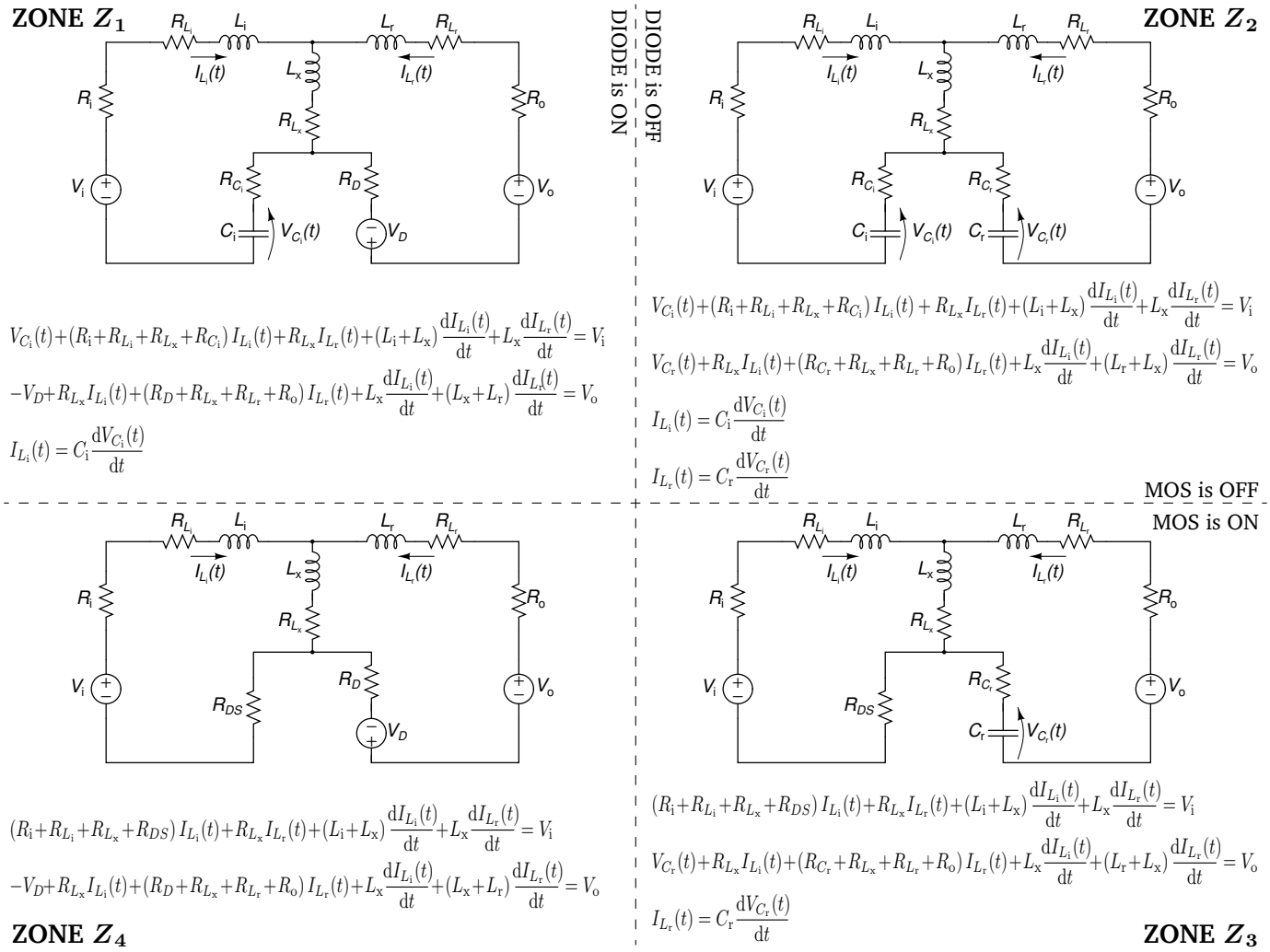

Fig. 6. Equivalent circuit models used for the converter analysis according to the four different zones. In Z_1 and Z_2 the MOS switch is OFF, and it is not taken into account; in Z_3 and Z_4 the MOS is ON and it is replaced by a R_{DS} resistance, while the C_r is not considered in the equivalent circuit. The rectifying diode is OFF in Z_2 and Z_3 and therefore it is removed from the equivalent circuit; in Z_1 and Z_4 the diode is ON, and it is modeled as a voltage source V_D and a resistance R_D, while C_i is not considered. In each zone the equivalent circuit is linear and its evolution is regulated by the differential equation system written below.

As previously explained, in all four cases the load network $R_l - C_l$ has been replaced by a constant voltage generator V_o.

The four achieved circuits are linear, and their evolution can be obtained by solving the four associated systems of linear ODEs, whose order ranges from 2 (in Z_4) to 4 (in Z_2), and which are reported below each schematic in Fig. 6. The evolution of the whole converter can then be obtained by ensuring the continuity of the capacitance voltages and of the inductor currents when switching from one zone to another one.

To express the results of our analysis in a more compact and useful form, we need to introduce a suitable normalization for all equations of Fig. 6. Let us consider current and voltage signals normalized respectively by I_o and V_o, and indicate them as function of the normalized time $\theta = \omega_s t$, that is:

$$i_{L_i}(\theta) = \frac{I_{L_i}(\theta/\omega_s)}{I_o}, \quad i_{L_r}(\theta) = \frac{I_{L_r}(\theta/\omega_s)}{I_o},$$
$$v_{C_i}(\theta) = \frac{V_{C_i}(\theta/\omega_s)}{V_o}, \quad v_{C_r}(\theta) = \frac{V_{C_r}(\theta/\omega_s)}{V_o} \tag{3}$$

Observing that $R_l = V_o/I_o$, let us also introduce the five dimensionless parameters q_i, q_r, q_x, k_i and k_r defined by:

$$q_i = \frac{1}{\omega_s C_i R_l}, \; q_r = \frac{1}{\omega_s C_r R_l}, \; q_x = \frac{\omega_s L_x}{R_l}$$
$$k_i = \frac{L_x}{L_i + L_x}, \; k_r = \frac{L_x}{L_r + L_x} \tag{4}$$

We express the equivalent series resistances for the five reactive elements L_i, L_x, L_r, C_i and C_r exploiting the definition of the quality factors Q_{L_i}, Q_{L_x}, Q_{L_r}, Q_{C_i} and Q_{C_r} as in (2). Then, let us also define

$$g_{DS} = \frac{R_l}{R_{DS}}, \; g_D = \frac{R_l}{R_D}, \; g_i = \frac{R_l}{R_i}, \; g_o = \frac{R_l}{R_o} \tag{5}$$

so that g_{DS}, g_D, g_i and g_o play the role of quality factors for, respectively, the MOS switch, the rectifying diode, and the input and output node.

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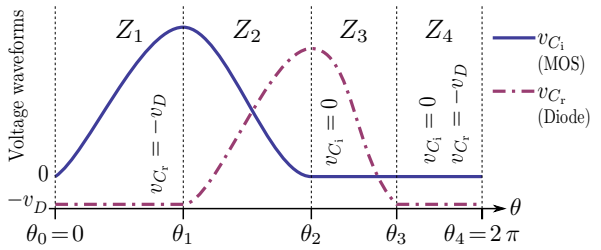

Fig. 7. Succession of zones considered in this paper.

Finally, μ and v_D are the normalization of the input voltage and the diode forward voltage drop:

$$\mu = \frac{V_\mathrm{i}}{V_\mathrm{o}},\ v_D = \frac{V_D}{V_\mathrm{o}} \tag{6}$$

The advantage of this approach is that the normalized system fully describes the circuit topology, and it is independent of the switching frequency and of the output voltage and power. Furthermore, let us introduce the two parameters m^{ON} and d^{ON}, with $m^{\mathrm{ON}} = 1$ ($m^{\mathrm{ON}} = 0$) when the MOS switch is ON (is OFF), and $d^{\mathrm{ON}} = 1$ ($d^{\mathrm{ON}} = 0$) when the rectifying diode is ON (is OFF). With these, the systems describing the evolution of the four zones can be written as in (7).

With this approach, the evolution of the circuit in a clock period can be easily described once the succession of zones is known. Despite a few different sequences can be observed, particularly in rather unpractical situations such as when the system is not in a steady-state condition, or when the considered quality factors of the components are extremely low, in all realistic cases the succession of zone is the one depicted in Fig. 7. For this reason, and since to consider a mathematical framework able to deal will all possible zone sequences would considerably complicate our design procedure without any real practical benefit, in the following we limit ourselves to consider this case only.

Mathematically, let us set the normalized time to $\theta = \theta_0 = 0$ when the MOS switch is turned OFF while the diode is still ON. At this time instant, we can approximate $v_{C_\mathrm{i}}(0) = 0$ and $v_{C_r}(0) = -v_D$, and we define $i_{L_\mathrm{i}}(0) = i_{L_\mathrm{i}}^0$ and $i_{L_\mathrm{r}}(0) = i_{L_\mathrm{r}}^0$. Then, Z_1 starts, followed by Z_2, Z_3 and Z_4 as described in the following.

Zone Z_1: Let us refer to normalized currents and voltages in this zone with $i_{L_\mathrm{i}}^{(Z_1)}$, $i_{L_\mathrm{r}}^{(Z_1)}$, $v_{C_\mathrm{i}}^{(Z_1)}$ and $v_{C_\mathrm{r}}^{(Z_1)}$. In this zone we can assume that $v_{C_\mathrm{r}}^{(Z_1)}(\theta) = -v_D$, while the evolution of $i_{L_\mathrm{i}}^{(Z_1)}(\theta)$, $i_{L_\mathrm{r}}^{(Z_1)}(\theta)$ and $v_{C_\mathrm{i}}^{(Z_1)}(\theta)$ is regulated by (7) with $m^{\mathrm{ON}} = 0$ and $d^{\mathrm{ON}} = 1$. The computation of the evolution is reported in the Appendix; the result can be found in (A.2), and the three coefficients c_1, c_2 and c_3 must be computed to satisfy the initial conditions

$$i_{L_\mathrm{i}}^{(Z_1)}(0) = i_{L_\mathrm{i}}^0,\quad i_{L_\mathrm{r}}^{(Z_1)}(0) = i_{L_\mathrm{r}}^0,\quad v_{C_\mathrm{i}}^{(Z_1)}(0) = 0 \tag{8}$$

The zone ends at $\theta = \theta_1$, that is defined as the normalized time instant in which the diode turns OFF. The value of θ_1 is computed by solving $i_{L_\mathrm{r}}^{(Z_1)}(\theta_1) = 0$.

Zone Z_2: Here $m^{\mathrm{ON}} = d^{\mathrm{ON}} = 0$ and (7) is turned into a 4^{th} order system in the variables $i_{L_\mathrm{i}}^{(Z_2)}(\theta)$, $i_{L_\mathrm{r}}^{(Z_2)}(\theta)$, $v_{C_\mathrm{i}}^{(Z_2)}(\theta)$ and $v_{C_\mathrm{r}}^{(Z_2)}(\theta)$, whose solution can be found in (A.4). The four coefficients c_1, c_2, c_3 and c_4 are computed by imposing the continuity of the current signals at θ_1

$$i_{L_\mathrm{i}}^{(Z_2)}(\theta_1) = i_{L_\mathrm{i}}^{(Z_1)}(\theta_1),\quad i_{L_\mathrm{r}}^{(Z_2)}(\theta_1) = i_{L_\mathrm{r}}^{(Z_1)}(\theta_1)$$

and by assuming

$$v_{C_\mathrm{i}}^{(Z_2)}(\theta_1) = v_{C_\mathrm{i}}^{(Z_1)}(\theta_1),\quad v_{C_\mathrm{r}}^{(Z_2)}(\theta_1) = -v_D$$

Z_2 ends at $\theta_2 = 2\pi(1{-}D)$, when the MOS switch is externally turned ON while the diode is still OFF. Note that, accordingly to the assumptions of Sec. II-B, θ_2 is actually a degree of freedom of the system, since D is not constrained but can be freely set.

Zone Z_3: Here $m^{\mathrm{ON}} = 1$ and $d^{\mathrm{ON}} = 0$, and we can approximate $v_{C_\mathrm{i}}^{(Z_3)}(\theta) = 0$ independently of $v_{C_\mathrm{i}}^{(Z_2)}$, and include $v_{C_\mathrm{r}}^{(Z_3)}$ in the pool of system variables along with $i_{L_\mathrm{i}}^{(Z_3)}$ and $i_{L_\mathrm{r}}^{(Z_3)}$. The evolution given by (A.6), where the coefficients c_1, c_2 and c_3 are given by imposing

$$\begin{gathered} i_{L_\mathrm{i}}^{(Z_3)}(\theta_2) = i_{L_\mathrm{i}}^{(Z_2)}(\theta_2),\quad i_{L_\mathrm{r}}^{(Z_3)}(\theta_2) = i_{L_\mathrm{r}}^{(Z_2)}(\theta_2), \\ v_{C_\mathrm{r}}^{(Z_3)}(\theta_2) = v_{C_\mathrm{r}}^{(Z_2)}(\theta_2) \end{gathered} \tag{9}$$

The zone Z_3 ends at θ_3, when the voltage $v_{C_r}(\theta)$ turns negative and is able to switch the diode ON. Mathematically, θ_3 is the normalized time that solves $v_{C_r}^{(Z_3)}(\theta_3) = -v_D$.

Zone Z_4: Here both MOS switch and diode are ON, so $m^{\mathrm{ON}} = d^{\mathrm{ON}} = 1$. We approximate $v_{C_\mathrm{i}}^{(Z_4)}(\theta) = 0$ and $v_{C_\mathrm{r}}^{(Z_4)}(\theta) = -v_D$, while the evolution of $i_{L_\mathrm{i}}^{(Z_4)}(\theta)$ and $i_{L_\mathrm{r}}^{(Z_4)}(\theta)$ is given by (A.8), where the coefficients c_1, c_2 are computed in accordance to the initial conditions

$$i_{L_\mathrm{i}}^{(Z_4)}(\theta_3) = i_{L_\mathrm{i}}^{(Z_3)}(\theta_3),\quad i_{L_\mathrm{r}}^{(Z_4)}(\theta_3) = i_{L_\mathrm{r}}^{(Z_3)}(\theta_3)$$

This zone ends at $\theta = \theta_4 = 2\pi$, when the MOS switch is turned OFF, and the system evolution starts again from Z_1.

$$\begin{gathered} \left(1-m^{\mathrm{ON}}\right) v_{C_\mathrm{i}}(\theta) + \left(\frac{1}{g_\mathrm{i}} + \frac{1-k_i}{k_i}\frac{q_x}{Q_{L_\mathrm{i}}} + \frac{q_x}{Q_{L_\mathrm{x}}} + \left(1-m^{\mathrm{ON}}\right)\frac{q_i}{Q_{C_\mathrm{i}}} + \frac{m^{\mathrm{ON}}}{g_{DS}}\right) i_{L_\mathrm{i}}(\theta) + \frac{q_x}{Q_{L_\mathrm{x}}} i_{L_\mathrm{r}}(\theta) + \frac{q_x}{k_i}\frac{\mathrm{d}i_{L_\mathrm{i}}(\theta)}{\mathrm{d}\theta} + q_x\frac{\mathrm{d}i_{L_\mathrm{r}}(\theta)}{\mathrm{d}\theta} = \mu \\ \left(1-d^{\mathrm{ON}}\right) v_{C_\mathrm{r}}(\theta) - d^{\mathrm{ON}} v_D + \frac{q_x}{Q_{L_\mathrm{x}}} i_{L_\mathrm{i}}(\theta) + \left(\frac{1}{g_\mathrm{o}} + \frac{1-k_r}{k_r}\frac{q_x}{Q_{L_\mathrm{r}}} + \frac{q_x}{Q_{L_\mathrm{x}}} + \left(1-d^{\mathrm{ON}}\right)\frac{q_r}{Q_{C_\mathrm{r}}} + \frac{d^{\mathrm{ON}}}{g_D}\right) i_{L_\mathrm{r}}(\theta) + q_x\frac{\mathrm{d}i_{L_\mathrm{i}}(\theta)}{\mathrm{d}\theta} + \frac{q_x}{k_r}\frac{\mathrm{d}i_{L_\mathrm{r}}(\theta)}{\mathrm{d}\theta t} = 1 \end{gathered} \tag{7}$$

$$i_{L_\mathrm{i}}(\theta) = \frac{1}{q_i}\frac{\mathrm{d}v_{C_i}(\theta)}{\mathrm{d}\theta}\quad (Z_1 \text{ and } Z_2 \text{ only}),\qquad i_{L_\mathrm{r}}(\theta) = \frac{1}{q_r}\frac{\mathrm{d}v_{C_r}(\theta)}{\mathrm{d}\theta}\quad (Z_2 \text{ and } Z_3 \text{ only})$$

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In conclusion, the normalized analytic evolution of the converter in the considered clock period is then given by the piecewise solution

$$\begin{aligned} i_{L_\mathrm{i}}(\theta) &= i_{L_\mathrm{i}}^{(Z_k)}(\theta) \quad v_{L_\mathrm{i}}(\theta) = v_{L_\mathrm{i}}^{(Z_k)}(\theta) \\ i_{L_\mathrm{r}}(\theta) &= i_{L_\mathrm{r}}^{(Z_k)}(\theta) \quad v_{L_\mathrm{r}}(\theta) = v_{L_\mathrm{r}}^{(Z_k)}(\theta) \end{aligned} \tag{10}$$

with $\theta_{k-1} \le \theta \le \theta_k$, $k = 1, \ldots, 4$, $\theta_0 = 0$ and $\theta_4 = 2\pi$, and which depends on the dimensionless parameters

$$\begin{gathered} \mu,\ D,\ i_{L_\mathrm{i}}^0,\ i_{L_\mathrm{r}}^0,\ k_i,\ k_r,\ q_i,\ q_x,\ q_r, \\ v_D,\ Q_{L_\mathrm{i}},\ Q_{L_\mathrm{x}},\ Q_{L_\mathrm{r}},\ Q_{C_\mathrm{i}},\ Q_{C_\mathrm{r}},\ g_{DS},\ g_D,\ g_\mathrm{i},\ g_\mathrm{o} \end{gathered} \tag{11}$$

Note that some of the above parameters are fixed by technological constraints (such as inductors and capacitors quality factors, as well as k_i and v_D) or circuital ones (such as μ). Others are not constrained, and can be set to achieve the desired ZVS and ZVDS behavior. In particular, the parameters that can be easily tuned by a designer are q_i, q_r, q_x and k_r, representing the normalized value of C_i, C_r, L_x and L_r. Also the duty cycle D can be tuned for optimization purposes. Conversely, the values of $i_{L_\mathrm{i}}^0$ and $i_{L_\mathrm{r}}^0$, despite unconstrained, are regulated by the circuit evolution.

IV. Circuit Design Technique

From (10) one can get the converter design once behavioral constraints are expressed into a mathematical form.

- **Stationary condition:** it is achieved when:

$$i_{L_\mathrm{i}}(2\pi) = i_{L_\mathrm{i}}(0) = i_{L_\mathrm{i}}^0 \tag{12}$$

$$i_{L_\mathrm{r}}(2\pi) = i_{L_\mathrm{r}}(0) = i_{L_\mathrm{r}}^0 \tag{13}$$

$$\frac{1}{2\pi}\int_0^{2\pi} i_{L_\mathrm{r}}(\theta)\,\mathrm{d}\theta + 1 = 0 \tag{14}$$

  Equations (12) and (13) are used to ensure that the two current waveforms $i_{L_\mathrm{i}}(\theta)$ and $i_{L_\mathrm{r}}(\theta)$ are periodic waveforms[1]. Equation (14) derives from (1) under the assumption to compute the mean value of $I_\mathrm{rec}(t)$ as its average value in a period, and considering the normalization introduced in (3). With (14) we ensure that the average current on C_l is zero, so that the average output voltage is unchanged justifying the assumption to replace it with an ideal voltage source.
- **ZVS:** the zero voltage switching is achieved by imposing:

$$v_{C_\mathrm{i}}(\theta_2) = 0 \tag{15}$$

- **ZVDS:** the zero voltage derivative switching is achieved when $\mathrm{d}v_{C_\mathrm{i}}(\theta)/\,\mathrm{d}\theta = 0$ for $\theta = \theta_2$. Accordingly to (7), this is equivalent to ask that:

$$i_{L_\mathrm{i}}(\theta_2) = 0 \tag{16}$$

Equations (12)-(16) represent a system of five (non-linear) equations in the seven (unconstrained) variables

$$D,\ i_{L_\mathrm{i}}^0,\ i_{L_\mathrm{r}}^0,\ k_r,\ q_i,\ q_x,\ q_r \tag{17}$$

and, once solved, ensure that the designed converter features both ZVS and ZVDS behavior at its steady state. Furthermore, note that they are independent of the switching frequency f_s, which is required to denormalize the system according to (4) and represents an additional free design parameter.

Unfortunately, the solution of these equations cannot be achieved in closed form due to their non-linearity. Yet, they can be fed into any numerical solver (usually, a numerical optimization tool) to get, with minimal computational effort, the parameters values that ensure the desired behavior. The Wolfram Mathematica notebook software developed for solving the system (12)-(16) is available online[2] and as paper additional material.

Interestingly enough, despite the non-linearity, we always observed that the achieved equation system has a "good" behavior: under the assumption that a solution exists, only five degrees of freedom are required to satisfy the five constraints (12)-(16). Furthermore, in the most common case (in particular, in the ideal lossless system, *i.e.*, when all quality factors are set to infinity and $v_D = 0$), convergence of the numerical optimization tool is not an issue, and the selection of a proper initial point is required only for reducing the computation time. With respect to this, it is worth highlighting that the system has shown to be smooth, so the best candidate as initial point is the solution of another system whose design parameters (e.g., μ, k_i, etc.) are similar to those of the considered one. As an example, the solution of the corresponding ideal lossless system is a good candidate as the initial point of a lossy system. This is the approach we followed in the two examples of Sec. VI.

Interestingly, from a mathematical point of view, only five among the unconstrained parameters in (17) are returned by the solver. This means that two parameters are actually degrees of freedom.

In the example provided is Sec. VI, aiming to optimize the the hardware implementation complexity of the converter, we fix the value of D and k_r. In fact, a 50% duty cycle clock is usually the simplest one to realize, while fixing k_r means setting the ratio between the inductances of the two inductors present in the circuit of Fig. 2(b) (or between the inductance of the inductor and the equivalent inductance and the transformer for the circuit in Fig. 2(a)). The latter may be extremely useful both in an off-the-shelf realization and in an integrated one, since the number of available inductors is usually much more limited with respect to the number of available capacitors.

Despite the one mentioned above is the optimization choice we made in this paper, it is worth stressing that other choices are possible and can be easily achieved. As an example, one may want to exploit the degrees of freedom to reduce the peak values of voltage or current on the active devices, so reducing their stress and improving reliability and/or reducing costs. Another option is to maximize the converter efficiency, η defined as the ratio between the power on the output load and the power required from the input source V_in, that considering

[1]Note that a similar condition for $v_{C_\mathrm{i}}(\theta)$ and $v_{C_\mathrm{r}}(\theta)$ is not necessary, since it is always satisfied.

[2]see http://dcdc.signalprocessing.it

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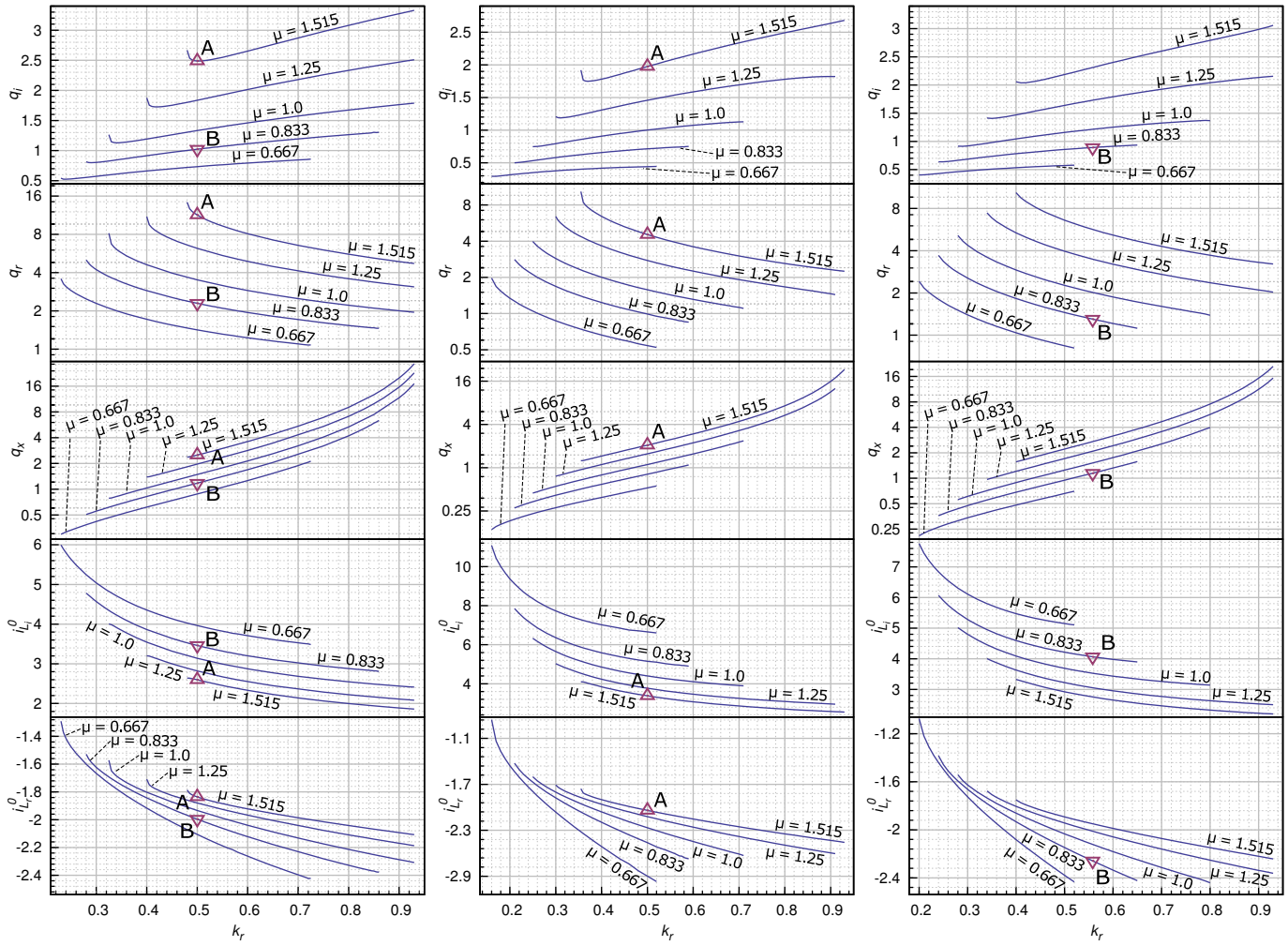

Fig. 8. Design curves for the dimensionless system. (a): for $D = 0.5$, $k_i = 1$, $v_d^{\rm ON} = 0$ and all quality factors to infinity (*i.e.,* a lossless system); (b): for $D = 0.5$, $k_i = 1$, $v_D = 0.091$, $Q_{L_{\rm i}} = \infty$, $Q_{L_{\rm r}} = Q_{L_{\rm x}} = 36$, $Q_{C_{\rm i}} = Q_{C_{\rm r}} = 28$, $g_{DS} = 162$, $g_D = 162$ and $g_{\rm i} = g_{\rm o} = 218$ (design example 1); and (c): for $D = 0.5$, $k_i = 0.98$, $v_D^{\rm ON} = 0.058$, $Q_{L_{\rm i}} = Q_{L_{\rm x}} = 45$, $Q_{L_{\rm i}} = 47$, $Q_{C_{\rm i}} = Q_{C_{\rm r}} = \infty$, $g_{DS} = 2700$, $g_D = 96$, $g_{\rm i} = 720$ and $g_{\rm o} = 56.5$ (design example 2). These design curves have been used in Sec. VI for the design of the two prototypes, whose working points have been identified by the markers A and B.

the normalization we introduced can be defined as

$$\eta = \frac{\displaystyle\int_0^{2\pi} i_{L_{\rm r}}(\theta)\,{\rm d}\theta}{\mu \displaystyle\int_0^{2\pi} i_{L_{\rm i}}(\theta)\,{\rm d}\theta} \tag{18}$$

Also in this case, to limit the complexity of this paper, we leave the detailed description of these optimized solutions to future contributions.

V. Design Curves

As observed in the previous section, the advantage of the proposed dimensionless analysis is that one can solve the system composed by (12)-(16) without any assumption on the real circuit parameters, thus obtaining general design curves. Then, a circuit designer can simply ensure the optimal working point by looking at the achieved dimensionless solution and denormalize it with the actual values of $V_{\rm o}$, $I_{\rm o}$ and f_s. In case of an isolated topology, also the value of n has to be used in the denormalization process.

In this paper we limit ourselves to propose the three design curves sets of Fig. 8. The curves refer to the two design examples that will be considered in Sec. VI, and have to be interpreted as follows.

The plots report, from top to bottom, the values of q_i, q_r, q_x, $i^0_{L_{\rm i}}$ and $i^0_{L_{\rm r}}$ that ensure both ZVS and ZVDS behavior at stationary condition, as a function of k_r and μ, under the assumption that k_i, D and all other technological constrained parameters are fixed. Given the actual value of μ, *i.e.,* given the ratio between input and output voltage, and by looking at the design curves corresponding to the actual values of the parameters fixed by technological constraints, a designer can simply select a value of k_r of his/her choice, and immediately get q_i, q_r and q_x. Then, given $V_{\rm o}$, $I_{\rm o}$ and f_s, by using (4) it is possible to get the values of $C_{\rm i}$, $C_{\rm r}$, $L_{\rm x}$ and $L_{\rm r}$ of the equivalent circuit of Fig. 5(c). In case of a non-isolated

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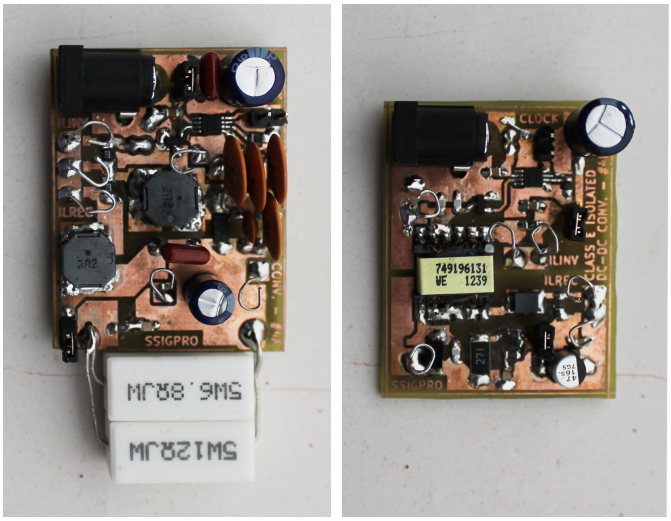

(a) (b)

Fig. 9. Photograph of the designed prototypes. (a): 2.5 W non-isolated dc-dc converter; and (b): 500 mW isolated dc-dc converter.

topology, these values correspond directly to $C_{\rm inv}$, $C_{\rm rec}$, $L_{\rm pair}$ and $L_{\rm rec}$; in case of an isolated topology, $C_{\rm rec}$ and $L_{\rm rec}$ are modified by the turns ratio value. In the next section, two design examples will be provided to better clarify the design procedure.

VI. Prototypes Design and Measurements

The proposed methodology is validated through the design, implementation and measurements of two dc-dc converters realized with off-the-shelves components. The first one has a non-isolated topology, a low switching frequency and it is built with low-quality inductors and capacitors. The second one is isolated, running at higher frequency and designed with high-quality reactive elements. The pictures of the two prototypes are shown in Fig. 9(a) and Fig. 9(b), respectively. The design procedure is composed of two steps: the first design step is performed neglecting any kind of loss in the circuit in order to get, with the help of the design curves of Fig. 8(a), a first approximation of the component values, and consequently an indication of their parasitics. Then we take into account all circuit non idealities (diode voltage drop, inductor and capacitor quality factors *etc.*) to reach the final accurate design point by exploiting the design curves of Fig. 8(b) and Fig. 8(c).

Design example 1. Let us consider a 2.5 W non-isolated dc-dc converter, with $V_{\rm in} = 5\,{\rm V}$ and $V_{\rm out} = 3.3\,{\rm V}$ (so $I_{\rm out} = 0.76\,{\rm A}$ and $R_{\rm load} = 4.36\,\Omega$), operating at approximately 500 kHz. The desired voltage ratio imposes $\mu = 1.515$ and, since it is a non-isolated topology, we have $L_{\rm i} = 0\,{\rm H}$ and so $k_i = 1$. Let us also set the two additional constraints $k_r = 0.5$ (to achieve $L_x = L_r$ and thus $L_{\rm pair} = L_{\rm rec}$) and $D = 0.5$ (*i.e.*, $\theta_3 = \pi$). If we initially assume that all circuit elements are ideal, *i.e.*, $V_D^{\rm ON} = 0$ and all quality factors equal to infinity, the solution of (12)-(16) is the point indicated with the marker "A" in Fig. 8(a) and it is given by:

$$q_i = 2.49,\ q_r = 11.3,\ q_x = 2.50,\ i^0_{L_{\rm i}} = 2.60,\ i^0_{L_{\rm r}} = -1.84 \quad (19)$$

Then q_i, q_r, q_x and k_r can be denormalized using (4) to get

$$C_{\rm inv} = 29.4\,{\rm pF},\ C_{\rm rec} = 6.43\,{\rm pF},\ L_{\rm pair} = L_{\rm rec} = 3.47\,\mu{\rm H}$$

Given a first approximation of circuit elements values, it is possible to get a realistic indication of their parasitics. For example, let us assume that we wish to design the converter with inductors that, in the range of a few μH and for the desired frequency, have $Q_{L_{\rm x}} = Q_{L_{\rm r}} \approx 36$. We desire to use standard ceramic capacitors with X7R dielectric, which have a quite low merit factor at the desired operating frequency, quantifiable in $Q_{C_{\rm i}} = Q_{C_{\rm r}} \approx 28$. Furthermore, we use a IRLML0030TR N-MOS transistor by International Rectifier, with $R_{DS}^{\rm ON} \approx 27\,{\rm m}\Omega$ ($g_{DS} \approx 162$) and a DB24307 Schottky barrier diode from Panasonic with $V_D \approx 0.3\,{\rm V}$ and $R_D^{\rm ON} \approx 30\,{\rm m}\Omega$ ($v_D = 0.091$ and $g_D \approx 145$). Finally, we add two $20\,{\rm m}\Omega$ current sensing resistors, with $g_{\rm i} = g_{\rm o} \approx 218$.

The design curves corresponding to these values have been computed and plotted in Fig. 8(b). The desired solution is the point with the marker "A", and it is given by

$$q_i = 1.97,\ q_r = 4.54,\ q_x = 2.06,\ i^0_{L_{\rm i}} = 3.38,\ i^0_{L_{\rm r}} = -2.04$$

that is *remarkably* different from (19), mainly due to the low quality factors of inductors and capacitors. This confirms how important is the consideration and the correct estimation of parasitics in this kind of converters. Denormalization leads to

$$C_{\rm inv} = 37.0\,{\rm pF},\ C_{\rm rec} = 16.1\,{\rm pF},\ L_{\rm pair} = L_{\rm rec} = 2.86\,\mu{\rm H}$$

For a more feasible solution, we exploit the last degree of freedom given by the oscillation frequency, noticing that by slightly increasing the f_s from 500 kHz to 649.6 kHz, we get

$$C_{\rm inv} = 28.5\,{\rm pF},\ C_{\rm rec} = 12.4\,{\rm pF},\ L_{\rm pair} = L_{\rm rec} = 2.2\,\mu{\rm H}$$

In this way, we can use two inductors with a standard commercial values for $L_{\rm pair}$ and $L_{\rm rec}$, while we can approximate $C_{\rm inv} = 30\,{\rm pF}$ and $C_{\rm rec} = 12.2\,{\rm pF}$ placing a few commercial capacitors in parallel.

Output voltage and current measured from the prototype are in the expected range ($V_{\rm out} = 3.1\,{\rm V}$ and $I_{\rm out} = 680\,{\rm mA}$). Also the measured efficiency (59%) agrees with the theoretical one (58%) computed accordingly to (18). The measured waveforms for $V_{C_{\rm inv}}(t)$, $V_{C_{\rm rec}}(t)$, $I_{\rm inv}(t)$ and $I_{\rm rec}(t)$ are plotted in Fig. 10 (solid line), along with the theoretical ones computed with the developed model (marker points). As it can be noted, the matching is almost perfect; it is also possible to see a very good behavior in terms of both ZVS and ZVDS.

Design example 2. Let us consider a 500 mW isolated dc-dc converter, with $V_{\rm in} = 5\,{\rm V}$, $V_{\rm out} = 12\,{\rm V}$ (so $I_{\rm out} = 41.7\,{\rm mA}$ and $R_{\rm load} = 288\,\Omega$), operating at approximately 1 MHz. Let us also assume a transformer turns ratio $n = 2$. By considering all the normalizations introduced in Sec. III, we have $\mu = nV_{\rm in}/V_{\rm out} = 0.833$. Here, k_i is given by the transformer coupling coefficient k (so ideally $k_i = 1$), while $k_r = kL_{\rm p}/(L_{\rm p} + L_{\rm rec}/n^2)$ determines the relation between $L_{\rm p}$ and $L_{\rm rec}$. As in the previous example, we can start with the assumption of ideal devices and $k_r = 0.5$, that leads from Fig. 8(a) (see marker "B") to

$$q_i = 1.03,\ q_r = 2.29,\ q_x = 1.18,\ i^0_{L_{\rm i}} = 3.46,\ i^0_{L_{\rm r}} = -1.99 \quad (20)$$

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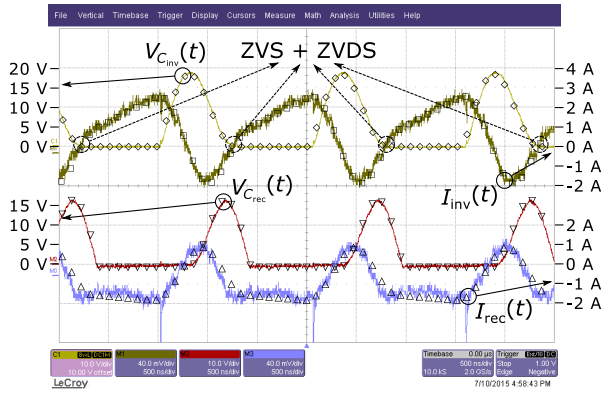

Fig. 10. Measured current and voltage waveforms for the 2.5 W non-isolated dc-dc converter prototype, compared with the expected theoretical ones (dark markers) computed with the proposed model.

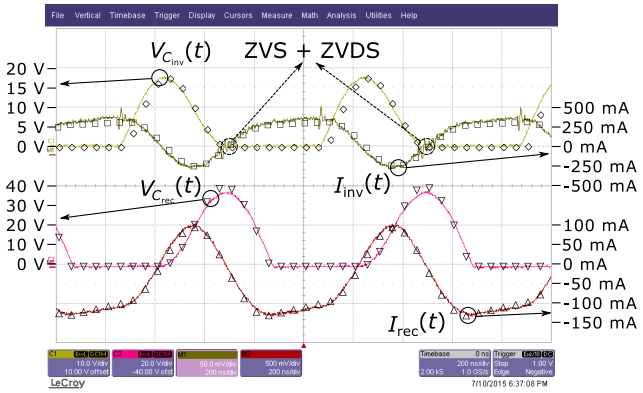

Fig. 11. Measured current and voltage waveforms for the 500 mW isolated dc-dc converter prototype, compared with the expected theoretical ones (dark markers) computed with the proposed model.

that is denormalized to

$$C_{\rm inv}{=}2.15\,{\rm nF},\ C_{\rm rec}{=}241\,{\rm pF},\ L_{\rm p}{=}13.5\,\mu{\rm H},\ L_{\rm rec}{=}54.1\,\mu{\rm H}$$

The best fit for commercial transformer is a $10.9\,\mu$H *WE-FLEX* transformer by Würth Elektronik, with coupling coefficient $k \approx 0.98$ and quality factor ≈ 45. Consequently, we use a smaller value also for the inductor, i.e., $L_{\rm rec} = 33\,\mu$H with a quality factor ≈ 47. Without any knowledge on how the transformer losses are divided into the $R_{\rm core}$ and $R_{\rm p}$, we assume $Q_{L_{\rm i}} \approx Q_{L_{\rm x}} \approx 45$, while $Q_{L_r} \approx 47$. Furthermore, $k_i \approx 0.98$ and $k_r \approx 0.558$. In this prototype we use ceramic capacitors with C0G dielectric, that ensure extremely high performance ($Q_{C_{\rm i}} > 1000$ and $Q_{C_{\rm r}} > 1000$) so that we can assume an infinite quality factor. We also use the same N-MOS as in the previous example (with here $g_{DS} \approx 2700$), while the rectifying diode of our choice is a ES1B by Vishay, with $V_D^{\rm ON} \approx 0.7\,{\rm V}$ and $R_D^{\rm ON} \approx 3\,\Omega$ ($v_D = 0.058$ and $g_D \approx 96$). The design is completed with two current sensing resistors, a $0.1\,\Omega$ at the primary side ($g_{\rm i} \approx 720$) and a $5.1\,\Omega$ at the secondary side ($g_{\rm o} \approx 56.5$)

The solution of the system considering these technological constrained parameters can be found looking at the design curves of Fig. 8(c). Due to the high quality of the component used, this design leads to a solution (the marker point "B" in the figure) not very different from (20)

$$q_i{=}0.910,\ q_r{=}1.35,\ q_x{=}1.16,\ i_{L_{\rm i}}^0{=}3.97,\ i_{L_{\rm r}}^0{=}{-}2.23$$

that, by slightly increasing the operating frequency to $f_s = 1.25\,{\rm MHz}$, is denormalized as

$$C_{\rm inv}{=}1.95\,{\rm nF},\ C_{\rm rec}{=}328\,{\rm pF},\ L_{\rm p}{=}10.9\,\mu{\rm H},\ L_{\rm rec}{=}33\,\mu{\rm H}$$

where we can approximate $C_{\rm inv} = 2\,{\rm nF}$ and $C_{\rm rec} = 330\,{\rm pF}$.

Measurements show $V_{\rm out} = 11.8\,{\rm V}$ and $I_{\rm out} = 40.3\,{\rm mA}$ with a 75% efficiency, that are very similar to the theoretically expected ones (12.0 V, 41.7 mA, 77%). Measured waveforms are plotted in Fig. 11 (solid lines) and compared with the ones computed according to the developed theoretical model (marker points). Also in this case the matching is extremely good.

VII. Conclusion

In this paper, a new approach for class-E dc-dc converter design has been proposed. Differently from the state-of-the-art approach, the proposed methodology is based on the *exact* circuit analysis, and does not need any strong simplifying assumptions such as the common sinusoidal approximation. Furthermore, the approach is capable of taking into account the most important circuit non-idealities, ensuring a very high adherence between the actual circuit evolution and the modeled one. A dimensionless approach also allows to achieve design curves that can be used to get in few seconds the optimized circuit design. As a proof of concept, two dc-dc converter prototypes are presented. Measurements confirm an almost perfect matching with the expected results.

Appendix
Mathematical Formulations of Sec. III

A. Zone Z_1

In Z_1 $v_{C_{\rm r}}^{(Z_1)}$ is assumed constant. Eq. (7) is so reduced to a third order system in the tree variables $i_{L_{\rm i}}^{(Z1)}$, $i_{L_{\rm r}}^{(Z1)}$ and $v_{C_{\rm i}}^{(Z_1)}$. By properly rearranging all terms in (7), the system can be conveniently rewritten as

$$\frac{\rm d}{{\rm d}\theta}\begin{pmatrix} i_{L_{\rm i}}^{(Z_1)}(\theta) \\ i_{L_{\rm r}}^{(Z_1)}(\theta) \\ v_{C_{\rm i}}^{(Z_1)}(\theta) \end{pmatrix} = \underline{\boldsymbol{A}}^{(Z_1)} \begin{pmatrix} i_{L_{\rm i}}^{(Z_1)}(\theta) \\ i_{L_{\rm r}}^{(Z_1)}(\theta) \\ v_{C_{\rm i}}^{(Z_1)}(\theta) \end{pmatrix} + \underline{\boldsymbol{B}}^{(Z_1)} \qquad \text{(A.1)}$$

where all elements of $\underline{\boldsymbol{A}}^{(Z_1)} \in \mathbb{R}^{3\times3}$ and of $\underline{\boldsymbol{B}}^{(Z_1)} \in \mathbb{R}^3$ can be retrieved by comparing (A.1) with (7) under the assumption that $m^{\rm ON} = 0$ and $d^{\rm ON} = 1$. Even if it is not possible to provide a full mathematical demonstration, the matrix $\underline{\boldsymbol{A}}^{(Z_1)}$ always features two complex conjugated eigenvalues $-\sigma_0 \pm j\omega_0$ (with associated eigenvectors $\underline{\boldsymbol{w}}_R \pm j\underline{\boldsymbol{w}}_I$) and a real negative one $-\lambda_3$ (with associated eigenvector $\underline{\boldsymbol{w}}_3$) that can be easily numerically computed. In this case, the solution of (A.1) in matricial form is given by (A.2). Note that three unknown coefficients c_1, c_2 and c_3 are presents, and determined once the initial condition of the system is given.

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$$\begin{pmatrix} i_{L_\mathrm{i}}^{(Z_1)}(\theta) \\ i_{L_\mathrm{r}}^{(Z_1)}(\theta) \\ v_{C_\mathrm{i}}^{(Z_1)}(\theta) \end{pmatrix} = \begin{pmatrix} \underline{\boldsymbol{w}}_R & \underline{\boldsymbol{w}}_I & \underline{\boldsymbol{w}}_3 \end{pmatrix} \begin{pmatrix} e^{-\sigma_0\theta}\cos(\omega_0\theta) & e^{-\sigma_0\theta}\sin(\omega_0\theta) & 0 \\ -e^{-\sigma_0\theta}\sin(\omega_0\theta) & e^{-\sigma_0\theta}\cos(\omega_0\theta) & 0 \\ 0 & 0 & e^{-\lambda_3\theta} \end{pmatrix} \begin{pmatrix} c_1 \\ c_2 \\ c_3 \end{pmatrix} - \left(\underline{\boldsymbol{A}}^{(Z_1)}\right)^{-1} \underline{\boldsymbol{B}}^{(Z_1)} \tag{A.2}$$

$$\begin{pmatrix} i_{L_\mathrm{i}}^{(Z_2)}(\theta) \\ i_{L_\mathrm{r}}^{(Z_2)}(\theta) \\ v_{C_\mathrm{i}}^{(Z_2)}(\theta) \\ v_{C_\mathrm{r}}^{(Z_2)}(\theta) \end{pmatrix} = \begin{pmatrix} \underline{\boldsymbol{w}}_{R1} & \underline{\boldsymbol{w}}_{I1} & \underline{\boldsymbol{w}}_{R2} & \underline{\boldsymbol{w}}_{I2} \end{pmatrix} \begin{pmatrix} e^{-\sigma_1\theta}\cos(\omega_1\theta) & e^{-\sigma_1\theta}\sin(\omega_1\theta) & 0 & 0 \\ -e^{-\sigma_1\theta}\sin(\omega_1\theta) & e^{-\sigma_1\theta}\cos(\omega_1\theta) & 0 & 0 \\ 0 & 0 & e^{-\sigma_2\theta}\cos(\omega_2\theta) & e^{-\sigma_2\theta}\sin(\omega_2\theta) \\ 0 & 0 & -e^{-\sigma_2\theta}\sin(\omega_2\theta) & e^{-\sigma_2\theta}\cos(\omega_2\theta) \end{pmatrix} \begin{pmatrix} c_1 \\ c_2 \\ c_3 \\ c_4 \end{pmatrix} - \left(\underline{\boldsymbol{A}}^{(Z_2)}\right)^{-1} \underline{\boldsymbol{B}}^{(Z_2)} \tag{A.4}$$

$$\begin{pmatrix} i_{L_\mathrm{i}}^{(Z_3)}(\theta) \\ i_{L_\mathrm{r}}^{(Z_3)}(\theta) \\ v_{C_\mathrm{r}}^{(Z_3)}(\theta) \end{pmatrix} = \begin{pmatrix} \underline{\boldsymbol{w}}_R & \underline{\boldsymbol{w}}_I & \underline{\boldsymbol{w}}_3 \end{pmatrix} \begin{pmatrix} e^{-\sigma_0\theta}\cos(\omega_0\theta) & e^{-\sigma_0\theta}\sin(\omega_0\theta) & 0 \\ -e^{-\sigma_0\theta}\sin(\omega_0\theta) & e^{-\sigma_0\theta}\cos(\omega_0\theta) & 0 \\ 0 & 0 & e^{-\lambda_3\theta} \end{pmatrix} \begin{pmatrix} c_1 \\ c_2 \\ c_3 \end{pmatrix} - \left(\underline{\boldsymbol{A}}^{(Z_3)}\right)^{-1} \underline{\boldsymbol{B}}^{(Z_3)} \tag{A.6}$$

B. Zone Z_2

The system evolution is regulated by

$$\frac{\mathrm{d}}{\mathrm{d}\theta} \begin{pmatrix} i_{L_\mathrm{i}}^{(Z_2)}(\theta) \\ i_{L_\mathrm{r}}^{(Z_2)}(\theta) \\ v_{C_\mathrm{i}}^{(Z_2)}(\theta) \\ v_{C_\mathrm{r}}^{(Z_2)}(\theta) \end{pmatrix} = \underline{\boldsymbol{A}}^{(Z_2)} \begin{pmatrix} i_{L_\mathrm{i}}^{(Z_2)}(\theta) \\ i_{L_\mathrm{r}}^{(Z_2)}(\theta) \\ v_{C_\mathrm{i}}^{(Z_2)}(\theta) \\ v_{C_\mathrm{r}}^{(Z_2)}(\theta) \end{pmatrix} + \underline{\boldsymbol{B}}^{(Z_2)} \tag{A.3}$$

where $\underline{\boldsymbol{A}}^{(Z_2)} \in \mathbb{R}^{4\times4}$ and $\underline{\boldsymbol{B}}^{(Z_2)} \in \mathbb{R}^4$. The matrix $\underline{\boldsymbol{A}}^{(Z_2)}$ has two couples of complex conjugates eigenvalues $-\sigma_1 \pm j\omega_1$ (with associated eigenvectors $\underline{\boldsymbol{w}}_{R1} \pm j\underline{\boldsymbol{w}}_{I1}$) and $-\sigma_2 \pm j\omega_2$ (with associated eigenvectors $\underline{\boldsymbol{w}}_{R2} \pm j\underline{\boldsymbol{w}}_{I2}$). The evolution of all normalized current and voltage signals is given by the sum of two damped sinusoidal tones, with angular frequency ω_1 and ω_2, whose expression is given in (A.4).

C. Zone Z_3

The evolution here is regulated by a third order system as in Z_1, and it is described by

$$\frac{\mathrm{d}}{\mathrm{d}\theta} \begin{pmatrix} i_{L_\mathrm{i}}^{(Z_3)}(\theta) \\ i_{L_\mathrm{r}}^{(Z_3)}(\theta) \\ v_{C_\mathrm{r}}^{(Z_3)}(\theta) \end{pmatrix} = \underline{\boldsymbol{A}}^{(Z_3)} \begin{pmatrix} i_{L_\mathrm{i}}^{(Z_3)}(\theta) \\ i_{L_\mathrm{r}}^{(Z_3)}(\theta) \\ v_{C_\mathrm{r}}^{(Z_3)}(\theta) \end{pmatrix} + \underline{\boldsymbol{B}}^{(Z_3)} \tag{A.5}$$

with $\underline{\boldsymbol{A}}^{(Z_3)} \in \mathbb{R}^{3\times3}$ and $\underline{\boldsymbol{B}}^{(Z_3)} \in \mathbb{R}^3$. Similarly to $\underline{\boldsymbol{A}}^{(Z_1)}$, also $\underline{\boldsymbol{A}}^{(Z_3)}$ features two complex conjugated eigenvalues $-\sigma_0 \pm j\omega_0$ (with associated eigenvectors $\underline{\boldsymbol{w}}_R \pm j\underline{\boldsymbol{w}}_I$) and a real one $-\lambda_3$ (with associated eigenvector $\underline{\boldsymbol{w}}_3$). The evolution of the system is regulated by (A.6).

D. Zone Z_4

In Z_4, $v_{C_\mathrm{i}}^{(Z_4)}$ and $v_{C_\mathrm{r}}^{(Z_4)}$ are constrained, and (7) is reduced to

$$\frac{\mathrm{d}}{\mathrm{d}\theta} \begin{pmatrix} i_{L_\mathrm{i}}^{(Z_4)}(\theta) \\ i_{L_\mathrm{r}}^{(Z_4)}(\theta) \end{pmatrix} = \underline{\boldsymbol{A}}^{(Z_4)} \begin{pmatrix} i_{L_\mathrm{i}}^{(Z_4)}(\theta) \\ i_{L_\mathrm{r}}^{(Z_4)}(\theta) \end{pmatrix} + \underline{\boldsymbol{B}}^{(Z_4)} \tag{A.7}$$

where $\underline{\boldsymbol{A}}^{(Z_4)} \in \mathbb{R}^{2\times2}$ and $\underline{\boldsymbol{B}}^{(Z_4)} \in \mathbb{R}^2$. Since $\underline{\boldsymbol{A}}^{(Z_4)}$ has always two real negative eigenvalues $-\lambda_1$ and $-\lambda_2$ with associated eigenvectors $\underline{\boldsymbol{w}}_1$ and $\underline{\boldsymbol{w}}_2$, the evolution is simply given by:

$$\begin{pmatrix} i_{L_\mathrm{i}}^{(Z_4)}(\theta) \\ i_{L_\mathrm{r}}^{(Z_4)}(\theta) \end{pmatrix} = \begin{pmatrix} \underline{\boldsymbol{w}}_1 & \underline{\boldsymbol{w}}_2 \end{pmatrix} \begin{pmatrix} e^{-\lambda_1\theta} & 0 \\ 0 & e^{-\lambda_2\theta} \end{pmatrix} \begin{pmatrix} c_1 \\ c_2 \end{pmatrix} - \left(\underline{\boldsymbol{A}}^{(Z_4)}\right)^{-1} \underline{\boldsymbol{B}}^{(Z_4)} \tag{A.8}$$

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