Power loss analysis and measurement of a high efficiency DC-DC converter for EV traction AC drives

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Abstract **- Previous works have shown the power design effectiveness of novel H-bridge-based dc-dc boost conversion structure, as well as the feasibility of real-time dc-link voltage adaptation to inverter load, in battery-supplied ac motor drives. In this paper a novel test bench has been developed, suitable for power loss measurements in high-efficiency bi-directional dc-dc converters. In order to allow for quasi-direct measurement of the lost power, the concept is to operate the converter by input current having constant module, handling alternating energy flow between two large capacitor banks at given input/output DC voltages. Accordingly, the input current reference is a low frequency (65 Hz) rectangular-wave, whose duty-cycle is regulated by suitable voltage loop due to constant module operation. Except for added large capacitor banks' losses and other secondary effects related to 65Hz operation, the input DC power supply is shown equivalent to conversion losses at given DC working point.**
The results point-out the high efficiency of the conversion structure well matched with simple analytical models.

I. INTRODUCTION

As far as dc-voltage battery-supplied ac motor drives are investigated [3], the cost-effectiveness of a proper H-Bridge-based boost dc-dc conversion structure has been demonstrated [1], interposed between battery and inverter to adapt the dc-link voltage to load requirements.

This result has been achieved thanks to the large current rating reduction in the inverter's power module design, mainly related to the wide voltage range of practical battery packs [1,3]. The possible drawbacks, in weight and cost of the input coupling reactor, have been shown balanced by considerable decrease on rms current requirements of filter capacitors, thanks also to the peculiar integration of inter-phase transformer and input coupling inductance functions in a single power reactor, namely "T+L" reactor [1].

New high rms-current-rated non-electrolytic small film power capacitors have been also adopted to filter the dc-link PWM current ripple [2]. Further improvements in size, cost and transient dc-link voltage response have been reliably achieved by adopting proper non-linear control and modulation strategies [2], purposely analyzed and developed in order to overcome the peculiar low energy-storage operation of the bi-directional boost conversion. The experimental verification in [2] has been carried-out on a 30 kW prototype convertor system adopting commercial 3-phase IGBT Intelligent Power Modules (IPM). This convertor system (whose scheme is reported in Fig.1) is under test in the work, concerning specifically the measurement of efficiency and the related verification of power loss models in the various operating conditions of practical interest in EV or HEV traction AC drives. The very high efficiency of the adopted boost conversion structure has requested a novel measurement concept, purposely defined and experimentally developed.

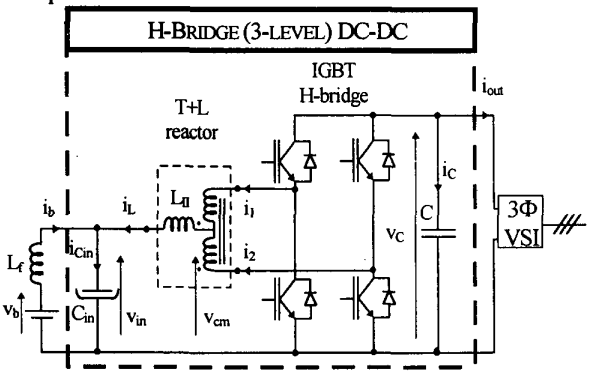

Fig. 1. Electric scheme of the H-bridge boost conversion structure suited for battery-supplied AC drives. The discontinuous frame includes the system under test throughout the paper.

II. DESCRIPTION OF THE POWER CONVERSION SYSTEM.

A summarized description of the conversion system is reported. Fig.1 reports the electrical scheme of the power converter as a part of battery supplied AC drive.

A. Variables definition.

With reference to Fig.1 scheme, a list of system variables and parameters is introduced as used in the following; mean values are expressed by capital letters of the corresponding instantaneous variables.

$P_{in} \cong V_{in} I_L$: converted input power;
i_L: total converted input current;
v_{in}: converter's input voltage;
v_c: converter's output voltage;
C_{in}: input capacitor inside the converter;
C: inner output capacitor (non-electrolytic);
L_{II}: T+L reactor's input inductance;
R_{ph}: T+L phase resistance (each winding);
$f_{SW}=1/T_{SW}$:switching modulation frequency (each phase);
I_{label}: H-bridge IPM rated current;
$a_{SW}=\Delta I_{L,pk}/I_L$: switching ratio (peak ripple/mean value);
m_1, m_2: modulation indexes;
D: H-bridge average duty-cycle ($\equiv M_1, M_2$).

TABLE I - RATINGS OF CONVERTOR SYSTEM.

RATED VALUES							
P_{in} [kW]	v_{in} [V]	v_c [V]	f_{SW} [kHz]	C_{in} [mF] 350[V] electrol.	C [μF] 600[V] film	L_{II} [μH]	I_{label} [A] PM200 CVA060
15 30 max	150÷ 300	v_{in}÷ 400	10	3.3	330	38	200

B. Current dynamics.

The T+L reactor behavior is modeled in terms of state variables through a transformation from "phase" to "mode" variables (common- and differential-mode of phase variables). Referring to a generic couple of phase variables x_1, x_2, the correspondent "mode" variables vector is:

$$\mathbf{x}_{cm,dm} = \tfrac{1}{2}\mathbf{U}\,\mathbf{x}_{1,2} \quad ; \quad \mathbf{U} = \begin{bmatrix} 1 & 1 \\ 1 & -1 \end{bmatrix} \qquad (1)$$

This transformation defines common and differential mode modulation indexes, voltages, currents and fluxes ($v_{cm,dm}$, $m_{cm,dm}$, $i_{cm,dm}$, $\psi_{cm,dm}$, respectively). Typical modulation index waveforms are shown in Fig.2, in two operating conditions differing for D value. D is equal to common mode index mean value, and then very close (excepting for inner voltage drops) to the i/o voltage ratio:

$$\mathbf{D} = \mathbf{M}_{cm} \cong {}^{V_{in}}\!/_{V_c} \qquad (2)$$

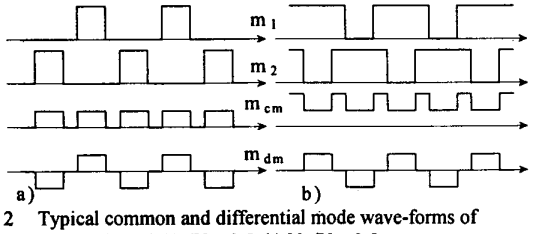

Fig. 2 Typical common and differential mode wave-forms of modulation: a) $V_{in}/V_C<0.5$; b) $V_{in}/V_C>0.5$.

Notice that, being the "phase" ripple frequency f_{SW}, and due to half modulation period displacement of phase modulation indexes, the common-mode fundamental frequency is "$2\cdot f_{SW}$" (second harmonic), while differential-mode frequency is f_{SW} (first harmonic).

"Mode" inductances (3) are derived as in (3):

$$\begin{cases} \mathbf{L}_{cm} = \dfrac{\psi_{cm}}{i_{cm}} = \dfrac{(\psi_1 - \psi_2)}{\frac{1}{2} i_L} = 2\mathbf{L}_{II} \\ \mathbf{L}_{dm} = \dfrac{\psi_{dm}}{i_{dm}} = \dfrac{\frac{1}{2}(\psi_1 - \psi_2)}{i_{dm}} = \dfrac{1}{2}\mathbf{L}_{\mu 12} \end{cases} \qquad (3)$$

where L_{II} and $L_{\mu 12}$ are the inductance values which can be measured: between common input and short-circuited phase terminals; between the phase terminals by common input left open (respectively 38μH and 3.3mH in the design).

The current dynamics can be then expressed in terms of common- and differential-mode variables, disregarding on (4) resistive and power switches drops:

$$\frac{\mathbf{d}}{\mathbf{dt}}\left\{\begin{bmatrix} \mathbf{L}_{cm} & 0 \\ 0 & \mathbf{L}_{dm} \end{bmatrix} \cdot \begin{vmatrix} i_{cm} \\ i_{dm} \end{vmatrix}\right\} = \begin{vmatrix} 1 \\ 0 \end{vmatrix} v_{in} - \begin{vmatrix} m_{cm} \\ m_{dm} \end{vmatrix} v_C \qquad (4)$$

C. Flux and current waveform and properties.

Multilevel conversion structures own peculiar properties concerning modulation ripple both on i/o currents and on T+L reactor fluxes, leading to a general reduction of ripple terms, falling down to cancellation in singular working points (D=1/2, in particular) [1]. Since the differential-mode flux is generated by modulation ripple without DC component, the differential-mode current can be freely designed to be very small with respect to common-mode one (3A peak max in the design). This is why "i_{dm}" will be ignored in the calculation of rms current values.

Referring to continuos current mode of operation, the input current ripple is a "second harmonic" triangle. The total input rms current can be then referred to mean value by (5):

$$\mathbf{I}_{L,rms} = \mathbf{I}_L \sqrt{1 + \frac{a_{SW}^2}{3}} \qquad \text{(continuos mode)} \qquad (5)$$

Note a_{SW} is a function of D by two-range expressions (6):

$$\mathbf{a}_{SW} = \frac{\Delta \mathbf{I}_{in,pk}}{\mathbf{I}_{batt}} = \begin{cases} \frac{1}{4}\dfrac{V_c}{I_L}\dfrac{T_{SW}}{L_{II}}(1-2D)\cdot D; & @\,D < \frac{1}{2} \\ \frac{1}{4}\dfrac{V_c}{I_L}\dfrac{T_{SW}}{L_{II}}(2D-1)\cdot(1-D); & @\,D > \frac{1}{2} \end{cases} \qquad (6)$$

Correspondingly, input and output capacitors' rms current values are derived (7,8) [1], as depicted in Fig.3.

$$\mathbf{I}_{Cin,rms} = \mathbf{I}_L \frac{a_{SW}}{\sqrt{3}} \qquad (7)$$

$$\mathbf{I}_{C,rms} = \begin{cases} \mathbf{I}_L \cdot \sqrt{\frac{1}{2} D\left(1 + \frac{1}{3} a_{SW}^2\right) - D^2} & @\,D \le \frac{1}{2} \\ \mathbf{I}_L \cdot \sqrt{\frac{1}{2}(3D-1)\left(1 + \frac{1}{3} a_{SW}^2\right) - D^2} & @\,D \ge \frac{1}{2} \end{cases} \qquad (8)$$

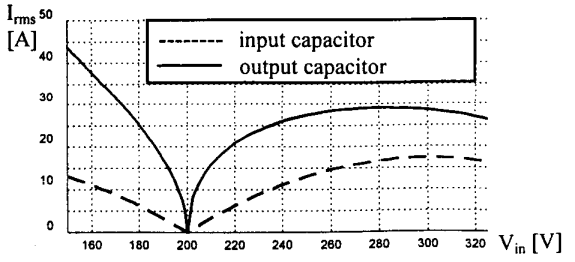

Fig.3 I/O capacitors rms current values vs. V_{in} @ V_c=400V, P=30kW

Common-mode flux peak value is reported (9), both in terms of common-mode and of converter's input quantities:

$$\psi_{cm,pk} = \mathbf{L}_{cm}\mathbf{I}_{cm} + \Delta\psi_{cm,pk} = \mathbf{L}_{II}\mathbf{I}_L + \Delta\psi_{cm,pk} \qquad (9)$$

where Δ indicates alternative components, the only component in differential-mode flux (steady state):

$$\psi_{dm,pk} \equiv \Delta\psi_{dm,pk} \qquad (10)$$

Common-mode waveform is a "second harmonic" triangle while differential-mode is a "first harmonic" trapezoid, according to integration of the respective waveforms in Fig.2.

Analogously to capacitor currents, the peak flux values (11,12) are differing in D operating ranges, as depicted by Fig.4, showing also the T+L reactor flux path.

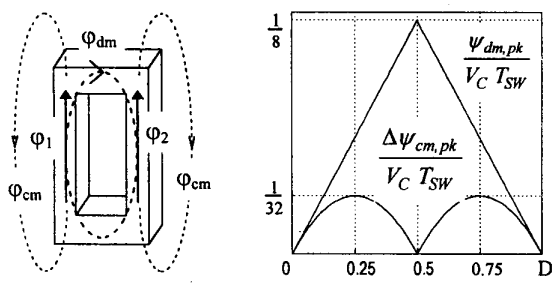

Fig. 4 T+L common- and differential-mode fluxes; their ripple peak values as a function of common mode index (M_{cm}≡D).

$$\Delta\psi_{cm,pk} = \begin{cases} \frac{T_{SW}V_c}{4} D(1-2D) & @D < \frac{1}{2} \\ \frac{T_{SW}V_c}{4}(1-D)(2D-1) & @D > \frac{1}{2} \end{cases} \quad (11)$$

$$\Delta\psi_{dm,pk} = \begin{cases} \frac{T_{SW}V_c}{4} D & @D < \frac{1}{2} \\ \frac{T_{SW}V_c}{4}(1-D) & @D > \frac{1}{2} \end{cases} \quad (12)$$

III. Convertor Loss Analysis and Model.

The detailed expression of convertor's power losses is:

$$P_{tot,conv} = P_{Cin} + P_C + P_{T+L} + P_{HB} + P_{aux} \quad (13)$$

1) P_{Cin} and P_C (input and output capacitors losses) are depending on their ESR, respectively R_{Cin} and R_C:

$$P_{Cin} = R_{Cin} \cdot \left(I_{Cin,rms}\right)^2 \quad \text{[refer to (7)]} \quad (14)$$

$$P_C = R_C \cdot \left(I_{C,rms}\right)^2 \quad \text{[refer to (8)]} \quad (15)$$

2) P_{T+L} (integrated transformer + inductor losses) must be modeled by copper and ferrite losses:

$$P_{T+L} = P_{Cu} + P_{Ferr} \quad (16)$$

The first term in (16) is expressed to depend on common-mode resistance R_{cm} (equal to "phase" resistance R_{ph}), by splitting the DC ad PWM contributions due to consistent impact of skin effects:

$$P_{Cu} = \frac{R_{cm}|_{DC}}{2} \cdot I_L^2 + \frac{R_{cm}|_{PWM}}{2} \left(I_{Cin,rms}\right)^2 \quad (17)$$

Ferrite core losses are very low, however an accurate model (18) has been tested for the purpose, where k_{ferr} factor encloses ferrite properties, core mass and section.

$$P_{ferr} \cong k_{ferr} \cdot \frac{\left(\psi_{cm} + \psi_{dm}\right)_{pk}^{2.19}}{T_{SW}^{1.39}} \quad (18)$$

3) P_{HB} (total H-bridge IGBT and free-wheeling diode losses) is composed by conduction and switching losses. Conduction losses are generally depending on duty-cycle, however this is cancelled by identical ON voltage drops on IGBTs and diodes thanks to peculiar alternative operation [1]. The best match with test-bench measurements is achieved by "averaging" the two drop functions, as in (19), providing a very accurate conduction loss model (20):

$$\frac{v_{CE,sat}(I) + v_{diode,forward}(I)}{2} \cong V_J + \Delta V_R \frac{I}{I_{label}} \quad (19)$$

$$P_{cond,HB} = 2 \cdot \left[V_J + \frac{\Delta V_R}{I_{label,HB}} \left|\frac{I_L}{2}\right| \cdot \left(1 + \frac{a_{SW}^2}{3}\right) \right] \cdot \left|\frac{I_L}{2}\right| \quad (20)$$

Switching losses are quite complex. According to factory specifications, (21) is a simple while effective model, being Δt_{comm} a switching time "constant" (temperature depending).

$$P_{sw,HB} \cong 2 \cdot \left\{ \frac{V_c}{T_{SW}} \cdot \frac{|I_L|}{2} \cdot \Delta t_{comm} \right\} \quad (21)$$

4) P_{aux} includes control board and auxiliaries power loss, and it's fairly constant (~27W). All the inherent devices are supplied from V_c by a small DC/DC converter.

IV. Test Bench Concept and Design.

A. Power loss dependence on input current.

According to previous equations (11 to 19), if V_c and D are constant values, converter's power losses do not depend on input current sign, but only on its module. This is the theoretical basis for the adopted test method.

B. Basic concept of operation.

The alternative operation at constant input voltage and current module and set output voltage is provided by a proportional-integrative voltage regulator. Its output is PW modulated to generate a variable duty rectangular wave, whose (constant) module is representing the current reference for power loss evaluation. The rectangular reference period is short to limit the i/o capacitor banks voltage ripples, while it has to be very large with respect to current loop time response (~200μs), in order to fairly disregard the effect of current inversion transients (and related "error" of input current with respect to the reference constant value). The suitable rectangular reference frequency is set to 65Hz, low enough also to minimize skin effects (extra losses) of such a rectangular-wave operating cycle.

C. Basic test-bench composition.

The proposed test bench is depicted in Fig.5, basically comprising the converter under test and a pair of outer large capacitor banks (input and output sides of the converter). Designed capacitance values are large enough to keep D as constant as practical (ΔD<8%) during the alternating 65Hz operation, holding validity of the power loss analytical models described in section III.

The two high-frequency filter inductances (L_{if} and L_{of} in series with i/o capacitor banks in fig.5), are disposed not to affect the inner capacitor ripples at switching frequency (PWM current ripples either on i_{Cin} or i_C). By this way, during the tests, i_{Cin} and i_C ESR losses are equivalent to ordinary steady-state DC/DC operating conditions.

The input voltage (*Supply stage* in Fig.5) is obtained by a small power voltage generator, followed by suitable CL filter (32mH-5mF) to counteract with input voltage ripple effects.

D. I/O capacitor banks and filters.

Each bank is constituted by smaller groups, adopting short, large section wires (16 ÷ 75 mm^2) to minimize any additional resistance. In addition, due to large data-sheet tolerances both on capacitance and ESR values, these ones have been measured by an AC 50Hz volt-amperometric test with 50V DC bias (useful to 65Hz validation). Calculated capacitance and ESR values are 66.6[mF], 3.6[mΩ] for input bank, and 40.4[mF], 6.3[mΩ] for output bank. The respective measured values are: 71.5[mF], 3.9[mΩ] at input; 44.0[mF], 5.5[mΩ] at output.

According to basic principle, inner capacitor currents (i_{Cin} and i_C in fig.5) should contain only high frequency components (PWM modulation ripples), leaving to outer capacitor banks (i_{CiB} and i_{CoB} in fig.5) the low frequency ones (65Hz). This is made practically possible for loss estimation by the two filter inductors (L_{if} and L_{of} in fig.5), reducing the 20kHz currents flow towards outer capacitor banks, without rising the banks impedance up at 65Hz harmonics. Some oscillations are anyway arising in response to power inversions as shown in the followings.

E. Power losses estimation.

Total test bench power loss, at set working point, comes from DC power supply stage measurement:

$$P_{SS} = V_{in} \times I_{SS} \tag{22}$$

where both factors are directly measured by real mean value voltmeters (I_{SS} is measured through R_{shunt} shown in fig.5). Obviously, effects and losses of the extra i/o large capacitor banks should be carefully evaluated.

Measured power (22) is composed as in (25):

$$P_{SS} = P_{conv} + P_{CiB} + P_{CoB} \tag{25}$$

where:

$$P_{CiB} = R_{CiB} \cdot I^2_{CiB,rms} \tag{26}$$

$$P_{CoB} = R_{CiB} \cdot I^2_{CoB,rms} \tag{27}$$

As assumed, I_{CiB} is a 65Hz rectangular shaped current with constant module:

$$I_{CiB,rms} \cong |I_L| \tag{29}$$

Considering a constant i/o voltage ratio, during the test at a set working point, output capacitor bank rms current is very close to (30):

$$I_{CoB,rms} \cong |I_L| \cdot \frac{V_{in}}{V_c} \tag{30}$$

Finally, quasi-direct measurement of convertor's losses is:

$$P_{conv} = P_{SS} - I_L^2 \cdot \left[R_{CiB} + \left(\frac{V_{in}}{V_c} \right)^2 \cdot R_{CoB} \right] \tag{31}$$

where the "error" term is as low as practical by design.

V. Experimental Results

A series of efficiency tests has been carried out, covering the whole V_{in}/V_c ratio operative range according to TBL.II. By constant V_c values (300V and 400V), two different constant-power tests (15-30kW) are provided. A further test, at rated power, refers to low constant input voltage (V_{in}=150V, $|I_L|$=100A) and variable output voltage.

TABLE II - Definition of Efficiency Test Conditions.

	Test group	P [kW]	V_{IN} [V]	V_c [V]	$\|I_L\|$ [A]
1	CONSTANT V_C	15 30	150÷300	400	50÷100 100÷200
2	CONSTANT V_C	15 30	150÷260	300	50÷100 100÷200
3	CONSTANT V_{in}	15	150	170÷400	100

A. Converted current waveform.

According to basical assessment, the converted input current is as close as possible to a rectangular wave. In Figs.6,7 the measured currents behavior is shown. Input and output capacitor banks currents are ripple-free while oscillating at every step. This is due to designed inductors filtering effects (L_{if} and L_{of} in Fig.5) oscillating with inner capacitors (C_{in} and C in Fig.5). In Fig.7 the quick response (~200μs) to one of the 65Hz alternated steps is evidenced.

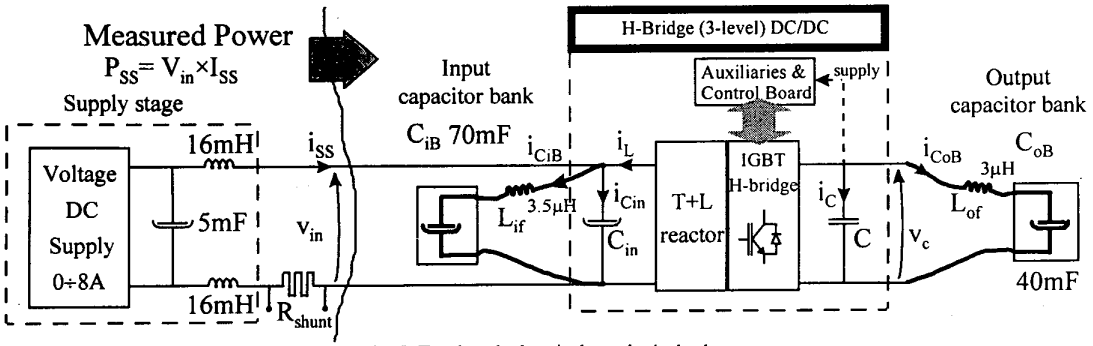

Fig. 5 Test bench electrical-topological scheme.

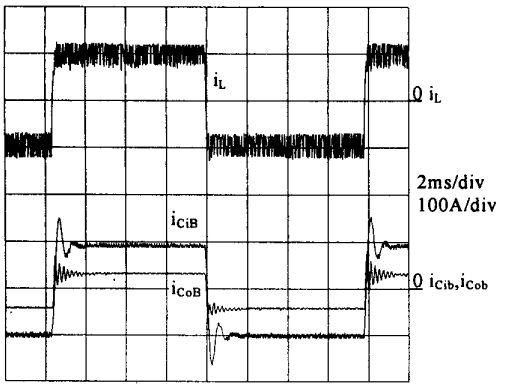

Fig. 6 Input converted current and i/o capacitor banks currents alternated behavior @ 65Hz operation; V_{in}=150V, V_c=400, $|I_L|$=100A.

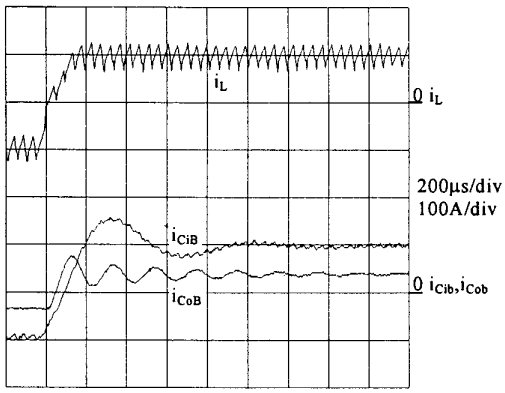

Fig. 7 Input converted current and i/o capacitor banks currents: responses to an inversion transient; V_{in}=150V, V_c=400, $|I_L|$=100A.

B. Measured losses. Mathematical model validation.

TABLE III - SUMMARY OF LOSSES MODEL PARAMETERS

	f_{sw}		[kHz]	10.124
IPM (I_{label}=200A)	V_j	$\vartheta_j \cong 75°C$	[V]	0.9
	ΔV_R		[V]	1.4
	Δt_{comm}		[ns]	260
T+L reactor	L_{ll}		[µH]	38
	$R_{cm\|DC}$		[mΩ]	5.0
	$R_{cm\|PWM}/R_{cm\|DC}$			13.5
	k_{ferr}		$[W \cdot s^{1.39} mWb^{-2.29}]$	40.8
Inner capacitors	R_{Cin}		[mΩ]	25.0
	R_C		[mΩ]	2.2
Outer capacitors	R_{CiB}		[mΩ]	3.9
	R_{CoB}		[mΩ]	5.5
Auxiliaries	P_{aux}		[W]	27

Referring to parameter values reported in TBL.III, the comparison between total measured and estimated losses is here reported. Figs.8,9 report the constant output voltage tests (V_c=300V and 400V), while Fig.10 reports the constant input voltage test (V_{in}=150V). All the reported plots refer to net measured losses, by 10 seconds operation at each working point, trying to operate IGBTs and diodes @75°C, by varying the initial heatsink temperature inversely with power. The reported power values come from the difference between P_{SS} (22) and measured auxiliaries term P_{aux} (=27W).

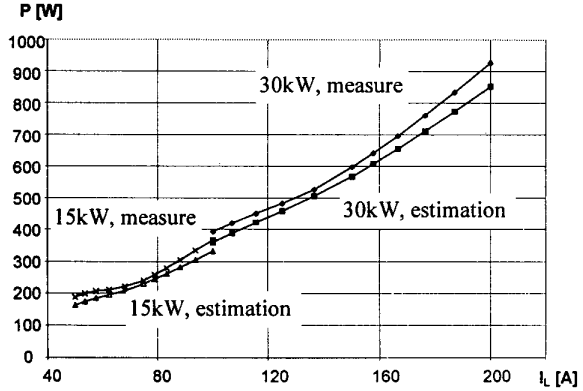

Fig.8 Estimated and measured net power losses comparison @V_c=400V

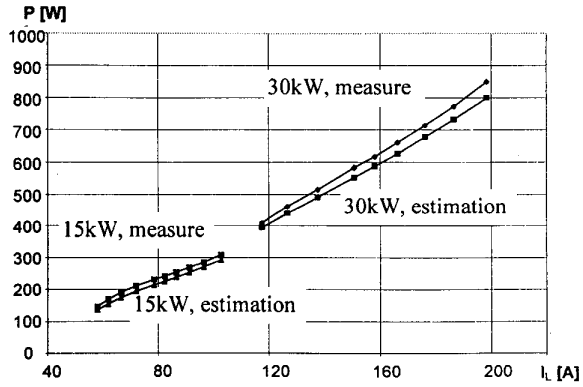

Fig.9 Estimated and measured net power losses comparison @V_c=300V

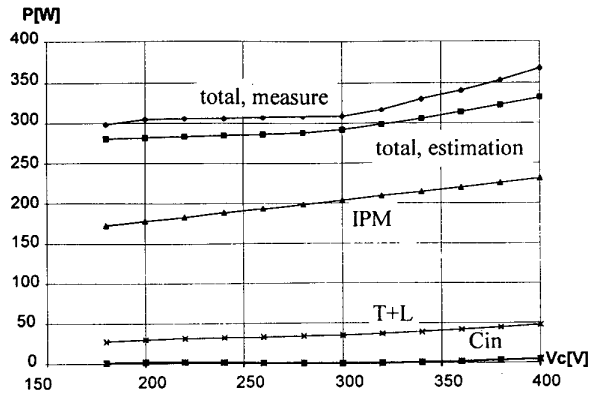

Fig.10 Measured and estimated power loss comparison and main inner estimated terms (P_C fairly null) @V_{in}=150V,$|I_L|$=100A.

The graphical comparison between Figs.8,9,10, shows a general underestimation trend of the losses model. The maximum absolute difference between model and measure is ~75W (on >900W measured losses @V_c=400V, V_{in}=150V, I_L=150A, Fig.8), while the relative estimation error is always under 10%. A first point of difference is evidenced by Figs.8,9, in which the difference between curve pairs generally grows up with converted input current module quite quadratically. This is a "resistive-equivalent" effect, due to an underestimation of rms current terms of loss (partially related to 65Hz skin effects). As a second point, a duty-cycle dependent discontinuous term of error is evidenced by Figs.8,10, with a minimum corresponding to D=1/2. The error shape is someway linked to common-mode flux ripple amplitude (11), reported as a function of D in Fig.4 (corresponding to underestimation of PWM skin effects). The comparison between Figs.8 and 9, clearly shows a general growth of the underestimation with V_c (300V in Fig.9, 400V in Fig.8) at set D value. This, accordingly to (11), would be a confirmation of the estimation error related to flux-ripple.

D. Model refinement.

Looking back to loss terms neglected in par.III analysis, other two terms depending on current-module can be found. The first term is due to the damping of the oscillating behavior evidenced by Figs.6,7 (estimated losses ~25W @ $|I_L|$=200A). A second analogous term refers to a further contribution to switching losses, due to stray commutation inductance on the dc-link connection between "C" and the IPM. Suitable small 100nF capacitor is locally mounted on IPM, resulting on 1.4MHz oscillations and estimated 130nH stray inductances. From measured transient overshoot value (~80% of switched current), the related loss term is ~20W @ $|I_L|$=200A. In both cases, these power losses are function of $|I_L|^2$, proportional to stored inductive energies.

Differing from previous terms, the effective common-mode ripple resistance, as defined by (17), should be upgraded with respect to TBL.III calculation @20kHz.

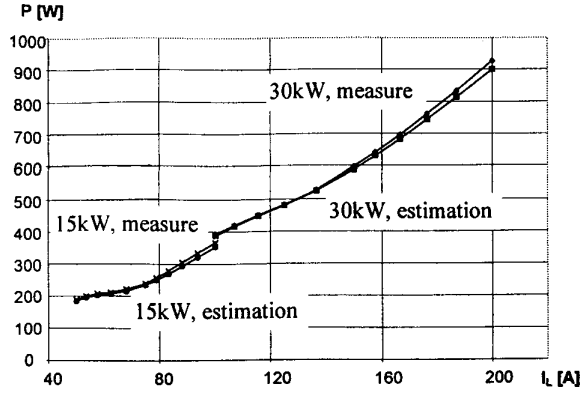

Fig.11 Estimated and measured net power losses comparison with estimation corrective terms @V_c=400V

Furthermore, common-mode flux path in air and related eddy currents on all conductors, heatsink and convertor's box should be also estimated. These losses can be equivalently estimated by increasing the skin effect on the windings.

By adding these three terms, Fig.11 shows the comparison analogously to Fig.8. The model accuracy, still slightly defecting, has become practically perfect. The added terms refer to:

- two terms in the form $K \cdot I_L^2$, due to inductive oscillating losses, where K factors suitably summarize inductance values, current steps and overshoots, respective frequency;
- 3 times the common-mode PWM resistance reported in TBL.III.

The maximum estimation error is then reduced to ~25W (on 900W measured losses).

E. Convertor's losses summary.

In all the effected tests, measured power losses are fairly under 1kW level. By subtracting from measured losses outer capacitor banks contributions, both ESR losses [P_{CiB} and P_{CoB} defined by (26),(27)] and KI_L^2 term due to filter inductances, an exact estimation of power convertor's losses is given. TBL.IV reports net convertor's efficiency, referring to rated and overload converted power (15,30kW @V_c=400V).

TABLE IV - NET CONVERTOR'S EFFICIENCY @V_c=400V

Converted Power [kW]	$\|I_L\|$ [A]	Net Power Losses [W]	η
15	50÷100	170÷315	0979÷0.989
30	100÷200	266÷654	0978÷0.991

VI. CONCLUSIONS.

The efficiency of a novel DC-DC three-level boost power converter has been investigated, already designed to adapt the battery voltage to PWM VSI in EV AC motor drives.

Due to very high efficiency, a new measurement method has been proposed, based on suitable alternating power flow between outer large capacitor banks.

An accurate analysis of power loss terms and model has been presented, in order to validate either the proposed measurement or the novel DC/DC convertor loss model.

The obtained results are completely satisfactory, demonstrating at the same time the very high efficiency of the novel DC-DC three-level boost converter, the accuracy of the power loss model and the effectiveness of the proposed measurement method.

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