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Digital Instrumentation for the Measurement of High Spectral Purity Signals

By

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Declaration

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2017

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I would like to dedicate this thesis to my loving family

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Abstract

Improvements on electronic technology in recent years have allowed the application of digital techniques in time and frequency metrology where low noise and high accuracy are required, yielding flexibility in systems implementation and setup. This results in measurement systems with extended capabilities, additional functionalities and ease of use.

The Analog to Digital Converters (ADCs) and Digital to Analog Converters (DACs), as the system front-end, set the ultimate performance of the system in terms of noise and their noise characterization will allow performing punctual considerations for the implementation or for the application of an efficient noise rejection technique. Moreover, most commercial platforms based on FPGA are clocked by quartz oscillators whose accuracy and frequency stability are not suitable for many time and frequency applications. In this case, it is possible to take advantage of the internal Phase Locked Loop (PLL) for generating the internal clock from an external frequency reference. However, the PLL phase noise could degrade the oscillator stability thereby limiting the entire system performance becoming a critical component for digital instrumentation. The information available currently in literature, describes in depth the features of these devices at frequency offsets far from the carrier. However, the information close to the carrier is a more important concern for time and frequency applications.

In this frame, my PhD work is focused on understanding the limitations of the critical blocks of digital instrumentation for time and frequency metrology. The aim is to characterize the noise introduced by these blocks and in this manner to be able to predict their effects on a specific application. This is done by modeling the noise introduced by each component and by describing them in terms of general and technical parameters. The parameters of the

models are identified and extracted through the corresponding method proposed accordingly to the component. This work was validated by characterizing a commercially available platform, Red Pitaya. This platform is an open source embedded system whose resolution and speed (14 bit, 125 MSps) are reasonably close to the state of the art of ADCs and DACs (16 bit, 350 MSps or 14 bit, 1 GSps/3GSps) and it is potentially sufficient for the implementation of a complete instrument. The characterization results lead to the noise limitations of the platform and give a guideline for instrumentation design techniques.

Based on the results obtained from the noise characterization, the implementation of a digital instrument for frequency transfer using fiber link was performed on the Red Pitaya platform. In this project, a digital implementation for the detection and compensation of the phase noise induced by the fiber is proposed. The beat note, representing the fiber length variations, is acquired directly with a high speed ADC followed by a fully digital phase detector. Based on the characterization results, it was expected a limitation in the phase noise measurement given by the PLL. First measurements of this implementation were performed using the 150 km-long buried fibers, placed in the same cables between INRiM and the Laboratoire Souterrain de Modane (LSM) on the Italy-France border. The two fibers are joined together at LSM to obtain a 300 km loop with both ends at INRiM. From these results the noise introduced by the digital system was verified in agreement with characterization results. Further test and improvements will be performed for having a finished system which is intended to be used on the Italian Link for Frequency and Time from Turin to Florence that is 642-km long and to its extension in the rest of Italy that is foreseen in the next future.

Currently, a higher performance platform is under assessment by applying the tools and concepts developed along the PhD. The purpose of this project is the implementation of a state of the art phasemeter whose architecture is based on the DAC. In order to estimate the ultimate performance of the instrument, the DAC characterization is under development and preliminary measurements are reported.

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Nomenclature

Roman Symbols

$\hat{v}_k$	ADC output - Digital value
$\mathsf{x}(t)$	Time noise. For the case of the ADC it is defined as the aperture jitter
x_k	Discrete-time random processes resulting from sampling $\mathsf{x}(t)$ at $t = kT_s$
$\tilde{v}_k$	ADC output referred to the input.
k	k-th sample
m	ADC resolution – nominal value
$n(t)$	Additive noise of input stage circuit
n_k	Discrete-time random processes resulting from sampling $n(t)$ at $t = kT_s$
n_q	Quantization noise
n_α	In-phase noise component of the ADC input stage
n_φ	Quadrature noise component of the ADC input stage
$r(t)$	Relative noise of the ADC voltage reference
r_k	Discrete-time random processes resulting from sampling $r(t)$ at $t = kT_s$
T_s	Sampling period
v_k''	Output of the sample and hold, k-th sample
$v'(t)$	Output of the input stage circuit

$v(t)$ ADC input signal

V_0 Input signal peak value

V_r ADC voltage reference

V_{r_0} Nominal value of the ADC voltage reference

Greek Symbols

α_k Total ADC amplitude noise. Normalized amplitude fluctuations. Non-dimensional

ν_0 Input signal carrier frequency

π $\simeq 3.1416\ldots$

$\varphi_\times$ Phase noise generated by the ADC aperture jitter

φ_k Total ADC phase noise in [radians]

Chapter 1

Introduction

1.1 High Spectral Purity Signals and Time and Frequency Metrology

Measuring time has been an important concern from ancient ages for different reasons like organizing daily activities, cultural events and even more complex such as navigation, travel schedules and communication networks. This necessity has required the development of incredible systems for measuring and keeping time [1, 2]. Only until some decades, the second was defined as one in 86400 parts of the day, assuming the length of the day constant and defined by astronomical observations of the Sun, the Moon, the Earth and other planets. However, due to the Earth's movement irregularities, the length of the day varies over the year, increasing the complexity of systems for reliable timekeeping and therefore for time interval measurements. Furthermore, due to the need of defining a standard unit for time that could be built everywhere, other approaches not based on astronomical observations for keeping time were proposed.

In general, for keeping time or for setting the time of a system, a high performance oscillator is required, that means, a repetitive action whose period remains constant over time. The performance of an oscillator is then determined through two features: the accuracy and the stability. The accuracy indicates

the deviation between the ideal frequency and the actual value, while the stability gives information about how much the frequency varies over time.

The first approach capable of keeping time with remarkable stability was the pendulum clock built by Christian Huygens (1656) which reached an error of around 10 seconds a day (10^{-4}). The oscillator was a pendulum whose period was determined by the length of the rod. Although this device could be easily reproduced, it was highly sensitive to length variations of the rod due to temperature and other environmental factors. Additionally, the pendulum movement was affected by friction. The highest stability of a clock of this kind was the one proposed by William Hamilton Shortt (1921) which was composed of two pendulums, the master and the slave. With this configuration the master was a free pendulum isolated in a vacuum chamber reaching a stability of 1 second a year or one part in 30 million (3×10^{-8}) [1, 3]. It was used as primary standard for time dissemination services and as time reference for detecting the irregularities of the Earth's rotation over seasons (1926).

Another approach for timekeeping is based on the quartz crystal oscillator that displaced the later mechanical clock due to the higher frequency stability achieved. The principle of operation relies on the piezoelectric property of this crystal, discovered and studied by Jacques and Pierre Curie around 1880 [4]. The first contributions for the design and the usage of quartz crystal as an oscillator were done by Walter G. Cady (1921) [5]. This approach was adopted soon as time and frequency standard (1930) reaching a stability of 1 second in 30 years or one part in one billion (10^{-9}) for the crystal clock developed by Warren A. Marrison (1930). However, these clocks are highly sensitive to temperature which degrades its long term stability. Besides, the frequency value depends on the shape and the size of the crystal; therefore there are no two identical crystal oscillators. For these reasons they were replaced, as frequency standards, by a more stable and reproducible approaches: atomic clocks. In spite of that, they are still widely used in electronic applications requiring short term stability and not concerned with long term stability, such as digital signal processing, radars, sensors, communications, navigation, guidance systems, etc., due to the good compromise between quality and price, and because it is the most compact solution, currently, available in the market. Moreover, quartz oscillators are usually used for backing up atomic clocks thereby taking

advantage of the high short term stability of quartz and the excellent long term stability of atomic resonance [6].

Since 1967 the second is defined as 9,192,631,770 periods of the cesium atom's resonant frequency [1, 2] making time (and its reciprocal, frequency) the most accurately measured physical quantity. Therefore, many applications and the definition of other physical quantities rely on time or are referred to a timebase. The principle of atomic clocks is based on the fact that atoms absorb and emit the same amount of energy when they change from one level of energy to another and when they move back. The resonance frequency is proportional to the difference between the two levels of energy and its value is the same for all atoms of the same element [7], feature that makes these kind of oscillators easily reproduced. Usually, they work frequency-locking an external oscillator, generally quartz, in order to improve their quality factor (Q). Atomic clocks are used as primary standards (cesium beam, cesium fountain and cesium optically pump) and as secondary clocks (industrial cesium clock, hydrogen maser and rubidium clock) in National Metrology Institutes, and as local oscillators in applications where high stability is required. Generally, these clocks have a stability of around one second in 100 million years equivalent to 3 parts in 10^{16} (3×10^{-16}) [8], but it depends on the implementation and topology.

An even more stable approach is already available using optical frequencies (1990s). The principle of operation of these clocks is based on the vibration of ions or atoms at optical frequencies rather than at microwaves, thereby increasing the clock accuracy since time is divided in smaller pieces [9]. The actual implementation of these clocks has been possible thanks to the optical comb [10] that acts as a ruler in order to link optical frequencies to microwaves making them compatible with available electronics. The stability that can be reached with these clocks is around one second in 5 billion years equivalent to 6 parts in 10^{18} (6.4×10^{-18}) [11]. This tremendous stability is exploited specially in fundamental physics for instance in the redefinition of constants and the study of quantum phenomena. Different topologies have been implemented depending on the atoms or ions used [12–14]. Due to its high stability, Ytterbium optical clock is one of the candidates for the redefinition of the second [15].

Currently, these high spectral purity signals are used in innumerable applications such as calibration in National Metrology Institutes, time dissemination,

frequency transfer, geodesy, Global Positioning Services (GPS), communication networks, instrumentation, space applications, Very Long Baseline Interferometry (VLBI), etc. Depending on the application requirements, it may be limited by the oscillator stability or by the system performance.

For instance: in digital communication systems, in particular when the most efficient encoding method is used which is imprinting the information on the phase of the carrier also known as N-PSK and coherent demodulation is applied for reducing the bit error (BER), the phase noise of the local oscillator generates coherence loss and interchannel interference causing cross-coupling, when N $>$ 2 [16]. Though a margin of error can be fixed for increasing the tolerance to noise effects in the receiver, the impact of the local oscillator phase noise depends on the application and on the demodulation technique implemented, increasing proportionally with N. Hence, phase noise measurements of the local oscillator may be desired in order to assess its suitability according to the application.

On the other hand, applications of time and frequency transfer include remote comparison of ultra-stable oscillators for calibration purposes. In this regard, the system used for performing the frequency transfer must feature a stability that minimizes the added noise and thereby avoids degrading the signal being transmitted. Currently, techniques based on fiber links are considered the most performing tools for frequency transfer because they allow delivering optical frequencies with a stability of the order of 10^{-18} over hundreds of kilometers [17]. However, length variations due to environmental factors add noise which should be detected in order to guarantee such stability especially in longer fiber links.

But how to determine the stability of a signal?

A real oscillator is affected by phase and amplitude noise generated by environmental factors and the intrinsic noise of the oscillator itself. Considering an ideal oscillator as $v(t) = V_0 \cos(2\pi\nu_0 t)$, the real oscillator signal is described by $v(t) = V_0(1 + \alpha(t)) \cos(2\pi\nu_0 t + \varphi(t))$, where $\varphi(t)$ and $\alpha(t)$ represent the phase and normalized amplitude noise present in the signal as it is sketched in Fig. 1.1. In high spectral purity signals, the phase and amplitude noise are small, that is, $|\varphi(t)| \ll 1$ and $|\alpha(t)| \ll 1$.

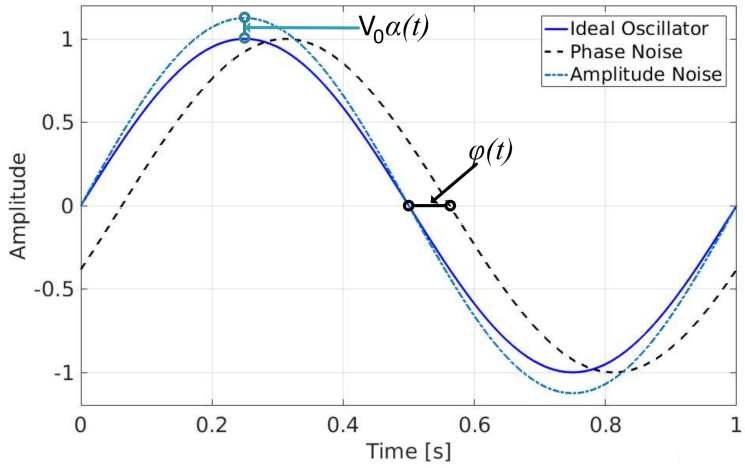


Fig. 1.1 Phase and amplitude noise in a real oscillator.

The stability of an oscillator is related to its amplitude, phase and consequently to its frequency fluctuations, considering that the frequency is the derivative of the phase. Hence, the accuracy and stability of an oscillator are obtained from the analysis of the amplitude, phase and frequency fluctuations [18].

Different techniques have been developed for phase and amplitude noise measurements. While traditional schemes are based on analog implementations, the increasing technological advances on electronic circuits have allowed the application of digital systems in recent techniques.

1.2 Comparison between Digital Instrumentation and Analog Schemes

In principle, an oscillator phase noise is measured by comparing or referring it to a more stable oscillator. The traditional method (analog implementation), sketched in Fig. 1.2, is based on the mixer operation [19]. The mixer works as a phase detector if the Device Under Test (DUT) and the Reference (REF) are in phase quadrature, that is with 90° of phase shift [20]. In order to guarantee and keep this condition the phase of the REF is controlled through a Phase Locked Loop (PLL).

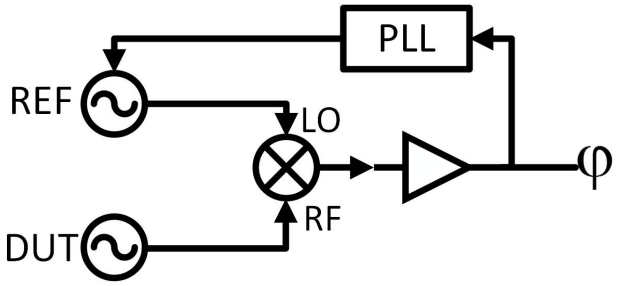


Fig. 1.2 Traditional method for phase noise measurement. Analog implementation.

This technique is highly limited by the REF noise, then whether a high stable DUT is intended to be measured a higher quality REF is required. In order to overcome this limitation the technique with two mixers and cross-spectrum was proposed [21, 22]. By using this approach, depicted in Fig.1.3, the uncorrelated noise, in this case the REF noise, is canceled by means of the cross-spectrum [23] thereby obtaining only the noise contribution of the DUT and therefore making the instrument less sensitive to the REF stability. The cross-spectrum is calculated through a Fast Fourier Transform (FFT) Spectrum Analyzer, that already implied a not fully analog implementation.

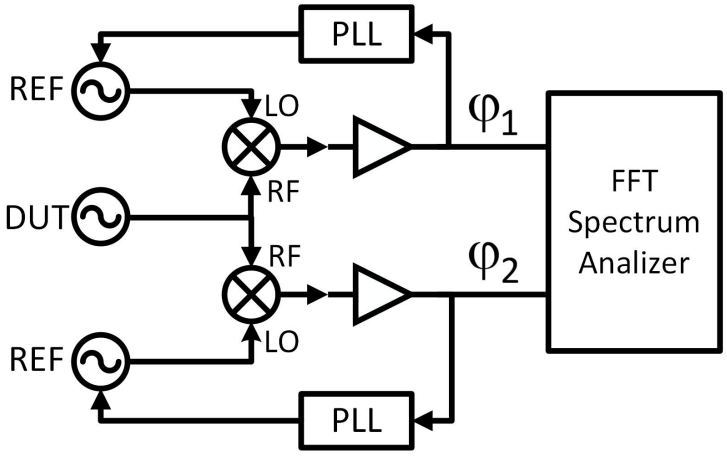


Fig. 1.3 Traditional method for phase noise measurement. Analog implementation plus cross-spectrum.

This method requires two oscillators at the same frequency of the oscillator under test, restricting the instrument operation range. Moreover, changing the DUT frequency implies to change the system configuration, and therefore

hardware modifications, because of the low flexibility of the analog implementation. Since the mixer works in saturated mode it suffers of non-linearity and it is also highly sensitive to impedance mismatch and power losses. Then, calibration and tuning procedures should be performed in order to guarantee the proper operation of this device. A similar scheme is proposed for amplitude noise metrology, but in this case the DUT and the REF should be in phase instead of quadrature [22]. Even if the same hardware is used for both measurements (PM/AM) additional calibration procedures are required for keeping the required phase conditions.

Recent studies have demonstrated that this scheme suffers from artifacts and errors [24, 25] that could generate underestimation on the measured phase noise.

In general, analog systems are highly sensitive to environmental conditions. Although low noise components are currently available on the market, the external connections between them are also dependent on temperature, humidity, mechanical noise, etc. Thinking on solving these issues, thereby improving the systems performance stability, digital approaches started to be proposed in different fields. The revolution of transistors and its stability regarding temperature and other environmental factors, made possible the development of digital machines for space and military applications where high stability in systems performance is required [26]. Software Define Radio (SDR) technique [27], proposed initially for communication applications, presents the structure for an ideal digital system (Fig. 1.4) based on three main blocks: an Analog to Digital Converter (ADC), the digital signal processing system and an eventual Digital to Analog Converter (DAC), if it is required for feeding further analog blocks.

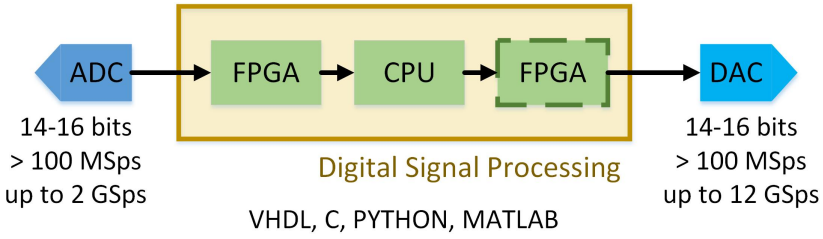


Fig. 1.4 Structure of a general purpose fully digital implementation.

In order to make feasible the implementation of this system, high speed and high resolution ADCs are required. The speed guarantees enough acquisition bandwidth which avoids loosing input information, while the resolution determines the accuracy of the digital representation of the analog signal. The first commercially available ADC (1954) was a vacuum-tube based of 11-bits and 50 kilo-Samples per second (kSps) [28]. The need of increasing the acquisition speed for communication, medical, radar, video and other applications, encouraged the development of ADCs with different architectures and features. Currently, ADCs and DACs of high resolution ($>$ 12 bits) and high speed ($>$ 100 MSps) are available on the market. However, high speed and high resolution acquisitions mean high data rates and therefore a fast and efficient digital data processing system is also needed. Developments over the last decades in electronic circuits, processors, embedded systems and programmable logic devices have produced a wide range of devices for digital processing such as processors with different architectures, Field Programmable Gate Arrays (FPGAs) and most recently, the System on Chip (SoC), that includes a processor and a FPGA embedded in the same chip.

Hence, thanks to all of these developments, the actual implementation of the ideal architecture stated by SDR is feasible for time and frequency applications and recently, new methods for phase and amplitude noise metrology have been proposed based on digital systems [29–36]. One of the most widely used approaches is the IQ demodulation technique (Fig. 1.5). The mixer is replaced by a numerical multiplication between the signal acquired through an ADC and a Numerically Controlled Oscillator (NCO) able of synthesizing arbitrary frequencies.

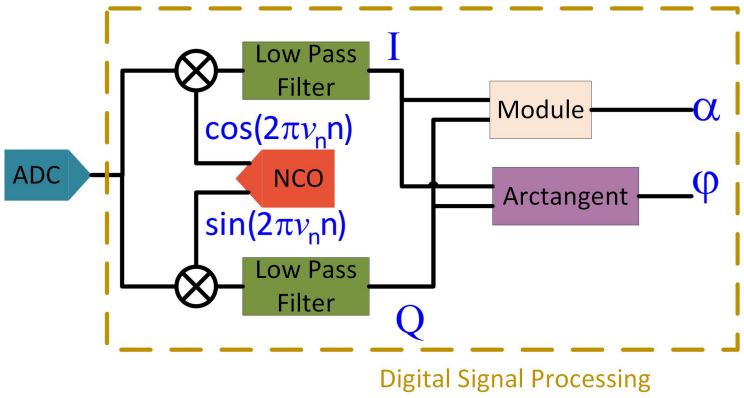


Fig. 1.5 Digital implementation for phase and amplitude noise measurement.

By generating the sine and cosine at the same frequency of the input signal, the in-phase (I) and quadrature (Q) components are obtained after filtering the high frequency components resulting from the multiplication. With this information, the phase and the magnitude of the input signal are extracted through the computation of the arc-tangent and the module, respectively.

$$\alpha(t) = \sqrt{I^2 + Q^2} \qquad \varphi(t) = \arctan\left(\frac{Q}{I}\right) \tag{1.1}$$

The data obtained can be sent to an external computer for post-processing or monitoring, or can be connected to further analog hardware through a DAC.

Hence, by replacing analog implementations with digital instrumentation some advantages are obtained: reduction of the analog components and therefore their contributions such as mechanical noise, temperature dependence, drift, aging and tuning. Digital implementations are more stable in terms of performance, once the code or configuration algorithm (FPGA) is working it will work in the same way over time. They are reconfigurable and flexible: modifications can be performed only by changing the algorithms either for the processor (CPU) or for the FPGA configuration, and no additional hardware modifications are required. This is advantageous specially for testing new approaches and techniques. Additionally, the systems can be easily reproduced and tuned just by changing parameters (gains, filter coefficients, data resolution, etc.).

However, replacing analog systems with digital implementations introduces some challenges as well, like discrete time (limited observation bandwidth), quantization, aliasing, proper representation of the sample (integer, fixed point, floating point) in order not to corrupt or not to lose information. Moreover, the ADCs and DACs, being the interfaces with analog signals, set the ultimate performance of the system in terms of noise. Although techniques of common noise rejection or cross-correlation can be applied for reaching a system stability beyond the limitation set by these components, their noise characterization may bring tools for the implementation of efficient rejection techniques. Hence, a proper understanding of these limitations could get them into opportunities for the development of new techniques and for an efficient system operation.

1.3 Importance of Noise Characterization of Digital Systems and State of the Art

In general, determining the noise of the critical components of a system provides key information for predicting undesired behavior in an application. The noise characterization results bring useful information related to the implementation feasibility of new techniques and for the selection of proper components according to the application requirements.

In this regard, different techniques have been developed for characterizing the noise of ADCs and DACs.

For the case of ADCs, while the histogram approach has been widely used for measuring static errors [37, 38], one group [39] proposed a method for estimating the voltage error generated by the aperture jitter plus the internal additive noise through the locked histogram technique, performing synchronous sampling. The distribution function of the noise, assumed normal, was obtained by modifying the mean of the input sine-wave by adjusting an offset as finely as one least significant bit (LSB) of the ADC under test, being a suitable approach for ADCs of low/medium resolution (maximum 10 bits). Several groups have studied the jitter of ADCs. The work presented in [40] proposed a model and a method based on SNR analysis in order to evaluate and discriminate the effects of the jitter components on the ADC performance, thereby giving a guideline

to compensate for such effects in future high-speed ADC designs. On the other hand, the authors of the work reported in [41] proposed a sampling jitter model with the purpose of discriminating the contributions from the clock interface and the sampling circuit. Such a model was validated through an experimental setup based on the analysis of different clock signal slopes (square signal and sine wave). A characterization technique based on the use of a Graychip and down-conversion was performed [29] for evaluating the viability and strategies of the direct-digital technique implementation for phase noise measurements. Characterization of high resolution, low speed ADCs ($\geq$20 bit, $\leq$5 MHz) have been performed [42] using a Programmable Josephson Voltage Standard. Recent results of high-resolution and high-speed ADCs noise characterization were obtained through a full digital approach based on common noise cancellation and digital down-conversion [43]. The power spectra density of ADCs phase noise is estimated after proper filtering and decimation stages.

Depending on the application, the digital system performance can be limited by the DAC rather than by the ADC. Therefore, the noise characterization of this component may provide important information for instrumentation design techniques. Although DACs perform a complementary function with respect to ADCs, their noise characterization has not been as extensive as their counterparts and the methods proposed are highly dependent on the DAC architecture. For current-steering DACs, the delay difference between the current sources generate noise that degrade the DAC performance. In this regard, the work presented in [44] proposed a mathematical model for the assessment and simulation of such effect on the Spurious Free Dynamic Range (SFDR). Additionally, the model was validated through experimental measurements. Another group [45] studied the effect of the noise introduced by the sampling clock on the Signal to Noise Ratio (SNR). It was done through simulations based on a model of the error output power. A characterization technique based on Least Square Estimation for the simulation of DACs linearity and speed was proposed [46]. This technique was implemented using Matlab and Spice, and it was applied for the evaluation of a binary-weighted 8-bit DAC. A method for DACs characterization using pulse signals was proposed [47] with the purpose of selecting the proper component for the implementation of a signal generator for Wireless Frequency Division Multiplexing. Analysis through

simulation of noise shaping on sigma-delta DACs have also performed [48, 49] in order to minimize information loss.

On the other hand, for some applications it is also important to refer the system timebase and the DUT to a common REF. Most commercial platforms based on FPGA are clocked by quartz oscillators whose accuracy and frequency stability are not suitable for many time and frequency applications being at the level of $10^{-10} - 10^{-9}$ in the short term, $10^{-8} - 10^{-7}$ in the medium term and with an uncertainty of tens of ppm. Standard low noise oscillators are available at 5 MHz, 10 MHz and 100 MHz, but generally digital systems are clocked at higher frequencies (like 125 MHz, 250 MHz); therefore a frequency synthesizer is necessary for generating the proper system clock. Since external commercial synthesizers are expensive and bulky, in these cases it is possible to take advantage of the internal PLL provided by the FPGA to generate the internal clock from an external frequency reference. However, the PLL phase noise could degrade the oscillator stability thereby limiting the entire system performance becoming a critical component for digital instrumentation.

Different methods for PLLs noise characterization have been proposed. An analysis of the noise introduced by filters, mixers, amplifiers and frequency multipliers in analog PLLs is presented in [50]. The results of such an analysis gave a guideline for phase noise reduction on further PLL designs. Another group [51] investigated the jitter in CMOS PLLs and its propagation along the circuit gates giving also design guidelines but in this case for digital chips. PLL assessment through noise modeling has been widely used with different purposes such as jitter extraction from the Power Spectral Density (PSD) of the phase noise [52] and prediction of long term effects caused by transistors degradation [53]. The authors of [54] presented a theoretical analysis of the phase noise and jitter, where the effects introduced by the main components, Voltage Controlled Oscillator (VCO), Phase Deterctor (PD), frequency multipliers and frequency dividers, are considered. A characterization based on the comparison of the PLL performance reached by using two different approaches for the Voltage Controlled Oscillator (VCO) design was proposed [55] focused on the implementation of high speed spectrum clock generators. An analysis of the PLL noise was performed recently [56], in order to evaluate a technique for reducing the noise effects a low frequencies. Based on these results a

PLL was fabricated, validating the theoretical analysis through experimental measurements in a frequency range from 10 kHz to 30 MHz.

Hence, in view of the fast advances in technology and in the frame of evaluating the limiting components for time and frequency applications, the work presented here is focused on the noise characterization of the front-end hardware (ADCs and DACs) and digital PLLs embedded in FPGAs, considered as the critical blocks of digital instrumentation for time and frequency metrology. From the characterization results the ultimate performance of the instrument is obtained thereby allowing to perform punctual considerations according to the application requirements resulting in an efficient system performance. Although the characterization is addressed to time and frequency applications, the results have general validity.

1.4 Outline of the Thesis

In Chapter 2, notions and definitions related to phase and amplitude noise metrology are developed. In order to characterize the noise introduced by ADCs, PLLs and DACs, this work proposes a noise model for each component under study. The models aim to discriminate the different contributions involved in the phase and/or amplitude noise processes. In this chapter a description of such models is performed together with the description of a proposed method for the extraction and measurement of the corresponding noise parameters. These models and methods are validated by characterizing a commercially available platform, Red Pitaya. The platform is an open source embedded system whose resolution and speed (14 bit, 125 MSps) are reasonably close to the state of the art of ADCs and DACs (16 bit, 350 MSps or 14 bit, 1 GSps) and it is potentially sufficient for the implementation of a complete instrument.

In Chapter 3 an overview of Red Pitaya is given. Additionally, the description of the methods implementation is presented and the results of the characterization are reported. Based on these results the ultimate performance of the platform is obtained and discussed. At the end of the chapter, a brief description of the assessment of a high performance platform, currently in development, is performed. Some preliminary results about the characterization of the DAC noise are reported.

In Chapter 4 the implementation of a digital instrument for frequency transfer using fiber link is presented. Based on the results obtained from the characterization, the feasibility of this instrument implementation using Red Pitaya platform was verified. In this chapter a brief introduction to frequency transfer is presented. Hence, the proposed digital system is described from the design point of view. Finally, according to the design considerations, the implementation of the system is presented. The results of the first measurements using this instrument on a 300 km loop fiber between INRiM and the Laboratoire Souterrain de Modane (LSM) on the Italy-France border are reported.

The last chapter, Chapter 5, reports the conclusions of this work. In addition, further developments, currently under implementation, are presented together with future perspectives.

Chapter 2

Characterizing Noise in Digital Electronics

2.1 Noise Definitions

The noise characterization proposed in this work aims to discriminate the different noise contributions of the critical components involved in digital instrumentation for time and frequency metrology. This is performed in the basis of two random noise classes: additive and parametric. Additive noise refers to a noise process that can be represented as a voltage or a current added to the signal, caused by the thermal noise on resistive elements and by shot and avalanche noise present in the junctions of semiconductors [57]. This noise is generated in the signal bandwidth and it is always present, even without carrier information. Instead, parametric noise refers to a non-linear near-DC process caused by non linearities present in electronic circuits due to contamination in semiconductors materials [58]. It is translated by action of a carrier, generating amplitude and/or phase modulation on the signal. Both noise mechanisms result in amplitude and/or phase noise on the radiofrequency carrier.

The phase noise $\varphi(t)$ [rad] is represented in the frequency domain through its power spectral density (PSD) $S_\varphi(f)$ [rad^2/Hz]. Alternatively, it is expressed as phase-time fluctuations $\mathsf{x}(t)$ [s], i.e., random phase fluctuations converted into time as stated in (2.1), where ν_0 is the carrier frequency.

$$\mathsf{x}(t) = \frac{\varphi(t)}{2\pi\nu_0} \tag{2.1}$$

The corresponding PSD of the time noise $\mathsf{x}(t)$ is expressed as $S_{\mathsf{x}}(f)$ [s^2/Hz] and it is related to $S_\varphi(f)$ by following (2.1) as

$$S_{\mathsf{x}}(f) = \frac{1}{4\pi^2\nu_0^2} S_\varphi(f) \tag{2.2}$$

The amplitude noise is represented by $\alpha(t)$ and it is defined as the random fractional amplitude [non-dimensional] induced by the device noise. The PSD of $\alpha(t)$ is $S_\alpha(f)$ given in 1/Hz.

A noisy signal can be also described through the phasor representation as shown in Fig. 2.1, where n_α and n_φ are the in-phase and quadrature components of the noise, respectively.

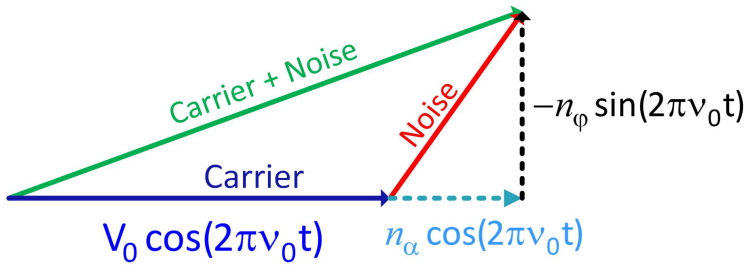


Fig. 2.1 Phasor representation of a noise sinusoidal signal. In-phase and quadrature noise components. The negative sign is only for convention purposes.

This is an useful representation for analyzing separately the effects of the noise on the phase and the amplitude on a certain signal.

$$\alpha(t) = \frac{n_\alpha}{V_0} \qquad \varphi(t) = \frac{n_\varphi}{V_0} \tag{2.3}$$

The polynomial law or power law is a meaningful model for noise description and analysis in which the random fluctuations are represented as the sum of independent noise processes. It has been widely used for describing phase noise in oscillators [59–61] and for the noise analysis of two-port components [58].

Hence, the PSD of the phase noise and the time noise are represented by the polynomial law in (2.4).

$$S_{\varphi}(f) = \sum_{j=\beta}^{0} \mathsf{b}_j f^j \qquad S_{\mathsf{x}}(f) = \sum_{j=\beta}^{0} \mathsf{k}_j f^j \tag{2.4}$$

The value of $\beta < 0$, the minimum polynomial order as found at the lower bound of the sums of (2.4), can be -4 or more negative for oscillators, but it is generally limited to -1 for two-port components, where 0 corresponds to white noise and -1 to flicker noise. The coefficients k_j are technical parameters of the device that quantify the induced time fluctuations.

The PSD of the voltage noise $n(t)$, $S_v(f)$ [V^2/Hz], is also described through the polynomial law (2.5). The coefficients h_j provide technical information of the device in analogy with the voltage noise parameter expressed in $\mathrm{nV}/\sqrt{\mathrm{Hz}}$ for analog electronics [57, 62].

$$S_v(f) = \sum_{j=\beta}^{0} \mathrm{h}_j f^j \tag{2.5}$$

According to the behavior of the statistical properties of $\varphi(t)$ and $\mathsf{x}(t)$ with respect to the input carrier frequency ν_0, two types of noise are defined: phase-type and time-type noise [63]. The phase-type (φ-type) noise is a noise mechanism for which the statistical properties of the induced phase $\varphi(t)$ remain invariant while changing ν_0. In this case, the phase fluctuations converted into time $\mathsf{x}(t)$ following the relation stated in (2.1). On the other hand, the time-type (x-type) noise is a noise mechanism for which the statistical properties of the generated time noise $\mathsf{x}(t)$ are constant by changing ν_0 while $\varphi(t)$ is proportional to ν_0 according to (2.1). These concepts are an useful tool for the discrimination of the different noise sources present in digital electronics.

The noise modeling presented in the sections below aims to describe the main noise sources of the components of interest (ADC, PLL and DAC) in function of their coefficients k_j and h_j having a complete description of the device performance at frequencies offsets close to the carrier. Once the coefficients are extracted, since they are equivalent to technical parameters of the devices, the noise contributions could be predicted for any operational condition.

2.2 Analog to Digital Converter - ADC

2.2.1 Noise Model

The ADC noise modeling presented here focuses on four main noise sources, as it is depicted in Fig. 2.2: input stage, aperture jitter, voltage reference and quantization.

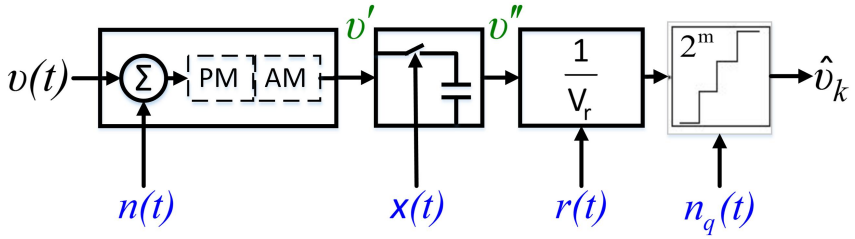


Fig. 2.2 ADC noise model. The parameters of the model represent the four noise sources involved in an acquisition process: input stage circuit, aperture jitter, voltage reference and quantization.

The contribution of the noise generated by the input stage has two components: additive and parametric. For the model proposed here, this noise source is assumed to be dominated by the additive noise $n(t)$. This assumption is verified through the experimental results reported in section 3.2.2. Hence, considering an input signal $v(t)$, the effect of the input stage noise is expressed as $v'(t) = v(t) + n(t)$.

The aperture jitter, $\mathsf{x}(t)$, defined as the variation of the sampling instant kT_s, is caused by time fluctuations in the sample and hold [64, 65]. These time fluctuations generate a parametric noise whose effects over the sampled signal are described by $v''_k = v'(kT_s + \mathsf{x}_k)$, where $\mathsf{x}_k = \mathsf{x}(kT_s)$.

At this point, the sample v''_k is converted into a digital value, as described in (2.6), where m is the resolution of the ADC, V_r is the voltage reference and n_q is the quantization noise.

$$\hat{v}_k = v''_k \frac{2^m}{V_r} + n_q \tag{2.6}$$

The voltage reference is considered as a non-ideal source, $V_r = V_{r_0}(1 + r(t))$, represented by the nominal value V_{r_0} and the relative noise $r(t)$. This noise

source is presented as a parametric noise whose features depend on the voltage reference topology [66].

The quantization noise n_q, well described currently in literature [67], generates white phase noise spread along the Nyquist bandwidth ($\frac{1}{2T_s}$). For high resolution ADCs, like the ones studied here, the effective number of bits (ENOB) is significantly lower than the nominal value, therefore the effect of this noise source can be neglected, at first order, with respect to the other noise contributions and for this reason it is not included in the proposed model.

Since m and V_{r_0} are constant values, it is convenient, in analogy with operational amplifiers, to refer the noise to the input by dividing the output by $\frac{2^m}{V_{r_0}}$. Then, the ADC output referred to the input can be expressed as $\tilde{v}_k = \hat{v}_k \frac{V_{r_0}}{2^m}$.

Under the assumption of $r \ll 1$, the ADC output is described by (2.7), where $n_k = n(kT_s)$, $\mathsf{x}_k = \mathsf{x}(kT_s)$ and $r_k = r(kT_s)$ are discrete-time random processes obtained from sampling the corresponding continuous-time random process at $t = kT_s$.

$$\tilde{v}_k = (n_k + v(kT_s + \mathsf{x}_k))(1 - r_k) \tag{2.7}$$

Now that the ADC output is stated in terms of the noise sources, their effects can be analyzed using a proper input for discriminating their contributions. Following (2.7), the contribution of x_k propagates to the ADC output depending on the slew rate of the input signal, while the impact of r_k depends on the input signal level. Note that in the case of $v(t) = 0$, the contribution of the aperture jitter and the voltage reference noise are negligible, therefore the ADC output corresponds to the additive noise of the input stage.

Then, assuming $v(t) = V_0 \cos(2\pi\nu_0 t)$ as input signal of the ADC, case of interest for time and frequency applications, (2.7) can be rewritten as

$$\tilde{v}_k = (n_k + V_0 \cos(2\pi\nu_0(kT_s + \mathsf{x}_k)))(1 - r_k) \tag{2.8}$$

Considering n_k, x_k and r_k independent processes, the total amplitude and phase noise generated by the ADC can be expressed as the sum of the different amplitude and phase fluctuations induced by each noise source, respectively.

The additive noise of the input stage n_k generates amplitude and phase noise on the converted signal. In order to better discriminate its effects, this noise source is represented as the in-phase n_α and quadrature n_φ noise components. The aperture jitter x_k results in pure phase modulation on the analog to digital conversion given by $\varphi_\mathsf{x} = 2\pi\nu_0\mathsf{x}$. The maximum voltage variations induced by this noise source occur at the samples of highest slew rate (SR), i.e., close to the zero-crossings and are described by $V_0 2\pi\nu_0\mathsf{x}_k$. Moreover, it is worth remarking that the samples of maximum amplitude are not influenced by this noise contribution at the first order. Instead, they are directly related to the voltage reference noise presented as amplitude modulation on the converted signal. It generates a maximum voltage error $V_0 r_k$ that occurs at the maximum amplitude samples of the input signal.

Hence, the total ADC phase noise φ_k and the total ADC amplitude noise α_k are described in (2.9), where φ_k is in radians and α_k is non-dimensional, being the normalized amplitude fluctuations [59].

$$\begin{aligned} \varphi_k &= \frac{1}{V_0} n_{\varphi_k} + 2\pi\nu_0\mathsf{x}_k \\ \alpha_k &= \frac{1}{V_0} n_{\alpha_k} + r_k \end{aligned} \tag{2.9}$$

The PSD of the ADC phase noise in rad^2/Hz and the PSD of the ADC amplitude noise in $1/\text{Hz}$ are described through the power law in (2.10).

$$S_\varphi(f) = \sum_{j=\beta}^{0} \mathsf{b}_{s_j} f^j \qquad S_\alpha(f) = \sum_{j=\beta}^{0} \mathrm{h}_{s_j} f^j \tag{2.10}$$

The difference between the analog bandwidth B and the sampling frequency f_s in a digital circuit generates aliasing on the white noise region of the sampled signal spectrum [63]. Hence, the voltage noise spectrum of the sampled signal can be represented as $S_{\tilde{v}}(f) = \frac{2B}{f_s}\mathrm{h}_0 + \sum_{j=N}^{-1} \mathrm{h}_j f^j$ $[\text{V}^2/\text{Hz}]$. For the case of the aperture jitter, aliasing is generated in the white noise region of the spectrum, caused by the fact that these fluctuations are sampled at the sampling clock (f_s). Thus, the spectrum of x_k can be expressed as $S_{\mathsf{x},s}(f) = \frac{2}{f_s}\mathsf{J}^2 + \sum_{j=N}^{-1} \mathsf{k}_j f^j$ $[\text{s}^2/\text{Hz}]$, where J is the root mean square (rms) time fluctuation of the aperture jitter

and $\mathsf{k}_0 = \frac{2}{f_s}\mathsf{J}^2$. The spectrums of n_{φ_k}, n_{α_k} [V^2/Hz] and r_k [1/Hz] represented through the polynomial law are described in (2.11). Since r_k represents a relative amplitude noise, the coefficients h_{r_j} are non-dimensional.

$$\begin{aligned} S_{n_\varphi,s}(f) &= \sum_{j=N}^{0} \mathrm{h}_{\varphi_j} f^j \qquad [\mathrm{V}^2/\mathrm{Hz}] \\ S_{n_\alpha,s}(f) &= \sum_{j=N}^{0} \mathrm{h}_{\alpha_j} f^j \qquad [\mathrm{V}^2/\mathrm{Hz}] \\ S_{r,s}(f) &= \sum_{j=N}^{0} \mathrm{h}_{r_j} f^j \qquad [1/\mathrm{Hz}] \end{aligned} \tag{2.11}$$

Hence, from (2.9), the spectrums of the phase and amplitude noise of the ADC are

$$\begin{aligned} S_{\varphi,s}(f) &= \frac{1}{V_0^2} S_{n_\varphi,s}(f) + 4\pi^2 \nu_0^2 S_{\mathsf{x},s}(f) \\ S_{\alpha,s}(f) &= \frac{1}{V_0^2} S_{n_\alpha,s}(f) + S_{r,s}(f) \end{aligned} \tag{2.12}$$

In this manner, from (2.12) the contribution of each noise source for each different noise process could be identified having a complete description of the device limitations.

2.2.2 Proposed method for extracting the model parameters

In order to extract the ADC noise components stated in the model, a method is proposed. Such a method is based on data acquisitions under three different measurement conditions that allow characterizing the three main noise processes of the model: input stage, aperture jitter and voltage reference. In the first condition, the input of the ADC is connected to ground through a 50 Ω resistor. In this case, the contribution of $\mathsf{x}(t)$ and $r(t)$ are negligible, since the slew rate and the level of the signal are zero. Therefore, the voltage noise on the data acquired is totally related to the additive noise of input stage. The other

two measurements are made by sampling synchronously two points of the cosine-wave at the input: the zero-crossings and the peak values.

Considering that the voltage noise of the zero-crossings is directly related to phase fluctuations (PM), the measurement of these variations will result in the estimation of the phase noise generated by $n_\varphi(t)$ and $\mathsf{x}(t)$. On the other hand, the voltage noise on the peak values is representative of the amplitude fluctuations (AM), therefore the measurement of the variation of these samples from period to period will yield the amplitude noise added by $n_\alpha(t)$ and $r(t)$. Hence, the total ADC noise can be estimated through these measures as described in (2.13), where $S_{\tilde{v},\varphi}$ and $S_{\tilde{v},\alpha}$ are the PSD of the voltage noise of the signal sampled at zero-crossings and at the peak values, respectively.

$$\begin{aligned} S_{\varphi,s}(f) &= \frac{1}{V_0^2} S_{\tilde{v},\varphi} \\ S_{\alpha,s}(f) &= \frac{1}{V_0^2} S_{\tilde{v},\alpha} \end{aligned} \tag{2.13}$$

It is important to notice that with a single channel configuration, the noise obtained is also influenced by the noise contributions of the sampling clock and the input signal generator. Since the objective of this work is to characterize the ADC for phase noise metrology which, in general, is based on differential techniques, a configuration with two independent channels is proposed as depicted in Fig. 2.3.

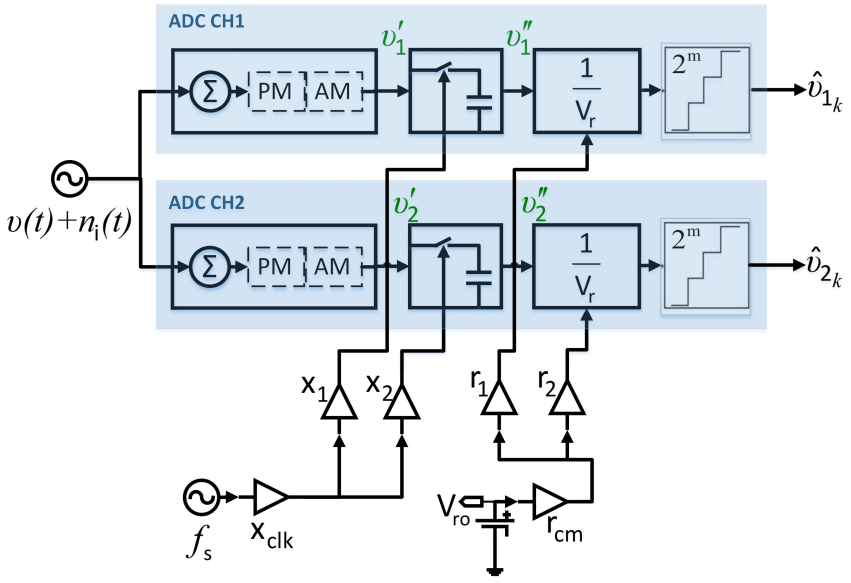


Fig. 2.3 Key interplay in dual converters. Discrimination between common noise and single channel noise sources in dual converters.

The common noise contributions such as the one coming from the input signal generator (n_i), the sampling clock (x_{clk}) and the voltage reference (r_{cm}) are canceled by subtracting the data obtained simultaneously from the two channels. In consequence, the noise estimated is the contribution of the two ADC channels. Since the channels are assumed to be uncorrelated, the noise of a single channel is half the total noise.

The scheme of the synchronous sampling system, that is in charge of acquiring the zero-crossings and the peaks of the cosine-wave, is shown in Fig. 2.4.

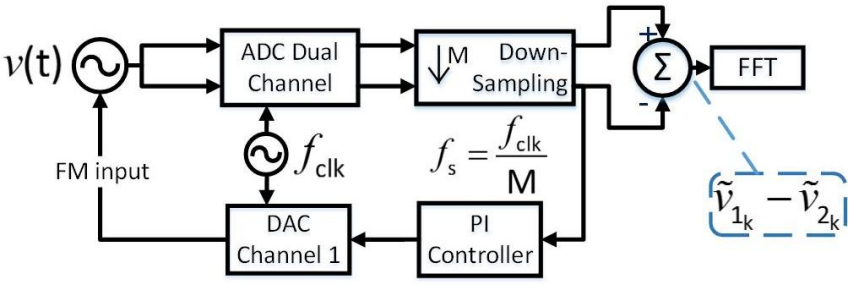


Fig. 2.4 The proposed scheme allows sampling synchronously one sample per period in order to measure, through its variations, the ADC noise effect on the output, as amplitude and phase fluctuations. The implementation is based on a dual ADC, and through the difference of the two outputs, the common noise is canceled obtaining only the corresponding noise contribution of each channel.

The principle of operation consists in aligning the input signal to the sampling clock by means of a Phase Locked Loop (PLL): the input signal is sampled and sent to a Proportional-Integral controller (PI) which drives the frequency of the signal generator through a DAC, providing the proper phase information. The input signal generator works as a Voltage Controlled Oscillator (VCO) correcting the signal generated to acquire the selected point, either for AM or PM characterization. For PM characterization, it is possible to sample input signals whose frequency is multiple of the sampling clock by means of sub-sampling. To extend the measurements at lower frequencies (ν_0 sub-multiple of f_{clk}) the data rate is down-sampled. Therefore, the sampling frequency f_s becomes equal to the input frequency ν_0, ($f_s = \frac{f_{clk}}{M} = \nu_0$). For AM characterization, an input frequency not higher than quarter the sampling clock is provided in order to guarantee the peaks acquisition. In this case, the system is still synchronized through the zero-crossings but only the peak values are acquired.

The PSD of the ADC noise is estimated in a bandwidth equal to the Nyquist frequency. The corresponding information at low frequencies can be obtained through decimation stages.

2.3 Phase Locked Loop - PLL

2.3.1 Noise Model

The noise analysis here presented is based on the scheme of the internal PLL provided by the FPGA embedded into the SoC Zynq 7010 from Xilinx (Fig. 2.5). Although this specific scheme is used, the analysis can be extended to any PLL taking into account the corresponding operation frequency range.

The Voltage Controlled Oscillator (VCO) of this PLL works between 800 MHz and 1.6 GHz and generates eight output phases each one with an independent counter (O). The Phase and Frequency Detector (PFD) provides a signal proportional to the phase and frequency difference between the input (ν_0/D) and the feedback signal (ν_{vco}/M). The driving voltage for the VCO is generated from this difference through the Charge Pump (CP) and the Low Pass Filter (LPF). Hence, under lock condition, the output frequency is given by $\nu_o = \frac{M}{DO}\nu_0$. The three parameters, M, D and O, can be configured by the user. The minimum input clock frequency is fixed by the FPGA topology and for this SoC (Artix-7 based FPGA) is 10 MHz.

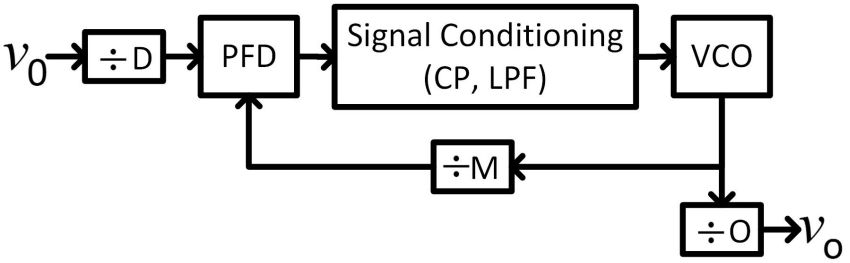


Fig. 2.5 Block diagram for PLL Analysis and Characterization. Scheme of Internal PLL - Xilinx.

The phase noise of the PLL $\varphi(t)$ is represented in the frequency domain through its power spectral density (PSD) $S_\varphi(f)$.

Here, two main noise sources are considered: the voltage noise $n(t)$ of the input threshold and the time noise $\mathsf{x}(t)$ induced by the delay on the propagation path of the PLL. The PSD of $n(t)$ is represented through the polynomial law as $S_v(f) = \sum_{j=m}^{0} \mathrm{h}_j f^j$. These voltage fluctuations generate time noise related to the input slew rate (SR) as:

$$\mathsf{x}_n(t) = \frac{n(t)}{SR} \tag{2.14}$$

Hence, by using (2.1), (2.14) is expressed as phase noise. Considering $v(t) = V_0 \cos(2\pi\nu_0 t)$ the input of the PLL, it is given by

$$\varphi_n(t) = \frac{n(t)}{V_0} \tag{2.15}$$

The PSD of $\mathsf{x}(t)$ is represented through the polynomial law as $S_{\mathsf{x}}(f) = \sum_{j=m}^{0} \mathsf{k}_j f^j$. Recalling (2.1), these time fluctuations are also expressed as phase noise:

$$\varphi_{\mathsf{x}}(t) = 2\pi\nu_0 \mathsf{x}(t) \tag{2.16}$$

The total phase noise of the PLL is then,

$$\varphi(t) = \frac{n(t)}{V_0} + 2\pi\nu_0 \mathsf{x}(t) \tag{2.17}$$

Both noise processes, $\mathsf{x}(t)$ and $n(t)$, are sampled at $2\nu_0$, in correspondence with the rising and falling zero crossings leading to a Nyquist bandwidth of ν_0. However, in digital electronics the analog bandwidth B is higher than the maximum ν_0 therefore the Nyquist theorem is not satisfied in the general case and aliasing occurs. As consequence, the phase white noise floor is degraded by a factor of B/ν_0, while the flicker level is unaffected by the sampling process [63].

For the PLL phase noise assessment and characterization, it is convenient to report the noise to the output. In this manner, the effects are directly analyzed at the particular frequency output of interest.

Hence, the phase noise induced by $n(t)$ and $\mathsf{x}(t)$, reported at the output of the PLL, are stated by (2.18) and (2.19) respectively, where the coefficients h_j and k_j are technical parameters of the device, as described in Section 2.1.

$$S_{\varphi,n}(f) = \frac{\nu_o^2}{\nu_0^2 V_0^2} \left(\frac{B\mathrm{h}_0}{\nu_0} + \sum_{j=m}^{-1} \mathrm{h}_j f^j \right) \tag{2.18}$$

$$S_{\varphi,x}(f) = 4\pi^2\nu_o^2\left(\frac{B\mathsf{k}_0}{\nu_0} + \sum_{j=m}^{-1}\mathsf{k}_j f^j\right) \tag{2.19}$$

2.3.2 Proposed method for PLL noise characterization

In order to discriminate the two noise sources, voltage noise and time noise, the dependence of the PLL noise characteristics with respect to the input slew rate are investigated. It is done by considering that the slew rate is defined by the input signal carrier frequency and power.

Hence, by changing the input carrier frequency and power, the PLL frequency stability and phase noise can be assessed. This allows predicting its contributions to the performance of a specific time and frequency application in a wide range of the PLL operating conditions.

The method proposed for extracting the PLL noise s shown in Fig. 2.6. The digital phasemeter, intended to be used, performs a technique for direct phase comparison between the input (IN) and the reference (REF), that may not be at the same frequency, while rejecting the common noise. By using the method proposed, the phase noise of the input signal is rejected, thereby obtaining directly the phase noise of the PLL. It is expected that the intrinsic noise of the FPGA (input and output stages) does not limit the PLL output stability. However, the phase noise of the FPGA is verified by applying the same method but in this case bypassing the PLL.

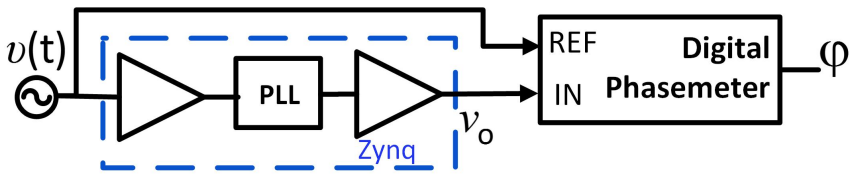


Fig. 2.6 Method proposed for PLL phase noise characterization.

2.4 Digital to Analog Converter - DAC

2.4.1 Noise Model

The noise introduced by the DAC is analyzed based on the fact that this component performs a complementary process with respect to the ADC. Therefore, the main noise sources involved in the digital to analog conversion are homologous to the noise sources on an analog to digital conversion: the quantization noise $n_q(t)$, the relative noise of the voltage reference $r(t)$, the aperture jitter of the sample and hold $\mathsf{x}(t)$ and the additive noise of the output stage $n(t)$ (input stage for the case of the ADC). Hence, the model proposed for the description of the DAC noise sources is shown in Fig. 2.7.

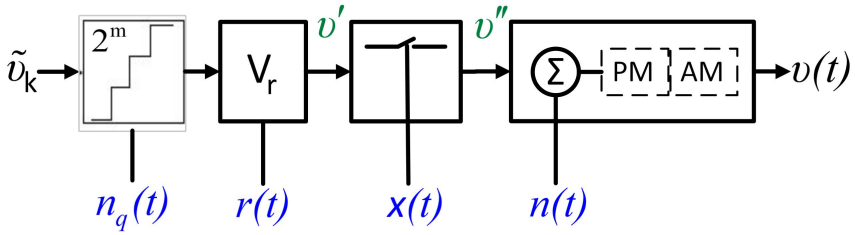


Fig. 2.7 Block diagram for DAC analysis and characterization.

The digital value $\tilde{v_k}$ is converted to voltage through an inverse quantization process with respect to the ADC, as described in (2.20), where m is the resolution of the DAC, V_r is the voltage reference and n_q is the quantization noise.

$$v'_k = \tilde{v}_k \frac{V_r}{2^m} + n_q \tag{2.20}$$

Since this noise analysis is addressed to high resolution DACs, the effect of the quantization noise, considered white phase noise spread along the Nyquist bandwidth $\left(\frac{1}{2T_s}\right)$ can be neglected, at first order; therefore it was not included in the DAC model studied here. The reference is considered as a non-ideal source described by $V_r = V_{r0}(1 + r(t))$, where V_{r0} is the nominal value and $r(t)$ is the relative noise.

Subsequently, the value v' is hold during a time T_s until a new value arrives. The time noise $\mathsf{x}(t)$ of the sample and hold generates pure phase modulation on

the signal converted v''. Finally, the effect of the additive noise of output stage $n(t)$, considered dominant with respect to the parametric noise (see 2.2.1 for further details) on the sample converted is described in (2.21), where $t = kTs$. Considering $r \ll 1$, the effect of $\mathsf{x(t)}$ on this noise source is negligible. As done in the ADC analysis, the noise is reported to the input by dividing the output by $\frac{V_r}{2^m}$.

$$v(t) = \tilde{v}(t + \mathsf{x}(t))(1 + r(t)) + n(t) \tag{2.21}$$

Thus, from (2.21) and from the analysis shown in Section 2.2.1 for the ADC noise, the phase and amplitude noises of the DAC are expressed as shown in (2.22), where $\varphi_n(t)$ and $\alpha_n(t)$ are the phase and amplitude noises introduced by the additive noise of the output stage, respectively. On the other hand, ν_0 is the frequency of the sine-wave $\tilde{v}(k) = V_0 cos(2\pi\nu_0 k)$, generated numerically for feeding the DAC.

$$\varphi(t) = \varphi_n(t) + 2\pi\nu_0\mathsf{x}(t) \qquad \alpha(t) = \alpha_n(t) + r(t) \tag{2.22}$$

Contrary to the ADC case, the voltage fluctuations of the output stage are not sampled; therefore they do not suffer of aliasing in the white region. Then, by using the power law, the spectrum of the these voltage fluctuations can be represented as $S_v(f) = \sum_{j=N}^{0} \mathrm{h}_j f^j$ [V^2/Hz]. For the case of the aperture jitter, aliasing is generated in the white noise region of the spectrum, caused by the fact that these fluctuations are sampled at the sampling clock (f_s). Thus, the spectrum of x_k can be expressed as $S_{\mathsf{x},s}(f) = \frac{2}{f_s}\mathsf{J}^2 + \sum_{j=N}^{-1} \mathsf{k}_j f^j$ [s^2/Hz], where J is the root mean square (rms) time fluctuation of the aperture jitter and $\mathsf{k}_0 = \frac{2}{f_s}\mathsf{J}^2$.

Thus, the PSD of the phase and amplitude noises of the DAC are given by

$$S_\varphi(f) = \frac{1}{V_0^2} S_v(f) + 4\pi^2 \nu_0^2 S_x(f) \tag{2.23}$$
$$S_\alpha(f) = \frac{1}{V_0^2} S_v(f) + S_r(f)$$

In this manner, a complete description of the DAC noise is obtained thereby being able to perform punctual consideration for the design of instrumentation based on the DAC operation with a measurement bandwidth of 5 Hz.

2.4.2 Proposed method for DAC noise characterization

Although the noise model includes the amplitude noise component, the model proposed here is focused on the extraction of the phase noise because this noise is, in general, the dominant contribution and therefore the main limitation for the implementation of a digital technique on time and frequency applications. This method will be eventually extended to the extraction of amplitude noise.

The method that is proposed here, is based on common noise rejection and it is intended to provide the residual phase noise of the DAC. As shown in Fig. 2.8, the DAC is fed with a sine-wave generated numerically by a Numerically Controlled Oscillator (NCO). A two channel DAC is used in order to cancel the common noise and in this manner to obtain only te contribution of the DAC. Assuming that the channels are uncorrelated, the noise of one channel is half the measured noise.

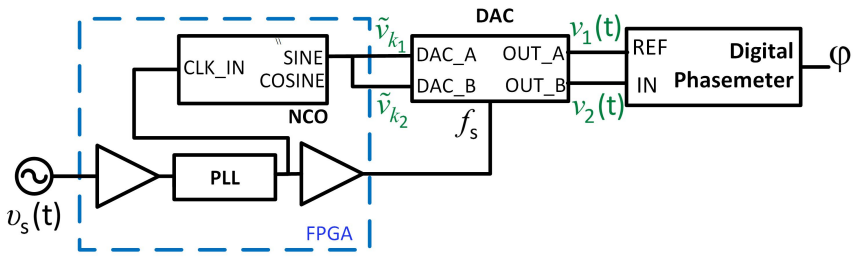


Fig. 2.8 Method proposed for DAC noise characterization.

Chapter 3

Noise Characterization of an Embedded Platform: Red Pitaya

3.1 Red Pitaya Platform Overview

Red Pitaya platform [68] is a commercially available and open source embedded system developed by Red Pitaya Company. It was designed for instrumentation purposes and some applications, currently available in the open repository [69], include oscilloscope, signal generator and spectrum analyzer.

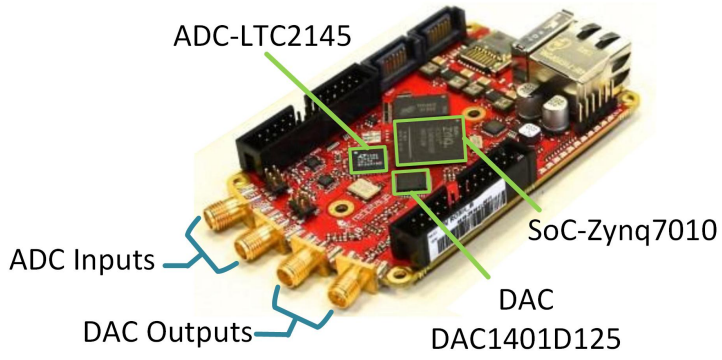


Fig. 3.1 Red Pitaya Platform. The models and methods for characterizing the noise introduced by ADCs, DACs and PLLs in digital instrumentation were validated in this commercially available platform.

This platform is provided with a dual-channel 14-bit ADC at 125 MSps - LTC2145 from Linear Technology, a dual-channel 14-bit DAC at 125 MSps - DAC1401D125 from NXP Semiconductors (for the version v1.0 of such a platform) and a Zynq 7010 System On Chip (SoC) from Xilinx. The SoC, described in Fig. 3.2, integrates the capabilities of the processing system (PS) based on a dual core Cortex-A9 ARM and Linux Operating System with the reconfigurability of the programmable logic (PL) that for this specific Zynq is based on the Artix-7 FPGA. This FPGA provides 28160 Logic Cells conformed by 4400 slices (four 6-input look up tables and eight storage elements), 80 Digital Signal Processing (DSP) slices for arithmetical operations, 60 configurable Ram Blocks (BRAM) of 36 kb each, and clocking resources such as two PLLs able of generating eight outputs each [70].

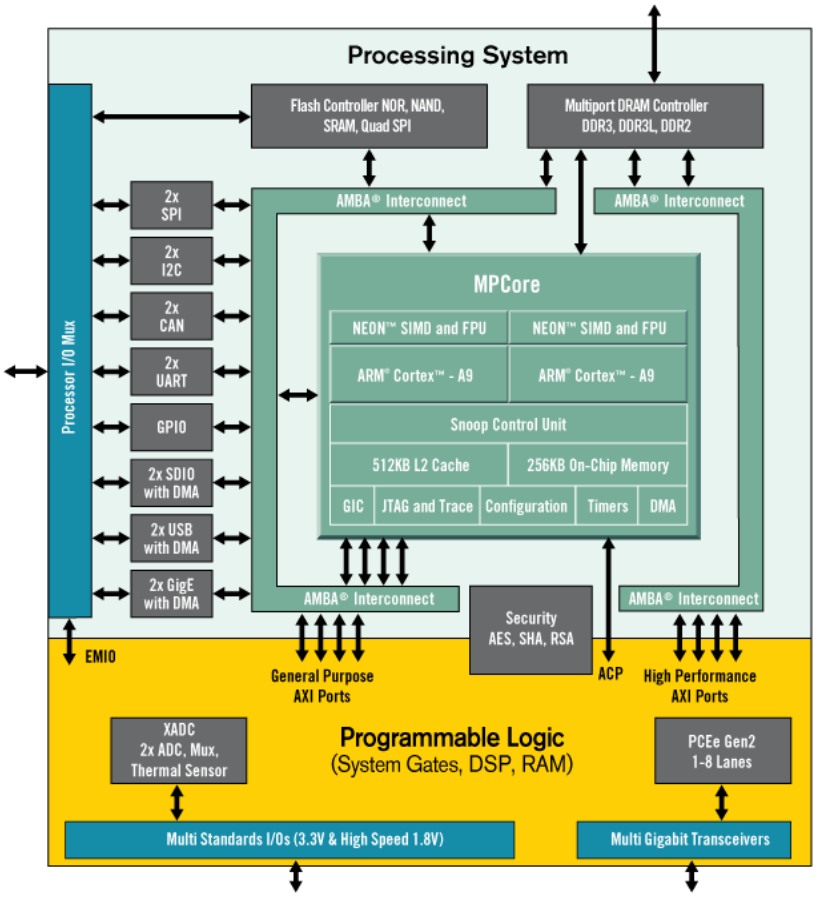


Fig. 3.2 Block diagram SoC Zynq 7000. From Xilinx website

The previously mentioned features make this platform a good option for the validation of the model and the methods here proposed. Based on the noise characterization results, the ultimate performance of Red Pitaya will be obtained; thereby assessing the implementation feasibility for a time and frequency application using this hardware. Furthermore, these results may allow a better general understanding of these components for time and frequency metrology.

3.2 ADC Noise Characterization

3.2.1 Implementation

Fig. 3.3 depicts a simplified block diagram of the method implemented in the Red Pitaya platform based on the analysis presented in Section 2.2. The input stage of Red Pitaya was modified by bypassing the amplifier and the low pass filter with a 1:1 RF transformer, allowing the acquisition of sine-wave signals up to 500 MHz in order to increase the input bandwidth and to expose the jitter effect. In this regard, the sample and hold has a bandwidth of 750 MHz [71]. The PSD of the ADC noise is estimated in a bandwidth equal to the Nyquist frequency. The corresponding information at low frequencies is obtained through six stages of decimation in order to acquire data down to 10 Hz or less according to the sampling frequency. Blocks of 16384 data per channel are post-processed offline using MATLAB.

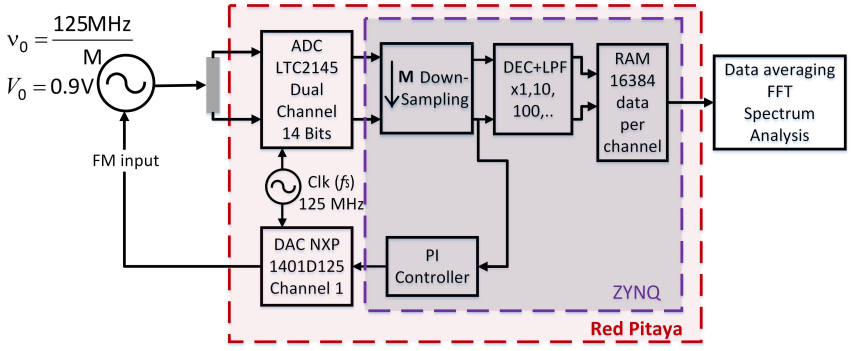


Fig. 3.3 Block diagram of method implemented in Red Pitaya platform. The data processing is performed offline using approximately 2×10^9 samples per each ADC channel.

3.2.2 Results

All the results presented in common mode are already scaled by -3 dB in order to analyze the noise of one ADC channel.

Additive Noise Input Stage

Fig. 3.4 shows the power spectral density of the voltage noise obtained by connecting the two ADC inputs to ground through a 50 Ω resistor, ($v(t) = 0$ V, $f_s = 125$ MHz). As described in section 2.2.1, this noise corresponds to the voltage error induced by the input stage. It presents an additive white noise of -154 dBV^2/Hz and an additive flicker of -107 dBV^2/Hz at 1 Hz. The quantization noise floor for the ADC under these conditions (14 bits and 2 V full scale) is -167 dBV^2/Hz [67]. The difference between this value and the estimated white noise floor is 13 dB, in agreement with the typical value of the effective number of bits (ENOB) stated in the ADC datasheet (11.8 bits).

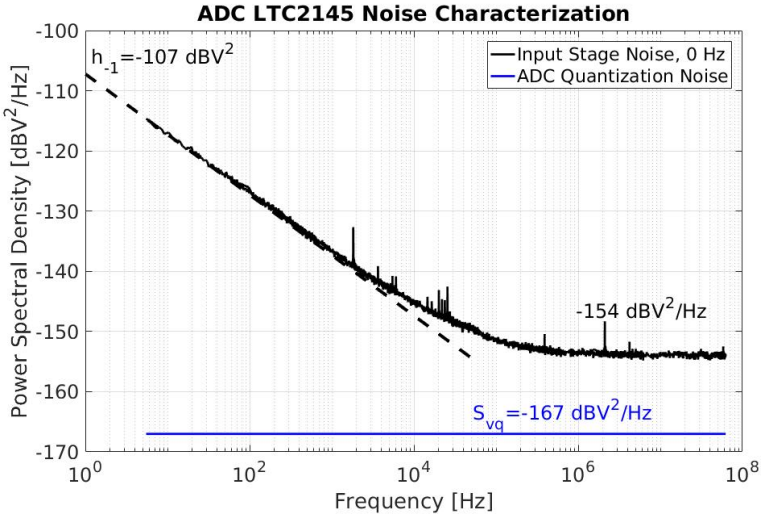


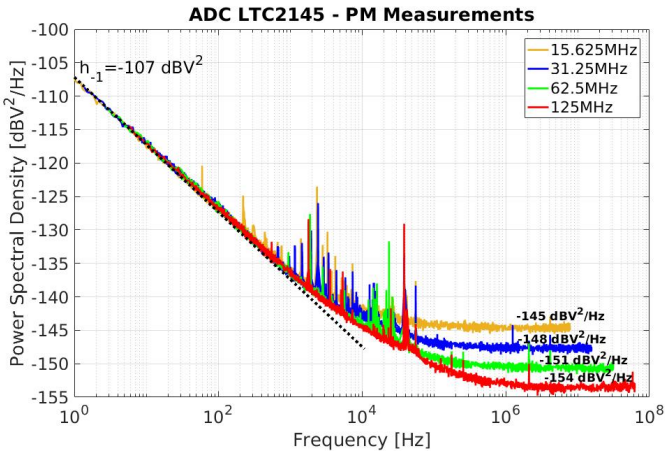
Fig. 3.4 Power spectral density of ADC LTC2145 input stage noise. The measurement was performed connecting the input to ground through a 50 Ω resistor.

PM Measurements

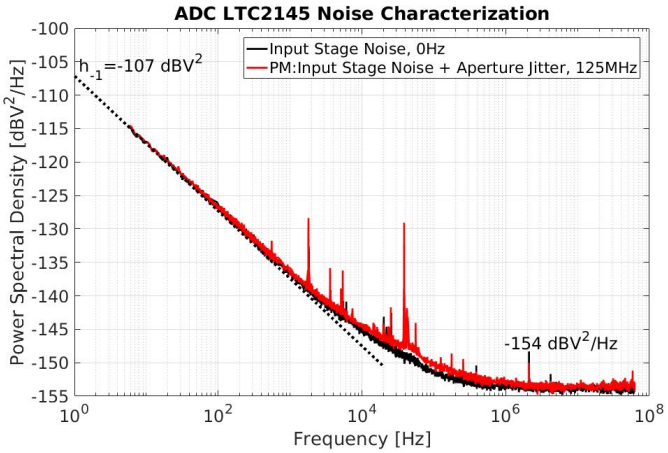
The measurements analyzed in this section were performed acquiring the zero-crossings of the input signal. The voltage noise generated in these samples

is induced by the additive noise of the input stage and by the aperture jitter multiplied by the slew rate, as described in (2.12). These two contributions can be discriminated by varying the amplitude and the frequency (i.e. the slew rate) of the input signal: for low slew rate, the additive noise dominates, while at high slew rate, the measure is representative of the aperture jitter.

Fig. 3.5a shows the ADC phase noise ($S_{\tilde{v},\varphi}$) estimated at different input frequencies and 0.9 V of peak amplitude. It can be observed that under these conditions the phase noise is independent of the carrier frequency; the white noise floor differences between each curve are due to aliasing caused by the down sampling performed in order to take only one sample per period. They correspond to aliased φ-type, phase noise caused by random fluctuations in the input stage circuit [63], where the variations are proportional to the ratio between the analog bandwidth B ($B = 750$ MHz for the ADC LTC2145) and the phase noise bandwidth (actual Nyquist frequency, $\frac{f_{clk}}{2M}$, according to the input frequency). On the other hand, the flicker phase noise is constant for all the input frequencies being the signature of pure φ-type noise, because it is not affected by aliasing. Fig. 3.5b shows the comparison between the additive noise of the input stage (measured with no signal at the input) and the zero-crossing noise induced by acquiring a sine-wave input with a frequency of 125 MHz and an amplitude of 0.9 V. These two noise spectrums are approximately equal. It suggests that the phase noise is dominated by the additive noise of the input stage and that this noise source is independent of the operation point. This is verified later on with the AM measurements. Furthermore, it confirms the assumption that, in this case, the parametric noise of the input stage is negligible with respect to the additive noise.



(a) Power spectral density of ADC phase noise.



(b) Input stage noise and aperture jitter comparison.

Fig. 3.5 a) The contributions of the input stage noise plus aperture jitter are shown. The measurements were taken at different carrier frequencies. The white phase noise level changes due to the aliasing introduced by the down sampling realized in order to take one sample per period at each carrier frequency. b) The phase noise introduced by the ADC is dominated by the additive noise of the input stage which is not dependent of the carrier frequency.

In order to expose the aperture jitter, the frequency input was increased, augmenting the slew rate. Fig. 3.6 shows the comparison between the PSD of the phase noise estimated at three different carrier frequencies: 125 MHz, 250 MHz and 500 MHz. The contribution of the aperture jitter can be appreciated from 250 MHz, especially in the flicker region, and it is more evident at 500 MHz. For frequencies higher than the sampling clock, the phase noise bandwidth remains at the maximum value (M is equal to 1 for these cases), therefore

the white phase noise floor reaches the minimum value. From these results we notice that the voltage noise induced by the aperture jitter starts to emerge at $\nu_0 = 250$ MHz.

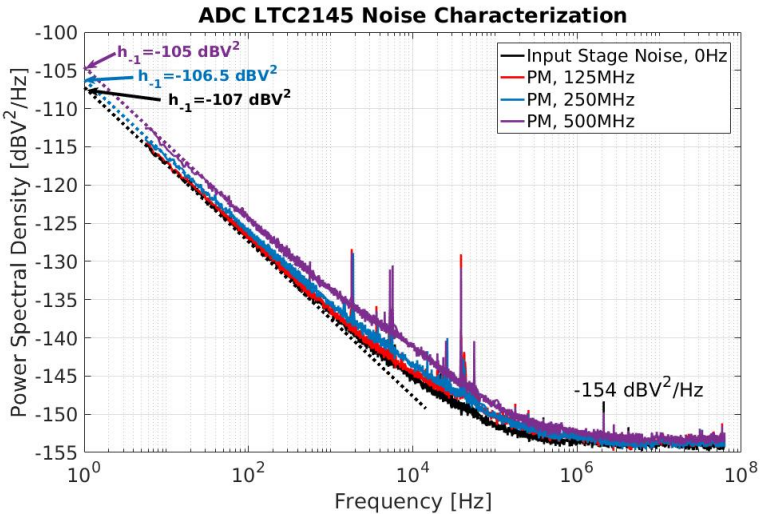


Fig. 3.6 Power spectral density of voltage noise induced in ADC conversion by phase and time fluctuations. The acquisitions were performed with ν_0 from 125 MHz to 500 MHz. The contribution of aperture jitter emerges at $\nu_0 = 250$ MHz.

The contribution of the aperture jitter can be estimated by subtracting the additive noise from the measures done at $\nu_0 = 250$ MHz and at $\nu_0 = 500$ MHz (Fig. 3.7). The ADC aperture jitter presents a white phase-time noise of -350 dBs^2/Hz for $\nu_0 = 500$ MHz, decreasing proportionally with the input frequency. According to the datasheet of the ADC LTC2145 [71], the aperture jitter is 100 fs$_{\text{rms}}$, that corresponds to a white noise of -338 dBs^2/Hz. The discrepancy could be due to the common noise rejection, estimating the residual aperture jitter for a single ADC channel. Additionally, the aperture jitter exhibits a flicker phase-time noise of -298 dBs^2/Hz at 1 Hz ($\sqrt{\mathsf{k}_{-1}} = 1.3$ fs), constant with respect to the frequency, signature of pure x-type noise [63].

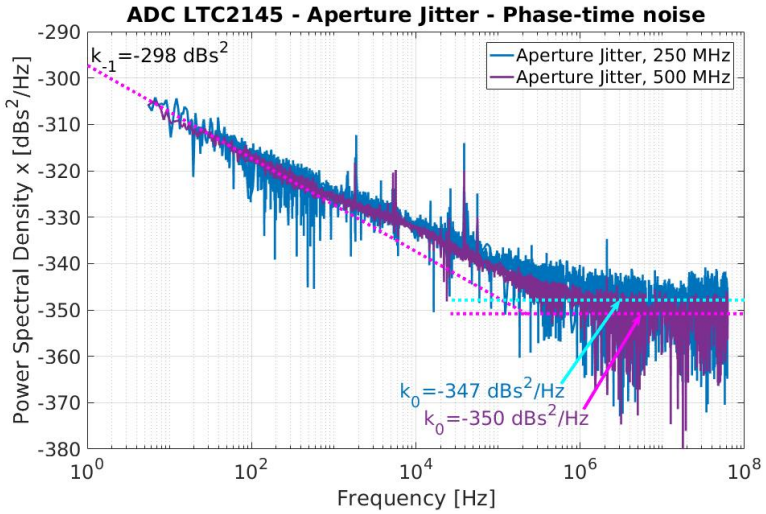


Fig. 3.7 Power spectral density of ADC aperture jitter. The aperture jitter is revealed from $\nu_0 = 250$ MHz. This result was obtained by subtracting the input stage noise from the ADC phase noise measured at zero-crossings. The obtained aperture jitter is differential and not absolute because of the common noise cancellation. The time jitter rms (J) is around 25 fs_{rms} related to the silicon, consistent with the datasheet information providing the absolute value of 100 fs_{rms}.

The previous results were obtained from the analysis of a series of spectra changing the input frequency, which confirm the presence of the two noise contributions. A similar analysis is performed in Fig. 3.8, but changing the input amplitude instead of the input frequency. Fig. 3.8 shows the total ADC phase noise ($S_{\varphi,s}$) at $\nu_0 = 500$ MHz when the aperture jitter is starting to emerge. It is seen that the total ADC phase noise is strongly dominated by the additive noise of the input stage, even if the aperture jitter is revealed. Moreover, it increases proportionally to $1/V_0^2$, as expected according to the model (2.12). From the results, reported in the precedent figures, the ADC LTC2145 has an ultimate phase noise floor of -153 dBrad^2/Hz (white) and -106 dBrad^2/Hz @ 1 Hz given by the additive noise of the input stage under maximum sampling frequency and full input voltage range. This noise floor agrees with the results presented in [43].

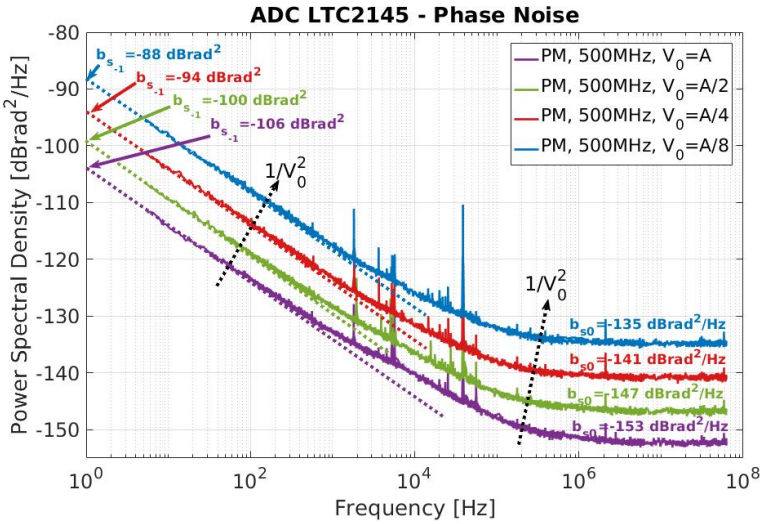


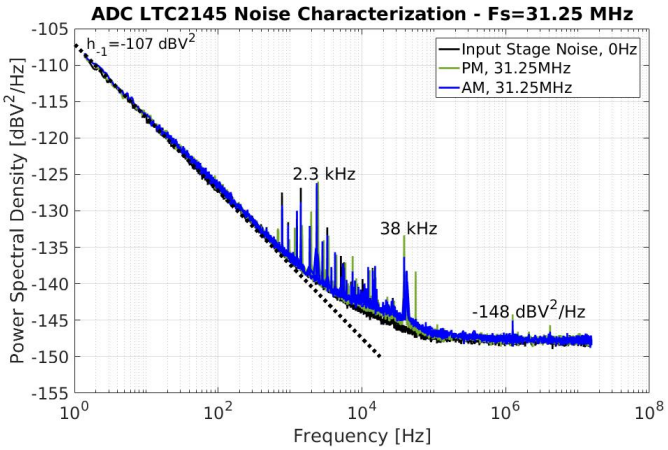
Fig. 3.8 Sensitivity of ADC phase noise to input amplitude.

AM measurements

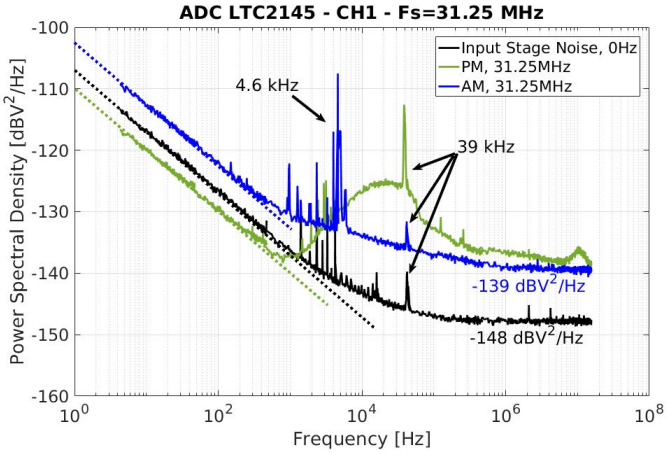
According to the model, the amplitude noise of the ADC is given by the superposition of the amplitude noise generated by the input stage and the voltage reference noise. Since the maximum voltage error induced by these noise contributions is generated at the points of maximum amplitude, they can be detected by sampling the peaks of the sine-wave. In order to guarantee the acquisition of these points, an input sine-wave of 31.25 MHz was used, i.e., quarter of the sampling clock (M=4).

Fig. 3.9 shows the comparison between the PSD of the voltage error estimated under the three measurement conditions: with no signal at the input ($S_{\tilde{v}}$), at zero-crossings ($S_{\tilde{v},\varphi}$) and at peak values ($S_{\tilde{v},\alpha}$). The results in common mode, depicted in Fig. 3.9a, suggest that the ADC amplitude noise is also dominated by the additive noise of the input stage. However, in order to confirm that the AM and PM measurements were done at the proper operating point, Fig. 3.9b shows the PSD of the voltage noise before the common noise rejection, i.e., in single channel. It can be noticed that the contributions of the PI and the feedback loop bandwidth (39 kHz) are evidenced in zero-crossings (PM), while at the peak values (AM) and with no input signal they are negligible. Instead of that, harmonic contributions at 4.6 kHz are observed which might be caused by the signal generator and that are also rejected in common mode.

These results confirm the method capability for discriminating the operation point (zero-crossings or peak values).



(a) PM and AM measurements comparison. Common mode.

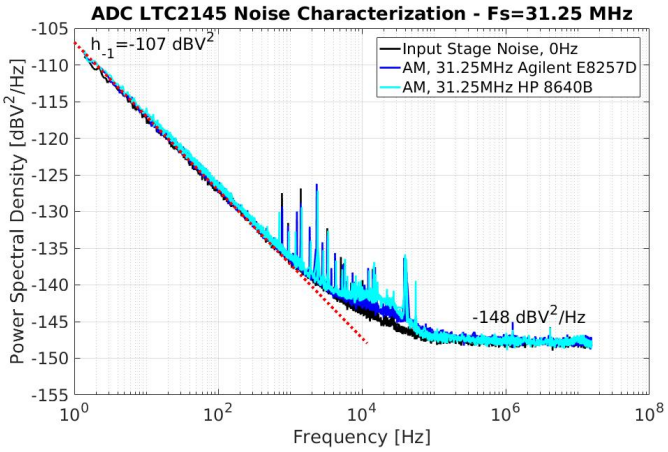


(b) PM and AM measurements comparison. Differential Mode – Channel 1.

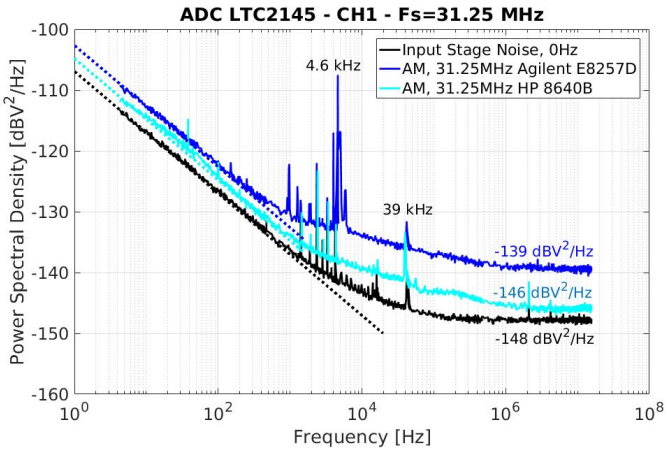
Fig. 3.9 a) The AM and PM noises are similar, suggesting that the input stage noise is equally distributed between the phase and amplitude noise. b) The zero-crossings and the maximum amplitude samples were well discriminated. While in zero-crossings is evidenced the feedback loop bandwidth (39 kHz), this contribution is not observed in maximum amplitude measurements.

Fig. 3.10 depicts the comparison between the amplitude noise estimated using two different synthesizers for generating the 31.25 MHz input sine-wave, the Agilent E8257D and the Hewlett Packard 8640B. From the differential mode results (Fig. 3.10b), it is seen that the harmonic contributions around

4.6 kHz were caused by the synthesizer and that although one induced a higher voltage error than the other, the common mode configuration rejects their contributions (Fig. 3.10a) reaching the ADC noise floor.



(a) AM in common mode.



(b) AM in single channel - Channel 1.

Fig. 3.10 ADC AM noise comparison using two signal generators. The amplitude noise generated by the ADC was estimated at the maximum amplitude points of the sine-wave input signal where the effects of this noise is higher.

In order to verify the impact of the voltage reference noise, first it was measured through a Fast Fourier Transform spectrum analyzer and afterwards it was compared with the estimated PSD of the amplitude noise. In order to perform properly this comparison, the transfer factor of this noise source on the ADC output was calculated adding an external sine-wave of 1 kHz to the internal voltage reference and measuring the impact on the ADC data for a

31.25 MHz, 0.9 V peak amplitude input signal. This measurement confirmed the equation stated in (2.12), where the transfer factor is 1. The comparison was done directly and the results are shown in Fig. 3.11. As can be seen, the voltage reference noise is lower than the voltage error generated by amplitude fluctuations in the input stage. The residual voltage reference noise of each channel after the common noise rejection is expected to be even lower and it seems not being a limiting factor for the ADC amplitude noise.

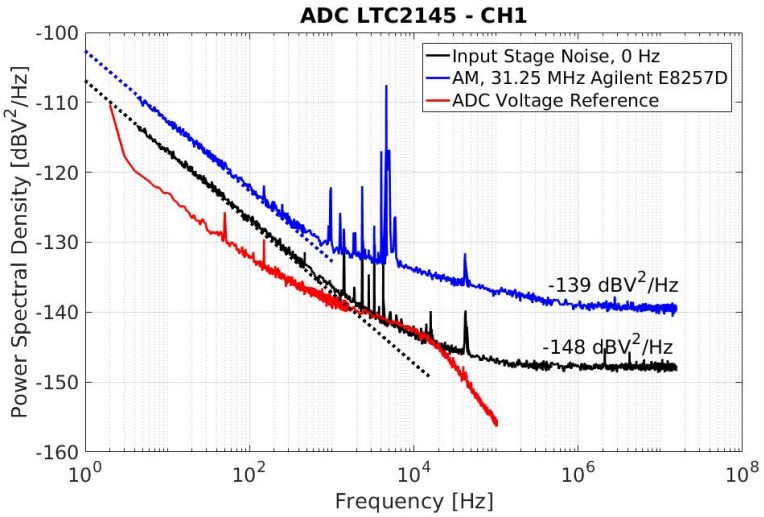
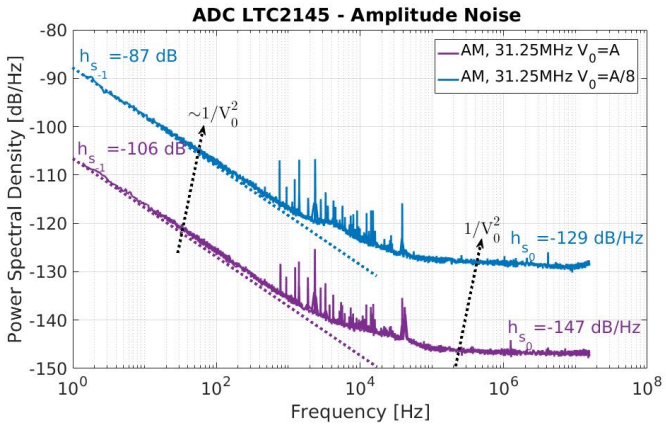


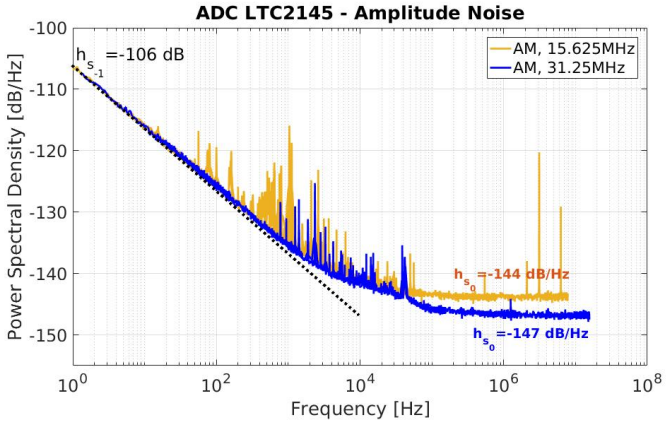
Fig. 3.11 Voltage Reference noise and its effect in single channel. It is seen that the amplitude noise generated by the input stage circuit is higher than this noise contribution and its effect is rejected in common mode.

Additionally, an analysis for assessing the properties of the ADC amplitude noise ($S_{\alpha,s}$) was performed, similar to the one reported for ADC phase noise. A first series of spectra were obtained by changing the input amplitude, from A (0.9 V) to A/8 (112.5 mV). From Fig. 3.12a it is seen that the amplitude noise is dependent on the input amplitude, as expected from the model (2.12). A second series of spectra were analyzed, this time changing the input frequency from 15.125 MHz to 31.25 MHz. For the analysis of AM noise the input frequency can not be increased beyond quarter the sampling clock in order to guarantee the acquisition of the peak values. Fig. 3.12b reports the PSD of the amplitude noise obtained. It exhibits the same behavior of the phase noise generated by the input stage. It confirms that the noise generated by the additive noise of

the input stage is independent of the operation point and its effects are similar on amplitude and phase noise.



(a) ADC Amplitude noise dependency with respect to input amplitude.



(b) AM noise dependency with respect to input frequency.

Fig. 3.12 ADC amplitude noise $S_{\alpha,s}$. In agreement with the ADC noise model, the ADC amplitude noise is dependent on the input amplitude and independent of the input frequency. The noise is dominated by the fluctuations generated by the additive noise of the input stage, which causes similar effects on the ADC phase and amplitude noise.

Interpretation of the ADC noise spectra

Table 3.1 reports the set of polynomial law coefficients that describes the ADC LTC2145 noise according to the model stated in (2.12) and based on the characterization results. These features can be compared with the performance

of other components, for instance with a generic analog mixer which has a flicker phase noise around -140 dBrad^2/Hz at 1 Hz [20].

Table 3.1 ADC Noise Model – Polynomial Law Coefficients. The boldface values indicate the input conditions at which each noise component was extracted.

Noise Source	**White Noise**	**Flicker Noise @1 Hz**
Phase Noise		
$S_{\varphi,s}(f) \approx \frac{1}{V_0^2} S_{n_\varphi,s}(f)$	$\mathsf{b}_{\mathsf{s}_0} = -153$ dBrad^2/Hz	$\mathsf{b}_{\mathsf{s}_{-1}} = -106$ dBrad^2
	$\boldsymbol{\nu_0 = 125}$ **MHz**	$\boldsymbol{\nu_0 = 125}$ **MHz**
	$\mathbf{V_0 = 0.9}$ **V**	$\mathbf{V_0 = 0.9}$ **V**
$S_{\mathsf{x},s}(f)$	$\mathsf{k}_0 = -350$ dBs^2/Hz	$\mathsf{k}_{-1} = -298$ dBs^2
	$\boldsymbol{\nu_0 = 500}$ **MHz**	$\boldsymbol{\nu_0 = 500}$ **MHz**
Amplitude Noise		
$S_{\alpha,s}(f) \approx \frac{1}{V_0^2} S_{n_\alpha,s}(f)$	$\mathrm{h}_{\mathrm{s}_0} = -148$ dB/Hz	$\mathrm{h}_{\mathrm{s}_{-1}} = -107$ dB
	$\boldsymbol{\nu_0 = 31.25}$ **MHz**	$\boldsymbol{\nu_0 = 31.25}$ **MHz**
	$\mathbf{V_0 = 0.9}$ **V**	$\mathbf{V_0 = 0.9}$ **V**
$S_r(f)$	$\mathrm{h}_{\mathrm{r}_0} = -156$ dB/Hz	$\mathrm{h}_{\mathrm{r}_{-1}} = -116$ dB
	$\boldsymbol{\nu_0 = 31.25}$ **MHz**	$\boldsymbol{\nu_0 = 31.25}$ **MHz**

However, since this work aims to extract the ADC information which allows predicting ADC noise effects on phase/amplitude noise metrology, more general parameters are required. Referring to the study of phase noise and jitter in digital electronics [63] and according to the model proposed here, Table 3.2 reports the main general ADC LTC2145 noise parameters obtained from the results shown in Table 3.1. Once these parameters are obtained $(\mathrm{h}_0\mathrm{B}, \mathrm{h}_{-1}, \mathsf{J}, \mathsf{k}_{-1})$, since they are generic values for this particular ADC, they can be used for re-estimating the ADC phase noise spectra and calculating the corresponding power law coefficients $(\mathsf{b}_{\mathsf{s}_0}, \mathsf{b}_{\mathsf{s}_{-1}})$ for an input signal of interest (ν_0, V_0, f_s). For instance if the noise of an oscillator of 10 MHz is intended to be measured, the ADC will have a phase noise floor given by $\mathsf{b}_{\mathsf{s}_0} = -153$ dBrad^2/Hz and $\mathsf{b}_{\mathsf{s}_{-1}} = -106$ dBrad^2. The aperture jitter will not limit the measurement having a phase noise given by $\mathsf{b}_{\mathsf{x}_0} = -194$ dBrad^2/Hz and $\mathsf{b}_{\mathsf{x}_{-1}} = -142$ dBrad^2.

Table 3.2 ADC noise parameters.

Parameter	**Square Root Value ADC LTC2145 Common Mode**
$h_0B = \frac{b_{s_0} f_s V_0^2}{2}$	$\sqrt{h_0B} = 159\ \mu V_{rms}$
$h_{-1} = b_{s_{-1}} V_0^2$	$\sqrt{h_{-1}} = 4.5\ \mu V$
$J^2 = \frac{f_s}{2} {k_0}^a$	$J = 25\ \mathrm{fs_{rms}}$
${k_{-1}}^b$	$\sqrt{k_{-1}} = 1.3$ fs

[a] $b_{x_0} = \frac{8\pi^2 {\nu_0}^2 J^2}{f_s}$
[b] $b_{x_{-1}} = 4\pi^2 \nu_0^2 k_{-1}$

In general, 10 MHz commercial low noise crystal oscillators exhibit phase noise floors below -110 dBc/Hz @1 Hz and -158 dBc/Hz white noise far from the carrier [72], therefore techniques for ADC noise rejection should be applied in order for the instrument not to limit the oscillator phase noise measurement. Based on the ADC characterization, the rejection level can be determined.

Furthermore, these parameters allow a straightforward comparison with analog components as amplifiers and mixers which are widely used in time and frequency applications. In Table 3.3 are reported the features of a generic mixer and a low noise operational amplifier.

Table 3.3 Parameters comparison

Parameter Phase Noise	**ADC LTC2145**	**Generic Mixer**	**Amplifier OPA354A**
$\sqrt{h_0}$	10 nV/$\sqrt{\mathrm{Hz}}$	3 nV/$\sqrt{\mathrm{Hz}}$	6.5 nV/$\sqrt{\mathrm{Hz}}$
	B = 250 MHz	5 - 10 MHz	B = 250 MHz
$\sqrt{h_{-1}}$	4.5 μV	0.1 μV	1.9 μV

Although, the ADC introduces higher noise, it can be handled and overcome through proper techniques (thanks to the noise characterization) while taking advantage of the benefits of using digital systems in time and frequency instrumentation.

3.3 PLL Noise Characterization

3.3.1 Implementation

The method proposed in Section 2.3 was implemented by using the phasemeter 5125A from Symmetricom (now Microsemi) as depicted in Fig. 3.13. The phasemeter measurement technique is based on the common noise rejection between the REF and the INPUT. In this manner, by using a sine-wave $v(t) = V_0 \cos(2\pi\nu_0 t)$ as common reference for both, the PLL and the phasemeter, the residual noise of the PLL is obtained by rejecting the noise of the REF.

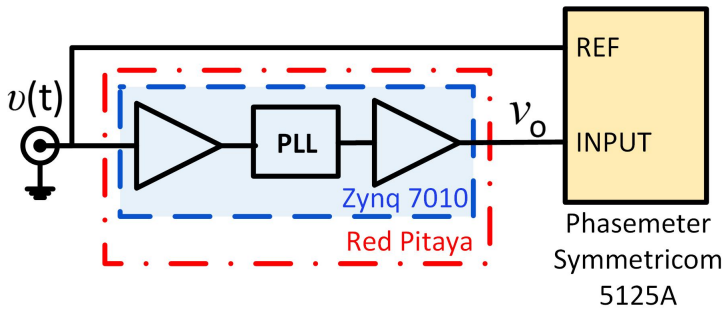


Fig. 3.13 Method implementation for PLL noise characterization.

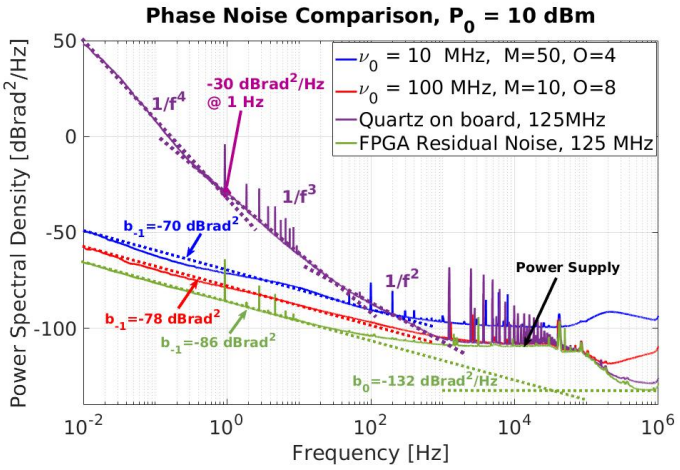
The PLL was configured for having the highest possible frequency at the input of the PFD ($D = 1$). Through the parameter M (refer to Section 2.3 for parameters description), the VCO was set to deliver a frequency close to 1 GHz for almost all the cases. In this manner, the noise analysis is performed under similar conditions for all the experiments, convenient for comparing results. Since the objective of characterizing the PLL noise is to verify its stability for generating the timebase of a digital system from a high-stability external reference, the output under test was fixed to 125 MHz that corresponds to the sampling and system clock (FPGA) used in Red Pitaya. It was done through the proper configuration of the parameter O. The different PLL configurations used for the experiments are reported in Table 3.4. Except when otherwise specified, the input power was set at 10 dBm ($V_0 = 1$ V).

Table 3.4 Set of PLL parameters configurations used for the phase noise characterization. The output frequency (ν_o) was configured for all the cases to 125 MHz.

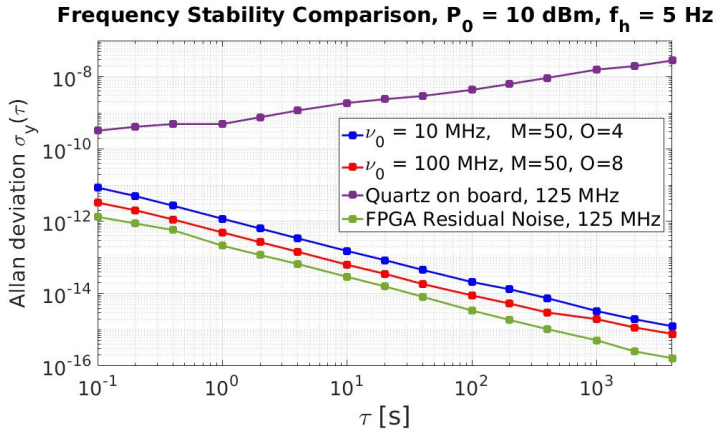
ν_0 [MHz]	**M**	**O**
10	50	4
20	50	8
40	25	8
80	11	7
100	10	8
125	8	8
160	7	9

3.3.2 Results

As first experiment, the improvement that can be achieved by using an external reference was quantified. Fig. 3.14 compares the spectrum of the phase noise (Fig. 3.14a) and the Allan deviation (Fig. 3.14b) of the on board crystal oscillator (violet) with the residual phase noise of the PLL driven by 10 MHz (blue) and 100 MHz (red) and with the residual noise of the FPGA when the PLL is bypassed (green). All the measurements were performed by using 10 dBm sinusoidal references ($V_0 = 1$ V) and by providing 125 MHz signals to the phasemeter. The phase noise at 1 Hz improved with respect to the oscillator on board from -30 to -70, -78 and -86 dBrad^2/Hz for the 10 MHz PLL, the 100 MHz PLL and the FPGA respectively. Similarly, the Allan deviation improved by 2-3 orders of magnitude at 1 s and by 7-8 orders of magnitude at 4000 s. This means, in case the PLL is locked to 10 MHz (the most diffused and, at the same time, the worst case) a residual frequency stability of 1.2×10^{-12} and 1.3×10^{-15} at 1 s and 4000 s respectively.



(a) Phase Noise Power Spectral Density.



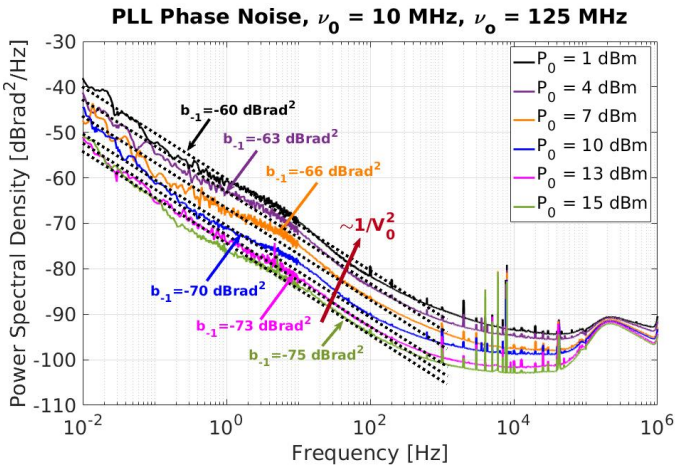
(b) Residual Frequency Stability. The measurement bandwidth f_h is 5 Hz.

Fig. 3.14 Noise Comparison. The system performance at frequency offsets close to the carrier improves in terms of phase noise by using an external reference and the internal PLL instead of the local oscillator.

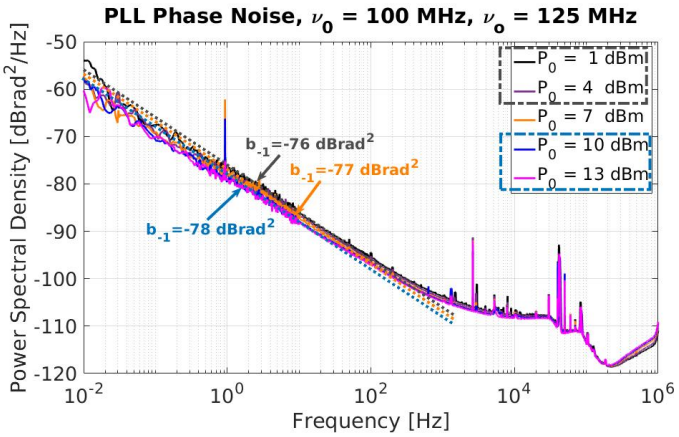
In the two experiments reported below, the contributions of $n(t)$ and $\mathsf{x}(t)$ were discriminated by changing the input slew rate: both input power and input carrier frequency were swept to vary this parameter.

First, the performance of the PLL regarding the input power P_0 was assessed for two reference frequencies. At $\nu_0 = 10$ MHz (Fig. 3.15a) the flicker phase noise of the PLL scales with the input power ($\sim 1/V_0^2$). It indicates that the noise is limited by the additive noise of the input stage having a phase noise inversely proportional to the input power. By using (2.18) we infer

that $\sqrt{\mathsf{h}_{-1}} = 25\ \mu V$. By contrast, for $\nu_0 = 100$ MHz (Fig. 3.15b) the noise is independent of the input power because of a significantly higher slew rate. It suggests that for higher frequencies the noise is dominated by the time fluctuations and therefore from (2.19) we can estimate the flicker component of $\mathsf{x}(t)$ that is $\sqrt{\mathsf{k}_{-1}} = 160$ fs.



(a) Input carrier frequency $\nu_0 = 10$ MHz.



(b) Input carrier frequency $\nu_0 = 100$ MHz.

Fig. 3.15 PLL as frequency multiplier. The input power dependency was assessed for two input carrier frequencies widely used as reference in time and frequency applications, 10 MHz and 100 MHz. Two different behaviors were observed. For $\nu_0 = 10$ MHz the PLL phase noise is dominated by the voltage noise of the input stage while for $\nu_0 = 100$ MHz the time noise generated by the propagation path is the one that dominates.

Finally, the slew rate was swept by changing the input frequency ν_0 in powers of two at a fixed amplitude $V_0 = 1$ V. The phase noise of the PLL

output is reported in Figure 3.16. At low ν_0, the noise improved by increasing the input frequency, according to (2.18), since the noise is dominated by the additive noise of the PLL input stage. Then, an asymptotic value is reached when the noise is dominated by the time noise according to (2.19). The cross-over frequency, $\nu_c = \frac{1}{2\pi V_0}\frac{\sqrt{h_{-1}}}{\sqrt{k_{-1}}}$, is 25 MHz for $V_0 = 1$ V that corresponds to a slew rate of 156 V/μs. The canonical form of the parameter b_{-1} induced by voltage noise and time noise [63] is observed when the noise is reported to the PLL input.

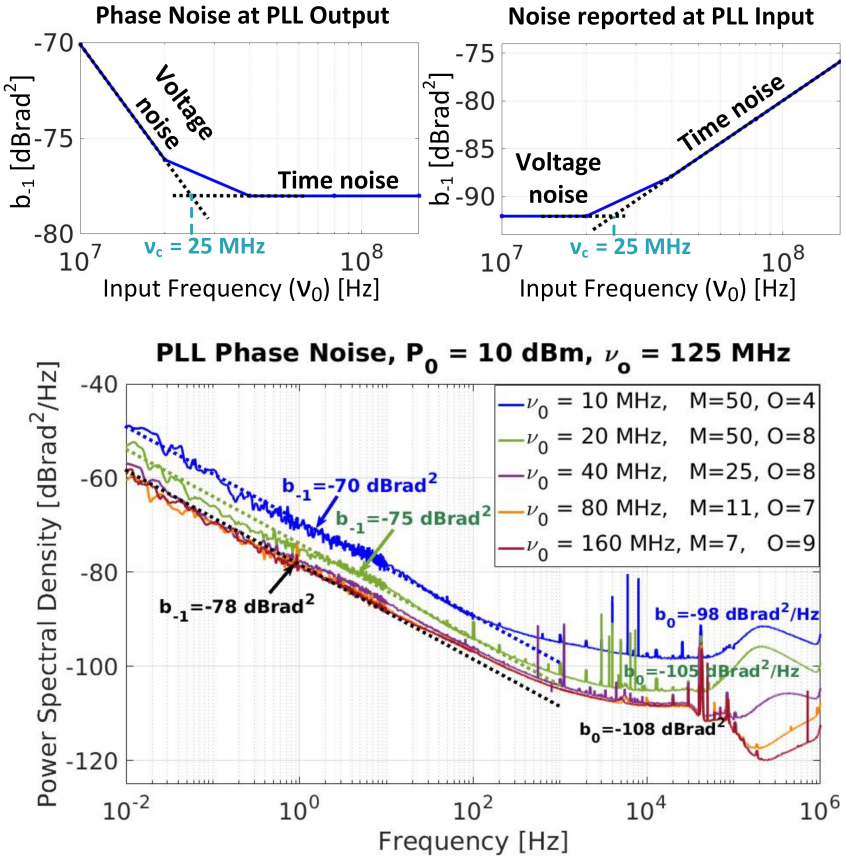


Fig. 3.16 For ν_0 higher than 25 MHz the PLL flicker phase noise is dominated by the time noise induced by the delay on the propagation path.

Interpretation of PLL noise spectra

Table 3.5 reports the parameters, $\sqrt{h_{-1}}$ and $\sqrt{k_{-1}}$, obtained from the phase noise spectra by using the noise model stated in (2.18) and in (2.19). With this

information the phase noise effects of the PLL under different conditions can be predicted.

Table 3.5 PLL noise parameters.

Parameter	**Square Root Value PLL Zynq 7010**
$\mathrm{h}_{-1} = \frac{\nu_0^2 V_0^2}{\nu_o^2}\mathsf{b}_{-1}$, $\nu_0 < \nu_c$ [a]	$\sqrt{\mathrm{h}_{-1}} = 25\ \mu V$
$\mathsf{k}_{-1} = \frac{1}{4\pi^2\nu_o^2}\mathsf{b}_{-1}$, $\nu_0 > \nu_c$	$\sqrt{\mathsf{k}_{-1}} = 160$ fs

[a] $\nu_c = \frac{1}{2\pi V_0}\frac{\sqrt{\mathrm{h}_{-1}}}{\sqrt{\mathsf{k}_{-1}}}$

For instance, if a 250 MHz output frequency is intended to be generated from a 10 MHz reference with $V_0 = 1$ V, the flicker phase noise expected will be around -64 dBrad^2/Hz at 1 Hz. If instead of the 10 MHz, a reference of 100 MHz is used, the flicker will be around -84 dBrad^2/Hz at 1 Hz. Then, the proper reference may be selected according to the application requirements. Although this noise is higher with respect to the ADC previously characterized (3.2), some application could tolerate it while using the advantages of having the synthesizer embedded in the digital system.

3.4 DAC Noise Characterization

3.4.1 Implementation

The method proposed for characterizing the DAC phase noise (Section 2.4.2) was implemented in the Red Pitaya platform as depicted in Fig. 3.17). The digital phasemeter used was the phasemeter 5125A from Symmetricom (now Microsemi) that implements a measurement technique based on the common noise rejection and direct comparison between the phases of the REF and the INPUT. In this manner, the common noise contributions such as the ones coming from the FPGA and the oscillator are rejected, obtaining only the noise of the DAC.

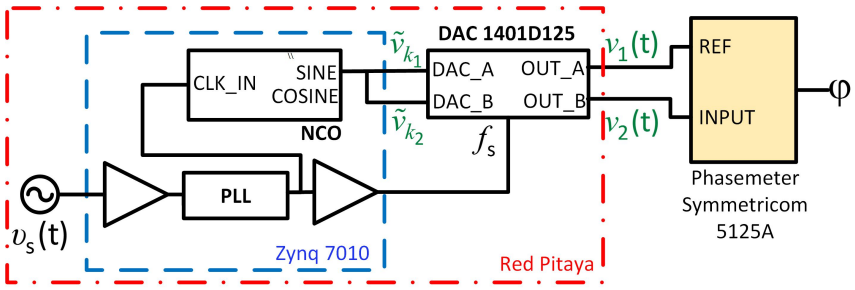


Fig. 3.17 DAC phase noise characterization. Method implementation by using the Red Pitaya platform.

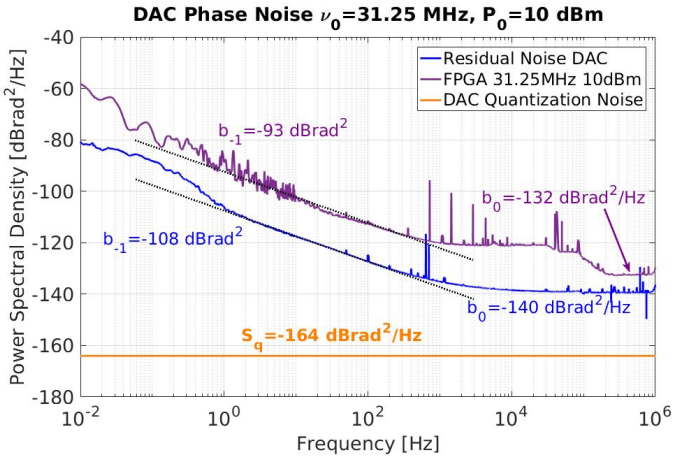
The NCO was configured with an output resolution of 14 bits in order to suit the resolution of the DAC without the need of additional truncation. The sampling clock used was the on board quartz at 125 MHz provided by the platform. The embedded PLL is required because the DAC works in interleaved mode; therefore it takes one data each 4 ns (250 MHz) sampling each channel at a frequency of 125 MHz. The peak amplitude of the DAC outputs were configured at 1 V (10 dBm).

3.4.2 Results

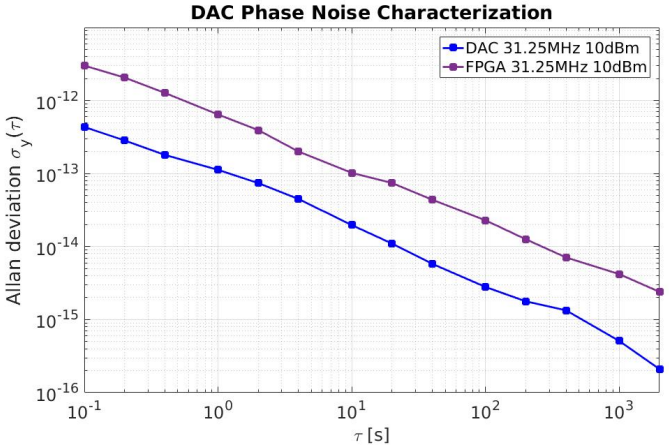
The characterization of the DAC of the Red Pitaya platform was not as extensive as the ADC or PLL characterization. The reason is that the application that is intended to be implemented in this platform is not based on the DAC operation, i.e., the noise of the DAC is not a limiting factor. However, a preliminary measurement was performed in order to validate the method and the results are reported here.

Fig. 3.18 shows the results of the measurement performed with the NCO configured for generating a sine-wave of 31.25 MHz, quarter the sampling frequency. Fig. 3.18a compares the power spectral densities of the theoretical quantization noise, the residual phase noise of the DAC and the phase noise of the FPGA acting as a buffer. From this measurements the assumption that the quantization noise is lower than the other noise contributions is verified. Additionally, the FPGA noise rejection was also verified. The DAC exhibits a white phase noise of -140 dBrad^2/Hz and a flicker phase noise of -108 dBrad^2/Hz at 1 Hz for a carrier of 31.25 MHz. From Fig. 3.18b we obtained that the DAC

exhibits a residual frequency stability of 1.12×10^{-13} at 1 s. These results provide a general view of the phase noise of this DAC.



(a) Phase Noise Comparison. The quantization noise of the DAC is shown in dBrad^2/Hz.



(b) Frequency Stability Comparison. Measurement bandwidth $f_h = 5$ Hz

Fig. 3.18 Comparison between: DAC residual noise, measured in differential mode. Absolute DAC noise, measured DAC vs PLL2 output. And the FPGA residual noise used as a buffer. All the measurements were done at 31.25 MHz and 10 dBm input power.

3.5 Discussion of the Obtained Noise Spectra

The noise model and methods for the characterization of the critical components for the implementation of a digital instrument for time and frequency applica-

tions were validated in the Red Pitaya platform. The results were consistent with the datasheet information (if available). Based on such results, not only the ultimate performance of the platform is known but also the noise introduced by each single component. It means that, the performance of different instrument working with any of these components will be known as well.

Since not all applications may be limited by the same components, these results also allow focusing on the critical effects in order to manage them efficiently.

3.6 Perspectives: Assessment of a Higher Performance Platform

Currently, a higher performance platform is under assessment by applying the tools and concepts developed along the PhD. The platform is based on the Zynq 7045 SoC from Xilinx (ZC706) and cutting edge converters are used: a dual-channel, 14-bit, 1 GSps ADC and a quad-channel, 16-bit, 2.8 GSps DAC. The purpose of this project is the development of a state of the art phasemeter based on the digital implementation of the tracking DDS approach [73] whose operation may be limited by the DAC noise and the communication speed between the components. In order to estimate the ultimate performance of the instrument, the DAC characterization is under development and preliminary measurements of its residual noise are reported.

3.6.1 Platform Overview

The phasemeter under research is being implemented by using the platform ZC706 [74] from Xilinx and the evaluation board AD-FMCDAQ2-EBZ [75] from Analog Devices, as depicted in Fig. 3.19. The latter contains the analog to digital and digital to analog converters, providing two analog inputs and two analog outputs sampled at 1 GSps. The data are processed at 250 MHz by means of the Zynq 7045 SoC, core of the ZC706 platform. The communication between the two boards is performed through the protocol JESD204B [76], a standard interface for high speed data converters that implements a serial

communication based on multi-lane with a maximum lane rate of 12.5 Gbps (Giga bits per second). With this feature the phasemeter operation is expected not to be limited by the communication speed.

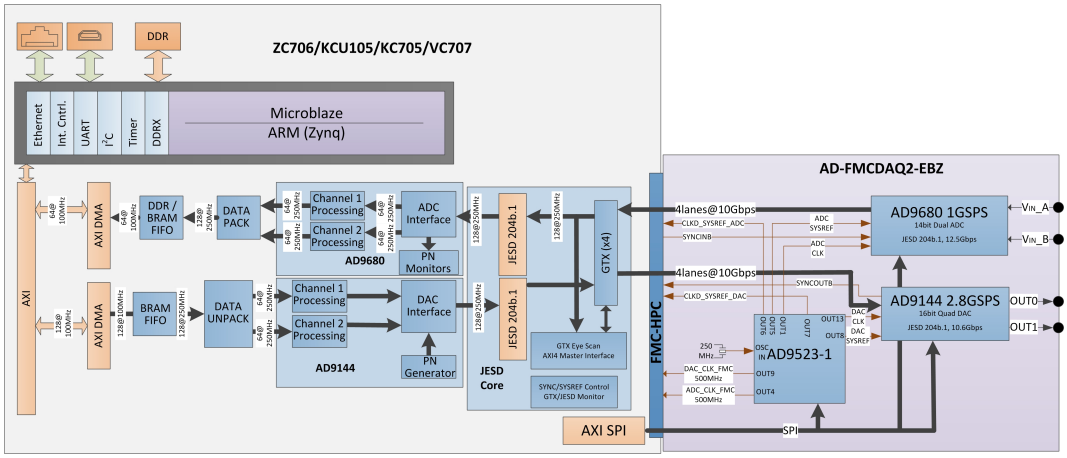


Fig. 3.19 Higher performance platform overview.

The first stage of this project is focused on the characterization of the front-end devices: ADCs and DACs. Since the technique that is intended to be implemented for phase noise measurement is based on the DACs operation, it is the first component that is being characterized in order to evaluate the implementation feasibility.

3.6.2 Preliminary Results

The DAC was characterized by using the Symmetricom 5125A and applying the method proposed for DAC noise characterization in Section 2.4.2. The DAC was fed with a sine-wave generated by a Numerically Controlled Oscillator (NCO) configured in the FPGA. Since this instrument implements a phase noise measurement technique based on common noise rejection, the two available DAC outputs were connected to the phasemeter (IN and REF) thereby extracting the residual noise of the DAC.

Fig. 3.20 shows spectrum of the DAC phase noise. It exhibits the signature of pure time-type (x-type) noise, scaling at the flicker region proportionally with ν_0^2 and in the white region proportionally to ν_0, according to the noise model described in Section 2.4.1. The DAC phase noise is of -113 dBrad^2/Hz

at 1 Hz (flicker) and -158 dBrad^2/Hz at frequency offsets far from the carrier (white) for a 62.5 MHz input signal. Its performance is comparable with low noise Direct Digital Synthesizers (DDSs) commonly used in time and frequency instrumentation (AD9854) that is of the order of -126 dBrad^2/Hz at 1 Hz and -159 dBrad^2/Hz far from the carrier clocked at 180 MHz for generating a signal of 5 MHz.

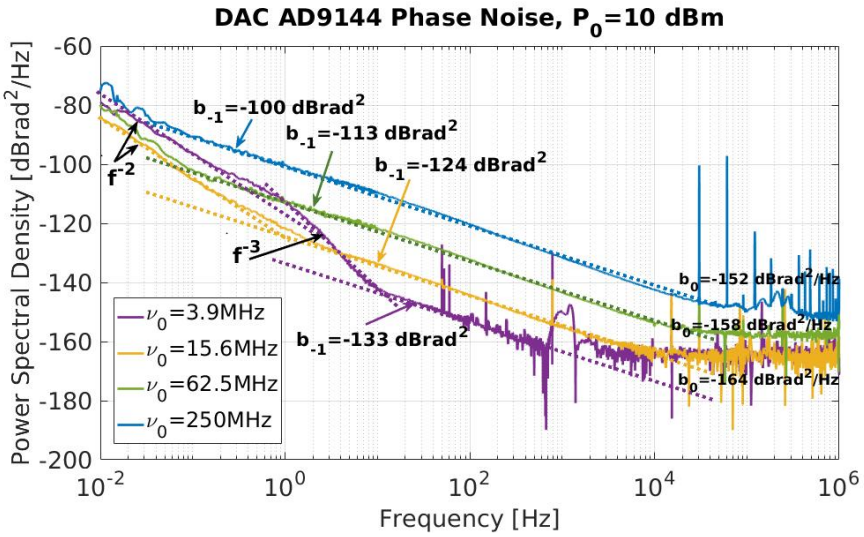


Fig. 3.20 Phase Noise Power Spectral Density of the DAC AD9144 at different input frequencies.

Table 3.6 reports the parameters of the model extracted from this characterization, obtaining a rms jitter (J) of 0.18 ps. Since the phase noise is dominated by the time fluctuations introduced by the sample and hold, the parameters related to the voltage fluctuations of the output stage can not be extracted from these measurements. Therefore a different configuration should be implemented in order to reveal $n(t)$ and thereby to have a complete description of the device. However, the results reported here provide a general view of the DAC performance and allow its assessment for time and frequency applications.

Table 3.6 DAC noise parameters.

Parameter	**Square Root Value AD9144**
$\mathsf{J}^2 = \mathsf{k}_0{}^a \frac{f_s}{2}$	$\mathsf{J} = 0.18$ ps
$\mathsf{k}_{-1} = \frac{1}{4\pi^2\nu_o^2}\mathsf{b}_{-1}$	$\sqrt{\mathsf{k}_{-1}} = 5.7$ fs

[a] $\mathsf{k}_0 = \frac{b_0}{4\pi^2\nu_0{}^2}$

Fig. 3.21 reports the fractional frequency stability of the DAC. From these results it is observed that the stability improves by using higher input frequencies and it is around 2×10^{-14} at 1 s for $\nu_0 = 250$ MHz.

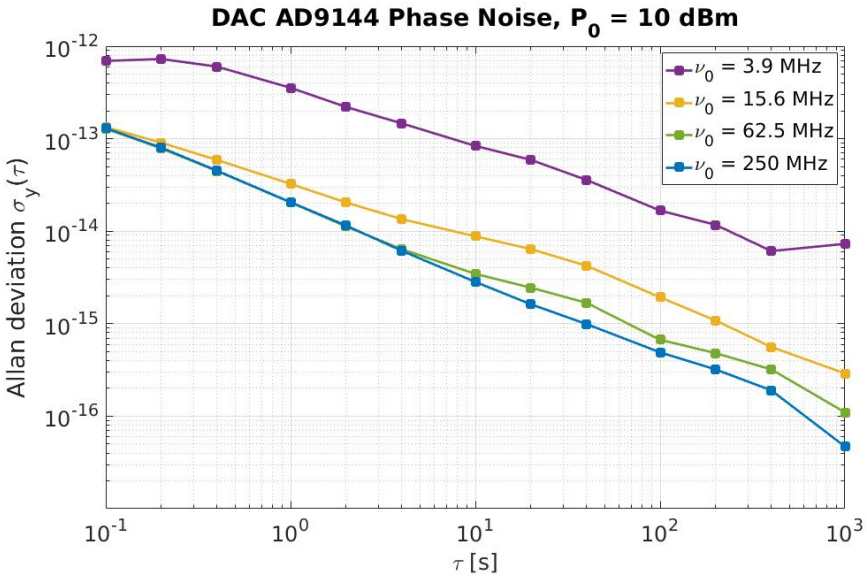


Fig. 3.21 Fractional frequency stability of the DAC AD9144 at different input frequencies. Measurement bandwidth $f_h = 5$ Hz

Chapter 4

Application: Fiber Link

Recent improvements on accurate clocks and frequency standards require the study of suitable techniques for frequency transfer that minimize the added noise and allow fully exploiting these clocks in metrology applications. Different experiments performed during the last decades validated fiber links as the most performing tool for frequency transfer. However, mechanical and temperature stresses generate fiber length variations and therefore phase fluctuations that must be compensated in order not to degrade the clock information. In this chapter, a digital instrument for the detection and compensation of the phase noise induced by the fiber is proposed. The implementation of such a system is performed in the Red Pitaya platform. Based on the characterization results reported in the previous chapter, it is expected a limitation in the phase noise measurement given by the PLL that presents a fractional frequency stability of about 10^{-12} at 1 s. Thanks to the leverage between RF and optical frequencies, the instrument is expected to affect the fiber link performance at a level below 10^{-18} at 1 s.

Further assessments of the implementation feasibility are presented here from the analysis of the main blocks design. They are focused on determining the proper data resolution (bits) and the FPGA resources utilization.

Preliminary results of the system operation are reported together with an analysis of the noise introduced by the digital instrument. From these results, the ultimate performance of the instrument in terms of noise is verified.

4.1 Frequency Transfer Using Fiber Link - State of the Art

The progress achieved on optical clocks along the last years, allows reaching frequency stability in the 10^{-18} range [11, 77, 78]. This tremendous stability is exploited not only in metrology applications such as relativistic geodesy [79, 80] and radio astronomy: Square Kilometer Array Telescope [81], VLBI [82], but it is also of particular interest for fundamental physics for instance for verifying the variations of fundamental constants [83, 84] and for testing and validating Einstein's theory of general relativity [85]. The applications previously mentioned involved the comparison of ultra-stable optical clocks that are generally not collocated. Then, it becomes necessary to apply methods for time and/or frequency transfer. The traditional techniques, based on Global Navigation Satellite System (GNSS) exhibit a stability of the order of 10^{-16} [86]. Although this is the method currently used for comparing frequency standards (based on atomic clocks) around the world, it is not suitable for time and frequency transfer using optical clocks.

Optical fibers, on the other hand, are environmentally isolated and therefore more stable than free space medium. The capability of optical fiber links for reaching stability levels lower than 10^{-17} has been demonstrated through different experiments [87–91], fact that has encouraged the use of this medium for ultra-stable frequency transfer and dissemination [92, 93]. The stability of this configuration is limited mainly by the length variations of the fiber due to mechanical stress, temperature and other environmental factors which induces phase noise. Such a noise should be detected and subsequently compensated in order not to degrade the clock stability [94].

In this regard, different techniques exist: the classical, Doppler compensation [87, 95] and the more recent, two-ways cancellation [96]. The general scheme of the Doppler compensation technique is shown in Fig. 4.1. The two ultra-stable signals L1 and L2 are located at different laboratories and they are transmitted to the remote user through two parallel bidirectional fibers (from laboratory 1 to laboratory 2 through Link 1 and from laboratory 2 to laboratory 1 through Link 2). The phase noise introduced by the fiber is detected by comparing the transmitted frequency (original signal) with a part of itself that

is returned back from the remote end on the same fiber. The returned signal is affected by twice the phase noise of the fiber, under the assumption that the phase noise induced by the incident and the return trip on the fiber are equal. In order to distinguish the returned signal from parasite reflexions, two acousto-optic modulators (AOMs) are added along the transmission path, at the local and remote sides, which introduce a known frequency offset to the signal at each pass. The beat note between the transmitted signal and its round trip is then detected through a photo-detector (PD). The phase error φ_e extracted from the beat note is actively compensated (φ_c) by acting on AOM at the local side. A second phase detector is added at each side for monitoring purposes. In this manner, the phase error between the transmitted and the received signals is detected (φ_m), i.e., between L1 and L2.

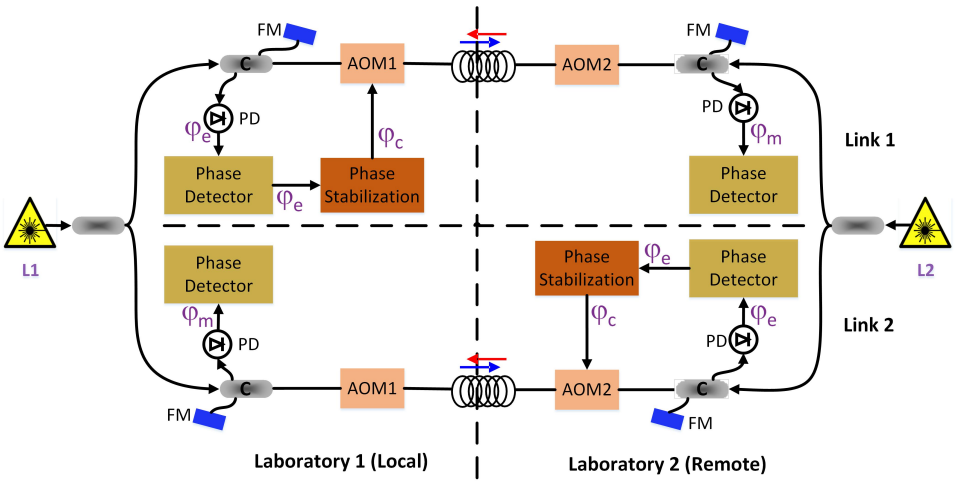


Fig. 4.1 General scheme of doppler compensation technique. FM (Faraday Mirror), C (Coupler or Power Splitter), PD (Photo detector).

For performing a proper phase noise compensation the following considerations are done [94]. The phase noise induced by the incident and the return trip on the fiber are assumed equal. It means that the processes involved in the generation of such a noise are considered stationary. In order to guarantee this assumption, the polarization on the fiber should be maintained for avoiding amplitude fluctuations in the beat detected. Furthermore, the coherence time of the signal being transmitted should be longer than twice the single pass delay δ on the fiber. In this manner, the signal will be phase coherent with the returned phase thereby assuring a proper phase noise cancellation. Considering

that the typical coherence time for optical frequencies ($\tau_c = \frac{1}{\Delta\nu}$) is much lower than few milliseconds, depending on the linewidth ($\Delta\nu$) of the source [97], and that the delay δ on the fiber is proportional to the fiber length as $\delta = \frac{nL}{c}$, where n is the refraction index (1.5 for glass), c is the speed of light in vacuum (299.792.458 m/s) and L is the fiber link length in meters, particular attention should be paid in order to satisfy this condition especially in the case of long fiber link configurations. Another important consideration is the additive noise generated by the photo-detection which induces excess of noise in the measurement. Generally, this noise is removed by means of a low pass filter whose bandwidth is of the order of hundreds of hertz.

In the case of the two-way compensation technique, the phase noise induced by the fiber is extracted through a single trip of the signal on the fiber. The two signals L1 and L2 (refer to Fig. 4.1 since the setup is similar for this technique) are sent in opposite directions towards the remote user. The received signal is compared with the local one and the phase noise introduced by the fiber is passively canceled by post-processing (open loop configuration) through synchronous measurements between the two ends. In this configuration the phase stabilization block is not needed. However, the fiber noise could be actively compensated through a closed loop configuration where the phase noise that represents the length variations is detected, similarly to the Doppler compensation technique.

The differences between these two approaches are related to the time delay of the signal traveling on the fiber. While in the two-way technique it is only δ, in the Doppler compensation it is 2δ (round trip). This defines the parameters for the bandwidth of the phase detector and the phase stabilization blocks. It also determines the limit for the coherence time of the transmitted signal. The main advantage of the two ways compensation is that the system is less affected by optical looses since the signal travels only once through the fiber. However, synchronization between the local and the remote ends is required in order to properly cancel the noise [96].

The traditional analog implementation for the detection and compensation of the phase noise generated by the fiber is depicted in Fig. 4.2. The noise introduced by the fiber is detected through a tracking VCO that cleans up the beat note, reducing the excess of noise due to the photo-detection and

amplification, and a frequency divider that increases the dynamic range of the mixer. Afterward, a servo (main servo) compensates for the noise by acting on the frequency that drives the Acousto-Optic Modulator (AOM). In order to monitor and to acquire the phase information, a phasemeter is required.

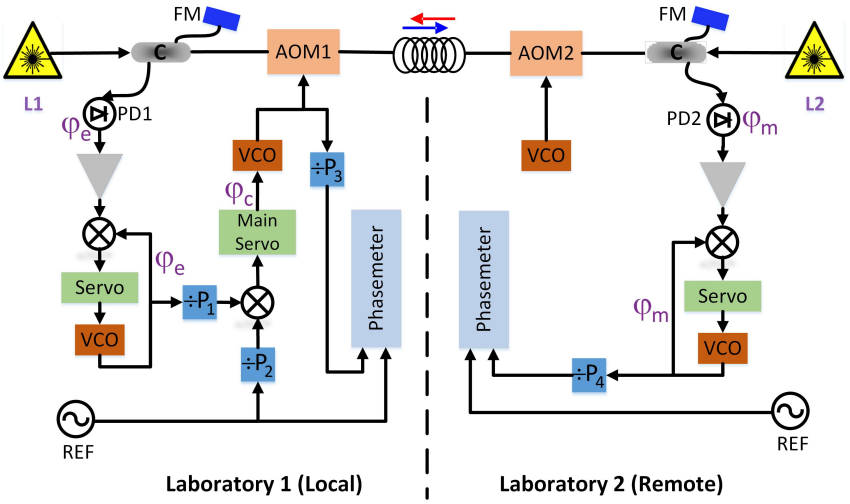


Fig. 4.2 Analog implementation for fiber phase noise detection and compensation. Only one fiber is shown since the implementation on both fibers is symmetrical. FM (Faraday Mirror), C (Coupler or Power Splitter), PD (Photo Detector), VCO (Voltage Controlled Oscillator), P (Frequency Divider)

This kind of configuration was demonstrated to work well [98, 13]. However, it has low flexibility and it is not predisposed naturally for efficient reconfiguration, monitoring and remote operation.

The advantages of a digital implementation on coherent fiber links were demonstrated, for the first time, by C. E. Calosso et al., in [73]. There, the approach is based on the Tracking Direct Digital Synthesizer (Tracking DDS) technique, which detects the fiber phase noise directly. Fig. 4.3 depicts the Doppler compensation method using the Tracking DDS approach. A first DDS tracks the phase of the beat note and retrieves the fiber link noise. Then, a servo (Main Servo) compensates for it by correcting the phase of a second DDS that drives the AOM.

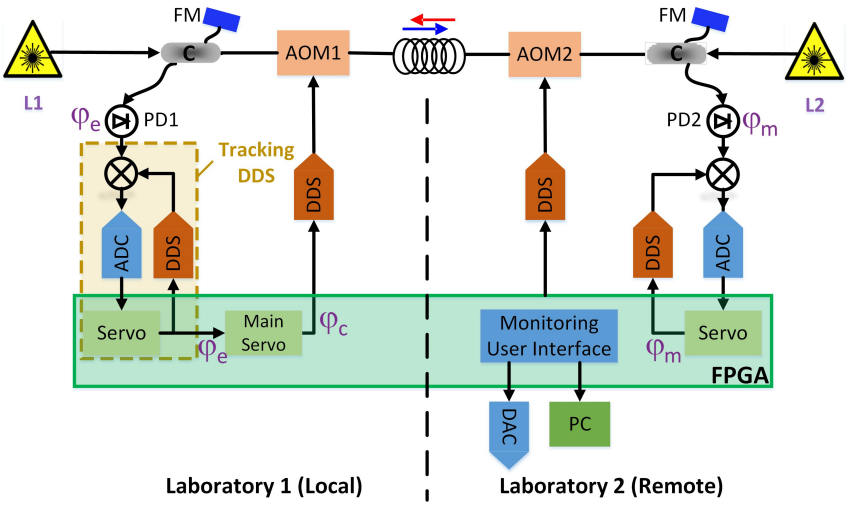


Fig. 4.3 Doppler compensation implementation using the Tracking DDS approach.

The flexibility of this system allowed demonstrating, a 6 dB improvement of the unsuppressed noise limit and the two-ways scheme, by only software reconfigurations and data realignment in post-processing [95]. The system was usable only up to hundred of kilometers, limited by the serial communication of the DDS. For extending its usability to thousand-kilometer link it is necessary to increase the tracking bandwidth from 20 kHz to the megahertz region; that means to redesign the board with parallel communication components.

In this project, a digital implementation for the detection and compensation of the phase noise induced by the fiber is proposed. The beat note, representing the fiber length variations, is acquired directly with a high speed ADC followed by a fully digital phase detector. This configuration reduces the components latency and the communication delay between different blocks, increasing the detection bandwidth to 10 MHz. The detection bandwidth of current analog systems is of the order of 100 kHz and it represents a limiting factor for long links, because it induces cycle slips in the phase measurement. A wider detection bandwidth allows extracting the phase information before the coherence of the sinusoid is destroyed by the phase modulation induced by the fiber noise. In this regard, a thousands kilometers link requires 1 MHz of detection bandwidth. It is worth to note that this wide detection bandwidth is advantageous not only for fiber links, but in general for time and frequency metrology in the optical domain.

4.2 Proposed Digital System: Considerations and Design

4.2.1 General Description

The system proposed here is based on the Tracking DDS scheme (Fig. 4.3). In this implementation, the tracking DDS is replaced by a fully digital phase detector that follows a high speed, high resolution ADC, as depicted in Fig. 4.4. Moreover, the DDSs that drive the AOMs are substituted by Numerically Controlled Oscillators (NCOs) followed by high speed and high resolution DACs. Hence, the beat-note that represents the fiber length fluctuations is acquired by the ADC and detected by the digital phase detector. The servo corrects this phase error by controlling the phase of the NCO that drives the AOM.

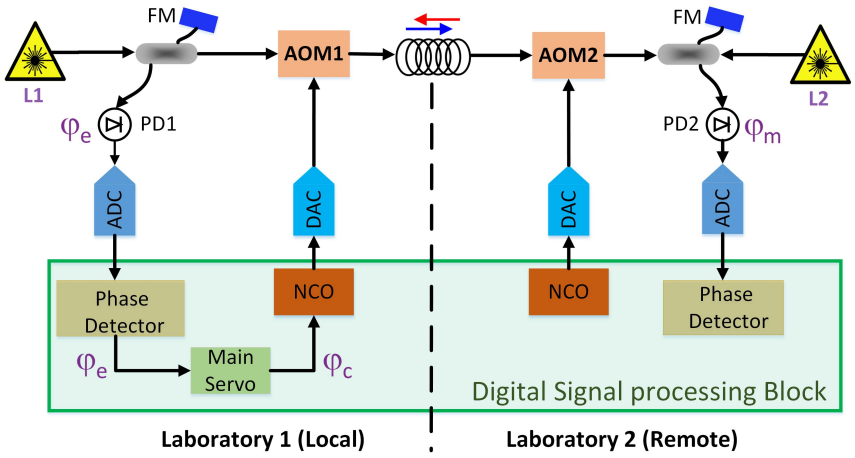


Fig. 4.4 General scheme of the proposed system for the detection of the noise introduced by the fiber in applications for frequency transfer.

The implementation of the system is performed on the Red Pitaya platform that provides the hardware required: a dual channel, 14-bit, 125 MSps ADC, dual channel, 14-bit, 125 MSps DAC and a SoC (see Section 3.1 for further details). Additionally, based on the characterization results, the noise limitations of the platform are known and therefore considerations for the system design can be performed.

The system timebase and the input signals (L1 and L2) are referred to a common high stability oscillator (generally a Hydrogen Maser). Therefore, the hardware of Red Pitaya was modified in order to allow the generation of the 125 MHz system clock from an external reference (Fig. 4.5). This is performed by using one of the two PLLs provided by the FPGA. Although the platform provides an optional input for an external 125 MHz signal, standard references are available at 5 MHz, 10 MHz and 100 MHz; therefore, the use of the PLL is convenient for this implementation (see Section 3.3).

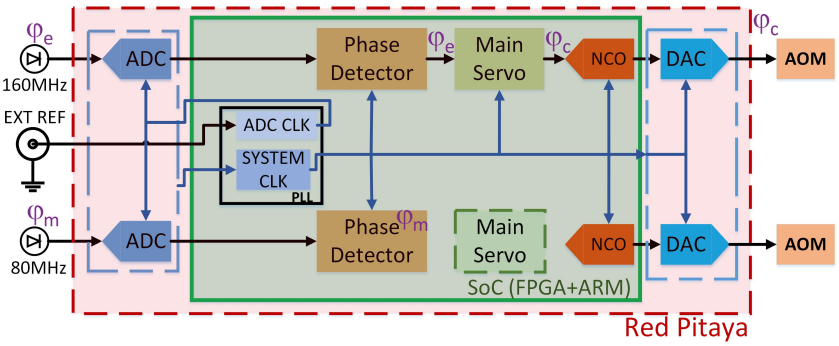


Fig. 4.5 Detailed scheme of the digital system. The system timebase and the input signals are referred to an external low noise reference.

The phase noise measurement is expected to be limited by the PLL that exhibits a fractional frequency stability of about 10^{-12} at 1 s when the frequency and power of the reference are 10 MHz and 10 dBm, respectively, according to the results presented in Section 3.3. Thanks to the leverage between RF and optical frequencies, the system is expected to affect the fiber link performance at a level below 10^{-18} at 1 s. The phase noise introduced by the fiber [99] is higher than the noise contributions of the ADC and DAC; therefore these components will not have an impact on the measurement in terms of noise.

Two different approaches for the implementation of the phase detector were tackled: Tracking NCO and I/Q phase detector. Both approaches were implemented in order to study their limitations in terms of delay and FPGA resources utilization; thereby verifying the entire implementation feasibility. In the first approach some limitations were found which prevented the actual implementation. Hence, the second approach was investigated and implemented.

In the following sections, the different blocks that conform the system are described. Furthermore, the design considerations and the implementation choices are reported.

4.2.2 Numerically Controlled Oscillator - NCO

The NCO implemented here is based on the DDS IP core provided by Xilinx [100], depicted in Figure 4.6. The principle of operation of this block relies on a phase accumulator that at each rising edge of the system clock (clk), and from a given phase increment ($\Delta\theta$) generates the phase information θ(n) with a resolution of B_θ bits. An optional adder is also provided whether a phase offset is required.

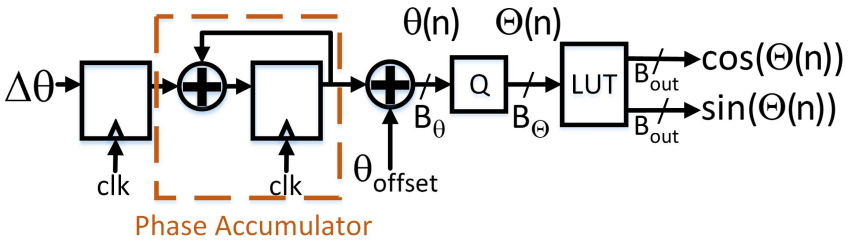


Fig. 4.6 Block diagram of Numerically Controlled Oscillator - IP from Xilinx.

Hence, one period of system clock that corresponds to a circumference of 2π is divided in small pieces of $1/2^{B_\theta}$ and it is swept in steps equal to $\Delta\theta$. The phase $\theta(n)$ is then converted into amplitude through a SINE/COSINE Look Up Table (LUT) in order to obtain the desired output signal. However, the resolution of the phase accumulator provided by this implementation is high (the maximum value of B_θ is 48 bits) thus, this conversion might require a huge LUT (2^{48} of depth) which is not feasible in terms of resources utilization. Therefore, $\theta(n)$ is properly truncated using optimization algorithms and taking advantage of the symmetry of sinusoidal signals, obtaining $\Theta(n)$ at the input of the LUT. The design parameters are the resolution of the output amplitude or output signal (B_{out}) and the resolution of the phase accumulator (B_θ).

The output frequency is generated from the system clock as stated in (4.1). The NCO provides two outputs at the same frequency with a phase shift of $\pi/2$, i.e., a pair of sine and cosine output signals.

$$f_{out} = \frac{\Delta\theta f_{clk}}{2^{B_\theta}} \tag{4.1}$$

The configuration of the NCO depends of the application requirements. For our system implementation, this component is used for two purposes: phase detection and for driving the AOM. In the first case, as it is explained in more detail in Section 4.2.4, the phase is detected by extracting the quadrature (Q) and in-phase (I) components of the input signal. This is done by multiplying the input signal by a sine and a cosine at the same frequency. Therefore, in this case the two outputs of the NCO are required, while the phase offset remains optional whether tuning is required. For this case the resolution of the output is configured taking into account that the effective number of bits (ENOB) of the ADC is 11.8 (Section 3.2.2). Hence, in order not to degrade the information acquired by the ADC, an output resolution (B_{out}) of 14 bits is set, the same of the ADC nominal value.

On the other hand, for driving the AOM (second case) only one of the two outputs is needed. The phase offset input is connected to the servo that provides the proper phase correction. In this case, the DAC resolution is the feature that sets B_{out}. Since a 14-bit DAC is used here, the output is also configured at 14 bits.

The resolution of the phase accumulator is configured at the maximum value, 48 bits, in order to have the maximum output frequency resolution for the two cases. Since one of the main concerns is the FPGA resources utilization, further configurations such as optimization algorithms, modes of operation and extra pins enable were performed in order to minimize the amount of FPGA resources required for the implementation.

4.2.3 Servo

The design of the servo for controlling the phase error introduced by the fiber is based on the scheme depicted in Fig. 4.7. The controller performs a Proportional and Integrative (PI) action over the phase error extracted by the phase detector. In order to obtain the phase correction at the output, an additional accumulator is performed. The parameter *gain* is the global gain of the controller and *i_gain* is related to the time constant of the PI

integrative part. Through a command of 8-bits the configuration of the servo can be modified in order to: change the loop sign ($sign$), disable or enable the proportional action (p_en), disable or enable the integrative action (i_en) and enable or disable the entire controller (cl, $reset$). This is useful for testing and setup purposes.

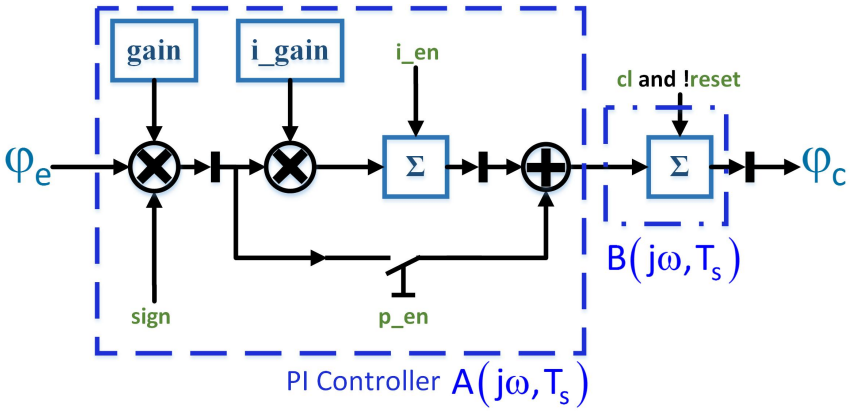


Fig. 4.7 Description of the digital controller. The proportional and integrative actions of the PI controller can be enabled independently through the inputs p_en and i_en respectively, while cl resets the accumulator when its state is low.

The discrete-time controller is described in the z-plane by using the Forward Difference approximation [101], which states that the current digital value of a certain output depends only on past values either of the output and the input, yielding to $s = \jmath\omega \approx \frac{z-1}{T_s}$. Then, the summation that in continuous time is equivalent to an integral, is represented in the z-plane as: $1/s \approx \frac{T_s}{z-1}$. The transfer function of the servo $C(z)$ is then:

$$C(z) = gain\left(1 + i\_gain\frac{T_s}{z-1}\right)\left(\frac{T_s}{z-1}\right) \tag{4.2}$$

In order to state the controller requirements in terms of the parameters $gain$ and i_gain, the analysis of the digital controller in the frequency domain is performed based on the analog controller frequency response. The transfer function of the digital controller is expressed as $C(\jmath\omega, T_s) = A(\jmath\omega, T_s)\, B(\jmath\omega, T_s)$, where T_s is the sampling period or the observation time of the analog systems $C(\jmath\omega)$, $B(\jmath\omega)$ and $A(\jmath\omega)$. The transfer functions of $A(\jmath\omega)$ (analog PI) and $B(\jmath\omega)$ (analog integrator) are:

$$A(j\omega) = K_p\left(1 + \frac{1}{j\omega\tau_i}\right) \qquad B(j\omega) = \frac{1}{j\omega} \tag{4.3}$$

Thus, the transfer function of the analog controller is given by (4.4), where K_p corresponds to the global gain of the controller and τ_i sets the time constant of the integrative action of the PI.

$$C(j\omega) = K_p\left(1 + \frac{1}{j\omega\tau_i}\right)\left(\frac{1}{j\omega}\right) \tag{4.4}$$

The block diagram of the entire system including the system to be controlled, $G(j\omega)$, and the system transducers, $H(j\omega)$, is presented in the Fig. 4.8.

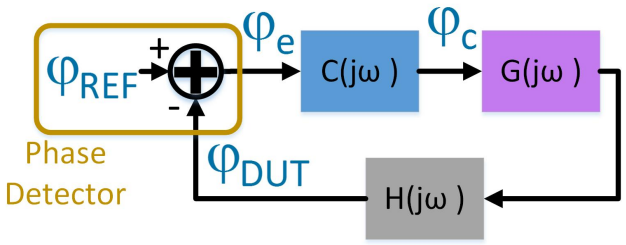


Fig. 4.8 Block diagram of the system for feedback control design.

In order to simplify the analysis, $G(j\omega)$ and $H(j\omega)$ are assumed only with proportional contribution, i.e., represented by the gains G and H respectively. Hence, the transfer function of the feedback loop $T(j\omega)$ is:

$$T(j\omega) = \frac{C(j\omega)\mathsf{G}}{1 + \mathsf{H}C(j\omega)\mathsf{G}} \tag{4.5}$$

The bandwidth of the system (B_s) corresponds to the frequency at which the gain of the loop is equal to 1, that is $|L(j\omega)| = |\mathsf{H}C(j\omega)\mathsf{G}| = 1$. For the controller under study $L(j\omega)$ is given by (4.6) and its magnitude is analyzed in Fig. 4.9.

$$|L(j\omega)| = \left|\mathsf{H}K_p\left(1 + \frac{1}{j\omega\tau_i}\right)\left(\frac{1}{j\omega}\right)\mathsf{G}\right| \tag{4.6}$$

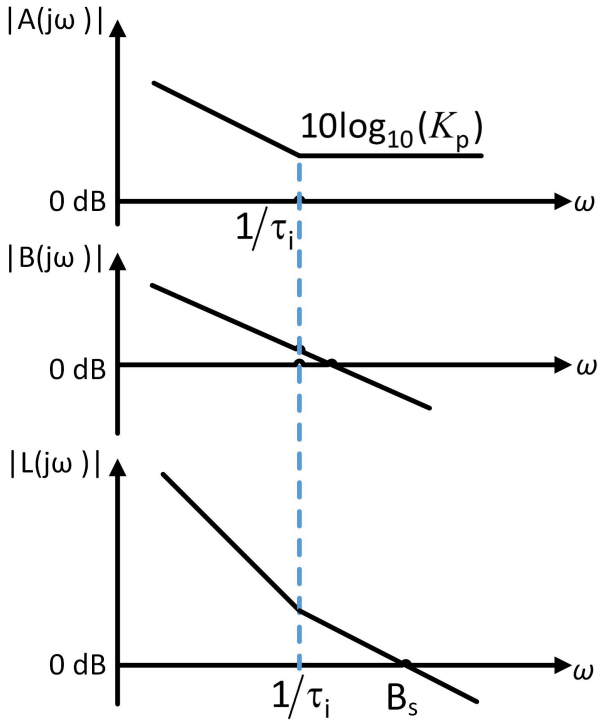


Fig. 4.9 Frequency domain analysis for control design.

While the term $\left(1+\frac{1}{j\omega\tau_i}\right)$ sets the time constant of the PI, B_s is determined by $|\mathsf{HG}K_p\frac{1}{j\omega}|$. Then, the system bandwidth B_s in hertz, is defined as:

$$B_\mathsf{s} = \frac{1}{2\pi}K_p\mathsf{GH} \tag{4.7}$$

Based on this analysis the digital controller is designed. The continuous-time transfer function $C(j\omega)$ is transformed in discrete-time by using the Forward Difference approximation.

$$C(z) = K_p\left(1+\frac{T_s}{\tau_i(z-1)}\right)\left(\frac{T_s}{z-1}\right) \tag{4.8}$$

Thus, the parameters of the digital controller, *gain* and *i_gain*, are expressed in terms of the system requirements, B_s and $1/\tau_i$, by comparing (4.2) and (4.8), and by replacing K_p according to (4.7):

$$gain = \frac{2\pi B_s T_s}{GH} \qquad i\_gain = \frac{1}{\tau_i} T_s \tag{4.9}$$

The resolution of *gain* and *i_gain* (number of bits for their representation) depends on the possible minimum and maximum values and consequently on the specifications for the implementation. This block is used for implementing the tracking NCO approach for the phase detector and the main servo of the general scheme (Fig. 4.5); therefore, further details are provided in the corresponding sections.

4.2.4 Phase Detector

Approach 1: Tracking NCO

In this approach, the phase of the DUT (see Fig. 4.8) that for this application corresponds to the phase noise introduced by the fiber, (phase difference between the signal transmitted and its round trip for the case of Doppler compensation or the single trip of the received signal for the case of two-way technique) is detected by extracting its quadrature component. It is done by means of the multiplication between a NCO configured at the same frequency of the DUT and a low pass filter (LPF) that removes the high frequency component resulting from the multiplication. If the AOMs add a frequency offset of 40 MHz, the beat note of the round trip will be around 160 MHz (80 MHz for single trip) but since the sampling frequency is 125 MHz it will be seen, due to aliasing, at 35 MHz (45 MHz). After obtaining the phase information, it is tracked through a servo which corrects the NCO phase as depicted in Fig. 4.10. An extension of this scheme can be performed in order to reveal not only the phase but also the amplitude of the noise introduced by the fiber. It is done by using the cosine output of the NCO. In this manner, the in-phase component of the noise is also obtained.

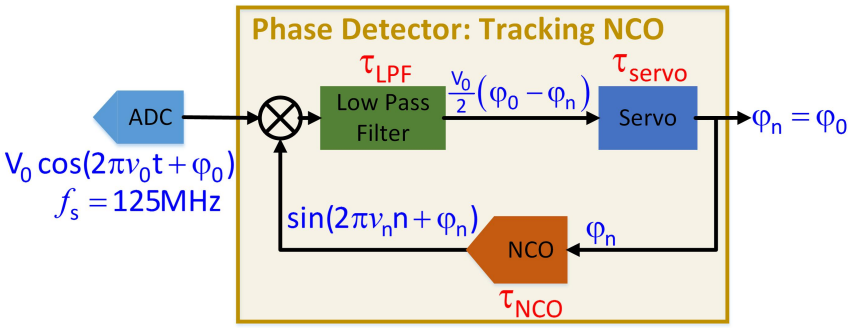


Fig. 4.10 Phase detector using tracking NCO approach.

The maximum bandwidth of the Tracking NCO is limited by the latency of the different blocks and the phase shift generated by the LPF. These contributions should be lower than $\pi/4$ in order to keep an adequate phase margin in the loop. The stability condition for the proposed phase detector is stated in (4.10), where $\tau_{total} = \tau_{LPF} + \tau_{servo} + \tau_{NCO}$.

$$2\pi f \tau_{total} + \varphi_{LPF} \leq \frac{\pi}{4} \tag{4.10}$$

Assuming linear phase in the filter pass band, the maximum tracking bandwidth that can be achieved with this approach is given by (4.11), where m_φ is the slope of the filter phase response in degrees per hertz, and f_N is the Nyquist frequency of the digital system (half the system clock frequency).

$$f_{max} = \frac{1}{4\left(2\tau_{total} + \frac{m_\varphi}{180 f_N}\right)} \tag{4.11}$$

The tracking bandwidth is inversely proportional to the total latency (τ_{total}), which is given by the contributions of the LPF, the NCO and the servo, and to the phase introduced by the filter. The critical component is then the LPF whose latency is proportional to the number of coefficients (case of FIR topology) or to the number of delay levels (case of IIR topology).

Hence, the critical requirement of this approach is the tracking bandwidth. A preliminary implementation of this scheme was performed in order to assess the limitations. On the other hand, the feasibility of the entire system implementation depends also on the FPGA resources utilization; therefore this

preliminary implementation is focused on quantifying the FPGA occupation of each block as well.

The NCO was designed by using the DDS IP core from Xilinx, described in Section 4.2.2 and the configuration implemented is summarized in Table 4.1. With such a configuration a latency of 2 clock cycles ($\tau_{NCO} = 2T_{clk}$) was obtained, and the FPGA occupation was: 85 of the 4400 available Slices (1.93 %), 0 DSPs and 1.5 of the 60 available BRAM (1.66 %).

Table 4.1 NCO configuration for preliminary assessment of the Tracking NCO approach.

Configuration Parameter	**Description**
Resolution Phase Accumulator	48 bits
Output width	14 bits
Phase Increment Programmability	Streaming. It means that the phase increment is not fixed and can be changed through the communication bus.
Phase Offset Programmability	Streaming. The phase offset is not fixed and can be changed through the communication bus. This allows the phase correction from the servo.
Latency	Configurable. The latency could be set according to the application requirements. For this implementation, it was set to the minimum value that is 2 clock cycles.

The servo was designed based on the block described in Section 4.2.3. The system was modeled by setting $G = V_0/2$ and $H = 1$ according to the scheme shown in Fig. 4.10. The bandwidth $B_\mathbf{s}$ required for this approach was 2 MHz. As design criteria, the frequency corresponding to $1/\tau_i$ was set to $\frac{1}{3}B_\mathbf{s}$. Then, from (4.9) the parameters $gain = 0.2$ and $i\_gain = 5.3 \times 10^{-3}$ were obtained, with $T_s = 1/f_s = 8$ ns (sampling frequency $f_s = 125$ MHz). Since the parameters values are smaller than 1, it was considered convenient to represent them by using fixed point. In this manner, simplifying the analysis of the required bits for not losing information due to the fact that the position of

the decimal point gives an indication about the resolution that the data would have. In order to represent 0.2, 5 bits in the fractional part are required, while 5.3×10^{-3} is expressed over 11 bits. Therefore, considering that these are the maximum values that the parameters would have, they are represented in 20 bits each one as [2.18] or 2Q18, i.e., two bits for the integer part and eighteen bits for the fractional part; thereby the minimum number that can be represented is 3.82×10^{-6} corresponding to $1/\tau_i = 477$ Hz and to $B_\mathsf{s} = 1.4$ kHz (according to the design criteria). With this configuration, a latency of 3 clock cycles ($\tau_{servo} = 3T_{clk}$) was obtained and the FPGA occupation was: 75 of the 4400 available Slices (1.70 %), 2 of the 80 available DSPs (2.5 %) and 0 BRAM.

The LPF design and implementation were studied carefully in order to minimize the FPGA resources utilization and guarantee the proper system performance. In this regard, the filter was first simulated by using MATLAB. The two topologies, FIR and IIR, were compared in order to assess the performance in terms of number of coefficients and delay.

The first approximation of the low pass filter required to remove the second harmonics generated by the multiplication of the sampled signal (beat note) and the NCO output was designed as a FIR filter. This kind of filter is commonly used for digital implementation due to its unconditional stability. However, it requires a higher number of coefficients with respect to IIR filters under the same specifications (cut-off frequency and attenuation in stop band). The specifications of the filter implemented here are: Cut-off frequency $f_c = 10$ MHz, Attenuation = 60 dB, pass band ripple = 0.5 dB, Filer Order = 45. The simulation results for this filter are shown in Fig. 4.11.

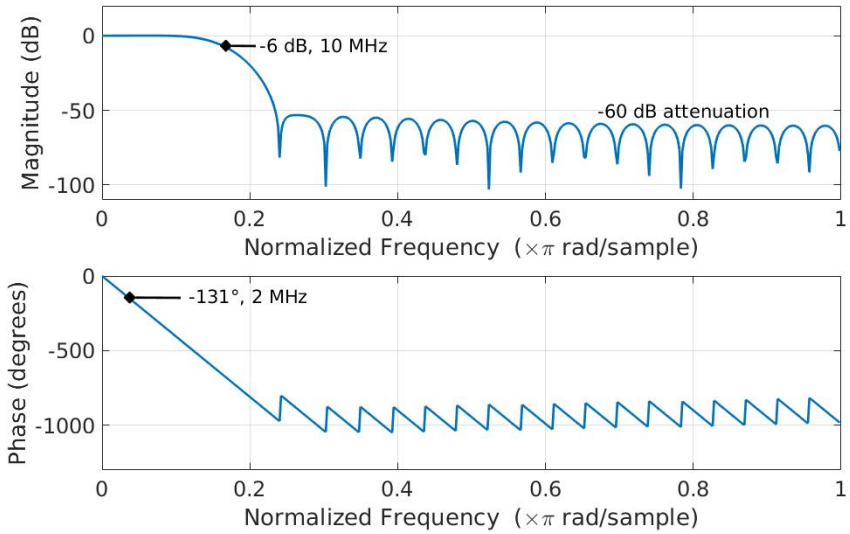
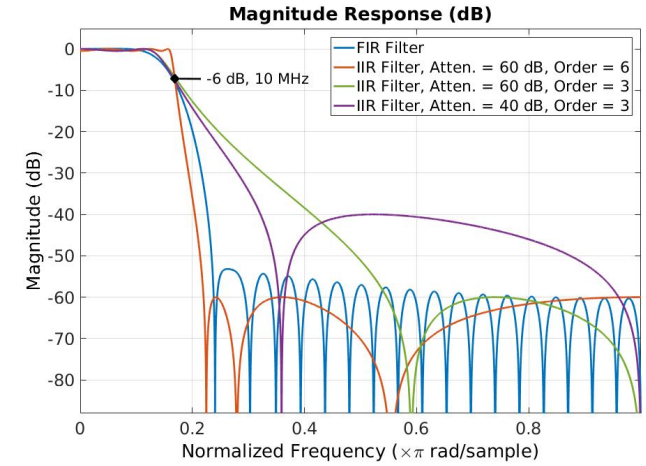


Fig. 4.11 Frequency response FIR filter. Cut-off frequency (f_c) 10 MHz. For this design, the MATLAB function fir1, based on the window method, was used. As design criteria, this function sets at -6 dB the normalized gain of the filter at f_c. The frequency is normalized to the Nyquist frequency.

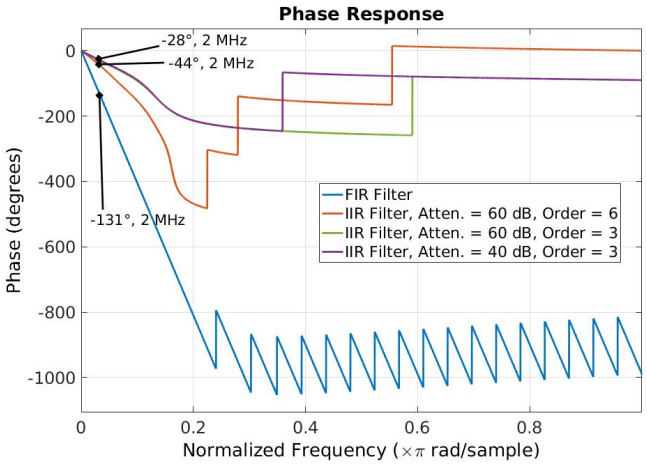
Although FIR filters guarantee a linear phase response in the pass band, an appreciated feature for different systems implementation, through this design it was observed that the phase shift at the cut-off frequency was around 634° and at the tracking bandwidth (2MHz) it was 131°. According to the loop stability analysis, the phase at the tracking frequency should be maximum 45°. Different configurations were assessed, by modifying the number of coefficients and cut-off frequency. However, lower number of coefficients implies wider pass band. The filter response was also evaluated with respect to different windowing techniques (Kaiser, Chebychev, Hann and Hamming) observing no improvement in the phase. The filter based on Hamming windowing was implemented in the FPGA in order to verify latency and resources utilization. The latency, proportional to the number of coefficients, was of 44 clock cycles (352 ns for a system clock of 8 ns). The FPGA resources utilization was: 321 of the 4400 available Slices (7.29 %), 23 of the 80 available DSPs (28.75 %) and 0 BRAM.

As second approach, the IIR topology was assessed. The design was based on the elliptic filter type because it allows achieving the specifications with lower number of coefficients than other techniques of the same topology. Different

configurations were evaluated in order to verify the phase shift according to the number of coefficients and the attenuation in the stop bandwidth. The specifications related to the cut-off frequency and pass band ripple were the same that the ones used for the FIR filter design ($f_c = 10$ MHz and pass band ripple = 0.5 dB). Fig. 4.12 shows the meaningful simulation results obtained and their comparison with the frequency response of the FIR previously described. The IIR filter exhibits a quasi linear phase within the pass band and the phase shift introduced is proportional to the order of the filter. By reducing the attenuation in the stop band the pass band becomes narrower. For the filter intended to be implemented, 40 dB of attenuation is enough in order to reject the high frequency component resulting from the multiplication between the input signal and the NCO. Hence, the filter that exhibits a better performance suiting the system requirements is the IIR filter of third order and 40 dB of attenuation; therefore it was selected for the implementation.



(a) Magnitude response.



(b) Phase response.

Fig. 4.12 Comparison between FIR and IIR frequency responses, $f_c = 10$ MHz. In order to perform the comparison properly, the normalized gain of all the filters at f_c is -6 dB.

The output of an IIR filter is described by (4.12), where $N-1$ is the order of the filter. In this topology the current output depends on the current input, the $N-1$ past input values and the $N-1$ past output values. Hence, it requires $2N-1$ coefficients, $2N$ adders, $2N-1$ multipliers and $2N$ delay blocks.

$$y(n) = \sum_{i=0}^{N-1} \mathrm{b}_i x(n-i) - \sum_{i=1}^{N-1} \mathrm{a}_i y(n-i) \tag{4.12}$$

The scheme for the implementation of such a filter is depicted in Fig. 4.13. The third order filter ($N-1=3$) was implemented by using the coefficients obtained during the simulation and representing them in fixed point. It is considered convenient for avoiding loss of resolution during the different stages of multiplication.

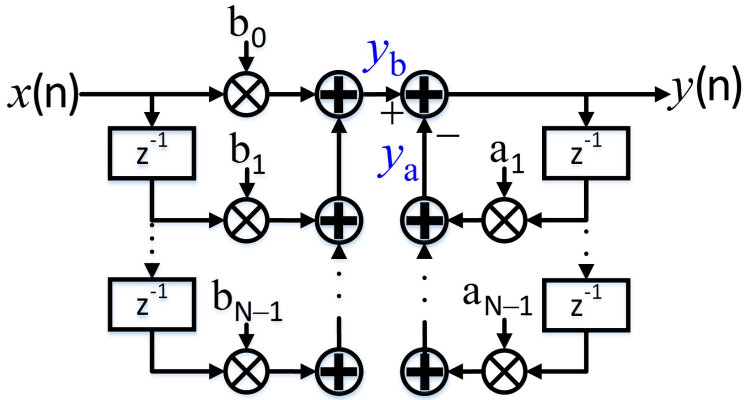
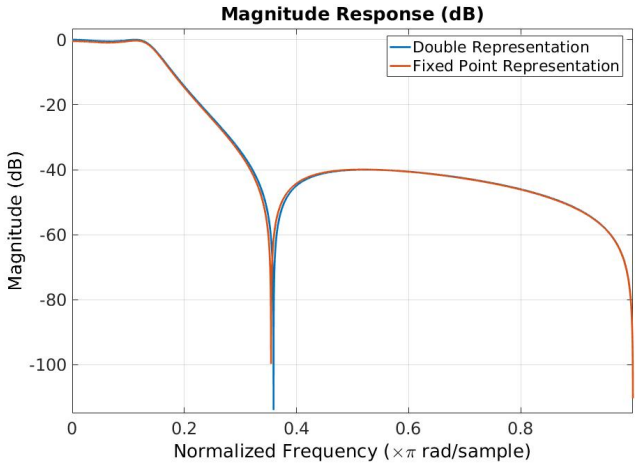
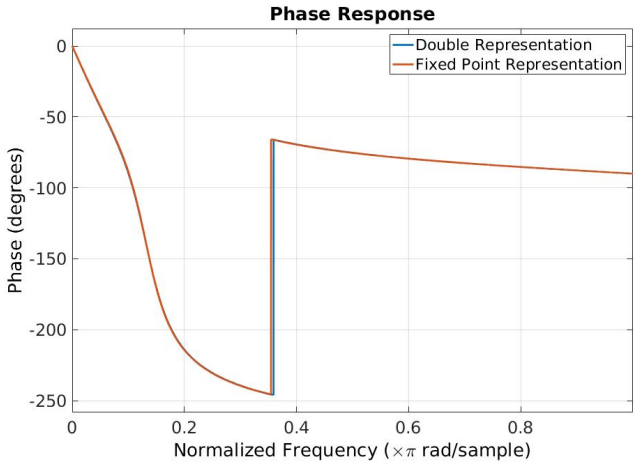


Fig. 4.13 Block diagram Infinite Impulse Response Filter. Direct Form I.

The number of bits for the coefficients representation was selected according to their maximum and minimum values. In order to verify that such a truncation does not degrade the filter frequency response, the comparison between the original filter, i.e., with double precision representation, and the fixed point representation was performed and it is shown in Fig. 4.14. As it can be observed, the requirements of phase, cut-off frequency and attenuation were still respected.



(a) Magnitude response.



(b) Phase response.

Fig. 4.14 Comparison between double precision and fixed point representations for the filter coefficients. The coefficients "b" were represented over 10 bits [0.10] or 0Q10, while the coefficients "a" were expressed also over 10 bits but as 3Q7 or [3.-7], where the negative sign indicates fractional part.

Then, the third order IIR filter was implemented on the FPGA according to the scheme shown in Fig. 4.13. The latency obtained was about 35.6 ns, approximately four times the system clock, in agreement with the number of delay levels, that for this filter order is four ($\tau_{LPF} = 35.6$ ns $\approx 4T_{clk}$). The FPGA resources utilization was: 24 of the 4400 available Slices (0.53 %), 10 of the 80 available DSPs (12.5 %) and 0 BRAM.

Table 4.2 summarizes the features obtained for the implementation of the Tracking NCO in terms of latency and FPGA resources utilization. The total latency of this implementation is 75.6 ns or approximately $9T_{clk}$.

Table 4.2 Latency and FPGA resources utilization.

Block	**Slices**	**DSPs**	**BRAM**	**Latency**
	4400	80	60	
NCO	1.93 % (85)	0	1.66 % (1.5)	$2T_{clk}$ (16 ns)
Servo	1.70 % (75)	2.50 % (2)	0	$3T_{clk}$ (24 ns)
IIR Filter				
Order: 3	0.53 % (24)	12.5 % (10)	0	$\approx 4T_{clk}$ (35.6 ns)

Recalling (4.11), the maximum tracking frequency also depends on the slope of the filter phase response. Since the IIR filter selected for the implementation exhibits a quasi linear phase on the pass band, the slope m_φ was extracted from the simulation reported in Fig. 4.14b, obtaining $m_\varphi = -876.2°$. Since the latency of the components was obtained in terms of clock cycles ($\tau_{total} = N_c T_{clk}$ for the general case), (4.11) is rewritten as (4.13). In this manner, the phase detector can be evaluated under different and more general conditions.

$$f_{max} \approx \frac{1}{4T_{clk}\left(2N_c + \frac{2m_\varphi}{180°}\right)} \tag{4.13}$$

Then, based on the design and implementation information, the maximum tracking frequency that can be achieved is around 1 MHz, ($N_c = 9$ and $T_{clk} = 8$ ns). Although this tracking bandwidth may be accepted for a first approximation of the instrument implementation, it is also important to verify that the actual implementation of this phase detector is capable of working at such a speed. For this purpose, the maximum frequency of operation (maximum system clock frequency allowed) of the implemented phase detector was assessed by using Vivado, the development tool from Xilinx. We observed that the minimum period of the clock should be around 11.4 ns in order to guarantee the proper system operation. The clock of the platform in which the system will be implemented is 8 ns, and even if it was eventually replaced by a lower frequency clock (1/11.4 ns = 83 MHz), the tracking bandwidth

would be approximately 819 kHz, insufficient improvement with respect to analog configurations currently available (100 kHz). Different techniques were applied for minimizing the latency. In particular, the filter design was reviewed; however, the IIR topology implies a feedback that restricts the use of some techniques like pipeline.

Then, in order to solve this issue, the approach for the implementation of the phase detector was replaced by the IQ detection technique.

Approach 2: IQ Detection

The I/Q phase detector is based on the extraction of the in-phase (I) and quadrature (Q) components of the DUT (beat note between the signal transmitted and its round trip for the case of Doppler compensation or the single trip of the received signal for the case of two-way technique). It is done through an NCO configured at the same frequency of the DUT and two identical LPFs that determine the measurement bandwidth. With this information the phase is obtained by computing the arc-tangent, $\varphi_0 = \arctan(Q/I)$ (Fig. 4.15). An extension of this scheme can be performed in order to reveal not only the phase but also the amplitude noise introduced by the fiber by calculating the module of the signal ($\alpha_0 = \sqrt{I^2 + Q^2}$). The main advantage of this approach is that a loop is not involved in the detection; therefore the latency introduced by the blocks is not a limiting factor for the detection bandwidth that should be high enough in order to avoid coherence loss due to the fiber noise. Actually, since the two branches, I and Q, are processed by using the same blocks, the data are affected by the same delays thereby remaining aligned.

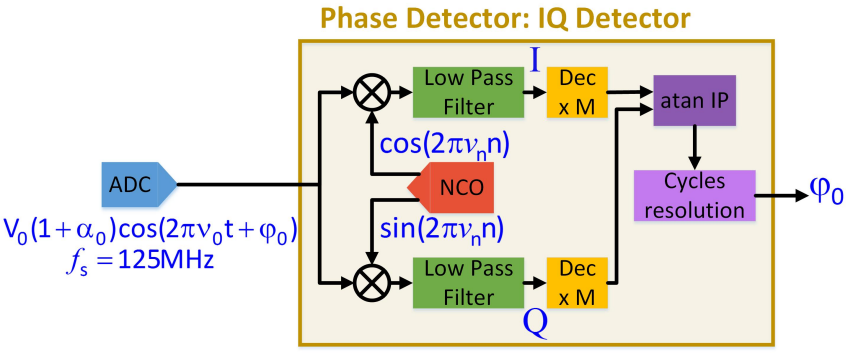


Fig. 4.15 Phase detector using IQ demodultation.

The potential limitations of this approach are related to: the FPGA resources utilization, the speed of the arc-tangent calculation and the phase resolution in order to be able to represent the phase noise introduced by the fiber. Hence, with the purpose of getting a general view of the impact of these limitations, a preliminary implementation of a phase detector was performed and it is here reported. According to actual beat notes (160 MHz and 80 MHz for the Doppler and two-way strategies respectively) the NCO was designed, as described in the Tracking NCO approach (Section 4.2.4), for obtaining 35 MHz or 45 MHz output frequencies. Although in this technique the phase offset is not needed, it remains accessible to the user through the communication bus for eventual alignment of the I/Q components or another purposes.

The LPFs were designed with cut-off frequency at 10 MHz in order to guarantee the required measurement bandwidth ($\geq$ 2 MHz) and the rejection of the high frequency component generated by the multiplication between the beat note and the NCO signal. From the experience acquired with the Tracking NCO implementation, the design was based on the FIR topology which allows applying extensive techniques for optimizing the implementation and it was implemented by using the FIR IP core from Vivado (Xilinx) [102]. The output of a FIR filter is given by $y(n) = \sum_{i=0}^{N-1} b_i x(n-i)$, where $N-1$ is the order of the filter. The canonical scheme for its representation is shown in Fig. 4.16. However, the IP core may use different structures in order to reduce FPGA resources and to increase speed.

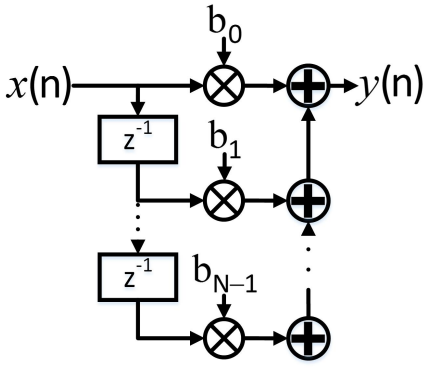
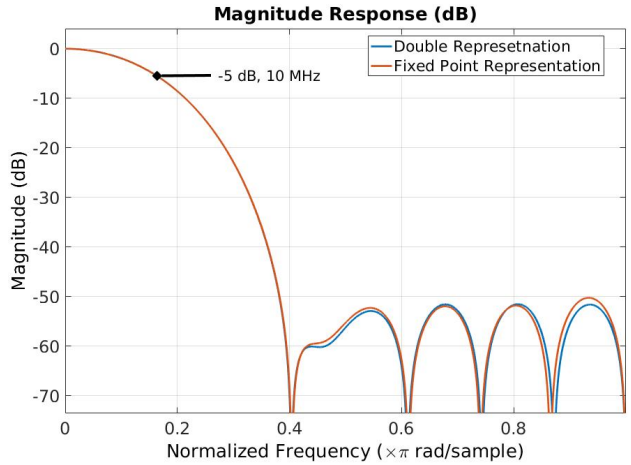


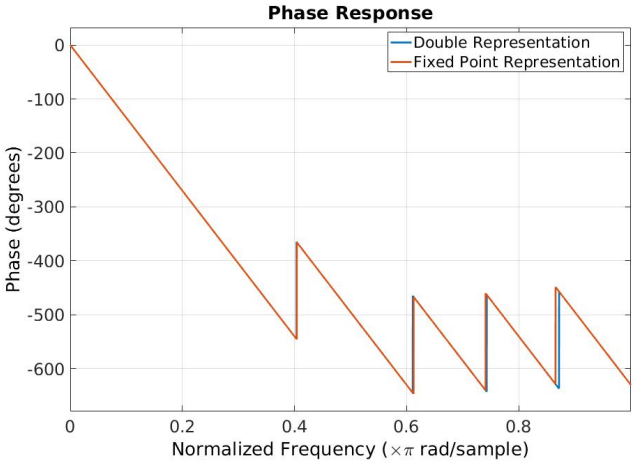
Fig. 4.16 Block diagram Finite Impulse Response Filter.

The filter was designed and simulated by using MATLAB. Specifically, the design was performed through the MATLAB function fir1 that is based on the

window method. As design criteria, this function sets at -6 dB the normalized gain of the filter at f_c. A file containing the resulting coefficients was generated in fixed point for the implementation. For this design a filter of 15th order was obtained. The coefficients are expressed over 12 bits, but since they have values much lower than 1 (0.170898 to -0.000977), only the 11 least significant bits are used thereby avoiding redundant information. The comparison between the original filter coefficients and the truncated version is shown in Fig. 4.17.



(a) Magnitude response.



(b) Phase response.

Fig. 4.17 Comparison between double precision and fixed point representations for the coefficients of the 15th order filter. The coefficients were represented over 12 bits in the fractional part and one bit for the sign, but only the 11 least significant bits were considered, [-2.-12] or 11Q12. This is because the value of the coefficients are so small that the most significant bits can be neglected and even the sign can be identified by the selected bits.

The frequency response suits the system requirements related to the cut-off frequency and the stop band attenuation with not excessive number of coefficients. According to Fig. 4.16, at maximum 16 DSPs will be used if not optimization is applied (and if the input does not exceed 25 bits of resolution considering that the DSP blocks perform operations between 18 bits and 25 bits inputs); therefore, since it is a good compromise between performance and estimated resources utilization, this filter was implemented on the SoC. The filter implemented exhibits a latency equal to $16T_{clk}$. The FPGA resources utilization was: 139 of the 4400 available Slices (3.15 %), 8 of the 80 available DSPs (10 %) and 0 BRAM.

At this point, the in-phase (I) and quadrature (Q) components of the DUT are obtained, and decimated by a factor M in order to reduce the data rate for the arc-tangent calculation. The arc-tangent is performed through the CORDIC IP core from Xilinx [103] which implements a generalized Coordinate Rotational Digital Computer (CORDIC) algorithm [104] for solving trigonometric, hyperbolic and root square equations, seven functions in total. By selecting the ArcTan function this block provides the four quadrant inverse tangent, arctan(Q/I). The inputs, Q and I, are represented between -1 and 1 and they are restricted to be expressed with 2 bits for the integer part while the fractional part can have a maximum of 46 bits. On the other hand, the output angle could be represented in radians from $-\pi$ to π or between -1 and 1 (scaled radians). In both cases, it is expressed by using 3 bits for the integer part and maximum 45 bits for the fractional resolution. Other configuration options are provided in order to optimize the implementation, such as Architectural Configuration, Pipeline Mode, etc. For the case here studied the resolution of the output phase was configured to 13 bits, i.e., 16 bits of total width ([3.-13] or 3Q13). Since the clock that is intended to be used for frequency transfer has an optical frequency of 194 THz, one cycle is equivalent to 5 fs. With 13 bits of phase resolution, the instrument will be able to measure the phase with a final resolution of 1×10^{-18} (5 fs/2^{13}). The configuration implemented is shown in Table 4.3. The FPGA resources utilization was: 285 of the 4400 available Slices (6.47 %), 0 DSPs and 0 BRAM.

Table 4.3 CORDIC configuration for arc-tangent implementation.

Configuration Parameter	**Description**
Functional Selection	Arc Tan
Architectural Configuration	Parallel
Pipelining Mode	Optimal.
Phase Format	Scaled Radians. Output angle between -1 and 1.
Input Width	16 bits. 2 bits for the integer part and 14 bits for the fractional part.
Output Width	16 bits. 3 bits for the integer part and 13 bits for the fractional part.

The phase added by the fiber is then measured in number of cycles through the block Cycles Resolution (Fig. 4.15). It is done by unwrapping the phase obtained from the arc tangent and by detecting a cycle increment or reduction, i.e., the movement of the phase in one direction or in the opposite. According to the experimental data presented by Calosso et al. [96] a fiber 47 km long accumulates approximately 11250 cycles (that corresponds to 60 ps) in 50000 s of measurement. In order to give sufficient resolution to the instrument for measuring the cycles introduced by a thousand kilometers link, the Cycle Resolution Block sets 27 bits for the integer part of the phase detector output ([27.-13] or 27Q13) thereby being able to measure 134.22×10^6 cycles (that corresponds to about 671 ns).

4.3 System Implementation

4.3.1 Further Considerations

In order to implement the digital instrument for the detection of the phase noise introduced by a fiber for frequency transfer, which is shown in Fig. 4.5 and whose design was previously described, further considerations were performed and they are reported below.

Main Servo

The parameters of the main servo, *gain* and *i_gain* depend on the system features, that means on the values of H and G that model the entire system (see Section 4.2.3). Since this instrument is intended to be used on the Doppler and two-way techniques, the model of the system may change according the technique used. For instance, in the case of applications using the Doppler cancellation technique, the system is model, in first approximation, as $G = 2$, because this technique is based on the round-trip of the signal on the fiber and therefore a factor of two is added to the phase introduced by the fiber. The system transducers are modeled as $H = 1$ because no gain is added to the phase before closing the loop. However, if the system model changes, it means that only by updating H and G, the parameters of the controller are adjusted to the new system conditions. On the other hand, the parameters of the main servo also depend on the system requirements, B_s and τ_i. For this servo, B_s is the compensation bandwidth that, contrary to the detection bandwidth (case of tracking NCO approach) is low, of the order of hundreds of hertz and inversely proportional to the fiber length [99, 105]. For the design of the main servo, the value of B_s was set to 100 Hz and the frequency corresponding to $1/\tau_i$ was set to $1/3B_\mathsf{s}$ (design criteria, see Section 4.2.3 for further details).

On the other hand, the decimation factor M was set to five reducing the data rate for the arc-tangent calculation and therefore for the main servo operation to 25 MHz ($T_s = 40$ ns).

The parameters of the controller, *gain* and *i_gain*, are then obtained by recalling (4.9), where $G = 2$, $H = 1$, $B_s = 100$ Hz, $1/\tau_i = 33.33$ Hz and $T_s = 40$ ns, according to the design criteria previously described.

$$\begin{aligned} gain &= \frac{2\pi B_\mathsf{s} T_s}{GH} = 1.26 \times 10^{-5} \\ i\_gain &= \frac{1}{\tau_i} T_s = 1.33 \times 10^{-6} \end{aligned} \tag{4.14}$$

For representing these values, 27 bits are required for the case of *i_gain* and 22 bits for the case of *gain*. Hence, they are expressed over 32 bits, [2.-30] or 2Q30, in order to provide a margin for lower frequencies configuration.

With 30 bits on the fractional part the minimum value that can be represented is 9.31×10^{-10} that corresponds to $1/\tau_i = 0.02$ Hz and $B_{\mathsf{s}} = 0.07$ Hz ($B_{\mathsf{s}_{min}} = 3/\tau_{i_{min}}$, according to the design criteria). The FPGA resources used for the implementation of this block were: 159 of the 4400 available Slices (3.61 %), 3 of the 80 available DSPs (3.75 %) and 0 BRAM.

IIR Chain: RF filters

In an actual implementation for frequency transfer, the photo diode (PD) that performs the beat note detection introduces additive noise that could generate errors in the phase measured, known as cycle slips [106]. Generally, this effect is prevented by using a PLL that acts as LPF [87, 96] with a bandwidth in the order of hundreds of kilohertz. For the instrument that is intended to be implemented here, this additive noise may corrupt the arc-tangent operation generating errors in the phase calculated when its power is comparable with the power of the beat note. In order to avoid this effect, a LPF is added before the arc-tangent block. In this regard, this filter is implemented as three cascaded first order IIR filters independently configured. The design and implementation of this filter chain is focused in reducing FPGA resources utilization while providing flexibility for the configuration bandwidth.

The design of the filters is based on the analysis of an analog first order LPF whose transfer function is given by (4.15), where $\omega_c = 2\pi f_c$ corresponds to the filter cut-off frequency.

$$H_f(s) = \frac{1}{1 + \frac{s}{\omega_c}} \tag{4.15}$$

The discrete-time transfer function $H_f(z)$ is obtained from the continuous-time $H_f(s)$ by using the Bilinear Transformation which allows mapping the imaginary axis of the s-plane onto the unit circle of the z-plane, thereby yielding the approximation $s = \frac{2}{T_s}\left(\frac{1-z^{-1}}{1+z^{-1}}\right)$, where T_s is the sampling period.

$$H_f(z) = \frac{\frac{\omega_c T_s}{\omega_c T_s + 2}\left(1 + z^{-1}\right)}{1 + \left(\frac{\omega_c T_s - 2}{\omega_c T_s + 2}\right) z^{-1}} \tag{4.16}$$

Considering that the canonical form for a first order IIR filter is given by $y(n) = b_0x(n) + b_1x(n-1) - a_1y(n-1)$, the transfer function in z-plane is:

$$H_f(z) = \frac{b_0 + b_1z^{-1}}{1 + a_1z^{-1}} \tag{4.17}$$

Thus, from (4.16) and (4.17), the IIR filter coefficients in terms of the analog bandwidth are:

$$b_0 = b_1 = \frac{\omega_c T_s}{\omega_c T_s + 2} \qquad a_1 = \frac{\omega_c T_s - 2}{\omega_c T_s + 2} \tag{4.18}$$

Considering that in general a digital low pass filter should satisfy the relation stated in (4.19),

$$\sum_{i=0}^{N-1} b_i - \sum_{i=1}^{N-1} a_i = 1 \tag{4.19}$$

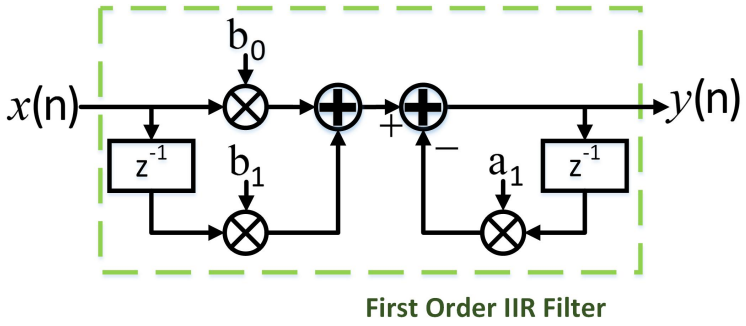
where N is the order of the filter, in order to avoid distorting the input signal in the pass band, the coefficients of the first order low pass filter stated in (4.18) could be approximated as expressed in (4.20) thereby reducing FPGA resources utilization.

$$b_0 = 2\frac{\omega_c T_s}{\omega_c T_s + 2} \qquad b_1 = 0 \qquad a_1 = \frac{\omega_c T_s - 2}{\omega_c T_s + 2} \tag{4.20}$$

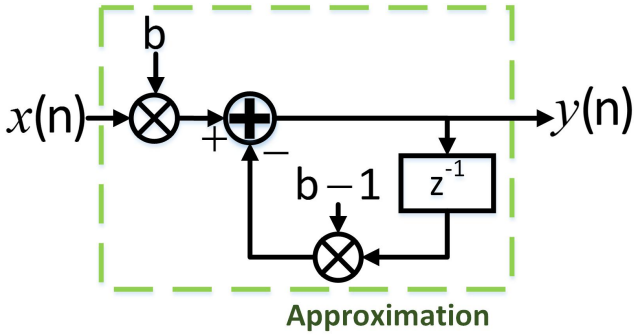
Taking into account that this filter is intended to operate in a frequency range between 10 kHz and 300 kHz, similarly to the PLL in current analog implementations, and considering that the sampling rate f_s is 25 MHz (125 MHz/5), then $f_c \ll f_s$, a second approximation ($\omega_c T_s \ll 1$) is performed still satisfying (4.19), resulting in the filter coefficients described in (4.21).

$$b_0 = b = \omega_c T_s \qquad b_1 = 0 \qquad a_1 = b - 1 = \omega_c T_s - 1 \tag{4.21}$$

Fig. 4.18 depicts the structure of the first order low pass filter obtained for the implementation. After the coefficients approximations, the cut-off frequency depends only on one parameter, b, instead of two, convenient not only for the implementation but also for bandwidth configuration once the system is implemented.



(a) First Order IIR filter.



(b) Approximation for first order IIR filter implementation

Fig. 4.18 First order IIR implementation. The purpose of this approximation is to minimize FPGA resources utilization and to increase system speed, considering that one IIR chain is required for each I and Q branch. Thus, in two channel configuration a total of 12 filters are used.

Fig. 4.19 shows the comparison between the filter obtained from the Bilinear Transformation and the one obtained from the subsequent coefficients approximations with cut-off frequency set to 10 kHz. The filters exhibit similar performance until 5 MHz, when the approximated filter attenuation remains at -55 dB. Considering that three filters of this kind will be cascaded, the resulting pass band will be narrower and the attenuation in the stop band will be lower than the single filter response depicted in the figure. This implementation

allows reducing FPGA resources utilization while obtaining an acceptable filter performance according to the system requirements.

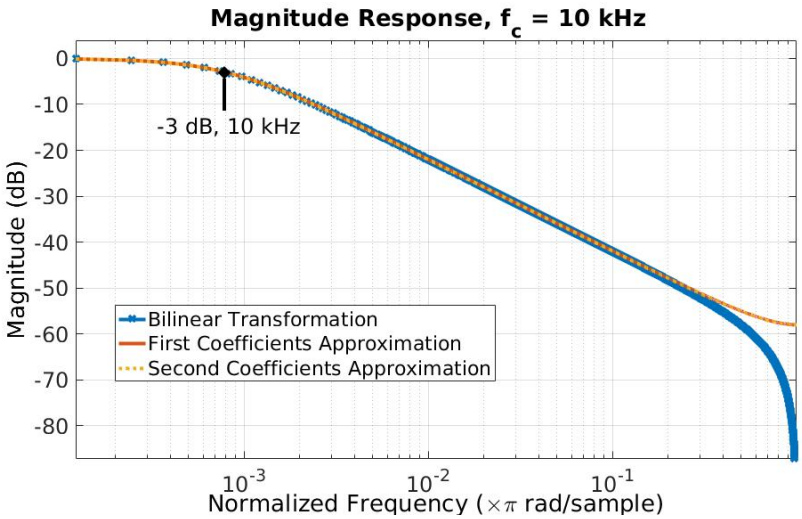


Fig. 4.19 First order IIR filter design. Subsequent approximations were performed to the coefficients in order to minimize resources utilization and to increase filter speed.

The resolution of the coefficient b is configured in order to obtain a cut-off frequency range between 4 kHz and 1 MHz approximately. Out of this range the filter will be disabled. This is performed by representing b over 11 bits, 1 for the integer part and 10 for the fractional part, [1:-10] or 1Q10. In this manner, the minimum value that could be represented is $b = 9.8 \times 10^{-4}$ that corresponds, from (4.21), to $f_c = 3.9$ kHz. The value $f_c = 1$ MHz is achieved when $b = 0.25$, but the maximum f_c that can be reached is 2 MHz ($b = 0.5$). Due to the approximations performed on the coefficients, the action of the filter becomes disabled when $b = 1$. Thus, through the proper configuration of this coefficient, a wide range of cut-off frequencies can be achieved according to the system requirements.

Sniffer: Data Storage and Decimation

In order to post-process, analyze and monitor the entire system, a block for data storage was developed (Fig. 4.20). It is based on a 16 channels multiplexer that according to the enable signal, stores the data decimated onto a First Input First Output (FIFO) memory block that features 64-bit of width length

and 14-bit of depth. The decimation factor DEC_N is represented over 30 bits yielding a resolution of 0.02 Hz. Two modes of data storage are configured: continuous and burst modes. In the continuous mode ($DEC\_N \geq 250$), the data are written in the FIFO each $DEC\_N/25$ MHz ($M = 5$), when it becomes ready. Under this mode, analysis at low frequencies is performed. The burst mode allows high frequency analysis by storing blocks of 16384 data written each 40 ns (M/f_s).

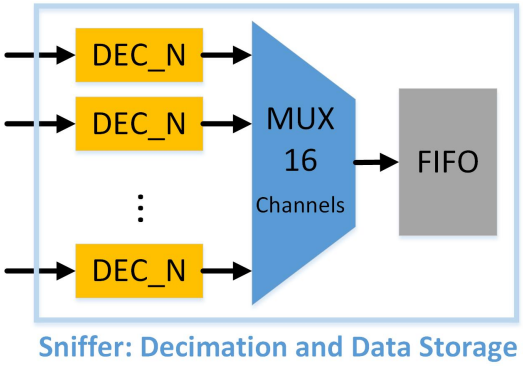


Fig. 4.20 Sniffer. Data storage for monitoring and post-processing. The decimation factor DEC_N is an input for the system given by the user. Similarly, the data (signals) to be stored are defined by the user.

Module

The beat note is detected correctly if the polarization between the two signals is properly aligned. This fact can be verified by extracting the amplitude noise present in the beat note. The block *Module* implements the root square algorithm in order to obtain the amplitude noise from the components I and Q already extracted for the phase detection. The design and implementation of this block is based on the CORDIC IP core from Xilinx [103]. By selecting the function Square Root, the equation $\sqrt{I^2 + Q^2}$ is solved. A first approximation of this block was implemented considering the resolution of I and Q equal to [2.-14]. The resolution of the output, is defined as half the input resolution plus one. For this case, the output resolution was set to [3.-14].

Based on the information obtained, a control for optimizing the polarization of the signals can be performed.

4.3.2 Implementation Results - Instrument Features

Based on the considerations and analysis previously described, the system shown in Fig. 4.21 was developed. It is capable of detecting phase and amplitude noise in 10 MHz bandwidth. Once the phase is detected the compensation bandwidth can be reduced through the RF IIR Chain as required for avoiding the effects of the additive noise introduced by the photo-detection.

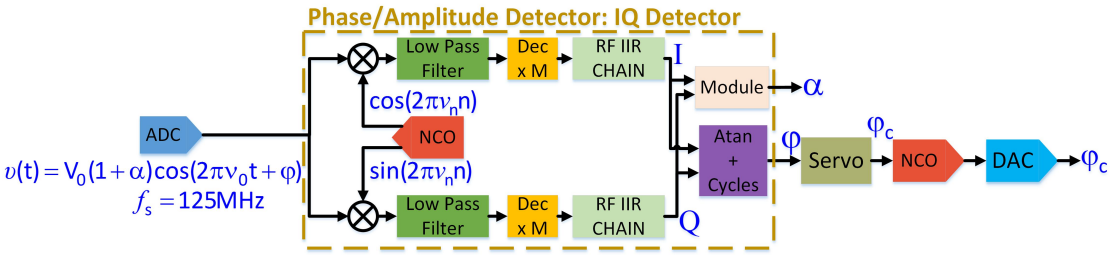


Fig. 4.21 Digital system for time transfer using fiber link. One channel implementation.

The complete scheme using two channels is depicted in Fig. 4.22. The different stages of the phase and amplitude detection can be monitored through the block Sniffer that stores the data on a FIFO for post-processing. Some stages of this post-processing such as data formatting and further stages of filtering (if required) are performed on the ARM embedded in the SoC before sending the data to the final user.

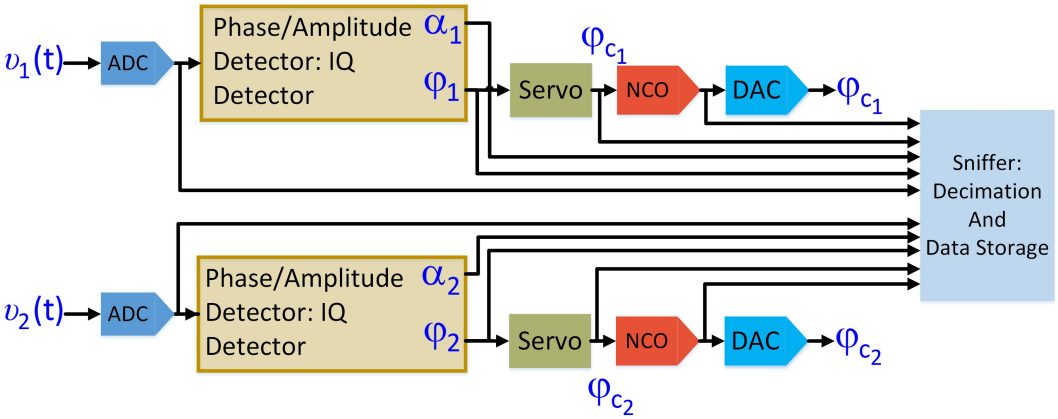


Fig. 4.22 Complete two channels implementation.

Table 4.4 summarizes the FPGA resources used for each block implemented. Additionally, an estimation of the total resources utilization required for the implementation of a two channels instrument is presented taking into account that for each channel the following blocks are required (see Fig. 4.21): two NCOs, two LPFs, six IIR filters (two IIR chains), one arctang, one Module and one Servo. One Sniffer block is capable of monitoring two channels. Based on this information, the feasibility of the instrument implementation on a determined platform can be verified.

Table 4.4 FPGA resources utilization of the instrument.

Block	**Slices**	**DSPs**	**BRAM**	**Total Blocks**
	4400	80	60	Two Channels
NCO	1.93 % (85)	0	1.66 % (1.5)	4
LPF- FIR				
Order 15	3.15 % (139)	10 % (8)	0	4
IIR				
Order 1	0.31 % (14)	3.75 % (3)	0	12
arctang	6.47 % (285)	0	0	2
Module	3.34 % (147)	0	0	2
Servo	3.61 % (159)	3.75 % (3)	0	2
Sniffer	1.5 % (66)	2.5 %(2)	0	1
Total				
Two Channels	52.5 % (2312)	95 % (76)	10 % (6)	

The complete system is reconfigurable through the parameters described in Table 4.5.

This system allows the implementation of any of the two techniques for the detection and compensation of the phase noise introduced by the fiber (Doppler or two-way) by only changing the parameters of some blocks such as NCOs, servo, filters, in order to guarantee the extraction of the phase information (I/Q demodulation frequency equals to the beat note and the proper detection and compensation bandwidth). Additionally, modifications on the techniques can be easily performed, for instance open loop or closed loop configurations, by enabling or disabling blocks through the system parameters as well.

Table 4.5 Configuration parameters of the instrument.

Block	Parameter	Description
Phase Detector		
NCO	Frequency	Output frequency for phase detection. Value according to input signal. 48 bits of resolution.
	Phase	Phase offset if alignment is required for proper I/Q demodulation. 48 bits of resolution.
IIR RF Chain	b_0, b_1, b_2	Coefficients of the IIR filters chain. Each filter can be enabled and configured independently. The coefficients are expressed in 12 bits using fixed point 2Q10. The bandwidth of each filter is defined from 4 kHz ($b_x = 1$) to 2 MHz ($b_x = 512$) and it gets disabled when $b_x \geq 1024$.
Servo	Command	8-bit command for servo configuration. The command is defined as: [rst sign cl p_en i_en 0 0 0]. See Section 4.2.3 for further details.
	gain	Control global gain. It is expressed over 20 bits in fixed point 12Q8.
	i_gain	Gain that corresponds to the time constant of the integrative block. It is expressed over 20 bits in fixed point 2Q18.
NCO AOM	Frequency	Output frequency for the AOM. The phase of this NCO is controlled by the servo. The frequency is provided with 48 bits of resolution.
Sniffer	DEC_N	Decimation factor for data storage. This value is represented over 30 bits
	sniffer_enable	This parameter allows the selection of the signals for data storage and monitoring. It is represented over 17 bits (16 channels + timetag).

4.4 Preliminary Tests and First Measurements

Preliminary tests were performed in order to assess the proper operation of the instrument and to verify the ultimate performance before an actual phase noise measurement was realized. Once the main blocks were verified, measurements on a fiber link for frequency transfer were done and the meaningful results are reported here.

4.4.1 Experiment 1: Phase detection - Open Loop

The main aims of this experiment are: to verify the phase detector operation, core of the instrument (see Section 4.2.4) and, based on the results obtained from this assessment, to estimate the noise contribution due to the electronics over each of the two techniques intended to be implemented by using the digital instrument (Doppler and Two-way). These estimations provide useful information for verifying whether an actual measurement is being limited by the noise of the instrument itself.

The experiment setup is depicted in Fig. 4.23. The two channels system (Fig. 4.22) was implemented on one Red Pitaya platform. One of the two channels was connected to a signal generator (Agilent E8257D) that simulates the beat note ($\nu_0 + \nu_{\text{offset}}$). In order to obtain a well known phase waveform at the output of the phase detector, a frequency offset (ν_{offset}) was introduced in the synthesizer. The system timebase and the synthesizer were referred to a low noise quartz-crystal oscillator of 10 MHz. With this configuration the phase measured should correspond to a ramp with a slope representing the frequency offset and whose maximum amplitude depends on the output phase resolution. For this experiment, the resolution of the phase detector was configured to 32 bits [19.13], i.e., 13 bits for the fractional part (resolution of one cycle) and 19 bits for the integer part (resolution of the phase accumulation in cycles - unwrapped phase).

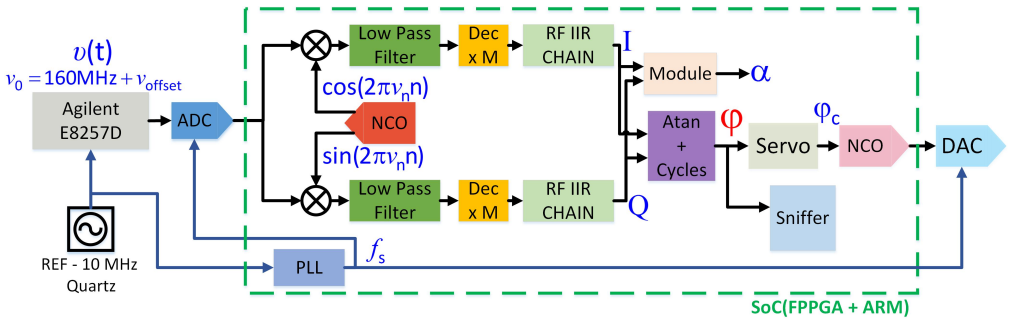


Fig. 4.23 The signal generator was configured for providing a sine wave of 160 MHz with a frequency offset of 100 Hz to the digital instrument. Since the sampling frequency f_s is 125 MHz, the input frequency set at 160 MHz is seen at 35 MHz due to aliasing. The output frequency of the NCO, that is part of the phase detector, is therefore set to such a value ($\nu_n = 35$ MHz) in order to properly extract the phase information by using the IQ phase detection approach.

Fig. 4.24 reports the results obtained by setting the simulated beat note ν_0 to 160 MHz with a frequency offset ν_{offset} of 100 Hz. Since one cycle is performed in 0.01 s ($\frac{1}{100\text{ Hz}}$), a sawtooth wave with period equals to 5242.88 s ($2^{19} \cdot 0.01$ s) was expected at the output of the phase detector.

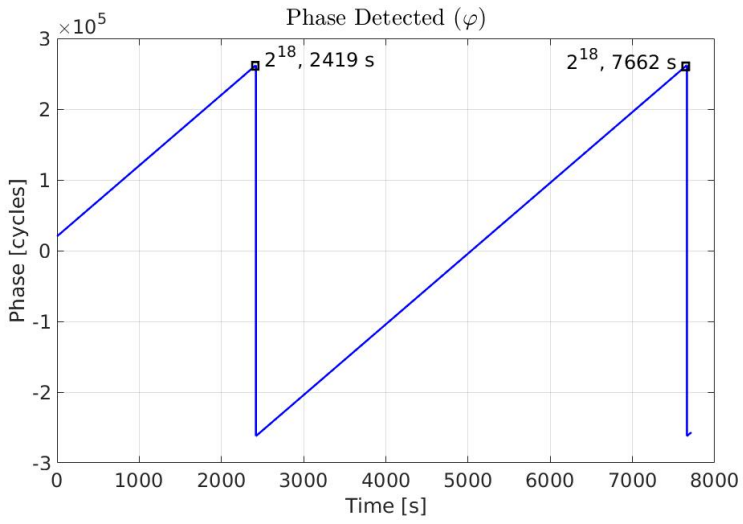


Fig. 4.24 Phase detected in open loop. The beat note was simulated by using a sine wave of 160 MHz and 100 Hz of frequency offset.

The phase detected in cycles correspond to the accumulated cycles on 19 bits of resolution for 100 Hz of frequency offset. These results not only validate the

phase detector operation but also the Sniffer block capabilities for storing data in continuous mode, since there are no data missing.

From the same set of data, the fractional frequency stability of the system was obtained and the results are reported in Fig. 4.25. The stability of the instrument is limited by the PLL noise as expected from the characterization results (see Section 3.3.2) being around 2×10^{-12} at 1 s of averaging.

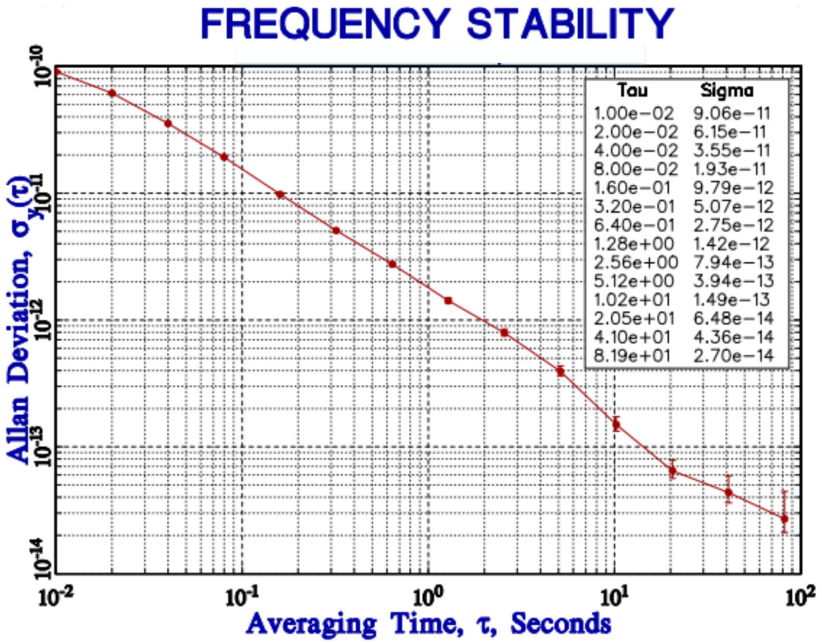


Fig. 4.25 Residual frequency stability of the system, preliminary results.

Based on these results, the contribution of the noise introduced by the electronics on the techniques for the detection and compensation of the fiber noise are estimated.

Fig. 4.26 depicts the general scheme for the implementation of the two techniques, Doppler and Two-way. Two digital instruments (i.e., two Red Pitaya platforms) are used, one at each of the two laboratories (at the local and remote end of the fiber). At each side, the digital instrument generates, through the NCOs and the DACs, the frequencies (ν_1 and ν_2) for driving the AOMs (AOM1 and AOM2). The phase-meters (ADC plus phase detector) extract, from the beat note provided by the photo detectors (PD1 and PD2), the phase information (φ_L and φ_R) that is intended to be compensated. In open loop configuration the servos are not used and the fiber noise is passively

compensated by post-processing; while in closed loop the servo of the local side provides a phase correction to the NCO that actively compensates for the noise induced by the fiber.

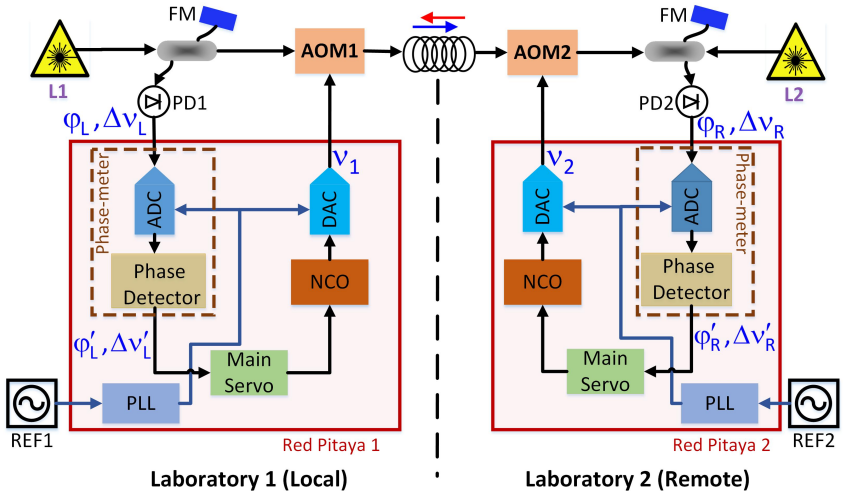


Fig. 4.26 Scheme for the Doppler and Two-way techniques implementation using the proposed digital instrument developed on the Red Pitaya platform.

Considering that an absolute frequency (carrier frequency) ν is defined as $\nu = \nu_0 + \Delta\nu$, where ν_0 is the nominal frequency and $\Delta\nu$ corresponds to the frequency fluctuations defined as $\Delta\nu = \frac{1}{2\pi}\frac{d\varphi}{dt}$, the fractional frequency fluctuations y are given by $y = \frac{\Delta\nu}{\nu_0}$ [59].

With the aim of estimating the contribution of the noise introduced by the electronics, the frequency fluctuations ($\Delta\nu_L$ and $\Delta\nu_R$), revealed by the photo detectors and subsequently measured by the digital instrument ($\Delta\nu'_L$ and $\Delta\nu'_R$) at the local and remote sides, are analyzed separately for each techniques.

Noise contribution of the electronics on the Two-way technique implementation

In the Two-way technique, the lasers L1 and L2 are sent in opposite directions (from Laboratory 1 to Laboratory 2 and from Laboratory 2 to Laboratory 1, respectively). At each side, the received signal is then compared with the original one, thereby extracting the beat note between them (see Section 4.1 for

further details). In general, this technique is used in open loop configuration, passively correcting the noise induced by the fiber.

The beat note revealed by the photo detector at the local laboratory (PD1) is described as: $\cos(2\pi(\nu_1 + \nu_2)t + \varphi_L)$, where φ_L is the phase that is intended to be extracted by the digital phase-meter and subsequently compensated. The frequencies ν_1 and ν_2, generated by the corresponding NCOs and DACs, are described as $\nu_1 = \nu_{01} + \Delta\nu_{DAC1}$ and $\nu_2 = \nu_{02} + \Delta\nu_{DAC2}$, respectively.

Then, the frequency fluctuations $\Delta\nu'_L$ measured by the digital instrument at the local laboratory are described in (4.22), where $\Delta\nu_{L1}$, $\Delta\nu_{L2}$, $\Delta\nu_{\overleftarrow{F}}$ and $\Delta\nu_{\varphi-meter1}$ correspond to the frequency fluctuations induced by the laser L1, the laser L2, the fiber in the direction from the remote to the local end, and the phase-meter at the local side, respectively.

$$\Delta\nu'_L = \Delta\nu_{L1} - (\Delta\nu_{L2} + \Delta\nu_{DAC1} + \Delta\nu_{\overleftarrow{F}} + \Delta\nu_{DAC2}) - \Delta\nu_{\varphi-meter1} \tag{4.22}$$

Considering that the noise introduced by the ADC and the DAC are lower than the contribution of the PLL, according to the characterization presented in Chapter 3, the frequency fluctuations generated by the electronics are dominated by the fluctuations in the system time base induced by the PLL. Thus, (4.22) is expressed as (4.23), where y_1 and y_2 are defined as the fractional frequency fluctuations induced by the PLLs of the digital instruments used at the local and the remote laboratories, respectively.

$$\Delta\nu'_L = \Delta\nu_{L1} - (\Delta\nu_{L2} + y_1\nu_{01} + \Delta\nu_{\overleftarrow{F}} + y_2\nu_{02}) - y_1(\nu_{01} + \nu_{02}) \tag{4.23}$$

Similarly, the frequency fluctuations $\Delta\nu'_R$ measured by the digital instrument at the remote laboratory are described in (4.24). In this case, $\Delta\nu_{\overrightarrow{F}}$ and $\Delta\nu_{\varphi-meter2}$ correspond to the frequency fluctuations induced by the fiber in the direction from the local to the remote end, and by the phase meter at the Laboratory 2, respectively.

$$\Delta\nu'_R = \Delta\nu_{L2} - (\Delta\nu_{L1} + \Delta\nu_{DAC1} + \Delta\nu_{\overrightarrow{F}} + \Delta\nu_{DAC2}) - \Delta\nu_{\varphi-meter2}$$
$$\Delta\nu'_R = \Delta\nu_{L2} - (\Delta\nu_{L1} + y_1\nu_{01} + \Delta\nu_{\overrightarrow{F}} + y_2\nu_{02}) - y_2(\nu_{01} + \nu_{02}) \tag{4.24}$$

Hence, in order to compensate for the noise induced by the fiber and thereby, to obtain the phase difference between the lasers, the subtraction between the two frequency fluctuations $\Delta\nu'_L$ and $\Delta\nu'_R$ is performed as described in (4.25).

$$\Delta\nu = \frac{\Delta\nu'_L - \Delta\nu'_R}{2}$$
$$\Delta\nu = \Delta\nu_{L1} - \Delta\nu_{L2} + \underbrace{\frac{1}{2}(\Delta\nu_{\overrightarrow{F}} - \Delta\nu_{\overleftarrow{F}})}_{\text{unsuppressed fiber noise}} + \underbrace{\frac{1}{2}(y_2 - y_1)(\nu_{01} + \nu_{02})}_{\text{electronics contribution}} \tag{4.25}$$

However, the information of interest $(\Delta_{L1} - \Delta_{L2})$ is still affected by unsuppressed fiber noise, already studied in [96], and by the noise induced by the digital instrument itself. The fractional frequency fluctuations y_{elect} generated by the electronics and relative to the optical frequency ν_{0opt} are given by:

$$y_{elect} = \frac{\Delta\nu|_{elect}}{\nu_{0opt}} = \frac{(y_2 - y_1)}{2}\frac{(\nu_{01} + \nu_{02})}{\nu_{0opt}} \tag{4.26}$$

The standard deviation of y_{elect} is obtained from (4.26) and expressed as (4.27) by assuming the noise processes y_1 and y_2 uncorrelated and by performing the following definitions:

- σ_{y_1} and σ_{y_2} are the standard deviations of the fractional frequency fluctuations induced by the digital system time base at the local and remote laboratories respectively.
- $\sigma_{y_{PLL}}$ is the standard deviation of the fractional frequency fluctuations induced by the PLL embedded into the digital instrument
- $\sigma_{y_1} = \sigma_{y_2} = \sigma_{y_{PLL}}$

$$\sigma_{y_{elect}} = \frac{\sigma_{y_{PLL}}}{\sqrt{2}} \frac{(\nu_{01} + \nu_{02})}{\nu_{0opt}} \tag{4.27}$$

According to the noise characterization performed on the Red Pitaya platform (Chapter 3), $\sigma_{y_{PLL}}$ is around 1-2 $\times 10^{-12}$ at 1 s of averaging. If the AOMs used for the two-way setup are configured for adding a frequency offset of 40 MHz ($\nu_{01} = \nu_{02} = 40$ MHz) and the frequency of the ultra-stable lasers L1 and L2 is 194 THz, a noise contribution due to the electronics $\sigma_{y_{elect}} = 2.9 - 5.8 \times 10^{-19}$ at 1 s of averaging is expected.

Noise contribution of the electronics on the Doppler technique implementation

For the case of the Doppler technique (refer to Fig. 4.26 for the general scheme), the laser L1 is sent from the local to the remote laboratory, where the received signal is compared with the laser L2. One part of the transmitted signal is returned to the local laboratory where the round trip signal is compared with the local signal L1 (see Section 4.1 for further details). In this manner, the noise induced by the fiber is detected and compensated, either actively (closed loop) or passively (open loop).

The frequency fluctuations $\Delta\nu'_L$ measured by the digital instrument at the local laboratory are described by (4.28). In this case, the phase meter extracts the phase from the beat note between the round trip signal and the L1.

$$\begin{aligned} \Delta\nu'_L &= \Delta\nu_{L1} - (\Delta\nu_{L1} + 2\Delta\nu_{DAC1} + \Delta\nu_{\overrightarrow{F}} + \Delta\nu_{\overleftarrow{F}} + 2\Delta\nu_{DAC2}) - \Delta\nu_{\varphi-meter1} \\ \Delta\nu'_L &= -2y_1\nu_{01} - \Delta\nu_{\overrightarrow{F}} - \Delta\nu_{\overleftarrow{F}} - 2y_2\nu_{02} - y_1(2(\nu_{01} + \nu_{02})) \end{aligned} \tag{4.28}$$

On the other hand, the frequency fluctuations $\Delta\nu'_R$ measured by the digital instrument at the remote laboratory are described in (4.29). In this case, the beat note is obtained from the single trip of L1 on the fiber.

$$\Delta\nu'_R = \Delta\nu_{L2} - (\Delta\nu_{L1} + \Delta\nu_{DAC1} + \Delta\nu_{\overrightarrow{F}} + \Delta\nu_{DAC2}) - \Delta\nu_{\varphi-meter2}$$
$$\Delta\nu'_R = \Delta\nu_{L2} - \Delta\nu_{L1} - y_1\nu_{01} - \Delta\nu_{\overrightarrow{F}} - y_2\nu_{02} - y_2(\nu_{01} + \nu_{02}) \tag{4.29}$$

In order to compensate for the noise induced by the fiber, the subtraction between the two frequency fluctuations $\Delta\nu'_L$ and $\Delta\nu'_R$ is performed as described in (4.30). The information of interest $(\Delta_{L2} - \Delta_{L1})$ is still affected by unsuppressed fiber noise, already studied in [95], and by the noise induced by the digital instrument itself.

$$\Delta\nu = \Delta\nu'_R - \frac{1}{2}\Delta\nu'_L$$
$$\Delta\nu = \Delta\nu_{L2} - \Delta\nu_{L1} + \underbrace{\frac{1}{2}(\Delta\nu_{\overrightarrow{F}} + \Delta\nu_{\overleftarrow{F}}) - \Delta\nu_{\overrightarrow{F}}}_{\text{unsuppressed fiber noise}} + \underbrace{(y_1 - y_2)(\nu_{01} + \nu_{02})}_{\text{electronics contribution}} \tag{4.30}$$

Then, for the case of the implementation of the Doppler technique, the fractional frequency fluctuations y_{elect} generated by the electronics and relative to the optical frequency ν_{0opt} are given by:

$$y_{elect} = \frac{\Delta\nu|_{elect}}{\nu_{0opt}} = \frac{(y_1 - y_2)(\nu_{01} + \nu_{02})}{\nu_{0opt}} \tag{4.31}$$

Similarly to the analysis done for the case of the Two-way technique implementation, the standard deviation of y_{elect} is obtained from (4.31) and expressed as (4.32), by assuming the noise processes y_1 and y_2 uncorrelated and by defining $\sigma_{y_1} = \sigma_{y_2} = \sigma_{y_{PLL}}$.

$$\sigma_{y_{elect}} = \sqrt{2}\sigma_{y_{PLL}}\frac{(\nu_{01} + \nu_{02})}{\nu_{0opt}} \tag{4.32}$$

Hence, for the implementation that is intended to be performed in which we have $\sigma_{y_{PLL}} = 1 - 2 \times 10^{-12}$ at 1 s of averaging, $\nu_{01} = \nu_{02} = 40$ MHz and $\nu_{0opt} = 194$ THz, the expected contribution of the digital instrument is: $\sigma_{y_{elect}} = 5.8 \times 10^{-19} - 1.17 \times 10^{-18}$ at 1 s of averaging.

From these analysis we observed that the noise contribution due to the electronics in the Two-way implementation is a factor of two lower than in the Doppler implementation. This is because of the method used by each approach in order to compensate for the noise generated by the fiber.

The estimation of the noise induced by the electronics helps to determine whether an actual measurement is limited by the noise of the instrument itself. This information will help to verify the reliability of the results in a real measurement.

4.4.2 Experiment 2: Phase detection - Actual Fiber Link

In this section, an actual measurement using the digital instrument for the detection and compensation of the noise induced by the fiber in the comparison of two ultra-stable lasers is described. The experiment setup is depicted in Fig. 4.27. The link configuration used is based on two 150 km-long buried fibers, placed in the same cables between the Istituto Nazionale di Ricerca Metrologica (INRiM) and the Laboratoire Souterrain de Modane (LSM) on the Italy-France border. For convenience of the experiment, the two fibers are joined together at LSM to obtain a 300 km loop with both ends at INRiM which are connected in common mode to one ultra-stable laser (L1). The laser of 194 THz (ν_{0opt}) is locked to one high-finesse Fabry-Perot cavity and phase-locked to a hydrogen maser using a frequency comb.

Each AOM introduce a frequency offset of about 40 MHz ($\nu_1 \cong \nu_2 \cong 40$ MHz) in order to distinguish the transmitted signal from parasite reflexions (see Section 4.1 for further details).

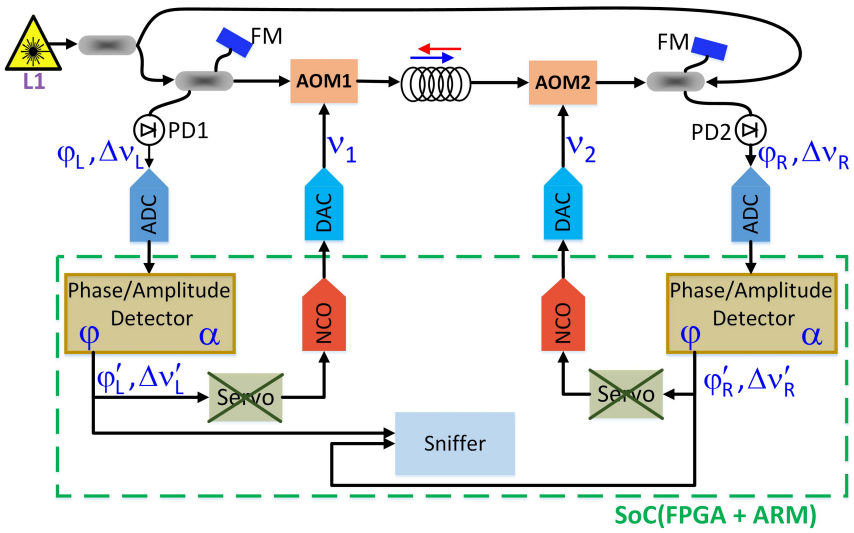
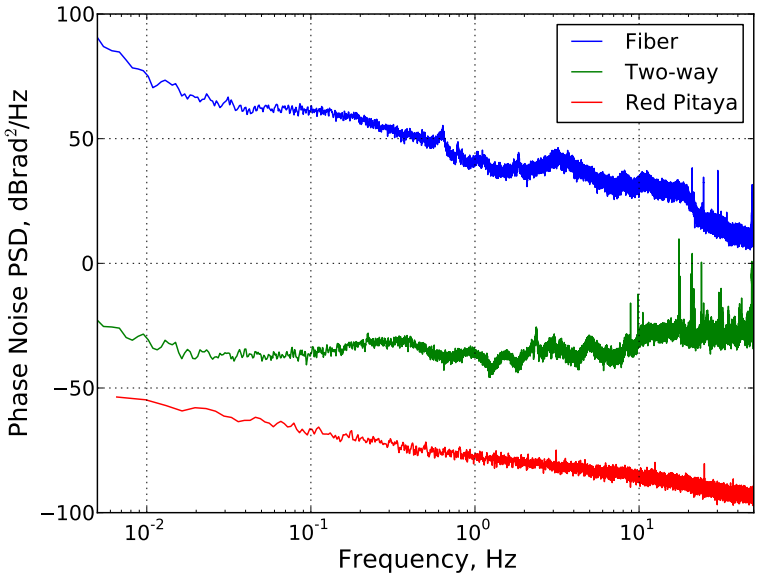


Fig. 4.27 Measurement in an actual Fiber Link for Frequency Transfer by using the Two-way technique for the detection and compensation of the noise induced by the fiber. With this configuration, the beat note measured by the photo detectors at each side of the fiber (PD1 and PD2) is 80 MHz. This information is seen at 45 MHz due to aliasing ($f_s = 125$ MHz).

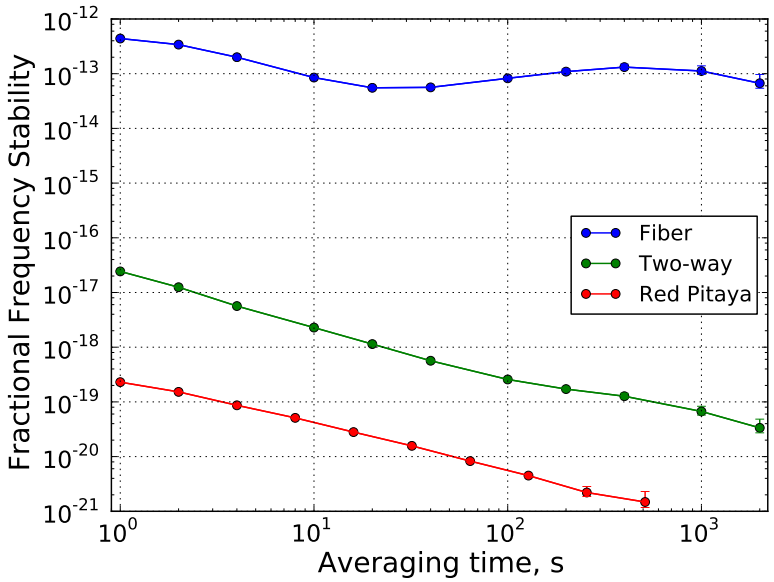
The complete two channels system (Fig. 4.22) was implemented and the two beat notes provided by the photo detectors, PD1 and PD2, were acquired by using a single Red Pitaya platform. The technique used for the detection and compensation was the Two-way approach in open loop configuration (Section 4.1); therefore the servos used for actively correcting the phase noise were not required. The data related to the phase detected by each channel were stored through the Sniffer block in continuous mode by using a decimation factor of 250000, that means a measurement resolution of 0.01 s.

The results of this experiment are reported as follows.

Fig. 4.28 compares the spectrum (Fig. 4.28a) and the Allan deviation (Fig. 4.28b) of: the fiber noise, i.e., the phase of one of the two beat notes (blue curve), the phase difference of the two beat notes (green curve) and the noise introduced by the electronics (red curve).



(a) Phase noise spectrum.



(b) Fractional frequency stability. Measurement bandwidth $f_h = 0.5$ Hz.

Fig. 4.28 Comparison of the phase of one of the two beat notes (blue curve), phase difference of the two beat notes (green curve) and noise introduced by the electronics (red curve).

The two-way technique reaches a fractional frequency stability of around 2×10^{-17} at 1 s and 4×10^{-20} at 2000 s of averaging, in agreement with the data reported in [96].

By comparing the estimated noise introduced by the electronics (red curve) with the detected fiber noise (blue curve), we observed that the digital instrument does not limit the measurement, exhibiting a fractional frequency stability around 2×10^{-19} at 1 s of averaging, that is around 10^7 times lower than the fractional frequency stability of the fiber noise.

The improvement on the system for frequency transfer by using the Two-way technique is verified from the comparison of the fiber noise (blue) and the Two-way (green) curves. An improvement of around one million times at 1000 s of averaging is observed which increases at long term operation.

Fig. 4.29 depicts the comparison between the phase (in seconds) induced by the fiber (blue curve) and by using the two-way technique for its compensation (green curve).

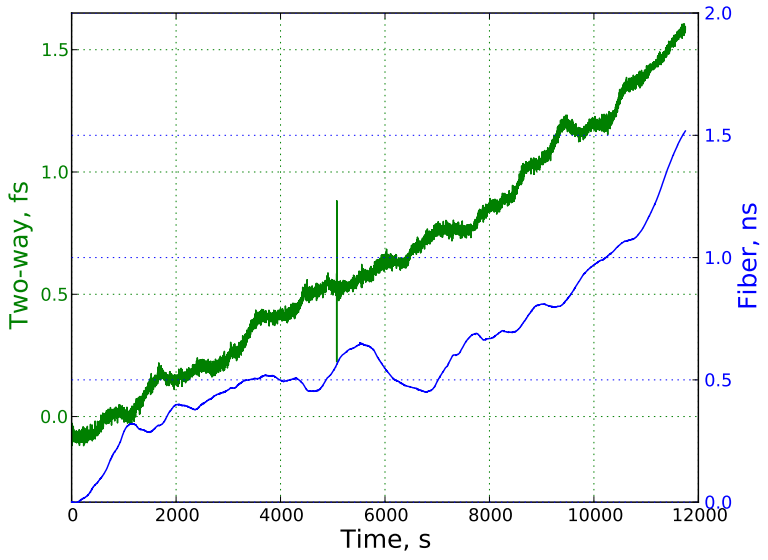


Fig. 4.29 Improvement of the system for frequency transfer by using two-way technique for noise detection. The measured phase of one of the beat notes (blue curve) and the phase difference (green curve) are reported in seconds.

Here the improvement on the system by using the two-way technique is also evidenced. The fiber accumulates around 1.5 fs at 12000 s, approximately one million times less than without compensation. In addition, it is worth to highlight that over the 12000 s of measurement cycle slips were not observed, while in measurements performed with the analog system one cycle slip is observed every one or two minutes.

4.4.3 Discussion of the Obtained Results

The performance of the system was verified through the experiments reported in the two previous sections. As expected, from the noise characterization performed on the Red Pitaya platform, the system is limited by the noise due to the PLL. However, it was verified that this is not a limitation for the detection and compensation of the phase noise induced by the fiber in the frequency comparison of ultra-stable optical clocks. Instead of that, the implemented digital instrument brings important advantages with respect to analog implementations that are currently available for this application.

The proposed digital instrument is a compact solution that integrates different functionalities such as phase-meter, stability control and polarization control in only one platform. Although the last two functions are still under test, the instrument already allows performing closed loops for actively controlling the phase induced by the fiber and it extracts the amplitude noise of the beat note provided by the photo detector. The amplitude contains information related to the rotation between the two signals polarization. Remembering that for a proper phase detection the polarization of the signals must be maintained aligned (Section 4.1), current analog implementations provide a polarization control that in general is performed manually and that limits the performance over long fiber links. By using the proposed digital instrument, such a control can be directly implemented.

The instrument allows remote access for configuration and monitoring. Hence, the system parameters, the FPGA configuration and the processor executable can be modified easily when required. Furthermore, the data obtained from the measurement, which are stored in memory by means of the Sniffer Block, can be downloaded and post-processed when needed.

Currently, the implementation of the Fast Fourier Transform (FFT) algorithm is under development. With this feature the instrument will be able to obtain the power spectral densities of the beat note before the phase extraction, the detected phase and the phase correction (in closed loop configuration). These spectra will be provided to the user for the visualization either on the same instrument, by using a web server or offline by downloading the obtained data.

Chapter 5

Conclusions and Future Work

The main noise sources of a high resolution, two-channel ADC are exposed through a low computational cost method by acquiring synchronously two operation points of a sine-wave input signal: zero-crossings and peak values. From the measurements in single channel and in common mode, we have verified the proper discrimination of each operation point and the two ADC channels un-correlation. According to their analysis, we conclude that the phase and amplitude noise are limited by the additive noise generated in the input stage which impacts similarly in these two ADC noise components (phase and amplitude). The voltage reference does not degrade the ADC acquisition even at maximum input voltage range. Albeit the aperture jitter does not have a high impact on the ADC phase noise in common mode, we could verify its properties and behavior. From these results we can claim that the ADC phase noise effects are lower at high sampling frequency and high input amplitude.

The technique for ADC noise characterization proposed here provides estimated amplitude and phase noise floors at frequency offsets close (down to 10 Hz) and far to the carrier (up to Nyquist frequency) which allows direct analysis for phase and amplitude noise metrology. It can be replicated for characterizing any high resolution ADC. The requirements are two-channel ADC, one DAC and a digital PI. For the nature of the digital processing the computational resources needed are not high: RAM blocks of 16 kB per channel and digital clock system at the maximum of the ADC sampling clock were used in the setup presented.

This work presents a differential ADC noise model, rejecting the common noise contributions. Alternatively, Non Linear Transmission Lines (NLTL) could be used [107] for changing the slew rate and for obtaining an absolute or complete ADC noise model.

The proposed ADC characterization allows having access to the main noise sources in order to predict the effects on phase noise measurements, useful information for phase noise metrology instrumentation design. Based on that, we can claim that high resolution ADCs are suitable for implementations at high frequency and high input amplitude. Albeit their phase noise could limit phase noise measurements of low noise oscillators, knowing the ADC noise properties could open the door to new techniques for ADC noise rejection on amplitude and phase noise metrology.

Extensions of this work could include, noise characterization of high resolution ADCs of different architectures and technologies, and the assessment of two-channel ADCs not embedded in the same chip where common noise rejection is expected to be lower.

We have characterized the internal PLL of Red Pitaya platform for time and frequency metrology. A better performance, in terms of phase noise can be achieve if the slew rate of the PLL input is higher than 156 V/μs. In this manner, the slew rate is high enough to make negligible the contribution of the input stage with respect to the delay on the propagation path that dominates the PLL.

The internal PLL is a flexible solution whose stability is suitable for most time and frequency applications.

The characterization of the Red Pitaya platform allowed predicting the effects of the electronics on an actual digital instrument implementation for frequency transfer using fiber link. The noise contribution due to the electronics was then verified through measurements performed by using the proposed digital instrument on a system for frequency comparison of ultra-stable clocks.

The digital instrument designed and implemented for the detection and compensation of the phase noise introduced by the fiber, allows the implementation of the two schemes, Doppler and Two-way, in closed and open loop, by only changing the parameters of the system and no additional hardware modification

are required. Furthermore, the instrument extracts the amplitude noise of the beat note, which contains information related to the polarization of the signals. Since maintaining aligned the polarization of the signals is crucial for the proper detection of the phase, current analog implementations provide a control for the rotation of the polarization that in general is performed manually. With the scheme proposed the amplitude noise is extracted together with the phase; therefore the polarization control can be directly implemented.

Cycle slips were not evidenced over the 12000 s measurement performed on the 300 km fiber link by using the digital instrument, while in the analog implementation one cycle slip is observed every one or two minutes, limited by the measurement bandwidth.

A state of the art phasemeter is intended to be design and implemented on a higher performance platform. The proposed technique is based on the digital implementation of the Tracking DDS whose performance may be limited by the DAC phase noise. In this regards, the characterization of the DAC is under development in order to assess the instrument implementation feasibility. Characterization measurements will be performed on the ADC as well in order to have a complete description of the platform.

Publications related to the work presented in this thesis are described as follows:

A first approximation of the model and the method for ADC noise characterization was presented as a talk at the Joint Conference of the IEEE International Frequency Control Symposium & the European Frequency and Time Forum (EFTF/IFCS) in 2015 [108].

Preliminary results of the instrument design for the detection and compensation of the phase induced for the fiber in an application for frequency transfer were presented as a poster at the European Frequency and Time Forum (EFTF) in 2016 [109].

The model and the method for the ADC noise characterization were improved and validated on the Red Pitaya platform. The analysis, implementation and results are reported in [110].

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