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Original
Effective Characterization of Radiation-induced SET on Flash-based FPGAs / Sterpone, Luca; Azimi, Sarah. - ELETTRONICO. - (2017). (Intervento presentato al convegno Radiation Effects on Components & Systems Conference tenutosi a Geneva, Switzerland nel 2-6 October 2017).

Availability:
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Publisher:
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12 October 2024

Effective Characterization of Radiation-induced SET on Flash-based FPGAs

Luca Sterpone, Sarah Azimi

***Abstract*— Single Event Transients (SETs) are one of the major concern for Flash-based Field Programmable Gate Arrays (FPGAs). In this paper, we propose a new analysis to characterize the SET phenomena within Flash-based FPGAs.**

***Index Terms*—Single Event Transient, Flash-based FPGAs, Radiation Effect.**

I. Introduction

RADIATION effects on VLSI technology are provoked when radiation particles such as neutrons, protons or heavy ions hit a sensitive region of the integrated circuits. A radiation particle strike deposits a charge that result in a voltage glitch on the affected node generating a spurious signal defined as Single Event Transient (SET). Once the voltage glitch is generated, it may reach the primary output of a circuit thus provoking a circuit functional interruption. Radiation-hardened by design techniques already provided a solution [1] for reducing their critical impact on design, while a definitive solution for mitigating radiation effects on combinational gates has not been developed yet. Due to the future technology node scaling, it is expected that radiation effects in combinational gates will dominate the future technology sensitive nodes [2].

In this paper, we proposed a new methodology for fully characterizing SET exploiting internal electrical pulse injection. The proposed approach emulate realistic SETs happening in harsh environments, furthermore, thanks to the novel contribution of this paper, it allows to effectively identify their impact on realistic circuit architectures.

II. Related Work

Several research activities have been done on the characterization of radiation-induced SETs in sequential and combinational circuits [3]. Most of the works have been performed at a simulation level including technology-based physical equation for the evaluation of the radiation strike and its propagation across the technological cell. The propagation of the transient pulse through the combinational logic data path and routing resources [1] on Flash-based FPGA. Previous work [11] showed that SET propagation depends on many factors such as the shape and width of the initial particle-hit, the path of the SET pulse through the logic cells in terms of fanout and load, the layout of the circuit and the user`s design configuration of the FPGA. New insight on flash-based FPGA is investigated in [4]. A new methodology for effectively measuring the width of radiation-induced transient faults has been proposed and developed in [5] [6]. However, they are not effective for a representative example of realistic designs. In these considerations, only the effect related to delay of SET has been investigated without respect to the filtering and broadening effects. Recent studies reported radiation test experiment and electrical fault injection of SET propagation on custom circuits designed specifically to observe SETs [7].

Previous work of accurate SET pulse electrical injection shows a strong SET pulse-width modulation when SET pulse traverses logic gates and the effect of type of traversed logic gates and routing architecture of the technology [7]. In [8], an analytical model for analyzing the sensitivity of SET nonmetric technology has been proposed. This model has been used for the accurate simulation of GPGPUs applications against the occurrence of transient errors. This model has been demonstrated to be effective, since it is possible to propagate SET pulses from the affected location to the registers involved in the computation allowing to determine the right influence of SEE in the GPGPU architecture [9].

The main scientific contribution of the present paper is a complete identification of the SET propagation scenario. Thanks to the developed method, we are able to cover the possible pulses propagation cases and its relative Propagation Induced Pulse Broadening (PIPB) effect on circuits implemented on Flash-based FPGAs.

III. Injection and Characterization Methods

The proposed method is based on two parts: the internal electrical injection of the SET pulse and the characterization of the pulse propagation. The electrical injection refers to the approach we introduced in [6], while the propagation has been analyzed considering two hypothetic conditions: the former consists on the presence of different logic gates after the SET pulse injection; the latter is related to the possibility that the propagation traverses several node with different fan-out gates. The basic principle of the developed characterization method is represented in Figure 1. This principle is based on the assumption that any kind of SET generated in sensitive nodes and propagated in different position encounter different points. At any point of its logic gate traversing, the SET propagation is dependent on two main factors: the subsequent combinational logic gates (e.g., observable in front of the pulse) and the fan-out gates present in a given position during the pulse

propagation (e.g., the logic fan-out affecting a propagation position).

In order to study the life-cycle of the SET from its generation to the reach of a destination point such as a Flip-Flop or an I/O pin, we observed the behavior of the SET by configuring different test setup while the SET has been injected using the same logic gate topology.

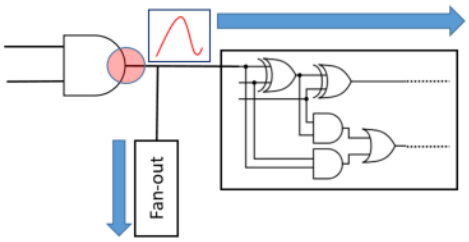

Fig.1. The main method hypothetic conditions with two observability points: towards next logic gates and towards fan-out (as shown by the arrows).

A. *Electrical SET injection*

There are three main methodologies in order to emulate SET pulses induced by particles that strike the semiconductor device: radiation test, laser test and electrical injection. One convenient and economical method to provide a voltage pulse is electrical injection [6]. Using this method, it is possible to control the parameters of the generated pulse and also the location and time of injections. Between the external and internal electrical injection, we choose internal electrical injection to provide pulse generated inside the circuit in order to avoid the filtering effect of I/Os structure and to have a better control of the pulse parameters. The pulse generator structure have been implemented into the FPGA architecture by programming logic cells with the corresponding pulse generator scheme illustrated in Figure 2.

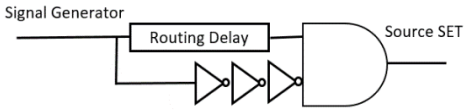

Fig.2. The developed logic scheme for the Internal Pulse Injection Generation.

In order to void the intrusiveness unpredicted behavior of the pulse generator scheme, we modified the placement and routing in such a way to avoid the SET pulse injection variation.

IV. Characterization Test Setup

Four types of test structures have been implemented for the SET characterization. According to the circumstances of the typical circuit design, the first scenario has been dedicated to the combinational logic, represented by an inverter-string, while in the second scenario the fan-out has been added to the inverter-string. Going into details of the typical circuits, we noticed the existence of divergence and convergence of combinational path in the design. Therefore, we continue the analysis, modifying the implemented design to study the effect of chain convergence and divergence in SET propagation.

A. *First scenario: analysis of inverter-string*

The fist analysis consists in the characterization of the logical gates chain with respect to the injection of SETs. For this purpose, we used inverter gates as logical gates while we used different length of inverter-string, as it is illustrated in Figure 3.. We report the result considering one type of SET injected at the input of the chain while collecting the result related to the observed SET at the end of the string. The internal electrical injection part has been used maintain the same placement and routing characteristics.

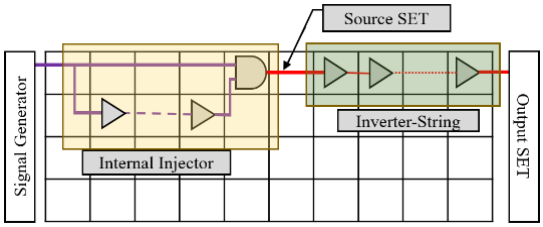

Fig. 3. An overview of the placement layout.

Please note that we place the logical gates in the same distance to have the same routing constants and guarantee the similar distance between each logic cell.

B. *Second scenario: analysis of inverter-string and fan-out of INVs*

The second scenario is an extension of the first one since it has the inclusion of various inverter gates as fan-out of the first scenario. The fan-out of inverter gates has been connected to the beginning of the string, where the SET has been injected. As it can be observed in the Figure 4, the design of place and route of the fan-out provides the minimal distance connection between each VersaTile. This placement has been design in a way that all the routing segment are similar and this placement has been fixed for all the experiments.

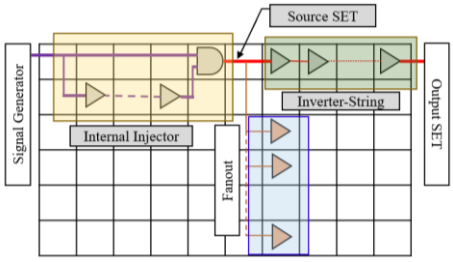

Fig. 4. An overview of the Placement area layout for the simultaneous analysis of Loads and Chain of gates.

Please note that each output of these INVs in the load has been tied to the output pin in order to not be simplified with the tool and this pinout has been fixed for all the tests.

C. *Third scenario: analysis of chain divergence*

For the next step, we moved toward the conditions of typical logical designs and considering the characteristics of SET while there is an occurrence of divergence of combinational paths. If we consider the typical adder structure, as it represented in the logical scheme of a Full Adder in Figure 5. When there is an occurrence of SET in the divergence point, independent of considering that SET has been generated here or propagated until here, SET will spread through divergence point and propagate through alternative logical string and reach to the storage elements connected to the affected string.

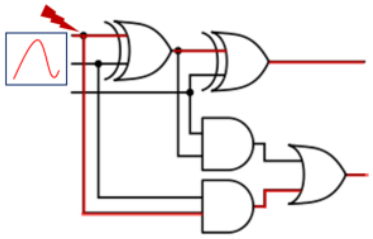

Fig.5. Logical Scheme of full adder affected by SET in the divergence point.

In order to study this phenomenon, we modified the second scenario to reconstruct the SET characterization in divergence point. As the new test, we enhance different length of inverter-string in the middle of the main string as represented in Figure 6. In order to observe the behavior of SET going through divergence point, we inject SET at the input of the main string while collecting the result of the SET behavior at the end of the main string and at the end of the added sting in the divergence point. The same as previous test, the placement and routing of the implemented design has been controlled totally and tied to the same placement for the all the tests.

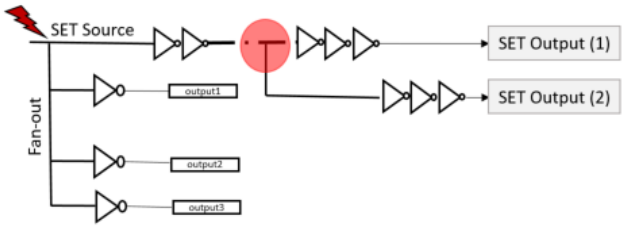

Fig. 6. Conceptual Scheme of third Scenario.

D. *Fourth scenario: analysis of chain convergence*

After divergence point in the circuit, the next typical condition is when the SET traverse through divergence point, propagate through different logical path and routing and reach to the convergence point of the circuit. As it is shown in Figure 7, adder is representing the condition under study.

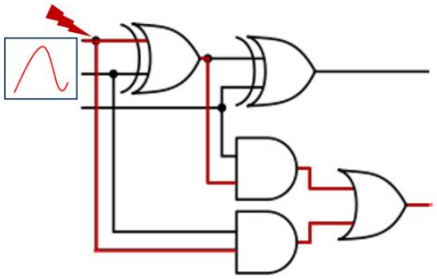

Fig.7. Logical Scheme of full adder affected by SET in the convergence point.

In order to reconstruct this phenomenon, we design a simple circuit, modifying the previous tests structures. Figure 8 represents the logical scheme of the developed design while the SET has propagated through path A and B, reach to the convergence point of C. We injected the SETs at the divergence point of the design and observed the SET at the output of the convergence point in order to characterize its propagation exclusively for the considered scenario.

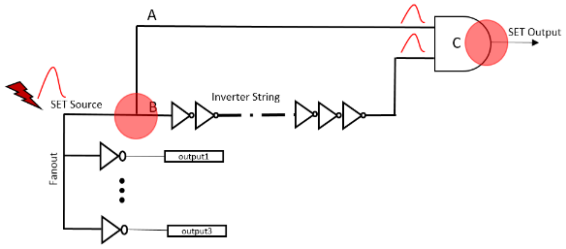

Fig.8. Conceptual Scheme of fourth Scenario related to the propagation through two convergence paths (A and B).

Please note, that the placement and routing of the electrical injection, inverter-string, fanout and pinout of the fanout has been fixed following the previous tests in order to provide comparable results.

V. Experimental Results

The experimental analysis have been executed on a MicroSemi ProASIC3 A3P250 Flash-based FPGA. As it has been mentioned before, for the entire performed test, we analyzed the result obtained from the observed SET at the end of the Inverter string. We classify the results in term of ratio between the output SET pulse at the end of the chain and the source injected SET at the start of the chain. To develop the tests, we also measured the delay between the source SET and output SET.

A. *First scenario: Inverter-string*

As the first test, the design represents 4 different length of string of 40, 60, 80 and 100. As it is presented in Figure 9, by increasing the length of the string, the PIPB is increasing until it reaches a saturation point. In addition, the delay is progressively increasingly in relation to the number of INVs in the chain.

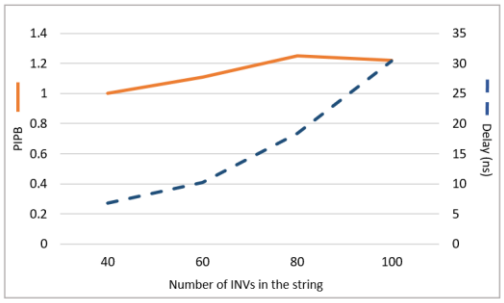

Fig.9. Propagation Induced Pulse Broadening and Delay.

B. *Second scenario: Inverter-string and fan-out*

We continued the first test by adding different number of 20, 40 and 60 inverter gates as fanout connected to the different number 40, 60, 80 and 100 inverters in the string. For each combination of inverter-string and fanout, the result related to the PIPB effect has been denoted in Figure 10. It is observed that by increasing the length of string, the PIPB increases which is a verification of the previous test. In addition, it can be observed that the PIPB is progressively attenuated by increasing fanout for a fixed number of inverters as a chain.

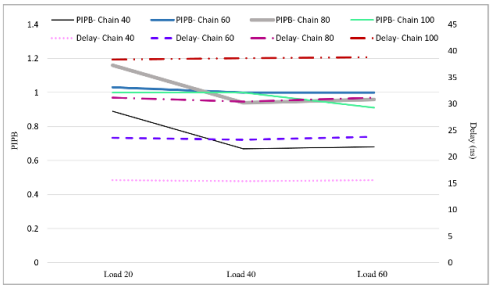

Fig.10 . PIPB and Delay report of the source SET and Output SET.

Considering the delay of the circuit, it is noticeable that for the fixed number of INVs in the chain, by increasing the number of INVs in the load the delay of the circuit is not changing as it has been presented in Figure 10. Therefore, if we evaluate the fan-out as the filtering part of the architecture, we can obtain the modification of PIPB without introducing a delay for the circuit.

C. Third scenario: Chain divergence

In order to study the SET behavior in divergence point of our circuit, we fix the length of the main string as 60 inverters and tied different number of 60, 80 and 100 inverters tied to the alternative string while the fanout has been considered as 60 inverters. The data related to the propagated SET in the main string and convergence string has been collected. Figure 11 reports the result of this test.

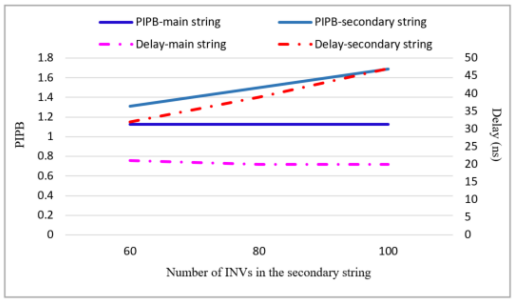

Fig.11. PIPB report of divergence scenario.

D. Fourth scenario: Chain convergence

We developed the fourth scenario to analyze the behavior of SETs while it has been multiplied into two SETs through divergence point of the design, propagated and reached to the convergence point. In order to do this, we consider a string of 20, 40 and 60 inverters and fanout of 20, 40 and 60. We inject SET at the start of the string and SET propagated through two-designed path where the first one has a string of inverters and the second one consists of routing segments only.

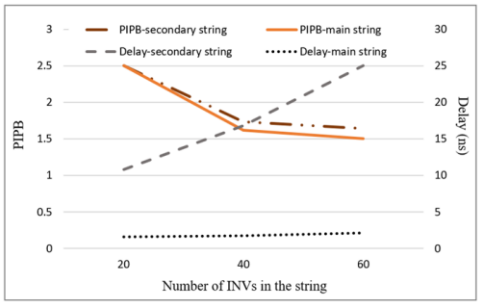

Fig.12. PIPB report of convergence scenario.

Figure 12 shows the obtained results demonstrating that the respective counterpart only marginally influences the PIPBs of the two strings. However, we also identify a particularly relevant phenomenon, which is due to the overlapping of the outcome of one SET. As it is illustrated in Figure 13, an SET can propagate through two convergence path and producing two different types of phenomena. The former happens when there is a large difference on the propagation delay of the two paths, therefore the two SET shapes are provided as two separate pulses (i.e., Figure 14, left). Vice versa, in case the delay difference between the paths is minimal it is possible to obtain a Convergence SET (C-SET) which is characterized by an extremely large width (i.e., Figure 14, right). Please note that this is typically the case of combinational arithmetic structures.

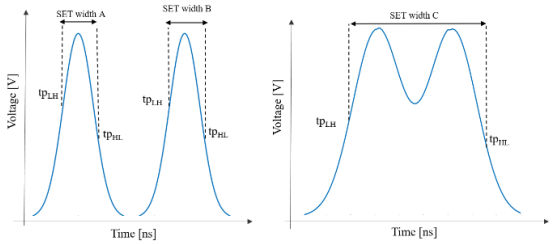

Fig.13. An example of SET propagated through two convergence paths and generating: two independent SET pulse (left) and a C-SET pulse (right).

VI. Conclusions and Future Works

In this paper, we presented a characterization method for exhaustive characterization of the SET phenomena affecting Flash-based FPGAs in radiation environments. As future work we plan to applied the developed model for the analysis of a realistic circuit.

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