A robust capacitive digital read-out circuit for a scalable tactile skin

A Robust Capacitive Digital Read-Out Circuit for a Scalable Tactile Skin

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***Abstract*— This paper presents a robust, capacitive digital Read-Out Circuit (ROC) for sensitive skin applications in humanoid robots. The ROC can be calibrated to null the parasitic effects of transducer variation due to physical assembly. A prototype is fabricated in a 130 nm RFCMOS process, with an active area of 221×79 μm^2 and 1.84 μW power consumption at $V_{\mathrm{DD}} = 1.2$ V and 1 ms read-out rate. The ROC output is robust to V_{DD} and temperature variations in a range $|\Delta V_{\mathrm{DD}}| \leq 20\%$ and (25 – 53) °C. Furthermore, it can provide up to 200 mV_{pp} power supply sine wave rejection in the range 50 Hz–5 MHz at $V_{\mathrm{DD}} = 1.1$ V, for an output standard deviation lower than one LSB. Owing to its features and its digital modularity, the ROC was co-designed with a scalable and modular Multi-Walled Carbon NanoTube (MW-CNT) nanocomposite transducer, to achieve a tunable output sensitivity by adjusting the sensor nominal capacitance and the reference capacitance. The maximum sensitivity of 5.23 fF per LSB was reached when both match. The ROC was then validated with the MW-CNT nanocomposite sensor which exhibits a piecewise behavior. 5.3 and 7.1 ENOB were extrapolated in the low-load and medium-load regions, respectively. Besides the major advantage of tunable sensitivity, the presented ROC features the lowest acquisition time and one of the most compact sizes among the state-of-the-art ROCs. Moreover, PVT robust output and ultra-low power consumption make this solution very attractive to replicate human physiology at robotic-level.**

***Index Terms*— Relative Count Detection, Robotic Skin, All-digital Read-Out Circuit, Multi-Walled Carbon Nanotubes (MW-CNTs).**

I. Introduction

Tactile sensing is crucial for the development of humanoid robots [1]–[4], which must be able to feature the human sense of touch, with measurement and processing rates as close as possible to those of humans. So far, practical pressure transducers exploited in humanoid robots are typically capacitive, as shown in [1], [5], [6], separately engineered to achieve a very large number of distributed sensors [7] and modular coverage [2]. Specifically, polymer/carbon filler nanocomposites are proving ideal candidates as transducers, thanks to their scalability, modularity, ease of manufacturing and flexibility [8].

Tactile information is acquired by using hundreds of sensing elements (e.g., ∼100 in [5] and 256 in [9]) and, since they commonly operate in parallel, communication bandwidth and available energy for each one becomes limited [10]. In fact, sensing coverage density tends to be aggressively increased to provide punctual and precise data throughout the robotic body and tactile skins are designed to feature both modularity [7] and high temporal (up to 1.9 kHz in [9]) and spatial resolution (up to 0.12 mm localization acuity over 4 mm sensor resolution in [11]), to properly reproduce human capabilities. In this regard, advanced techniques are engineered to overcome the existing resolution limits both at design and acquisition-level. For instance, in [11] the cross-talk phenomenon between close modules is exploited to reach superresolution. Furthermore, modularity is closely related to scalability [7], as compact modules can be scaled into smaller units and replicated all over the surface, leading to more integrated solutions and lower production and set-up costs. Hence, at transducer-level, the targeted resolution must be achieved even when the sensor is scaled down in modules. At electronic-level, to enable such a modular read-out and besides scalability, each ROC must feature compact size, ultra-low power consumption, robustness and minimization of bias circuitry (as robots are electrical noisy and physically constrained environments).

Specifically, a compact size for the read-out circuitry becomes essential to achieve the targeted peformance. The smallest possible silicon area should be used in order to reduce production costs. Furthermore, designing a compact ROC makes it possible to increase the density of read-out units or the number of functional blocks integrated within a single silicon chip.

Increasing the density of read-out units, more tactile sensors can be interfaced with a single chip, which could lead to the increase of spatial resolution. Increasing the number of functional blocks, different circuits can be integrated within the chip, which would then be able to perform several tasks, such as post-processing, communication, computing, control.

This paper presents a 130 nm robust, digital, modular capacitive read-out core [12], specifically co-designed with a scalable MW-CNT nanocomposite material transducer, with the aim of achieving tunable sensitivity as featured by the human body. Sec. II revises the state-of-the-art ROCs for

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tactile sensors in humanoid robots and briefly outlines the Capacitance-to-Digital Converters (CDCs). The parameters needed for the co-design of the sensor and the read-out unit are presented in Sec. III, while circuit-level design is detailed in Sec. IV. Sec. IV-C presents post-layout simulations and Sec. V outlines the circuit performance. The overall system comprising the ROC and the sensing material, described in Sec. VI, is, then, validated in Sec. VII. Finally, a comparison w.r.t. state-of-the-art ROCs and CDCs is provided in Sec. VIII and conclusions are drawn.

II. Position in current research

In humanoid robots, scalable and modular tactile sensor arrays are generally interfaced with commercial components, which locally convert the sensor analog signal into a digital output. In particular, microcontrollers are the most adopted blocks to process data from tactile sensors (e.g., [2], [3], [13]–[15]), as they permit to perform several tasks and handle multiple channels, at the cost of high power consumption (ranging within $1-1000$ mW, considering the maximum current at full-power mode [2], [13], [15]) and large chip size. Recently, commercial MEMS comprising the sensor and the electronic read-out in the same package have been proposed [16]. However, despite the compact layout and the low-power consumption ($\sim$16.5 μW), this solution loses interest for robotic skin applications, due to the impossibility of tuning the sensitivity along the robotic body and separate the electronic and sensing parts, in case of failure.

Flexible electronics is also attracting increasing attention to replicate human skin flexibility in humanoid robots [17], [18]. Since bendable electronics are still facing major technological problems, soldering the off-chip electronic and sensing components on flexible substrates is one of the most accepted solutions [17] and, in these cases, area-consuming microcontrollers are generally replaced with compact Analog-to-Digital Converters (ADC) to interface tactile sensor arrays (e.g., [1], [4], [19]).

Nevertheless, all the aforementioned commercial components are not designed to be aggressively array replicated, because of their high power consumption and large active area. Furthermore, even if smart assignment of modules can help to reduce the number of wires, the presence of analog circuits prevent to reach high scalability.

In state-of-the-art CDCs, several works exploit a ring oscillator and different solutions are implemented to handle the output frequency. In [20] a phase detector measures the phase difference w.r.t. a digitally steered oscillator: the sensor value, hence the frequency variation, is proportional to the duty cycle at the phase detector output, once the Phase Locked Loop (PLL) is locked. When a Ring Oscillator (RO) is powered from a charged capacitance, the number of RO cycles required to discharge the capacitance to a fixed value is linear with the capacitor value. This mechanism is used in [21] to evaluate the capacitance by a comparator and a counter. Finally, the solution presented in [22] computes the pulse width of the RO output. Commonly, in these ring oscillator-based ROCs, the sensor is single-ended connected to the electronic interface and calibration systems are implemented to counterbalance sensor parasitic capacitance and partially attenuate deviation due to PVT variations. For instance, in [21] a one-point calibration is obtained by discharging a reference capacitor (with known capacitance) and storing the ratio between the capacitance and its correspondent digital output. This value is later used to convert digital values back into capacitance.

The presented ROC is designed to be scalable, modular and robust against PVT variations, which are all generally not featured by the state-of-the-art CDCs, especially the analog ones.

The most exploited alternative to RO-based CDCs are analog circuits, e.g., Successive Approximation Registers (SAR) [23], switch-capacitors $\Sigma-\Delta$ ADCs [24], and single comparators [25], [26], which generally lead to higher design complexity. Commonly, SAR ADCs feature lower conversion energy but limited resolution, while switch-capacitors $\Sigma-\Delta$ converters achieve higher resolution at the cost of larger active area and poor conversion energy. Even though the performance in term of resolution and ENOB could be higher, ADCs may not be the best solution for this specific application, since low active measurement time, small area and tunable sensitivity are needed. Viceversa, the presented solution features all aforementioned requirements, as it has active measurement time of 4 μs only, a compact active area of $221 \times 79\,\mu\mathrm{m}^2$ and sensitivity can be tuned at design or sensor level.

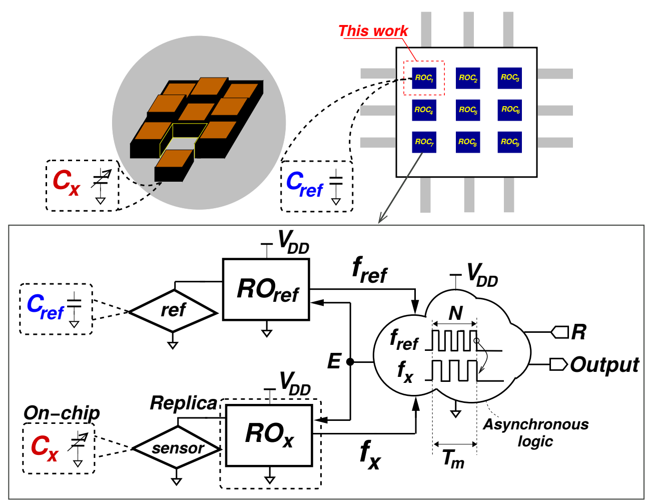


Fig. 1. Schematic of the ROC which can be co-designed with the MW-CNT nanocomposite transducer, to tune the ROC sensitivity by properly adjusting the sensor thickness. The relative count detection scheme is depicted in the red box. C_x and C_{ref} are, respectively, under test and reference capacitors. The relative frequency of two Ring Oscillators (ROs) $\frac{f_x}{f_{\mathrm{ref}}}$ is used to quantitatively determine the value of C_x, detected by counting the number of $\mathtt{RO}_\mathrm{x}$ events within N $\mathtt{RO}_\mathrm{ref}$ clock cycles.

III. System-level Design

Fig. 1 schematizes the read-out scheme used to quantify the transducer capacitance, based on a relative count detection. One of the two ring oscillators, $\mathtt{RO}_\mathrm{x}$, is loaded single-ended with the capacitor under test C_x, while the other ($\mathtt{RO}_\mathrm{ref}$) is connected to a reference capacitor C_{ref}, When read signal $\mathtt{R}$ goes high, the two digital oscillators are asynchronously duty cycled

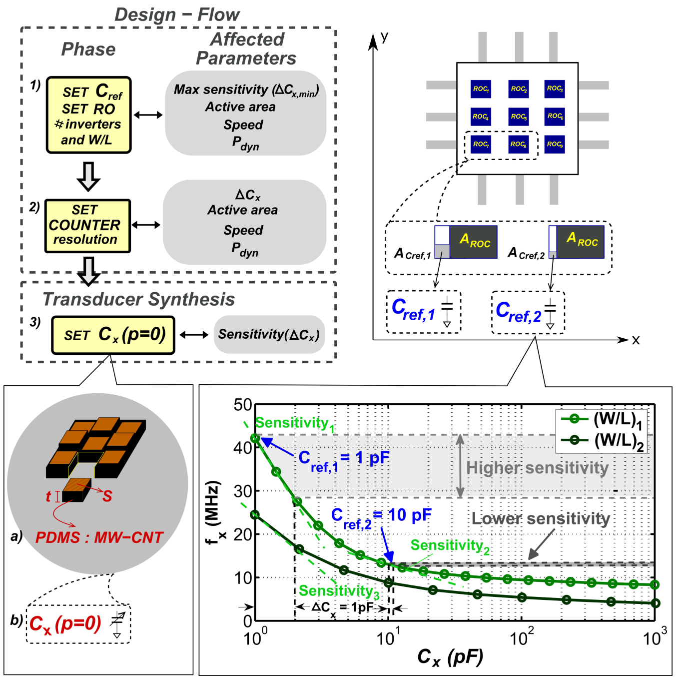


Fig. 2. Circuit and transducer co-design parameters. The RO number of inverters and inverter aspect ratio determines the behavior of the output frequency w.r.t. the capacitive load, while C_{ref} decides the reference frequency along the curve, where the targeted maximum sensitivity is achieved. For instance, fixing the RO design (i.e., the f_x trend), a capacitive variation (i.e., $\Delta C_x = 1\,$pF) can be associated to different output, according to the C_{ref} bias. The nominal capacitance of the transducer can be properly modulated to vary the sensitivity w.r.t. its maximum value, obtained when $C_{\mathrm{ref}} = C_x(\mathrm{p}=0)$. Using a MW-CNT nanocomposite sensor, $C_x(\mathrm{p}=0)$ can be adjusted either chemically or physically.

in parallel with activation signal E, and both provide quasi-digital conversion and timing reference for the successive asynchronous logic without other external references besides voltage supply V_{DD}. To quantitatively evaluate C_x, the $\mathrm{RO_{ref}}$ output is used by the asynchronous logic to stop $\mathrm{RO_x}$ after a number of $\mathrm{RO_{ref}}$ clock cycles N, for an active measurement time T_m. Both RO frequency (f_x and f_{ref}) are locally affected by the same global PVT variations but, as further detailed in Sec. IV, as a first approximation $\frac{f_x}{f_{\mathrm{ref}}}$ depends only on C_x. The next logic counters which by-design meet both ROs timing requirements, provides relative count Output following the same PVT variations of the oscillators, thus providing robust operation.

As introduced in Sec. I, this work presents a circuit that was conceived with the important feature of allowing the co-design with the transducer, to properly tune sensitivity, without re-designing the overall architecture. Fig. 2 outlines the main design-parameters to be considered: 1. C_{ref} (f_{ref}) and the RO number of inverters and inverter $\frac{W}{L}$, 2. the counter bit resolution and 3. the nominal sensor capacitance at zero pressure $C_x(\mathrm{p}=0)$.

1. The sensitivity, limited by the RO flicker noise [27], can be tuned by exploiting the hyperbolic dependence of the RO frequency w.r.t. the capacitive load. The trend of RO frequency is determined by the number of inverter and the inverter aspect ratio, while C_{ref} decides the operative frequency f_{ref} along this curve, where the maximum targeted sensitivity is achieved. In fact, the ROC sensitivity is maximum when the reference and nominal sensing capacitance at zero pressure match ($C_{\mathrm{ref}} = C_x(\mathrm{p}=0)$). The bottom plot in Fig. 2 shows that (with a fixed RO design) the RO frequency curve presents different first derivatives according to the C_{ref} operating point. Therefore, the frequency variation corresponding to a fixed ΔC_x (e.g., 1 pF in Fig. 2) directly depends on the C_{ref} bias.

Viceversa, fixing C_{ref}, the RO number of inverters and $\frac{W}{L}$ determines the RO frequency curve trend w.r.t. the capacitive load, hence the ROC response to a certain ΔC_x. Simulations show that in our process $C_{\mathrm{ref}} = 100\,$fF and $C_{\mathrm{ref}} = 10\,$fF determine a sensitivity 4 and 10 times higher w.r.t. the case with $C_{\mathrm{ref}} = 1\,$pF.a

Therefore, a proper trade off between the RO design and C_{ref} value must be achieved to obtain the targeted sensitivity. Observe that a change of C_{ref} could impact the ROC active area (A), which is essential to keep into account when an aggressive integration of multiple ROCs is necessary. The overall ROC A can be split in two contributions related to the digital logic ($\mathrm{A_{ROC}}$) and the reference capacitance ($\mathrm{A_{Cref}}$), respectively. While $\mathrm{A_{ROC}}$ is a constant term, which depends on the technology used to implement the circuit, the contribution of $\mathrm{A_{Cref}}$ is linear with C_{ref}, i.e., $\mathrm{A_{Cref}} = \alpha \mathrm{C_{ref}}$, with $\alpha = 86.67\,\mathrm{pF}/\mu\mathrm{m}^2$ and becomes relevant for $C_{\mathrm{ref}} > 1\,$pF. For instance, with C_{ref} ranging from 100 fF to 1 pF, A is affected by a variation of 0.5% only (as $\mathrm{A_{ROC}}$ is the dominant term), while with $1\,\mathrm{pF} < C_{\mathrm{ref}} < 10\,$pF, A can vary up to 4.75 %.

In the herein presented solution, the system must detect a minimum capacitive step $\Delta C_{x,min}$ of at least 10 fF/LSB, with a reference capacitance of 1 pF. Hence, we ran parametric simulations at transistor-level on the RO number of inverters and inverter $\frac{W}{L}$ to maximize the RO relative frequency variation when the capacitive load varies by $\Delta C_{x,min}$, i.e., $\frac{\Delta f_x}{f_{\mathrm{ref}}} = \left(\frac{f_{\mathrm{ref}} - f_x(C_{\mathrm{ref}} + \Delta C_{x,min})}{f_{\mathrm{ref}}}\right)$. To be acceptable, the designed $\frac{\Delta f_x}{f_{\mathrm{ref}}}$ must guarantee at least a bit toggle of the ROC output when the sensing capacitance varies of $\Delta C_{x,min}$.

The RO design directly affects speed, active area and power consumption, hence proper trade-off must be reached, as detailed in Sec. IV-A.

2. The counter bit resolution is chosen primarily to match the requirements of successive electronic blocks but it can also affect $\Delta C_{x,min}$ and dynamic range. In first approximation, the longer the counting, the higher the resolution and the lower the dynamic range. In fact, a small frequency (i.e., capacitive) variation can be detected if the delay of each inverter stage can accumulate long enough to cause a bit toggle in the counter. However, a $\Delta C_{x,min}$ tuning through bit resolution comes at the cost of higher power consumption, due to the longer activation of the ROs, and larger active area.

3. Once the RO design is fixed to target a minimum $\Delta C_{x,min}$, the sensitivity can be further modified by tuning the nominal sensor capacitance at zero pressure $C_x(\mathrm{p}=0)$. In fact, when $C_x(\mathrm{p}=0) = C_{\mathrm{ref}}$, f_x lies within a frequency region around the operative frequency (set at step 1 by C_{ref}), which permits to detect the targeted $\Delta C_{x,min}$ (i.e., maximum sensitivity). Viceversa, if $C_x(\mathrm{p}=0)$ differs from C_{ref}, the sensitivity decreases and the detectable $\Delta C_{x,min}$ increases, as shown in Sec. VII. This

feature can be exploited to replicate the different sensitivity range along the human body. As detailed in Fig. 2, the herein presented material $C_x(\mathrm{p}=0)$ can be modified both physically and chemically, by properly a) sizing the sensing module (active area S and thickness t), b) setting the percentage of MW-CNT and PDMS (see Sec. VI) to obtain a target sensitivity. This method permits also to recover the maximum sensitivity in case of PVT variations on the integrated C_{ref}, while the residual capacitance mismatch due to transducer deployment and packaging parasitic can be effectively recovered by running calibration. More details on the calibration system are provided in Sec. IV-B.1. In Sec. VII, we demonstrate that the sensitivity can be successfully tuned by modifying the sensor section S, i.e., $C_x(\mathrm{p}=0)$. The effect of the other parameters will be studied in future implementations.

In the presented ROC, the number of bit is 8 by design and the frequency is chosen to be within 300 kHz and 50 MHz, to have i) a computational measurement $< 10\mu$s, ii) a power consumption $< 10\mu$W. Receptive cells in human skin generally react to stimuli at different frequency, hence the response time requirements of the sensors (and, consequently, the read-out frequency of the sensor interface) must match the range to which the different mechanoreceptors react [28]. This notwithstanding, as concluded in [28], in robots each tactile sensor is expected to respond at least 1 kHz rate to real time detect contacts, hence the circuit read-out time can be practically set to 1 ms.

IV. Circuit-level Design

A. Ring Oscillator and Detector Analysis

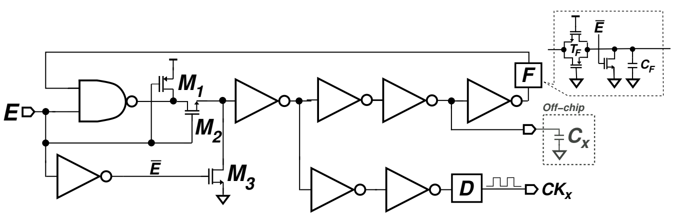


Fig. 3. Schematic of the RO. F implements a single pole RC low-pass filter, E is the enable signal, D is a frequency divider and C_x is the external load.

Fig. 3 shows the schematic of the RO. When pressure is applied, C_x is assumed to increase, causing in turn the $\mathrm{RO_x}$ frequency f_x to decrease, as the circuit needs more time to charge and discharge the capacitor.

As described in III, we run parametric simulations to maximize $\frac{\Delta f_x}{f_{\mathrm{ref}}}$ for a 10 fF ΔC_x, with $C_{\mathrm{ref}} = 1$ pF. The number of inverter was ranged within 3–25 (only odd numbers are considered), L was varied within 120 nm and 8 μm, and W within 120 nm and 2.4 μm, for a maximum output frequency f_x at $C_x = C_{\mathrm{ref}} = 1$ pF included in the interval 300 kHz–50 MHz. After simulating all combinations, the maximum $\frac{\Delta f_x}{f_{\mathrm{ref}}} = 0.34\%$ is obtained by setting the number of inverting elements to 5 and the aspect ratio to $(\frac{W}{L})_n = \frac{160}{120}$ and $(\frac{W}{L})_p = \frac{480}{120}$. This small relative variation still guarantees an output bit toggle for $\Delta C_x = 10$ fF. To fit the targeted frequency range, two toggle flip-flops are added as asynchronous 2^2 frequency dividers (D), without exploiting area-consuming capacitors.

To duty cycle and power off the RO, we use dedicated switches asynchronously activated by the enable signal E, that interrupts the loop ($\mathrm{M_2}$). A single pole low-pass filter F, implemented with a minimum sized transmission gate T_F and a 500 fF MOS capacitor C_F, is added to filter spurious glitches, due to the RO fast switching oscillation transients. The bottom plot in Fig. 2 depicts the effects of C_x on f_x. Even if the trend is hyperbolic, it can be linearized for small C_x variations, as demonstrated in Sec. V-A when $\Delta C_x < 100$ fF. Observe that the sensitivity tends to decrease for high capacitive loads.

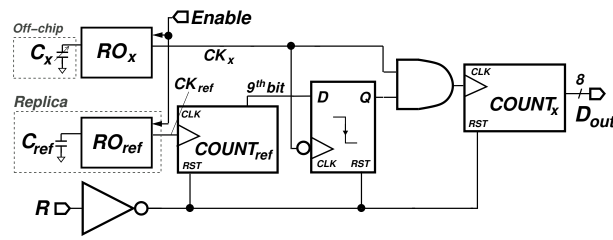


Fig. 4. Schematic of the relative count detector sub-system. Each RO output feeds a different counter: the 9th bit toggle is synchronized by the D flip-flop, before freezing $\mathrm{COUNT_x}$ clock. R is the read signal, positive edge triggered, and D_{out} is the output data.

Fig. 4 shows the schematic of the relative count detector, realized following these considerations. The detector includes two ring oscillators [$\mathrm{RO_x}$ and $\mathrm{RO_{ref}}$, $\mathrm{CK_x}$ and $\mathrm{CK_{ref}}$ outputs, with common enable signal (Enable)] respectively connected to C_x and $C_{\mathrm{ref}} = 1$ pF, both working as clock generator for the downcounters $\mathrm{COUNT_x}$ (8 bit) and $\mathrm{COUNT_{ref}}$ (9 bit), running in parallel for an overall count of N=256. For the duration in which $\mathrm{RO_{ref}}$ runs a fixed number of periods N, in our design 256, $\mathrm{RO_x}$ will always run a number of periods independent on temperature or V_{DD}, function of C_x only.

When no pressure is applied and nominally $C_x(\mathrm{p}=0) = C_{\mathrm{ref}} = 1$ pF, the two ROs run at the same frequency (from simulations, $f_x = f_{\mathrm{ref}}$ =42.31 MHz, 50 % duty cycle) and $\overline{\mathrm{COUNT_x}}$ gets to the maximum value $'11111111'$. Contrariwise, when a certain pressure $p_x > 0$ is applied and $C_x(\mathrm{p}>0) > C_{\mathrm{ref}}$, more time is required for charging and discharging C_x, hence $f_x < 42.31$ MHz, causing, in turn, $\overline{\mathrm{COUNT_x}}$ to get to a value $< '11111111'$. Ripple effects need to be prevented for both downcounters, hence, we use the $\mathrm{COUNT_{ref}}$ 9th bit as terminal count signal, synchronized by-design with an $\mathrm{RO_x}$ output falling edge, to avoid glitches generation. The output D_{out} is then available when the 9th $\mathrm{COUNT_{ref}}$ goes to '0' and gates the CLK input of $\mathrm{COUNT_x}$. The calibration system, discussed later, eliminates offsets, so that a $'00000000'$ output can be set when no pressure is applied.

PVT variations have often represented an issue in IC design, as the circuit must guarantee fault-free operation within a temperature and V_{DD} working range and in case of mismatch and variations of fabrication parameters w.r.t. nominal values [29]. In the presented ROC, robustness to global PVT variations is achieved thanks to the architecture organization, based on a two-level differential measurement. The first level is embedded in the relative count technique and it is due to the mutual trigger (stopping clock) between the oscillators. In fact, even if the read-out time may change because of PVT variations,

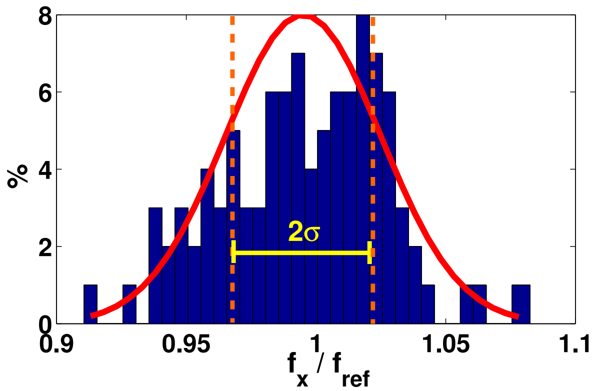


Fig. 5. $\frac{f_x}{f_{\mathrm{ref}}}$ distribution due to process variation, 100 Monte Carlo simulation runs (worst case with both mismatch and process variations), with superposed Gaussian fitting curve ($\sigma = 0.027$).

the result of the RO self-synchronization is unaffected, hence, the number of rising edges within N reference rising edges depends on C_x only. The second level is achieved thanks to the calibration-system, which nulls the effect of assembly parasitic and reduces even more the residual effects of temperature and V_{DD} variations (see Sec. IV-B.1).

At layout-level, local process variations are partly reduced by placing the two ROs (featuring a very small active area) close in the chip. We run 500 ns process and mismatch Monte Carlo simulations (worst case, 100 runs) on the circuit in Fig. 4 to estimate the impact of process variations on the relative count detection architecture, for $C_x = 1.01$ pF and $C_{\mathrm{ref}} = 1$ pF. Fig. 5 shows the recurrence of $\frac{f_x}{f_{\mathrm{ref}}}$ in adjacent intervals of 5‰. All data fit a Gaussian spreading curve with standard deviation $\sigma = 0.027$. From the analysis, we conclude that process variations can still affect the measurements, but, even in presence of mismatch, the $\pm 2.7\%$ relative frequency variation can be still effectively recovered by the calibration logic. Moreover, the target sensitivity can be recovered even in presence of C_{ref} fluctuations by properly co-designing the sensing element $C_x(\mathrm{p}=0)$ to match C_{ref}.

Fig. 6 demonstrates that f_x linearly depends on both temperature and power supply but f_x/f_{ref} is almost unaffected by V_{DD} and temperature variations. As a consequence, the number of $\mathtt{RO_x}$ rising edges included within a finite number of $\mathtt{RO_{ref}}$ rising edges, i.e., the ROC digital output, can be, in first approximation, considered independent on temperature and V_{DD} fluctuations.

The finite degree of residual sensitivity to supply voltage and temperature is investigated, by interpolating f_x/f_{ref} with a first degree polynomial curve and studying the angular coefficients K_{Vdd} and K_{T} ($f_x/f_{\mathrm{ref}} \propto K_{\mathrm{Vdd}} V_{\mathrm{DD}}$ and $f_x/f_{\mathrm{ref}} \propto K_{\mathrm{T}} \mathrm{T}$). K_{Vdd} and K_{T} depend on the input capacitance variation w.r.t. the reference value ($\Delta C_x = C_x - C_{\mathrm{ref}}$), e.g., for $\Delta C_x = 10$ pF, K_{Vdd} and K_{T} are lower than 10% and 0.02%, respectively. Considering the impact on the resolution ($\Delta C_x = 10$ fF), the maximum $\Delta(f_x/f_{\mathrm{ref}})$ are 1.66 % and 2.7 %, for $\Delta\mathrm{T} = 110\,^{\circ}$C and $V_{\mathrm{DD}} = (1.1 \pm 0.1)$ V, respectively. These values lies within the mismatch standard deviation analyzed, hence, they can be considered negligible. The output can be considered PVT robust also because the target sensitivity is $\sim$ tens of fF. When an even higher sensitivity is required, other solutions need to be implemented to further nullify PVT effects.

B. Read-Out Circuit

Fig 7 shows a simplified schematic of the entire ROC architecture. Correct timing is guaranteed using *ad hoc* monostable element cells as delays, rather than inverters, for ease of configuring and to have long delays (in this design $\sim$90 ns) in a limited silicon area. When $\mathtt{COUNT_{ref}}$ counter gets to 2^8=256, i.e., the 9^{th} bit toggles, the clock of $\mathtt{COUNT_x}$ is frozen and the result is read, inverted and stored in the register $\mathtt{REG_x}$, after a delay $\mathtt{D_1}$. This delay must be introduced before sampling the $\mathtt{COUNT_x}$ output, to guarantee that each bit terminates its toggling transient, after the last rising edge of the clock. Delay duration is controlled by capacitor C_D, MOS-based and nominally 3 pF. The monostable element, whose schematic is depicted in the dotted box, is also used to ensure proper timings of critical signals and guarantee registers CLK sampling with large set-up margins. In the following subsections we introduce calibration, data transfer and a system-level operation diagram.

1) Calibration: When $\mathtt{C}$ is high, the $\mathtt{COUNT_x}$ inverted output is also saved in the register $\mathtt{REG_{cal}}$. The correct timing is guaranteed by $\mathtt{D_4}$ (comprising a chain of 8 inverters), while $\mathtt{D_1}$ and $\mathtt{D_2}$ gate the $\mathtt{CLK}$ signal of the calibration register. The saved offset is maintained until the next calibration occurs and it is subtracted from the $\mathtt{REG_x}$ output after a new measurement. The 2's complement difference is implemented with an 8 bit full adder, with the first carry equal to '1' and by inverting the $\mathtt{REG_{cal}}$ output. $\mathtt{D_3}$ allows all bits to be calculated correctly, before being saved in the sum register $\mathtt{REG}$. With this simple but effective calibration technique, output is set to $\mathtt{Output}$ = '00000000', when $C_x = C_{\mathrm{ref}} = 1$ pF and insensitivity to thermal drifts is increased.

We have demonstrated that a 10 fF ΔC_x causes a bit toggle in $\mathtt{COUNT_x}$ and a $\frac{\Delta f_x}{f_{\mathrm{ref}}} = 0.34\%$. Considering the linear relation of f_x/f_{ref} w.r.t. T (presented in Sec. IV-A), we must assure that $\Delta f_x/f_{\mathrm{ref}}$ caused by temperature drift is minor than 0.34%. In other words, temperature fluctuation must not cause a bit toggle, which would lead to the misleading detection of a false positive 10 fF ΔC_x. Using $\Delta f_x/f_{\mathrm{ref}} = K_{\mathrm{T}} \Delta\mathrm{T} < 0.34\%$, we conclude that we can still recover temperature effects with a calibration period minor or equal to 17 s, assuming a fast thermal process of 1 °C/s.

2) Serializer: Output data transfer is achieved with a Parallel Input Serial Output (PISO) register, configured to work as an SPI when 8 clock periods are provided by the successive electronic blocks. When the $\mathtt{COUNT_{ref}}$ 9^{th} bit toggles, after a delay $\mathtt{D_5}$, it is inverted, sampled and reused as data ready signal $\mathtt{DR}$. This signal is synchronized with $\mathtt{REG}$ clock using a re-sampling flip-flop further used as enable signal for the PISO unit. The read signal $\mathtt{R}$ both triggers a single measurement cycle and, when disabled, operates as a reset signal for all flip-flops and counters.

3) Operation Diagram: Fig. 8 shows the basic operation and the timing of the most important signals depicted in Fig. 7

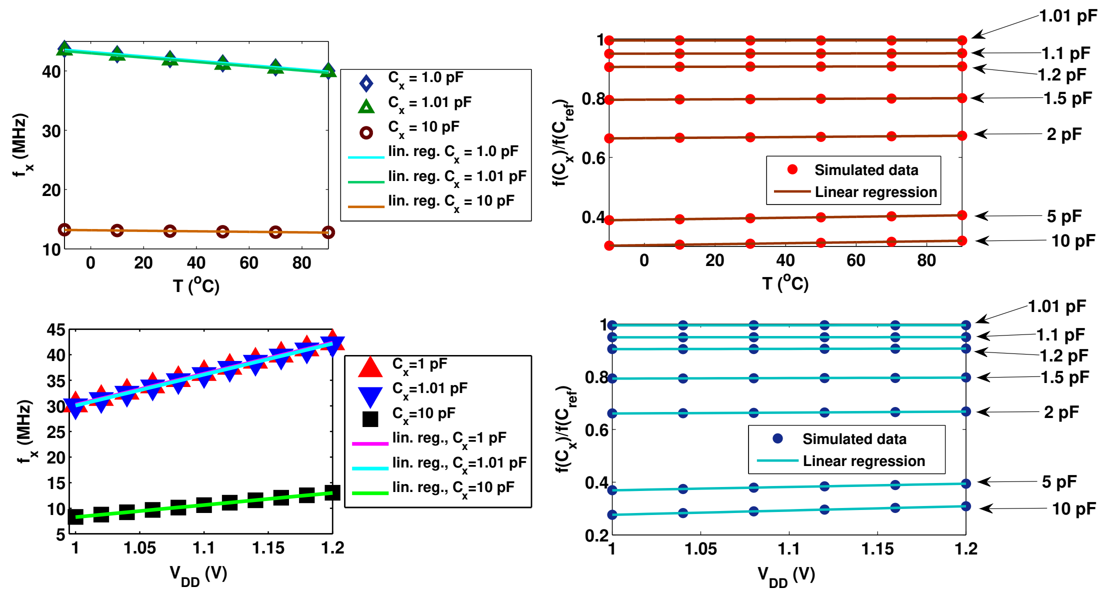


Fig. 6. *First Column:* simulated RO frequency f_x as a function of temperature at 1.0 V (top) and as a function of V_{DD} (bottom). Both simulated data and linear regression are shown for C_x=1 pF, C_x=1.01 pF and C_x=10 pF. *Second Column:* $\frac{f_x}{f_{\mathrm{ref}}}$ (C_{ref} = 1 pF) as a function of temperature (top) and supply voltage (bottom) at different C_x [12]. In first approximation, $\frac{f_x}{f_{\mathrm{ref}}}$ is independent on both T and V_{DD}.

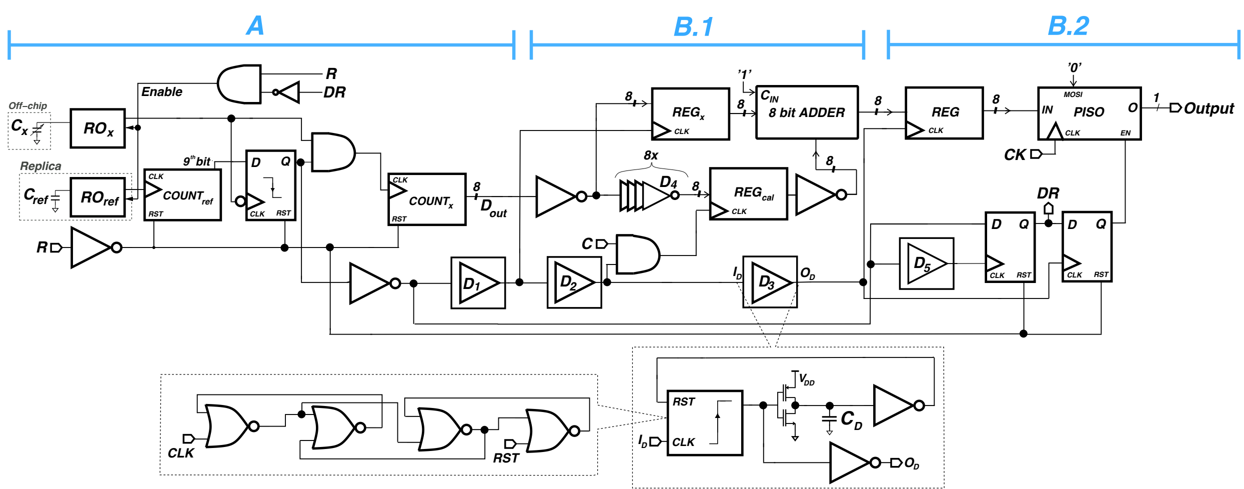


Fig. 7. Simplified schematic of the ROC. C_x is the external load, C_{ref} = 1 pF, C is the calibration pin, active high, R is the read signal, DR is the data ready signal which is used to load the 8 bit output in the PISO, working with an external clock CK. The dotted schematic show the internal architecture of D_i (i=1, 2, ..., 5), where C_D sets the delay between I_D and O_D. In the top part of the figure, blue labels show the sub-parts of Sec. IV where each block is described.

for an entire measurement cycle. The signals in the yellow box are obtained with active calibration and $C_x = C_{\mathrm{ref}} = 1$ pF. Since $\mathtt{CK_x}$ and $\mathtt{CK_{ref}}$ periods are the same, the two downcounters are synchronized, hence when $\mathtt{COUNT_{ref}}$ reaches $'256'$ (in decimal system), $\mathtt{COUNT_x}$ overflows to $'0'$. The inverted $\mathtt{COUNT_x}$ output is saved in both $\mathtt{REG_x}$ and $\mathtt{REG_{cal}}$, and their difference $\mathtt{Output} = '00000000'$.

When the calibration is disabled and C_x varies under the action of an external force, $\mathtt{CK_x}$ frequency lowers, causing $\mathtt{COUNT_x}$ to run slower w.r.t $\mathtt{COUNT_{ref}}$ (e.g., $'8'$ instead of $'0'$ in Fig. 7). The inverted $\mathtt{COUNT_x}$ output is saved in $\mathtt{REG_x}$ and subtracted to the previously saved $\mathtt{REG_{cal}}$ value ($'255'$), leading to $\mathtt{Output} = '00001000'$. T identifies the transients before the RO oscillation becomes stable. The event-driven circuit consumes active current I_{on} only during measurement time T_m, i.e., the delay between the rising edges of R and DR, corresponding to the logic computing time to run a single measurement.

C. System-level Simulations

We simulated the ROC both at transistor and post-layout levels to verify that i) it can detect $\Delta C_x = 10$ fF with one LSB toggle, ii) the calibration system works correctly, zeroing the output when $C_x = C_{\mathrm{ref}} = 1$ pF, and iii) the ROC is robust, as described at design-level in Sec. IV-A and experimentally demonstrated in Sec. V-A.2. In simulations the read time is set to 1 ms. The average simulated power consumption $\bar{P}$ when R is active is 5.94 μW and it is calculated as $\bar{P} = \frac{\int_0^{T_s} I(t)\, V_{\mathrm{DD}}\, dt}{T_s}$,

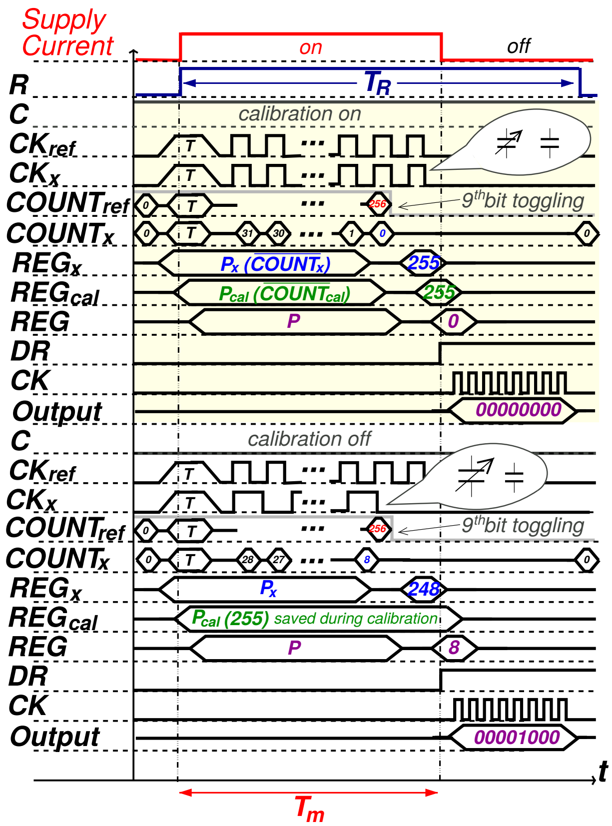


Fig. 8. Signal timing of the most important signals: two examples are shown, first enabling the calibration (yellow box) and, second, disabling the calibration and modifying C_x, with no parasitic. T highlights the transient before the RO oscillation becomes stable (~ 100 ns from simulations). Notice that registers are never reset, but just overwritten and all counter are downcounting. When calibration is active and $C_x = C_{\mathrm{ref}} = 1$ pF (i.e., no pressure is applied), the inverted counter output is saved in the calibration register and Output $=$ '00000000', as $\mathrm{P_x} = \mathrm{P_{cal}}$. When the calibration is off and $C_x \neq C_{\mathrm{ref}}$ (i.e., the pressure is applied), the inverted counter output is saved in $\mathrm{P_x}$ and subtracted to the previously calibrated offset ($\mathrm{P_{cal}}$), for an Output $=$ '00001000'.

where T_s=1 ms and $V_{\mathrm{DD}} = 1.2$ V. The simulated leakage power obtained when R is low (and all logic is inactive) is 879 nW at $V_{\mathrm{DD}} = 1.2$ V. Simulations with temperature in the range (-10 – 90) °C are run to verify the correct operation of the logic blocks depicted in Fig. 4 (particularly the $\mathrm{COUNT_x}$) and the correct operation is experimentally demonstrated in Sec. V. The most significant simulations are post-layout, since we expect that due to additional routing delay, on-chip parasitic capacitance i) reduces f_x, ii) impacts on sensitivity $\Delta C_x = 10$ fF and iii) consequently generates an output $\neq$ '00000000' for $C_x = C_{\mathrm{ref}} = 1$ pF. The maximum PISO operation frequency is 10 MHz. As our experimental set-up has been designed to favor small capacitance measurements and it is limited for large values, simulations permit an estimation of the maximum capacitance, leading to an input range of 1 pF – $\sim$10 nF.

V. ROC Validation

Fig. 9 shows the layout of the chip ($221 \times 79\,\mu\mathrm{m}^2$), with the most significant terminals highlighted and the chip microphotograph, (100× optical zoom). All logic cells (full custom) have been manually floorplanned and the metallic layers have been arranged to reduce the parasitic capacitance around the oscillators, that can potentially impact on the read-out performance.

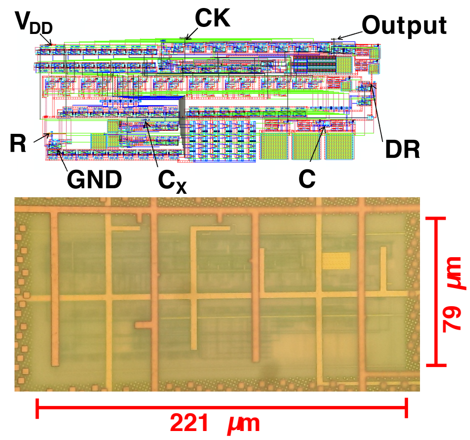


Fig. 9. Layout (top, $221.54 \times 79.17\,\mu\mathrm{m}^2$ active area) and chip microphotograph (bottom, optical zoom 100×).

The circuit is prototyped in a 130 nm RFCMOS technology (HS transistors) and bonded on a 48-pin QFN, with other circuits sharing the same die. The QFN package introduces a small parasitic capacitance, which does not significantly affect C_x measurements [30]. The PCB design is focused on the reduction of parasitic capacitance, hence, the ground plane has been eliminated under the capacitance to test and the PCB striplines of the C_x terminal have been routed straight to the chip. Moreover, we used a high PCB thickness of 3.2 mm to reduce parasitic capacitance between the metallic lines on the top layer and the bottom ground plane. Lastly, careful stripline routing and spacing have been considered not to inject interference on the C_x terminal. The PCB includes an MSP430G2553 microcontroller, which cyclically runs calibration once every million measurements with $T_{\mathrm{R}} = 100$ ms, controls the activation of inputs, collects each measurement output and displays results on a laptop. The microcontroller drives the CK signal of the PISO with a period T_{CK}, which may change depending on the running microprogram (maximum 1 MHz). To interface to the microcontroller, the ROC I/O signals are translated to 3.3 V using dedicated SN74AUP1T34 level-shifters. In Sec. V-A, we previously show the circuit response to a variable input capacitance C_x before presenting in Sec. VII the results of the ROC interfacing a capacitive tactile sensor. A 7 mm surface mount plastic dielectric capacitor, operating in a wide temperature range (-25 – 85)°C) is used to trim the external load C_x. Before use, we calibrated the trimmers through impedance measurements (using Agilent 4294A precision impedance analyzer), in a frequency range 1 Hz – 1 MHz and we verified that the impedance linearly depends on the rotation angle.

A. Experimental Results

1) Sensitivity: We measured the average sensitivity, extrapolating the average capacitance variation associated to one LSB toggle under linear operation. Hence, we interpolated measurement data with a linear regression curve (calibration curve) and computed the reciprocal of its slope. We first calibrated the system at $C_x = C_{\text{ref}} = 1\,\text{pF}$, then, we trimmed C_x to cover all digital outputs, in the range $'00000001'$–$'00001101'$. Fig. 10 shows the calibration curve, from which we extrapolated a sensitivity of 5.23 fF, consistent with simulations. ΔC_x associated to the maximum output variation ($'00000000' - '00001101'$) is 71.7 fF. The actual computational time to perform a single measurement (T_m) is $\sim 4\,\mu$s, much lower than T_R, which is chosen to be 1 ms to be compliant with human tactile read-out time.

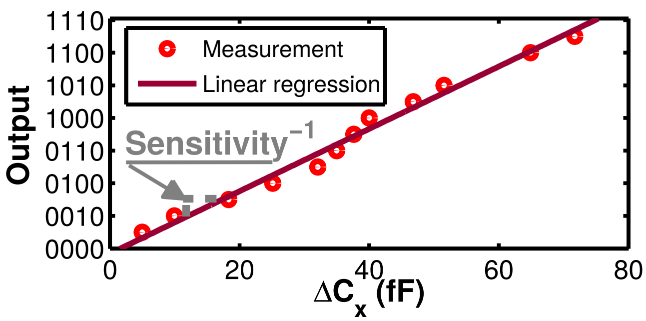
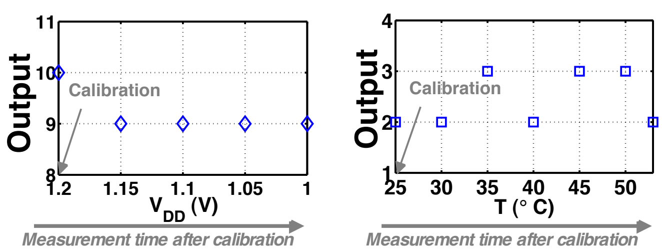


Fig. 10. Calibration curve, measured data and linear regression, with sensitivity of 5.23 fF/LSB.



(a) (b)

Fig. 11. Measured `Output` after initial calibration and a dynamic V_{DD} (a), and temperature (b) variation.

2) Robustness: In the experiments we calibrated only once at the beginning of all sessions, to provide a constant and invariant C_x, consistent for same measurement data-sets. Fig. 11(a) demonstrates DC power supply robustness. After the system was calibrated at $V_{\text{DD}} = 1.2\,\text{V}$ and the output was adjusted to $'00001010'$, the voltage supply was decreased with steps of 50 mV, to 1.0 V. Despite a variation for the first 50 mV (probably due to a count stop on the edge of the $'00001001'$ value), `Output` remained constant in a range of 0.15 V, exhibiting no further variations. We observed that read-out output is very stable, as data remained unvaried for at least 1000 consecutive measurements after a single calibration. Hence, we can conclude that the design can be considered even robust to noise. In case of an extremely noisy environment, noise robustness can be further improved by calibrating the ROC at higher rate.

To verify temperature robustness, the chip was warmed up by a hot plate, placed directly in contact with the PCB and a thermocouple measured temperature in the surroundings of IC. We could not obtain temperatures higher than 53 °C, due to dissipation and low thermal conductivity of the FR4 PCB. Results in Fig. 11(b), show `Output` was constant until T$< 35\,°$C, then the system toggled between two consecutive values. Observe that the LSB toggling could be removed if calibration was re-run when DC supply voltage and temperature conditions varied.

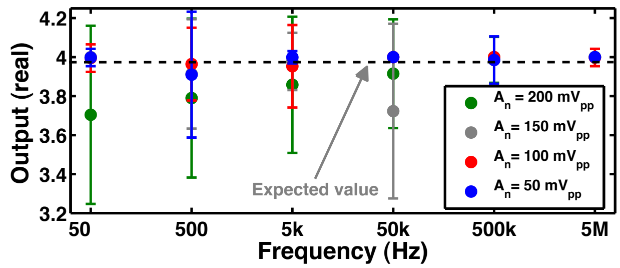


Fig. 12. Power supply sine wave rejection for different peak-to-peak amplitude A_n ($50-200\,\text{m}V_{\text{pp}}$), V_{DD}=1.1 V, expected value $'00000100'$. With such level, the standard deviation is below one LSB.

As in commercial components actually used in humanoid robots (see, e.g., the commercial product [31] used in [1]), we measured power supply sine wave rejection for T_R=1 ms and V_{DD}=1.1 V, whose mean and standard deviation are computed (calibration was run once for each data-set). A sine wave with variable amplitude in the range $50-200\,\text{m}V_{\text{pp}}$ and 5 orders of magnitude frequency range was injected on the supply line and 1000 consecutive measurements were run. Fig. 12 shows that, even in presence of large sine amplitude A_n, i) the average `Output` (now plotted in real values) is very stable and matches the expected value, ii) the standard deviation is lower than one LSB.

In fact, since the two ROs share the same V_{DD}, they are both modulated in the same way when an AC signal is injected in the supply terminal. Their instantaneous relative delay relationship, though, remains unvaried leading to a constant output depending on C_x only, which proves again the ROC robustness to V_{DD} within 1.0–1.2 V.

3) Power Consumption: Supply current was measured with the electrometer Keithley 6517B in series to the the V_{DD} supply line and with a voltage meter in parallel, to detect only the power effectively consumed by the ROC, leaving out the off-chip microcontroller and level-shifters. With the current IC we could not measure leakage of the sole ROC, as we shared power lines with other circuits. The measured current includes both static ($\bar{I}_{\text{off}}$) and dynamic ($\bar{I}_{\text{on}}$) contributions. The static contribution was measured with `R` disabled and includes the ROC leakage and the DC power consumed by other systems integrated on the same die. At V_{DD}=1.2 V, the measured $\bar{P}_{dyn}$ is 1.84 μW, 3.3 times lower than simulations under nominal process conditions. Also the measured $\sim$4 μs T_m differs from the expected $\frac{256}{42.31\text{MHz}} \sim 6\mu$s. The measured T_m and power consumption is lower w.r.t. simulated values, while the sensitivity is higher, which can be all attributed to a $C_{\text{ref}} < 1\,\text{pF}$, caused by PVT variations. This notwithstanding, the circuit has been verified to operate correctly providing this way a qualitative validation to process robustness. Dynamic power consumption can be further decreased to 1.21 μW, if

V_{DD} is brought to 1.0 V. Being the active measurement time much lower than $T_R = 1$ ms, i.e., the targeted read-out time, it is possible to increase the read-out frequency to read fast changing of sensor data in a dynamic environment, at the cost of higher power consumption.

VI. MW-CNT Nanocomposite Capacitive Sensor

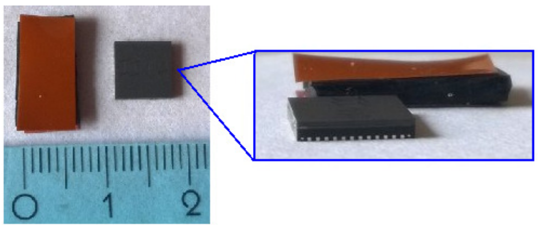


Fig. 13. Photograph of the capacitive sensor next to the QFN-48 chip, which includes the presented ROC.

The presented plastic material can be considered particularly suitable for robotic sensitive skin application, because of its scalability, modularity and flexibility, which permits to easily replicate the sensor module along the body, also covering curved surfaces, e.g., arms or legs. Owing to its features, the soft polymeric sensor improves the whole-body contact between the metallic armor and the sensors and, at the same time, guarantees a further cover against impacts for the electronic interfaces.

The piezoimpeditive transducer, shown in Fig. 13 is prepared by compounding Multi-Walled Carbon Nanotubes (MW-CNTs) with polydimethylsiloxane (PDMS). MW-CNTs (Nanocyl™ NC 7000 purchased from Nanocyl s.a.) were dispersed in a PDMS matrix (RTV-S691 A purchased from Wacker Chemie AG) in a ratio 1 : 90, using a planetary centrifugal mixer for 10 minutes at 2000 rpm. The curing agent (RTV-S691 B) is added in a ratio 9 : 1 (RTV-S691 A : RTV-S691 B) and the thermal curing is performed at 60 °C for 4h. The robotic skin is the outermost layer and the most exposed part to the external environment. The matrix and filler choice permits to achieve a robust and sensitive skin, without adding an extra shield, which could hinder the sensor sensitivity and response to external stimuli.

Since the curing temperature is quite low, the sensor can be prepared and cured directly on the PCB without causing any damage to the electronic components. As a consequence, the distance between the sensor and the ROC, i.e., the parasitic capacitance, is reduced and the quality of the measurement is, therefore, enhanced. The nanocomposite material is casted in a thin sheet (1 mm thickness) and then contacted for the electrical characterization using metalized Kapton® foils.

The obtained sensor has a piecewise linear capacitive response w.r.t. the applied load, as demonstrated in Sec. VII and its reference capacitance (at zero pressure) is proportional to the active area of the electrodes. Since the ROC sensitivity is maximized when $C_x(\mathrm{p}=0) = C_{\mathrm{ref}} = 1$ pF, we can tune the sensitivity along the robot body, by properly varying $C_x(\mathrm{p}=0)$. In the following tests, we obtained this feature by properly sizing the sensor. Once the transducer active area is optimized for a specific surface, the nominal capacitance can be tuned by adjusting the material composition or, when possible, the sensor thickness. Furthermore, by tuning the MW-CNTs density in the final polymer we can increase the relative capacitance response to applied pressure [32], [33]. For instance, when the number of MWNTs increases, the gaps among MWNTs becomes smaller, leading to greater electronic polarization of the dielectric layers, i.e., an overall larger capacitance [32]. So far, thicker samples are sensitive even to air blows, but further studies are required to reproduce this high sensitivity also in cured thin sheets.

VII. Measurements with ROC and nanocomposite sensor

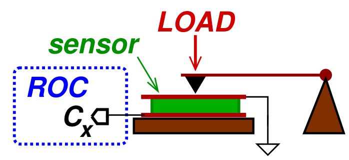


Fig. 14. Schematic of the equipment used to applied pressure to the sensor.

The pressure is applied on the sensor by using a tip mounted at the free end of a cantilever, as schematically presented in Fig. 14. Since the sensor outer layer is wired to ground, the coupling between the sensor and the surrounding conductive elements can be considered negligible. Fig. 15 shows the ROC output, averaged on 150 consecutive measurements (lasting 1 ms each and taken after the sensor is loaded), obtained by increasing and decreasing the applied load within 0–150 g. We chose this range to be comparable with the range used in [34] (0–200 g) for fingertip applications in humanoid robots. Since the pressure is applied punctually, we can assume that the sensor capacitance is modified just locally. Hence, the capacitance sensed by the ROC is an average value between the nominal capacitance $C_x(\mathrm{p}=0)$ (at the edges, where the pressure effects can be considered negligible) and a larger capacitance (in a small region around the tip where pressure is applied). If the same load had been applied uniformly on the whole sensor surface, C_x would have been globally modified (i.e., increased) at once, causing the output to vary more significantly w.r.t. the presented case, hence providing a higher sensitivity. In case of abrupt loading, we verified that the ROC output immediately reaches the maximum value "11111111" and returns to the calibrated value ("00000000"), once the load is removed.

The measurements are repeated on two sensors (A and B) of different size (30 mm^2 and 15 mm^2, respectively). The sensor A area is chosen to have a nominal sensor capacitance very close to the nominal value of the reference, i.e., $C_x(\mathrm{p}=0) = 1.2$ pF. Concerning sensor A, the sensitivity abruptly increases when the calibrated load varies from 50 to 80 g, hence, it is possible to divide the sensor characteristic curve in three regions, i.e., low-load (0 – 50 g), medium-load (50 – 80 g) and high-load (80 – 130 g). The plot in the left square of Fig. 15 demonstrates that the same abrupt increase was observed during the electrical characterization with the

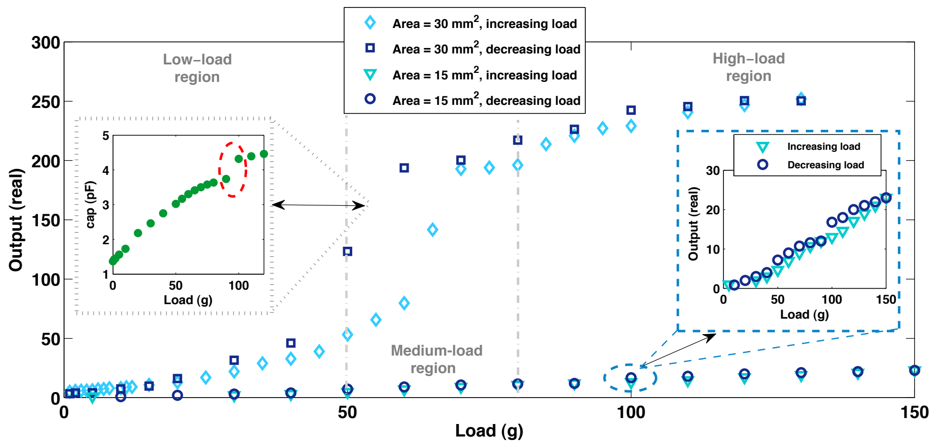


Fig. 15. ROC output using two MW-CNT Nanocomposite tactile sensors of different size. Each data correspond to the average value of 150 consecutive measurements. In the small plot on the left, the electrical characterization of the bigger sensor, using the impedance meter is shown. In the small plot on the right, a the y axis range is reduced to better appreciate the linear output trend using the smaller sensor.

impedance meter, hence we can consider it as an intrinsic property of the nanocomposite itself. The load at the edge between low and medium-load regions lies within 50 g and 100 g: this wide spread is due to the evident hysteric behavior of the material.

TABLE I

MESURED SENSITIVITY AND STANDARD DEVIATION IN LOW-LOAD, MEDIUM-LOAD AND HIGH-LOAD REGIONS FOR SENSORS A AND B.

Active area (mm^2)	Operating region	Sensitivity (LSB/g)	Standard Deviation$^{\triangle}$ (LSB)
30	Low-load	0.84	0.46
	Medium-load	6	3
	High-load	0.81	1
15	All	0.16	0.4

$^{\triangle}$ = Computed for each data-set of 150 consecutive measurements.

Since the piecewise characteristic is linear in each region, we extrapolated the measurement sensitivity, listed in Tab. I, by fitting each subdomain data with a linear regression curve and taking the slope. The sensitivity is 0.84 for low load, 6 for medium load and 0.81 LSB/g for high load regions. Fig. 15 shows that the medium load region presents the highest sensitivity, while in the low load and high load regions the sensitivity is almost the same ($\sim$ 0.8 LSB/g). The sensor B presents a lower sensitivity of 0.16 LSB/g. However, an analogous sensitivity increase is observed when the load is lowered (around 100 g), as highlighted in the plot on the right. Observe that lowering the sensor area, the difference between $C_x(\mathrm{p}=0)$ and C_{ref} increases, leading to a lower sensitivity. This demonstrates our initial assumption and also proves that the sensitivity can be tuned along the robotic body by properly co-designing C_{ref} and $C_x(\mathrm{p}=0)$.

Each data-set comprises 150 consecutive measurements and the standard deviation, used to estimate the measurement error, is listed in Tab. I. For sensor A, the maximum standard deviation is even lower than a LSB (0.46 LSB) in the low-load region, and it increases up to 3 LSB in the medium-load region, before decreasing back to 1 LSB in the high-load region. The maximum error in the measurements with the B sensor is 0.4 LSB, therefore negligible. Thanks to the measurements on the sensor A, the linear capacitance range can be extended to 4 pF, which is the maximum C_x at the edge between the low and medium region. This is still a limitation w.r.t. the ROC full potential, since the jump between low and medium-load region is due to the sensing material and not to the ROC itself.

The ENOB and the Integral Non-Linearity (INL) are computed to evaluate the ROC performance as a capacitance-to-digital converter. The first parameter is calculated using the formula in [24], i.e., $\mathrm{ENOB} = \left(20 \log\left(\frac{C_{\mathrm{range}}}{C_{\mathrm{resolution}}}\right) - 1.76\right)/6.02$, while the latter is the maximum deviation of the measurements w.r.t. the linear regression curve. Considering the measurements of Sec. V, INL is ± 0.7 LSB, while the ENOB can not be properly estimated because we covered just a small subinterval ($'0' - '13'$ in decimal system) of the whole linear output range, causing an underestimation of the achievable $\mathrm{C}_{\mathrm{range}}$.

When both ROC and transducer measurements are exploited, the overall performance can be also evaluated. Particularly, ENOB and INL must be separately calculated in all linear regions, to properly account for the piecewise behavior of the sensor. The ENOB is 5.3 and 7.1, while the INL is ± 2.1 LSB and ± 3 LSB in the low-load and high-sensitivity regions, respectively. The split of the overall $\mathrm{C}_{\mathrm{range}}$ in subdomains (due to the piecewise nature of the sensor) definitively causes a degradation of the ENOB, especially in the low-sensitivity regions.

VIII. DISCUSSION AND CONCLUSION

Tab. II presents a synthetic comparison between the ROC performance and the state-of-the-art pressure sensors read-out circuits for humanoid robots. Clearly, state-of-the-art commercial ROCs for tactile sensing can provide high performance. However, this work offers some major advantages for the considered application: tunable sensitivity, ultra-low power consumption and compact size, coupled with very low acquisition time (4 μs only).

The ROC can be successfully co-designed with the MW-CNT nanocomposite sensor to tune sensitivity along the

TABLE II

COMPARISON W.R.T. STATE-OF-THE-ART READ-OUTS FOR TACTILE SENSORS IN HUMANOID ROBOTS

	[16]	[1]	[13] ([14])	[2] ([3])	[15]	[19]	This work
Description	Digital Barometer	AD7147-programmable CDC ($\Sigma-\Delta$ ADC)	C8051F330 (113) Microcontroller	PIC32MX6(7)95F512H Microcontroller	ATmega328 Microcontroller	ADS1258 ADC	130 nm RFCMOS Full-custom IC
Supply Voltage (V)	3.3	2.6 – 3.6	2.7 – 3.6	2.3 – 3.6	1.8 – 5.5	2.7 – 5.25	1.0 – 1.2
Power Consumption (mW)	0.0165	2.97△	1.2♦	<1080⊕	<1000▼	42	0.0012 – 0.0018
Number of Channels	1	13	25	16	6 – 8	24	1
Bit Resolution	10	8	10	10	10	8 – 16	8
Single Channel Test Read-out Time (T_R, ms)	1.6	0.7–3.07	0.005	0.1	0.013 – 0.260	3	1
Active measurement Time (T_m, ms)	1.6	0.7–3.07	0.005	0.1	0.013 – 0.260	3	0.004
Duty cycle (%)	100	100	100	100	100	100	0.4
ENOB	NA	NA	9	9.5	NA	19.5–21.6	5.3–7.1
FoM (pJ/step)	NA	NA	11.7	$<1.49\ 10^5$	NA	39.6	8.8 – 46.7
INL	NA	NA	±0.5 LSB	-1<Typical<1 LSB	1 LSB	0.0003% FSR	±0.7 LSB□ (±2.1 LSB∞)

△ = 0.9 mA is the typical current in full-power mode. ♦ = Typical value at V_{DD} = 3.0 V at 200 ksps. ⊕ = 300 mA maximum current into V_{DD} pins. ▼ = 200 mA current into V_{DD} pins, with V_{DD} = 5.0 V. □ = Calculated from data in Fig. 10. ∞ = Calculated from data in Fig. 15.

TABLE III

COMPARISON W.R.T. THE STATE-OF-THE-ART CAPACITANCE PRESSURE SENSOR READ-OUT CIRCUITS

	[35]	[26]	[36]	[23]	[21]	[25]	This work
CMOS Process (L, μm)	0.18	0.18	1.5	0.18	0.04	0.16	0.13
Supply Voltage (V)	1.4	3.6-1.2-0.6	2.0-2.5	0.9-1.2	1	1	1.0 – 1 .2
Power Consumption (μW)	33.7	0.11	36♦	0.16	1.84	14	1.21 – 1.84
Active Area (A, mm^2)	0.456	0.105	4.84^A	0.49	0.0017⫛	0.05	0.017
Capacitance Range (pF)	0 – 24	5.3 – 30.7	N/A	2.5 – 75.3	$0.7 - 10^4$	0 – 8⊛	$1 - 10.5\ 10^3$
Linear Capacitance Range (C_{range}, pF)	0 – 24	5.3 – 30.7	N/A	2.5 – 75.3	$0.7 - 10^4$	1 – 8⊛	1 – 4▶
Capacitance Accuracy ($C_{sensitivity}$, fF)	0.16	8.7	0.075	6	12.3	0.255	5.23
Bit Resolution	15.4⋊	9.7⋊	10	13.3-14.2⋊	20	13.1⋊	8
Calibration⊡	N	N	Y	Y	Y	Y	Y
Temperature Range (°C)	N/A	N/A	N/A	N/A	-20 – 100	N/A	25 – 53
Active Measurement Time (μs)	230	6400	500^B	4000	19.06	6860	4
Read-out Time (T_R, μs)	230	6400	500^B	4000	19.06	6860	1000
ENOB	15.4	9.7	10.5	13.3–14.2	7.9	10.6 – 13.1	5.3–7.1
FoM (pJ/step)	0.175	0.85	4.14	0.064	0.141	1.87 – 10.6	8.8 – 46.7

♦ = C/V converter and cyclic ADC only. ⊕ = Including both the sensor and the integrated read-out circuit. ⫛ = Without accounting for internal capacitances. ^{A} = Including FSK transmitter and adaptive RF-DC converter.

⊛ = Reported in Fig. 27.7.6, but larger capacitances can be handled. ▶ = Measured linear range (i.e., constant sensitivity). ⋊ = Effective number of bit. ⊡ = Yes (Y) or No (N).

^{B}= ADC only. N/A = Not Available.

robotic body without re-designing the entire architecture, as detailed in Sec. III. This allows a significant reduction of costs, as human physiology can be replicated at robotic-level without designing dedicated IC solutions for those parts of the robotic body with different levels of sensitivity.

A general-purpose microcontroller can interface a whole sensor array at once, exploiting the multiple ADC channels, but it can not be aggressively replicated because of the large active area and high power-consumption. By contrast, the ROC presented in this paper is single-channel. This seems to be a limit for our specific application domain, however, the compact size and the ultra-low power consumption allows replication of the ROC modularly and interface of a sensor array. Furthermore, multiple ROCs can be daisy chained thanks to the jtag-like approach, taking advantage of the PISO register Master Output Slave Input (MOSI). This makes it possible to transmit the chained outputs on the same bus, minimizing the overall number of wires. When aggressive replication is required (e.g., interfacing a sensor matrix), proper solutions must be engineered to deal with cross-talk between either neighboring sensors or PCB stripelines of different C_x terminals. Cross-talk phenomena can be prevented by designing clever shielding systems, or exploited to feature superresolution [11]. An additional advantage of the ultra-low power consumption is the possibility to exploit innovative energy solutions, e.g., scavenging or fuel cells, as demonstrated in [37].

In this regard, the very low acquisition time (T_m) of only 4 μs becomes a critical feature, as it allows interfacing several sensors at the same time. In fact, within the 1 ms read-out time (i.e., human reaction time to touch), such a low T_m makes it possible to scan a whole array of 500 sensors by daisy chaining 500 ROCs and using a time division multiplexer. This triggers all ROCs and delays each `R` signal of 2 μs w.r.t. to the previous signal. In a QFN-48 the ROC can be replicated 38 times to provide 38 independent input channels, as long as some controlling blocks, e.g., a time division multiplexer and some registers, are added.

The low T_m also permits the increase of the read-out frequency up to 250 kHz at the cost of higher power consumption, in highly dynamic environments where fast changes of external data need to be sensed.

As reported in [18], biological mechanosensing circuits are characterized by low power consumption and minimal noise and thermal drift, partially afforded by frequency encoding of pressure information. Hence, the use of a ring-oscillator to translate the pressure into a frequency variation is considered

TABLE IV

EXPECTED AND ACHIEVED APPLICATION-LEVEL PERFORMANCE.

Feature	Specification	Result
RO Frequency range (MHz)	0.3–50	42.31$^{\triangle}$
Read-out rate (kHz)	$\geqslant$1	1–250
Active measurement time (μs)	<10	4
Power consumption (μW)	<10	1.21–1.84
Active Area (μm$\times\mu$m)	~I/O PAD (90 × 90)	221 × 79
Robustness: T Range (°C)	20–50^{H}	25–53
Robustness: V_{DD} Range (V)	1.0–1.2	1.0–1.2
Sensitivity (fF/LSB)	$\leq$10	5.23
Calibration	Yes	Yes
Tunability	Yes	Yes

$^{\triangle}$ = Simulated value. ^{H} = Ambient temperature operation but larger upper bound due to Joule heating of robot high-power actuators.

an optimal way to reproduce human behavior at robotic-level.

Tab. III presents the comparison of the ROC performance w.r.t. the state-of-the-art pressure sensor CDCs. State-of-the-art pressure sensor CDCs generally perform better ENOB and ADC Figure of Merit (FoM), i.e., $\mathrm{FoM} = \frac{\bar{P}T_m}{2^{\mathrm{ENOB}}}$. Conversely, the presented ROC is one of the most compact and has the lowest active measurement time. As already mentioned, this feature makes it ideal to be replicated along the robotic body and interface a sensor array, which can be scanned in 1 ms, complying to human response after touch.

Furthermore, the sensitivity can be varied along the robotic armor, by properly co-designing each sensor with the ROC. This is an advantage generally not featured by other CDCs. Differently from analog circuits, the ROC architecture can be implemented in a different technology with little effort and the target sensitivity can be recovered by properly trimming C_{ref} and modifying the RO design only.

Scalability and modularity are achieved at architecture-level by designing all blocks, including the analog blocks, with standard logic cells. Using digital methods for analog blocks makes it possible to overcome device mismatch and reduce bias and temperature dependence, with the aim of increasing reliability and reducing component variability during process-scaling [38]. This improved robustness, which is generally not featured by all-analog circuits, makes the system even more attractive to reproduce the human sense of touch [18].

Tab. IV lists expected and obtained application-level performance. All requirements were successfully fulfilled (e.g., compact size, tunability, sensitivity range, PVT robustness) and, in some cases (e.g., active measurement time and power consumption), experimental results even exceeded targeted expectations.

To sum up, the presented read-out circuit is an ideal candidate to reach large integration density for tactile skin applications, because it features: i) modularity, ii) scalability, iii) a small active area, iv) ultra-low power consumption, v) robustness, vi) capacitance offset compensation (calibration), vii) good sensitivity over the measured range, viii) tunable sensitivity. Hence, considering these factors, this ROC can be considered a better interface for tactile sensors w.r.t. a commercial ADC. Furthermore, the implemented jtag-like approach drastically reduces the number of wires and cables needed inside the robot, making this solution even more effective [7]. These advantages make it possible to exploit the presented ROC in a wider range of applications based on capacitive sensing (e.g., proximity sensing, humidity sensing, liquid-level detection) that are not restricted to tactile applications.

In future implementations, the ROC will be modularly replicated on the silicon chip, which will be bonded on a flexible surface covering the robotic armor. Size limitation will become an even stricter constraint, mostly dictated by the technology used to implement the design and the chip package.

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