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Development of Reference Tools for Medium Voltage Measurements in Smart Grids

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Declaration

I hereby declare that, the contents and organization of this dissertation constitute my own original work and does not compromise in any way the rights of third parties, including those relating to the security of personal data.

Mohamamd Modarres

2017

* This dissertation is presented in partial fulfillment of the requirements for **Ph.D. degree** in the Graduate School of Politecnico di Torino (ScuDo).

I would like to dedicate this humble thesis to

my beloved wife and best friend, **Mohanna**

my loving parents **Bahaoddin** *and* **Azar**

and my siblings **Amin** *and* **Mahsa**

this humble work is sign of my love to you

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Abstract

The aim of this project is the design and the realization of a 30 kV reference voltage divider (VD) for smart grid monitoring, which will be mainly used in laboratories to characterize and calibrate the voltage transducers. The scale factor ratio error introduced by a normal voltage transducer (VT), according to technical report IEC/TR 61869-103 must be limited to a maximum of 1% up to 2^{nd} harmonics and to a maximum of 5% up to the 50^{th} harmonics. The maximum acceptable phase error should be no more than 18 mrad up to the 2^{nd} harmonics and 90 mrad up to the 50^{th} harmonics. Of course, the target for a reference voltage transducer should be much more accurate than the requirement of the standards for a normal VT.

A reference voltage transducer is expected to show high accuracy also at higher frequencies, since this feature is needed in smart grids, due to the considerable amount of harmonics after the 50^{th} harmonics even up to 10 kHz, although this peculiarity is not required by the standards for transducers in normal electrical networks. Then, in the bandwidth up to 10 kHz, the maximum target deviation from the rated scale factor for the reference VD has been selected equal to 0.05 % and the maximum phase error equal to 9 mrad.

To reach such a high accuracy, there is a need for a design tool, which can model and simulate the divider with a very good accuracy. Then, this tool could be used for the design procedure of the structure and of the definition of the geometrical parameters of the reference VD, in order to realize an extremely accurate measurement device satisfying the demanding constraints mentioned above.

To begin with, two methods, the Finite Element Method (FEM) and the Boundary Element Method (BEM), were examined in calculating the stray capacitance between two (physically infinite) planes. The comparison of BEM and FEM results with the analytical ones shows a better accuracy and a lower CPU simulation time in FEM rather than in BEM approach. Thus, the physical model of the reference VD has been simulated by FEM.

The output of the FEM software is a matrix defining the stray capacitance network between different nodes (equipotential surfaces) of a voltage divider. This matrix is used as an input of a MATLAB program, which solves the electrical circuit of the VD. Furthermore, a small voltage divider was realized to prove the capability of this modeling

approach. The measurement results of the test VD shows a good agreement with the results obtained from the theoretical method.

An innovative approach was presented in the modeling of resistors, which have been divided into two parts, instead of being modeled as a single component. The important role of the resistor body modeling in calculating the stray capacitances in the VD has been highlighted. The validation procedure was repeated for a real 20 kV VD that was already available. The comparison between measurement and theoretical results confirms the validity and high accuracy of the proposed modelling approach. The research carried out up to here has been published in "IEEE Transaction on power delivery".

The realization of the numerical tool has allowed the design of the reference 30 kV VD. The first issue was to find the best configuration for the VD. It is not clear in literature what kind of configuration could be the best or what should be considered in the design and realization course. Such a lack of guidelines is the main reason that impeded the application of an optimization method in this project. In fact, the optimization process could be used for a device, which has a known and fixed configuration with a limited number of geometrical and electrical variables that can be selected in order to find the best value for the best objective function.

The design realized in this project aimed also at configuring shape and structure of the divider for future optimization process. In other words, some different VD configurations and effect of different parameters variation have been deeply investigated.

At the start of assessment, different kind of stray capacitances and their effect on the frequency behavior of a VD have been discussed. This subject has been investigated by introducing the equivalent circuit of a simple VD. Then the effect of modifying different kind of stray capacitances on the VD frequency behavior has been shown. Besides, the best condition for the stray capacitances that can lead to a good frequency behavior has been discussed.

The initial VD design procedure was done in order to mainly understand the effect of geometrical parameters like the distances between the HV resistors and between HV and LV sections. The goal was to lower (and also balance) the stray capacitances. Then, a grounded plate has been introduced and discussed in the resistive VD with horizontally placed resistors, in the attempt of reducing and better balancing the stray capacitances. The effect of the presence and also the size of the plate has been discussed and the effect of the distances between the resistors were also studied (Section 3.3).

At this stage, new circuital components have been introduced in the divider. The compensation of the low voltage (LV) side with an extra LV capacitor (CBT) is explained (this subject is explained in detail in section 3.3.7). As the next step, a Reference Voltage

Divider (RVD) considering the voltage requirements (30kV) and high voltage (HV) resistors (with rated voltage of 10 kV) has been designed. The first design has been dedicated to the simplest configuration with vertically placed HV resistors. Then the geometrical parameters (distances) has been changed and the effect was studied. At the end of this part, a VD configuration with vertically placed HV resistors has been modelled and simulated. The simulation has been carried out with an accurate model including all the details of the components available for the VD realization like, for instance, insulation supports, resistors and pillars. Design simulations show very good results that comply the uncertainty limitations of a reference VD. However, there was a drawback in that first design configuration. Its size was quite large compared to the similar measurement devices in this voltage range. Despite this fact, the finalized RVD was realized and its frequency behavior was measured using two digitizers at the low voltage side. Although the measurement results were following the frequency behavior of the simulation results, a significant discrepancy between the measured and simulated frequency responses has been found.

Section 3.6.1 show the analysis of the discrepancies between the model and measurements. The reason was due to the ground below the VD that was disregarded in the simulations. The agreement between computed and measured response of the VD with vertically placed resistors significantly improves when the ground is correctly modeled. However, the ground presence worsens the frequency behavior of the VD, which becomes undesirable for a RVD, even if acceptable with respect to the requirement of the standards for a normal voltage transducer. The analysis of the VD with vertically placed HV resistors has been published in the journal of “International review on electrical engineering”.

In a next step, the general behavior of the 30 kV VD with horizontally placed HV resistors has been investigated since this configuration results to be more compact and should be less sensitive to proximity objects. In the previous configuration (the vertical one), the distances between high voltage nodes were large enough that small changes in the resistor placement or in the shield dimensions do not modify significantly the electric field. However, in this new configuration (the horizontal one), the electric field must be calculated by FEM for any modification of the parameters. Two different way of connections between HV resistors were modeled (section 3.7) with long and short connections. The comparison between the two configurations shows that the VD with shorter copper tube connection have a better behavior and so has been further investigated in the following.

The RVD with horizontally placed resistors could give a good frequency behavior. However, the maximum electrical field strength could not be further lowered due to the

nature of this configuration (section 3.7). In order to get an improved frequency behavior a zig-zag configuration has been introduced a topological variation of the horizontal configuration. The zig-zag VD lowers the maximum electrical field strength compared to the horizontal resistor VD (section 3.8). More than 50 cases of zig-zag VD with different parameters were simulated to reach the goal of the project design. A main part of the focus was on the shielding of the RVD in a way to control and manipulate the stray capacitances in order to make the VD error compliant with the design specification. The main drawback of this zig-zag RVD is the sensitivity towards the proximity effect.

In section 3.8.8, a shielding with three different screen parts has been proposed. Such a shield could give a good frequency behavior with small proximity sensitivity. However, the model with three screens could not be realized at the moment as it requires special workshop tools, not available at the moment.

A different approach has been achieved providing a reduction of the proximity effect (section 3.10). The zig-zag RVD has been fitted with an LV shield. The measurement results show an accuracy of ±980 ppm for the scale factor, up to 50 kHz, and less than 9 mrad for the phase error up to 32 kHz (2.1 mrad up to 10 kHz). This zig-zag RVD could be used in any laboratory environment after calibration for the specified perimeter.

To further reduce the proximity sensitivity, HV capacitors have been added to the zig-zag RVD, which significantly reduces the effect of the stray parameters and the VD is much less affected by the proximity changes (stray capacitance changes). The result of zig-zag RCVD with LV connected shield shows a promising frequency behavior which could be considered as a reference voltage transducer.

By connecting the LV shield to the ground one can obtain a further reduction of the proximity effect (section 3.10.3). The zig-zag reference RCVD with ground connected shield shows a maximum 244 ppm of scale factor uncertainty and less than 345 μrad of the phase error uncertainty from DC up to 10 kHz.

The proximity effect investigation done in Sect 3.10.3 has highlighted that this divider (with ground-connected shield) exhibits very small proximity sensitivity. For example, if a grounded (or floating) object having size similar to the one of the divider approaches the VD up to 30 cm, the scale factor changes less than 91 ppm and the phase error is modified about 82 μrad.

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Chapter 1

Introduction

1.1 General Introduction; reasons for using a voltage divider

There is a need for smarter electrical grid applying new technologies and tools to work more efficiently, more reliably with affordable maintenance, with ability to accommodate more renewable energy sources, to reduce consumer carbon footprint and so forth [1].

To achieve this target a huge number of smaller renewable sources of electricity (e.g. solar-voltaic panels, wave power and wind turbines – both domestic and commercial) are generating supply, and feeding into the grid. Renewable sources are by their nature intermittent, they are geographically diverse, and thus they behave quite differently from large power plants [2]. The incorporation of many decentralized electricity sources into the grid can cause deterioration of the power quality, and degradation of the grid supply [2]. The interactions between the many sources and the multiple loads, which draw power from the grid, are highly complex and take place over an intricate network of distribution links. Then more measurements related to power quality and network stability are substantially needed to ensure the quality and reliability of the electricity supply, because the current metrological infrastructure cannot ensure reliable traceable measurements required by a complex grid [2]. A further challenge is the monitoring of the smart grid to ensure that the revenue metering of such a complex two way supply can be accurately monitored and fairly billed. Then there is a potential for [2]:

- insecurity of the electricity supply because it is hard to monitor;

- unfair trade between parties trading electrical energy to and from the grid. In order to achieve Grid Stability the grid must first be accurately and reliably monitored, indeed actual measurements in the grid are a key issue for Smart Grid R&D [2].

Also, common medium voltage (MV) power systems are nowadays experiencing an increase in connected nonlinear loads and time-varying distributed generation energy sources equipped with switching converters, with a consequent degradation of the quality of the distributed electrical power [3].

Moreover, the liberalization of the energy market in many countries has increased the importance of the accurate estimation of energy flows in the grid and the monitoring of the power quality parameters. Eventually, it could be said that there is a high need for development of new transducers able to match good metrological performances, with reduced dimensions and cost [4].

In other words, besides the common requirements in terms of accuracy and high electric insulation between input and output, a wide bandwidth is also required to properly evaluate the current and voltage signal spectra [5].

As far as MV network measurements are concerned, two main solutions could be available for voltage measurement: voltage dividers (VD) and magnetic core voltage transformers [6].

It is hard or almost impossible to achieve a high bandwidth by employing transducers based on traditional HV electromagnetic transformers [5].

The reason is that with increasing frequency, voltage drops in the series elements of the equivalent circuit and the effect of the stray capacitances (capacitive coupling in the turns of the windings and between the two windings) increase [6].

This problem is particularly evident in instrument transformers for medium and high voltage systems, where the insulation requirements are stronger and impose the use of larger sizes, thus determining larger stray capacitances and leakage inductances to appear [6].

In general, VTs frequency and transient responses becomes unacceptable at around 1 kHz (or even at lower frequencies), well below the frequency limit established in the relevant standards [7]. Also at higher voltages, resonance or ferroresonance phenomena can be encountered at lower frequencies, since inductances and capacitances values can vary with insulation and manufacturing requirements [7].

As a consequence, especially in medium and high voltage systems, VTs could not be suitable to measure voltages with significant high frequency components [6].

Furthermore, all transformers have an intrinsically nonlinear behavior, owing to the presence of the magnetic core. Only below the knee of the magnetizing curve transformers work almost linearly. But, when the primary voltage becomes very high, as it happens for dysfunctions like faults or lightning, the device works in the saturation

region and the errors increase dramatically. This makes such devices definitely not suitable to provide accurate measurements in the presence of these events [6].

It should be noted that according to the technical report IEC/TR 61869-103 [7] or the standard IEC 60044-8 [8], only 50% of the VTs could perform accurately up to 700 Hz if the accuracy requirements for the phase are considered [7].

Consequently, the focus of this project is on MV voltage dividers (VD) for high voltage attenuation in a wide bandwidth. There are diverse kind of VDs, whose differences are based on the elements used in them such as; inductive VDs (IVD), resistive VDs (RVD), capacitive VDs(CVD), or combined elements VDs like; resistive-capacitive VDs(RCVD). VDs could be also categorized according to the type of operating voltage as DC VDs or AC VDs.

In the next section an introduction of a general VD will be given. Then a general view concerning the state of the art on VDs up to now will be introduced in the next part.

1.2 Setting up and Operation of a voltage divider

A Voltage divider is generally used to reduce the voltage up to a value that can be read by electronic devices such as oscilloscope. It usually consists of series elements. A simple circuit representing a general VD is shown in Fig. 1.1. Output voltage can be obtained as follows:

$$\bar{V}out = \frac{\bar{Z}_{\mathrm{LV}}}{\bar{Z}_{\mathrm{HV}} + \bar{Z}_{\mathrm{LV}}} . \bar{V}_{in} \tag{1.1}$$

Each of Z_{HV} and Z_{LV} could be consisting a series (or/and parallel) of different resistors, and/or inductors, and/or capacitors.

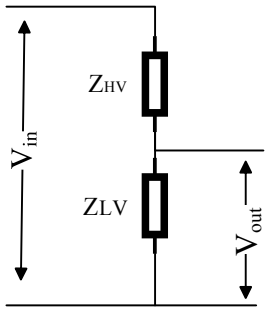


Fig. 1.1. Simple circuit representation of a VD

The two important parameters that describe the performance of a voltage transducer (which includes VDs) are the scale factor "K" and the phase error "$\Delta\varphi$", which can be calculated by using the following equations:

$$K = \frac{\left|\bar{V}_{in}\right|}{\left|\bar{V}_{out}\right|} = \frac{\left|\bar{Z}_{HV} + \bar{Z}_{LV}\right|}{\left|\bar{Z}_{LV}\right|} \qquad (1.2)$$

$$\Delta\varphi = \varphi_{out} - \varphi_{in}$$

V_{out} and φ_{out} are the magnitude and phase of the secondary voltage, while V_{in} and φ_{in} identify the primary voltage phasor [4]. Note: as can be seen from the equation (1.2), the scale factor and phase error act reversely, as the scale factor is the ratio of the input to output while the phase error is calculated by decreasing the input phase angle from the output phase angle. Then, if the scale factor increases (due to any reason), the phase error goes towards a negative value. This issue will be discussed in detail in section 3.2.

Clearly, in an ideal situation the phase error of a voltage transducer should be zero; in addition, both scale factor and phase error should be independent of the frequency. In reality, the scale factor and phase error will change depending on frequencies. The reason is the presence of stray parameters such as internal stray parameters of the elements and/or the external stray parameters introduced by the structure of the divider. Then definitely, presence of sub harmonics, DC components, as well as harmonics increase the negative effect of stray parameters. Eventually, the scale factor and phase error will deviate from the rated values by frequency variation. That is exactly the same reason that measurement voltage transformers does not work well in MV smart grids or networks with distributed generation (DG) and they need a new reference tool (such as a precise VD with high frequency bandwidth) to be calibrated and/or need to be substituted by newly designed voltage transducer.

The next sub-section is devoted to different works on VDs presented up to now.

1.3 State of the art on VDs

There are many papers in literature studying IVDs [9-12]. Normally, IVDs are not suitable for the MV networks, because the core magnetic properties limits the IVDs bandwidth. That is why high-accuracy inductive voltage dividers (IVD) are widely applied in many precision AC parameter meters below 1 kHz. Moreover, some researches indicated that the non-linear characteristic of IVDs might induce harmonic distortion [13]. Also

structures of IVDs are complicated [9, 13]. The IVDs, which are used for more than 1 k Hz, have a nominal voltage far smaller that of required by MV network and usually an small scale factor [12]. IVDs are ideal for applications where the voltage is up to 1000 V [11].

There are also CVDs which could be used in high voltage even more than the one required in MV network. CVDs usually have high frequency bandwidth since, at the higher frequencies up to some hundreds of kHz, the capacitive reactance will be so small and the effect of stray parameters will be negligible. Then the CVDs act like as pure capacitive VD, which are not affected by stray parameters. For example [14] shows the result of a 400 kV CVD working at 60 Hz with a quite good accuracy. Reference [15] studies a 150 kV CVD with max 3% error at 50 Hz. Papers [16, 17] developed a coaxial CVD for high voltage pulses. As well as IVD, CVDs are not suitable for MV smart grids or networks with distributed generations, although they could work at high voltages with a satisfying frequency bandwidth. The main problem is due to the DC voltage component injected into the MV grid or power network consisting of DGs [18]. Another problem is linked to an extra electric charge that may be arise in continuously operating CVDs, engendering errors in a short period of time. The last but not least disadvantage of CVDs compared to RVDs is related to cost because of using high voltage capacitors that are far more expensive than resistors.

There are also some literature studies on RC-VDs [6]. Authors of [19] added different capacitors in parallel to resistors to improve the result of an RVD, but with a higher cost due to adding the mentioned capacitors. Authors in [20] designed 3 kV VD for measurement of the impulse voltages up to 10kV, in which they used stray capacitors as the high voltage arm capacitor of the VD. In this way, the cost problem of CVDs is solved. However, the simulation results of impulse response are not presented, which makes the comparison between the simulation and experiment impossible. In other words, it is not feasible to check out the accuracy of the presented model. It is also not practicable to use the same procedure for the modeling of the VDs using the commercial available resistors as the paper uses virgate high resistance in Glass enamel film (not common commercially for medium and high voltages). In addition, the stray parameters in HV and LV parts are not calculated and are achieved by a procedure similar to the “try and error” approach.

The reference [6] gives a comparison between the result of a measurement voltage transformer and that of an RC-VD up to 2.5 kHz. The result the RC-VD is far more accurate than the measurement voltage transformer.

A 20 kV RC-VD coupled with an analog optical transmission system (for development of a galvanic insolation between the VD and the measurement/protection device) is realized and studied in [21-23]. To control the capacitive coupling due to surrounding

components and to shield from the electromagnetic interferences caused by the nearby conductors or external sources, a two section cylindrical shield was introduced. The scale factor and phase error uncertainty were 4% and about -120 mrad at 10 kHz for the input voltage of 500 V. This uncertainty meets the requirements for an on-site measurement but not for a reference transducer.

The reference [24] proposes a compensation method using a digital filter for the improvement of the frequency behavior of measurement transducers. The results show that the developed technique allows a compensation of the RC-VD behavior from 10 Hz to 100 kHz, reducing its frequency response errors of a factor enclosed between one and three orders of magnitude, depending on the frequency value.

One of the most commonly used VDs is RVD because it is simple in structure and easy in use when compared to others [25]. There are many literatures studying RVDs. For example, a highly accurate 100 kV DC RVD is developed in [26]. To prevent leakage and compensating currents, the measuring divider is arranged on a supporting structure consisting of Teflon (PTFE) rods with a specific resistance higher than 10^{18} Ω cm. Besides, an extra RC-VD (working as a shield VD) is setup parallel to the main RVD in five sections of 20 kV. This ensures a linear voltage distribution in each section of the main RVD, thus protecting the main RVD resistors from transient voltage overload while switching on or off. Also the effect of the SF6 (the insulating gas that electrically isolate the resistors) pressure and the resistor warm-up behavior are investigated.

Reference [27] studied the design of a 500 V AC RVD. The focus was on the optimization of the shape of the shell (shield) covering the RVD.

According to [28] there are differences from 20% to 30% in unit step response (USR) of a same class RVD at eight different laboratories in Japan due to conductivity and/or permittivity of laboratory floors. Then the focus of the [28] was on studying the effect of conductivity and permittivity of floors on USR of the RVD and acquiring the best height for a shield ring to decrease the effect of the environment on the results. Then, this introduces acceptable reproducible measurements at different laboratories.

The research [29] presented an RVD design for wideband power measurements in electric drive applications. A simulation framework that considers the parasitic elements of the resistors and the layout is shown.

In [30], the authors improved the result of an RVD by using a coaxial cable guard circuit combined with an extra CVD which acts like an active shielding, reducing the value of stray capacitors from each resistors towards the ground. In this way, they could obtain low phase error for frequency up to 1.5 kHz and for the voltage up to 1 kV.

An RVD using two other extra VDs for shielding and guarding of the main RVD in order to acquire a high accuracy VD up to 1 kHz is developed in [31]. At the end, the result is compared with that of an already calibrated IVD.

The RVD developed in [32] gives a high accurate response for frequencies up to 100 kHz, but only works for voltages up to 240 V. A bras pipe guard driven by a second resistor chain is used to reduce the value of stray capacitances between resistors and the ground.

The authors in [33] constructed a reference RVD compensated with an output capacitor for characterization of MV voltage transformers. It uses 20 SMD resistors and operates up to 2 kV. The scale factor and phase error uncertainty at 20 kHz are ±0.07% and ±25 min (7.2 mrad), respectively.

Paper [34] presented a design for an RVD module for HVDC measurements up to 200 kV. Authors placed a wideband shielding CVD around the reference RVD to enhance the wideband frequency response of the latter. The estimated overall uncertainty of the 200 kV RVD is about 13 μV/V. Following the previous reference, authors presented a 1000 kV HVDC reference RVD, using 5 series modules of the mentioned 200 kV RVD [35-37]. The relatively high capacitance of the shield divider chain (due to the second divider with capacitors connected to the main divider) yield the field distribution along the reference 1000 kV RVD linear. The on-site calibration showed an uncertainty lower than 50 μV/V at 1000 kV DC.

In [25], authors analyzed some error sources such as leakage current, normal mode rejection ratio of the voltmeter, temperature coefficient, and their effects which might be commonly encountered in using the RVDs.

Among different types of VDs, RVD shows interesting features, as it behaves better than IVD's in terms of frequency bandwidth, especially for frequencies more than 1 kHz, and it has a far cheaper cost than CVDs and RC-VDs.

In chapter 2, a detailed modeling approach will be introduced. A small RVD will be realized to investigate the accuracy of a proposed FEM based modeling approach. Then the model will be also applied for modeling a 20 kV RVD and to investigate more deeply the accuracy of the model.

In chapter 3, a high accurate reference RVD will be designed using the proposed modeling approach. Finally in chapter 4 the reference RVD will be realized and the measurement results will be presented.

In chapter 5 the final conclusions and recommendations for future studies will be given.

Chapter 2

Numerical Tool, modeling and verification

2.1 Introduction

The purpose of this chapter is to develop an accurate model able to envisage the VD behavior. Then the proposed model will be used to design a reference MV VD.

There are many studies investigating the modeling of the divider. However, it is not so common to fully model the details of the VD such as leads of resistors, the effect of the resistor body, or the supports and insulation bars [28, 30, 32, 38]. The main goal is calculating and modeling the stray parameters as they determined the major deviation from the rated phase error and scale factor.

In [39] an HV resistive divider made of five 200 kV modules is surrounded by a capacitive path, which acts as a shield. A 3D Finite Element (FEM) modeling approach is utilized to determine the optimal capacitive grading that minimizes the response time of the system. Capacitors are modeled but nothing is said about the resistor modeling. In other cases, arrangements for the reduction of stray capacitance effects are proposed following experimental verifications [40].

In [41], a mega volt RVD for high-impulse measurement with two toroids as shield is studied. Firstly, various kind of stray capacitances are represented. The stray capacitance distribution is represented by parallel capacitances between the nodes along the HV arm, capacitances between nodes and the ground, capacitances between shielding electrode and the ground. Next, an electro-static RVD equivalent circuit consisting of different stray capacitances is developed. Then after applying 1 V voltage to the HV terminal, the

voltages of each node and the shield are calculated by a 2D electro-static model of the RVD considering the conductor parts and the shields. Then the different stray capacitances were calculated by the applying equations similar to the Kirchhoff's current law at every node. However, the effect of the resistors bodies were not considered.

Reference [19] introduced a hybrid FEM-analytical approach and a corresponding equivalent circuit for analyzing the impulse voltage response of the RVD. Authors did not consider, however, the effect of resistor body and made approximations for the supporting bars.

In the [20], the capacitances in the HV arm are estimated starting from the tuned LV capacitance and the 2-D FEM simulation is done to choose the better shield minimizing the effect of stray capacitances [4]. Only shields and supporting insulator are modelled in 2D FEM model, which could not be so precise.

Paper [13] introduces an equivalent similar to the one in [41], but without a precise way to calculate the stray capacitances except an estimation value for the capacitive coupling between resistors and between conductor parts and the ground.

2.2 The model and numerical tool

The numerical tool is constituted by two modules. In the first one, the stray capacitances due to capacitive couplings between different parts of the divider should be computed. The result of such a module will be inserted as an input to the second module, which solves the equivalent electrical circuit of the VD.

Both FEM and Boundary Element Method (BEM) could be used to extract the stray capacitances as two most common numerical techniques. To investigate the accuracy of the two numerical methods, a comparative analysis of those two approaches will be carried out. Then the most accurate one will be chosen to pursue with.

The finite element approach here considered is a standard 3D approach for an electrostatic field problem, where the unknown is the electric scalar potential ϕ defined as $\mathbf{E} = -\nabla\phi$. The divergence of the electric flux density D is linked to the p.u volume charge density ρ through the well-known Poisson equation. The governing law of the electrostatic field is

$$-\nabla \cdot (\varepsilon \cdot \nabla \phi) = \rho \tag{2.1}$$

where ε is the dielectric permittivity. This study takes advantage of the implementation of eqn. (2.1) through the commercial well known and validated FEM code Opera 3D, by Cobham. Conversely, the non-commercial BEM code Sally 3D, developed by INRIM and Politecnico di Torino, is considered.

The BEM approach originates from the scalar form of the Green theorem applied to a volume *V* having boundary Ω, which is

$$\int_{V}(\psi\cdot\nabla^2\phi - \phi\cdot\nabla^2\psi)\,\mathrm{dv} = \int_{\Omega}(\psi\frac{\partial\phi}{\partial n}-\phi\frac{\partial\psi}{\partial n})\cdot\,\mathrm{ds} \tag{2.2}$$

where ψ is the Green scalar function defined as $\psi(\mathrm{P},\mathrm{P}') = \frac{1}{4\pi r}$, being *r* the distance between the computational point P and the source point P'.

It is easy to verify that the Laplacian of the Green function is null so that the following equation can be obtained:

$$\zeta\ \phi(\mathrm{P}) = \int_{\Omega'}\left(\psi\ \nabla\phi\cdot\mathbf{n} - \phi\ \nabla\psi\cdot\mathbf{n}\right)\mathrm{ds} + \int_{V}\frac{\rho}{\varepsilon}\ \psi\ \mathrm{dv} \tag{2.3}$$

where the coefficient ζ is equal to 0.5 on the boundary Ω and is 1 inside the volume *V*. Eqn. (2.3) gives the potential in the computational point by introducing the continuity conditions between the media (a) and (b), these last divided by surface Ω,

$$\begin{aligned}\phi^{(\mathrm{a})} &= \phi^{(\mathrm{b})};\\ \varepsilon^{(a)}\left\{\nabla\phi^{(a)}\cdot\mathbf{n}^{(a)}\right\} &= -\varepsilon^{(b)}\left\{\nabla\phi^{(b)}\cdot\mathbf{n}^{(b)}\right\}\end{aligned} \tag{2.4}$$

For each *i-th* discretization element four unknowns are identified, $\phi_i^{(a)}$, $\phi_i^{(b)}$, ($\nabla\phi_i^{(a)}\cdot\mathbf{n}_i^{(a)}$) and ($\nabla\phi_i^{(b)}\cdot\mathbf{n}_i^{(b)}$), which reduce to two by applying eqn. (2.4). More details can be found in [42].

2.2.1 Stray capacitance matrix calculation

The computation of the stray capacitance network can be carried out starting from the electrode potentials or from the electrode voltages (by choosing one of the *n*+1 electrodes/conductors as a reference). In the first case, a potential and a charge is assigned to each conductor/electrode to form the so called "generalized capacitance matrix" (2.5) which describes the system behavior:

$$\begin{bmatrix} q_1 \\ \vdots \\ q_{n+1} \end{bmatrix} = \begin{pmatrix} C_{11} & C_{12}\cdots & C_{1,n+1} \\ \vdots & \ddots & \vdots \\ C_{n+1,1} & C_{n+1,2}\cdots & C_{n+1,n+1} \end{pmatrix} \cdot \begin{bmatrix} \phi_1 \\ \vdots \\ \phi_{n+1} \end{bmatrix} \tag{2.5}$$

where C_{ij} represents the generalized capacitance, ϕ_i and q_i are the potential and the charge of the *i-th* electrode respectively. In the FEM computation, the zero potential can be assigned to the far boundary elements, using Dirichlet boundary conditions. In the case of BEM, the boundary condition is implicit. In both cases, the computation of the generalized capacitances is done by rows. Assigning a unitary potential to the *i-th* electrode and zero to the other ones, the capacitance C_{ij} is computed through the integral

$$q_j = C_{ij} = \int_{\Omega j} \mathbf{D}\cdot\mathbf{n}\cdot ds \qquad \begin{cases} \text{being: } \phi_i=1 \text{ and } \phi_j\big|_{j\neq i}=0; \\ \quad i=1, 2 \ldots, n+1 \\ \textit{and } \phi_{boun}=0 \text{ at the boundary} \end{cases} \tag{2.6}$$

where Ω_j is the surface of the electrode j.

The transformation between the generalized capacitance matrix (based on potentials) and the circuital matrix (based on the voltages) can be done, without loss of generality, by the choice of one conductor/electrode as a reference electrode with zero potential. By choosing the n+1 conductor as a reference the terms of the circuital matrix can be computed as

$$C_{ij} = C_{ij} - \frac{\left(\sum_{k=1}^{n+1} C_{ik}\right)\cdot\left(\sum_{m=1}^{n+1} C_{mj}\right)}{\sum C} \tag{2.7}$$

where the denominator of the previous equation gives the summation of all values in the generalized capacitance matrix (*C'*) and the circuital matrix is

$$\begin{bmatrix} q_1 \\ \vdots \\ q_n \end{bmatrix} = \begin{pmatrix} C_{11} & C_{12}\cdots & C_{1,n} \\ \vdots & \ddots & \vdots \\ C_{n,1} & C_{n,2}\cdots & C_{n,n} \end{pmatrix} \cdot \begin{bmatrix} V_1 \\ \vdots \\ V_n \end{bmatrix} \tag{2.8}$$

and

$$V_j = \phi_j - \phi_{n+1} \tag{2.9}$$

The circuital matrix is the one which is needed to build and solve the circuital network. According to [43] the matrix (2.8) can be directly computed as follows. When $i = j$ (2.10) will be applied, while (2.11) will be considered when $i \neq j$.

$$q_i = \sum_{j=1}^{n} C_{ij} = \int_{\Omega_j} \mathbf{D} \cdot \mathbf{n} \cdot ds$$
$$\begin{cases} \text{being: } V_i = 1 \text{ and } V_j\big|_{j \neq i} = 0; \ i = 1, 2 \ldots, n \\ \quad \textit{and } V_{boun} \text{ floating at the boundary} \end{cases} \tag{2.10}$$

$$q_j = -C_{ij} = \int_{\Omega_j} \mathbf{D} \cdot \mathbf{n} \cdot ds$$
$$\begin{cases} \text{being: } V_i = 1 \text{ and } V_j\big|_{j \neq i} = 0; \quad i = 1, 2 \ldots, n \\ \quad \textit{and } V_{boun} \text{ floating at the boundary} \end{cases} \tag{2.11}$$

In both cases the condition at the boundary is equivalent to floating potential. The result is presented in (13), which is consistent with eqn. (9).

$$\begin{bmatrix} q_1 \\ \vdots \\ q_n \end{bmatrix} = \begin{pmatrix} \sum_{j=1}^{n} C_{1j} & -C_{12} \cdots & -C_{1,n} \\ \vdots & \ddots & \vdots \\ -C_{n,1} & -C_{n,2} \cdots & \sum_{j=1}^{n} C_{nj} \end{pmatrix} \cdot \begin{bmatrix} V_1 \\ \vdots \\ V_n \end{bmatrix} \tag{2.12}$$

2.2.2 Investigation of using FEM and BEM

To compare the computational accuracy of the two methods (FEM and BEM), a simple case having an analytical solution has been chosen. It consists of two parallel plates as shown in Fig. 2.1, where the analytical solution is available. In this case, the ratio of the plate surface S to the distance d is set to 1600 cm, so that the circuital capacitance of the system is close to the analytical value $C = \varepsilon \cdot S/d$, where ε is the air permittivity.

As evidenced by the results in Table 2.1, the BEM approach uses a number of mesh elements that is nearly two orders of magnitude lower than the volume elements in FEM, for the same mesh density of the surfaces. However, it must be noted that the algebraic matrix associated with the BEM is full (~$2 \cdot 10^8$ non-zero elements), while the FEM stiffness matrix is sparse (~$3 \cdot 10^7$ non-zero elements), so that the computational burden is comparable., The BEM result shows a greater discrepancy with respect to the analytical solution, in comparison with the one of the FEM approach. To this reason, the FEM approach is implemented in the tool.

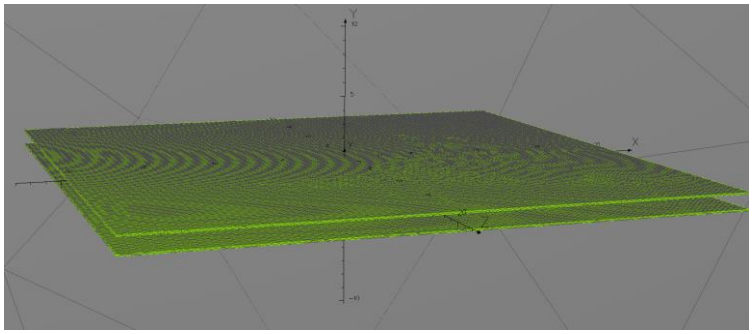


Fig. 2.1. 3D FEM model of the parallel plate capacitor. Only the mesh of the plates and the far boundary surface are visible. The plates are 1 cm far from each other and each side is 40 cm

Table 2.1. Comparison between FEM and BEM for two parallel plates

	3D FEM Circuital matrix	3D FEM General matrix	3D BEM
Discretization elements	965798	965798	14808
General cap. term $C_{11}=C_{22}$ (pF)	-	150.4	175.8
General cap. term $C_{12}= C_{21}$ (pF)	-	143.8	167.2
Circuital capacitance (pF)	147.0	147.1 using (2.7)	171.5 using (2.7)

The result of the circuital capacitance from the analytical formula is 141.7 pF.

2.2.3 Electrical network solution of VD

The second module of the numerical tool aims at solving the circuital network that simulates the voltage divider. The high voltage arm is subdivided into elementary cells series connected. Each cell represents a high voltage element. It is constituted by two nodes and two or three branches, depending on its resistive or resistive-capacitive nature. For each high voltage element the stray parameters can be introduced (internal stray capacitances of the resistors, internal stray inductance and internal equivalent series resistance of the capacitors). The low voltage arm is simply represented by an equivalent parallel RC bipole. The electrical circuit that has to be solved is made of passive bipoles and a voltage source [23]. Because of the presence of an ideal voltage source, which cannot be substituted by a Norton equivalent bipole, the modified nodal approach [44] is implemented. It is written in the frequency domain using Matlab™. The modified nodal approach requires the substitution of the pure voltage source with ideal current source of

unknown amplitude and the consequent addition of an equation imposing the voltage between the two nodes. A projection matrix is introduced to extrapolate the unknown currents from the array, which contains all the branch currents (known and unknown). The algebraic system, for a graph with N_n nodes and N_b branches has the following form:

$$\begin{bmatrix} [\mathbf{AYA}^t] & [-\mathbf{AT}^t] \\ [-\mathbf{TA}] & [0] \end{bmatrix} \cdot \begin{Bmatrix} [V_u] \\ [I_u] \end{Bmatrix} = \begin{Bmatrix} \mathbf{A}I_k \\ V_k \end{Bmatrix} \tag{2.13}$$

where $\mathbf{A}[N_n, N_b]$ is the incident matrix describing the network topology, $\mathbf{Y}[N_b, N_b]$ is a diagonal matrix containing the branch admittances, and $\mathbf{T}[N_b, 1]$ is the projection matrix. V_u and I_u are the unknown nodal potential and current source arrays respectively, while I_k and V_k are the known terms. In this specific case, the network does not include known current sources, thus the term $[\mathbf{A}I_k]$ is a zero array and the arrays V_k and I_u are, actually, scalar quantities. The first quantity is the applied voltage and the second one is the unknown current source, which replaces the supply source.

The incident matrix is built in three steps. In the first one the incident sub-matrix which describes the circuital topology of a elementary high voltage cell is replied on the diagonal of the matrix **A** as many times as the number of high voltage cells. Then M columns are added, where M is the number of stray capacitive couplings among divider electrodes (number of upper triangular part of capacitance matrix defined in (2.8). Finally, two branches simulating the RC low voltage equivalent bipole are introduced by adding the last two columns to **A**. This approach allows the automatic building of the incident matrix associated with a divider of arbitrary structure.

2.3 Verification of the numerical tool using a small test voltage divider

To validate the computational tool a test RVD has been set up. The analysis focuses on the frequency response of the device. To predict such a response, the equivalent network of the VD, containing stray capacitance and circuital components, is solved, as described in the previous section. The frequency response of the VD equivalent circuit is compared with the voltage scale factor K and the phase error $\Delta\varphi$ measurements carried out on the test device.

2.3.1 Characteristics of the test VD and modeling approaches

A sketch of the low voltage test VD is shown in Fig. 2.2. It consists of six resistors and seven conductors (electrodes), the latter of which connected to ground. The high voltage arm is constituted by four non-inductive 10 MΩ, 10 kV resistors, while the low voltage arm has two 2 kΩ resistors, with a consequent rated scale factor of 10001. Two plastic transparent and parallel insulation plates, acting as a support for resistors and electrodes, are shown in Fig. 2.2(i). Two metallic plates are placed at the top and bottom of the VD.

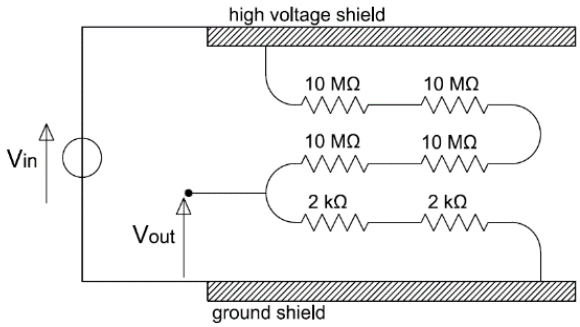


Fig. 2.2. Sketch of the test divider

To investigate the effect of including resistors in the calculation of parasitic parameters, three configurations have been considered:

case #a - stray parameters computed considering only electrodes (Fig. 2.3(ii));

case #b - stray parameters computed including the resistors (Fig. 2.3(iii)). Each electrode and each resistor are considered as separate elements in the FEM computation of stray parameters, while in the circuit representation the resistor is split into two parts;

case #c - stray parameters computed including the resistors, each of them divided into two parts Fig. 2.3(iv)), where each part of the resistor contributes to the calculation of the parasitic capacitances of the contiguous electrode. The part including each electrode and a half resistor is assumed as one element of the FEM stray parameter computation, while in the circuit representation the resistor is considered as a whole.

In case #a and #c the circuital network has seven nodes, which correspond to the seven electrode potentials. The circuital network is built around these nodes. In case #b, the capacitance network is more complex, since the resistors are equivalent to six additional nodes. In this case the value of each resistor is divided by two in the electric circuit solving

program and each parasitic capacitance due to resistors is considered connected in the middle as shown in Fig. 2.4.

To complete the investigation a further case has been considered being

- **case #d** – as the case #c, but including the dielectric plates as shown in Fig. 2.3(i).

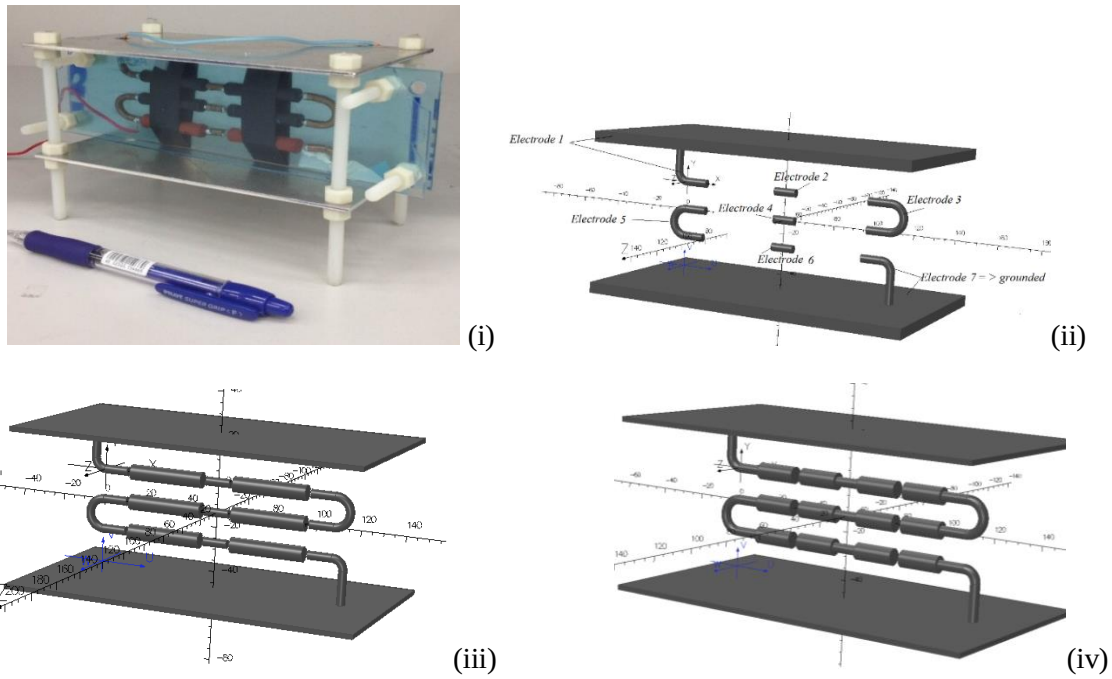


Fig. 2.3. (i) Picture of the test divider. Geometric model of the test divider: (ii) only electrodes (case #a), (iii) electrodes with entire resistor bodies (case #b), and (iv) electrodes with split resistor bodies (case #c).

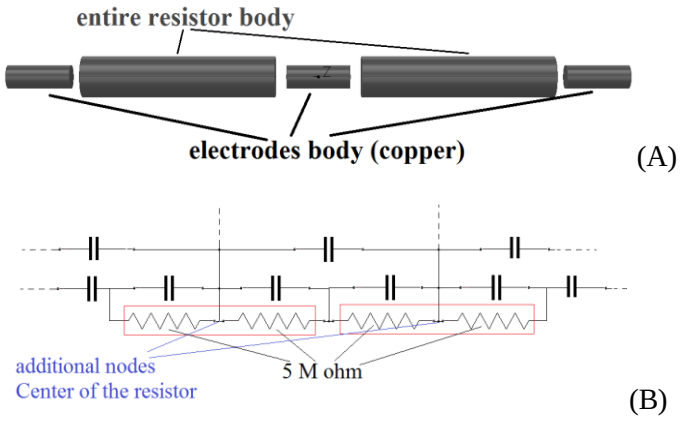


Fig. 2.4. Simulation of the case #b - (A) some resistors and electrodes in FEM model (B) part of the equivalent electric circuit with stray capacitances

2.3.2 Experimental characterization of the VD

The frequency behavior of the scale factor and phase error are obtained by measuring the output signal of the device under test and the applied voltage. The signals are digitized by two Agilent 3458 multimeters (AMM), configured for DCV digitizing and synchronized by an external trigger (FLUKE397) (Fig. 2.5). DCV digitizing mode (of Agilent 3458) implements voltage measurements with a short integration time and a short interval between samples with respect to the frequency of the signal being digitized. Thanks to the different selectable ranges, signals whose amplitude differs up to five orders of magnitude can be acquired. To evaluate the sinusoidal parameters (amplitude a, phase φ and offset component c) of each signal [21] a four-parameter nonlinear fit algorithm is used, whose function is

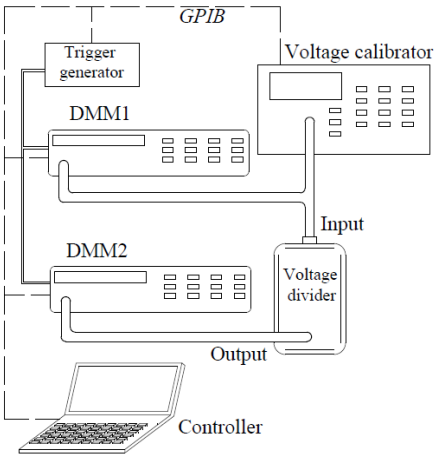
$$f(t) = a \cdot \sin(2\pi f \cdot t + \varphi) + c \tag{2.14}$$

The frequency characterization is carried out supplying the divider with a stable 50 V voltage by means of a calibrator. The supply and measurement chain is remotely controlled. A Python program manages the supply and the acquisition systems and sets frequency sweep for the measurement of the divider scale factor and phase error. Because of the low pass filter of the different cut-off frequency introduced by digitizers, a correction factor on the measured phase error has to be applied.

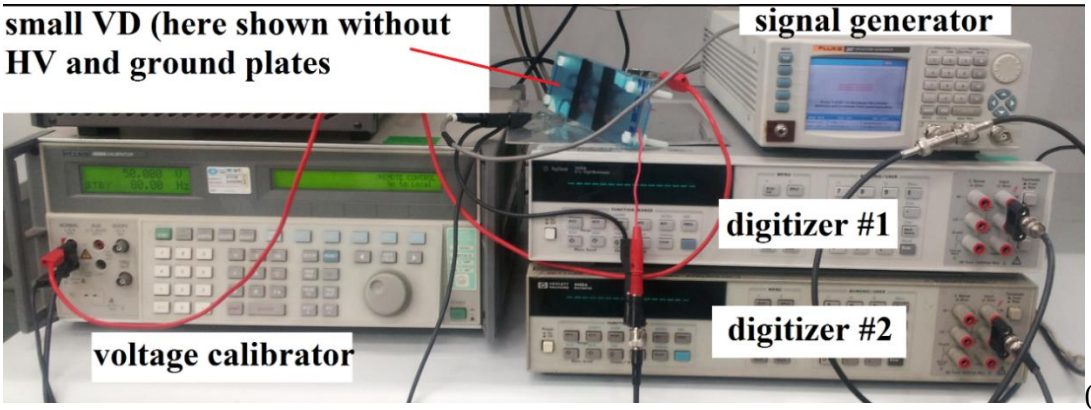
Each digitizer acts as a first order low pass filter. Also the cut-off frequency of each voltage range is different. Then the phase difference between input and output of a single digitizer in the frequency f (caused by internal properties of digitizer) can be calculated as follows:

$$\varphi_2 - \varphi_1 = \arctan(f / f_0) \tag{2.15}$$

where φ_1 and φ_2 are the phase angle of the input and output signal of a digitizer, respectively. f_0 is the cutoff frequency of the digitizer.



(a)



(b)

Fig. 2.5. Experimental setup for the measurement of the resistive VD frequency response; (a) the scheme (b) the real set-up

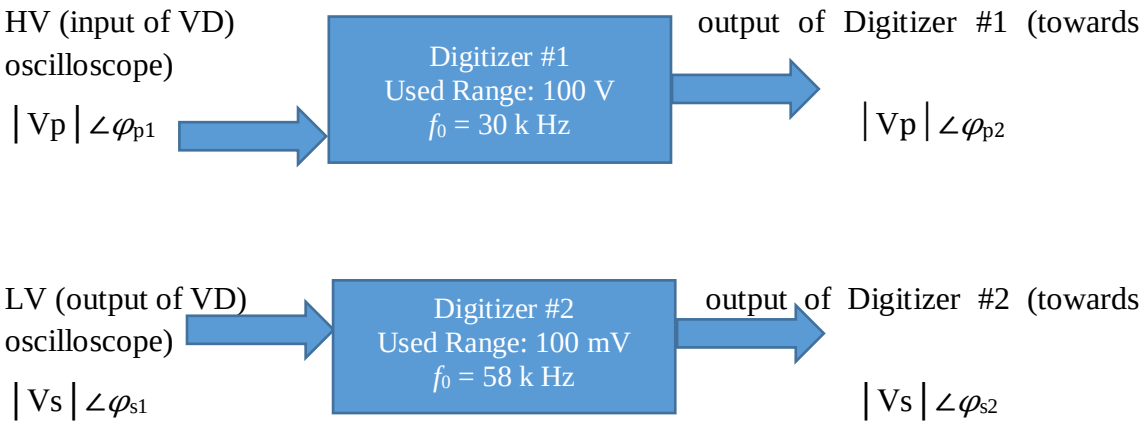


Fig. 2.6. Scheme for calculating phase error correction factor caused by digitizer

By a first order model of the two filters, a correction factor should be deduced and applied to the measured divider phase error. The measured cut-off frequency for the first digitizer employed in the range of 100 V (for the VD input) is about 30 k Hz, and for the second digitizer employed in the range of 100 mV (for the VD output) is about 58 kHz [45]. The phase difference between outputs of digitizers (introduced only by the internal characteristics of digitizers) in an arbitrary frequency *f* is:

VD Phase error correction factor (for frequency *f*) = (2.16)

$(\varphi_{s2} - \varphi_{s1}) - (\varphi_{p2} - \varphi_{p1}) = \arctan(f/30000) - \arctan(f/58000)$

where φ_{p1} and φ_{p2} are the phase angle of the input and output signal of digitizer #1, and where φ_{s1} and φ_{s2} are the phase angle of the input and output signal of digitizer #2, respectively. The Fig. 2.6 is depicted to make the equation (2.16) more clear.

The comparison between the proposed models is shown in Fig. 2.7, which puts in evidence a quite good agreement between measurements and computed results in the case #d up to 10 kHz. The deviations versus frequency of computed results from the measured values are shown in Table 2.2, where

$$\varepsilon_K \% = \frac{K_{meas} - K_{comp}}{K_{meas}} \cdot 100 \tag{2.17}$$

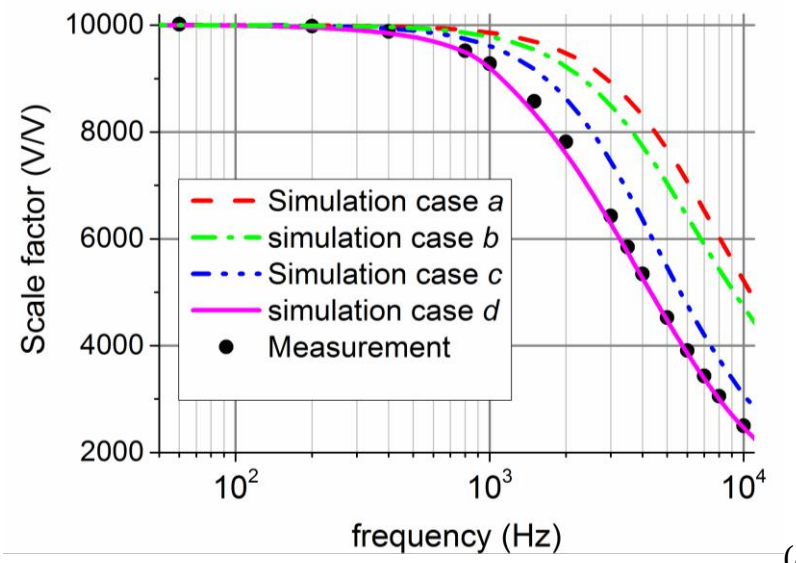
and

$$\varepsilon_{\Delta\varphi} = \Delta\varphi_{meas} - \Delta\varphi_{comp} \tag{2.18}$$

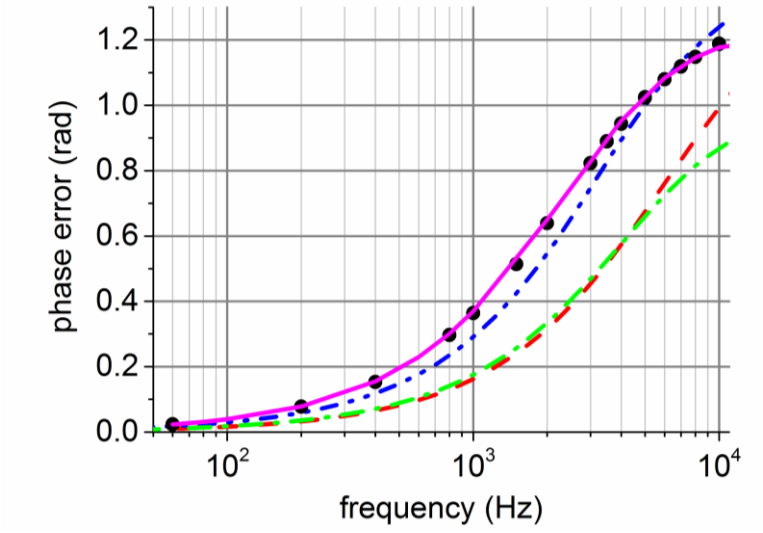
being K_{meas} and K_{comp} the measured and computed scale factors respectively, while $\Delta\varphi_{meas}$ and $\Delta\varphi_{comp}$ are the measured and the computed phase errors.

It is worth to underline, how ε_k% is lower than 0.2% up to 1 kHz, reaching 4 % at 10 kHz. Disregarding the stray capacitance due to the dielectric boards (case #c) worsen the results, as clearly shown by the dashed-dot-dot curves in Fig. 2.7 and by the Table 2.2 data. The relative deviation of computed scale factor from the measured values rises up to 4 % at 1 kHz and ~21% at 10 kHz. When the resistors are not properly modelled, as in case #b, where they are considered as an entire body, or in the cases #a, where they are not considered at all, the limits in the computation of the stray capacitances considerably

affects the computed frequency response of the VD. In these cases, the computed results differ from the measured ones several percent at 1 kHz and 151% at 10 kHz.



(a)



(b)

Fig. 2.7. Results of the test VD. (a) Scale factor and (b) phase error of measured and computed results in different conditions.

Table 2.2. Small VD validation measurement: deviations of computed values from the measured ones for the scale factor and phase error.

	Case #a		Case #b		Case #c		Case #d	
f [kHz]	ε_K %	$\varepsilon_{\Delta\varphi}$ (mrad)	ε_K %	$\varepsilon_{\Delta\varphi}$ (mrad)	ε_K %	$\varepsilon_{\Delta\varphi}$ (mrad)	$\varepsilon_{\Delta\varphi}$ (mrad)	ε_K %
0.06	-0.2	-18	-0.2	-12	-0.2	-6	-0.2	+ 1
0.4	1	-114	0.8	-79	0.5	-34	-0.1	-2
0.8	5	-217	4	-150	2	-62	-0.1	-4
1	8	-264	6	-181	4	-73	-0.2	-6
2	29	-430	18	-291	10	-92	-0.8	-10
5	107	-410	54	-338	20	-25	-2	+ 5
10	151	-115	85.5	-288	21	-55	-4	-10

The validation tests confirm the capabilities of the tool to reproduce the VD behavior, highlighting the need for a detailed inclusion of dielectrics and all circuital components in the FEM model, to get accurate results in the range of frequencies where the stray couplings become significant.

2.4 Validation of the numerical tool on an actual 20 kV VD

The validated modelling procedure is then applied to the 20 kV/2 V resin insulated RVD shown in Fig. 2.8(a), developed for 50 Hz measurements and protection.

The resistors are arranged in a circular configuration; their layout is shown in Fig. 2.8(b). The geometry of the VD created in the FEM pre-processor, as shown in Fig. 2.8(b), includes halved modelled resistor bodies and takes into account the insulation material properties.

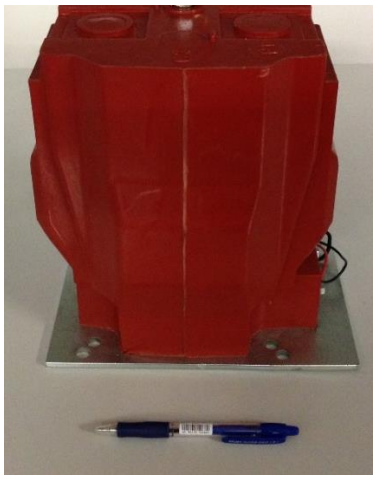
The output of FEM gives a 17×17 capacitance matrix, as there are 17 electrodes excluding the divider bottom plate, which is grounded. The capacitance matrix is the input for the Matlab™ program that solves the electric circuit including the resistors. Concerning simulations, two cases are considered. In the first one the resistor bodies are modelled in the FEM computation (complete simulation) while they are disregarded in the second one. The measured and computed scale factor and phase error behaviours of the VD, presented in Fig. 2.9, show that the complete simulation provides, as expected, the most accurate results. In addition, two measurement conditions (both presented in fig.2.9) have been considered:

• case #1 - cable grounding the bottom plate placed near to the VD's body (shown in Fig. 2.10 (a));

• case #2 - cable grounding the bottom plate placed on the ground (shown in Fig. 2.10 (b));

In the case #1 the ground cable passes close to the VD body, whose stray capacitances towards ground are modified due to potential introduced by the ground cable. In the case #2 that cable is "shielded" by the ground plate and its effect is negligible. This result proves a need for proximity investigation in design of VD.

In conclusion, a good agreement between measured and computed results can be found also for the 20 kV VD provided that a complete model of the device is used. This analysis confirms that the simulation accuracy strongly decreases when the resistor bodies are not included in the FEM simulation. In the complete simulation the maximum relative discrepancies between measured and computed values, in the frequency range up to 10 kHz, are limited to 5.7% for the scale factor and to 24 mrad for the phase error (Table 2.3).


(a)

(b)

Fig. 2.8 . Structure of the 20 kV VD (a) sealed with insulation (b) the FEM model (here shown without insulation and ground plate)

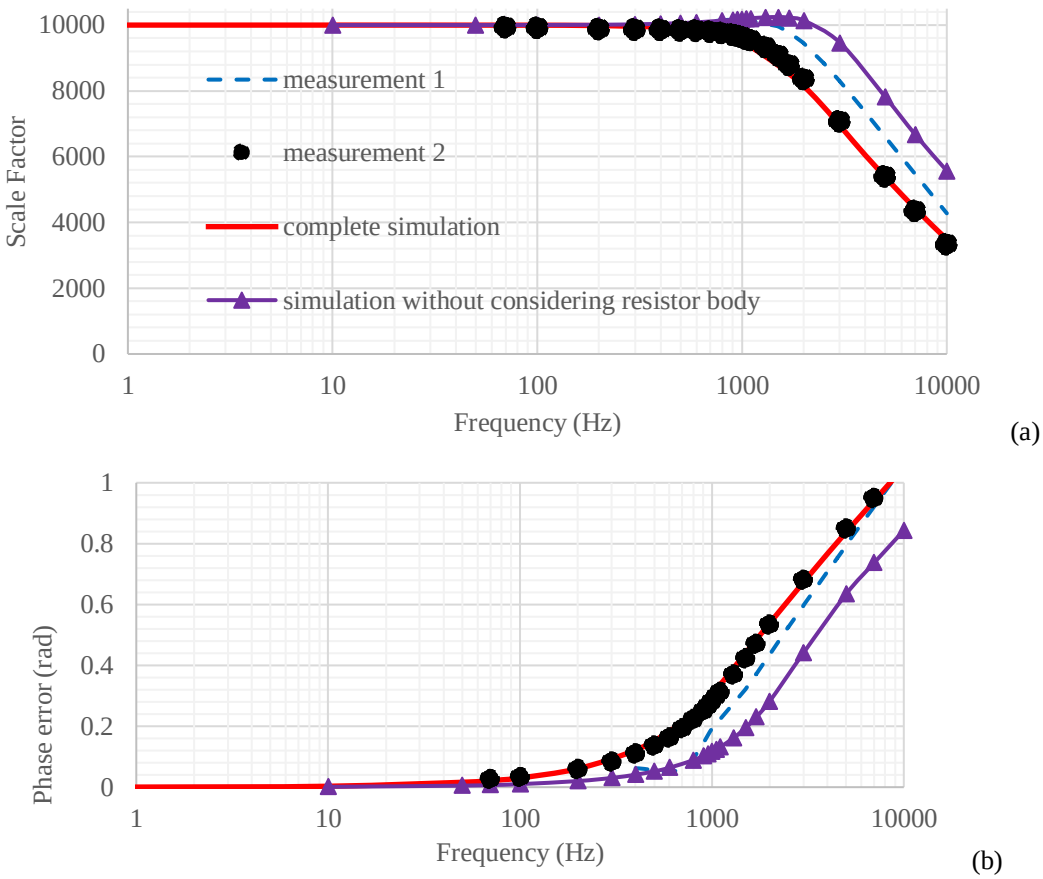


Fig. 2.9. Results of the 20 kV VD a) Scale factor and b) phase error of measured and computed results. The curves with triangle markers on the line are obtained without considering the resistor bodies in the computation of the stray capacitances.

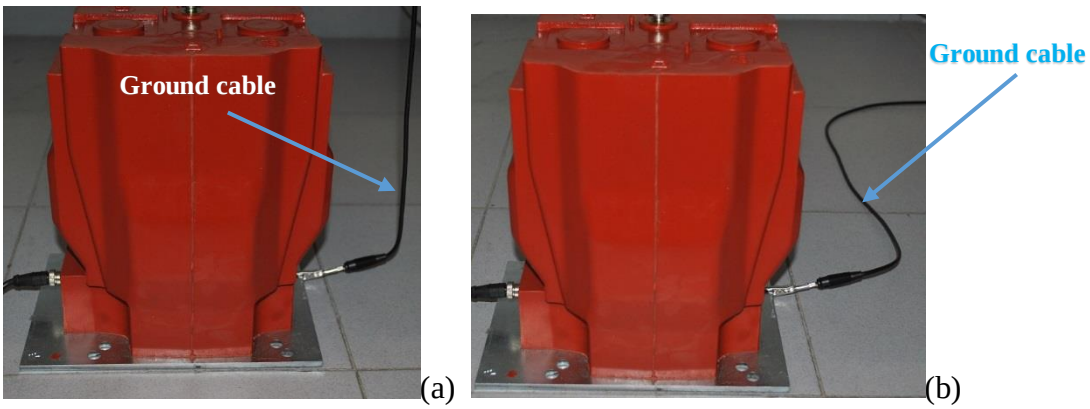


Fig. 2.10. The placement of the ground cable in the 20 kV VD (a) ground cable laid on the ground (b) ground cable placed close to VD's body

Table 2.3. Discrepancies between measured and computed values of the scale factor and phase error of the 20 kV VD

	Complete simulation	
f [Hz]	ε_K %	$\varepsilon_{\Delta\varphi}$ *(mrad)*
70	-0.8	3
400	-0.9	-14
800	0.6	-24
1000	1.3	-24
2000	2.5	-7
5000	0.1	10
7000	-2.2	8
10000	-5.7	4

Chapter3

Design and realization of the reference VD

3.1 Design of a new reference voltage divider

A new reference 30kV VD should be designed and realized through the reliable numerical tool able to accurately model a VD (30 kV input, less than 10V as output, with high accuracy that is about two order of magnitude better than the requirement of standard voltage transducers). The object of this chapter is the study of the influence of different parameters on the VD frequency response. Finally, the best configuration according to the performed investigation will be chosen for realization that will be described in the next chapter.

The goal of implementing the small test divider was not obtaining a good frequency response but the verification of the numerical tool accuracy. Then, a numerical tool reliable and able to accurately predict the behavior of the divider allows the simulation of different geometries and designs. Besides, the sensitivity of voltage divider versus different parameters could be analyzed. Then the best configuration will be chosen to be realized.

3.2 Different kind of stray capacitances

Before starting the study, it is useful for a better understanding and analysis to mention various kinds of stray capacitances in a resistive voltage divider. There are three different stray electric field couplings that give rise to stray capacitances in an RVD:

1- Stray capacitances between the HV elements and also between HV elements and LV elements (here named CHV)

2- Stray capacitances between HV elements and the ground (here named CG)

3- Stray capacitances between the LV elements and also between LV elements and the ground (here named CLV)

These three kinds of stray capacitances (CHV, CG, and CLV) will be taken into account in the sensitivity analysis aiming at finding a good VD configuration with respect to its frequency response.

Neglecting stray capacitances in an RVD, the scale factor $(Z_{HV}+Z_{LV})/Z_{LV}$ is simply calculated as the ratio of the resistances as (see Fig. 1.1):

$$SF = \left|1 + \frac{R_{HV}}{R_{LV}}\right| \tag{3-1}$$

This SF is constant versus frequency and the phase error is zero. Then if a CHV is added in parallel to a pure RVD, Z_{HV} will decrease by increasing the frequency. Then enhancing the CHV in the RVD circuit shifts down the scale factor. It actually acts like a pole of the VD scale factor shown in the following equation:

$$SF = \frac{\left|\overrightarrow{V_{in}}\right|}{\left|\overrightarrow{V_{out}}\right|} = \left|1 + \frac{R_{HV}}{R_{LV}(\mathrm{j}\omega \mathrm{R}_{HV} C_{HV} + 1)}\right| \tag{3-2}$$

In addition, CHV increases the phase error of the VD towards a more negative value as it reversely acts compared to the scale factor.

Similarly, if a CG or a CLV are added to a pure RVD, the output voltage will decrease with increasing the frequency. Therefore, the scale factor will be shifted up compared to the pure RVD's one. It actually acts like a zero of VD scale factor as shown in the following equation

$$SF = \frac{\left|\overrightarrow{V_{in}}\right|}{\left|\overrightarrow{V_{out}}\right|} = \left|1 + \frac{R_{HV}(\mathrm{j}\omega \mathrm{R}_{LV} C_{LV} + 1)}{R_{LV}}\right| \tag{3-3}$$

The phase error of the VD will also increases towards a positive value.

Table 3.1 summarizes the effects of different kind of stray capacitances on the scale factor and phase error.

Table 3.1. Effect of various kind of stray capacitances on frequency behavior

Type of stray capacitances	Scale factor in higher frequencies :	phase error in higher frequencies :
If CHV : increases	decreases	Increases towards a positive value
If CG : increases	increases	Increases towards a negative value
If CLV : increases	increases	Increases towards a negative value

A simple VD electrical circuit is represented in Fig. 3.1 as an example for explanation of the relation between CHV and CG. The values of R1, R2, and C_{HV} are 2 MΩ, 1 kΩ, and 2 pF, respectively. (As Table 3.1 summarizes) if the CHV (in Fig. 3.1) is too smaller than the CG, there will be a major drop in SF. In addition, if the CHV is greater than the CG, there will be a lift in SF. Then as explained, the design of a new VD with a nearly flat scale factor (and low phase error) means to find the right configuration with right ratio between different kind of stray capacitances. This issue is practically shown by using the simple VD electrical circuit of Fig. 3.1. The frequency behavior of the sample circuit is shown in the Fig. 3.2 for different C_G values assuming a fixed value of C_{HV} (2 pF). As can be seen, even a low value of C_G value in the considered circuit does not give the best results and it should be somehow in balance (approximately equal in case of the schematic representation of the RVD equivalent circuit shown in Fig. 3.1) with the value of C_{HV}.

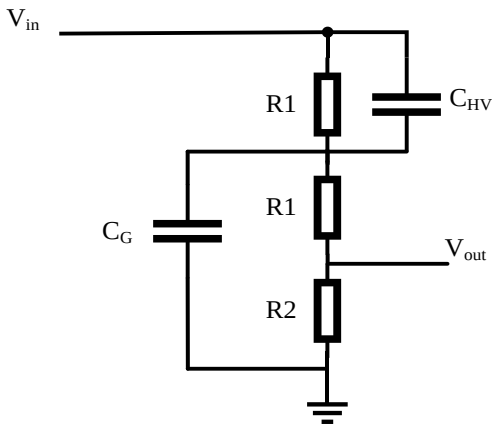


Fig. 3.1. Scheme of an RVD circuit

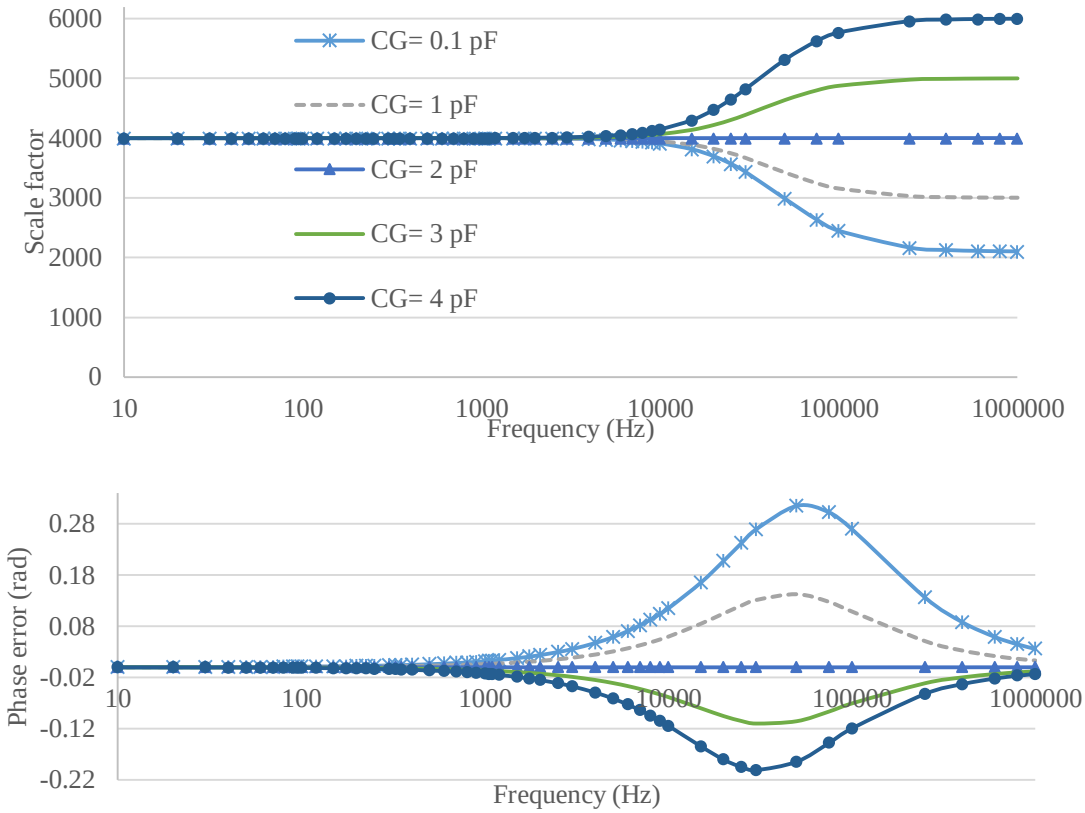


Fig. 3.2. Frequency behavior of the sample VD (shown in Fig. 3.1)

3.3 Initial design of the reference VD

As the final target is the realization of a reference voltage divider, the simulations will be done according to the correct geometry and size of the standard available resistors. Detail of parameters and their values for the initial design is in Table 3.2.

Table 3.2. Parameter values of the initial design (case 1)

Description of the parameter	Initial value
conductor thickness connecting the last resistor of HV part to the first LV resistor (Cu_lv_rad)	2 mm
grounded plate size	200 mm × 100 mm
LV layer distance from the grounded plate (cu_h_lv)	4 mm
the distance between the grounded plates and the first HV layer (dis1)	50mm
the distance between 1st and 2nd HV layer (dis2)	40 mm
the distance between the 2nd HV layer and the Top HV plate (dis3)	50 mm

The initial geometry shown in Fig. 3.3 is consisting of four 1 MΩ resistors in HV part (upper section of the VD) and two 2 kΩ resistors in LV part (below part of the VD). Both HV and LV resistors are cylinders with 37.5mm length, and 3.75mm radius. The top plate is connected to the HV and the lower plate is connected to the Ground. Each row in HV or LV part including the resistors and conductive elements will be called HV layer or LV layer for the sake of easiness to be referred. In the initial design, there are two HV layers and one LV layer shown in Fig. 3.3. It must be noted that the conductor connecting the last resistor of HV part to the first LV resistor is going through a grounded plate but insulated with respect to the ground plate.

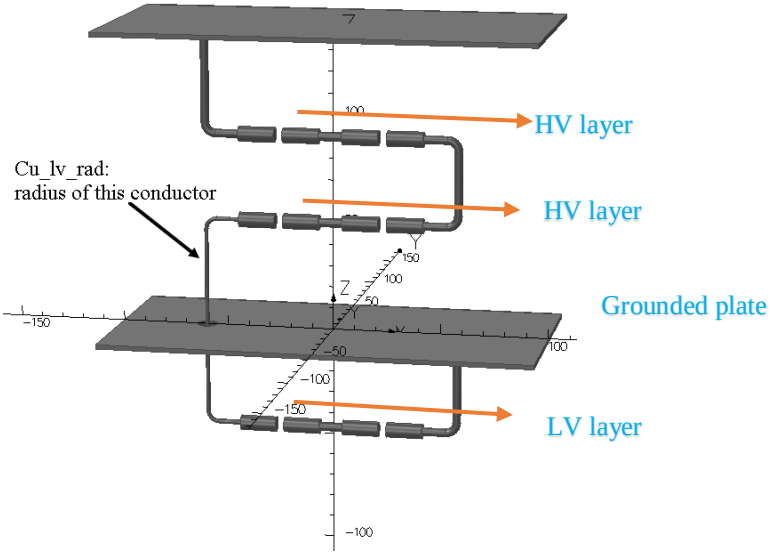


Fig. 3.3. Initial geometry of the voltage divider

The influence of the conductor thickness connecting the last resistor of HV part to the first LV resistor on the frequency behavior of the scale factor and of the phase error is demonstrated in Fig. 3.4. The result obtained with the small test VD are also presented for comparison as an index to compare the results easier. The aforementioned conductor radius can be 1 mm (called case 1) and 2 mm (called case 2).

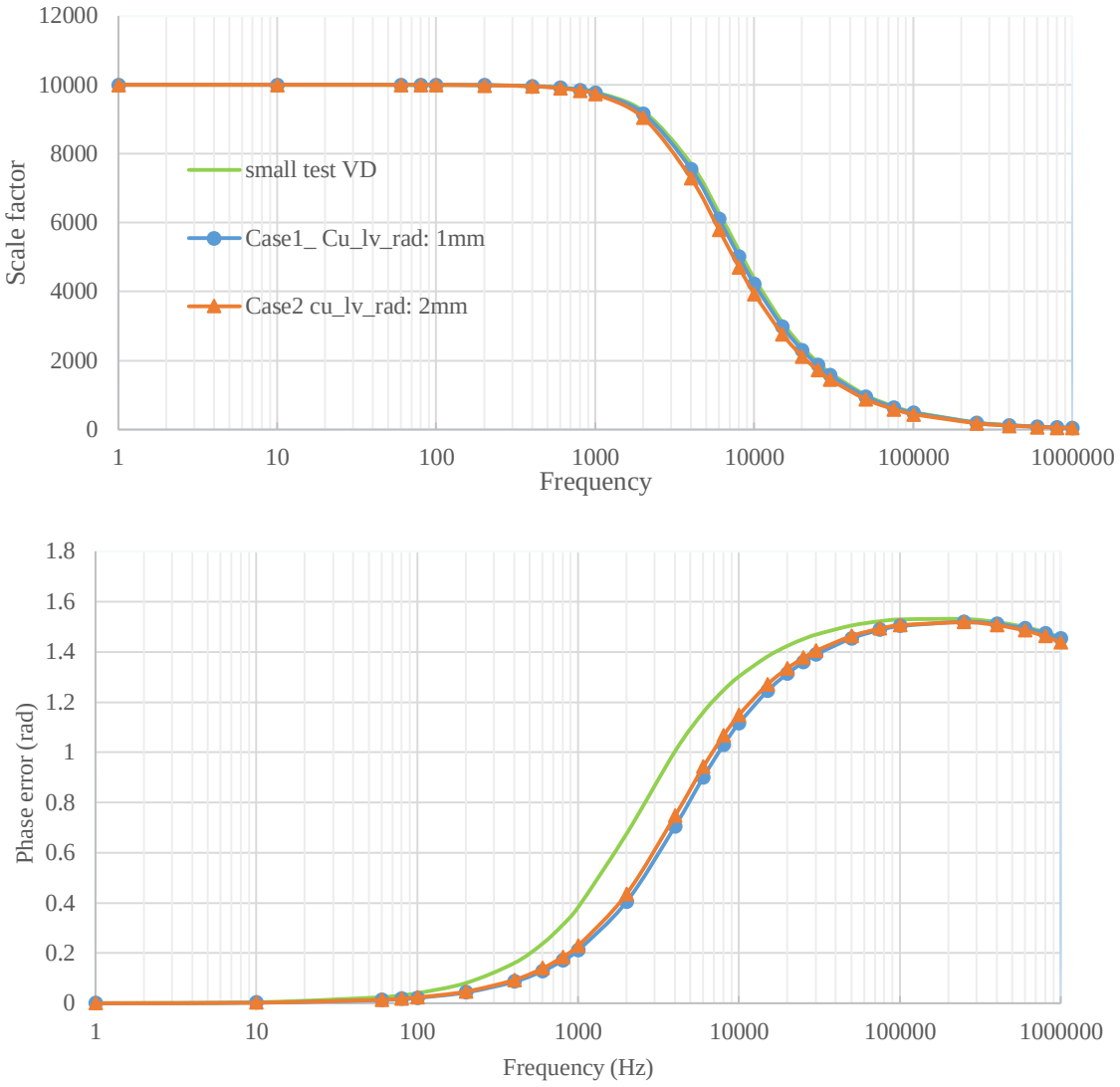


Fig. 3.4. Result of Simulation of case 1 and 2 (the results of small VD are also presented for comparison)

As can be seen from the results, case 1 and case 2 have approximately similar frequency responses. As the external surface of the conductor is decreased, all the stray capacitances CHV, CG, and CLV decreased a little. Moreover, one can be observe that higher CHV decreases the SF and the two other stray capacitances increase the SF.

3.3.1 The effect of the grounded plate size (in the initial design)

The effect of the grounded plate size on the VD frequency behavior is illustrated in Fig. 3.5. The size of the ground plate is 20000 mm^2 (200 mm × 100 mm) and 60000 mm^2 (300 mm × 200 mm) in case 1 and case 3, respectively. The small scheme depicted in

Fig. 3.5 shows the variable length and width of the plate. As can be seen from the results, case 3 with the larger ground plate has a better frequency response compared to the case 1. The reason is that in case 3 the ground plate shields the electric field between the HV part and the LV part producing a CHV decrease. Moreover, as the surface of the ground plate increases, the electric field between HV layers tends to go toward the ground plate decreasing the value of CHVs less. In addition, increasing the surface of the ground plate also increases each stray capacitances toward the ground. It means all values of CLVs and CGs increases. That is why the frequency behavior of the case 3 is better than the case 1. Then the same reason justifies decreasing the phase error as it reversely acts compared to the scale factor.

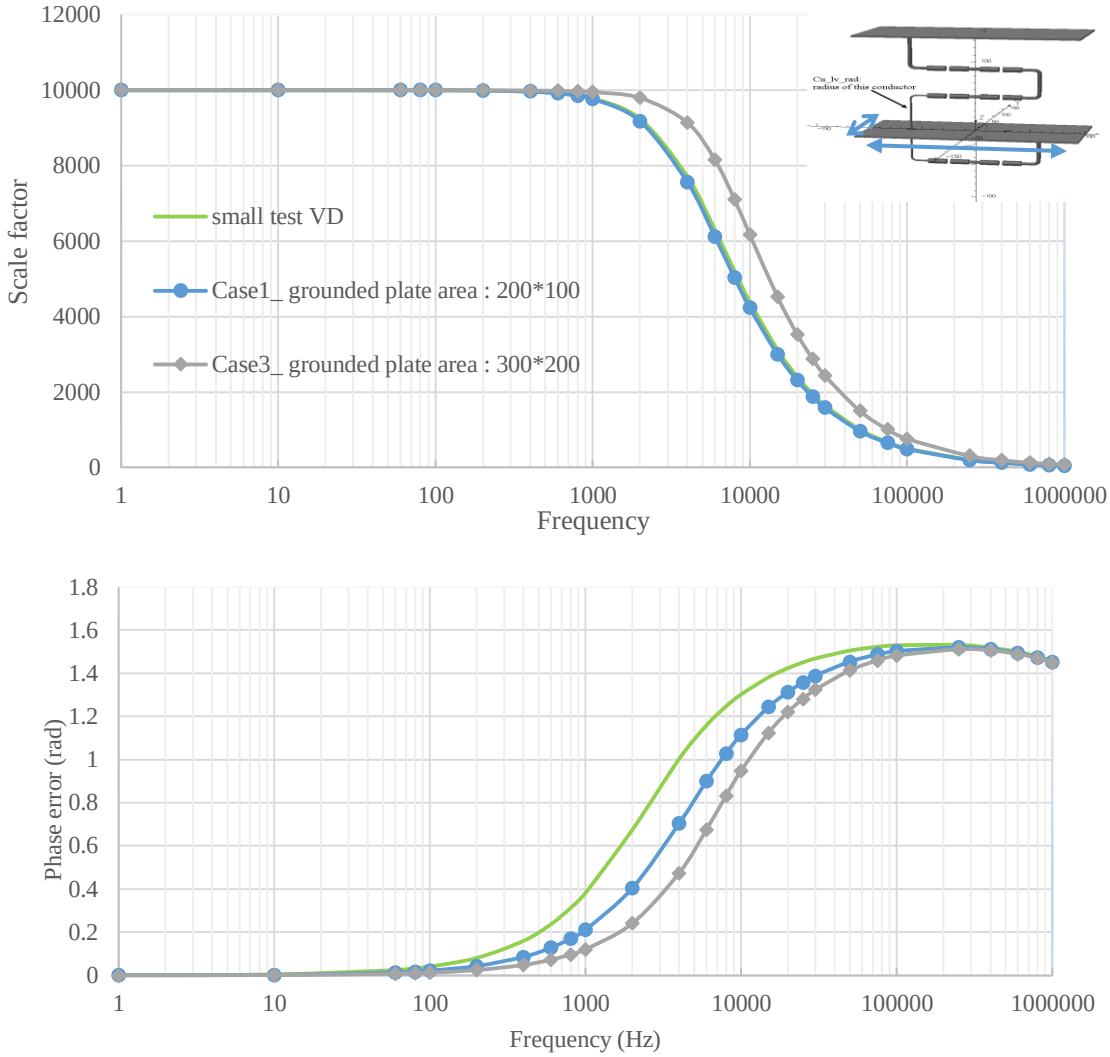


Fig. 3.5. Effect of grounded plate size of frequency behavior

3.3.2 The effect of the LV layer distance from the grounded plate (in the initial design)

The effect of distance of the LV layer from the grounded plate on the VD frequency behavior is illustrated in Fig. 3.6. The distance of the LV layer from the grounded plate is reduced from 40 mm (case 3) to 10mm (case 4). As evident in the Fig. 3.6, the case 4 with less distance between LV layer and the grounded plate shows better frequency behavior. The reason is that in case 4, electric field, previously going from the LV parts towards the HV layers, tends to go towards the ground. Then definitely, CHV values decrease, while CLV values increase. It subsequently increases SF and decreases phase error.

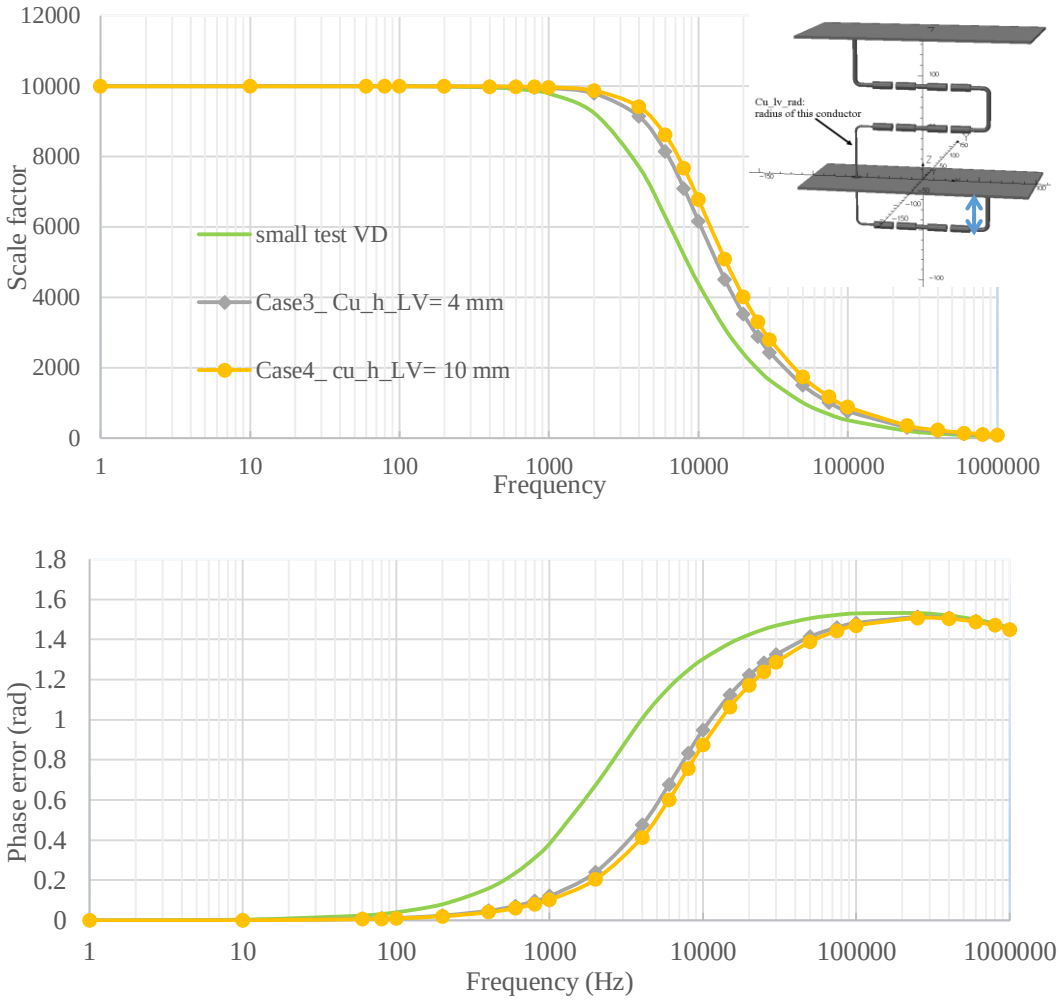


Fig. 3.6. Effect of the LV layer distance from the grounded plate

3.3.3 The effect of extra grounded plate (in the initial design)

Since the actual VD usually works near a ground floor, in the simulation one grounded plate is added simulating the ground floor at the bottom of the geometry (case 5 shown in Fig. 2.7). Case 5 is built as a variation of case 4, to make the structure more comparable to the real case.

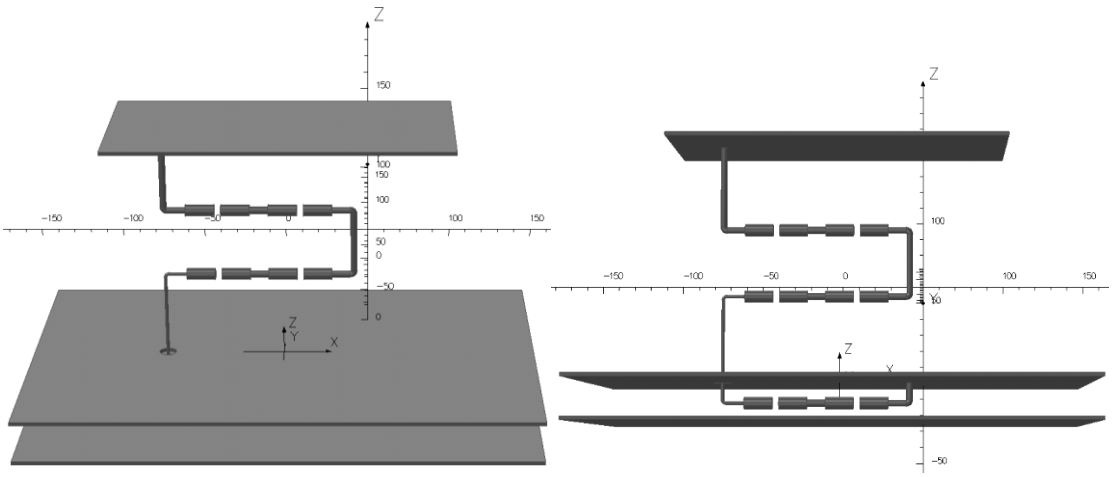


Fig. 3.7. Two different views of Simulation case 5 including two grounded plates

The effect of the extra grounded plate (ground floor) is presented in Fig. 3.8. The better frequency response (in this case more SF and less phase error) of case 5 compared to the case 4 can be noticed. It can be explained by the increase of CLV (as the surface of the ground electrode near to the LV part is doubled), while other stray capacitances are almost unchanged (as the added ground surface is far from the HV part).

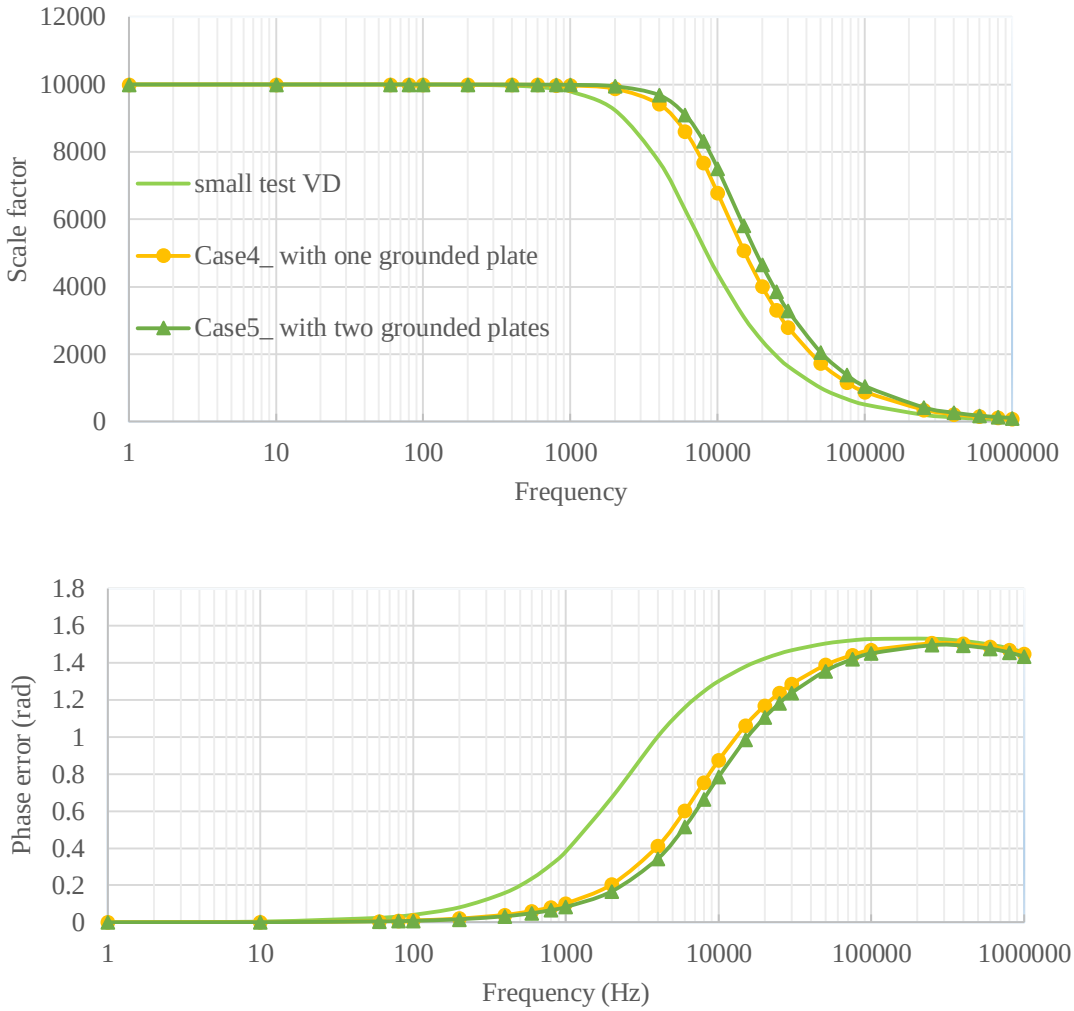


Fig. 3.8. Effect of added grounded plate on initial design of VD

3.3.4 The effect of the distance between the grounded plates and the first HV layer (initial design with double grounded plates)

In the next step the sensitivity analysis of VD versus –parameter "dis1" (the distance between the grounded plates and the first HV layer composed of the lower resistors of HV part) is investigated, by considering four different values (case1: dis1=50 mm, case2: dis1=80 mm, case3: dis1=20 mm, case4 dis1=35 mm). The distance between 2nd HV layer and 1st HV layer, and also between 2nd HV layer and HV plate are kept constant in all cases. The results shown in Fig. 3.9 demonstrates that, decreasing the mentioned distance, the scale factor increases and obviously the phase error decreases. The reason is that by increasing the parameter "dis1", stray capacitances between HV part and the ground (CG)

decreases while other kind of stray capacitances are approximately unchanged. As explained in 3.2, decreasing CG increases the SF and reduces the phase error.

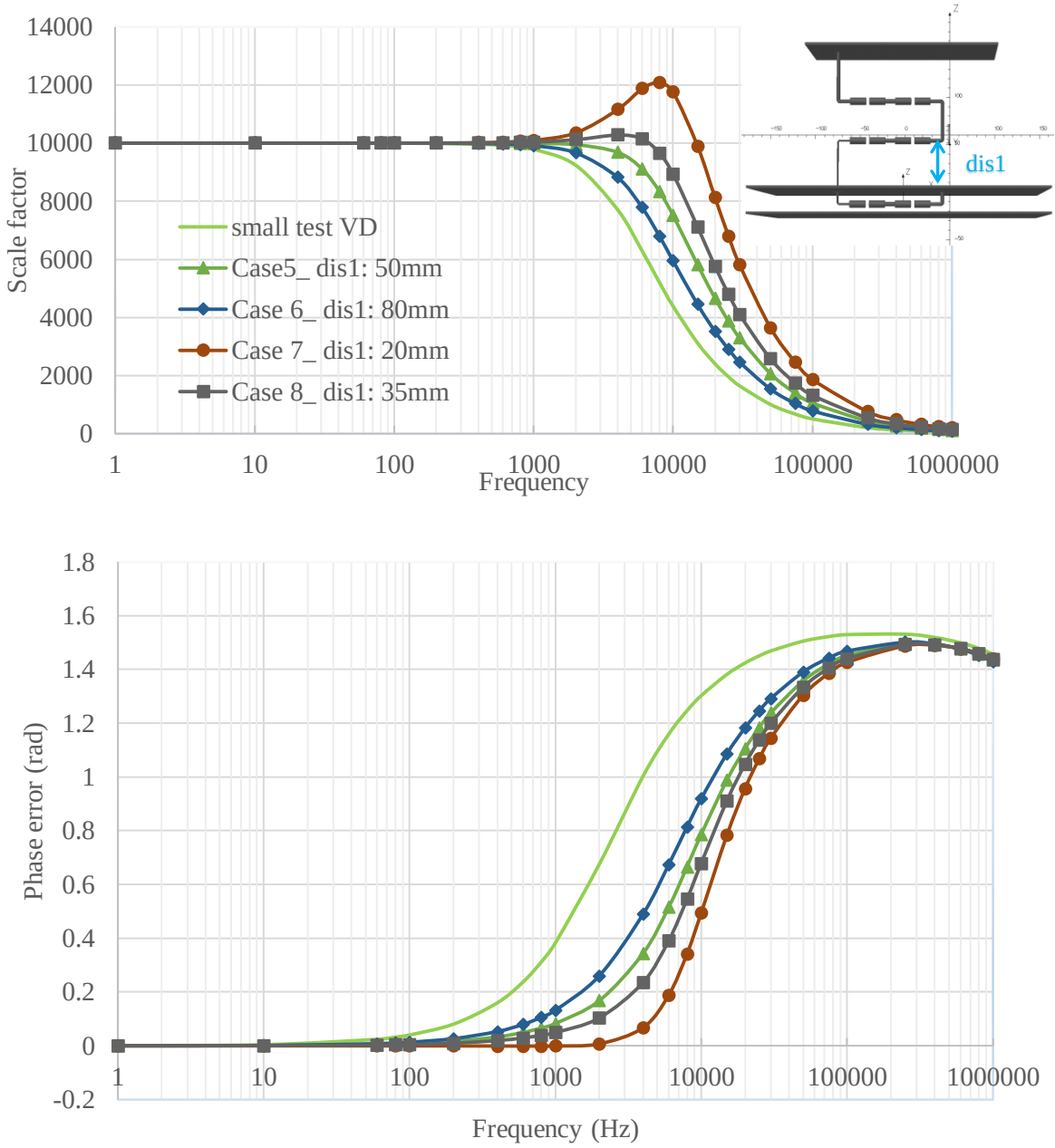


Fig. 3.9. Sensitivity analysis of VD performance versus the parameter “dis1”

3.3.5 The effect of the distance between the 1st and 2nd HV layer (in the initial design with double grounded plates)

The sensitivity analysis of the VD performance versus parameter "dis2" (the distance between 1st and 2nd HV layer) is investigated, by considering three values (case 8: dis2= 40 mm, case 9: dis2= 60 mm, case 10: dis2= 35 mm). Parameters dis1 (35 mm) and dis3 (50 mm) are kept constant. The results are shown in in Fig. 3.10 together with a small scheme which shows the variable parameter.

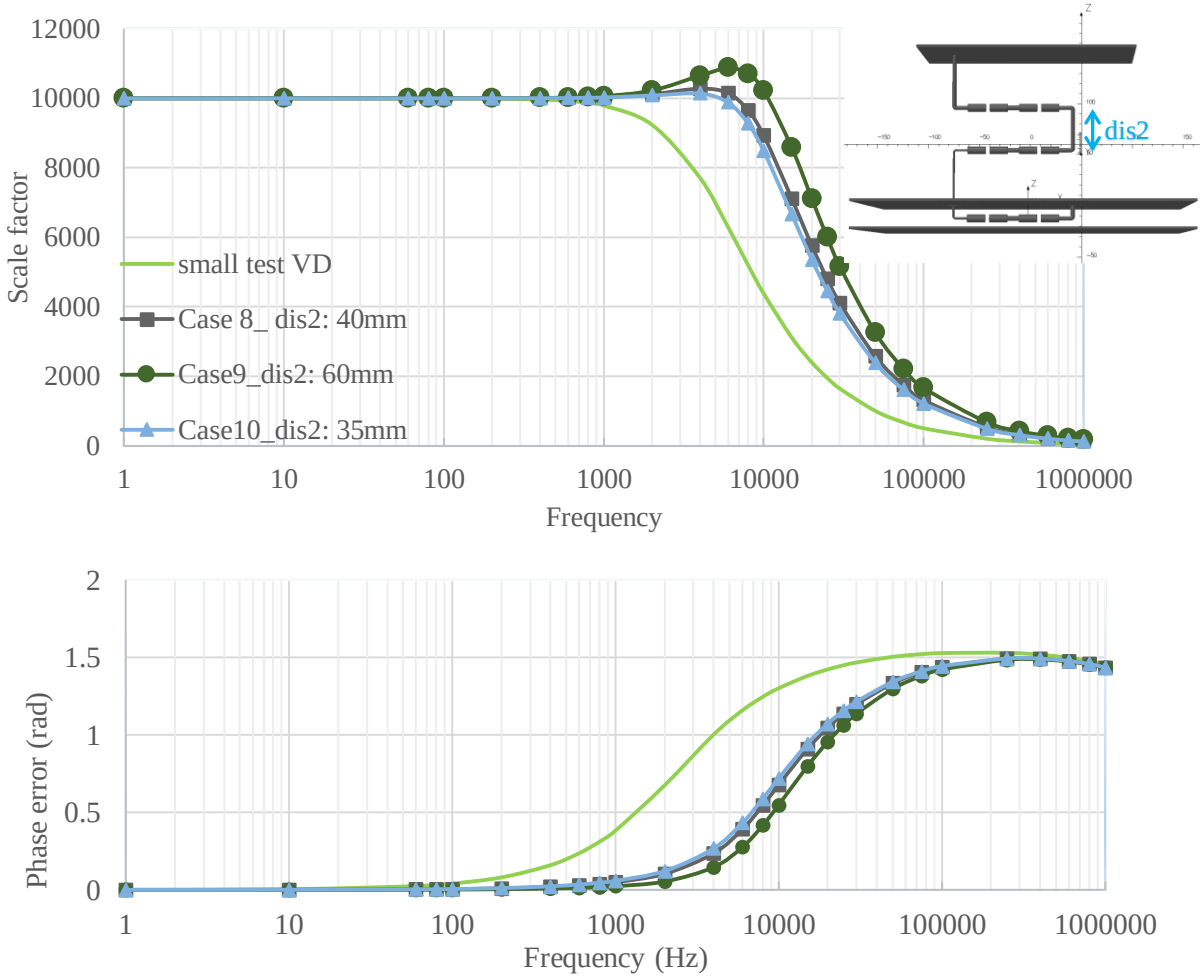


Fig. 3.10. Sensitivity analysis of VD performance versus the distance between the 1st and 2nd HV layer

As the parameter "dis2" increases, the distance between HV layers increases. Then the CHV values decreases making the SF increases. Although the CG values related to the top part of the VD decrease (making the SF less), the weight of the effect of the CHV is

greater, because HV layers are closer to each other, compared to the distance between the top part of the VD and the ground.

3.3.6 The effect of the distance between the 2nd HV layer and the Top HV plate (in the initial design with double grounded plates)

The sensitivity analysis of the VD performance versus parameter "dis3" (the distance between the 2nd HV layer and the Top HV plate) is also investigated, making constant dis1 (35 mm) and dis2 (35 mm). Results obtained with dis3 = 35 mm (case 11) are compared in Fig. 3.11. 3.

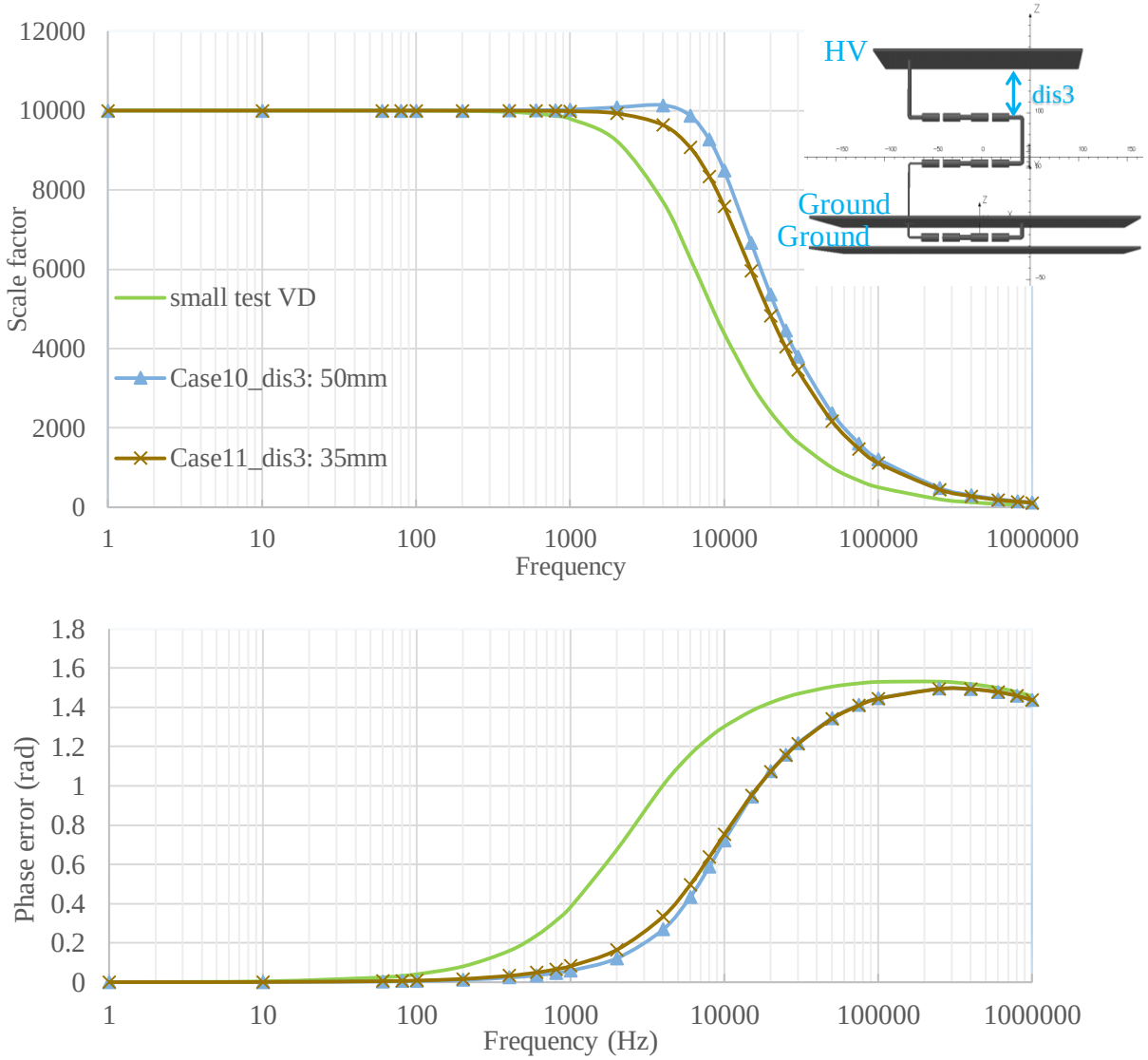


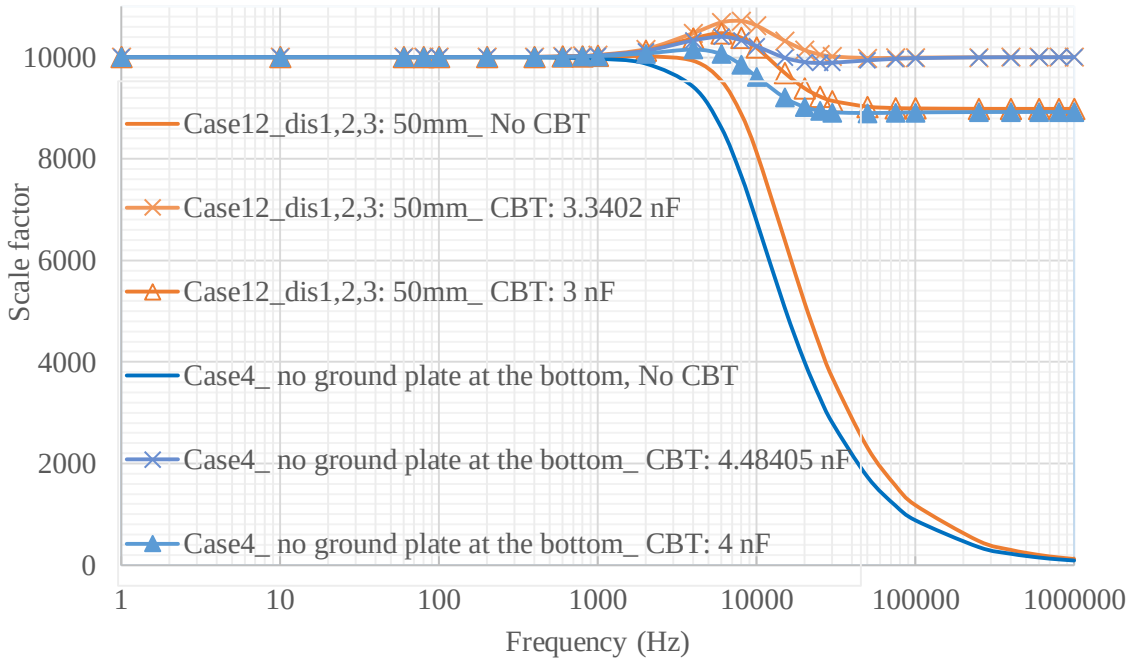
Fig. 3.11. 3Sensitivity analysis of VD performance versus the distance between the 2nd HV layer and the top HV plate

The result shown in Fig. 3.11. 3 can be justified with the same reason explained for the result shown in Fig. 3.10.

3.3.7 The effect of an external added capacitor on one and double grounded plate designs (initial designs)

In the next step, the case 4 and the case 12 (with an additional grounded plate as in case 5, dis2 is different in cases 5 and 12) with one grounded plate and double-grounded plates, respectively are chosen as reference cases, to analyze the effects of an external added capacitor (hereafter named as CBT) parallel to the output voltage. The results are shown in Fig. 3.12. As expected, increasing the CBT, which acts as a CLV, increases the SF and decreases the phase error in both arrangements. If the CBT has a value so that the SF is equalized at high (>30 kHz) and low (<1kHz) frequencies, it appears that around 8 kHz the SF increases more than 4% of its rated value not meeting the requirement for the standard voltage transducer.

Therefore, the design should be changed in order to limit the SF increase around this frequency range. In another words, there is need for a pole in the transfer function of the VD. For this purpose, the CHV should be increased.



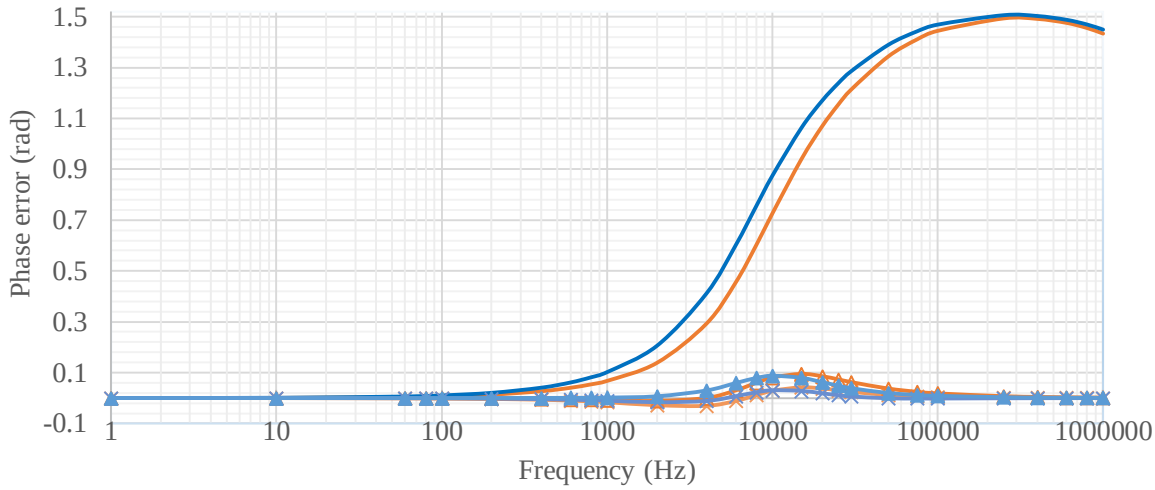


Fig. 3.12. The effect of CBT on the VD frequency behavior

3.3.8 Study of a VD design with an LV connected plate (two resistors in each HV layer)

As a first attempt in order to increase the CHV values, the plate between the LV part and the HV part is connected to the LV instead of the ground. This solution should shield the electric field going from HV towards the ground. This means the CHV values should increase, while CG and also CLV values should decrease in comparison with the arrangement where this plate is grounded. Two different views of the initial design of the VD with the middle LV plate (case 13) are shown in Fig. 3.13, where three plates are connected to HV, LV, and the ground from top to the bottom, respectively. All three distances between the HV layers and also between HV layers and nearest plates are 35mm.

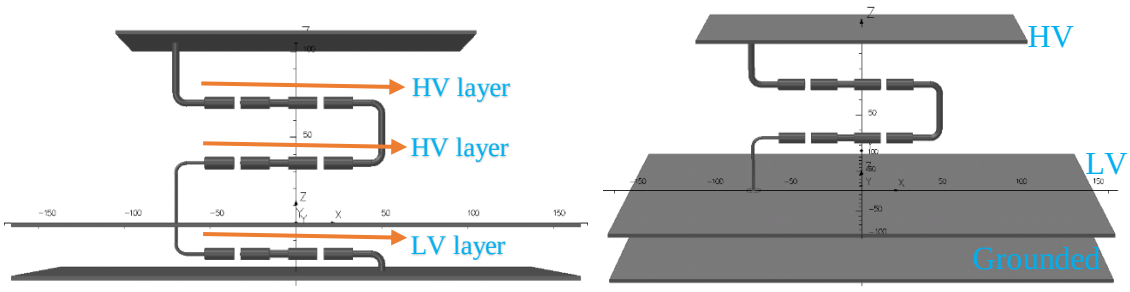


Fig. 3.13. Initial design of RVD with LV-connected plate (the middle plate is connected to the LV)

For study the effect of LV added plate, two different designs (cases 11 and 13) are compared and the results are presented in Fig. 3.14. The whole geometry and distances in the arrangements of cases 11 and 13 are the same except the electric connection of the middle plate.

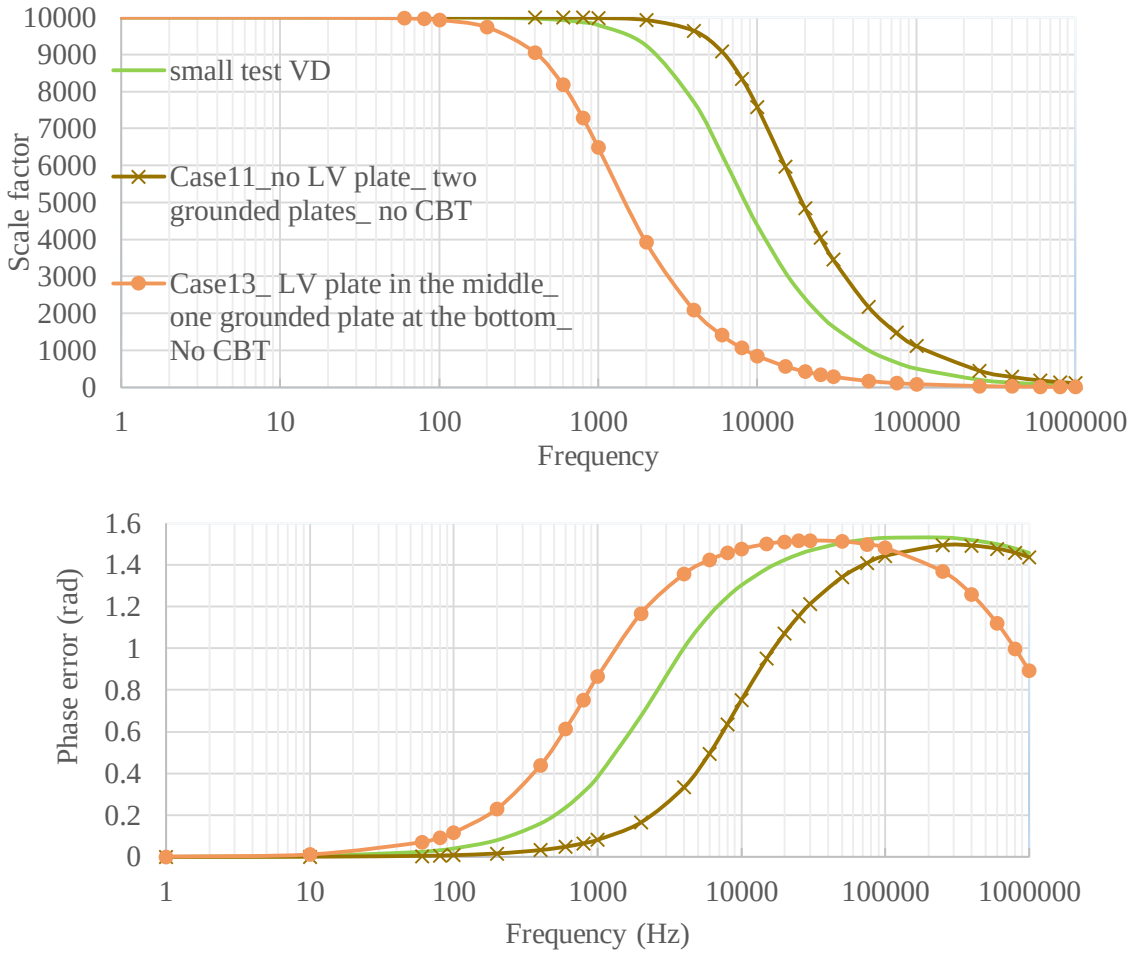


Fig. 3.14. The effect of adding an LV-connected plate on frequency behavior of the RVD

The results of the case 13 show a worsening with respect to the case 11 in both SF and phase error, because in case 13 CHV increases and CG and CLV decrease.

In the next step, the CBT is modified for each case to get the SF in high frequency equal to the rated SF. As expected and explained before, the new design shows much better results (Fig. 3.15). In case 13 the maximum SF deviation from the rated value is about %0.30 which does not meet the requirement for a reference tool (although showing the best result up to now) and still needs to be improved.

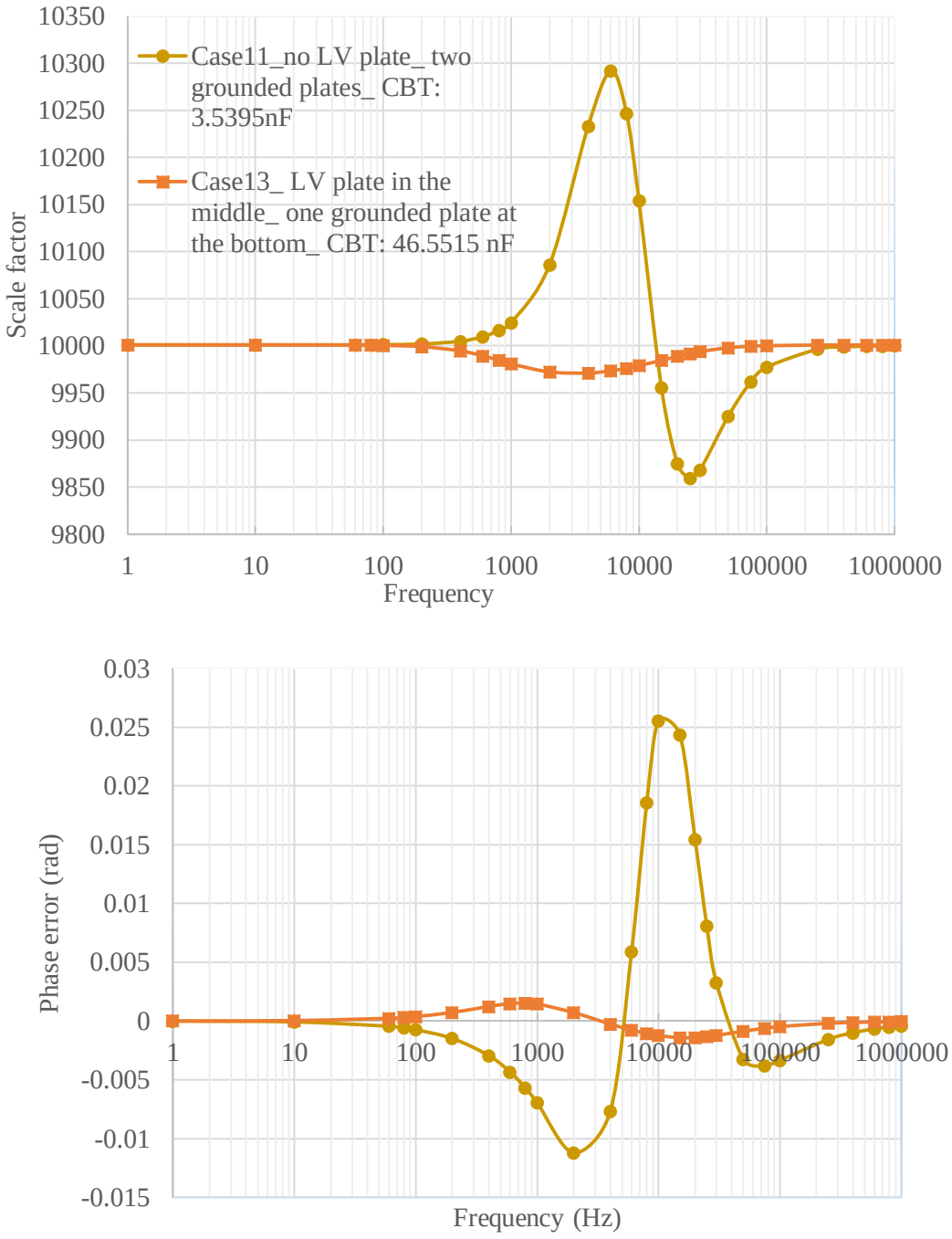


Fig. 3.15. The effect of added LV-connected plate on frequency behavior of the RVD with added CBT

Parameters of "dis1", "dis2", and "dis3" and the condition of bottom and middle plate for cases from 1 up to 13 are presented in Table 3.3.

Table 3.3. Parametrs and connection of different plates in the cases from 1 up to 13

	dis1 (mm)	dis2 (mm)	dis3 (mm)	Grounded middle plate	Grounded bottom plate	LV middle plate
Case 1	50	40	50	✓	-	-
Case 2	50	40	50	✓	-	-
Case 3	50	40	50	✓	-	-
Case 4	50	40	50	✓	-	-
Case 5	50	40	50	✓	✓	-
Case 6	80	40	50	✓	✓	-
Case 7	20	40	50	✓	✓	-
Case 8	35	40	50	✓	✓	-
Case 9	35	60	50	✓	✓	-
Case 10	35	35	50	✓	✓	-
Case 11	35	35	35	✓	✓	-
Case 12	50	50	50	✓	✓	-
Case 13	35	35	35	-	✓	✓

3.3.9 Study of a VD design with one resistor in each HV layer (with an LV connected plate)

Next, another geometry design will be tested by inserting only one (instead of two) resistor in each HV layer (case 14), while the distances between layers and size of the plates are the same as in case 13. The geometry of case 14 is shown in Fig. 3.16.

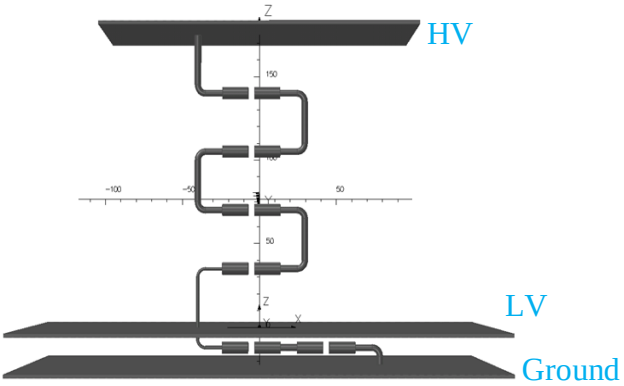


Fig. 3.16. Geometry of the case 14 with one resistor in each HV layer

The result of cases 13 and 14 are compared in Fig. 3.17.

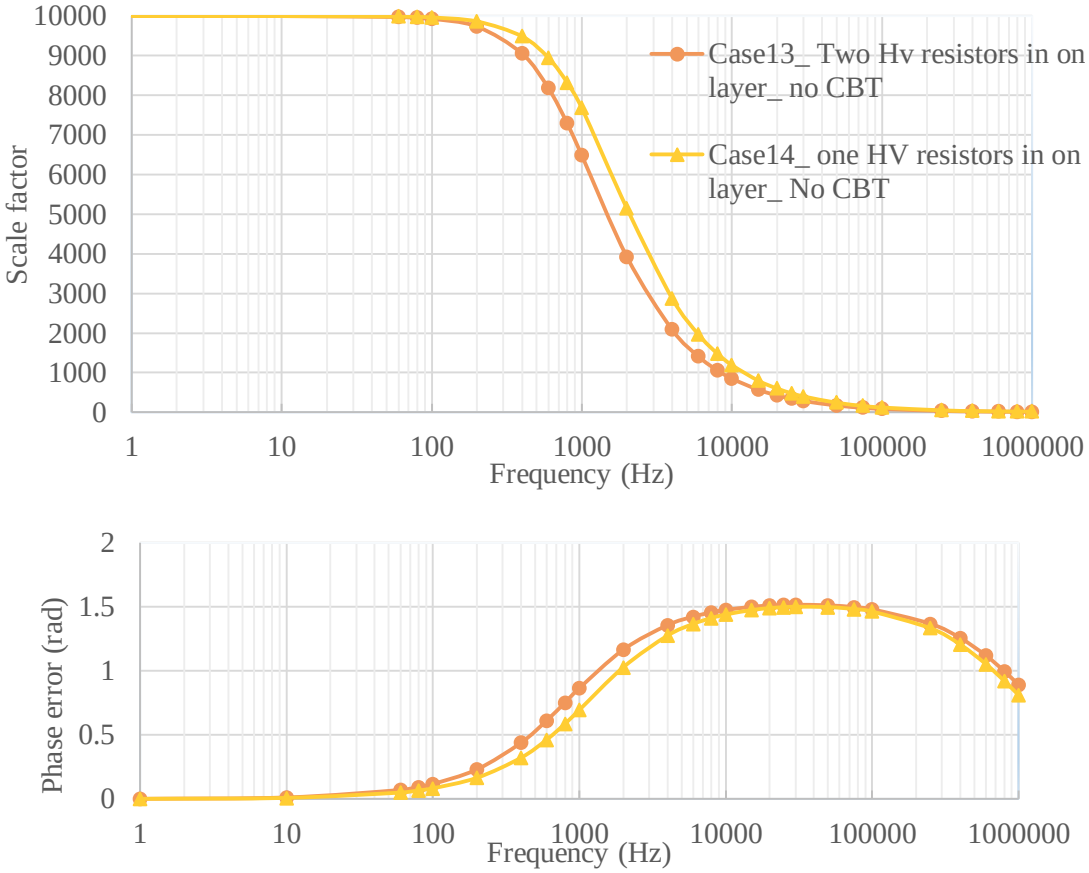


Fig. 3.17. Results of cases 13 and 14

In case 14 the CLV cannot be changed much compared to the case 13 as in both cases the LV layer is sandwiched between two plates and the electric field does not change significantly near to the LV layer. In addition, the CG has negligible variations, as HV layers are shielded from the ground by the LV-connected plate. However, the CHV values considerably decrease, as the distance between top parts of HV section and the LV-connected plate increases. It should be mentioned that the biggest stray capacitance is the one between the HV plate and the LV-connected plate. Then, if the distance between the top HV plate and the LV plate increases, the stray capacitance between these two plates changes a lot more than other stray capacitances. Decrease of the aforementioned stray capacitance is, hereupon, more than other capacitances in case 14 (compared to the case 13). Therefore, the SF of case 14 increases, while the phase error subsequently decreases.

Fig. 3.18 shows the results of cases 13 and 14 obtained by adding a CBT whose value is such that the high frequency SF remains the same as the rated one. As it can be seen, the deviation from the rated SF of the SF in case 14 (around 0.25%) is less than that of in

case 13. The change of the arrangement from case 13 to 14 slightly improved the transducer response. However, in the light of the studies of the laboratory ground (Section 0) such advantage must be revised.

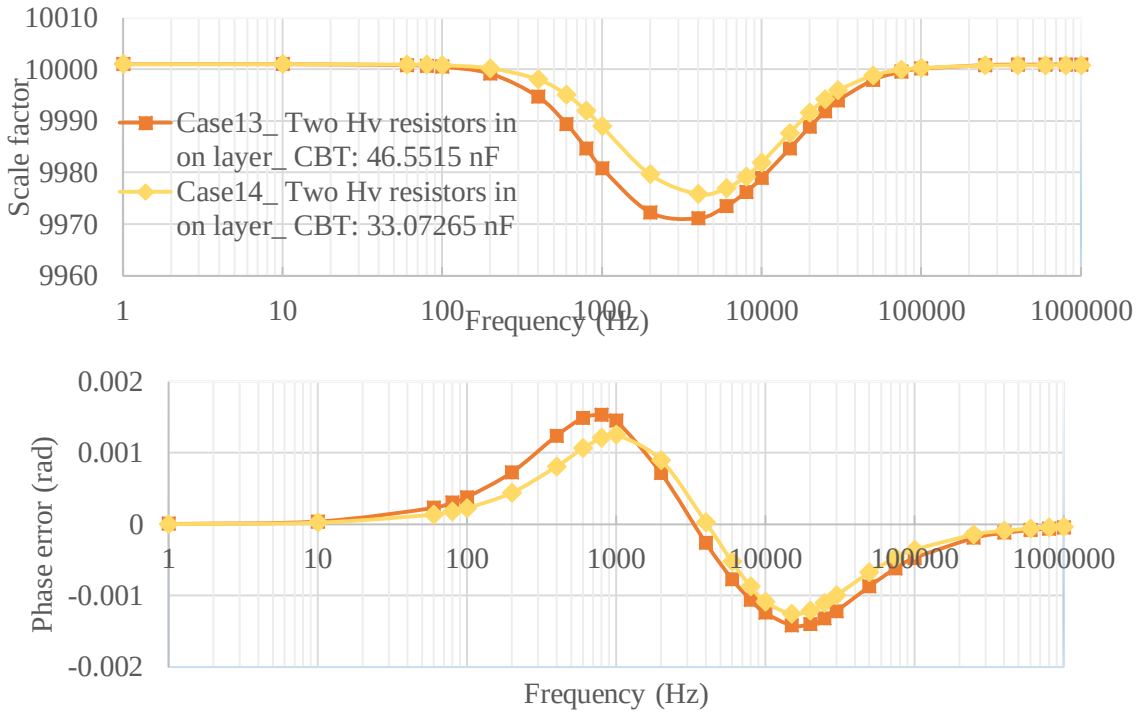


Fig. 3.18. The result of cases 13 and 14 with the CBT

Up to here, all simulations have been done without considering the value of resistors or the input voltage. In other words, the cases 1 up to 14 have been simulated only to have a general view of the effect of different parameters or the influence of different plates used in the VD. In the next section the rated voltage and resistor values will be taken into account because the final designed reference VD realized.

3.4 Study of vertical VD design consisting 6W, 30kV resistors

The availability on the market of recent HV resistors with higher power (30 kV, 6W) makes some different designs and geometries possible. The new arrangements using the new HV resistors are presented in the following.

The case 16 uses one 10 MΩ resistor in the HV part and two 500 Ω resistor in the LV part and its geometry is depicted in Fig. 3.19. The middle plate is connected to the LV, while the top and bottom plates are connected to the HV and ground, respectively. The results of case 16 are shown in Fig. 3.20, having used a tuned CBT (a single extra

capacitor added parallel to the output voltage) which gives rise to the high frequency SF similar to the rated one.

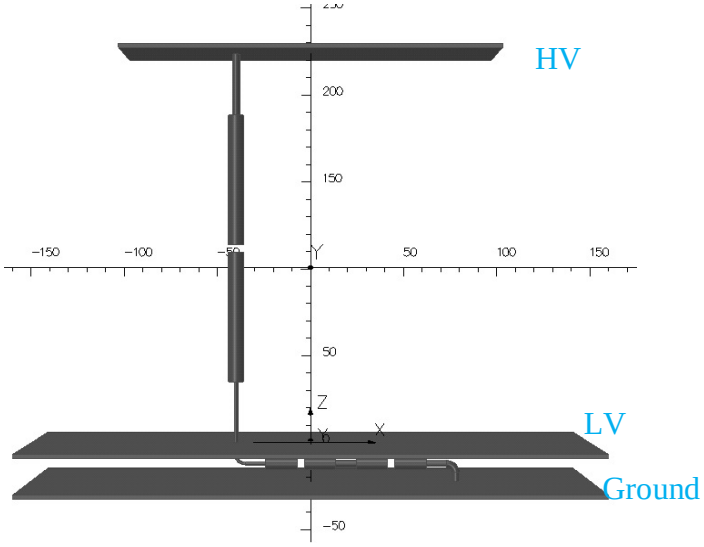


Fig. 3.19. The geometry of case 16 with a 30kV resistor

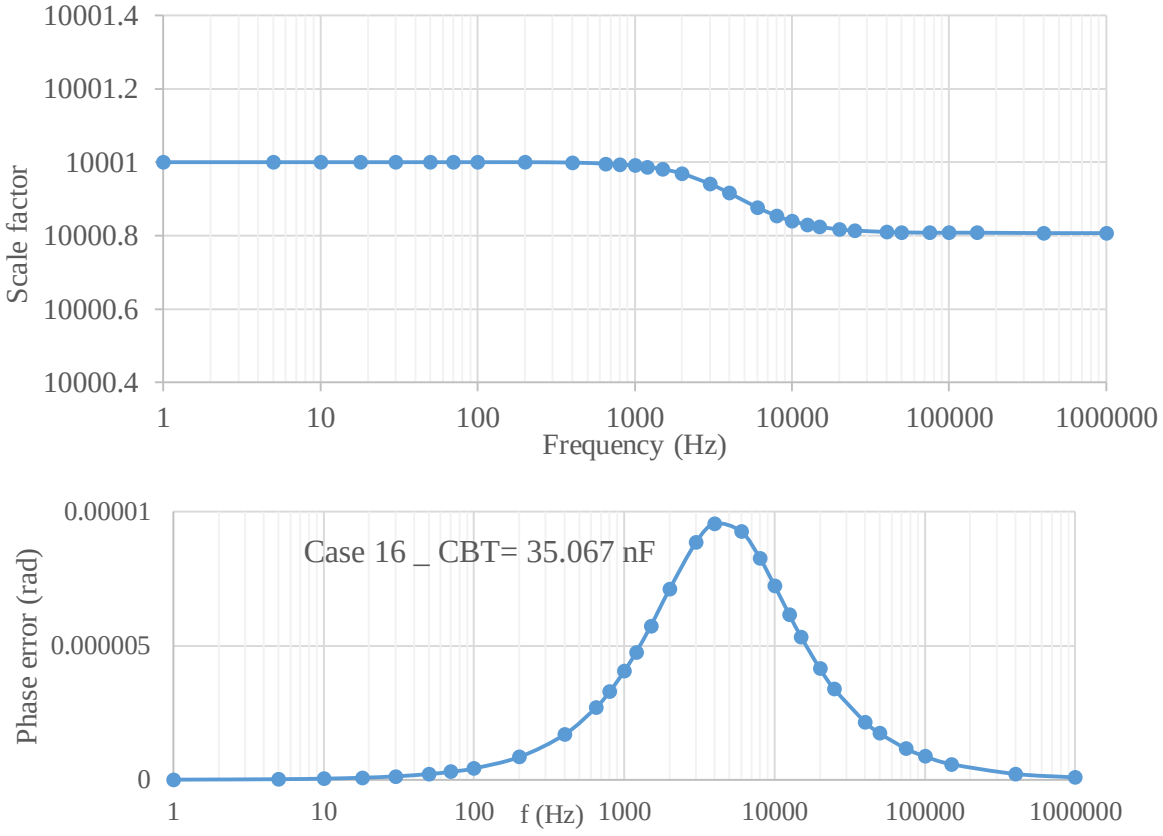


Fig. 3.20. Result of the case 16 with CBT

As can be seen in Fig. 3.20, in case 16 the maximum deviation of the SF from its rated value is less than 0.002%. The case 16 could be used up to 7.75 kV considering the maximum 6 W for the 10 MΩ HV resistor.

The result of the case 16 with the HV resistor is far better than the results of RVD designs using LV resistors in the HV part (cases from 1 to 14). The following thereupon will study the RVDs using 6W HV resistors.

3.4.1 Study of a vertical VD design with rounded plates

For the voltages in the range of kilovolt, there could be hot spots of electric fields in the body of the VD. Therefore, rounded edges are preferred in comparison with the sharp edges in the body of the VD. Then, in order to be closer to a practical VD, case 17 (shown in Fig. 3.21) utilizes two rounded plates (with the radius of 20 cm) placed at the bottom and top of the VD. There are three 10 MΩ HV resistors in HV part and one 3 kΩ resistor in the LV part. This RVD can be used up to 23 kV, taking into account the 6W maximum power for each HV resistor. The radius of the LV-connected plate is 141mm. The results of the case 17 using the tuned CBT to get the rated SF at high frequency are shown in Fig. 3.22. The deviation of around 5.2% from rated SF is far from the requirement for a reference tool.

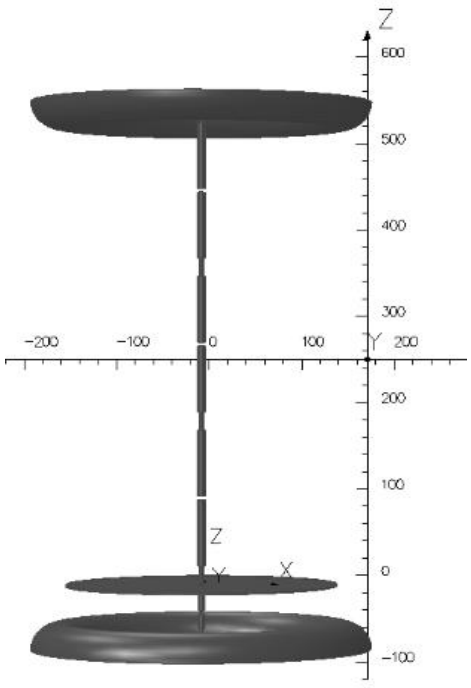


Fig. 3.21. The geometry of case 17

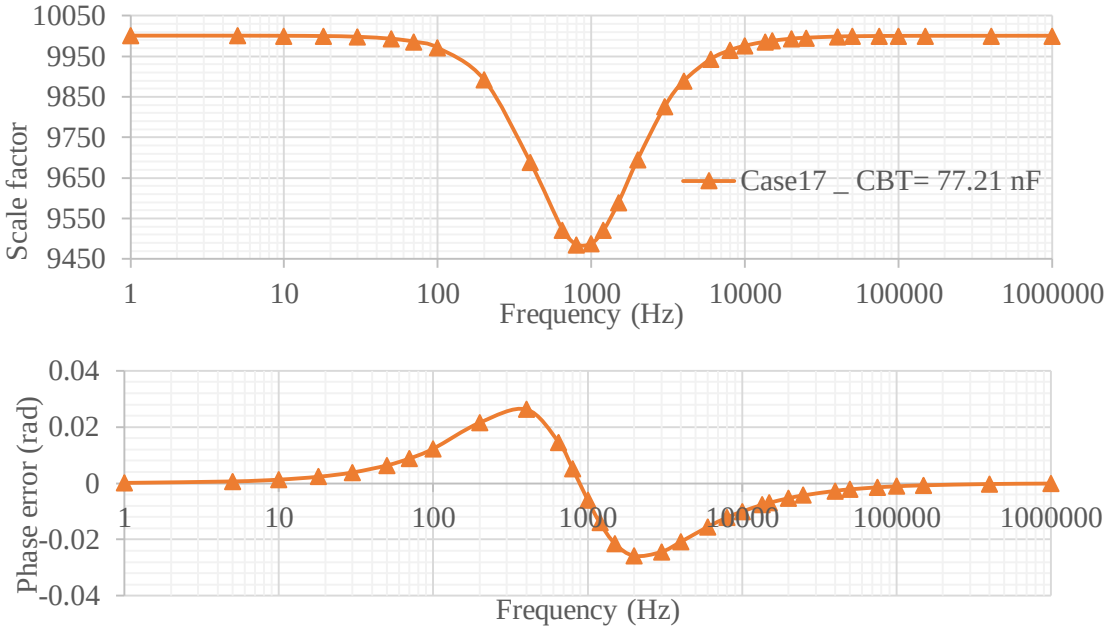


Fig. 3.22. The result of case 17 with CBT

3.4.2 Effect of the LV plate radius on the vertical VD design with rounded plates

In order to check out the effect of the radius of the LV-connected plate on the frequency behavior of the RVD, the case 18 and 18.2 (with three 30MΩ HV resistors and 9 kΩ and geometry similar to the case 17) with different radii for the LV-connected plate are simulated. The radius of the LV-connected plate is 140, 171, and 100 mm for the cases 17, 18, and 18.2, respectively. The SF of cases 17, 18, and 18.2 are displayed in Fig. 3.24.

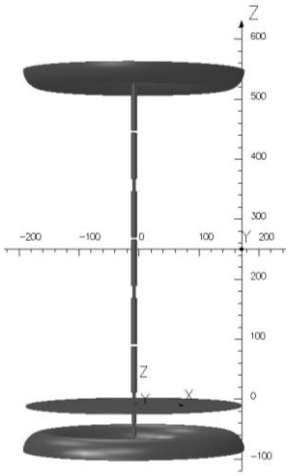


Fig. 3.23. The geometry of case 18

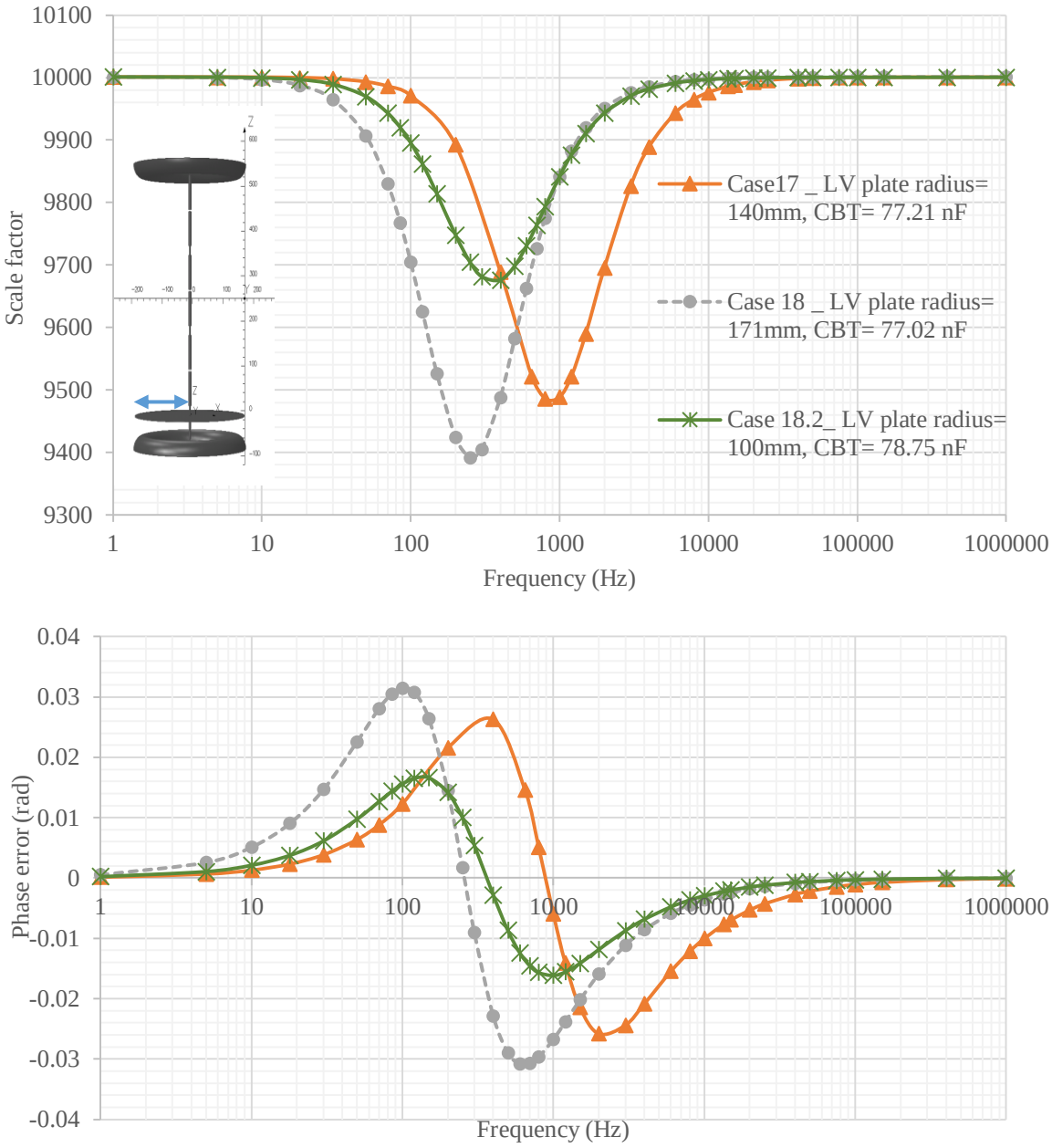


Fig. 3.24. The effect of the LV-connected Plate radius

As can be seen bigger LV-connected plate worsens the frequency behavior of the VD. The reason is that the stray capacitances between HV electrodes (CHV) increase while the CG decreases as the bigger plate (LV-connected) better shields the HV part from the ground. Both of these effects worsens the frequency behavior as explained before.

Although the result with higher radius LV-connected plate shows more deviation of SF from the rated SF, the LV-connected plate radius will be kept big in the next simulation

cases because, in my opinion, the big plate should shield some stray capacitance versus the ground, which was not seen up to now in the simulations. The reason is that the result may be better in the simulation in which there is no grounded floor, but in reality, there will be a grounded floor below the VD in experiment that makes the result of the simulation not reliable. That is why the weight of the effect of the CG should be kept small by choosing a larger radius for the LV-connected plate.

3.4.3 Study of the vertical VD design with four 30kV resistors

Although the case 18 could be used up to 40 kV considering 6W for each HV resistor, four HV resistor are employed in case 19 (shown in Fig. 3.25) to prevent HV resistors using maximum rated that might cause higher temperatures and consequently an actual worse frequency behavior. The results of case 19, illustrated in Fig. 3.26, show that the voltage could be used up to 53.6 kV with 6 W consumed by each HV resistor; and up to 30 kV with consumed power limited to 1.87 W so that a confident distance from the maximum power of each resistor is ensured. The SF deviation from its rated value is about 2.8%, still far from the requirement. The maximum phase error is about 15 mrad again far from the requirement.

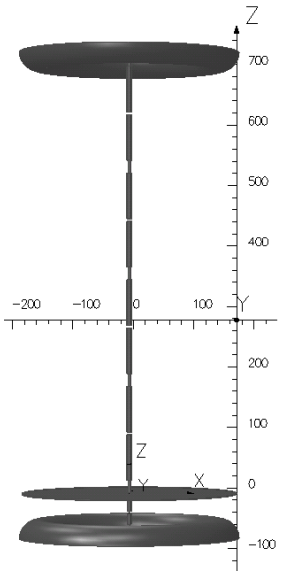


Fig. 3.25. The geometry of the case 19

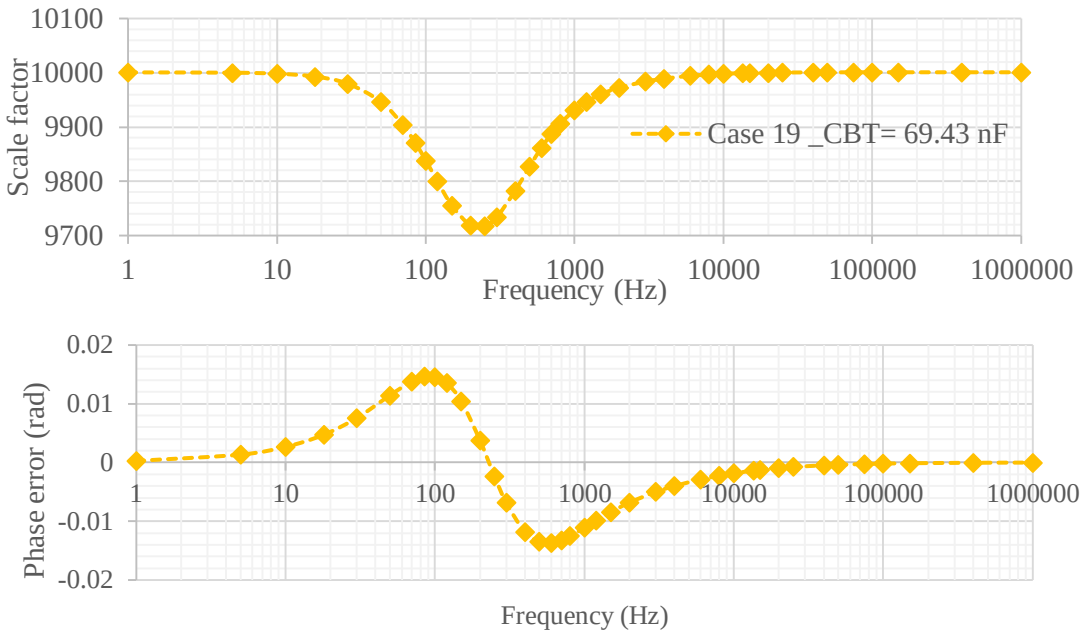


Fig. 3.26. The result of the case 19 with four HV resistors

The geometry in case 20 is similar to the case 19 but the radius of the LV-connected plate is increased up to about 200 mm, large enough to shield the HV part from the ground. A comparison between two cases 19 and 20 is shown in Fig. 3.27.

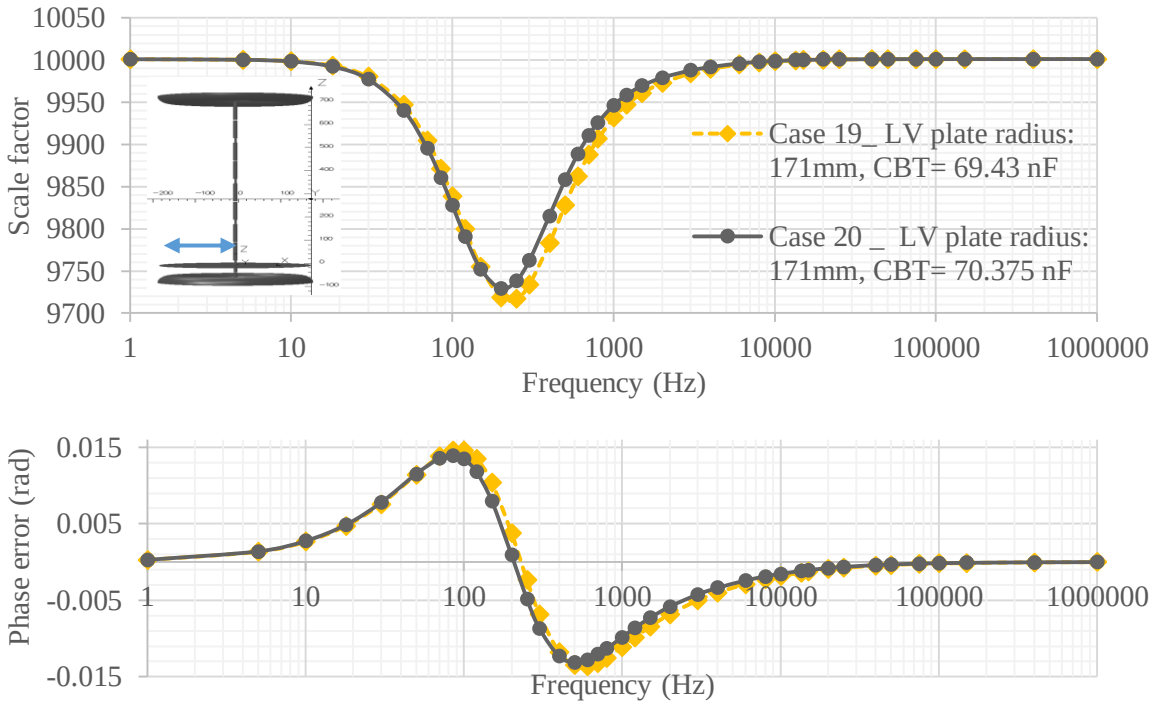


Fig. 3.27. Comparison between results of cases 19 and 20

As can be seen the case 20 with larger LV-connected plate improves in a very limited way the frequency response.

3.4.4 The effect of the distance between LV and ground plates in vertical VD

To analyze the effect of the distance between LV and ground plates (here named "#G"), the geometry of case 21.1 has been simulated, where the mentioned distance becomes about 137.5 mm, with respect to 67.5 mm for case 20, while the other dimensions remain unchanged. The comparison between two results is depicted in Fig. 3.28. The results of case 21.1 show a deviation from rated SF of ~0.11% (with maximum ~0.5 mrad phase error) which is 45 times better than the requirement of a standard device of voltage transducer.

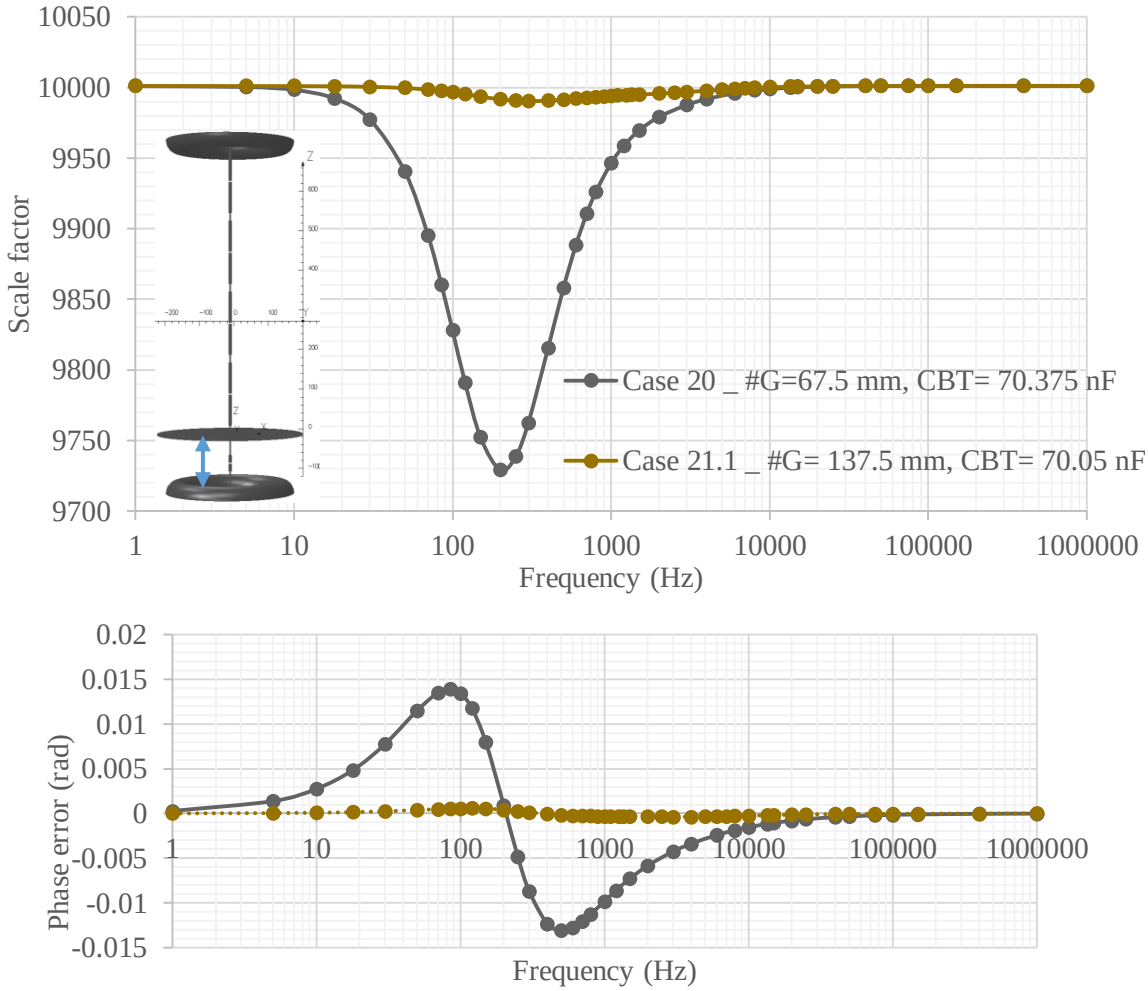


Fig. 3.28. Comparison between results of cases 20 and 21

It seems that the RVD with vertically placed resistors could give a good result. However, it could be considered as big in size compared to the voltage transducers in the similar voltage range. In the next section, the possibility of having good frequency behavior from a smaller VD configuration will be investigated. If the result is promising, the smaller (new) configuration will be realized. Otherwise, the study will be continued on the RVD with vertically placed resistors in order to improve its results and to realize it.

3.5 Study of horizontal VD designs consisting 6W, 30kV resistors

In order to decrease the volume of the VD and to investigate the possibility of acquiring a frequency response better than the case 21.1, other arrangements will be developed using horizontally placed resistors. The first design with horizontally placed HV resistors has been presented in Fig. 3.29 as case 22. The structure uses four HV 30 MΩ resistors with an LV-connected plate radius of 200 mm analogous to the case 21.1.

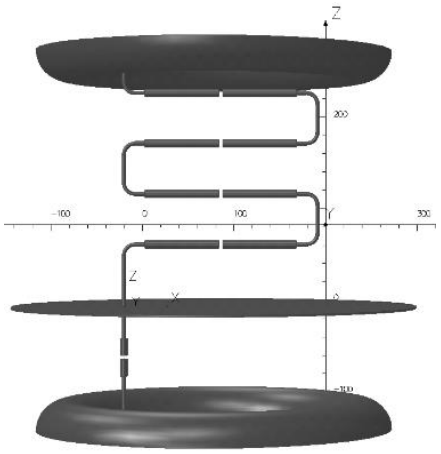


Fig. 3.29. The initial design of the horizontally placed HV resistors as case 22

The next subsection will analyze the effects of four parameters: the distance between LV plate and first HV layer (dis1), the distance between HV layers (dis2), the distance between LV and ground plates (#G), and the radius of the LV plate (#Pr). In each analysis, all but one parameters will be kept constant and the frequency response of the VD will be studied.

3.5.1 The sensitivity analysis of horizontal VD

As a first attempt the effect of the distance between LV and ground plates (#G) is investigated, while the distances dis1, dis2, and #Pr are set to 61 mm, 50 mm, and 200 mm, respectively. The results of cases from 22 to 26 with different #G values are shown in Fig. 3.30. As could be seen, the optimum #G value is about 87.5 mm.

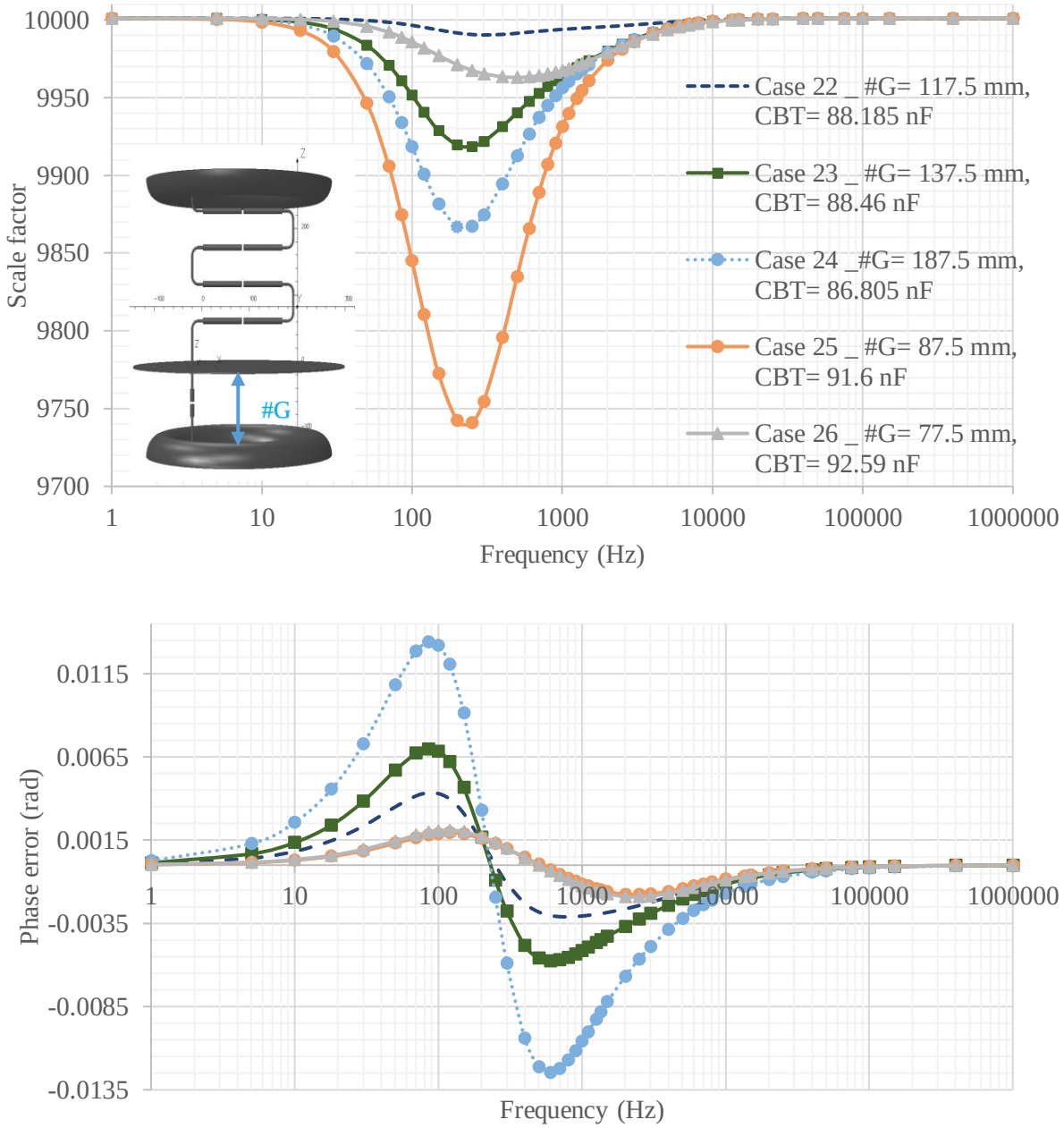


Fig. 3.30. The effect of "#G" on the SF of the RVD

Among the studied cases (from case 22 to 26), the case 25 (#G = 87.5 mm) provides the best results. The maximum deviation of SF from the rated value is 0.38% and the maximum phase error is ~0.2 mrad, in case 25. In the following, the "#G" will be kept constant to the best value and other parameters will be changed one by one.

3.5.2 The effect of the parameter "dis2" on horizontal VD

In the case 27 the results for a different dis2 value (60 mm) are compared with case 25 (dis2 = 50 mm) and depicted in Fig. 3.31.

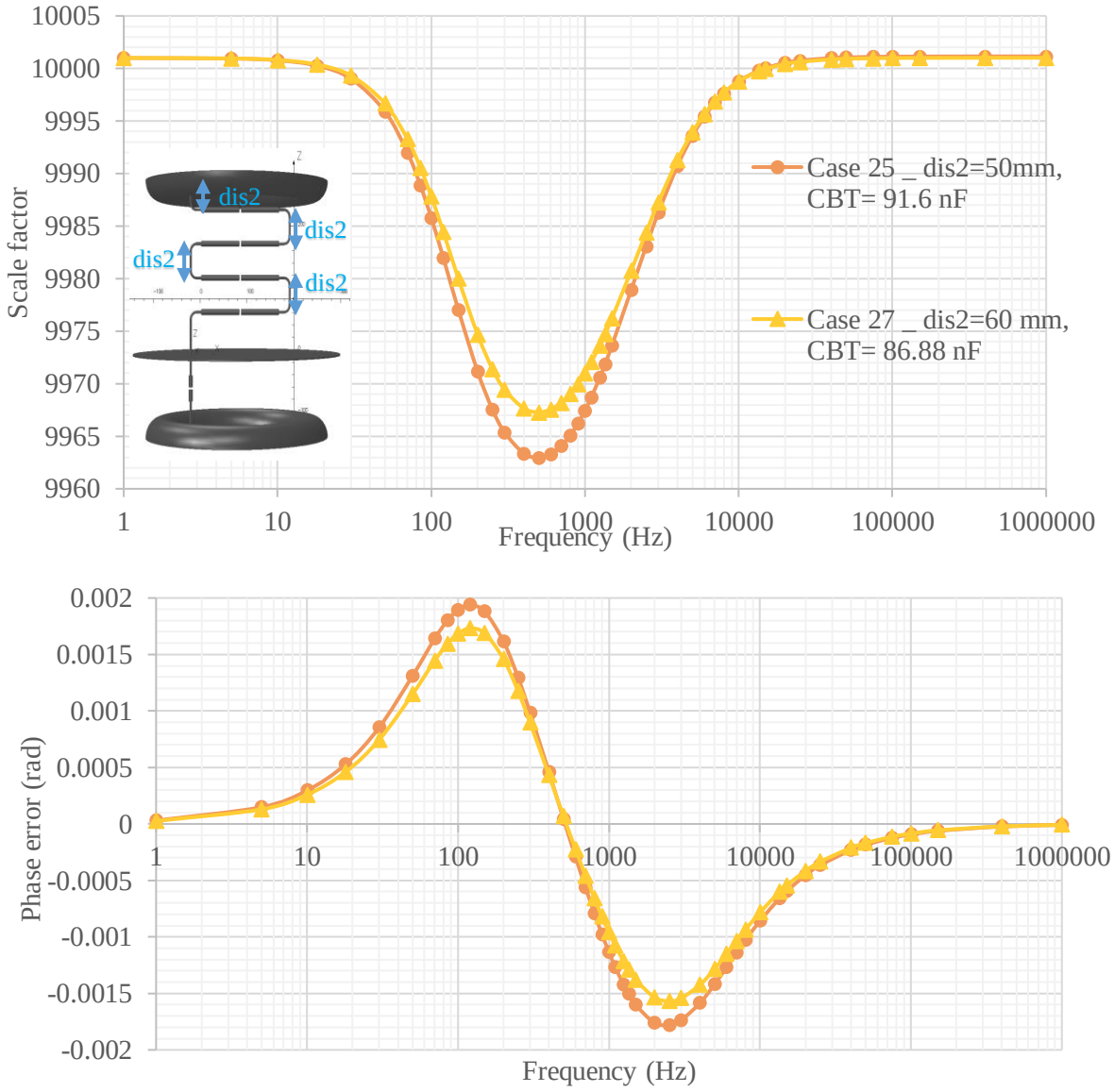


Fig. 3.31. Comparison between result of cases 25 and 27

As could be seen, the case 27 improves the results: the deviation of SF is ~0.33% far from the rated value and the maximum phase error reduces to ~1.7 mrad. For the next steps, the distance dis2 will be kept constant to 60 mm and the parameter dis1 will be changed.

The results of case 28 (dis1 = 81 mm) in comparison with those the case 27 (dis1= 61mm) are represented in Fig. 3.32.

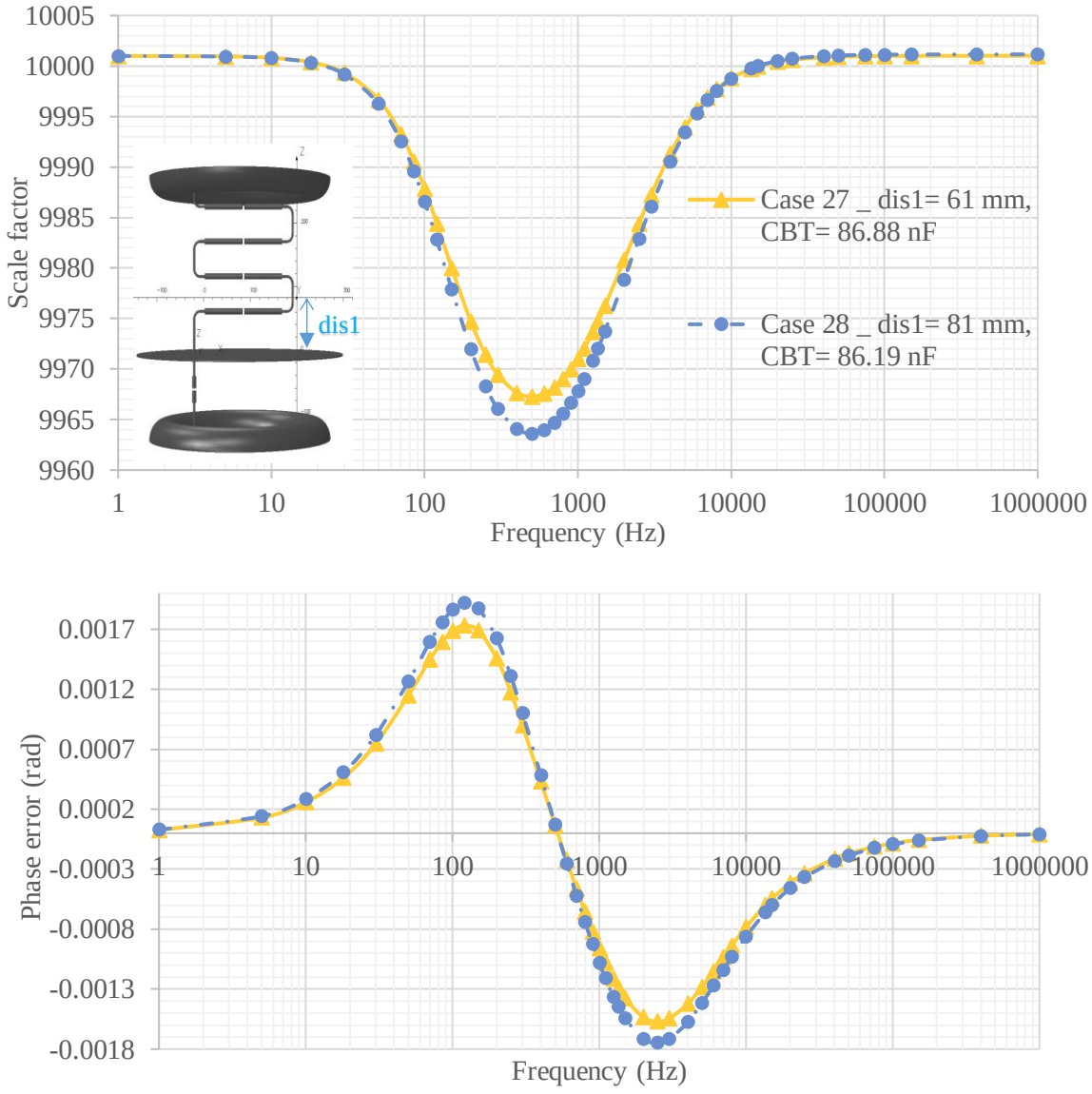


Fig. 3.32. The comparison between result of case 27 and 28

The three geometry variables; dis1, dis2 and #G are changed in next cases to check whether there could be any better frequency response for the horizontally placed HV resistors.

In cases 29 and 30, parameters dis1 and dis2 are kept to 81mm and 60 mm, respectively like those in case 28, while #G is set to 87.5 mm, 107.5 mm, and 127.5 mm in cases 28, 29, and 30, respectively. The results are shown in Fig. 3.33. None of preceding cases improves results with respect to the case 27.

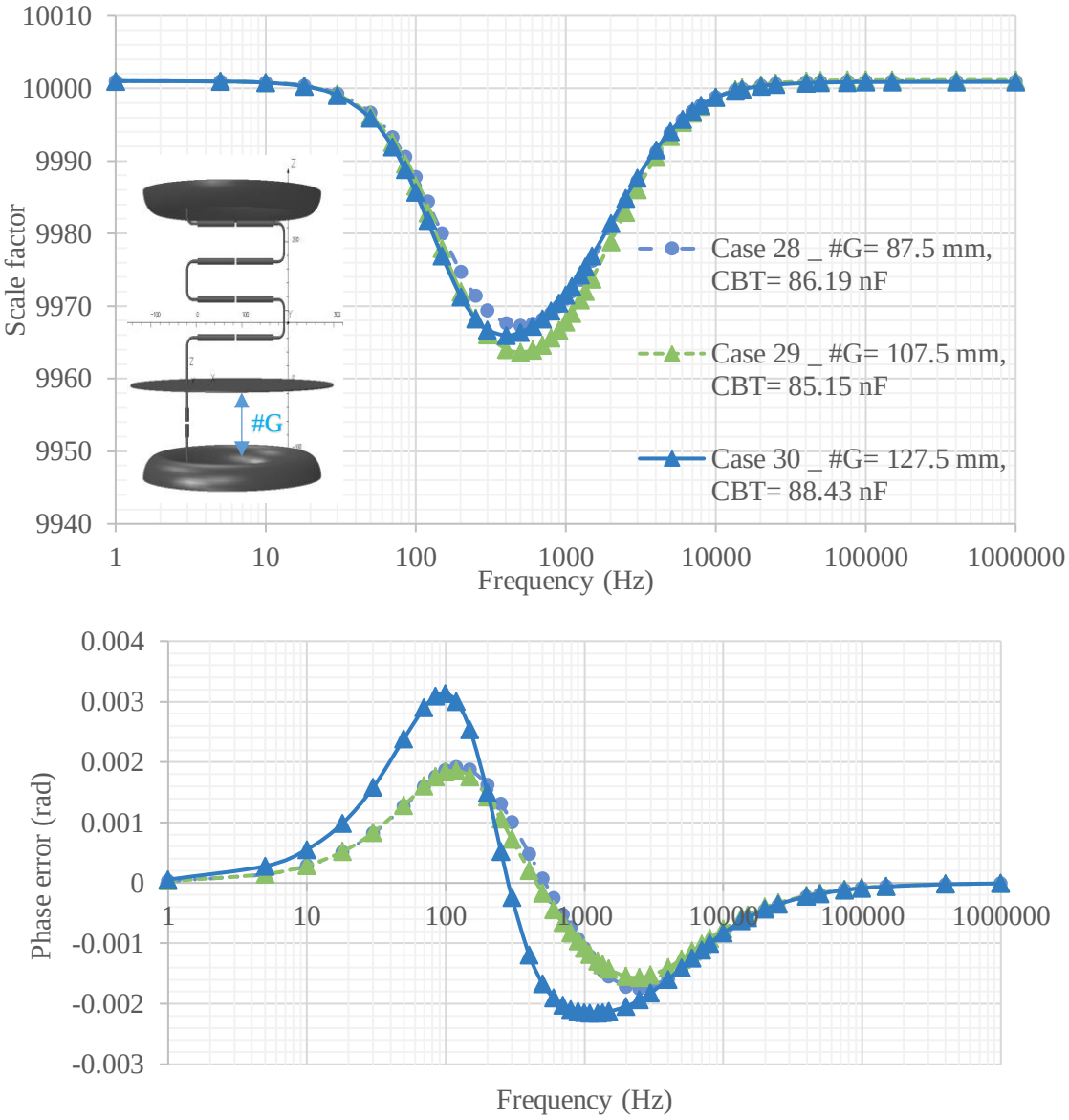


Fig. 3.33. Effect of the variable “#G” while “dis1”= 81 mm and “dis2”= 60 mm

In cases 31, 32, 33.1, and 34, parameters; “dis1 and dis2 are kept to 81mm and 70 mm, respectively, while #G is varied. The results are presented in Fig. 3.34, where the maximum deviation of SF from the rated value indicates 0.24% (and maximum phase error of 1.2 mrad) in case 33.1 which is better than that of case 27.

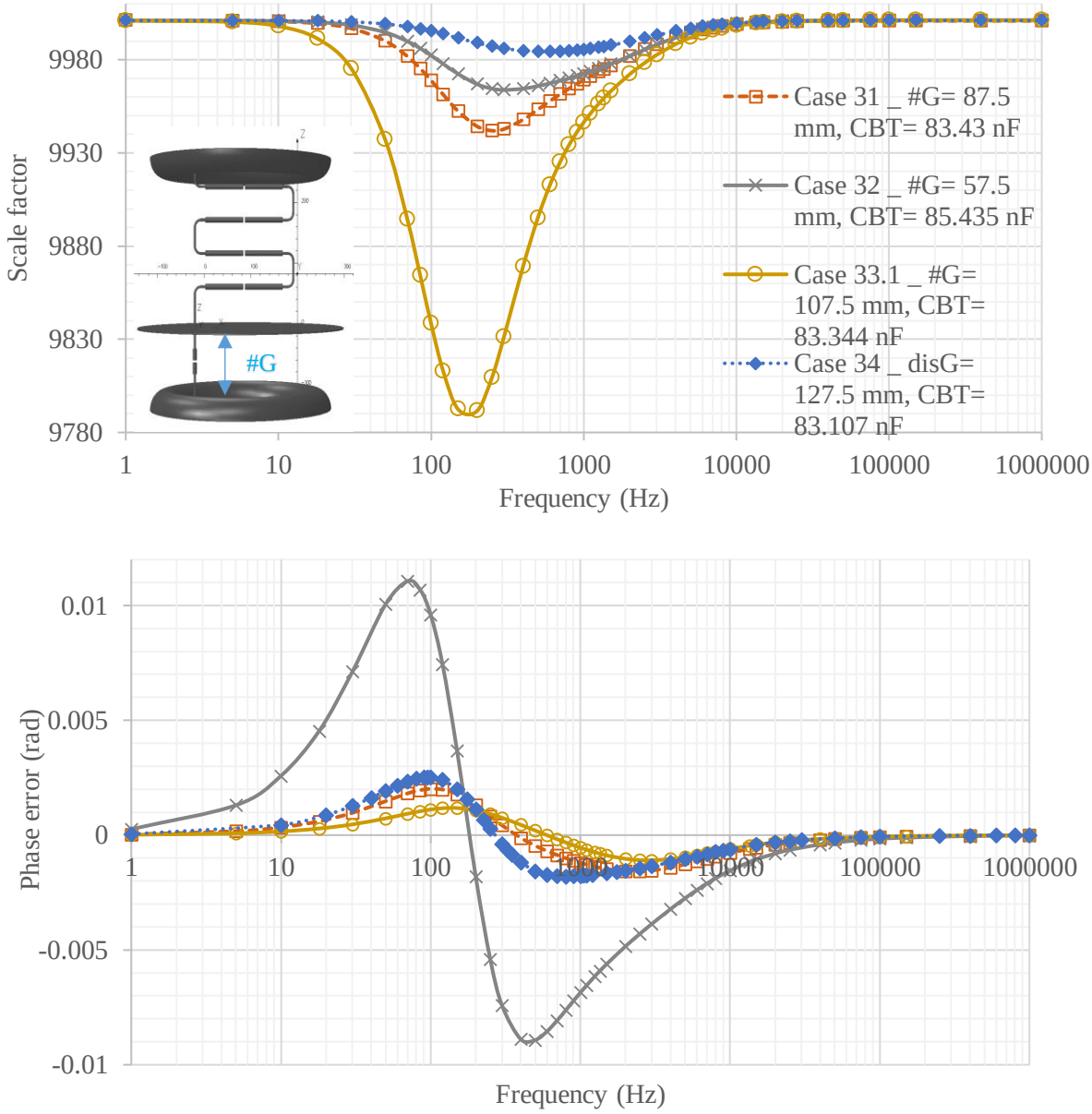


Fig. 3.34. Effect of the variable #G while dis1 and dis2 are 81 mm and 70 mm, respectively

In the cases 33.2, 33.3, and 33.4, dis2 and #G are kept to 70 mm and 107.5 mm as in the case 33.1, while the parameter dis1 is varied. The results are shown in Fig. 3.35.

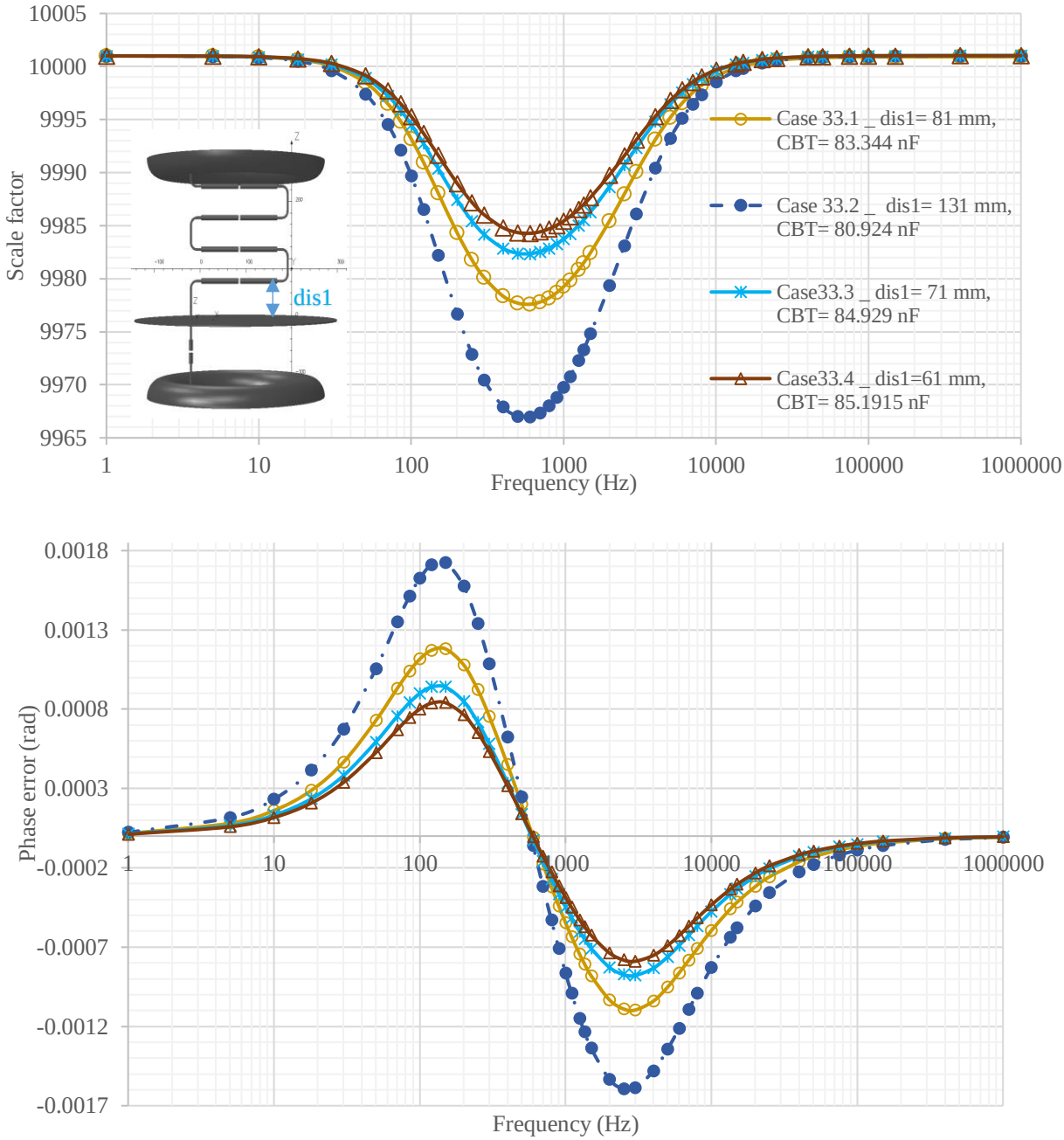


Fig. 3.35. Effect of the variable “dis1” while “dis2” and “#G” are 70 mm and 107.5 mm respectively

The results in Fig. 3.35 shows that the least value of dis1 gives the best frequency response. The case 33.4 represents the best result among horizontally placed HV resistors up to now.

In cases 35, 36, 37, 38, and 39, dis1 and dis2 are kept to 81mm and 90 mm, respectively, while the parameter #G is varied. The results displayed in Fig. 3.36 shows that the optimum #G is about 117.5 mm (case 38). The case 38 with 81 mm, 90 mm, and 117.5 mm for dis1, dis2, and #G has the best results among horizontally placed HV resistors arrangements analyzed up to here.

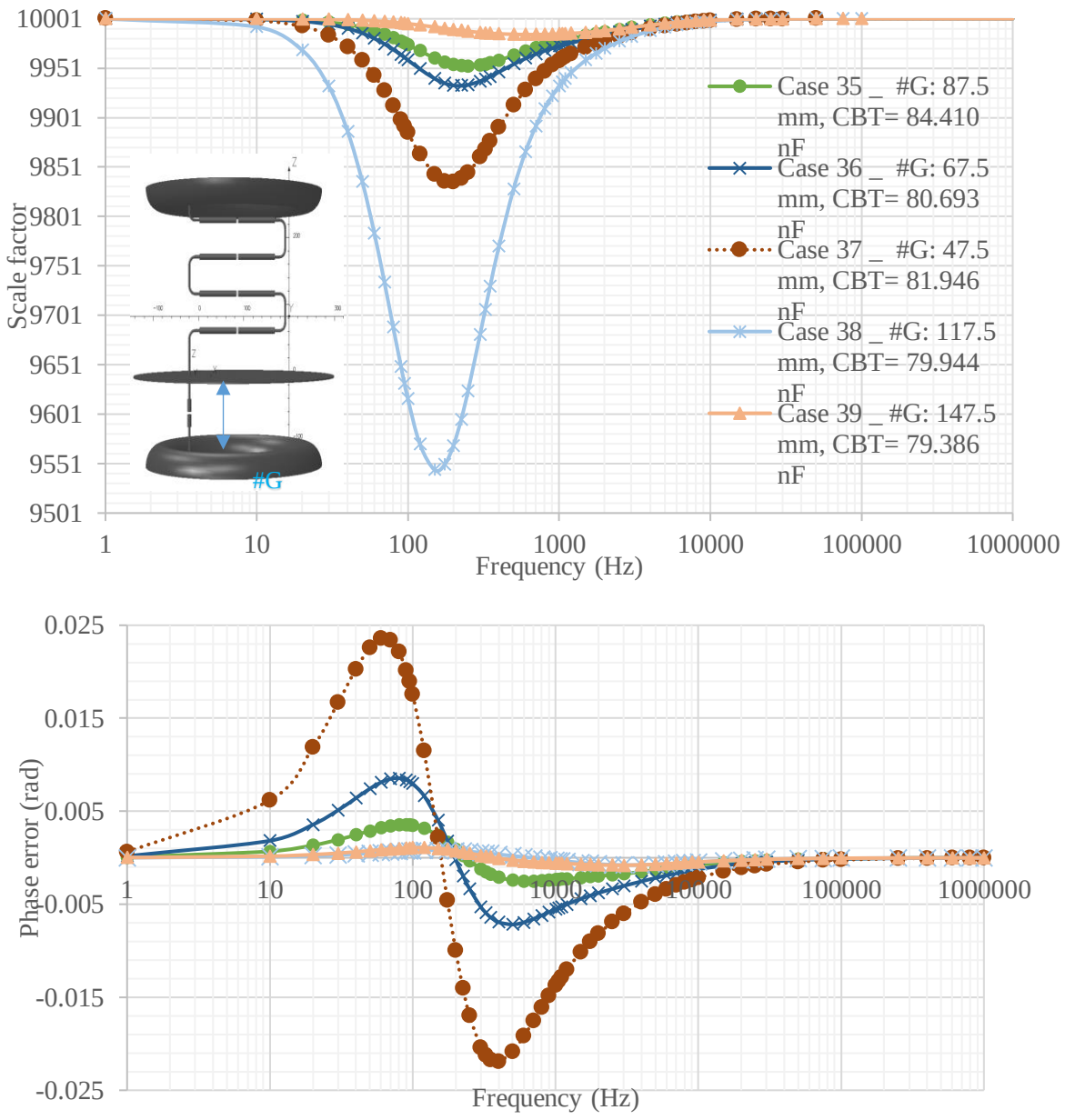


Fig. 3.36. Investigation of optimum “#G” while “dis1” and “dis2” are 81 mm and 90 mm respectively

Also, in cases 40, 41, 42, and 43, dis1 and dis2 are kept to 81mm and 110 mm, respectively, while the #G are varied. Results are presented in Fig. 3.37. The result shows the approximate optimum value of the #G as 147.5 mm (case 40). The case 40 shows the maximum deviation of the SF from rated SF is about 0.15% (and the maximum phase error is around 1.1 mrad) better than that of the case 38. However, it still needs to be improved in order to satisfy the requirement for a reference tool.

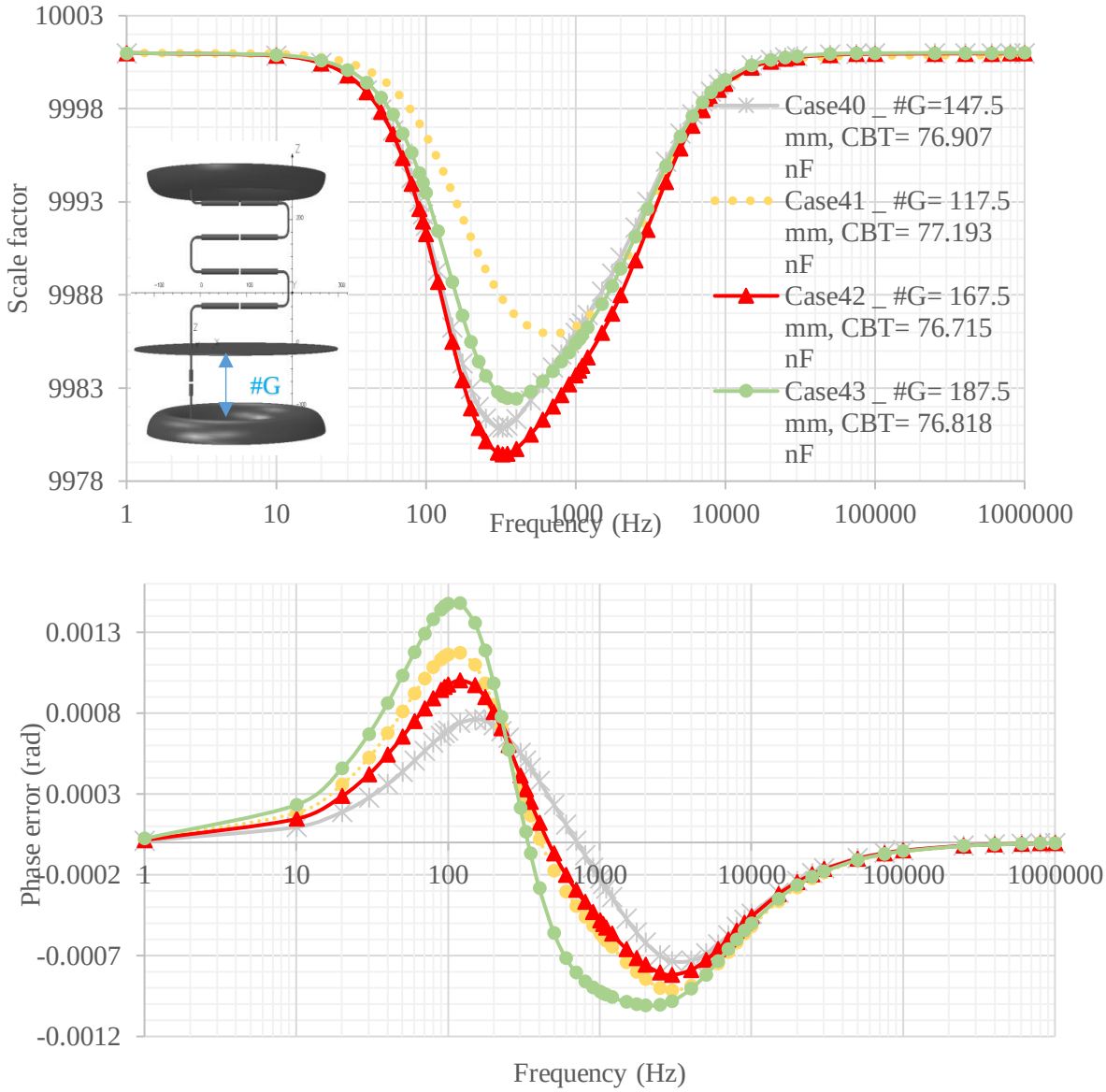


Fig. 3.37. Investigation the optimum "#G" while "dis1" and "dis2" are 81 mm and 110 mm respectively

In addition, the effect of the radius of LV-connected plate (here named "#Pr") is investigated on the frequency behavior of the VD. To do this, the cases 44, 44.2, 44.3, 44.4, 44.5, with different #Pr values are simulated. The results are shown in Fig. 3.38.

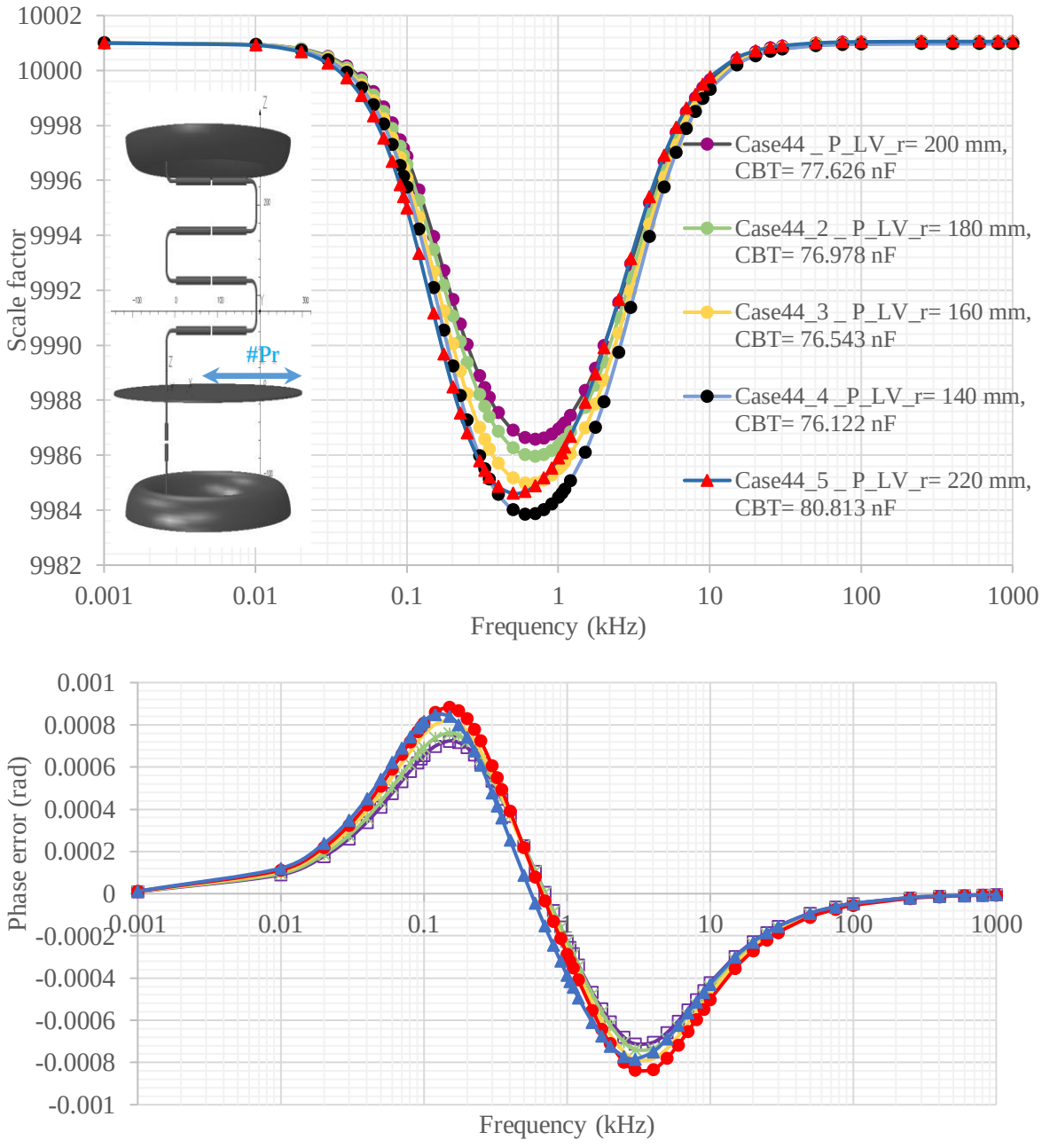


Fig. 3.38. The effect of the parameter "#Pr" on the frequency behavior of the VD

As can be seen, there is an optimum value for the parameter "#Pr" (case 44).

Furthermore, in cases 40, 44, and 45 parameters dis2 and #G are kept 110 mm and 147.5 mm, respectively while the parameter dis1 is varied. Results are presented in Fig. 3.39. The result shows the least the "dis1" the better the frequency behavior of the VD.

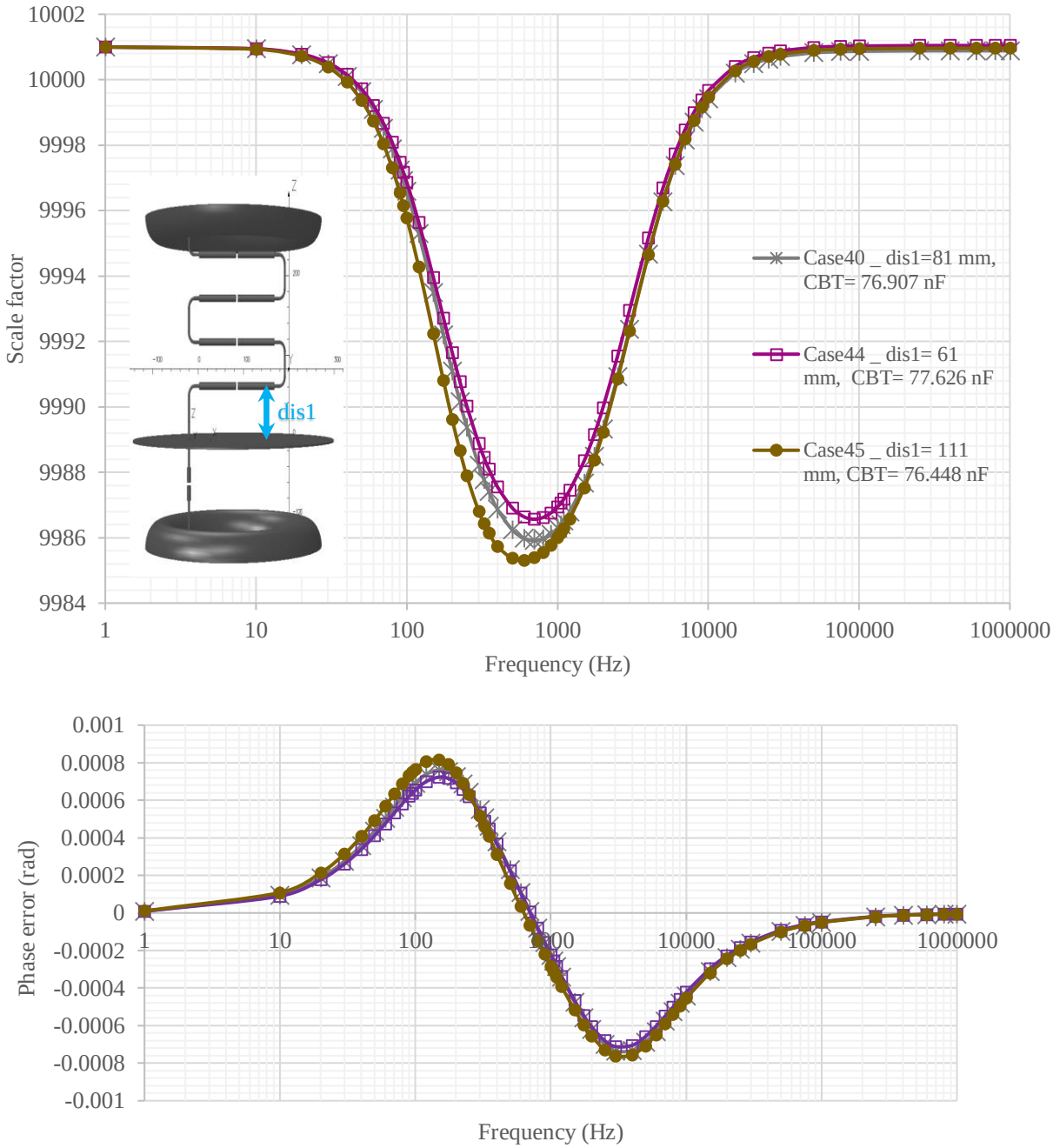


Fig. 3.39. The effect of parameter "dis1" on frequency behavior of the VD other parameters are constant

In addition, in cases 46, 47, 48, 49, and 50, parameters dis1 and dis2 are held constant as 61 mm, and 130 mm, respectively and parameter #G is changed. Fig. 3.40 presents the results of cases 46 up to 50. As could be seen, increasing the parameter dis2 increases the value of the optimum #G will. However, it still cannot offer a SF deviation less than 0.05% and a phase error less than 0.5 mrad.

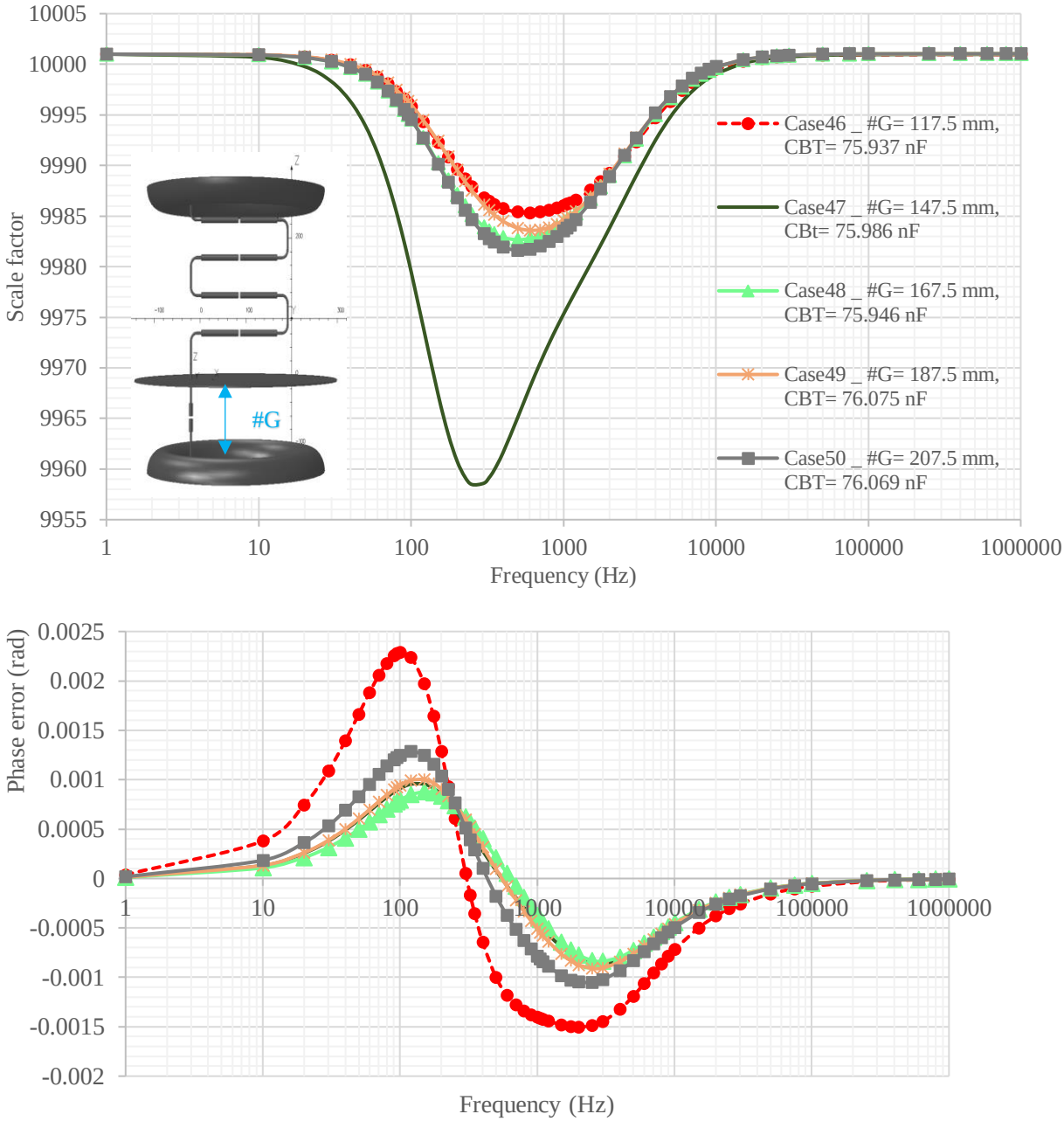


Fig. 3.40. The effect of the parameter "#G" on frequency behavior of the VD

Table 3.4 summarizes the value of parameters in all simulated cases of horizontally designed VD. The case 44 provides the best results among the RVD with horizontally placed resistors. The maximum SF deviation is about 0.144% and maximum phase error is around 0.724 mard. These results are not satisfactory for a reference voltage transducer. The best result among designed HV dividers has been provided by the vertically placed HV resistors (case 21.1) up to here, whose maximum SF deviation from the rated SF is about 0.11% with maximum 0.5 mrad for the phase error. Then the case 21.1 should be studied more in order to improve its result. In next steps, the sensitivity analysis of vertically designed VD will be studied.

Table 3.4 Parameters of horizontal VD design

Parameter / case number	dis1 (mm)	dis2 (mm)	#G (mm)	LV plate radius (mm)	Max SF deviation from the rated SF (%)	phase error (mrad)
22	61	50	117.5	200	0.82	4.35
23	61	50	137.5	200	1.34	6.975
24	61	50	187.5	200	2.6	13.395
25	61	50	87..5	200	0.38	1.938
26	61	50	77.5	200	0.4	2.095
27	61	60	87.5	200	0.33	1.731
28	81	60	87.5	200	0.373	1.916
29	81	60	107.5	200	0.35	1.858
30	81	60	127.5	200	0.59	3.131
31	81	70	87.5	200	0.371	2.015
32	81	70	57.5	200	2.095	11.077
33.1	81	70	107.5	200	0.234	1.181
33.2	131	70	107.5	200	0.34	1.726
33.3	71	70	107.5	200	0.186	0.939
33.4	61	70	107.5	200	0.167	0.840
34	81	70	127.5	200	0.482	2.527
35	81	90	87.5	200	0.678	3.563
36	81	90	67.5	200	1.654	8.55
37	81	90	47.5	200	4.568	23.57
38	81	90	117.5	200	0.1599	0.81
39	81	90	147.5	200	0.201	1.08
40	81	110	147.5	200	0.150	0.762
41	81	110	117.5	200	0.215	1.17
42	81	110	167.5	200	0.185	1.00
43	81	110	147.5	200	0.278	1.478
44	61	110	147.5	200	0.144	0.724
44.2	61	110	147.5	180	0.150	0.761

44.3	61	110	147.5	160	0.160	0.822
44.4	61	110	147.5	140	0.171	0.883
44.5	61	110	147.5	220	0.1639	0.850
45	111	110	147.5	200	0.1569	0.817
46	61	130	117.5	200	0.425	2.288
47	61	130	147.5	200	0.183	0.955
48	61	130	167.5	200	0.174	0.878
49	61	130	187.5	200	0.194	1.00
50	61	130	207.5	200	0.241	1.285

3.6 The sensitivity analysis of the Vertical VD design

In the realization, there should be an insulation between the top and bottom plates mechanically supporting the structure of the VD. The case 21.2 shown in Fig. 3.41 is similar to the case 21.1, but uses an insulating support (with the relative permittivity of 4) between the plates.

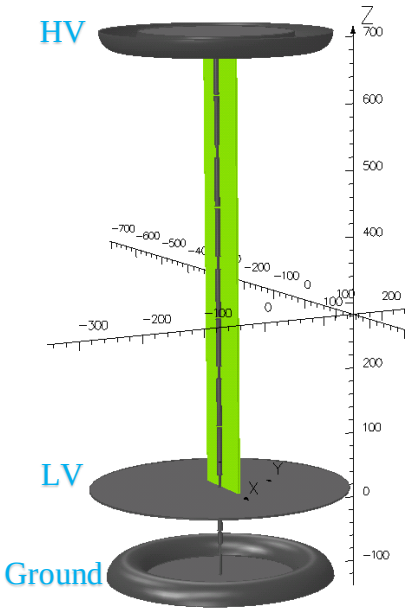


Fig. 3.41. The structure of the case 21.2 with the support (the green part)

The results of the case 21.2 compared to the case 21.1 are shown in Fig. 3.42. As can be seen the result of the case with the insulation support, worsen the frequency behavior as

the insulating part gives a better connection between HV layers for the electric field, making the CHV more and subsequently increasing the discrepancies with respect to rated SF and the phase error.

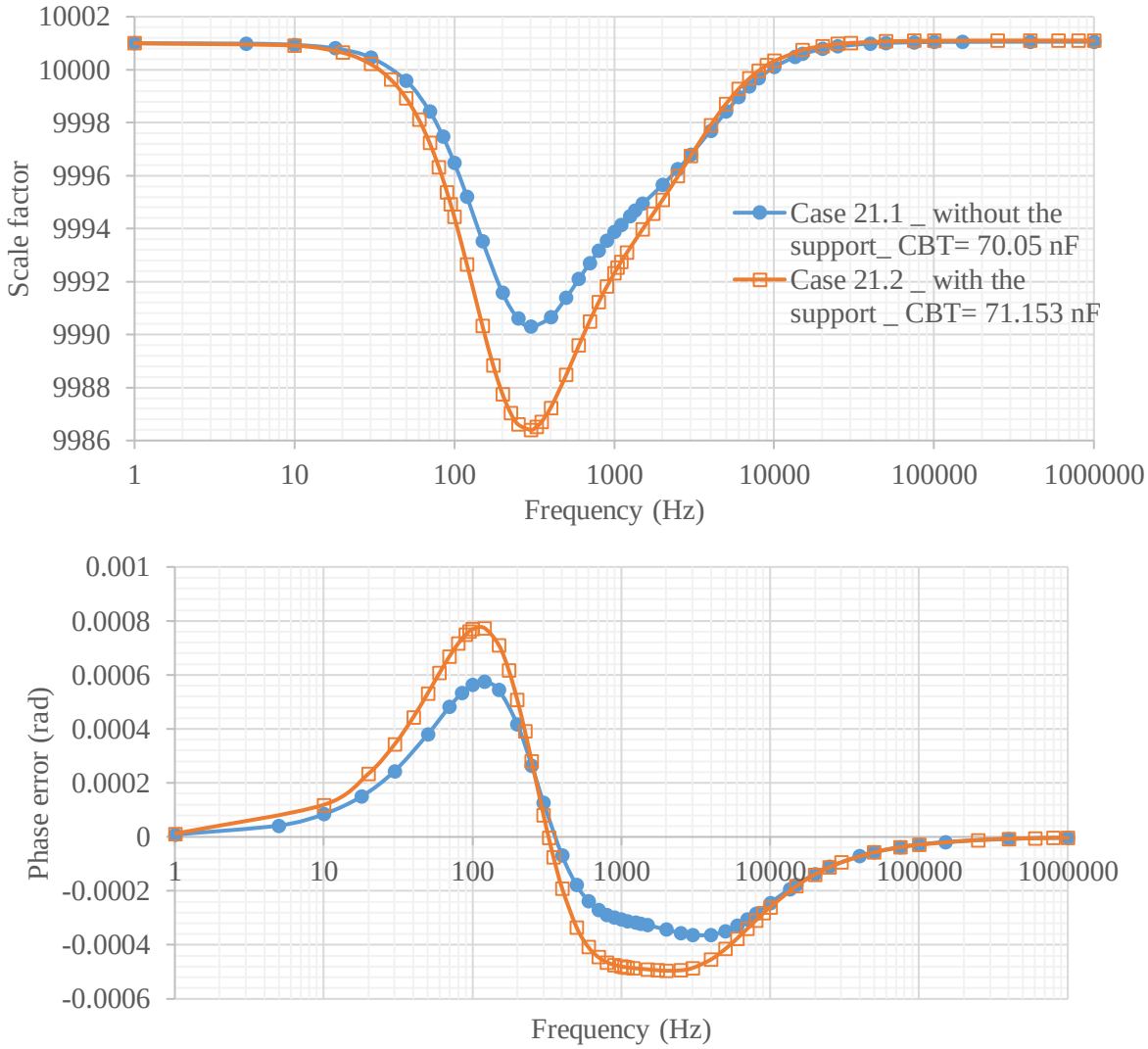


Fig. 3.42. The result of the cases 21.1 and 21.2

Cases 21.2, 21.3, 21.4, and 21.5 are simulated with the presence of the insulation support and with different distances between the LV-connected plate and the ground plate (here called "#G"). The results are shown in Fig. 3.43. As could be seen, the best results are computed with the greatest #G value. In the case 21.5 (#G" = 167.5 mm) the maximum deviation of SF from its rated value is ~0.05% (with a maximum phase error of ~0.27

mrad), which is the first structure among previously designed VDs that can meet the requirements of a reference tool.

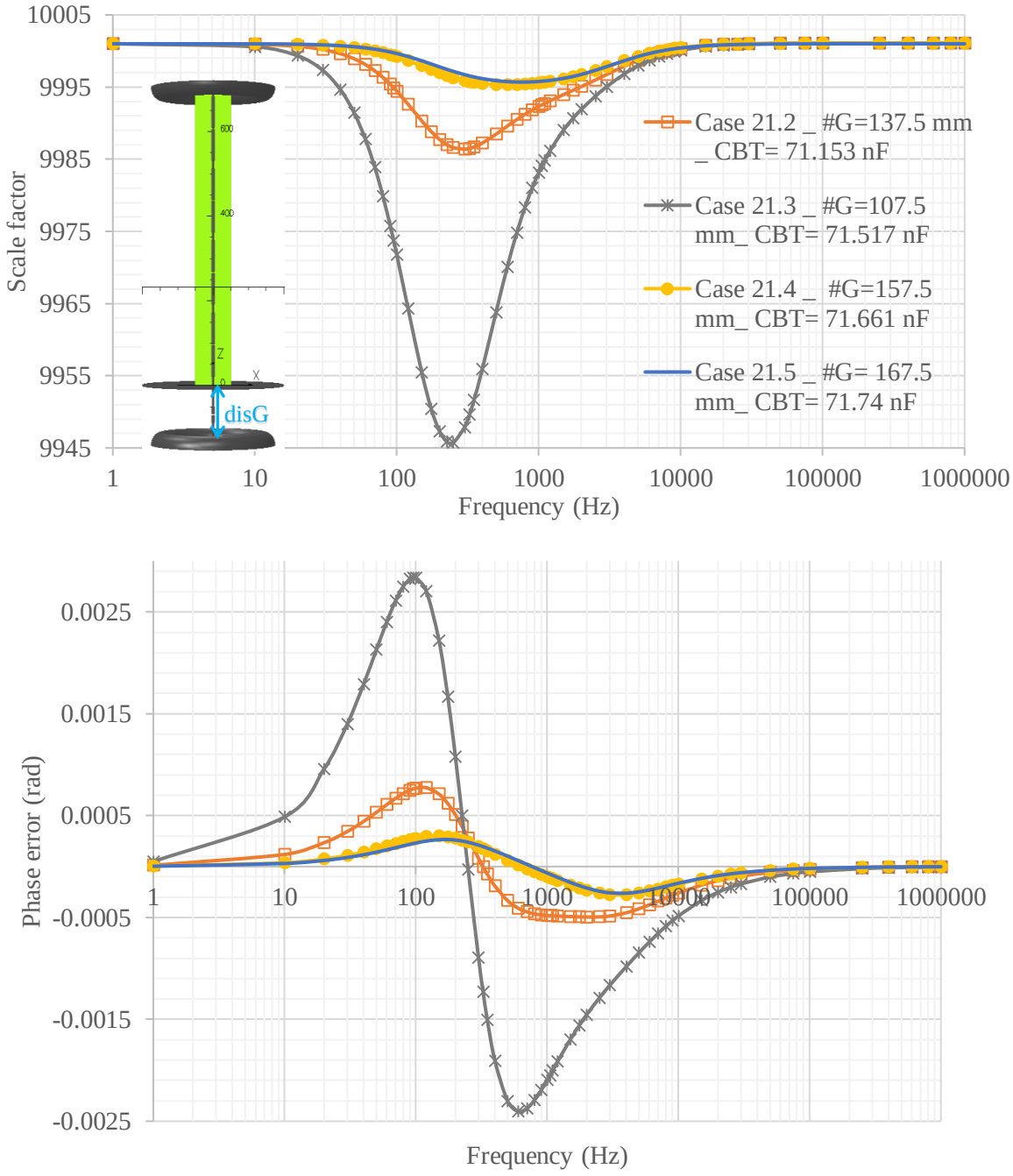


Fig. 3.43. Effect of the parameter "#G" on the vertically placed HV resistors design

In the following sub-sections, the effect of the vertical distance between the LV connected plate and the adjacent HV resistor (here called “dis1”) is investigated. The results of cases 21.5, 21.6, and 21.7 with different “dis1” are shown in Fig. 3.44.

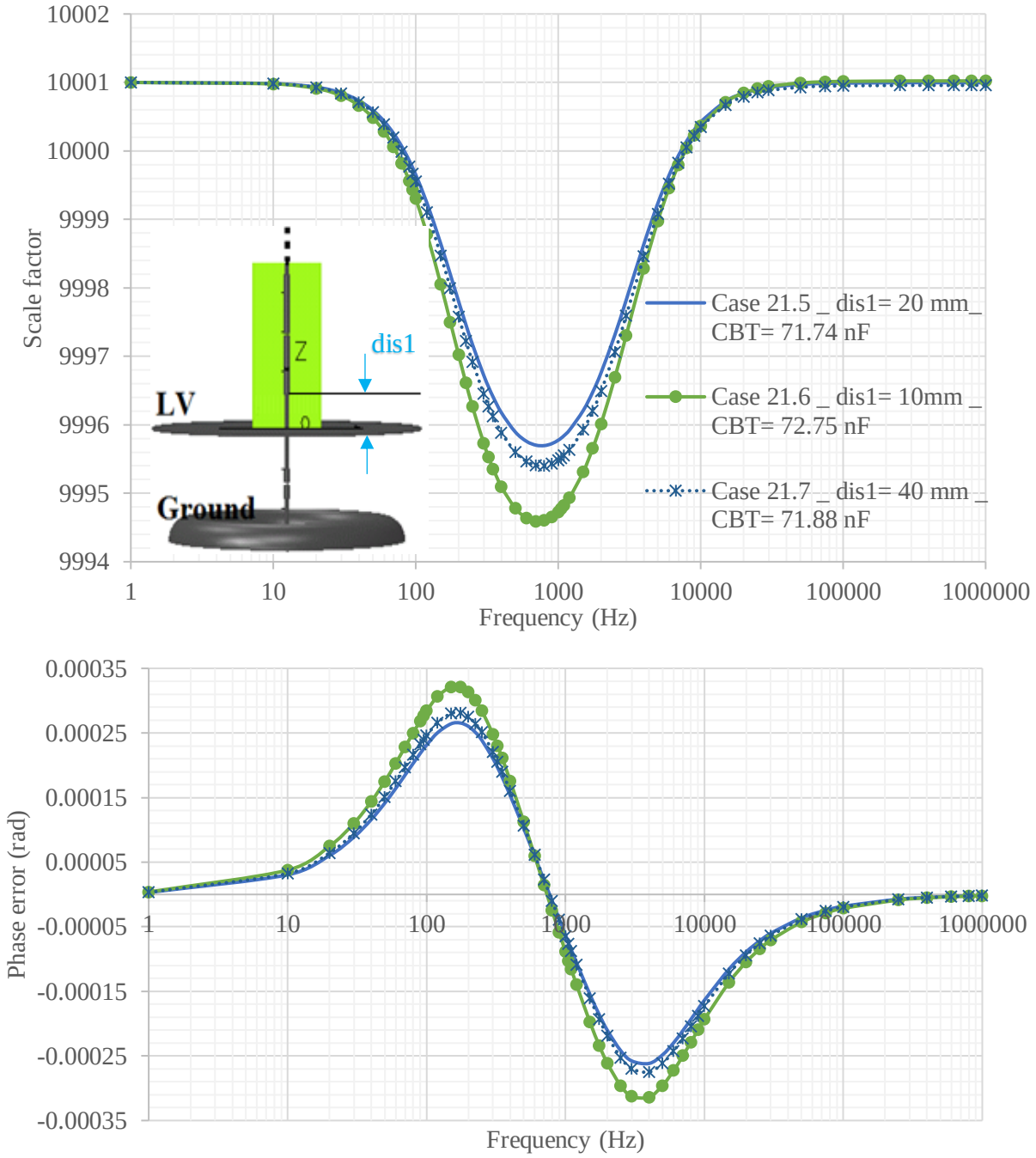


Fig. 3.44. Effect of the vertical distance between the LV connected plate and the adjacent HV resistor

The case 21.8 is similar to the case 21.7 with difference in the value of the vertical distance between the HV resistors (here called “dis2”). The results depicted in Fig. 3.44 and Fig. 3.45 does not show much difference for the change of “dis1” and “dis2”. The case 21.5 should be chosen for its greater improvement being slightly better than the case 21.7. However, this latter should be chosen since its frequency behavior is approximately as good as case 21.5 but it could be easily retrieved to case 21.5 afterwards (in the realization stage) by reducing the height of the insulating support and the parameter “dis1”.

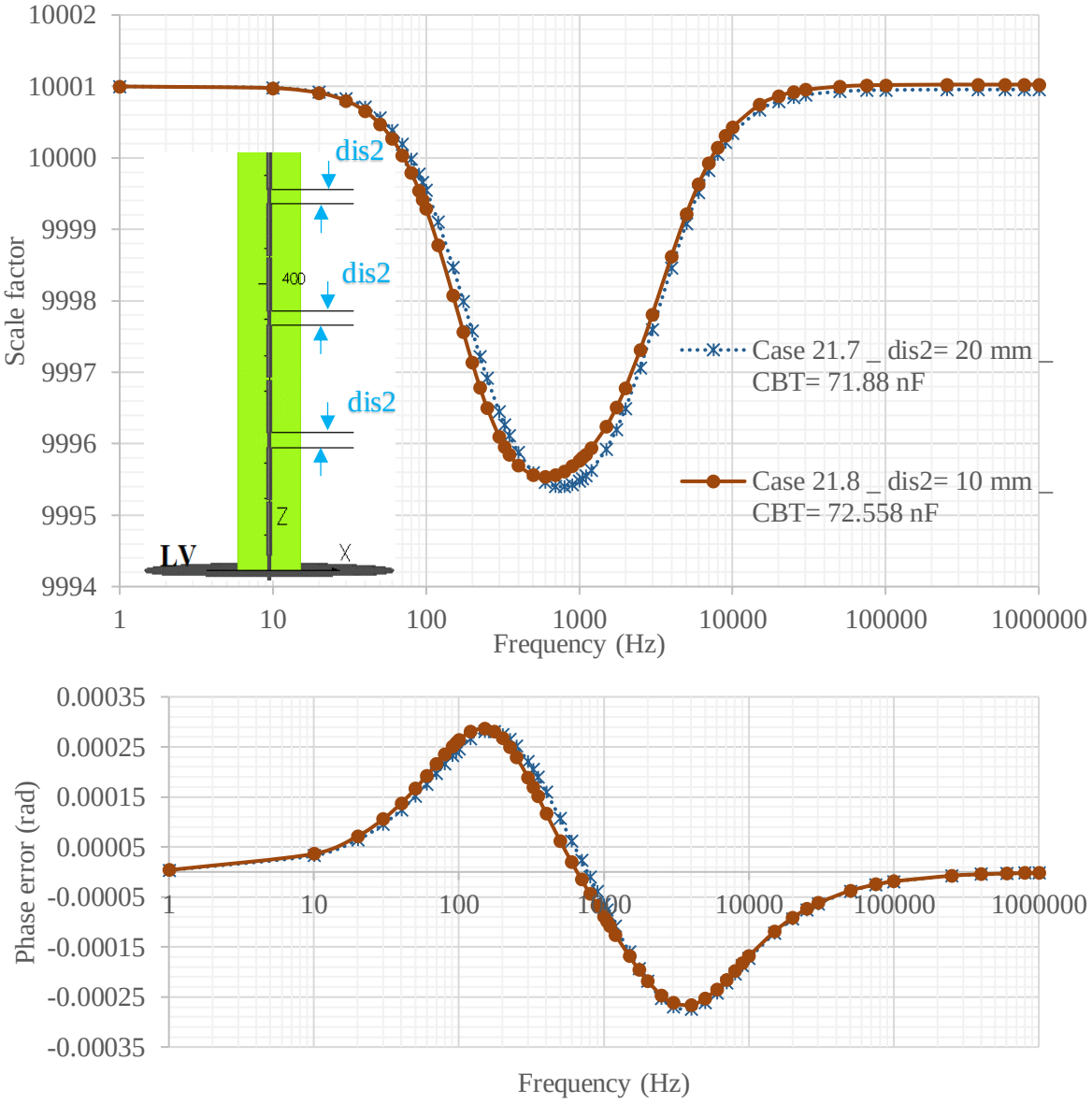


Fig. 3.45. The effect of parameter “dis2” on frequency behavior of the VD

In next designs, we analyze some modifications in the shape or structure of the insulation support in order to modify the electrical field and consequently reduce the stray capacitances of the VD. There are two air slots at the top and bottom of the support in case 21.9 (shown in Fig. 3.46) and five air slots in the case 21.10 (shown in Fig. 3.47) to decrease the electric field flowing through the insulation support and decrease the CHV (in order to increase the SF and decrease the phase error). In the case 21.11 (presented in Fig. 3.48) there is an added insulation layer parallel to the main one. Moreover, in case 21.12 (shown in Fig. 3.49) there is an insulation plate attached to the top of the LV-connected plate. In case 21.13 (presented in Fig. 3.50) there is a thicker insulation containing three top HV resistors in addition to the support. In case 21.14 (shown in Fig. 3.51) there is a thick insulation layer containing the top HV resistor in addition to the support. The results of cases 21.9, up to 21.14 are shown in Fig. 3.52.

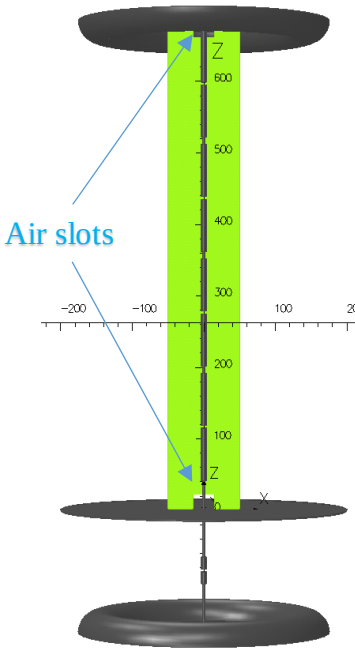


Fig. 3.46. The geometry of the case 21.9 with two air slots in the support

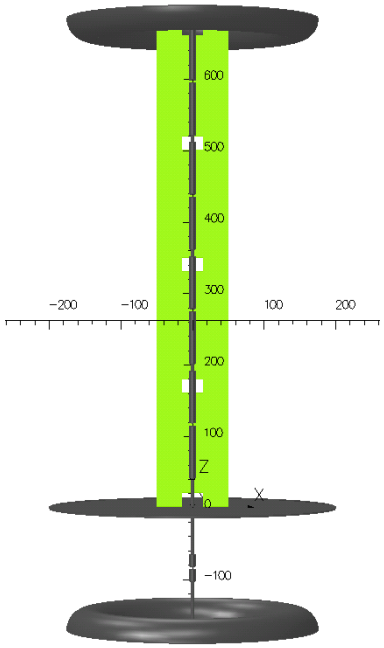


Fig. 3.47. The geometry of the case 21.10 with five air slots in the support

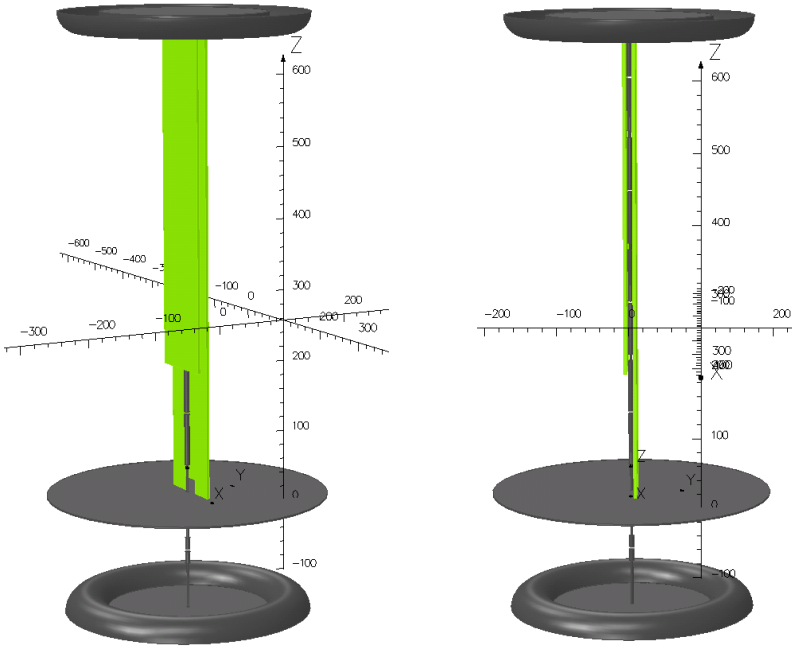


Fig. 3.48. The geometry of the case 21.11 with an added insulation parallel to the main support

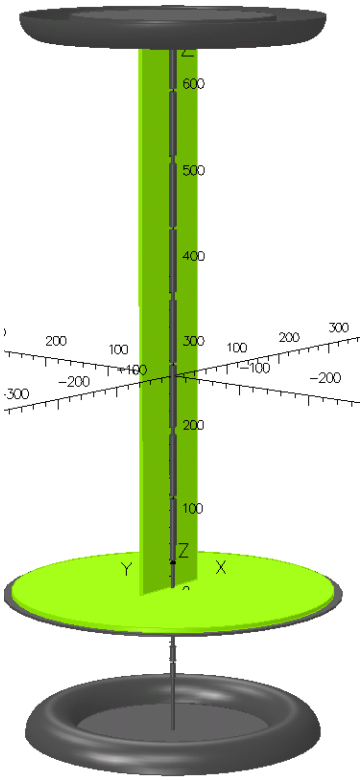


Fig. 3.49. The Geometry of the case 21.12

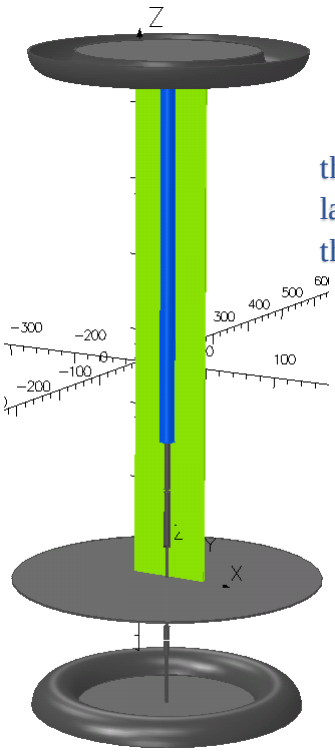


Fig. 3.50. The Geometry of the case 21.13

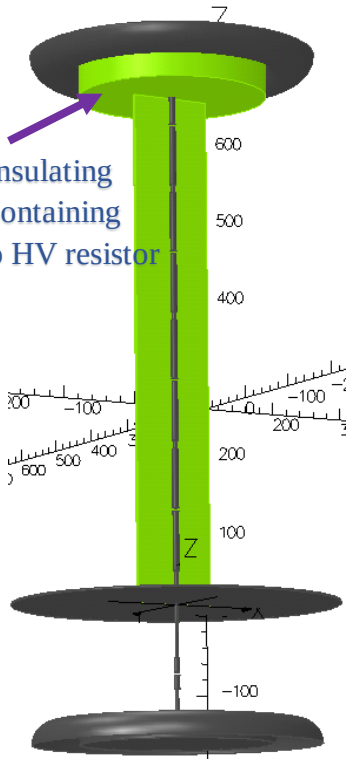


Fig. 3.51. The Geometry of the case 21.14

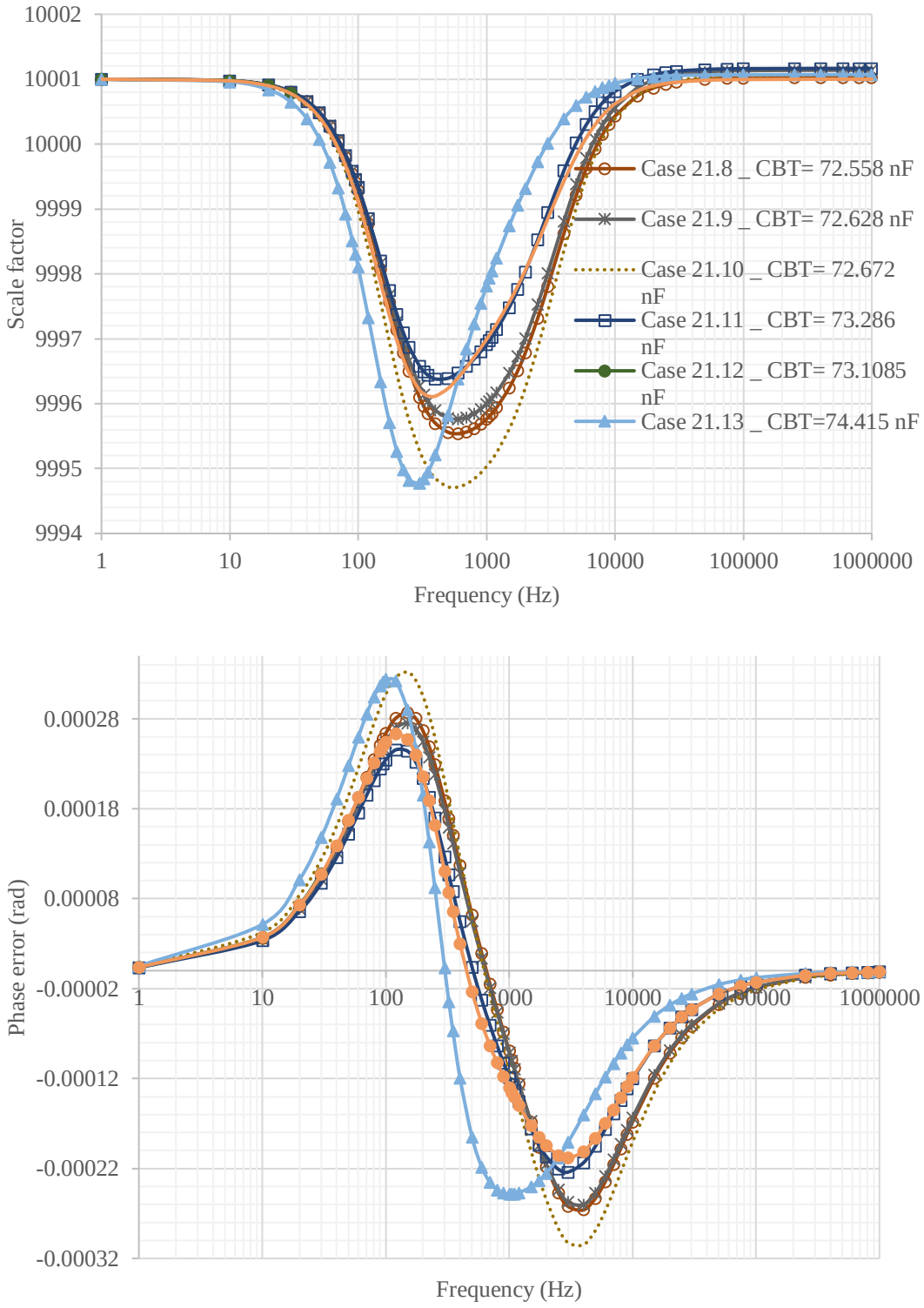


Fig. 3.52. The results of cases 21.8 up to 21.14

As can be noticed by comparison of all results presented in figures from Fig. 3.26 up to Fig. 3.52, the case 21.11 seems to be the geometry with the best frequency behavior among the simulated vertical RVDs. However, the case 21.8 is easier to be realized and its result is just slightly different. Then, in the next step the case 21.8 will be implemented. If it could provide the expected results the case 21.11 could be built afterwards.

Table 3.5 shows the value of parameters in all simulated cases of vertically designed RVD.

Table 3.5. Parameters of vertical VD design

Parameter / Case number	dis1 (mm)	dis2 (mm)	#G (mm)	"#Pr" (mm)	max SF deviation from the rated SF (%)	phase error (mrad)
21.1	20	20	137.5	200	0.107	0.576
21.2	20	20	137.5	200	0.146	0.774
21.3	20	20	107.5	200	0.553	2.836
21.4	20	20	157.5	200	0.0568	0.299
21.5	20	20	167.5	200	0.0531	0.265
21.6	10	20	167.5	200	0.0641	0.321
21.7	40	20	167.5	200	0.056	0.281
21.8	40	10	167.5	200	0.0546	0.287
21.9	40	10	167.5	200	0.0523	0.275
21.10	40	10	167.5	200	0.0628	0.332
21.11	40	10	167.5	200	0.0463	0.245
21.12	40	10	167.5	200	0.0534	0.283
21.13	40	10	167.5	200	0.0623	0.323
21.14	40	10	167.5	200	0.0488	0.263

A procedure using a digital filter parallel to the output voltage for improving the frequency behavior of the VD has been developed at INRIM presented in [24]. The same procedure is used for the case 21.5 to improve the result. A second order filter is designed and added to the output of the VD. The final result of the case 21.5 after using the digital filter and its comparison with that of the case 21.5 before using digital filter is shown in Fig. 3.53. As evident, the frequency behavior of the VD is highly improved by using

digital filter. The maximum deviation of the SF from the rated one is about 0.02% and the maximum phase error is less than 0.15 mrad after using digital filter in case of 21.5.

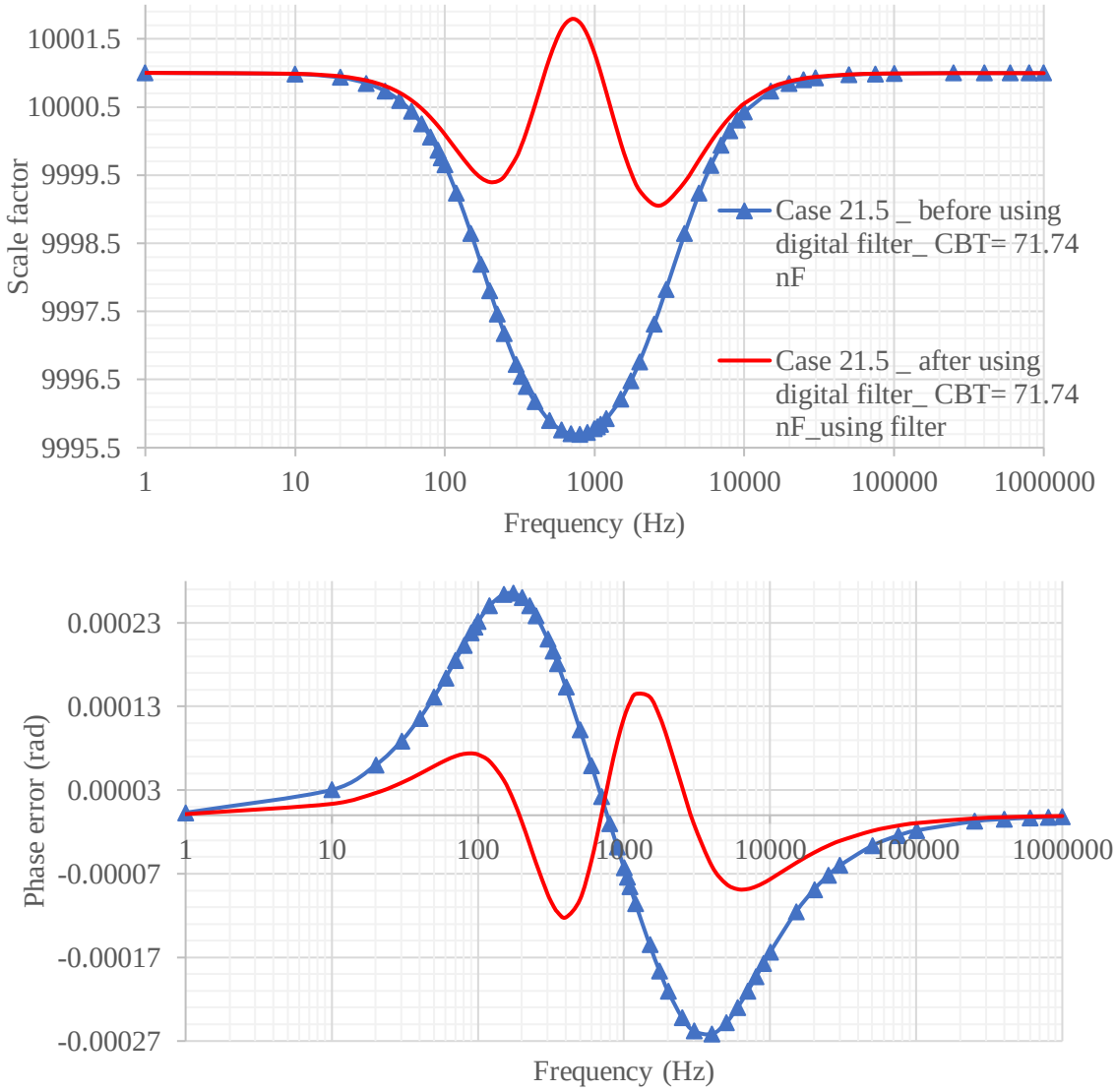


Fig. 3.53. The result of the case 21.5 with and without using digital filter

3.6.1 Realization of the vertical RVD

The case 21.8 is realized with four HV resistors as discussed before. The implemented vertical RVD is shown in Fig. 3.54. The LV section is created on the LV breadboard in order to easily change and achieve the best CBT.

Fig. 3.54. Real case of vertical RVD

Due to some constraints (like the minimum distance between the copper tube and the HV resistors), the actual vertical RVD has been changed with respect to the simulated one adopted during the implementation procedure. These changes are also applied to the simulation as the case 21.8.2 shown in Fig. 3.55. The simulation and measurement results of vertical RVD are drawn in Fig. 3.56.

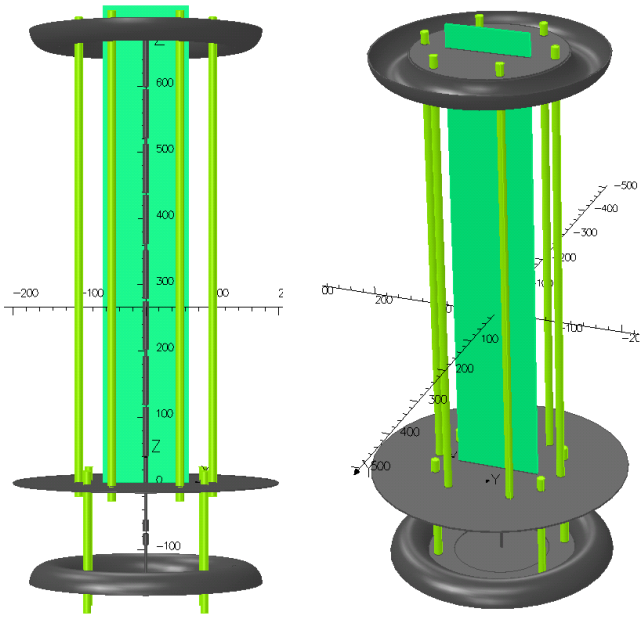


Fig. 3.55. Simulation case 21.8.2 (by correcting the geometry of the case 21.8)

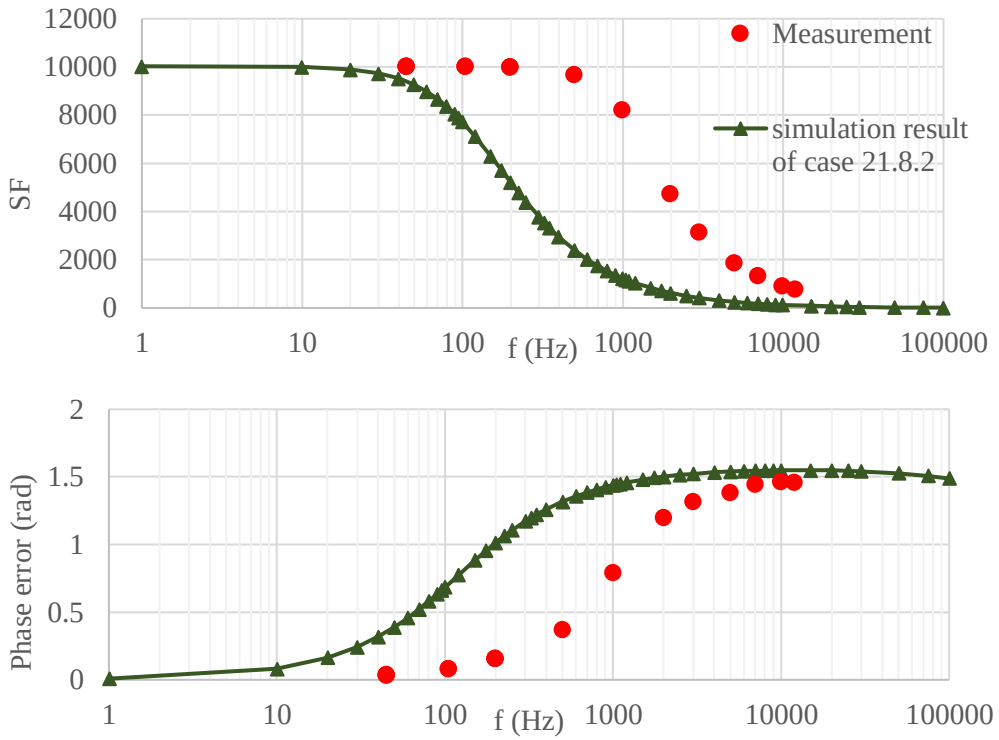


Fig. 3.56. Frequency behavior of the simulation of case 21.8.2 and the measurement of the realized vertical RVD

As can be seen in Fig. 3.56, there is no agreement between the simulation and measurement results of the vertical RVD. The main reason could be that the ground effect has been disregarded In order to include this phenomenon, a surface with assigned ground potential is modelled below the vertical RVD. The FEM model of the vertical RVD with the grounded surface (representing the floor) is displayed in Fig. 3.57.

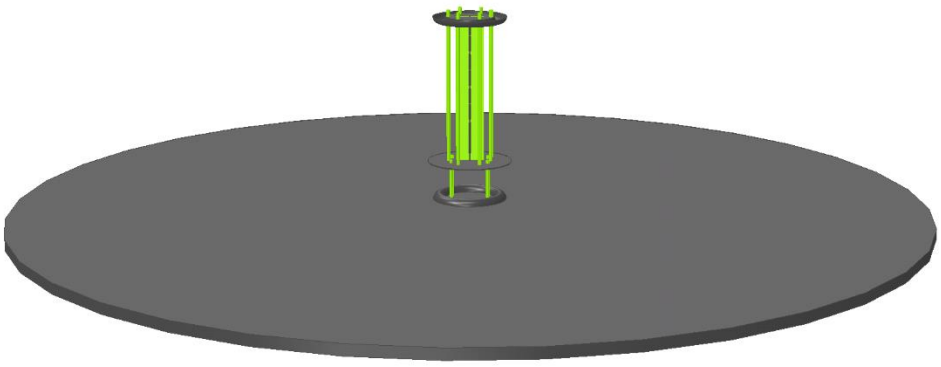


Fig. 3.57. Modeling the effect of ground in Real case 6

The measurement result of the vertical VD compared with its simulation performed considering the ground effect is shown in Fig. 3.58.

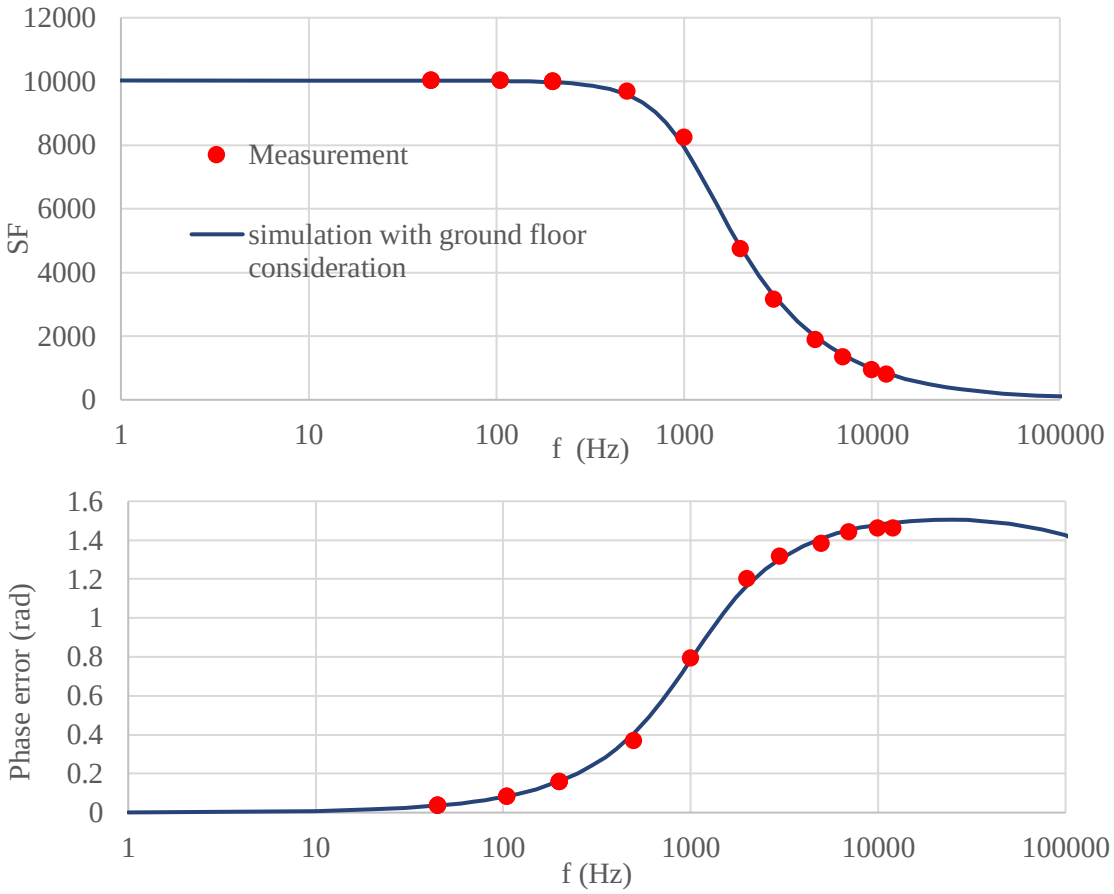


Fig. 3.58. Frequency behavior of the simulation with gournd floor consideraton and the measurement of realized vertical RVD

As can be seen in Fig. 3.58, the good agreement between simulation and measurements evidences that it is mandatory to correctly consider the ground effect in the simulation phase. However, the frequency behavior of the vertical RVD is not acceptable for a standard voltage transducer as the SF deviation from the rated SF is about 61% at 2.5 kHz and the phase error is more than 1.2 rad. To overcome this problem, an extra capacitor (CBT) is added to the output of the RVD. The result of vertical RVD considering the ground effect and compensated with CBT is shown in Fig. 3.59. The best CBT is chosen in order to make the high frequency SF similar to the low frequency one. When considering the ground effect, the results show that the RVD frequency response even with a compensation (CBT) cannot be as good as before considering the ground effect. The reason is that HV part of the vertical RVD is openly (widely) exposed to the ground floor creating higher CGs.

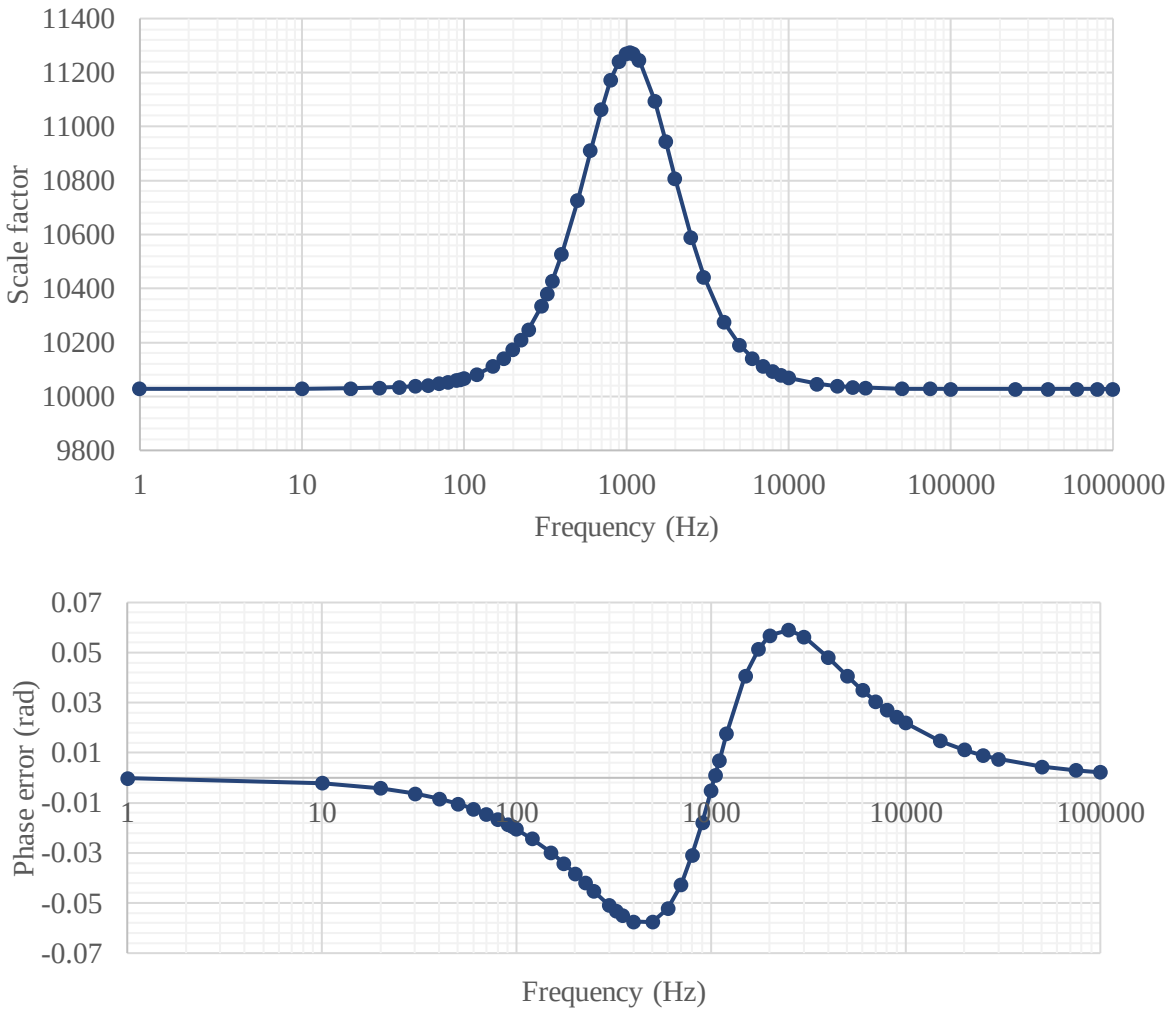


Fig. 3.59. The result of the vertical RVD considering the ground effect with CBT

In the model without ground, there was a specific correlation between parameters #Pr and #G. However, because of physically infinite ground, such a dependence is different and an increase of #G should give better results. Actually, CGs will be reduced by increasing the parameter #G. Then a change of the geometry of the RVD in the HV section (from the middle plate up to the HV top plate) will not affect the CGs. Furthermore, CBT could compensate the CHVs. It is worth to mention that compensation of CGs needs high voltage capacitances not intended at this stage of the project due to the high cost.

This issue is investigated by varying the two parameters #Pr and #G while the other ones are kept constant. The reults are shown in Fig. 3.60, Fig. 3.61, and Fig. 3.62.

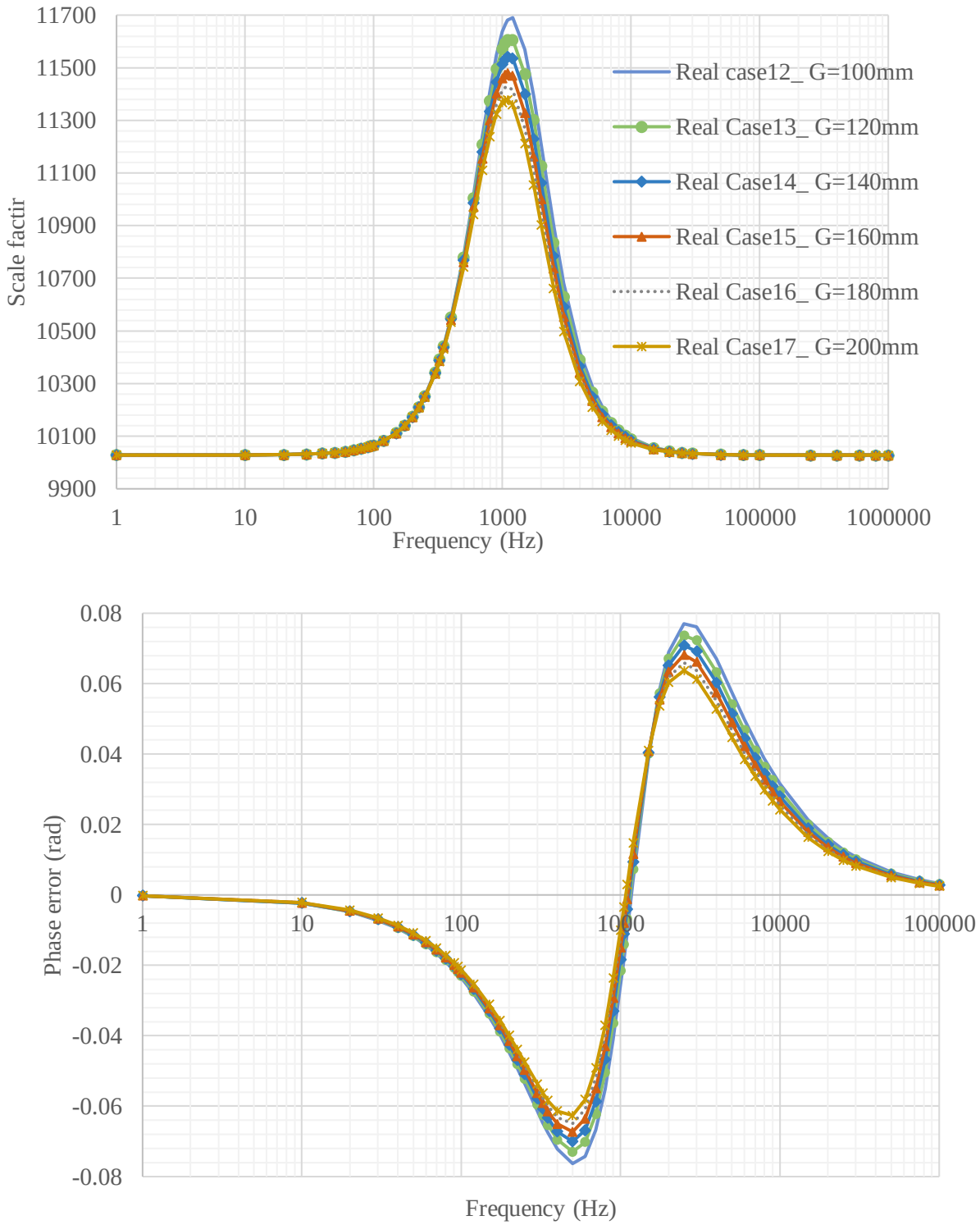


Fig. 3.60. Result of vertical RVD response for different #G values being #Pr=180 mm constant.

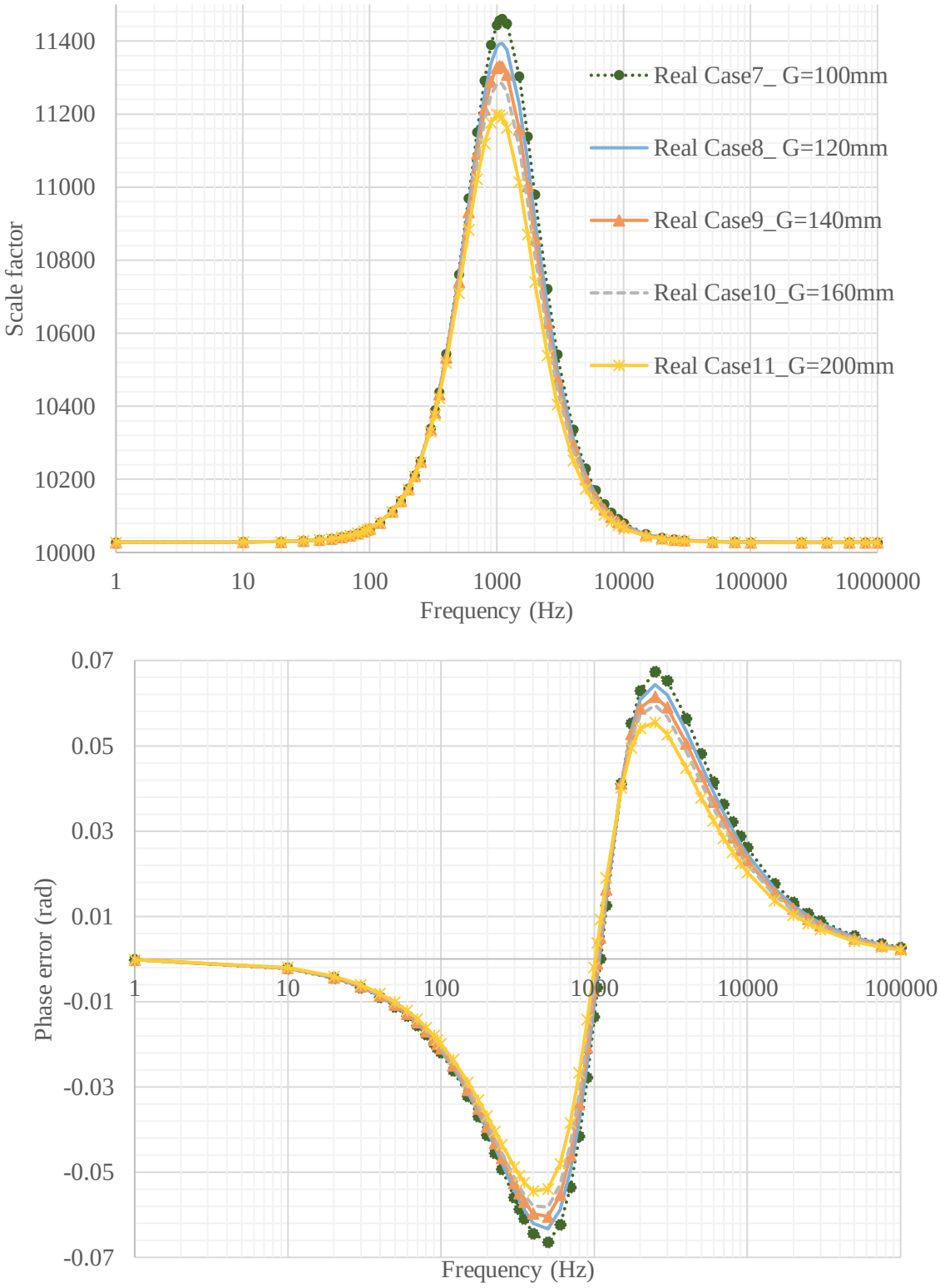


Fig. 3.61. Result of vertical RVD for different #G values when #Pr=200 mm is constant.

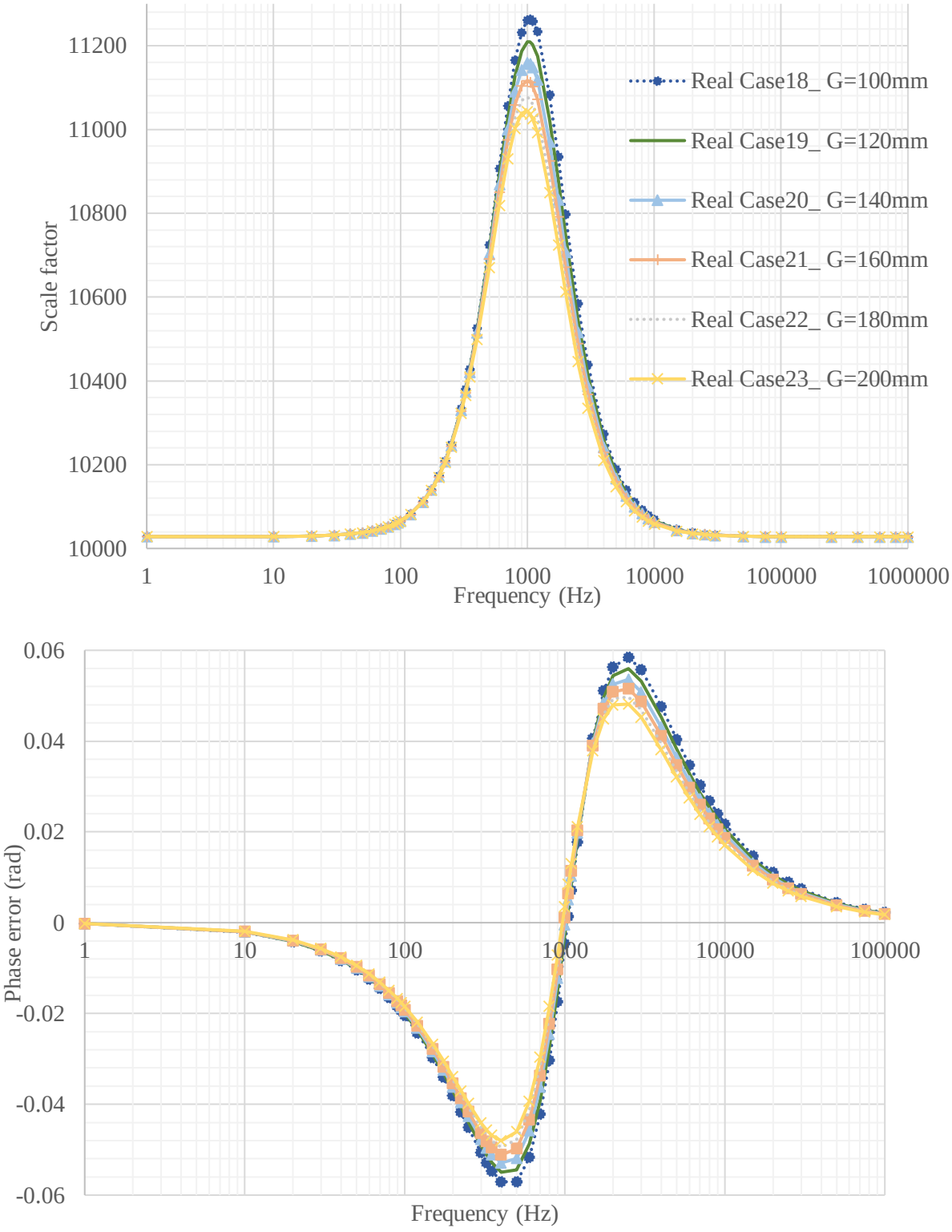


Fig. 3.62. Result of 4R vertical VD for different #G values while #Pr=220 mm is constant.

Furthermore, in order to decrease the CGs, the distance between LV plate and the ground should be increased. When #G is increased, the frequency response of VD could be better. On the other hand, a great value for #G, however, increases the RVD's size. The value of 180 mm is chosen for #G as a compromise.

In addition, another complementary procedure to decrease the CG is the use of a shield. The shield can be added to the LV plate in order to decrease the electric field flowing between the HV section and the ground. On the other hand, if the LV shield is too tall the CHVs increase and CGs dramatically decrease, producing a not proper frequency behavior. Futhermore, the radius of the LV connected shield can change both CHV and CG. Then after choosing the value for the parameter #G, the best value for the LV shield height and radius should be obtained. The Fig. 3.63 shows the simulation model of the vertical VD with the LV-connected shield.

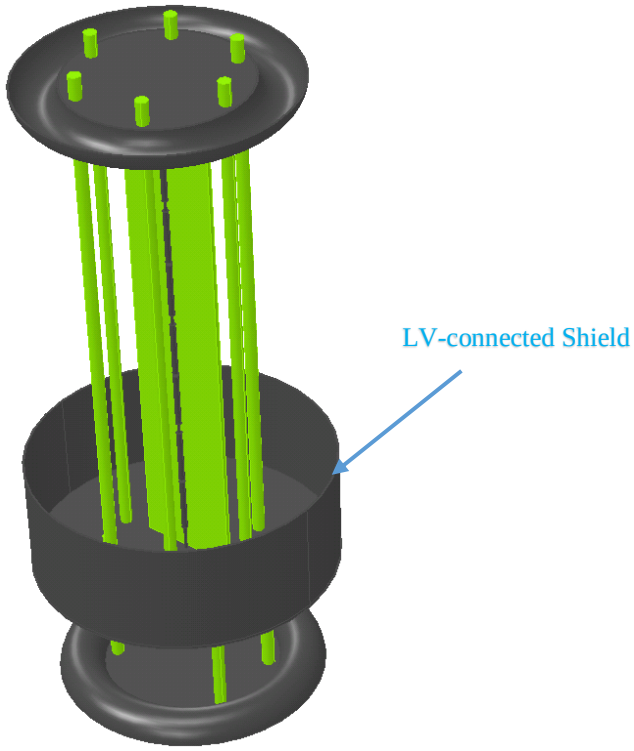


Fig. 3.63. Vertical RVD with LV-connected shield (the ground is not shown here, though considered)

The results of the vertical RVD with CBT and including the ground are shown in Fig. 3.64.

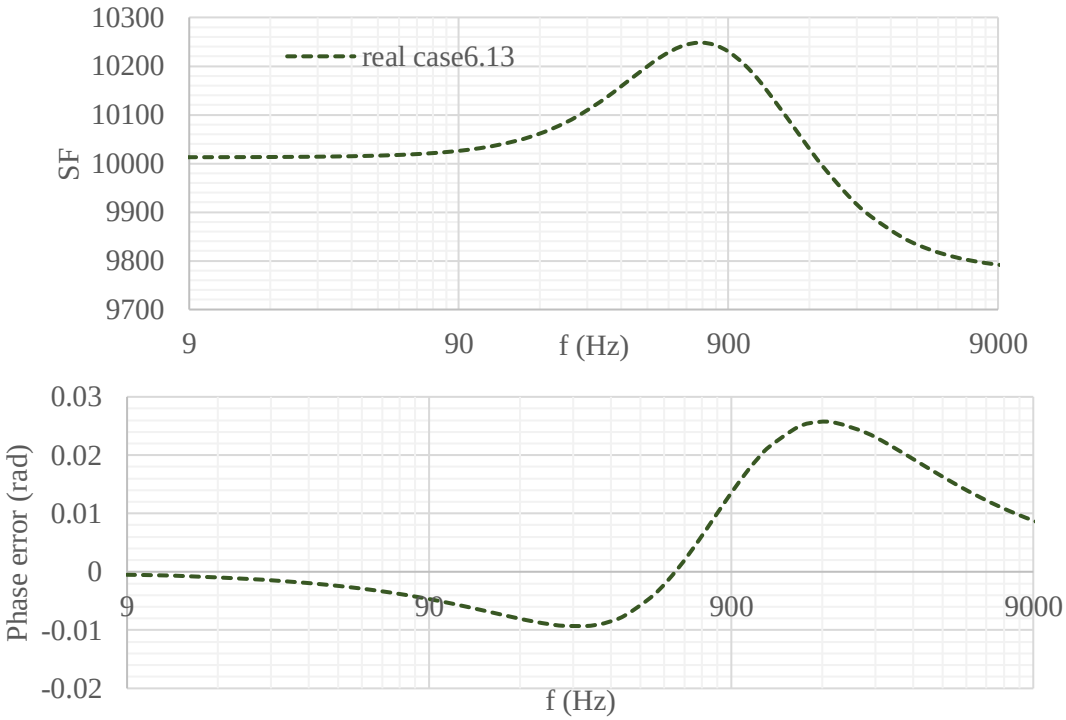


Fig. 3.64. The simulation result of vertical RVD with shield and CBT

The realized case 6.13 is presented in Fig. 3.65. The results of this LV shielded vertical RVD and compensated with CBT are shown in Fig. 3.66. The limits for normal voltage transducer defined by the standards are also shown in Fig. 3.66.

Fig. 3.65. Relization of the case 6.13

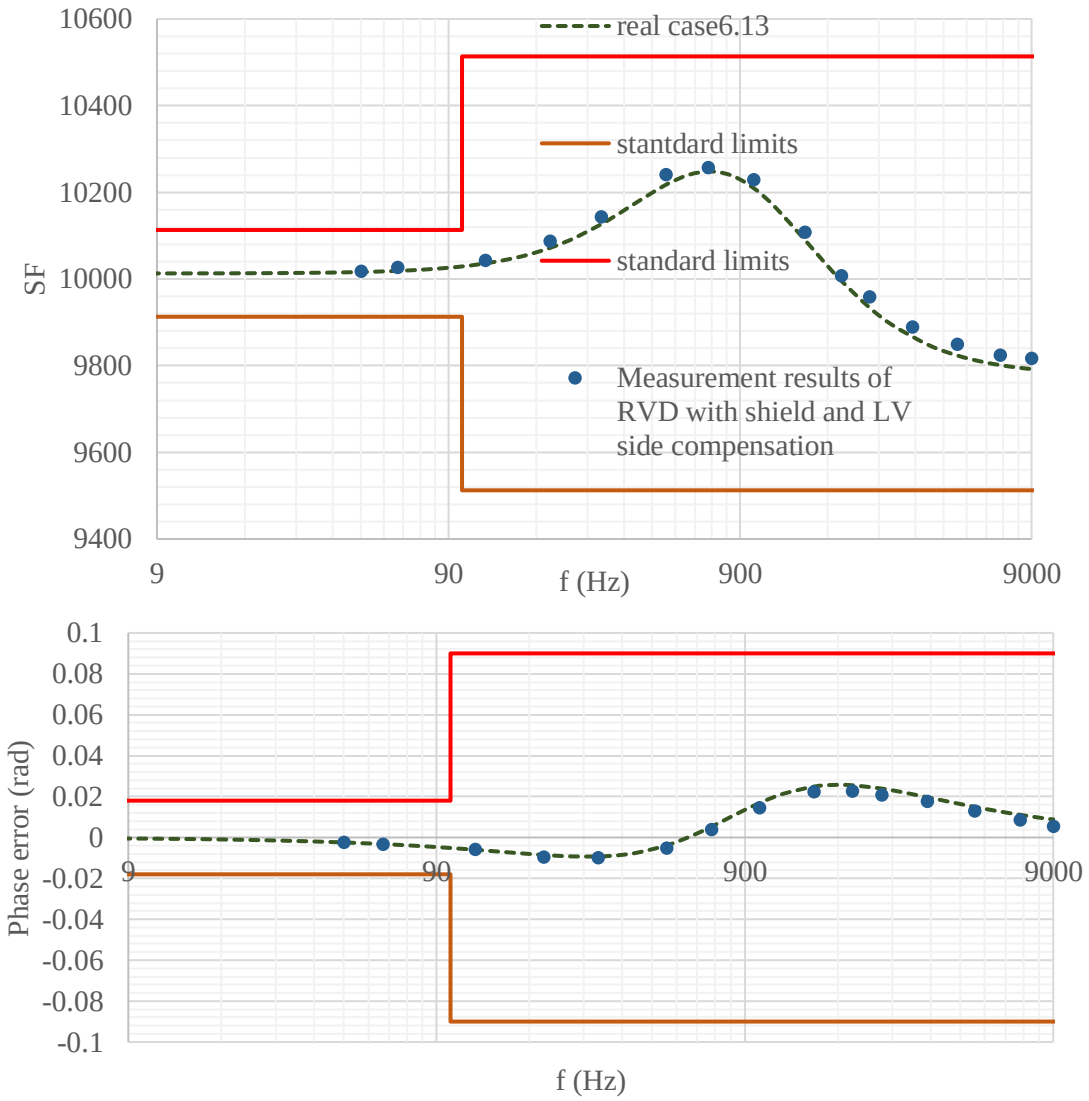


Fig. 3.66. Simulation and measurement results of real case6.13 (4R vertical VD)

The frequency behavior of a reference voltage transducer should be much more accurate than the one (expressed in the standards) required by a normal voltage transducer, although the results shown in Fig. 3.66 are not satisfactory for a reference VD. Therefore, some new configurations of VD should be investigated.

3.7 Horizontal RVD simulations considering the Bus bar and ground floor

The horizontal VD simulations are also repeated with LV shield considering both the ground and a 3m long HV bus bar, which is present in the test laboratory for connecting the HV to the top of VD and it was not considered before.

There could be two different connection between adjacent HV resistors. The first connection could be the shortest possible path as shown in Fig. 3.67 (case H.1) joining the closest HV resistor pins to each other. The second connection is longer as shown in Fig. 3.68 (case H.L.1) joining one HV resistor pin to the opposite pin of the adjacent HV resistor.

The advantage of the first assembly is that the surface of copper tubes used as connection is much lower than the second construction making the overall stray capacitances smaller.

In the second connection, the surface of the copper used in the VD is more than double resulting in overall greater stray capacitances. However, it may result in a better electric field distribution with lower maximum field values, useful to avoid possible corona effect.

In order to investigate the two possible horizontal dispositions discussed above, the two configurations shown in Fig. 3.67 (case H.1) and Fig. 3.68 (case H.L.1) are investigated. The correspondent frequency behaviors are shown in Fig. 3.69.

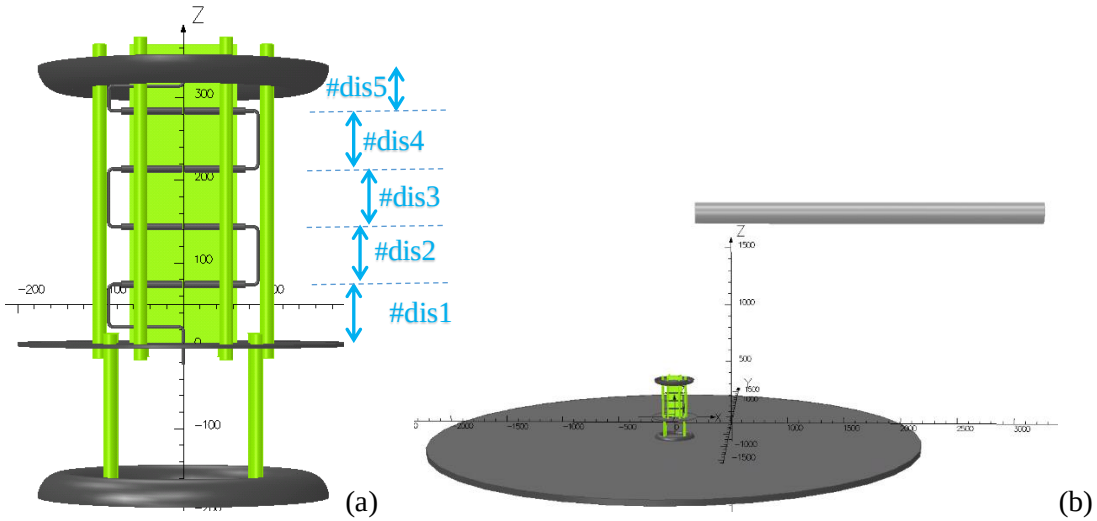


Fig. 3.67. The FEM model of horizontally placed resistors VD with short connections (case H.1) (a) only the VD (b) the ground and HV Bus bar models together with VD

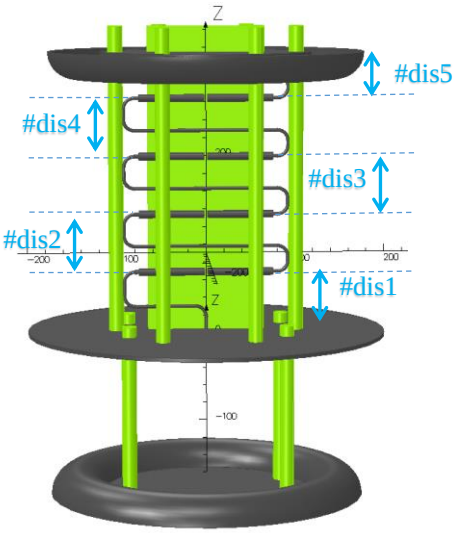


Fig. 3.68. The FEM model of horizontally placed resitors VD with long connections (case H.L.1) (the ground and HV bus bar both are considered, however, not shown here)

The comparison between the two capacitance matrices, the output of FEM simulations, shows that CHVs are higher in case H.L.1 (with longer connection) compared to the case H.1 (with shorter connection). The reason is that in case H.L.1 the HV side has a larger surface that causes higher electric field coupling between HV electrodes (while CGs does increased much). As expected, the result of case H.1 is better than the one of the case H.L.1 because of greater CHVs due to longer copper tubes in the case H.L.1. However the maximum electric field strength of the case H.L.1 is lower than the other case, as shown in Fig. 3.70.

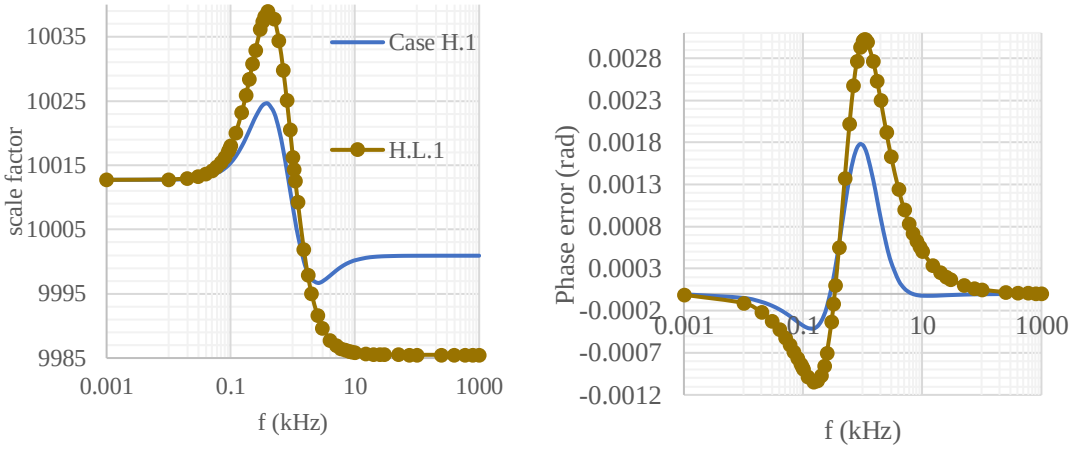


Fig. 3.69. The results of cases H.1 (short connection between HV resistors) and H.L.1 (Long connection between HV resistors)

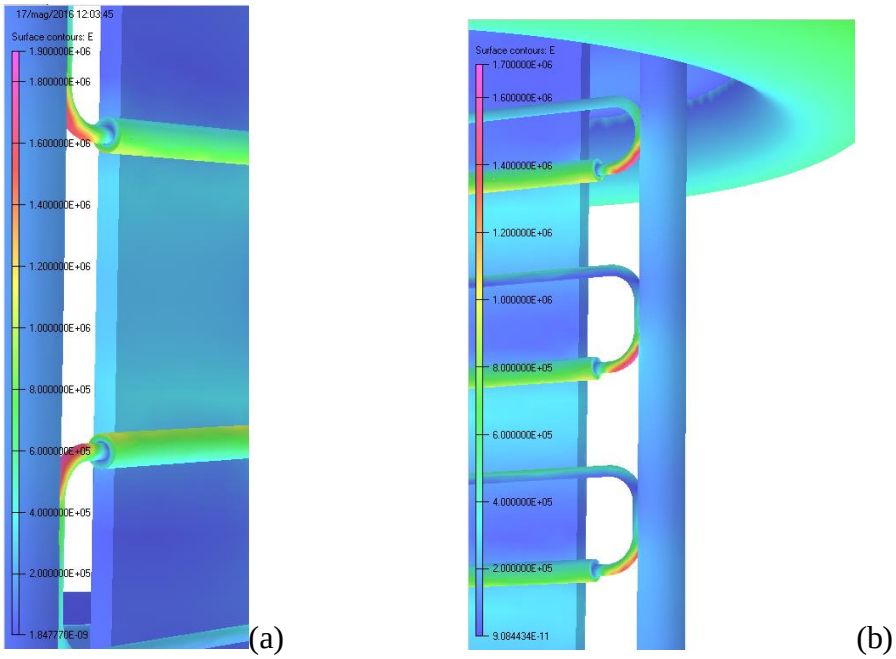


Fig. 3.70. Electric field strength distribution in (a) case H.1 and (b) case H.L.1

The parametrs dis1, dis2, dis3, and dis4 are decreased from 70mm to 65mm (model H.L.2) and 60mm (model H.L.3) in order to investigate, through the model, if a better result is achievable with longer copper tubes. The cases H.L.2 and H.L.3 are simulated and compared with the case H.L.1 (shown in Fig. 3.71).

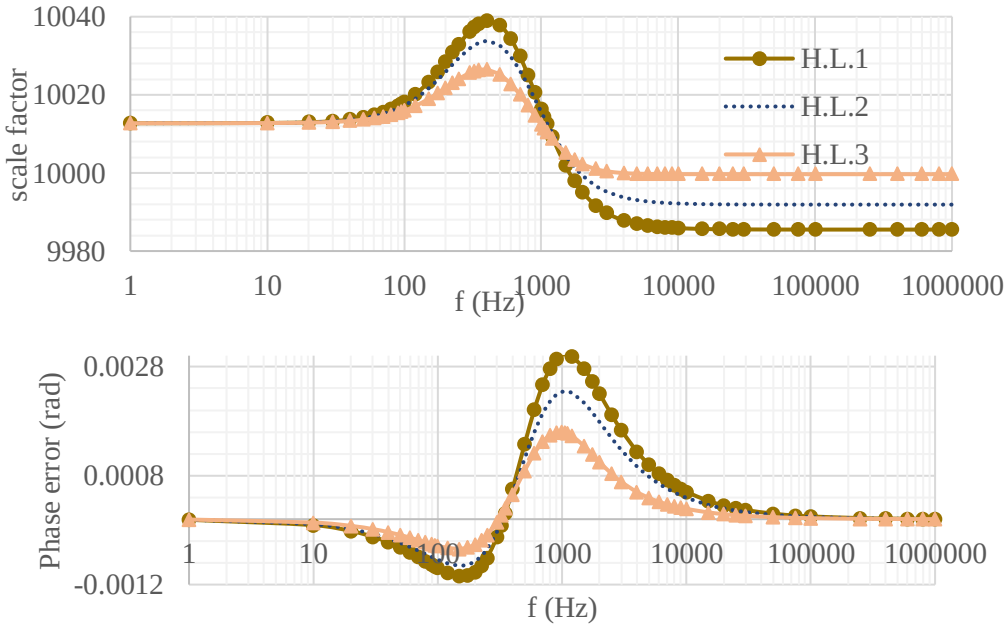


Fig. 3.71. The results of three different cases with long connection between HV resistors

As can be seen, from the Fig. 3.71 the frequency behavior improves when distances between each HV layer decrease. The reason is that the electric field coupling between HV electrodes increase by decreasing the distances. This issue decreases the electric field coupling between the HV electrodes and the ground resulting in CGs reduction. Both increasing CHVs and decreasing the CGs make a balance that results to a better frequency behavior. However, decreasing the distances between HV layers increases the electric fields strength on the conductor parts. The simulation results show that the maximum electric field in cases H.L.1, H.L.2, and H.L.3 are 1.7 kV/mm, 1.8 kV/mm, and 1.9 kV/mm, respectively (the maximum electric field in case H.1 is about 1.6 kV/mm as shown in Fig. 3.70).

Then, the case of H.1 will be developed to investigate if there is any possibility to improve the RVD frequency behavior and limiting the electric field strength.

As a first step, to analyze the effect of considering HV bus bar, the case H.2 without the HV bus bar with a similar geometry with respect to the case H.1 is simulated. The results are shown in Fig. 3.72.

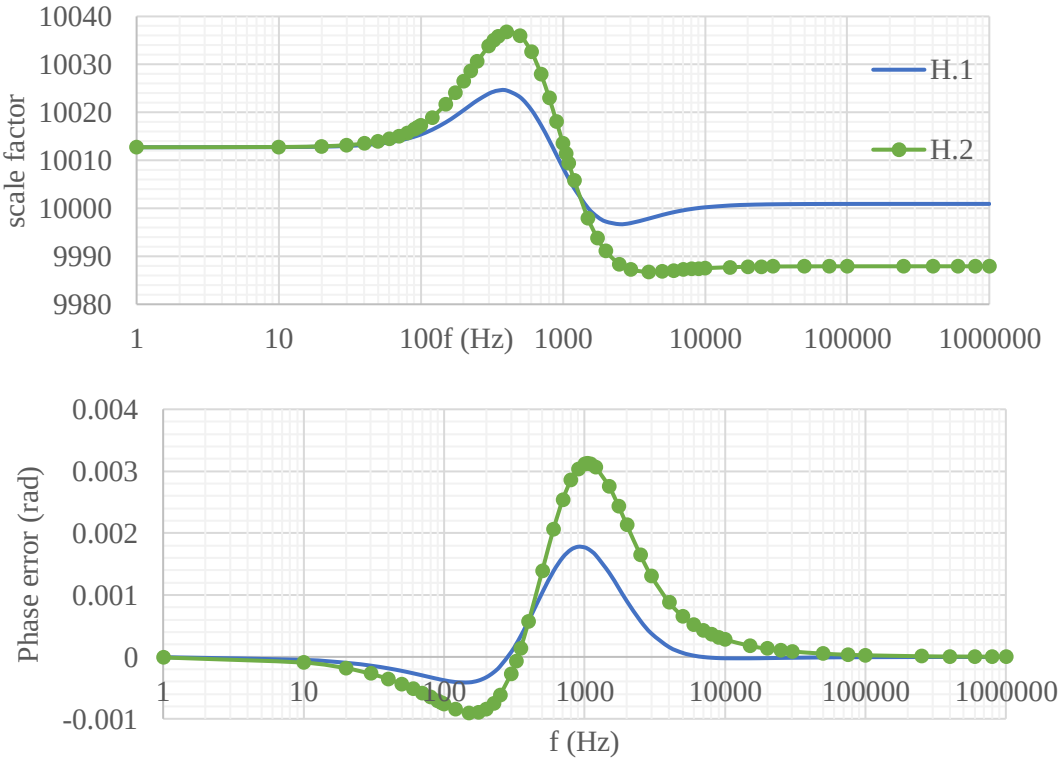


Fig. 3.72. The results of cases H.1 (with HV bus bar) and H.2 (without HV bus bar)

As the results in Fig. 3.72 shows, the presence of HV bus bar can change the frequency behavior of the VD. The reason is that the HV bus bar is close enough to the VD to be considered as an electrode of the VD. This means that the CHVs increases compared to the case without HV bus bar. This result shows that the presence and modeling of the HV bus bar is important. This means that an RVD should be designed either by including the presence of the HV bus bar or by perfectly shielding VD from the HV bus bar (to make the RVD less sensitive to the proximity effect).

In order to make a right ratio between CHVs and CGs to improve the frequency behavior, the distances between HV layers could be changed. Decreasing the mentioned distances clearly increases the electric field strength in the RVD. A solution could be the increase of parameter #dis5 from 50 mm (case H.1) to 70 mm (case H.3), while all other HV layer distances are 70 mm. The results are presented in Fig. 3.73. The increase of parameter #dis5 does not alter the CGs as much as CHV, because distances between the HV electrodes are much smaller than the distances between HV electrodes and the ground. Then, increasing the parameter #dis5 decreases the CHVs. This modification results to a worse frequency behavior (shown in Fig. 3.73) meaning that either CHVs should be increased or CGs should be decreased.

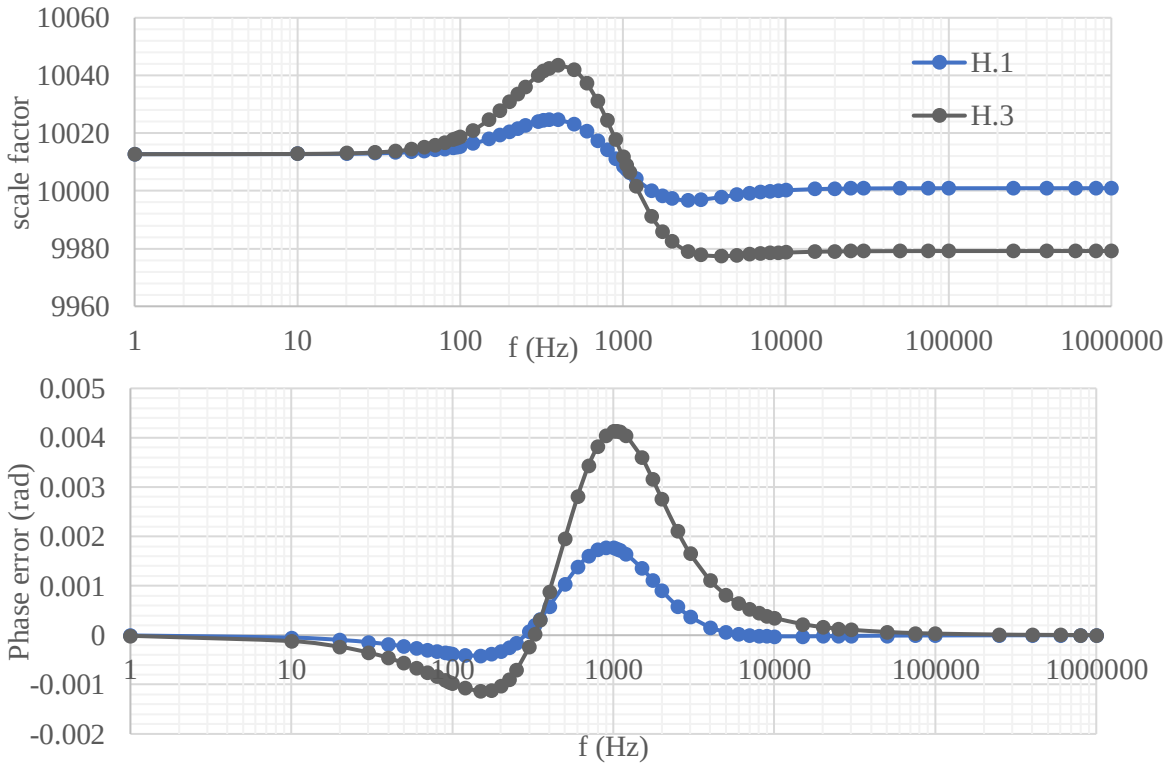


Fig. 3.73. The results of cases H.1 (#d5= 50 mm) and H.3 (#d5= 70 mm)

The case H.1 could be a reference transducer if not only the frequency behavior satisfies the requirement, but also the lowest possible maximum electric field strength can be achieved. In order to decrease the maximum electric field strength in the case H.1, two parameters #cu_t (radius of the copper curvature) and #cu_l (length of the copper connected exactly next to the HV resistors) are changed, as shown in Fig. 3.74.(a). As it can be seen in Fig. 3.70.(a), the maximum electric field strength arises in the copper curvatures. Then in case H.4, the parameters #cu_t and #cu_l are changed in order to avoid semi-sharp copper edges which can produce the electric field hot spots, while the copper length between HV resistors is almost same. Parameters #cu_t and #cu_l, which are 5mm and 10mm in case H.1, become 11mm and 4mm in case H.4, respectively(see Fig. 3.74). In this arrangement, the frequency behavior remains almost the same, while the electric field hot-spot could be reduced. The frequency behaviors of cases H.1 and H.4 are shown in Fig. 3.75.

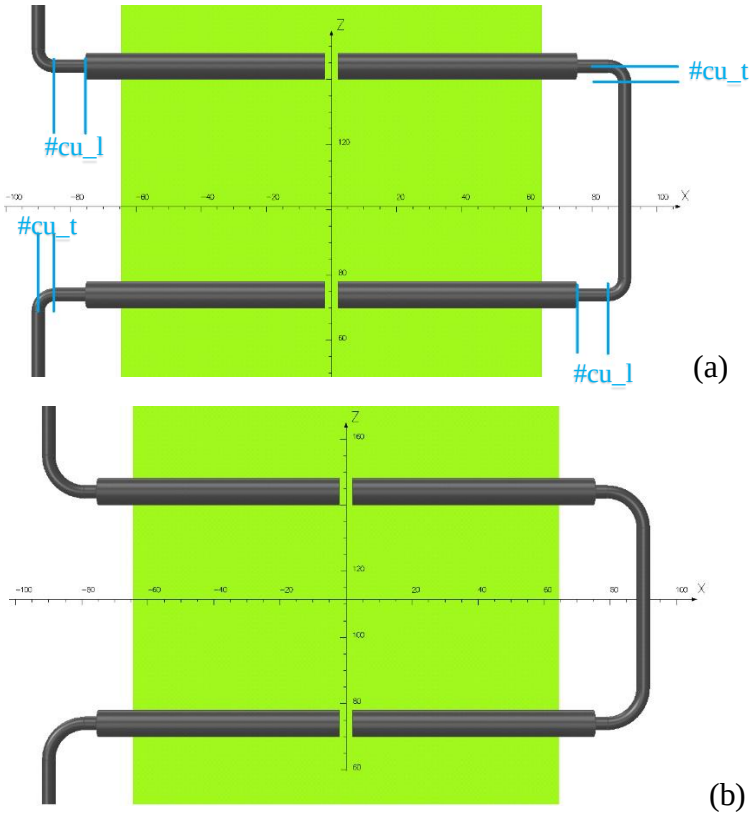


Fig. 3.74. Introducing parameters for copper conductor in (a) case H.1 (#cu_t=5mm, #cu_l=10mm) (b) case H.4 (#cu_t=11mm, #cu_l=4mm)

As shown in Fig. 3.76, the electric field hot-spot is decreased in case H.4, however not so much, if compared to the one in case H.1. In order to decrease the electric field coupling between the HV electrodes and the ground, an LV-connected metallic shied is introduced in case H.5, where the parameters #cu_t and #cu_l, are kept at 11mm and 4 mm, respectively. The case H.5 with LV-connected shield is represented in Fig. 3.77. The height of the LV shield is varied from Cases H.5 up to H.8, where the arrangements differ only for the height of LV shield. The results are shown in Fig. 3.78.

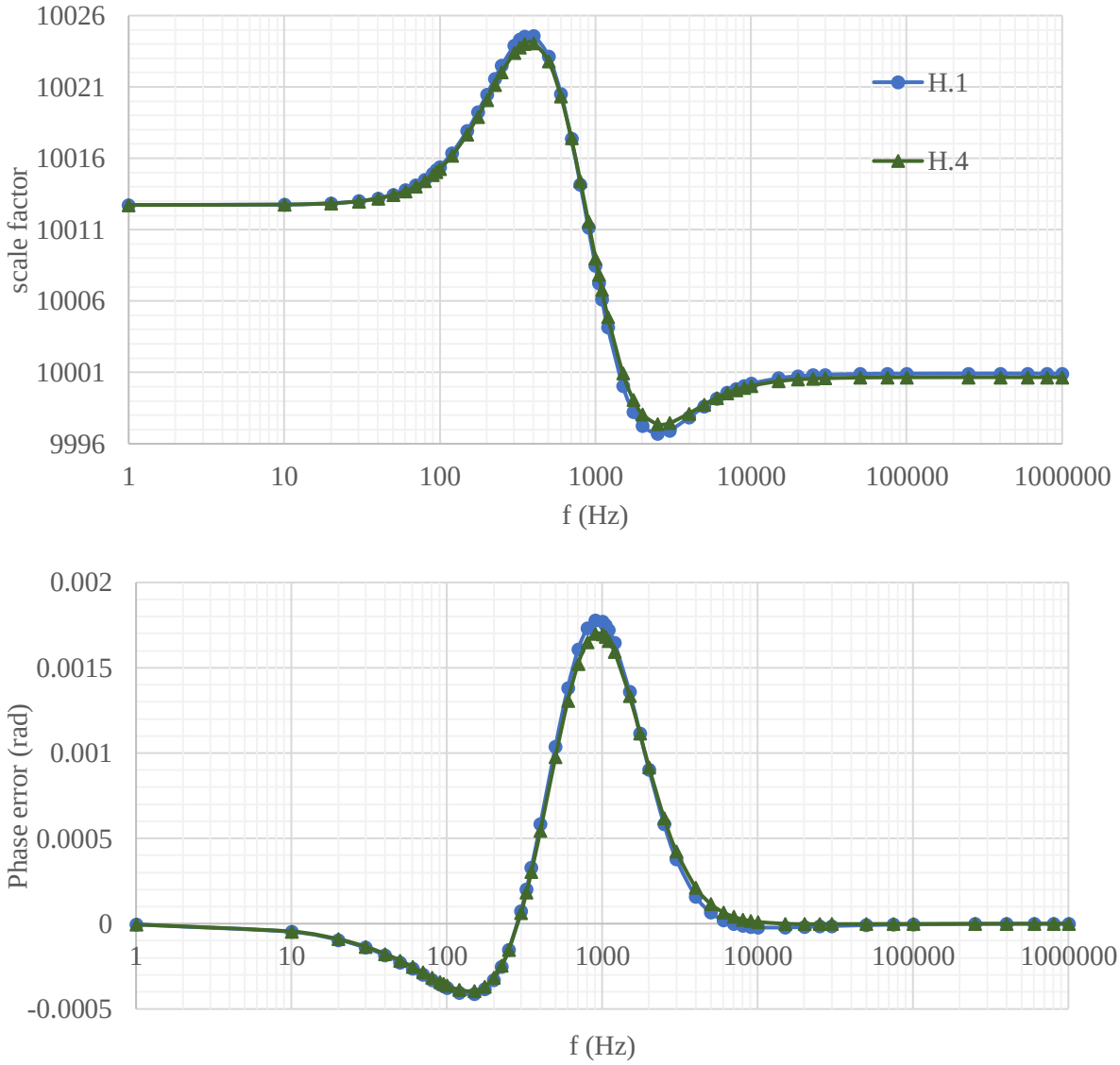
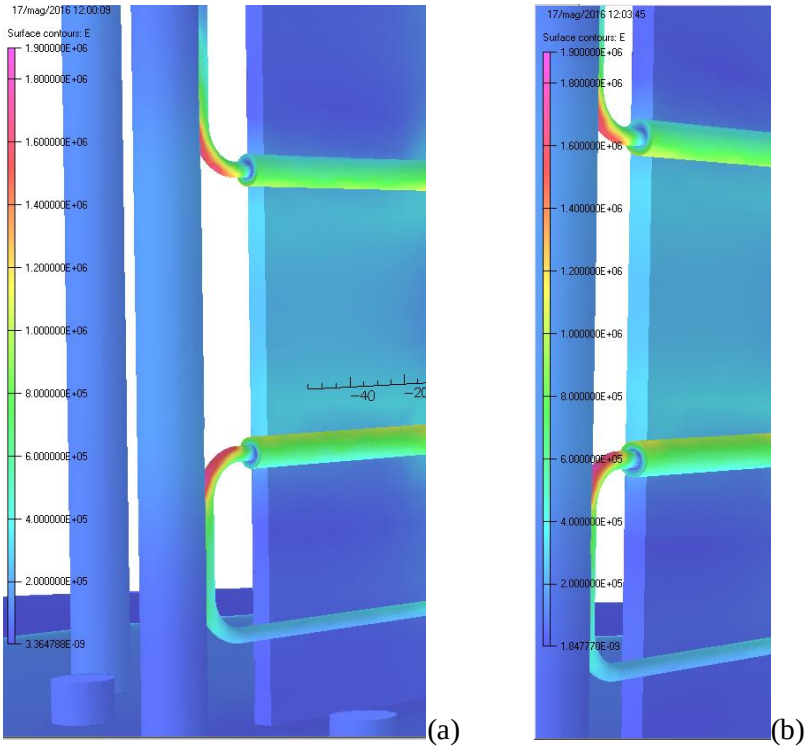


Fig. 3.75. The results of case H.1 (#cu_t=5mm, #cu_l=10mm) and the case H.4 (#cu_t=11mm, #cu_l=4mm)



(a) (b)

Fig. 3.76. Electric fiend hot-spots in (a) case H.1 (#cu_t=5mm, #cu_l=10mm) (b) case H.4 (#cu_t=11mm, #cu_l=4mm)

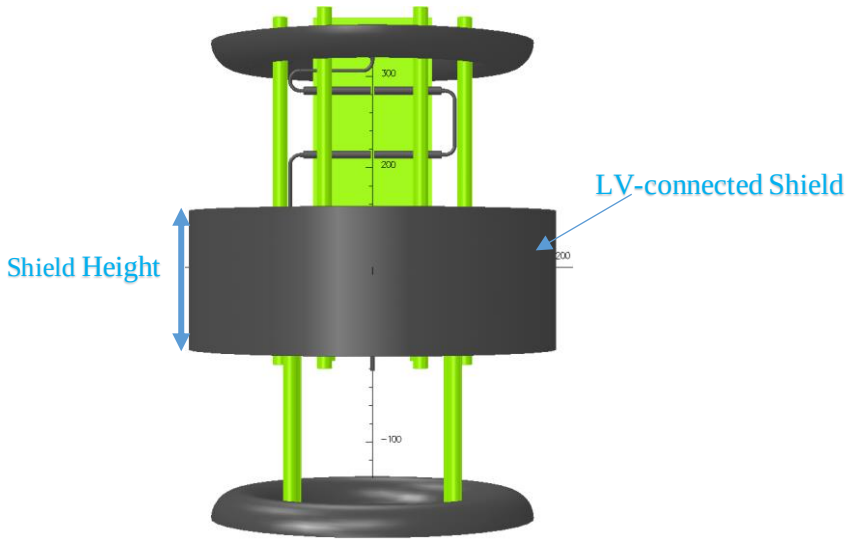


Fig. 3.77. Introducing an LV- connected shield as in case H.5

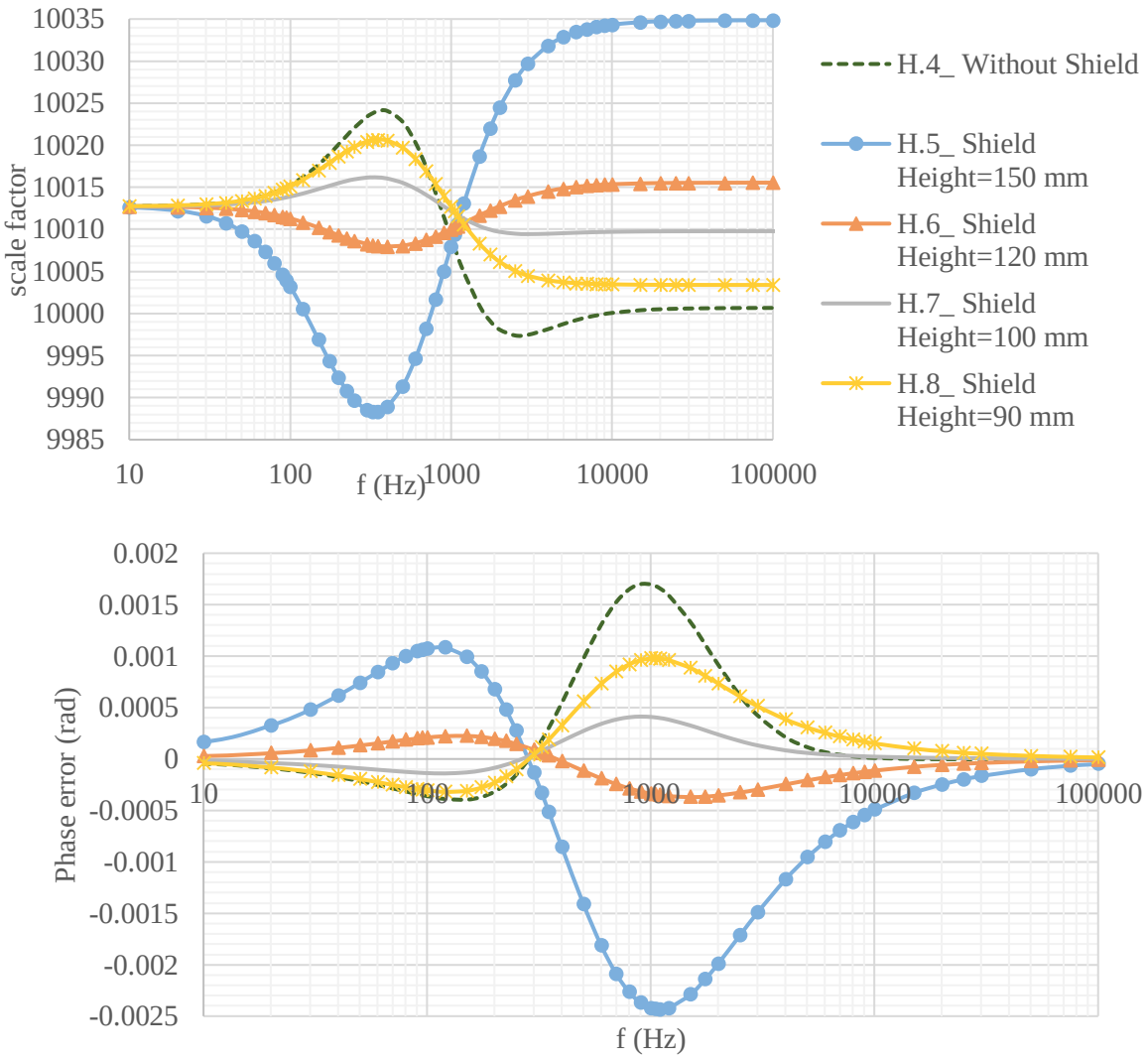


Fig. 3.78. The results of case H.4 without LV-connected shield and the cases H.5, H.6, H.7, and H.8 with LV-connected shields

The result shown in Fig. 3.78 firstly shows that LV-connected shield modifies the CHV and CG in a way to get an improved frequency behavior. The optimum height for the LV shield is in a range between 100 mm and 120 mm. The electric field distribution in LV connected shields are shown in Fig. 3.79. As can be seen, the maximum electric field increases by increasing the shield height. This happens because the shield is connected to the LV potential, which is approximately equal to the ground potential (from the point of view of electric field calculation). Then, as the LV shield is closer to the HV electrodes, the maximum electric field strength increases. Therefore, the shield height is chosen 100 mm (case H.7) in order to limit the reduction of the distance between the shield and the HV electrodes.

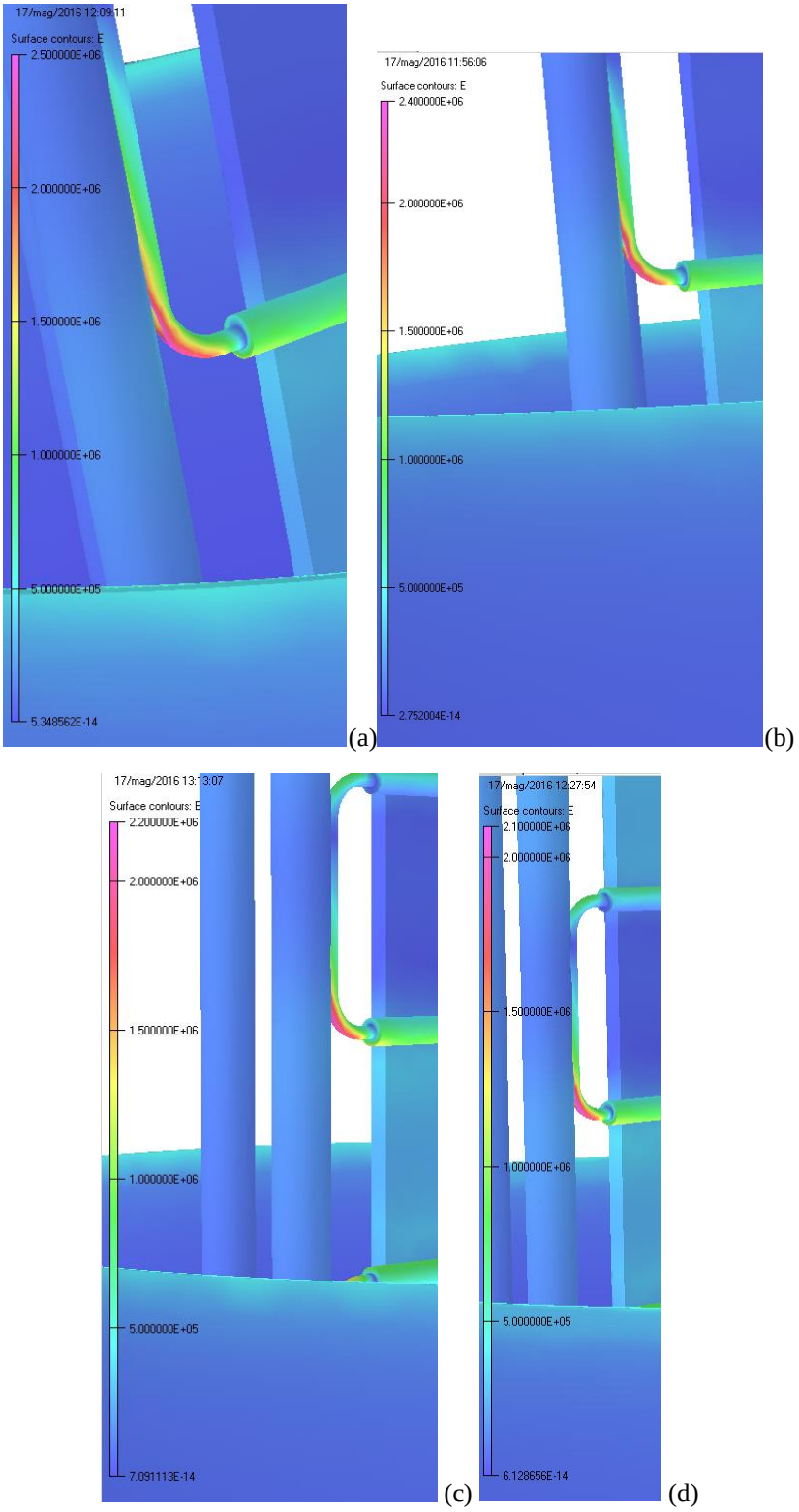


Fig. 3.79. The results of cases (a)H.5, (b)H.6, (c)H.7, and (d)H.8 with different Shield heights

The curvature radius of the copper (parameter #cu_t) is increased from 11mm (case H.7) to 15mm (case H.9) and to 20mm (case H.10), in order to reduce the maximum value of the electric field. The frequency behavior of the cases H.7, H.9, and H.10 with different copper curvature radii is compared in Fig. 3.80. The curves are practically superimposed and all cases presented in Fig. 3.80 can satisfy the requirement of a reference VD. The electric field strength distribution of the cases H.7, H.9, and H.10 are shown in Fig. 3.81.

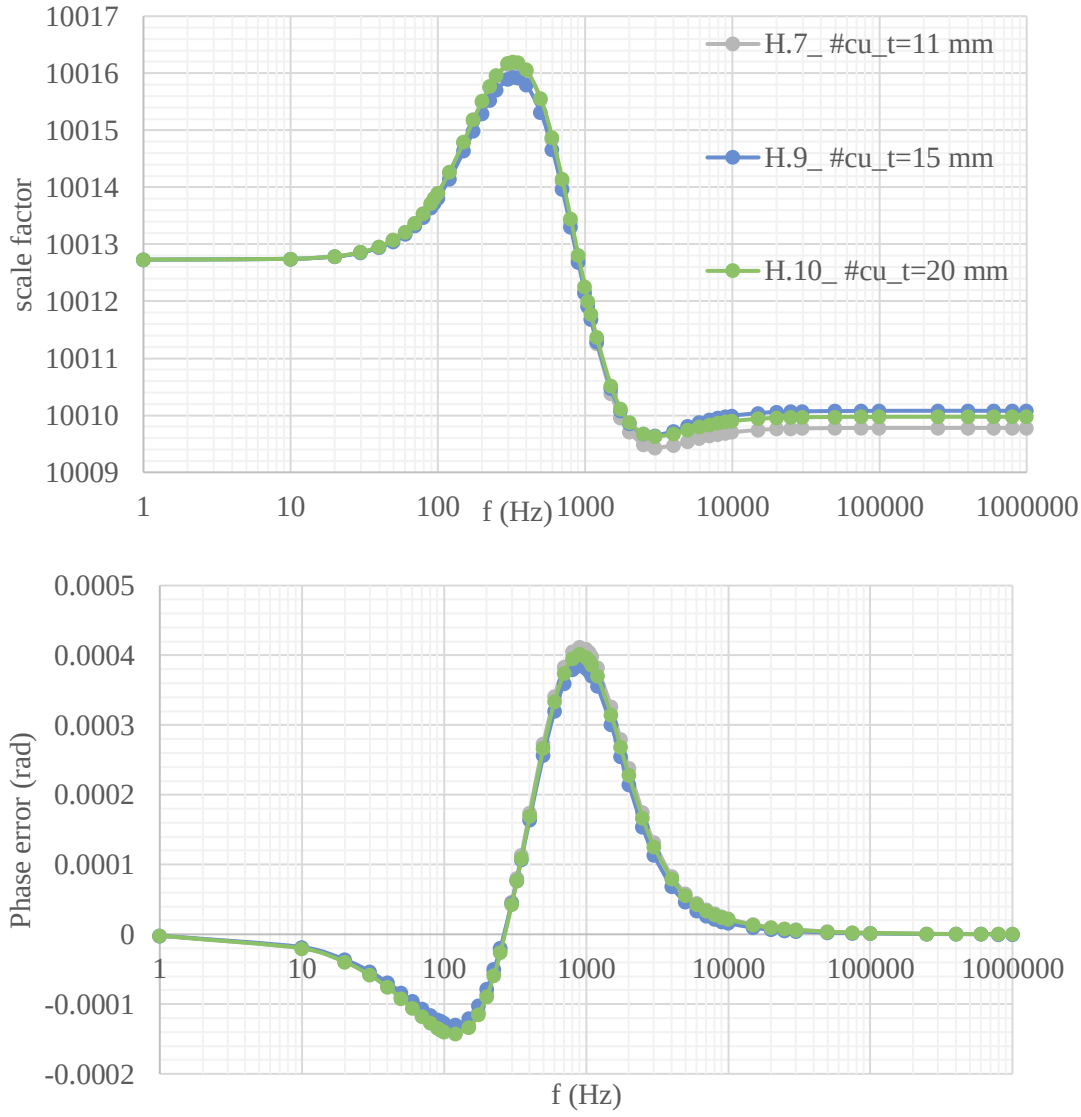


Fig. 3.80. The frequency behavior of the cases H.7, H.9, and H.10 with different copper curveture radius

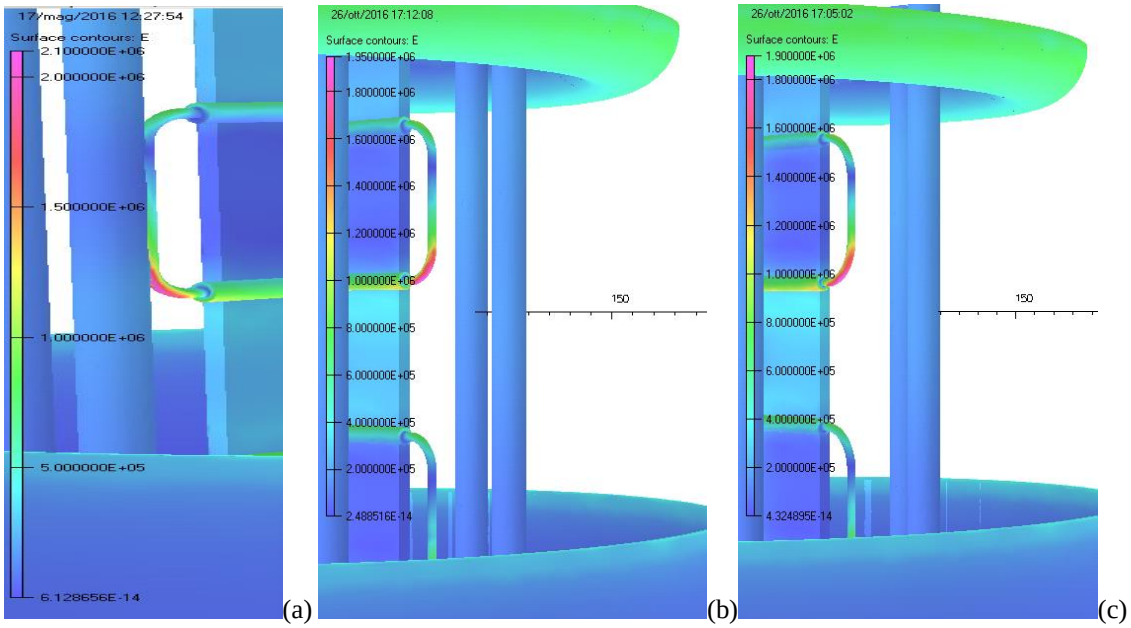
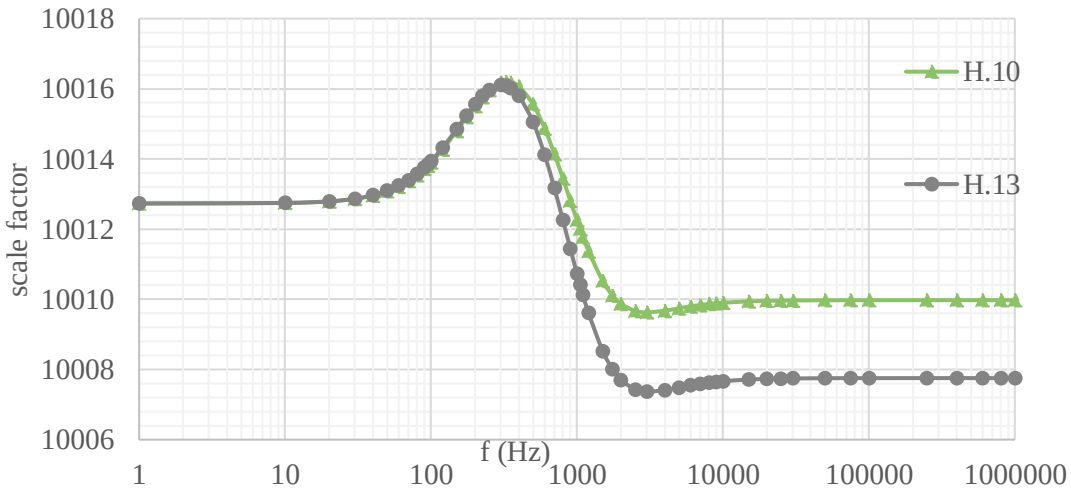


Fig. 3.81. The electric field distribution in cases (a) H.7, (b) H.9, and (c) H.10 with different copper curveture radius

As expected, increasing the parameter #cu_t decreases the maximum value of electric field. However, a further reduction of this quantity is still required. For such a purpose, the values of parameter #cu_l and #cu_t are modified from 4 mm and 15 mm (case H.10) to 0.1 mm and 20 mm (case H.13). The frequency behavior of and electric field distribution in two cases H.10 and H.13 are shown in Fig. 3.82 and Fig. 3.83, respectively.



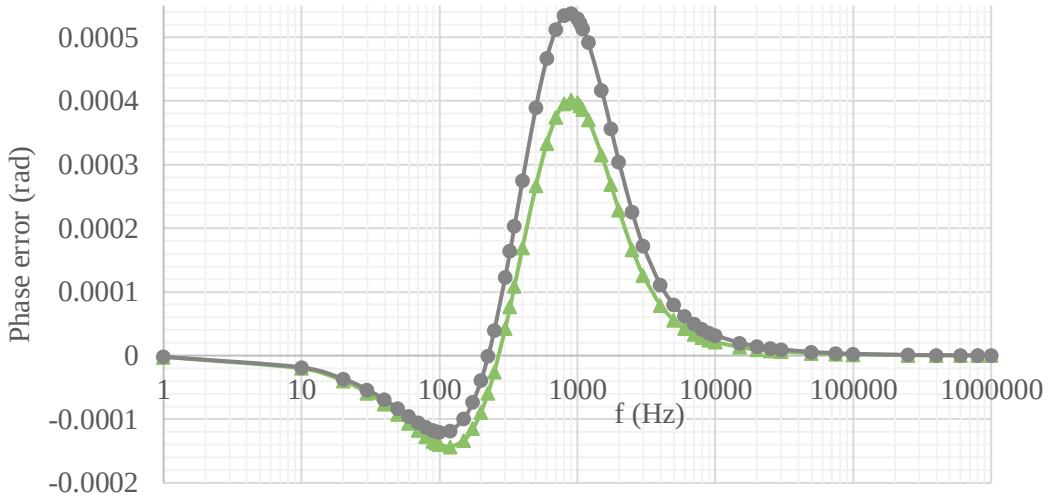


Fig. 3.82. The frequency behavior of the cases H.10 and H.13

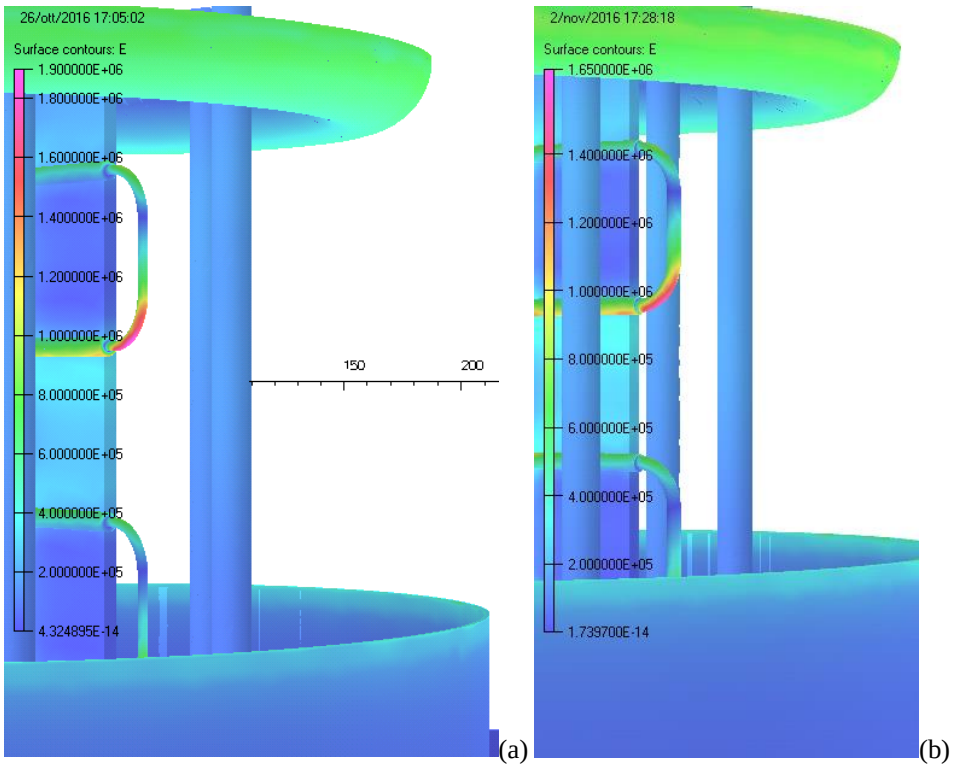


Fig. 3.83. The electric field distribution in cases (a) H.10, (b) H.13

Fig. 3.82 and Fig. 3.83 show that decreasing the parameter #cu_l brings down the maximum electric field strength but the frequency behavior is slightly worsen. The analysis of the capacitance matrix (the output result of the FEM) proves that CHVs are

decreased causing a reduction in ratio of CHVs to CGs. This issue deteriorates the frequency behavior. However, the frequency response of the case H.13 is still acceptable and meets the requirement of a reference VD. In the next step, the parameter #cu_t (radius of the copper curvature) in case H.14 is increased a bit more in comparison with the case H.13, to further reduce the maximum electric field strength. The results, presented in Fig. 3.84 and Fig. 3.85, show that the modification parameter #cu_t (radius of the copper curvature) does not substantially modify the frequency behavior, as the metallic surface in the geometry slightly changes. On the other hand, the maximum electric field strength is decreased from 1.65 kV/mm (case H.13) to 1.6 kV/mm (case H.14).

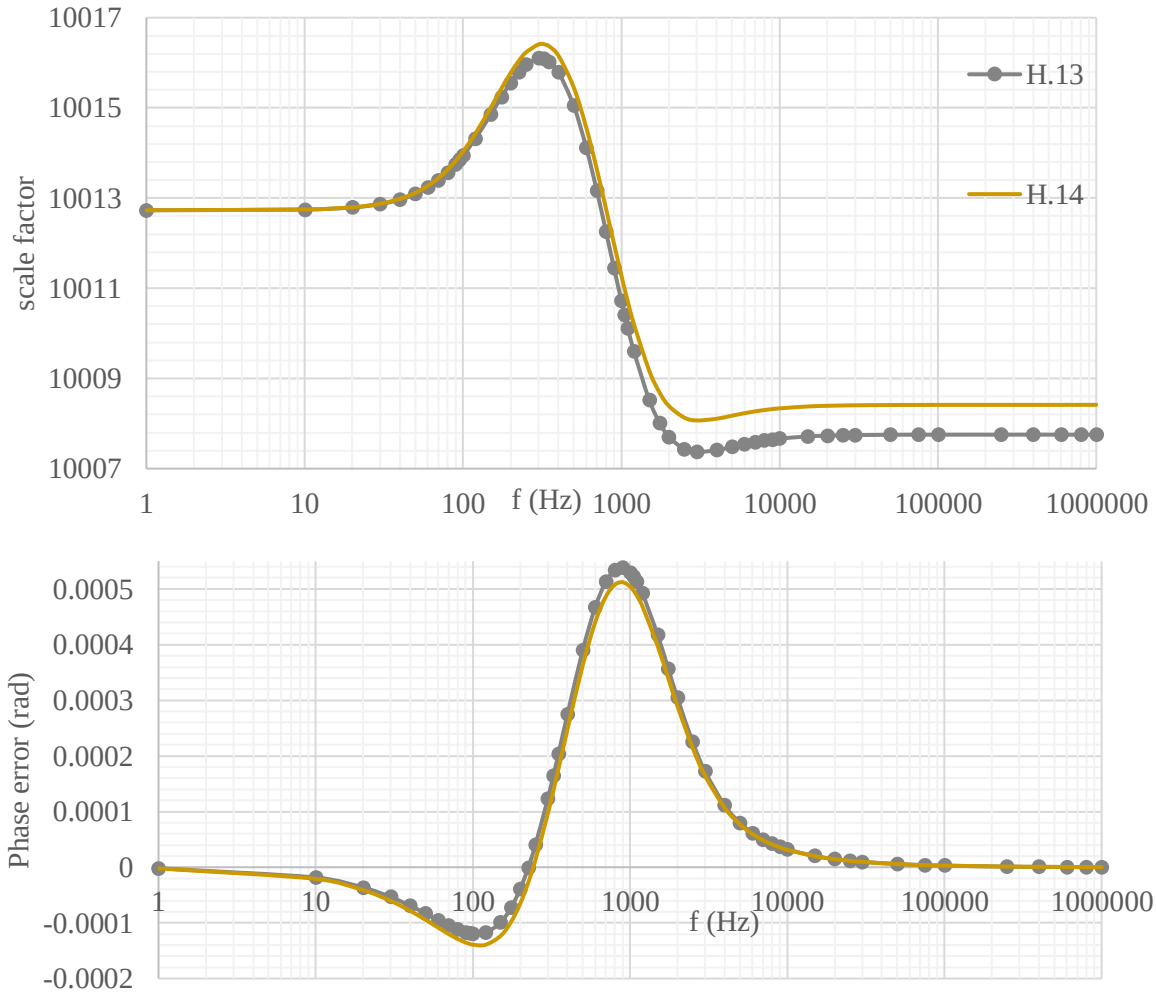


Fig. 3.84. The frequency behavior of the cases H.13 (#cu_t= 20 mm) and H.14 (#cu_t= 23.2 mm)

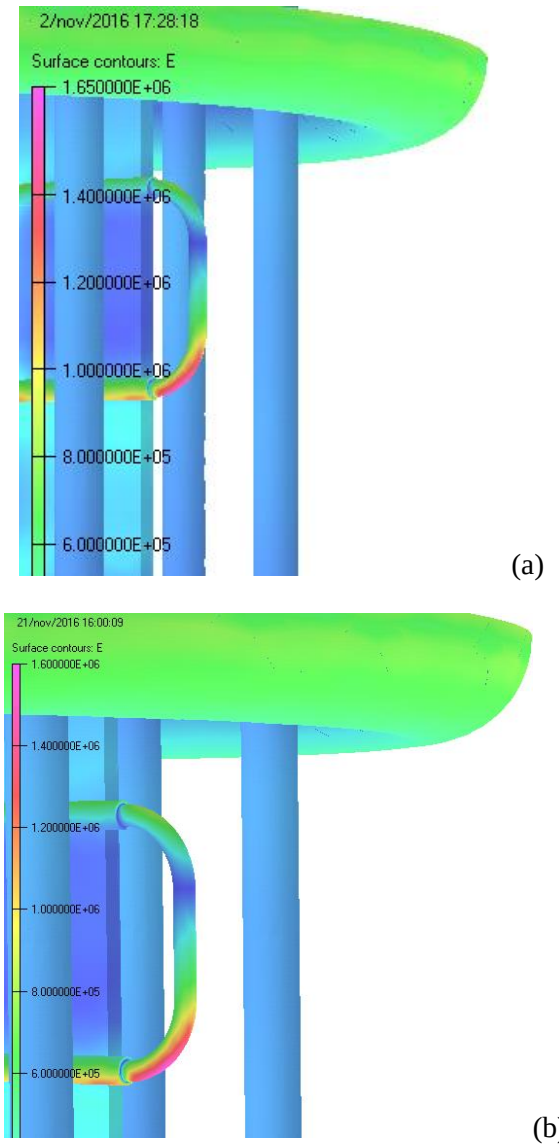


Fig. 3.85. The electric field distribution in cases (a) H.13 (#cu_t= 20 mm), (b) H.14 (#cu_t= 23.2 mm)

In all configurations with horizontally placed resistors RVD, the thickness of LV-connected shield has been 2 mm. In order to decrease the weight of the RVD, the thickness of the shield is decreased to 1 mm in case H.17. However, the electric field strength should be calculated on the edge of the shield as it becomes particularly thin in a high voltage area.

The frequency behavior of two cases H.14 and H.17 are quite similar, as shown in Fig. 3.86. Moreover, the maximum electric field strength on the edge of the shield is still low (about 0.5 kV/mm) in case H.17 as shown in Fig. 3.87.

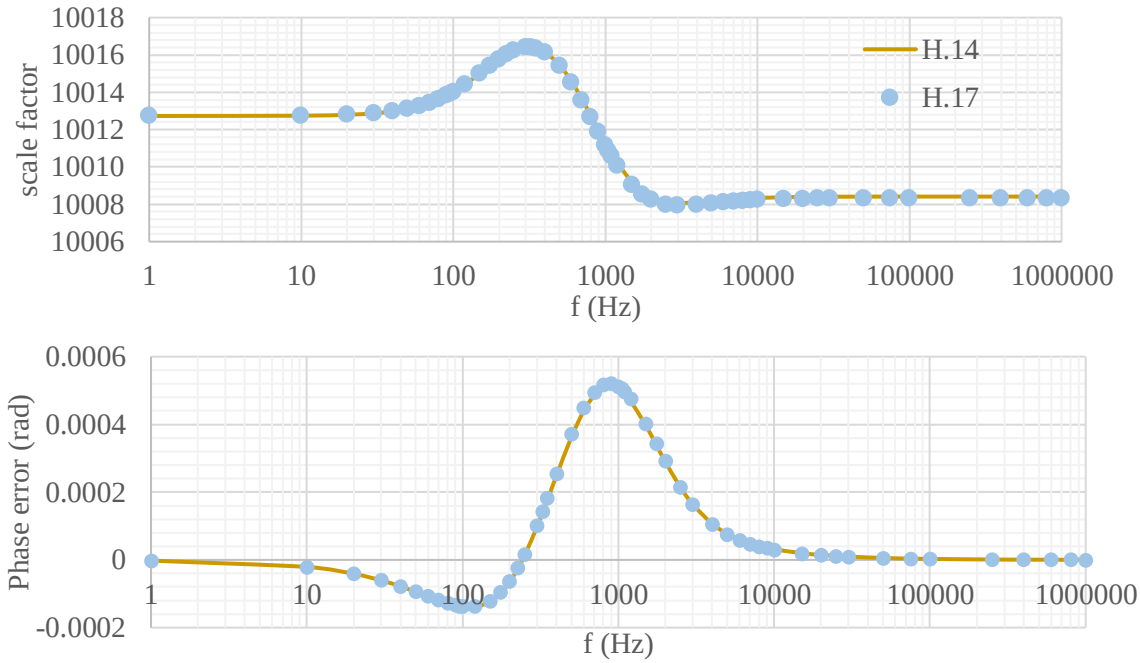


Fig. 3.86. The frequency behavior of the cases H.13 and H.17

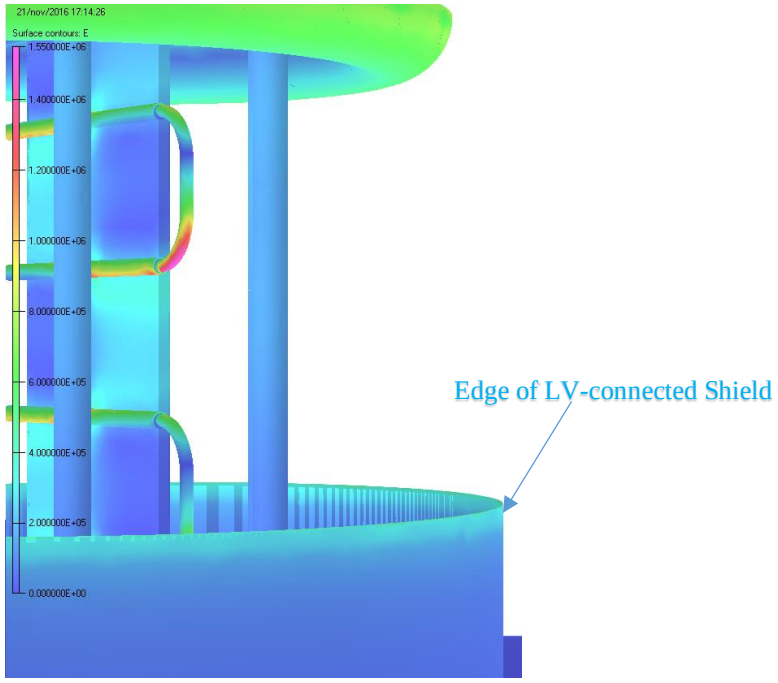


Fig. 3.87. Electric field strngth distribution in case H.17

The frequency behavior of the cases H.13, H.14, and H.17 are satisfactory and these arrangements could be realized for a reference voltage transducer. However, in those

cases there is still an electric field hot-spot in the curvature of the copper tubes, which increases the probability of the corona effect. Furthermore, the maximum electric field strength will be tried to be lowered, up to a value where the frequency behavior is not worsened. The electric field decrease is required since the environmental condition (especially humidity and air composition) may decrease the electric field strength threshold that can activate the corona effect. Two possible solutions can be adopted in the horizontally placed resistors RVD to overcome this problem. The first solution is to increase the distance between the HV electrodes. Increasing the distance between the electrodes, being constant the potential difference between them, can bring down the electric field value in the hot-spots. However, the total height and the volume of the VD increases. The second solution consists in a geometry change of the VD. This matter is introduced in detail in the next section.

3.8 Zig-zag RVD simulations

3.8.1 Initial model

In order to get a similar frequency behavior as in the horizontal VD layout, also avoiding the electric field hot-spot at the same time, a new RVD with zig-zag configuration is introduced. The zig-zag RVD is obtained by tilting and decreasing the length of each copper tube, as shown in Fig. 3.88. In this way, the distance between the elements subjected to a HV/2 voltage drop is increased, while the terminal potential difference remains unchanged. Then, electric field strength interesting copper tubes should be consequently reduced. Furthermore, the CHVs decrease as the surface area of each electrode decreases. The initial model of zig-zag RVD as case Z.1 is shown in Fig. 3.89. The full FEM model of case Z.1 considering the ground effect and HV bus bar is shown in Fig. 3.90. The detailed dimensions and conditions of all simulated zigzag RVDs are shown in Table 3.5.

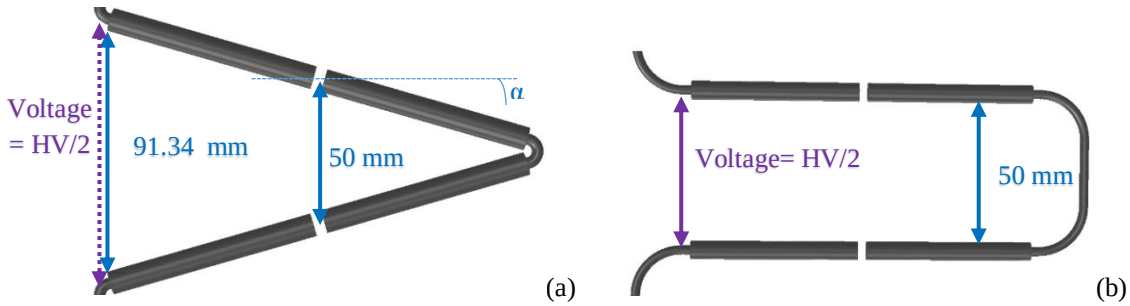


Fig. 3.88. The resistor placement in (a) zig-zag RVD (b) horizontally placed RVD

The frequency behavior of the zig-zag RVD is shown in Fig. 3.94. The frequency behavior of the case H.17 is added to the Fig. 3.94 for sake of comparison. In case Z.1 and in all other arrangements of zig-zag VD (except the proximity effect investigations), the CBT (a single extra capacitor added to the output voltage in parallel) is chosen in a way such that the SF deviation from the rated SF is as low as possible. Besides, in Fig. 3.95 the electric field distribution on the zig-zag RVD is given.

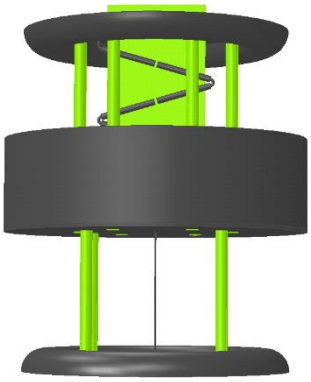


Fig. 3.89. Initial model of Zig-Zag RVD (case Z.1)

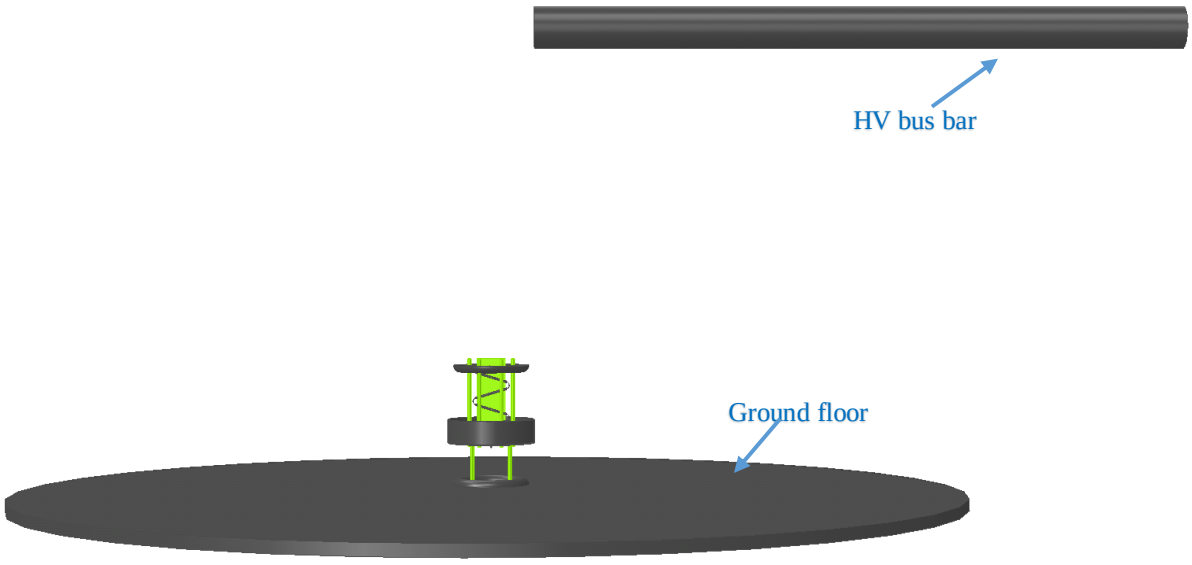


Fig. 3.90. Full FEM model of the case Z.1

Different parameters used in the modeling of the zig-zag VD are defined in Table 3.6.

Table 3.6. List of parameters defined for zig-zag RVD

Name of parameter	Initial value (mm)	Explanation of the parameter
#d1	70	distance from the middle plate up to center of the 1st HV resistor (shown in Fig. 3.91)
#d2	70	the distance from center of the 1st HV resistor up to the center of the 2nd HV resistor (shown in Fig. 3.91)
#d3	70	distance from center of the 2nd HV resistor up to the center of the 3rd HV resistor (shown in Fig. 3.91)
#d4	70	distance from center of the 3rd HV resistor up to the center of the 4th HV resistor (shown in Fig. 3.91)
#d5	50	distance from center of the 4th HV resistor (the top one) up to the surface of the HV plate at the top of the VD (shown in Fig. 3.91)
#G	180	distance between the middle plate and the ground plate (shown in Fig. 3.91)
#Pr	200	radius of the middle plate (shown in Fig. 3.91)
#α	16	angle between the resistor and the horizontal axis (shown in Fig. 3.88)
#a	0	distance between the center of the VD and the start of the HV bus bar (in the direction of the HV bar) (shown in Fig. 3.92)
#b	0	distance between the center of the VD and the start of the HV bus bar (perpendicular to the HV bar direction) shown in Fig. 3.93
#eps	2.9	electrical permittivity of the insulations used in the VD

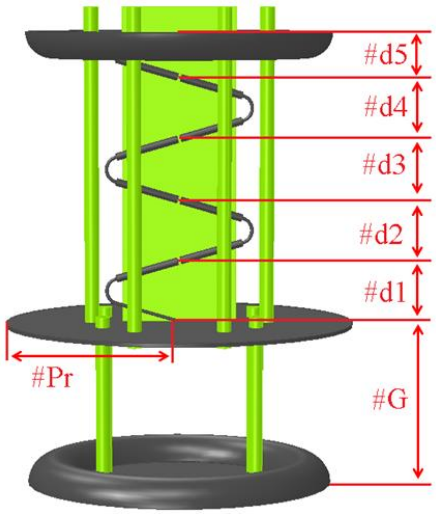


Fig. 3.91. Definition of the differemnt parameters in zig-zag VD

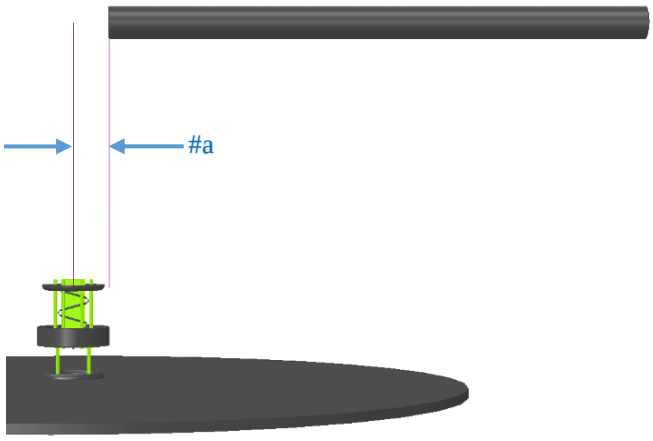


Fig. 3.92. Definition of the parameter #a

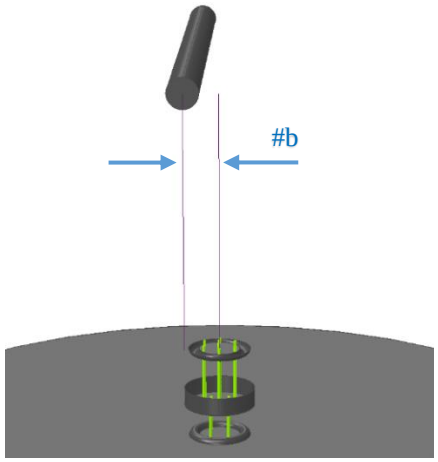


Fig. 3.93. Definition of the parameter #b

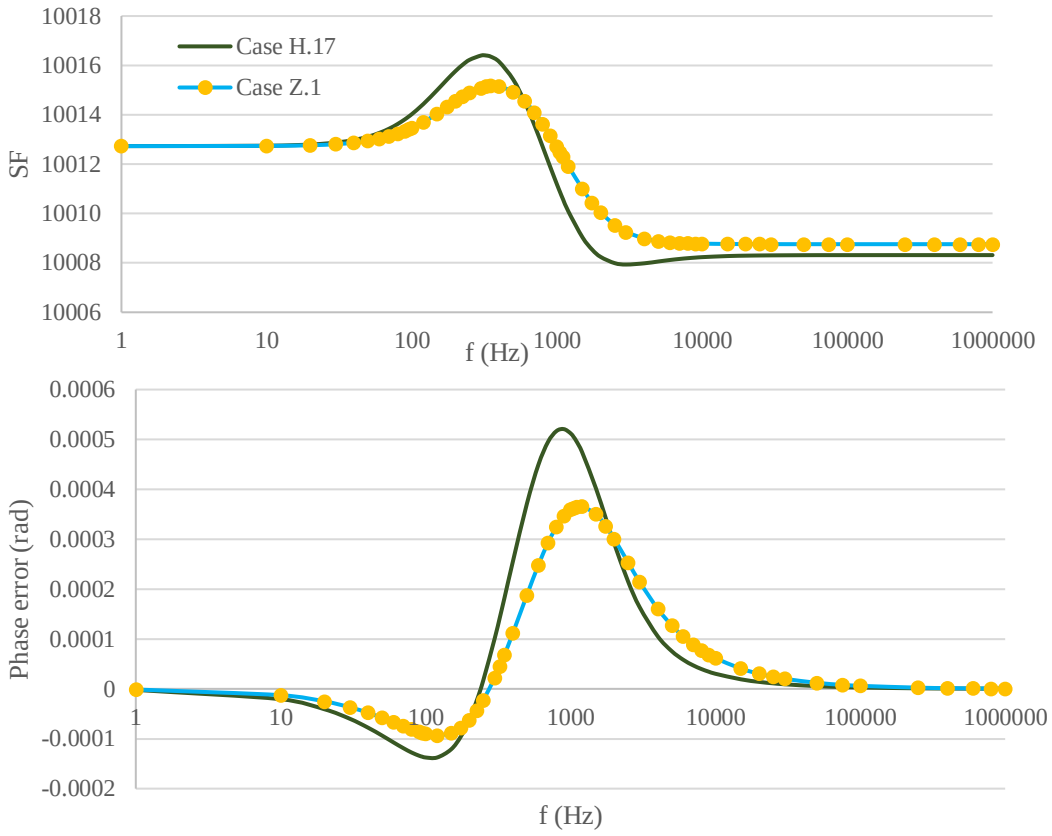


Fig. 3.94. Frequency behavior of the 1st Zig-Zag RVD (case Z.1) and the last horizontal RVD (case H.17)

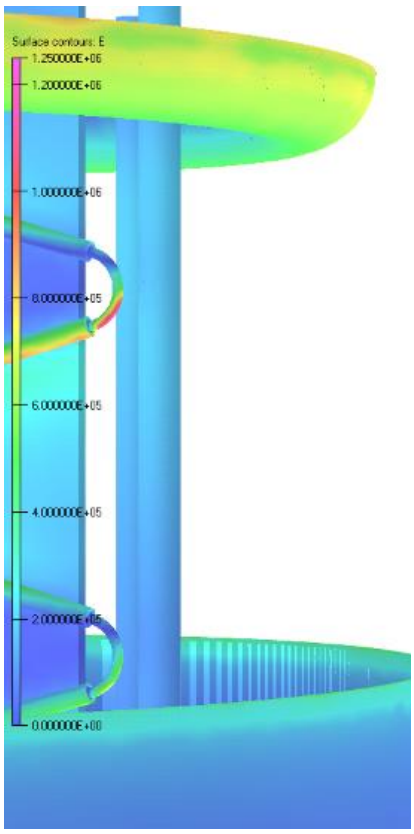


Fig. 3.95. Electrical field distribution in the Zig-Zag RVD (case Z.1)

As can be seen, the frequency behavior of the case Z.1 meets the requirement of a reference voltage transducer. Besides, the maximum electric field (E_{max}) in the zig-zag RVD is about 1.25 kV/mm which is considerably lower if compared with the horizontally placed resistors studied in section 3.7.

Although the maximum electric field E_{max} seems to be sufficiently low for avoiding the corona effect, the next cases will be modelled in order to find a VD layout having a lower E_{max}, while the frequency behavior satisfies the requirement of a reference voltage transducer and the VD size is not much larger than the case Z.1.

The case Z.2 has the same dimensions as the case Z.1 with the different #d1, which is increased from 70mm to 80mm, in order to decrease the maximum electric field occurred on the copper curvature. The outcomes of case Z.2 are shown in Fig. 3.96 and Fig. 3.97.

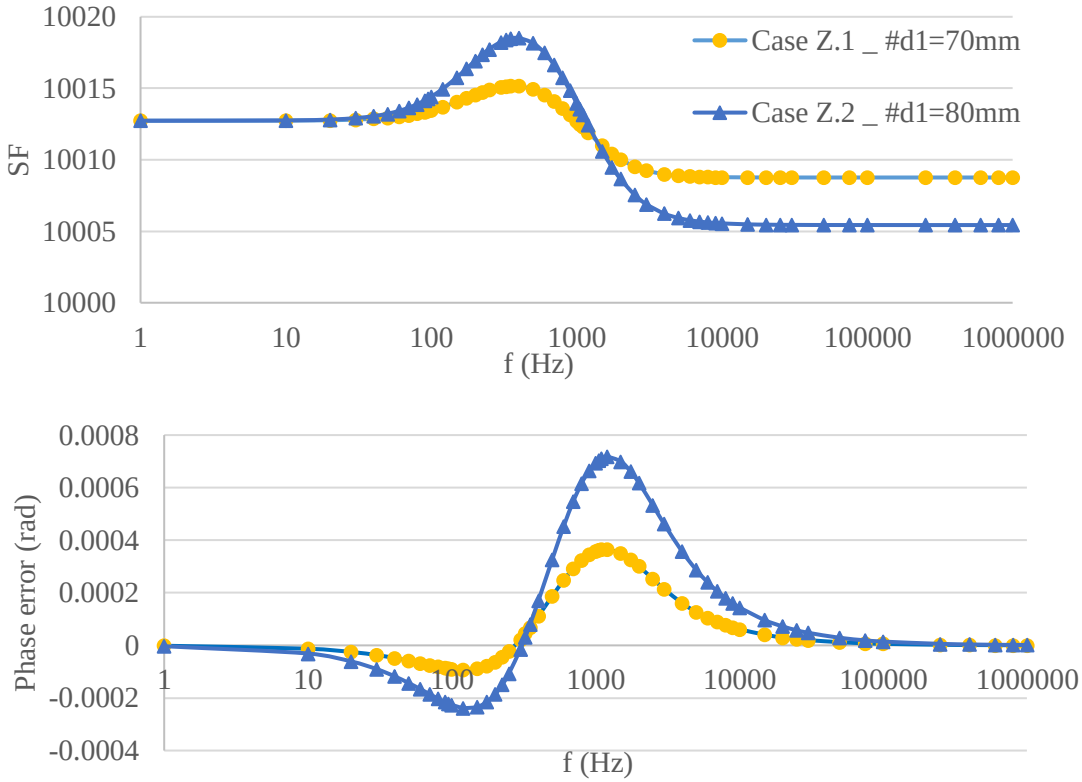


Fig. 3.96. Result of the Zig-Zag RVD (case Z.2)

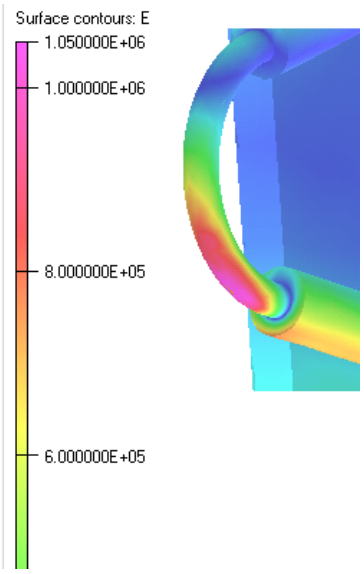


Fig. 3.97. Electric field distribution in the case Z.2

The results in Fig. 3.97 show that the E_{max} is sensibly decreased from 1.25kV/mm to 1.05 kV/mm. However, the CHV frequency behavior is worsened as shown in Fig. 3.96. In case Z.1, the ratio of CHVs to CGs was perfect for having an approximately flat SF and a very small phase error in the case Z.1. However, by increasing #d1 both CHVs and CGs raise and consequently the ratio between CHVs and CGs changes in case Z.2. Therefore, the frequency response of the case Z.2 is not as good as the one of the case Z.1.

3.8.2 Effect of the external HV feeding section on behavior of the zig-zag RVD

In this section the HV feeding section (outside of the RVD geometry), which is present in any HV laboratory or environment for connecting the VD to the HV side, is considered for modeling. Actually, the stray electrical field going from inside of the VD towards the HV feeding section modifies the stray capacitance matrix of the VD. Therefore, this feeding section may change the frequency behavior of the VD, by acting as an HV electrode.

In order to check out the sensitivity of the zig-zag RVD behavior versus the presence of the HV section, the case Z.4 is introduced. Case Z.4, shown in Fig. 3.98, is modelled with the same geometry and size used in the case Z.1, but removing the HV bus bar that was present in all previous zig-zag cases. The frequency behaviors of both cases Z.1 and Z.4 (with and without HV bus bar, respectively) with the same fixed CBT are presented in Fig. 3.99. The CBT is firstly tuned in case Z.1 to the value that provides the best frequency response (versus CBT). Then the same CBT is used in the case Z.4. As it can be seen in Fig. 3.99, the removal of HV bus bar has profoundly worsened frequency behavior by modifying the stray capacitance matrix of the Z.4 with respect to the case Z.1.

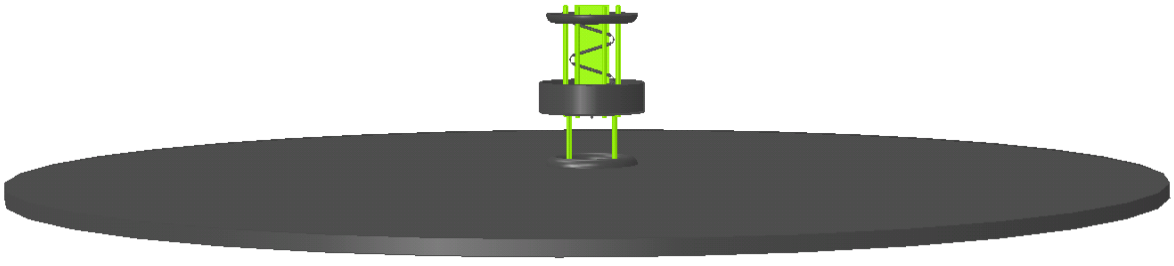


Fig. 3.98. The case Z.4 without considering HV bus bar

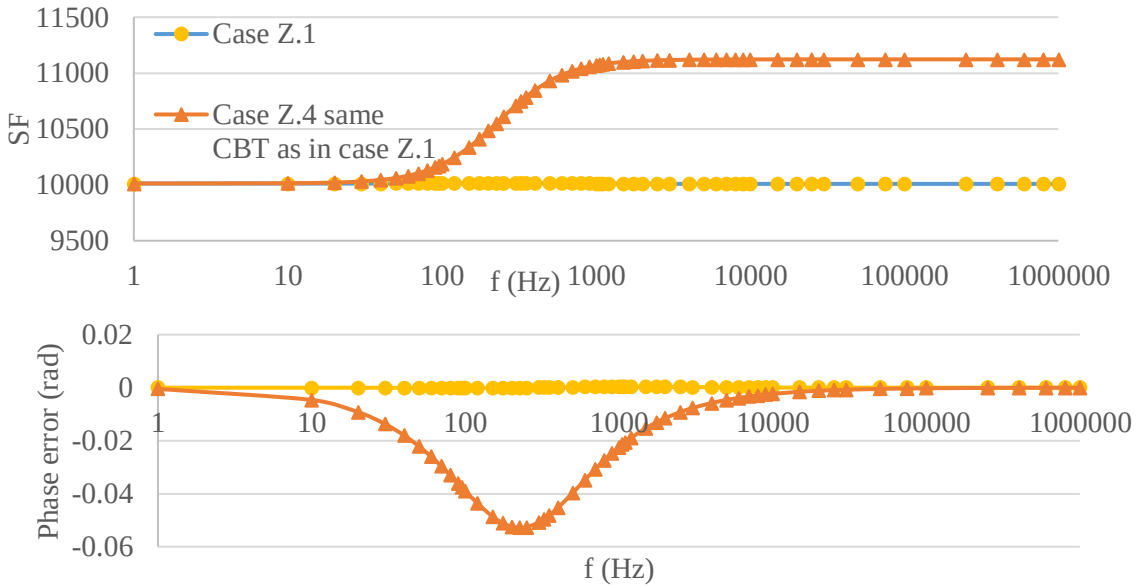


Fig. 3.99. Frequency bahvior of the cases Z.1 and Z.4 with the same CBT

As the application of the reference transducer is in the laboratory for the calibration of other voltage transducers, then it is possible to use the model Z.1 after tuning the CBT considering the HV feeding section. The result of the case Z.4 after tuning the CBT for the condition without an HV bus bar (different CBT from the one in case Z.1) is presented in Fig. 3.100. It is clear that the zig-zag RVD can still provide a striking frequency behavior providing that the CBT is tuned according to the laboratory conditions.

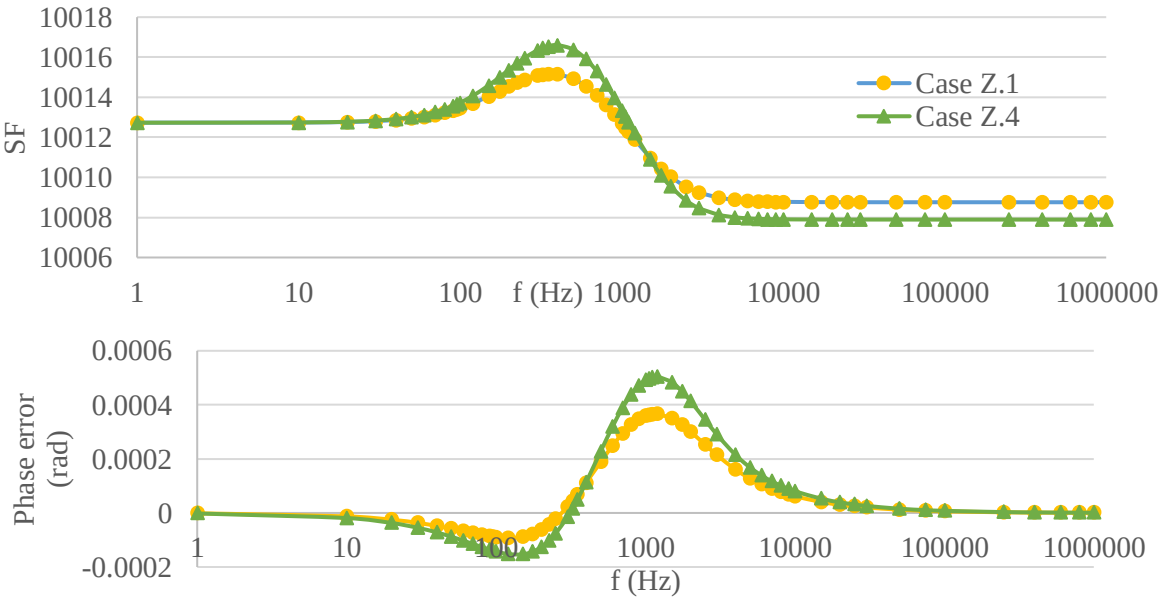


Fig. 3.100. Result of the Zig-Zag RVD with different CBT

It is clear from the results presented in Fig. 3.99 and Fig. 3.100 that the laboratory conditions extremely affect the frequency behavior of the zig-zag RVD. A way-out from this sensitivity is accurately shielding the inner HV section of the VD from the outer parts of the VD as the solution proposed in Fig. 3.101. In this way, any change of the position or shape of the objects outside of the VD does not modify the electrical field coupling between inner part of the VD and the proximity objects. However, if the shield is connected to LV, the effects of stray capacitance between proximity objects and the LV electrode changes. This again means that proximity effect modifies the frequency behavior. This issue can be solved by electrically connecting the shield to the ground or to HV, so that the stray capacitance between the HV electrodes and the grounded objects cannot modify the frequency behavior. On the contrary, the introduction of a grounded or HV-connected shield, which fully or semi-fully covers the VD, produces two new problems:

- At first, the distance between HV and grounded parts will decrease giving rise to a high electrical field strength distribution and consequently corona effect.
- Secondly, it increases the CGs if the shield is connected to the ground.

This means that we need HV capacitors in the HV part to compensate the over-developed CGs. This solution that is expensive is not analyzed at this stage. On the other hand, if the shield is connected to the HV, the CHVs extremely increase. Although it can be compensated by tuning and obtaining the best CBT, the frequency behavior will be worsened, as the CHVs increases too much giving rise to a peak or a sag in the VD frequency behavior when using the best CBT.

In order to deepen this problem, the case Z.3 is modelled with a long shield connected to the LV potential. The frequency behavior of the case Z.3, displayed in Fig. 3.102, shows that the additional CHVs created by the long shield produce an extreme sag in the frequency response, which cannot be compensated with a CBT.

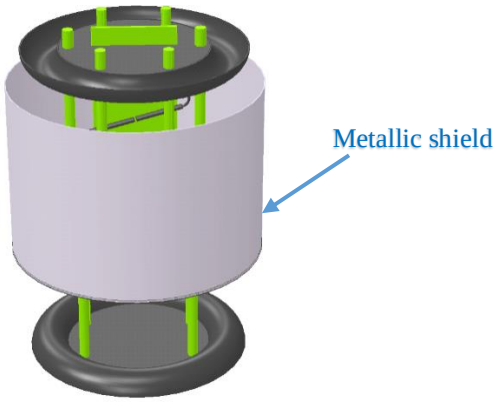


Fig. 3.101. The case Z.3 with a long shield

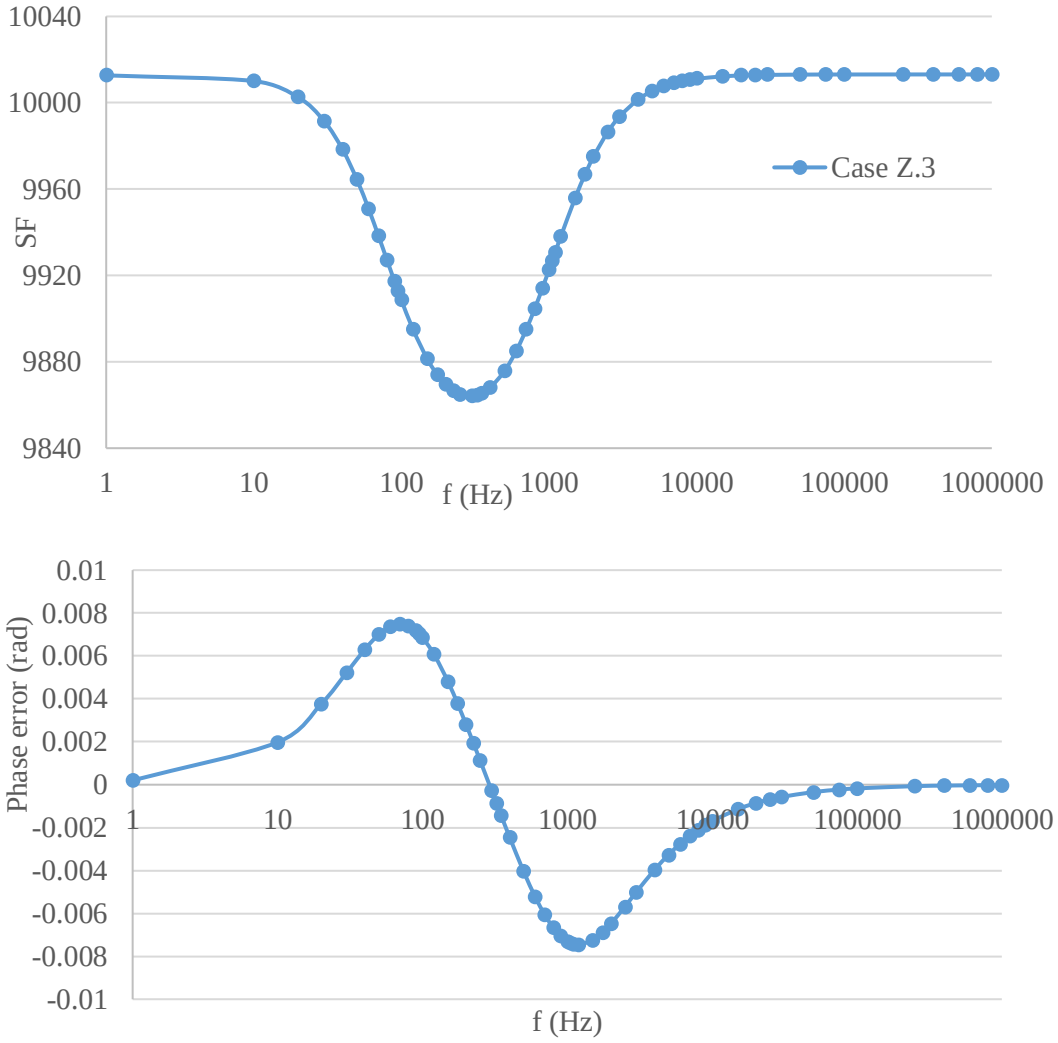


Fig. 3.102. Frequency behavior of the case Z.3 with a long LV-connected shield

In order to decrease the size of the zig-zag RVD, the case Z.5 is introduced, where parameters #d2, #d3, #d4, and #d5 are decreased by 10mm with respect to the case Z.1. This operation makes the HV electrodes closer to each other, probably causing more CHVs. On the other hand, the CGs should not increase much compared to the CHVs, as the distances between HV electrodes are much lower than the distance between the ground and HV electrodes. In order to have the best ratio between CHVs and CGs, the CGs should also increase. Then the case Z.6, having the same geometry of the Z.5 but lower #dG, is modelled. In this way, the CG can slightly increase to compensate the increased CHV. However, the electric field should be also investigated, as the lower

distances can produce electrical field hot spots. The results of both cases Z.5 and Z.6 are presented in Fig. 3.103. The electrical field distribution of the cases Z.5 and Z.6 are displayed in Fig. 3.104.

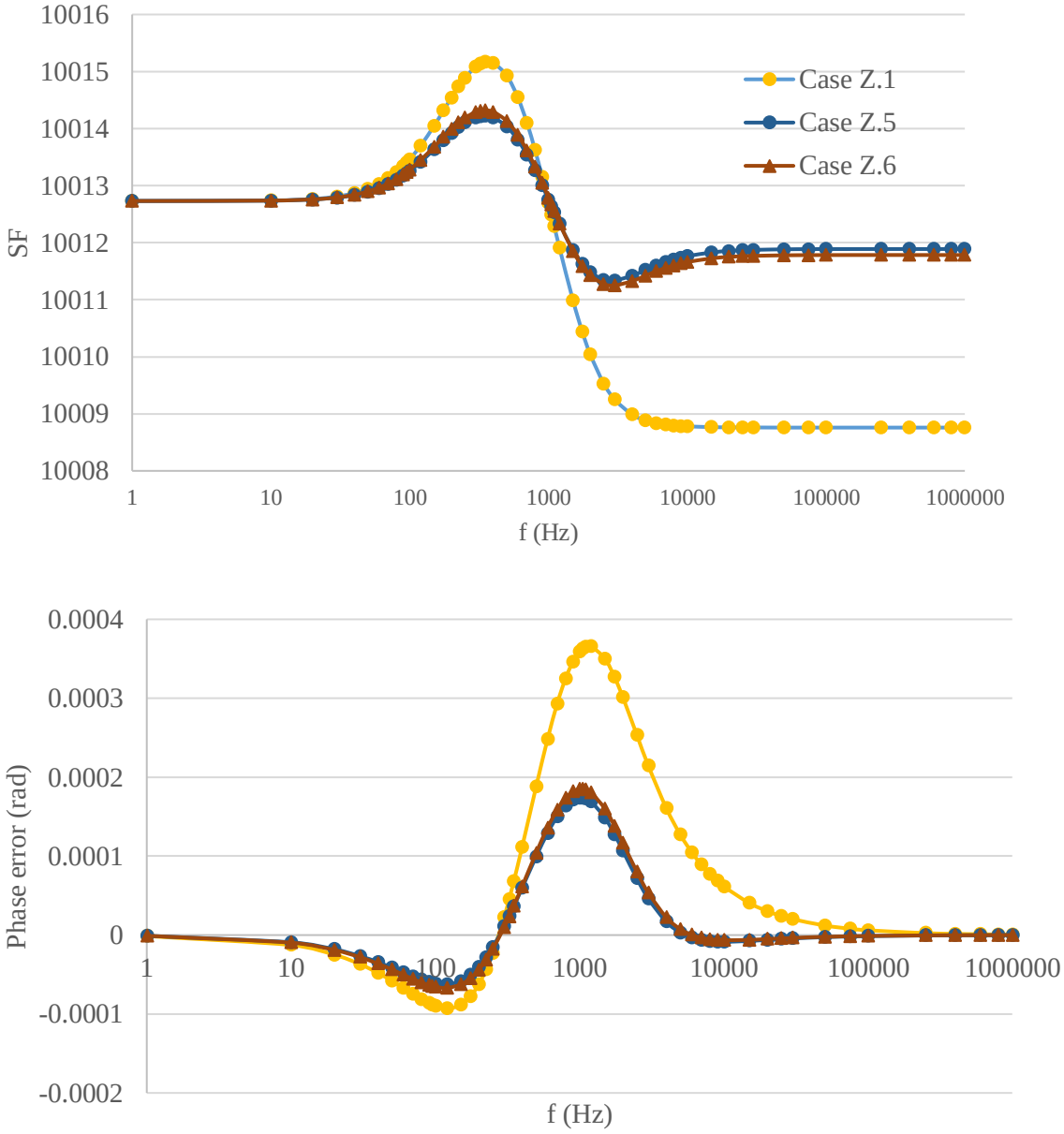


Fig. 3.103. Frequency behavior of the cases Z.5 and Z.6 with lesser height compared to the case Z.1

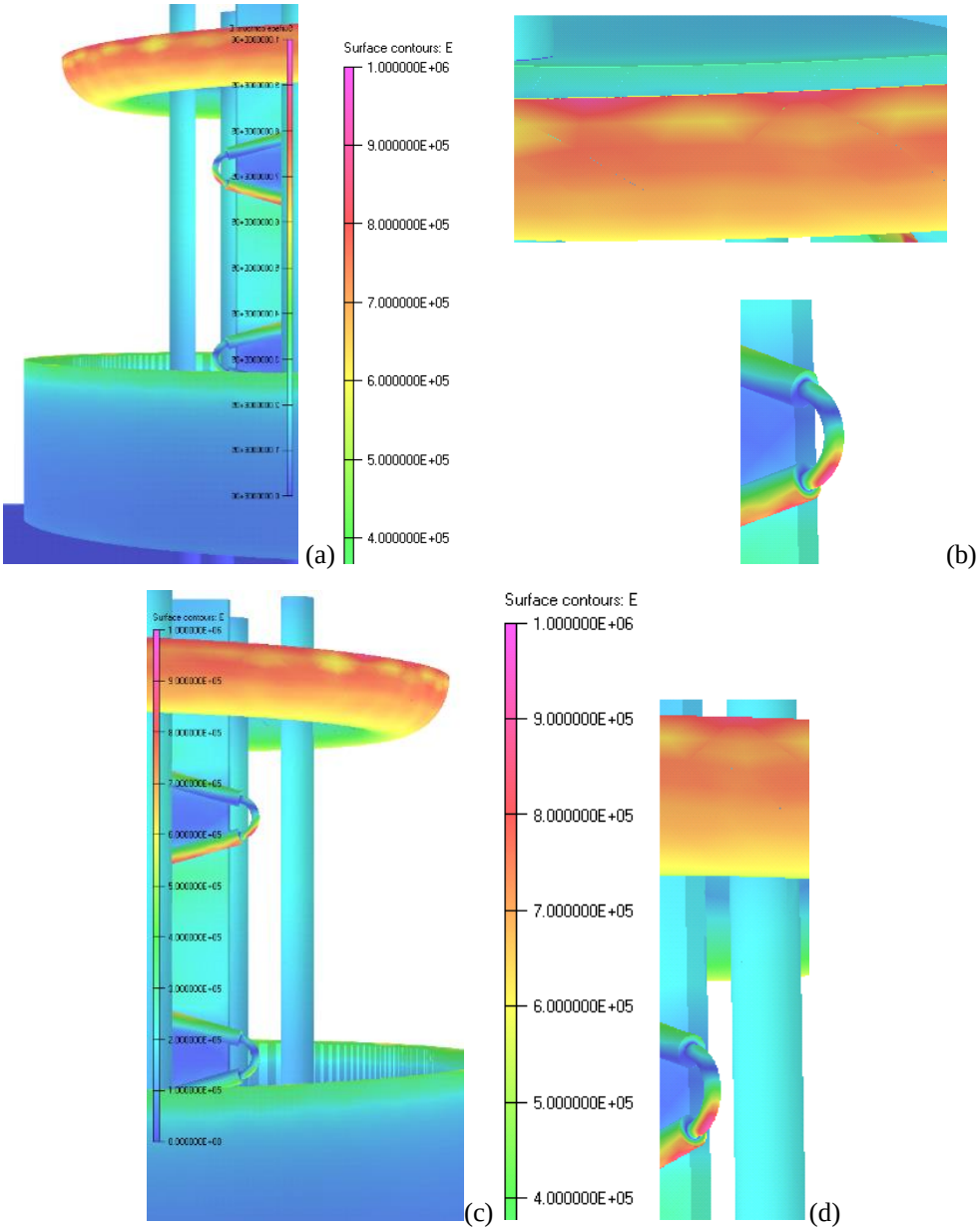


Fig. 3.104. Electrical field distribution in the Case Z.5 (a)overall (b) zoom in hot spots, and in Z.6 (c) overall (d) zoom in in hot spots

As seen in Fig. 3.103, the frequency behavior of both cases Z.5 and Z.6 are perfectly meeting the requirement of a reference voltage transducer. However, the electrical field hot spots (as in Fig. 3.104) appear not only on inner copper but also on the HV plate curvature, which should be carefully considered in realization step as a near grounded proximity can increase the value of the electrical field hot spot.

In order to reduce the total height of the RVD, the parameters #d2, #d3, and #d4 are reduced to 50mm and the parameter #d5 is decreased to 35mm in cases Z.7, Z.8, Z.9 and Z.12. At the same time, the shield height is also changed in all four mentioned cases with the aim of investigating the optimum height of the LV-connected shield. The detailed dimensions of mentioned cases are presented in Table 3.7. Frequency responses of cases Z.7, Z.8, Z.9 and Z.12 with different shield heights are presented in Fig. 3.105. The electrical field strength in four cases Z.7, Z.8, Z.9 and Z.12 are shown in Fig. 3.106. The maximum electric field is always lower than 1.1 kV/mm, a value acceptable to avoid the corona effect in the VD.

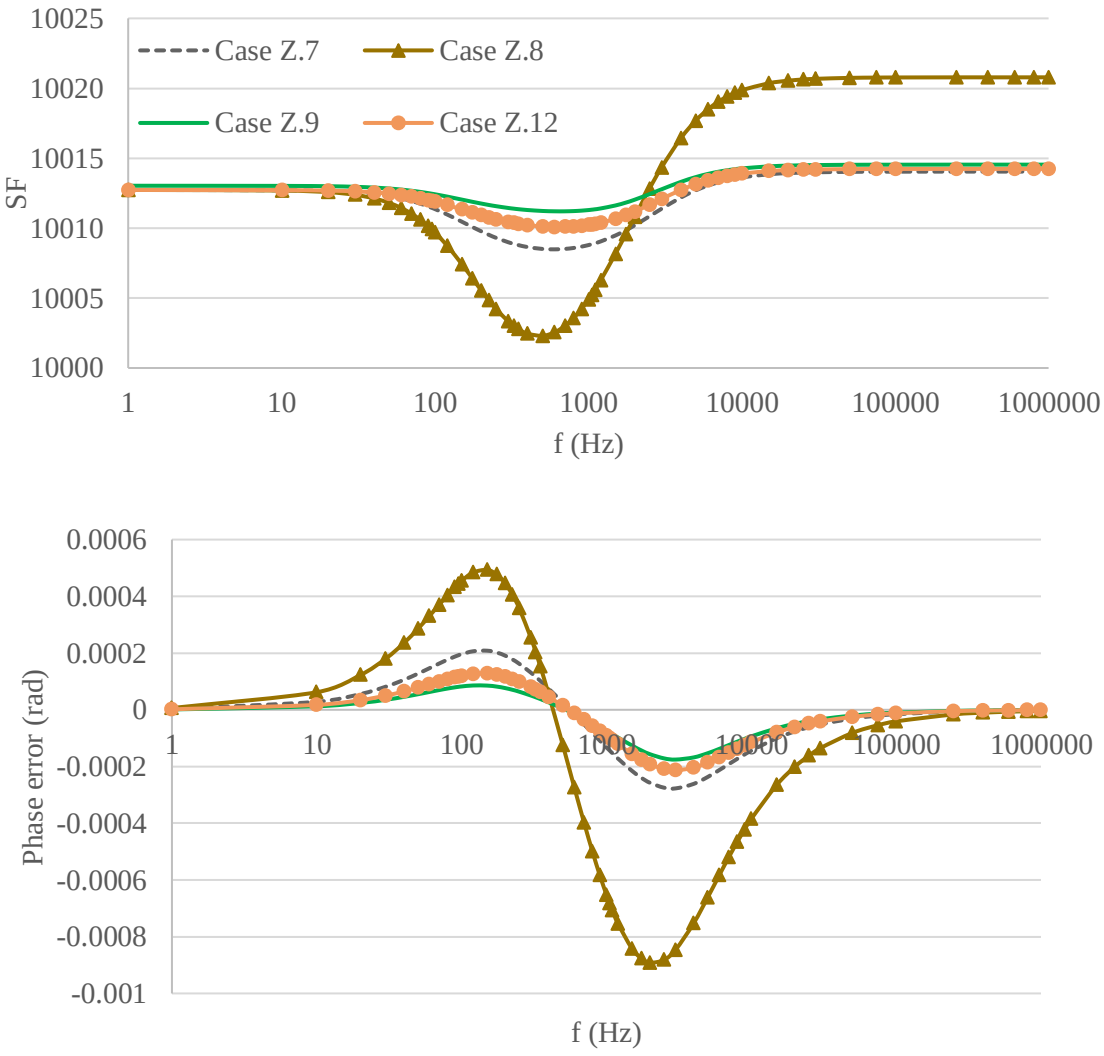


Fig. 3.105. Frequency responses of cases Z.7, Z.8, Z.9 and Z.12 with different shield height

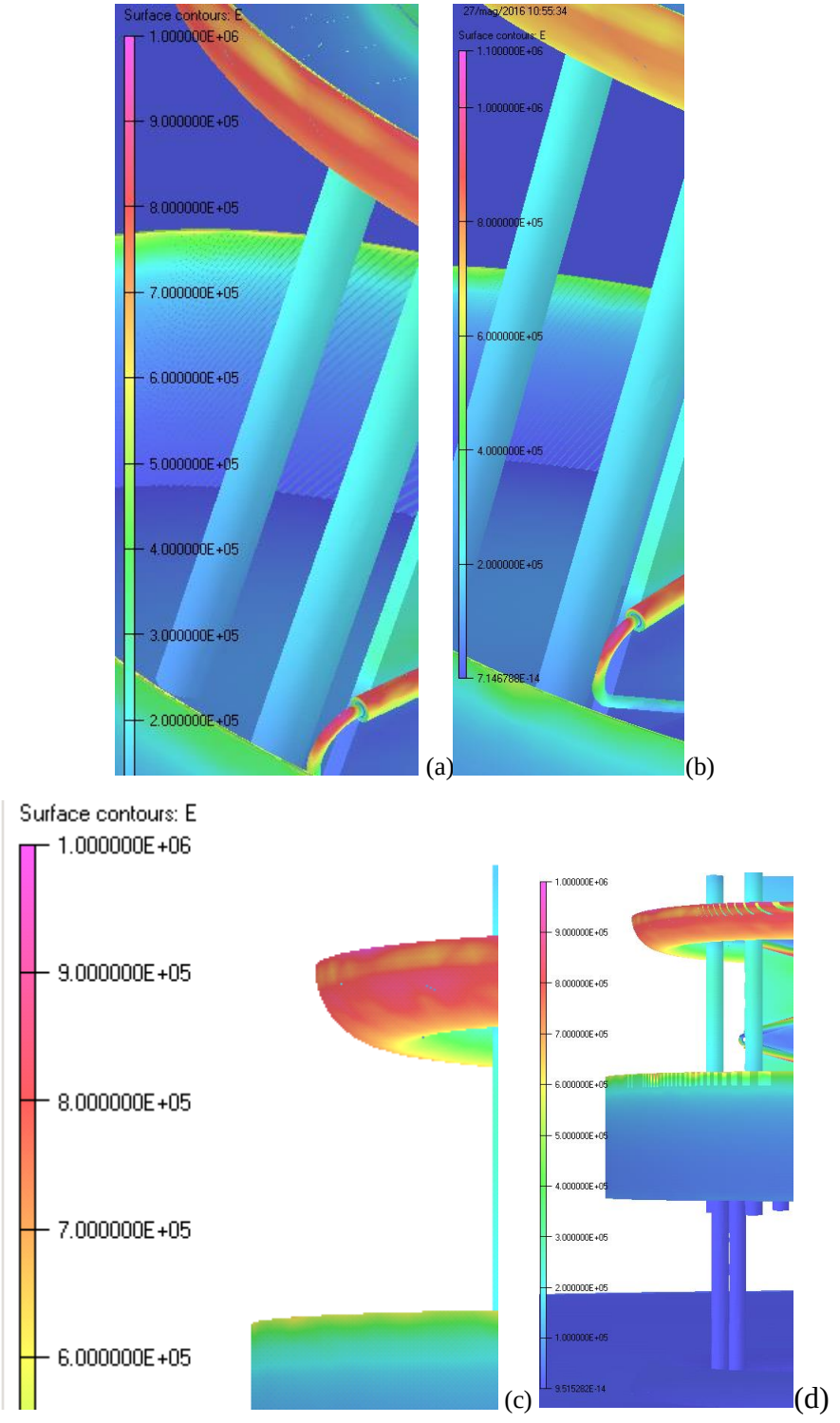


Fig. 3.106. Electric field strength in cases (a) Z.7 (b) Z.8 (c) Z.9 (d) Z.12

The results of Fig. 3.105 put in evidence that the optimum shield height is about 120 mm. Considerable deviation from this value worsens the frequency response of the zig-zag RVD.

3.8.3 Proximity effect on zig-zag RVD

In this section, an object of equal size of the zig-zag RVD is introduced in order to investigate the proximity effect on the case Z.9 with and without considering HV feeding section. To begin with, the case Z.9.2 is modelled exactly like the model Z.9, but without the HV bus bar. Then, a grounded object with the almost same volume of the case Z.9 is put near the zig-zag RVD to study the proximity effect. The distance between the object and zig-zag RVD is assumed to be 500 mm in case Z.9.3 (shown in Fig. 3.107) and 250 mm in case Z.9.4 (shown in Fig. 3.108).

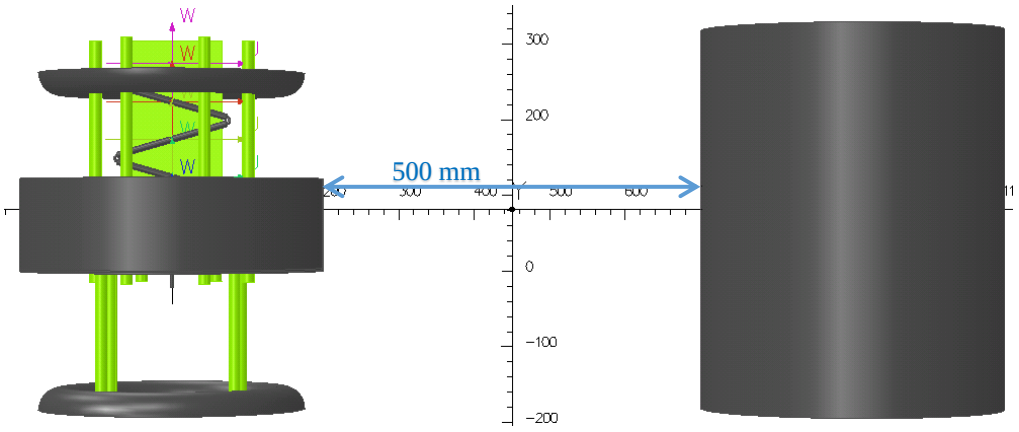


Fig. 3.107. The case Z.9.3 with the grounded object in 500mm distance

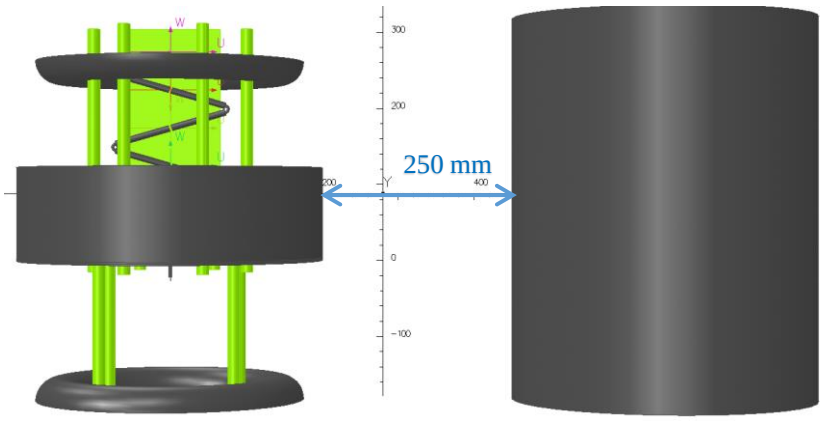


Fig. 3.108. The case Z.9.4 with the grounded object in 250mm distance

The result of the case Z.9.2 (without HV feeding section) is given in Fig. 3.109. As already seen in Fig. 3.99, the HV feeding section substantially affects the frequency

behavior of the zig-zag RVD, for a fixed value of CBT. However, the modification of the CBT, according to the laboratory condition and environment can again give an appreciable frequency response. The result of the case Z.9.2 with the modified CBT is displayed in Fig. 3.110.

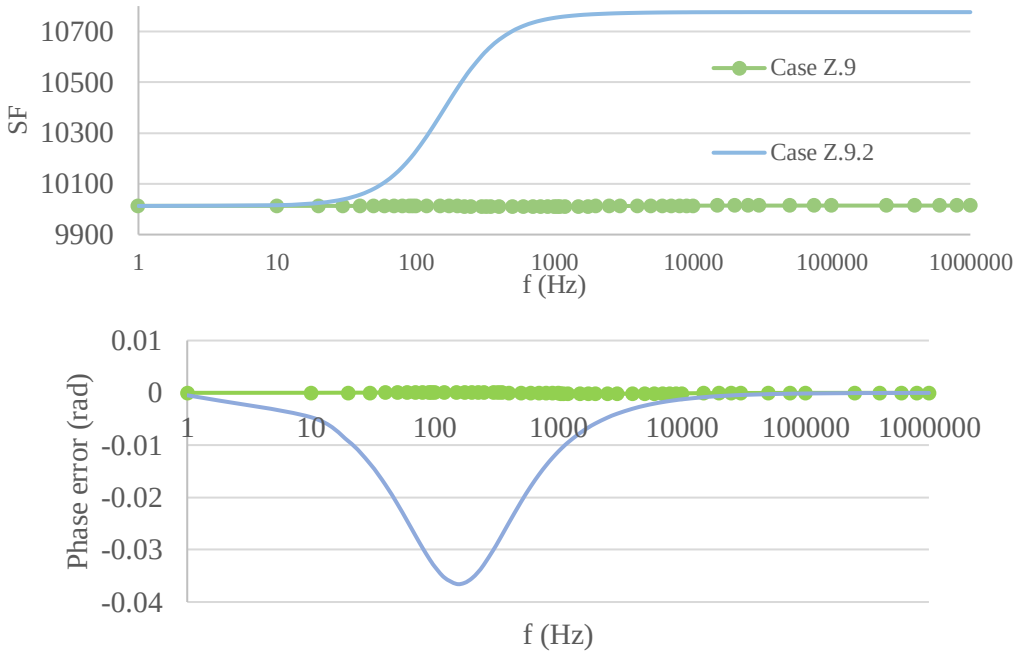


Fig. 3.109. Frequency responses of the case Z.9.2 and Z.9 with same CBT

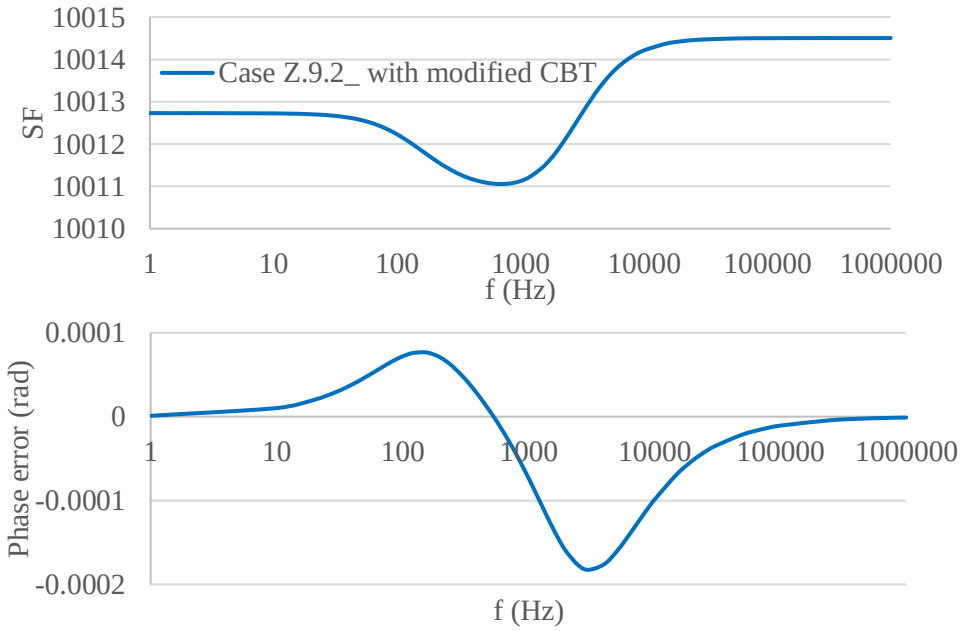


Fig. 3.110. Frequency responses of the case Z.9.2 with modified CBT

As clear in Fig. 3.110, the case Z.9.2 can still have the features of a reference voltage transducer, provided that the CBT is modified according to the laboratory condition.

As mentioned previously, the cases Z.9.3 and Z.9.4 are simulated in presence of an object near to the zig-zag RVD. The results are shown in Fig. 3.111.

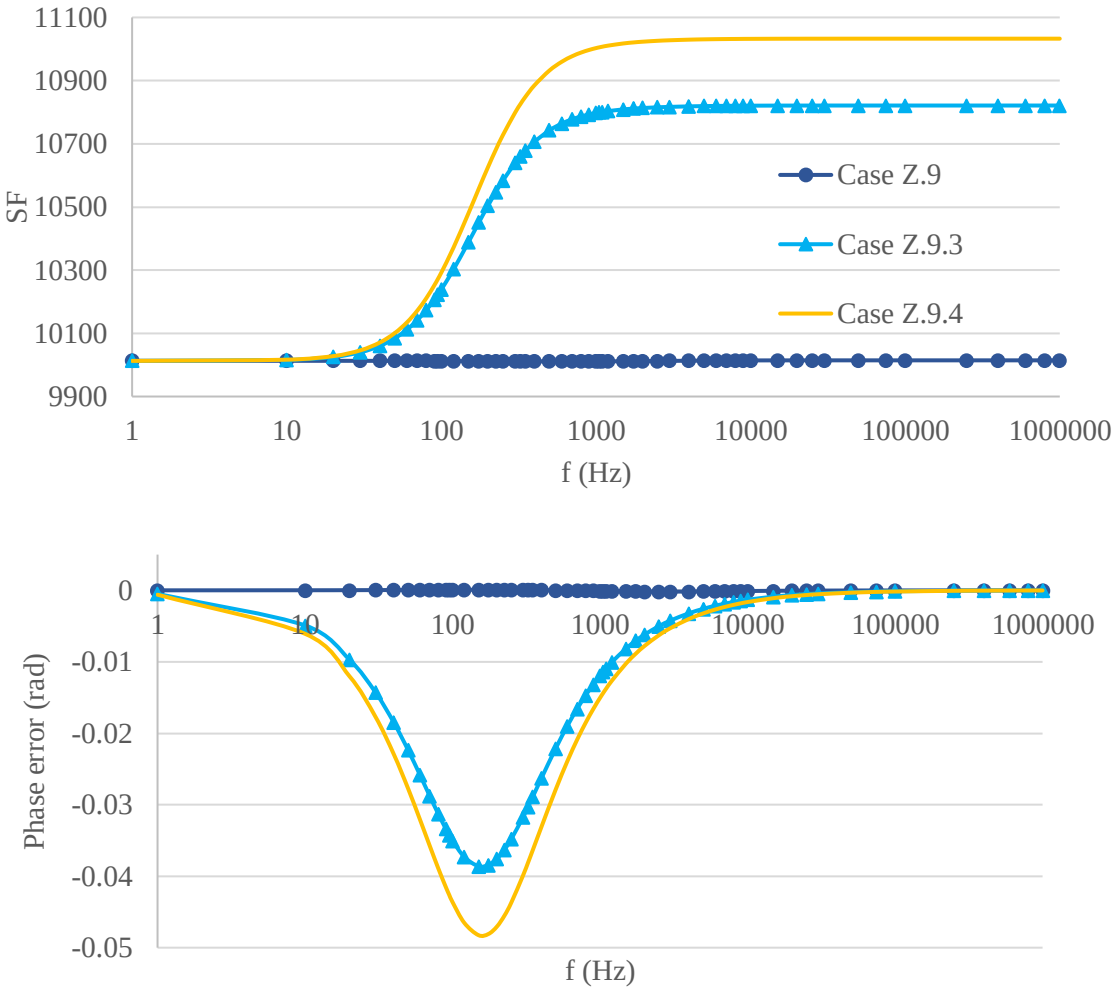


Fig. 3.111. Frequency responses of the case Z.9.3 and Z.9.4 with same CBT as the one in case Z.9

The CBT in cases Z.9.3 and Z.9.4 is again modified to investigate whether a proper frequency response can be achieved in the case of proximity objects near to the zig-zag RVD or not. This investigation results are shown in Fig. 3.112.

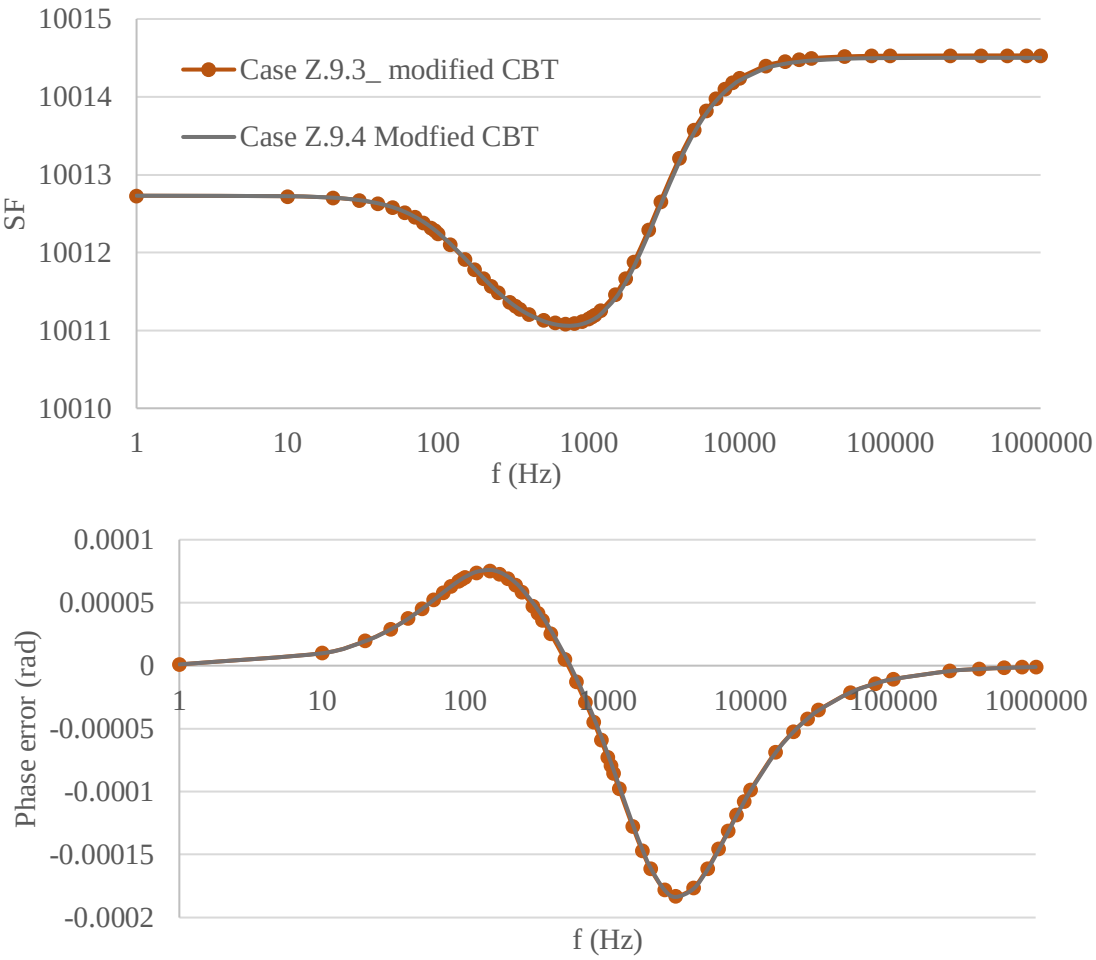


Fig. 3.112. Frequency responses of the case Z.9.3 and Z.9.4 with modified CBT different from the one in case Z.9

The results given in Fig. 3.112 prove that an acceptable frequency response is possible even with an object (with the same size as the RVD) near to the zig-zag RVD.

Cases Z.9.5 and Z.9.6 maintain the geometry of the case Z.9, but the parameter #a (case Z.9.5) and the parameter #b (case Z.9.6) are assumed to have the value of 200 mm. The position of zig-zag RVD is changed with respect to the HV bus bar in cases Z.9.5 and Z.9.6, in order to study the effect of the displacement of the RVD. The frequency responses for Z.9.5 and Z.9.6 are presented in Fig. 3.113 with the same CBT value as the of the case Z.9.

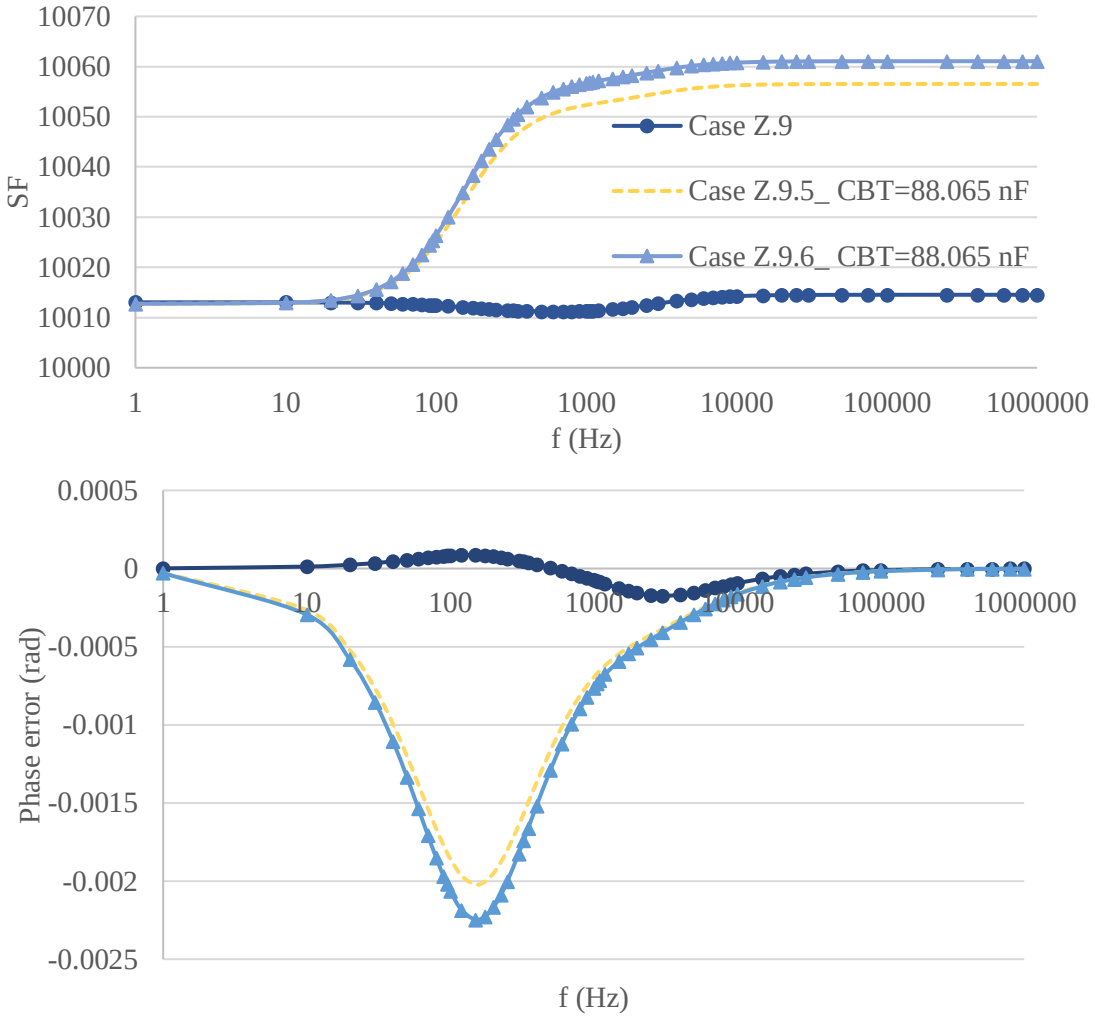


Fig. 3.113. Frequency responses of the case Z.9.5 and Z.9.6 with same CBT equal to the one in case Z.9

The results of zig-zag RVD with displacement of the HV bus bar show that the frequency behavior depends on the HV bus bar position as a proximity object. However, the results confirm that a small displacement could be acceptable for a general voltage transducer. As defined in the IEC technical report [7] and also in the standard [8], a general voltage transducer could have a 1% maximum deviation from the rated SF and maximum phase error of 18 mrad. On the other hand, the zig-zag RVD models, as Z.9.5 and Z.9.6, need a modified CBT in order be considered as a reference voltage transducer. The results of the models Z.9.5 and Z.9.6 with adjusted CBT are shown in Fig. 3.114.

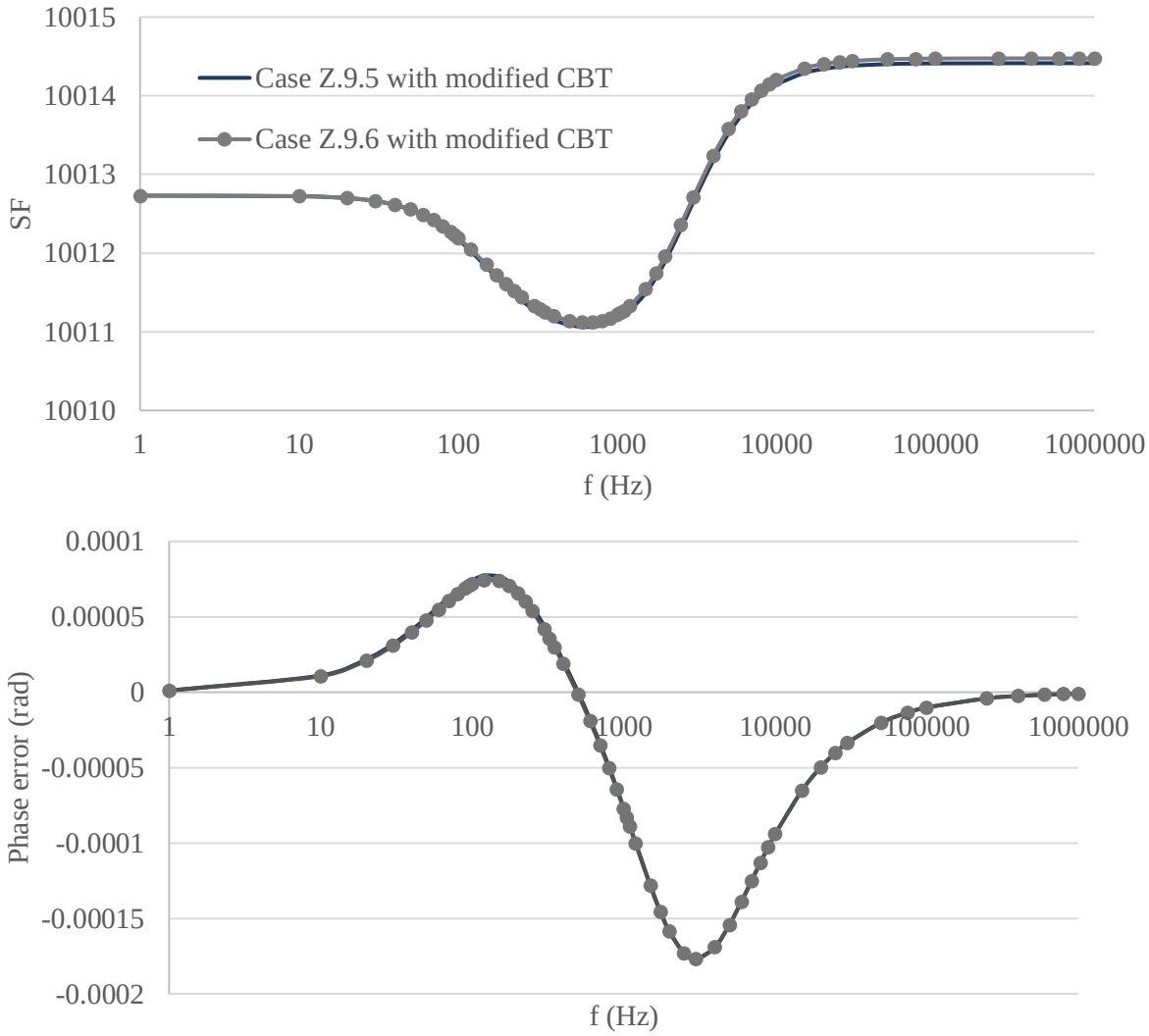


Fig. 3.114. Frequency responses of the case Z.9.5 and Z.9.6 with CBT different from the one in case Z.9

The frequency behavior of cases Z.9.5 and Z.9.6 (Fig. 3.114) justifies that a satisfactory frequency response can be reached even after displacement of the zig-zag RVD.

3.8.4 Reducing the size of the zig-zag RVD

With the purpose of having a smaller reference zig-zag RVD, the parameters #d2, #d3, and #d4 are decreased from 50 mm in the case Z.7 (one of the models showing a satisfactory result) to 47 mm (case Z.10). Consequently, the angle of the HV resistors with the horizontal axis (parameter #α) will decrease from 16 to 14 degree and the total height of zig-zag RVD reduces by about 9 mm. The result of the case Z.10 is presented

in Fig. 3.115. The electrical field strength should be also investigated, as the modification in the dimensions can change the hot-spot value. The electrical field hot-spot of case Z.10 is shown in Fig. 3.116.

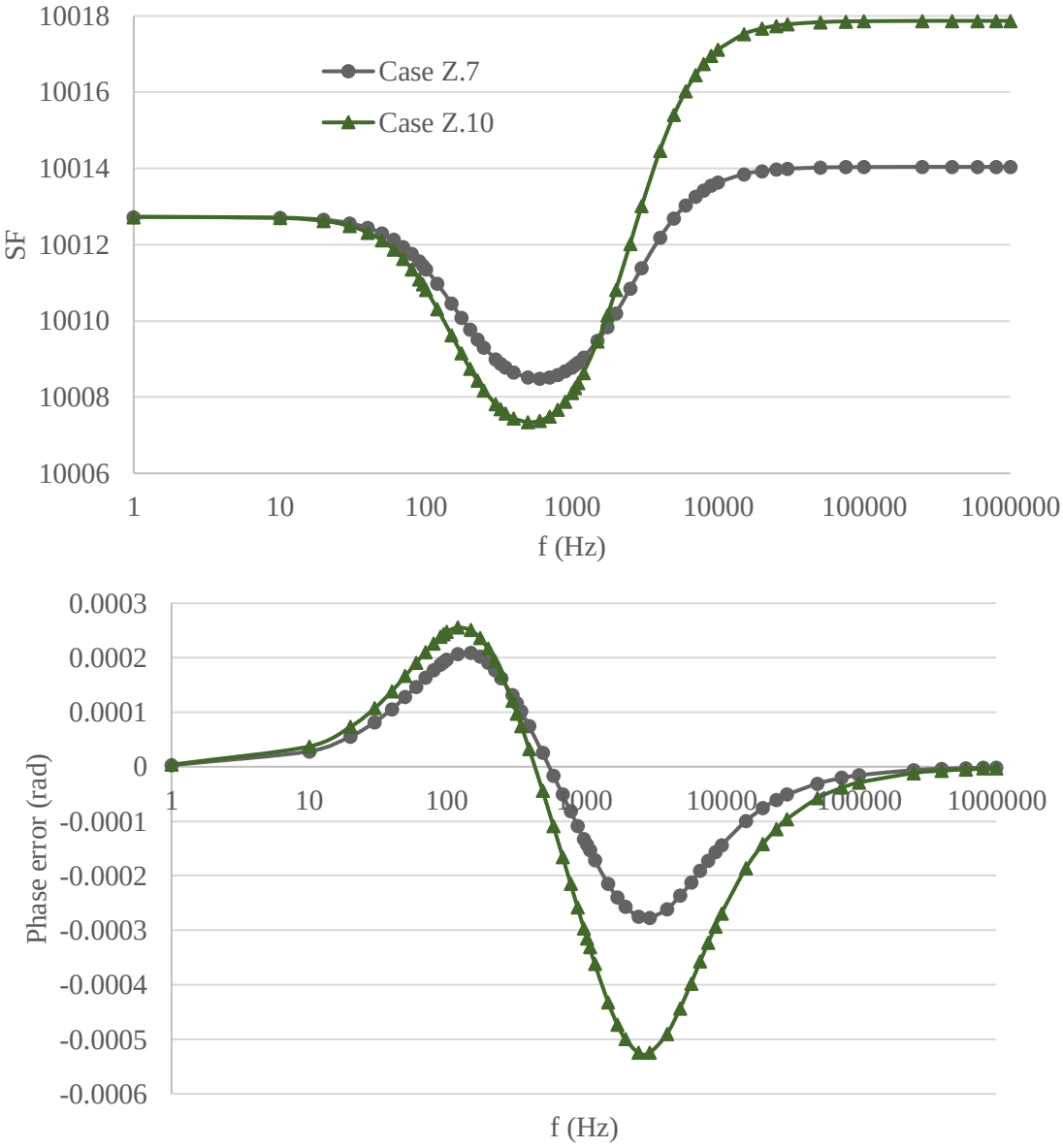


Fig. 3.115. Frequency response of the case Z.10

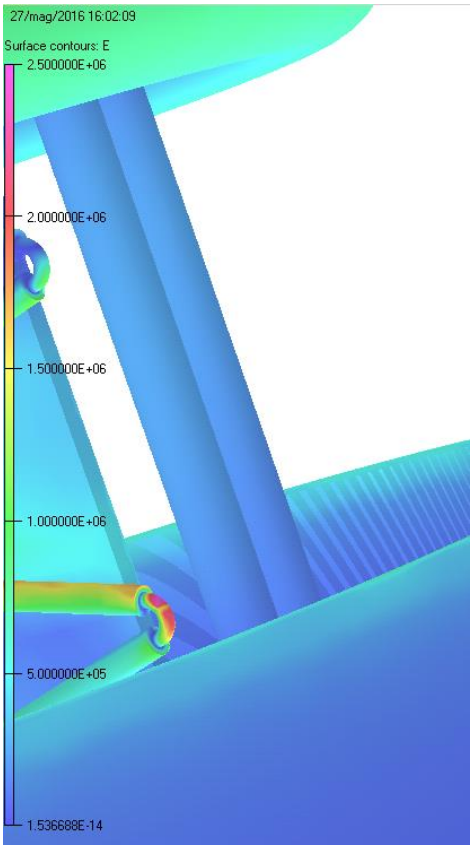


Fig. 3.116. Electrical field hot-spot in the case Z.10

As clear in Fig. 3.115, the reduction of the distances between HV resistors worsens the frequency response of the zig-zag RVD. The reason is that a reduced distance of the HV electrodes from each other changes the CHVs and consequently the ratio of CHV to CG. At the same time, the electrical field hot-spot is increased, as a lower angle between the HV resistor and the horizon direction makes the copper edge sharper.

On the other hand, the voltage drop between different HV electrodes remains unchanged, while the distances between HV electrodes decreases, so that the electrical field hot-spot values are increased as shown in Fig. 3.116.

Up to now, cases Z.9 and Z.12 have shown the best results. In order to investigate the feasibility of decreasing the volume of the zig-zag RVD, the radius of both LV shield and the middle plate is reduced from 200 mm (case Z.12) to 180 mm (case Z.13). The frequency behavior and the electrical field hot-spot are shown in Fig. 3.117 and Fig. 3.118, respectively.

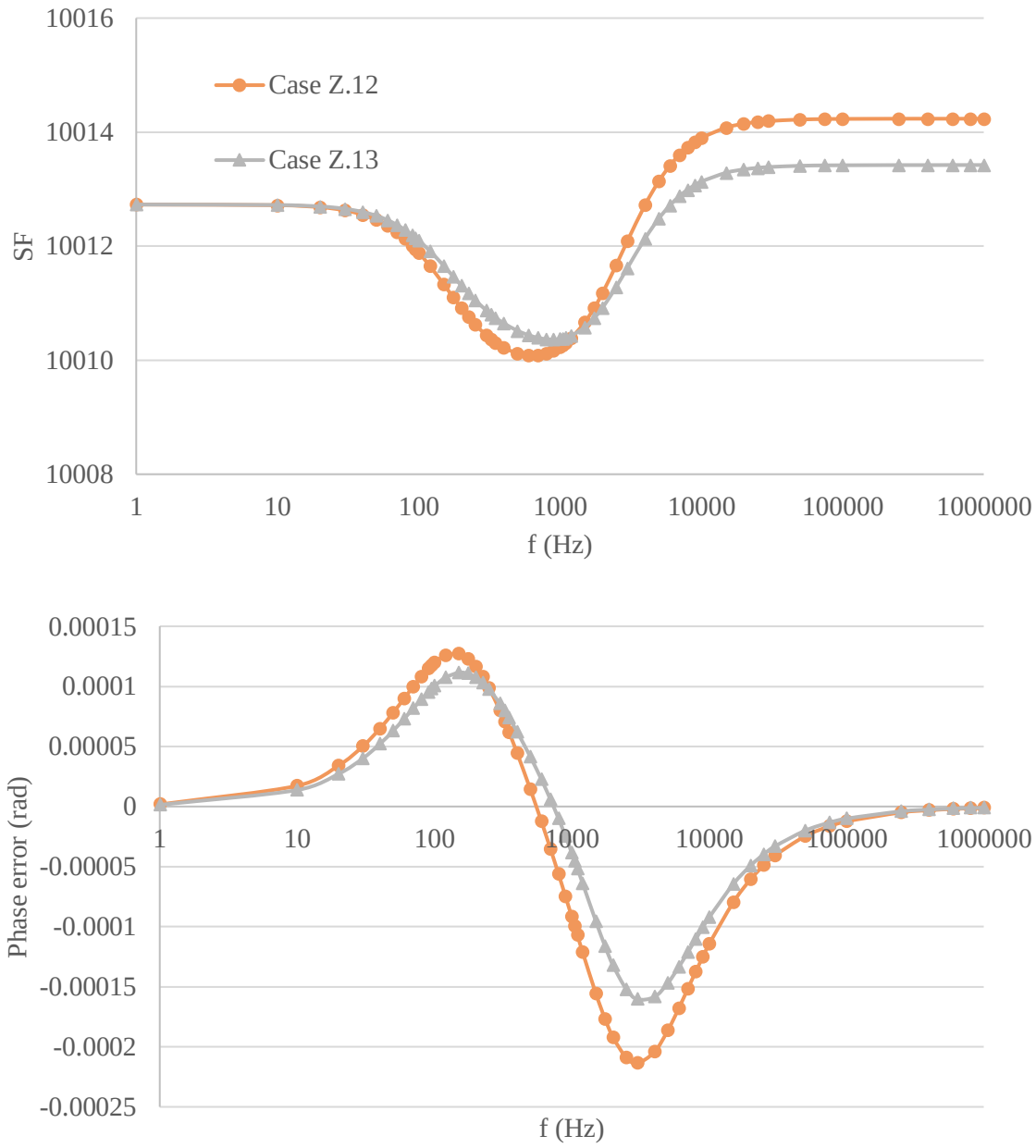


Fig. 3.117. Frequency response of the case Z.13

As can be seen from Fig. 3.117, decreasing the radius of the shield and the middle plate from 200 mm (case Z.12) to 180 mm (case Z.13) does not modify the frequency response and it still could be considered as a reference voltage transducer.

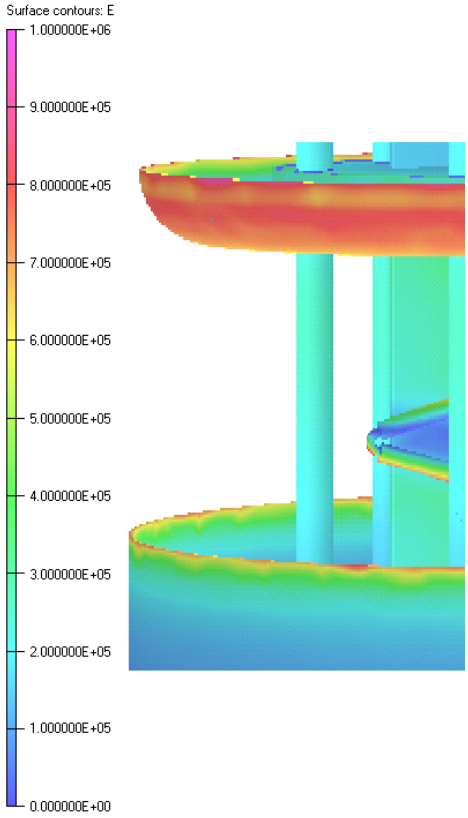


Fig. 3.118. Electrical field hot-spot in the case Z.13

However, reducing the radius of the shield causes the shield to be closer to the HV part of the RVD, so that the E_{max} starts to appear on the shield edge as shown in Fig. 3.118.

3.8.5 The effect of HV-connected shield on behavior of the zig-zag RVD

In order to decrease the proximity effect of the behavior of the zig-zag RVD, the electrical field coupling between the inner electrodes and outside proximity should be minimized or fixed. For such a purpose, in case Z.14 an HV-connected shield (with the height of 89 mm) is put at the top of the zig-zag RVD, while the LV-connected shield is also present. The size and geometry of the case Z.14 is similar to the case Z.9 except the HV shield which is only present in case Z.14. Detailed dimensions of the shields are given in Table 3.7. In case Z.14.2, the RVD is displaced 200 mm (with respect to the position of the case Z.14) in direction of the HV bus bar (the parameter #a is chosen 200 mm). Frequency responses of both cases are shown in Fig. 3.120.

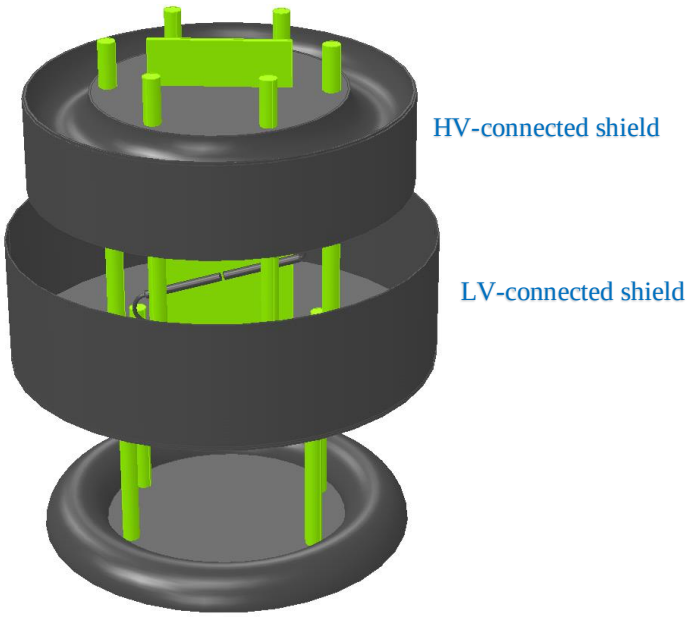


Fig. 3.119. FEM model of the case Z.14 with both LV-connected and HV-connected shields (HV shield height= 87 mm)

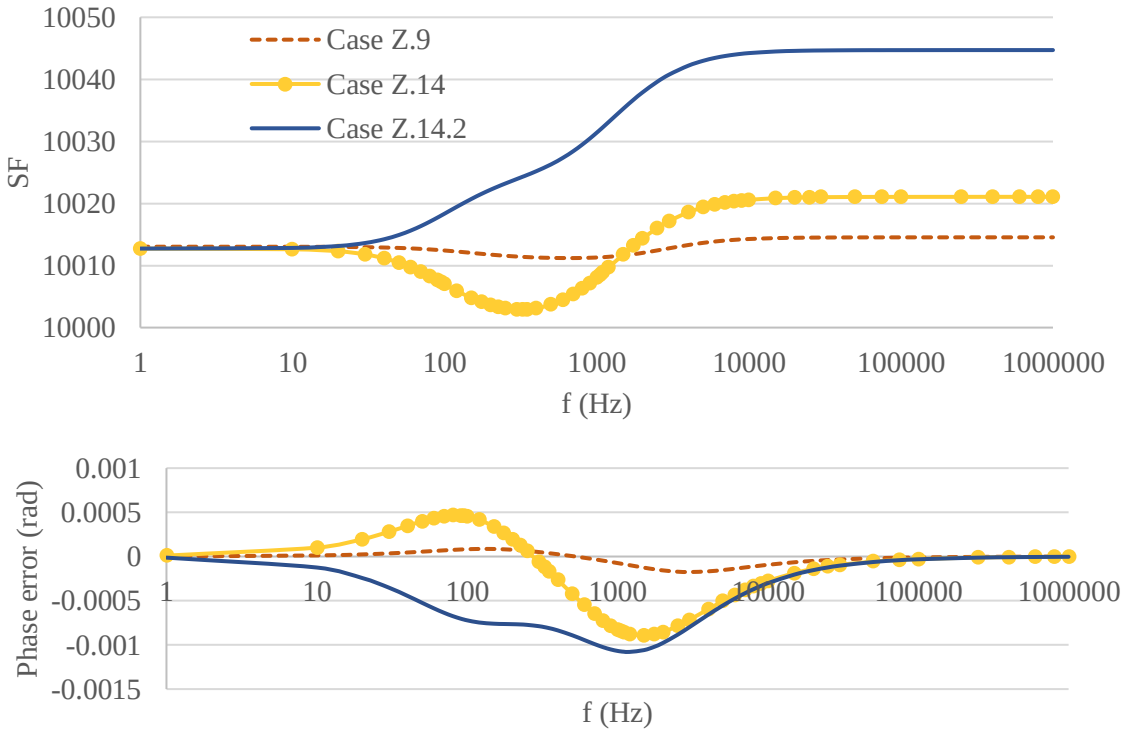


Fig. 3.120. Frequency response of the cases Z.14 and Z.14.2 (with the same CBT)

Fig. 3.120 shows that the addition of an HV-connected shield can reduce the proximity effect on the zigzag-RVD behavior. Besides, the maximum phase error is still 100 times lower than the range of limits defined in [7] and [8]. However, SF is not favorable any more, and the proximity effect is still considerable and not acceptable for a reference voltage transducer. In addition, the electrical field hot-spots (about 1.2 kV/mm) arise not only on the copper curvature, but also on the shields edges with potential risk of corona effect.

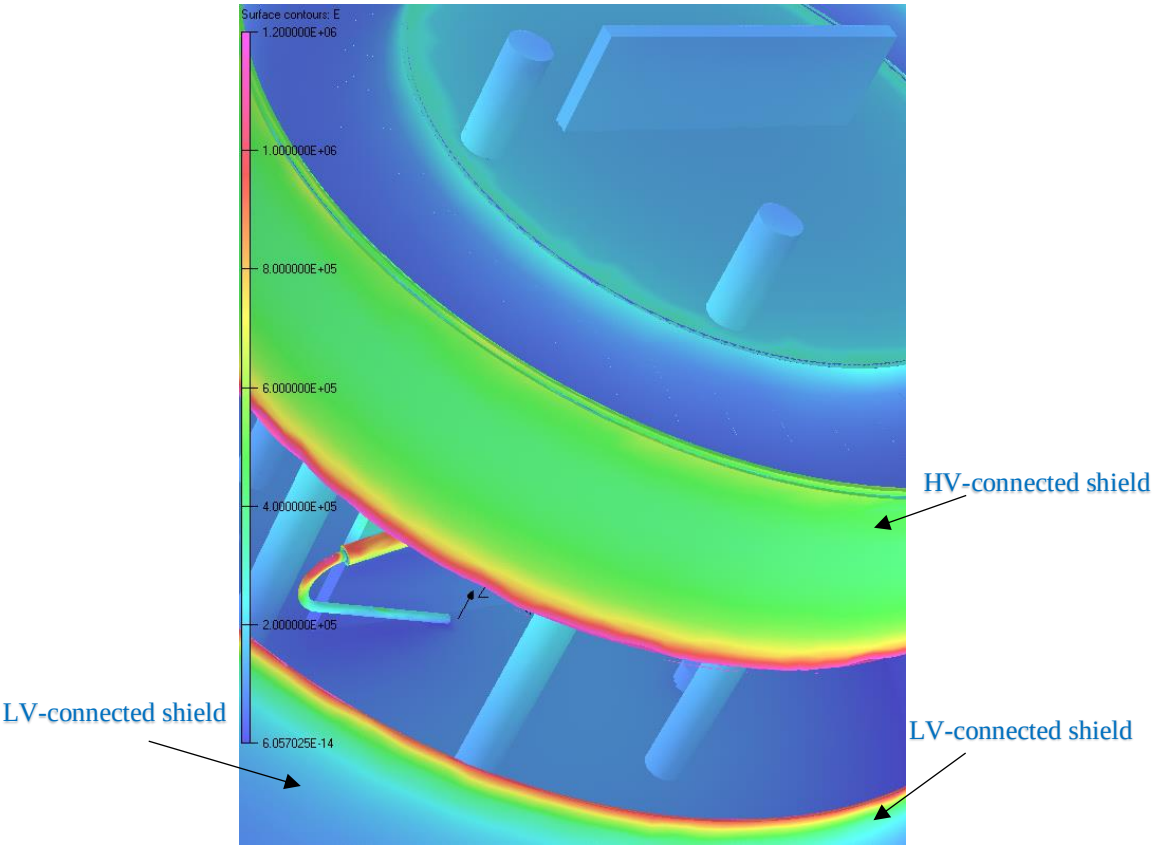


Fig. 3.121. Electrical field hot-spot in the zig-zag RVD with both LV-connected and HV-connected shields

In order to improve the previous investigation on case Z.14, the case Z.15 with “taller” HV-connected shied (height of 137mm) is modelled to study the possibility of having a zig-zag RVD with a small sensitivity versus the proximity effect. The case Z.15 model is shown in Fig. 3.122. As it can be seen, the HV and LV shields are quite close to each other, introducing a major problem in terms of electrical field hot-spot and corona effect. In spite of the previous concern, the semi-closed (the HV side is approximately isolated from the outside of the RVD) zig-zag RVD (case Z.15) is simulated and the results are

presented in Fig. 3.123. Although the phase error shows a promising outcome, the SF is not acceptable for a reference voltage transducer. The result of case Z.15.2 with 200 mm displacement is also presented in Fig. 3.123. The proximity effect is significantly lower and results are in the range of 0.1% for 200 mm displacement of the RVD, but it is still high for a reference voltage transducer. The comparison of the stray capacitance matrices (in cases Z.14, Z.14.2, Z.15, and Z.15.2) proves that the stray capacitances between different electrodes do not change substantially, except the capacitance between the LV shield and the HV section. This issue is occurred because the LV shield is openly exposed to the outside environment.

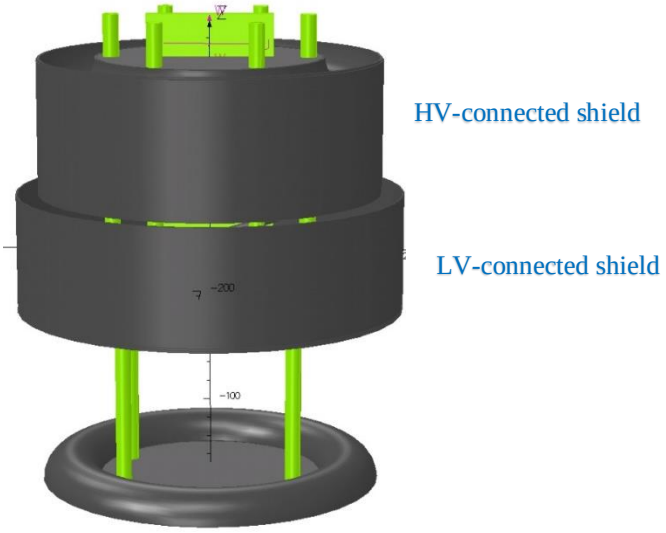


Fig. 3.122. FEM model of the case Z.15 with both LV-connected and HV-connected shields (HV shield height= 137 mm)

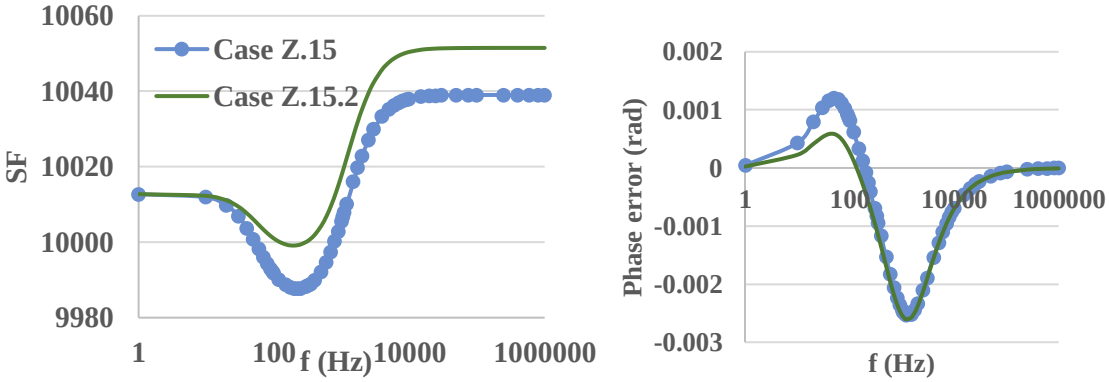


Fig. 3.123. Frequency response of the cases Z.15 and Z.15.2 (with the same CBT)

3.8.6 Effect of distance between the ground and the middle plate (in presence of HV shield)

The distance between the ground and middle plate (parameter #G), when there is no HV-connected shield, should be as high as possible to reduce the CGs. Then, the best CHV could be found by changing the LV shield's height to obtain an acceptable frequency response. On the other hand, the CHVs in the cases with HV shield are greater and the electrical field coupling the ground to the electrodes in the HV part of the RVD are lower. Thus, the CGs are lower in comparison with the ones of the cases without HV shield. Therefore, results for arrangements with HV shield may behave different when changing the parameter #G. In cases Z.17 and Z.18 the geometry is the same as in case Z.15, but with different values of #G. The results are shown in Fig. 3.124.

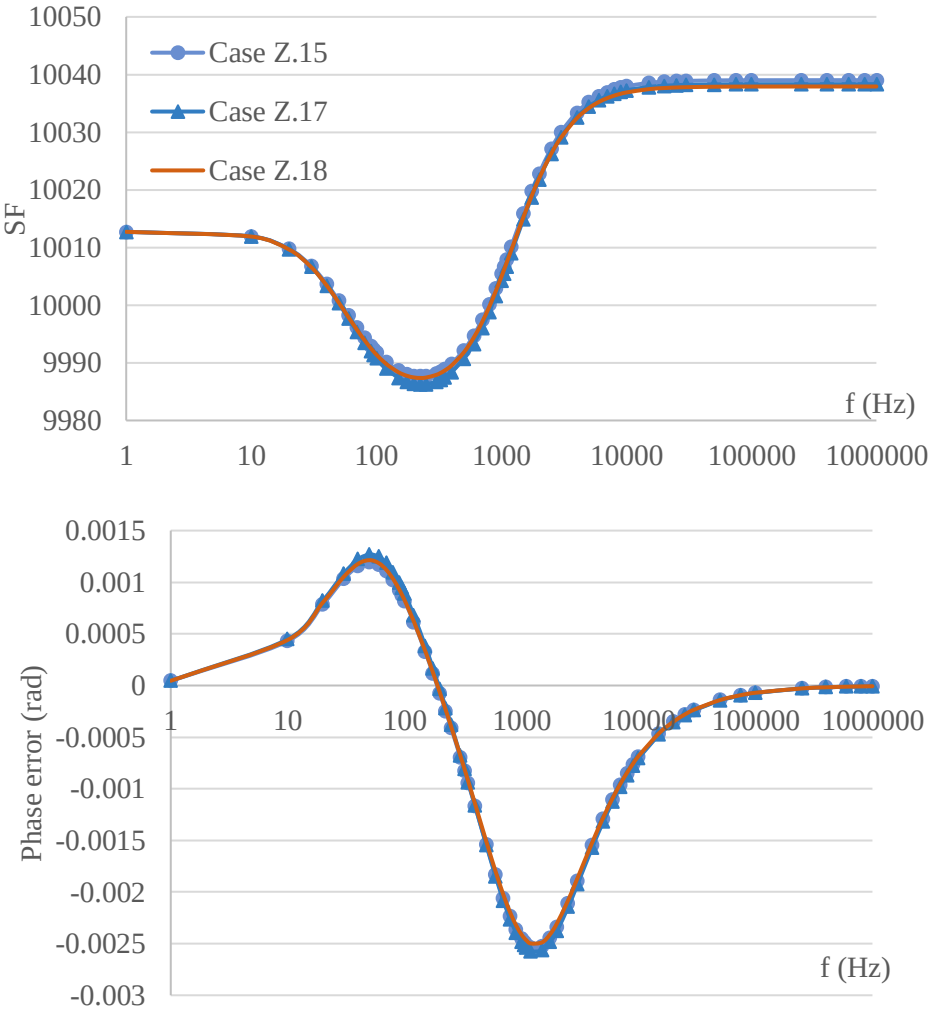


Fig. 3.124. Frequency response of the cases Z.15(#G=160mm), Z.17(#G=100mm), and Z.18(#G=250mm) with different CBTs

As can be found from Fig. 3.124, parameter #G practically does not affect the frequency behavior, because the HV shield causes a better electrical field coupling between electrodes in the HV side (means more CHVs) and reduces the coupling between the ground and the electrodes in the HV side (means less CGs).

The increase of the distance between the middle plate and the ground does not modify significantly the CGs, which remain very small (and also the CHVs remain the same as they are almost well shielded from the other parts).

The cases Z.17 and Z.18 with a displacement of 200 mm are identified as cases Z.17.2 and Z.18.2. The results (with the same CBT) are illustrated in the Fig. 3.125. As expected, according with the results in Fig. 3.123 for the case Z.15, the displacement in both cases with different values of the parameter #G causes different frequency behavior, leading to a situation that does not satisfy the requirements of a reference voltage transducer.

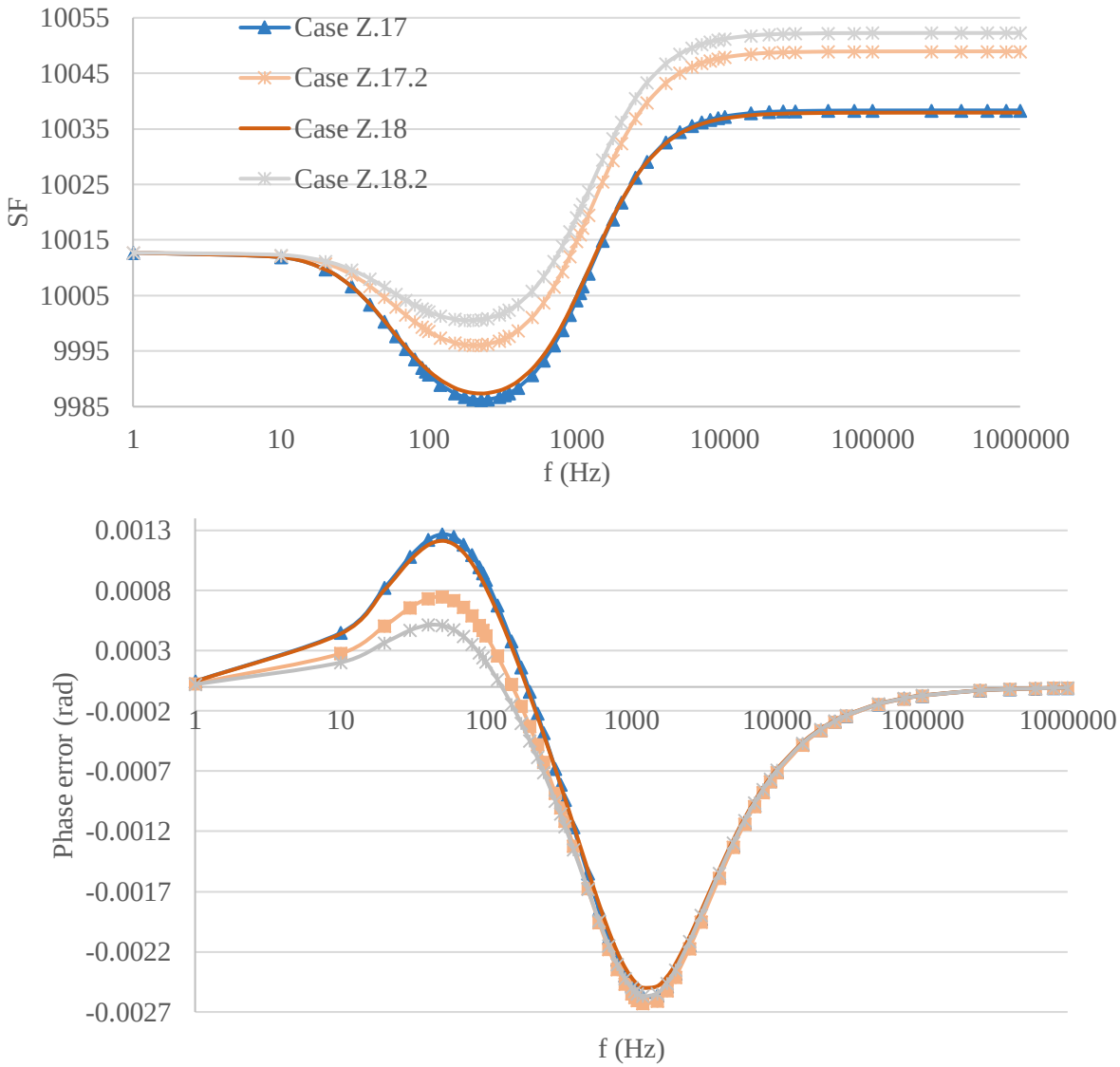


Fig. 3.125. Frequency responses of the cases Z.17, Z.17.2, Z.18, and Z18.2

Even if these arrangements are not satisfactory for a reference voltage transducer, it is worth to mention that the effect of proximity is reduced with respect to the cases without HV shield.

3.8.7 Impact of Grounded shield on proximity sensitivity of the zig-zag RVD

As far as one can see, a stray capacitance between the HV electrodes and the ground cannot change the electrical equivalent circuit of a VD. Then, if a grounded object

approaches the RVD, the change in the stray capacitance between the HV and the ground (parallel capacitance to the input voltage) cannot produce a proximity sensitivity effect. On the other hand, there is evidently a large metallic surface for the LV electrode due the relatively big LV-connected shield compared to other metallic surfaces. Consequently, if a grounded object gets close to the RVD, the stray capacitance between the LV and the ground, which is a type of CG parallel to the output, will be modified and worsens the frequency response of the RVD. In addition, if the position of the RVD changes with respect to the HV feeding section, the stray capacitance between the HV and LV (a type of CHV) will be modified and the frequency response of the RVD get worse.

To isolate the LV shield from the surrounding objects and also from the HV feeding section outside of the RVD geometry, a ground-connected shield shown in Fig. 3.126 is introduced in the geometry of the RVD preserving the electric field distribution and the LV shield from the proximity effect. The new case study (Case Z.20 shown in Fig. 3.126) is modelled only by adding an extra grounded shield to the case Z.15.

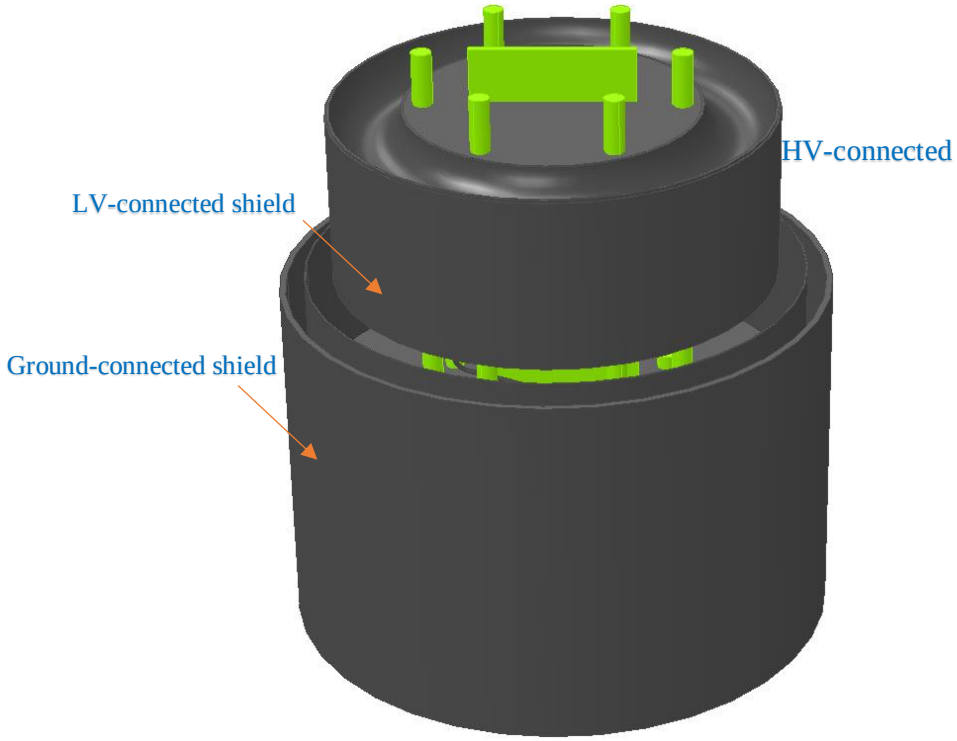


Fig. 3.126. The case Z.20 with three various shields

At first, the result of the case Z.20 should be compared to the one of the Z.15 to check out the effect of adding an extra ground shielding. This investigation is necessary to assess how the frequency behavior varies decreasing the proximity sensitivity. The results of the two mentioned case studies with different CBTs are shown in Fig. 3.127.

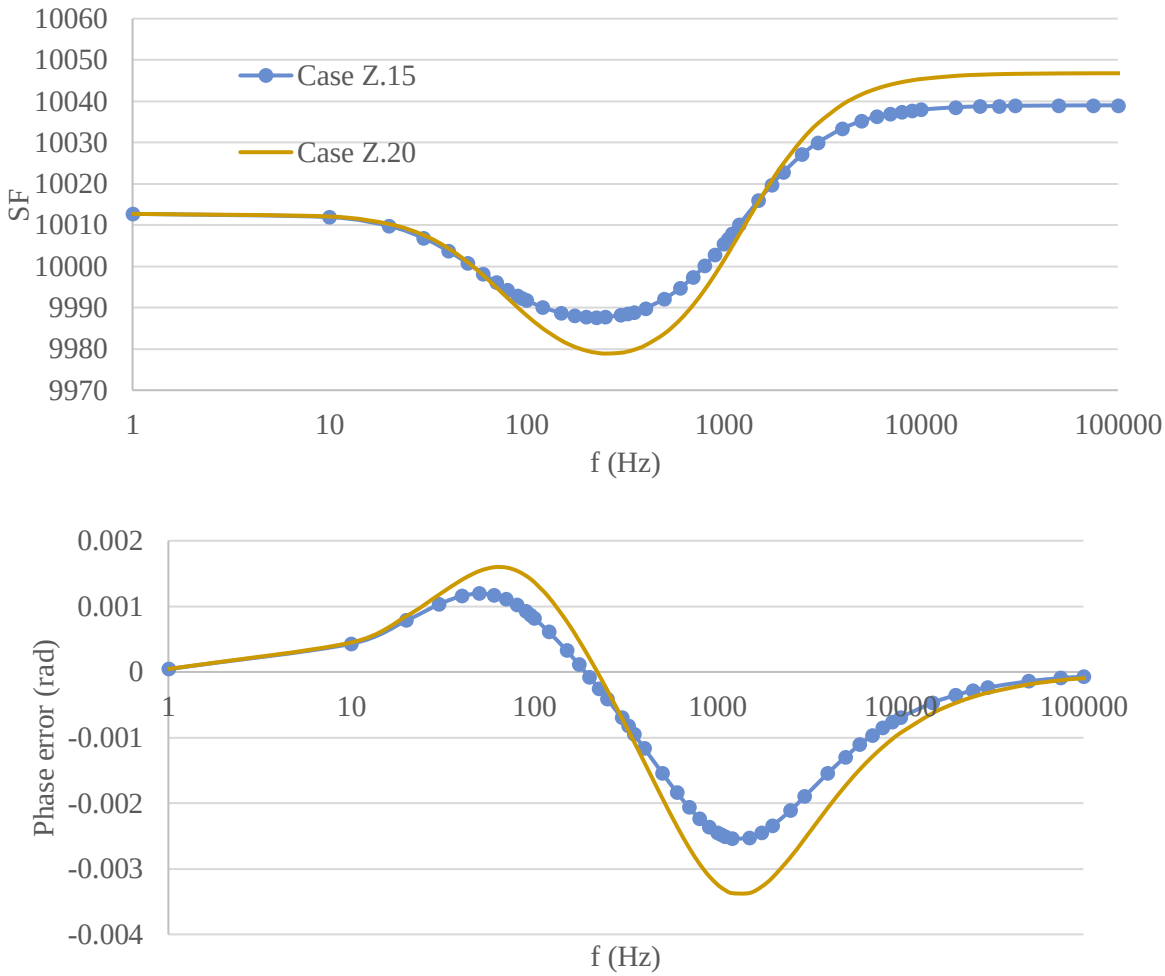


Fig. 3.127. Frequency responses of the cases Z.15 and Z.20

The results presented in Fig. 3.127 are quite promising and indicates that the phase error variation ranges from 2.5 mrad to 3.3 mrad being both very small and acceptable with respect to the requirements of a standard voltage divider. However, the SF variation reached about 7000 ppm that must be reduced. A further analysis with different HV and LV shields is presented in section 3.8.8.

In the next step, the zig-zag RVD (case Z.20) position is displaced with respect to the one of the HV bus bar. The case Z.20 is simulated with the parameters #a=0 and #b=0. Afterwards, the parameter #a is chosen 200 mm and then 400 mm in cases Z.20.2 and Z.20.3, respectively. Later, the cases Z.20.4 and Z.20.5 are simulated with #a=#b=400 mm and #a=#b=1000 mm, respectively. Top view of the cases Z.20 and Z.20.5 are shown in Fig. 3.128. The results of the effect of HV feeding section on the frequency behavior of the zig-zag RVD (containing three different shields) with different positions of HV bus bar are shown in Fig. 3.129.

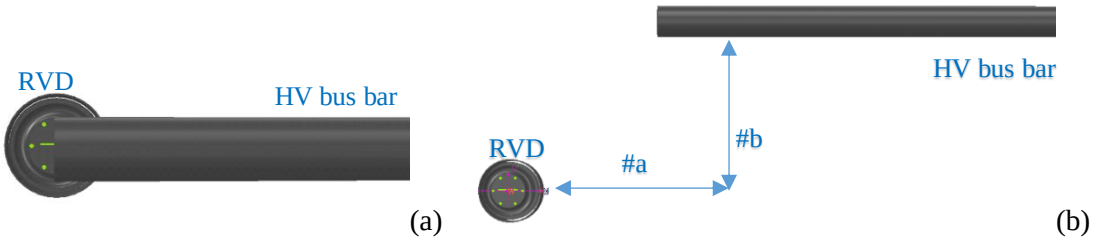
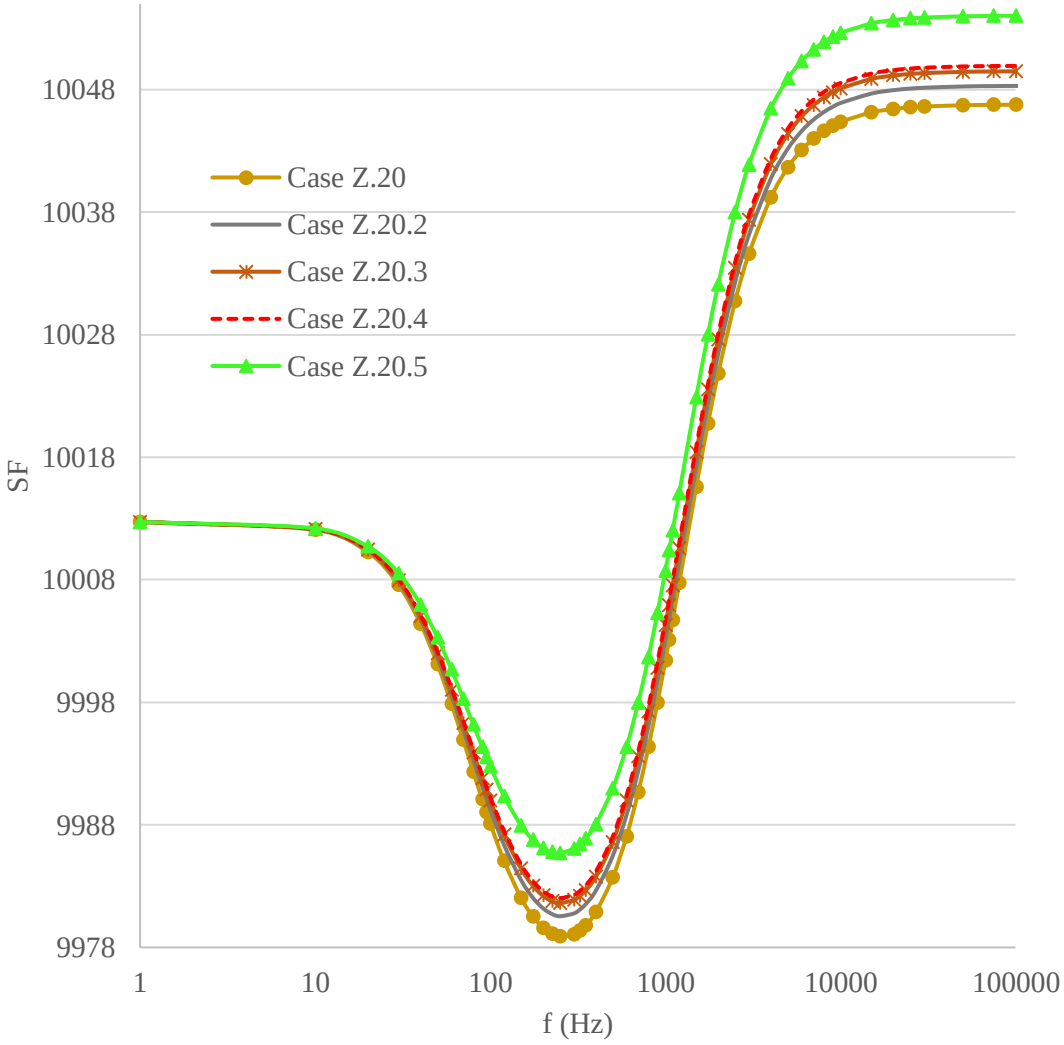


Fig. 3.128. Top view of FEM model of cases (a) Z.20(#a=#b=0 mm) and (b) Z.20.5(#a=#b=1000 mm)



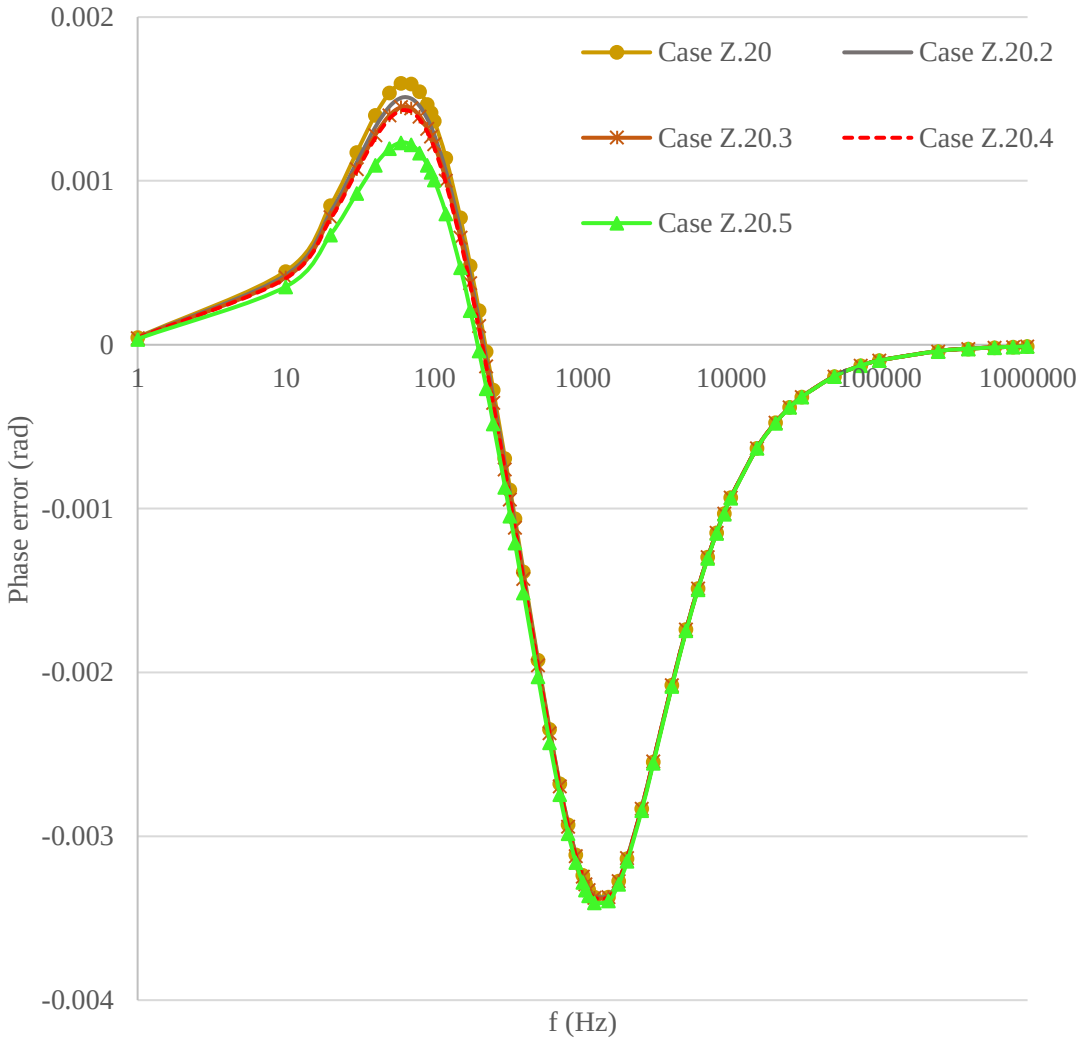


Fig. 3.129. Effect of zig-zag RVD displacement with respct to the HV bus bar

The results presented in Fig. 3.129 show that the ground shield can extremely decrease the proximity effect on the RVD and the frequency behavior remains practically unchanged. For instance, if the HV bus bar is displaced 400 mm in both along and perpendicular to the direction of the HV bus bar (#a=#b= 400mm), the scale factor changes just around 300 ppm (phase error changes about 0.18 mrad). Although it is not the goal for a standard reference divider, this result is the best results obtained up to now.

Two other issues should be addressed. The first one: the frequency behavior of the zig-zag RVD with three shields that should be corrected in order to reach the performance of a reference voltage transducer and the proximity effect analysis should be deepened. The

second issue is the maximum electrical field strength which should be studied afterwards. Such issues are addressed in the next sections.

3.8.8 Determining the best of shields height for a standard frequency behavior

In seven cases of Z.19, and Z.19.n (n=2,3,4,5,6,7), the LV and HV shield heights are changed in order to reach the best shields height. The Case Z.19 (as the case with the longest HV shield) and Z.19.7 (as the case with the longest LV shield) are shown in Fig. 3.130. The radial distance between the HV and LV shields is about 12.5 mm in all cases here mentioned.

The sum of LV and HV shield heights is always constant and, in the mentioned cases, is around 257 mm, so that the HV and LV shields cover the whole HV part. This means that the electric field coupling the inner electrodes to the outside perimeter will be cut and the stray capacitance between the inside and outside of the RVD will substantially decrease. The result of the cases Z.19, and Z.19.n (n=2,3,4,5,6,7) are displayed in Fig. 3.131.

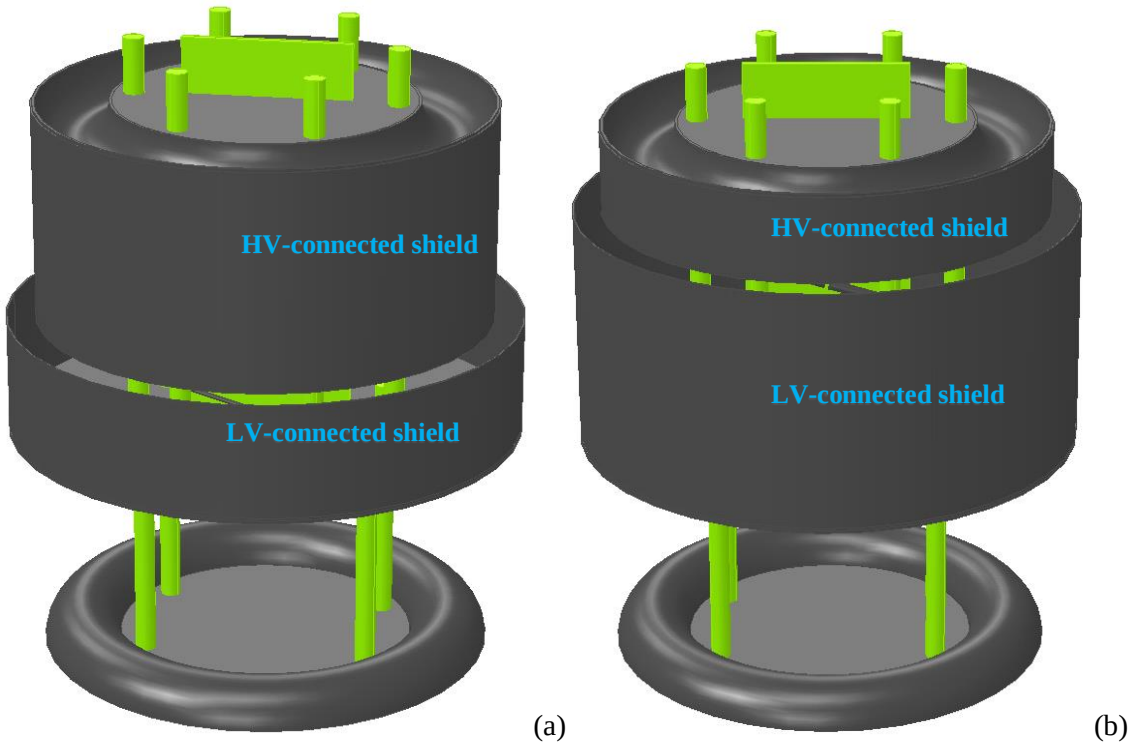


Fig. 3.130. FEM model of the case (a) Z.19 (b) Z.19.7

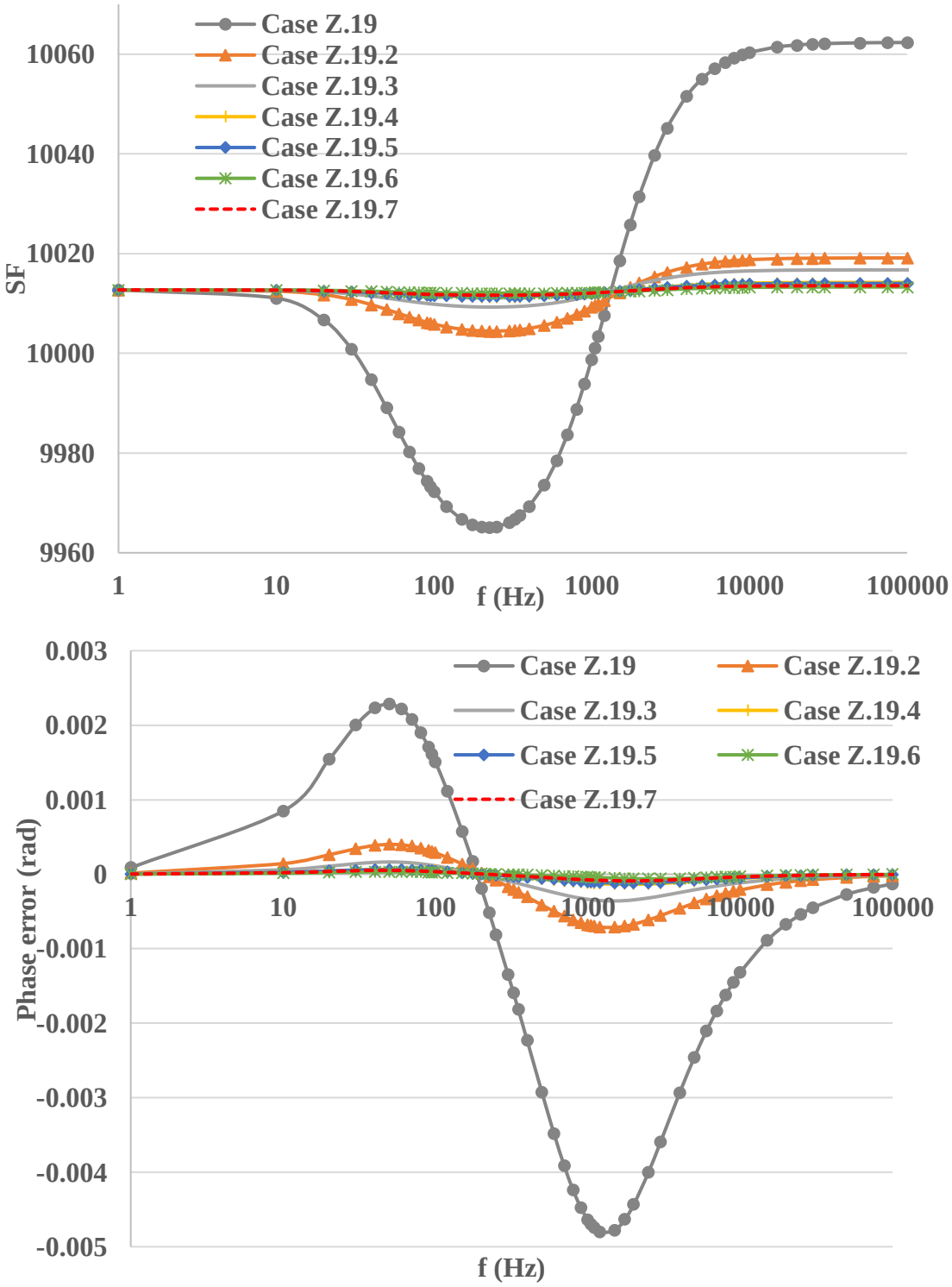


Fig. 3.131. Frequency responses of the cases Z.19 and Z.19.n (n=2,3,4,5,6,7) with different HV and LV shield heights

As can be found from Fig. 3.131, cases Z.19.4, Z.19.5, Z.19.6, and Z.19.7 can provide a very good frequency behavior. The deviation of their SF from the rated SF is less than 250 ppm and the phase error is less than 0.13 mrad (in cases Z.19.4, Z.19.5, Z.19.6, and Z.19.7). Although these cases can provide a very good frequency behavior, there is still drawback of proximity effect due to the fact that LV shield is openly exposed to the perimeter of the RVD.

Next, the case Z.19.7 is selected to be studied further. The case Z.19.7.2 (shown in Fig. 3.132) is thereupon simulated based on the geometry of the case Z.19.7 with appending a ground-connected shield covering the LV shield from the outside of the RVD. The result of the case Z.19.7.2 is shown in Fig. 3.133 compared to the result of the case Z.19.7 (without grounded shield).

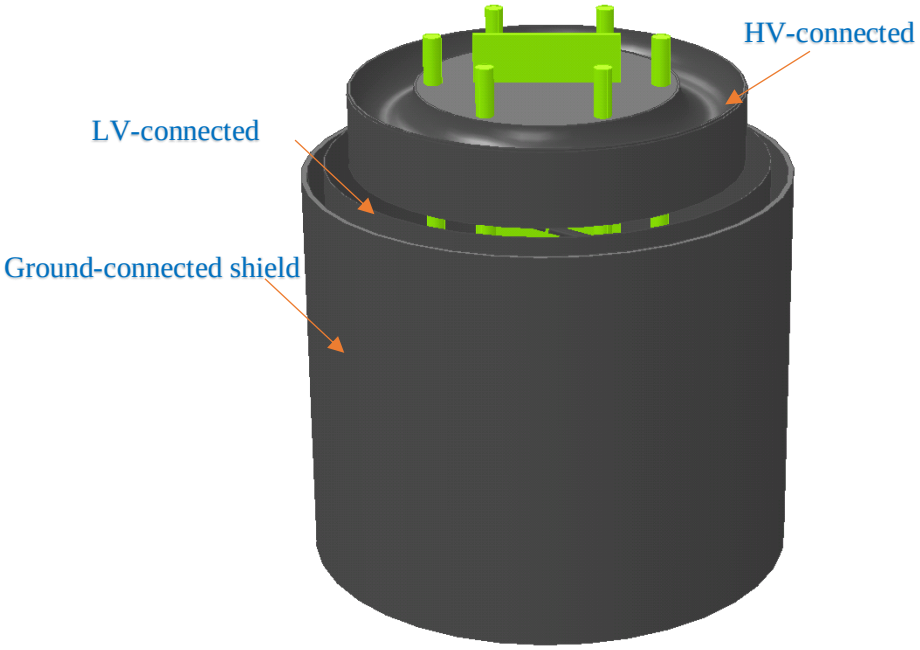


Fig. 3.132. FEM model of the case Z.19.7.2 (the ground and HV bus bar not shown here)

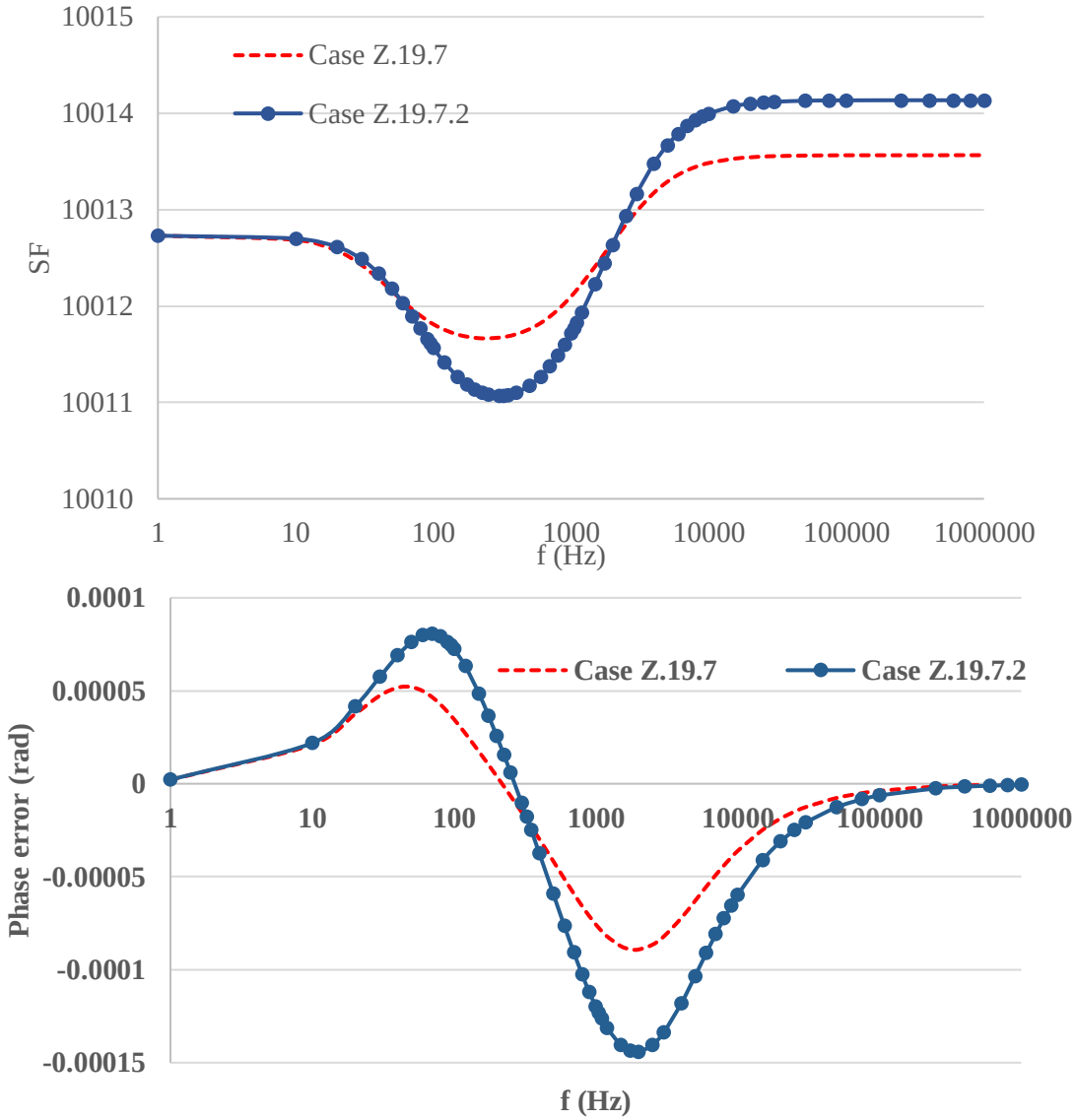


Fig. 3.133. Frequency responses of the case Z.19.7.2 compared to the one of the Z.19.7

The comparison between the cases Z.19.7.2 and Z.19.7 demonstrates that appending the ground connected shield does not practically changes the frequency behavior of the case Z.19.7. In the next step, the distance between the HV bus bar and the RVD is changed (cases Z.19.7.3, Z.19.7.4) in order to investigate the effect of proximity on the result of the zig-zag RVD. The case Z.19.7.5 is also simulated without the HV bus bar. The result of three aforementioned cases together with the result of the case Z.19.7.2 are presented in Fig. 3.134.

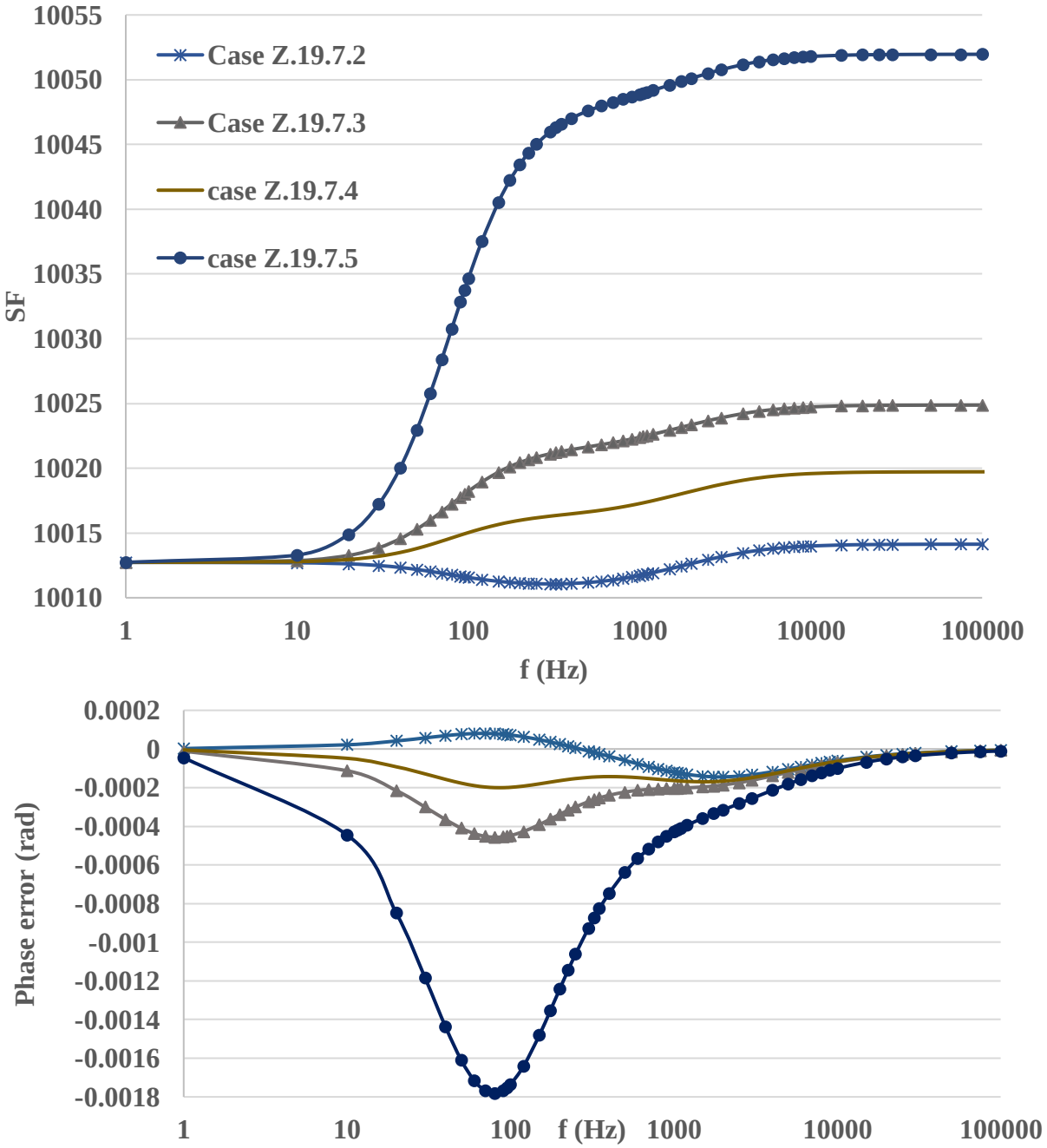


Fig. 3.134. Frequency responses of the case Z.19.7.2, Z.19.7.3, Z.19.7.4, and Z.19.7.5 with the same CBT

The results presented in Fig. 3.143 shows that the frequency behavior of the zig-zag RVD could be enough good for a reference voltage transducer if used in the laboratory. It means that it should be calibrated in low voltage after its placement in its position, and then it can be used as a reference voltage transducer.

Detail information about different parameters of the simulated zig-zag VDs are shown in Table 3.7.

Table 3.7. Different simulated cases of zig-zag RVD before realization of the zig-zag RVD

Case study	#d_1(mm)	#d_2=#d_3=#d_4(mm)	#d_5 (mm)	#G (mm)	Shield radius(mm)× height(mm)× thickness(mm)	Shield connected to:	#Pr (mm)	#α (deg)	HV bus bar	#a (mm)	#b (mm)	#eps
Z.1	70	70	50	180	200×100×1.2	LV	200	16	Yes	0	0	2.9
Z.2	80	70	50	180	200×100×1.2	LV	200	16	Yes	0	0	2.9
Z.3	70	70	50	180	200×280×1.2	LV	200	16	Yes	0	0	2.9
Z.4	70	70	50	180	200×100×1.2	LV	200	16	No	0	0	2.9
Z.5	70	60	40	180	200×100×1.2	LV	200	16	Yes	0	0	2.9
Z.6	70	60	40	160	200×100×1.2	LV	200	16	Yes	0	0	2.9
Z.7	70	50	35	160	200×100×1.2	LV	200	16	Yes	0	0	2.9
Z.8	70	50	35	160	200×80×1.2	LV	200	16	Yes	0	0	2.9
Z.9	70	50	35	160	200×120×1.2	LV	200	16	Yes	0	0	2.9
Z.9.2	70	50	35	160	200×120×1.2	LV	200	16	No	0	0	2.9
Z.9.3	70	50	35	160	200×120×1.2	LV	200	16	No	0	0	2.9
Z.9.4	70	50	35	160	200×120×1.2	LV	200	16	No	0	0	2.9
Z.9.5	70	50	35	160	200×120×1.2	LV	200	16	Yes	200	0	2.9

Z.9.6	70	50	35	160	200×120×1.2	LV	200	16	Yes	0	200	2.9
Z.10	70	47	35	160	200×100×1.2	LV	200	14	Yes	0	0	2.9
Z.11	80	47	35	160	200×100×1.2	LV	200	14	Yes	0	0	2.9
Z.12	70	50	35	160	200×110×1.2	LV	200	16	Yes	0	0	2.9
Z.13	70	50	35	160	180×110×1.2	LV	180	16	Yes	0	0	2.9
Z.14	70	50	35	160	175×89×1.4 : HV 200×120×1.2 : LV		200	16	Yes	0	0	2.9
Z.14.2	70	50	35	160	175×89×1.4 : HV 200×120×1.2 : LV		200	16	Yes	200	0	2.9
Z.15	70	50	35	160	175×137×1.4 : HV 200×120×1.2 : LV		200	16	Yes		0	2.9
Z.15.2	70	50	35	160	175×137×1.2 : HV 200×120×1.2 : LV		200	16	Yes	200	0	2.9
Z.16	70	50	35	160	200×185×1.2	Middle electrode	200	16	Yes		0	2.9
Z.17	70	50	35	100	175×137×1.4 : HV 200×120×1.2 : LV		200	16	Yes		0	2.9
Z.17.2	70	50	35	100	175×137×1.4 : HV 200×120×1.2 : LV		200	16	Yes	200	0	2.9
Z.18	70	50	35	250	175×137×1.2 : HV 200×120×1.2 : LV		200	16	Yes		0	2.9
Z.18.2	70	50	35	250	175×137×1.4 : HV 200×120×1.2 : LV		200	16	Yes	200	0	2.9

Z.19	70	50	35	180	175×167×1.4 : HV 200×90×1.2 : LV	200	16	Yes	0	0	2.9
Z.19.2	70	50	35	180	175×107×1.4 : HV 200×150×1.2 : LV	200	16	Yes	0	0	2.9
Z.19.3	70	50	35	180	175×97×1.4 : HV 200×160×1.2 : LV	200	16	Yes	0	0	2.9
Z.19.4	70	50	35	180	175×87×1.4 : HV 200×170×1.2 : LV	200	16	Yes	0	0	2.9
Z.19.5	70	50	35	180	175×77×1.4 : HV 200×180×1.2 : LV	200	16	Yes	0	0	2.9
Z.19.6	70	50	35	180	175×67×1.4 : HV 200×190×1.2 : LV	200	16	Yes	0	0	2.9
Z.19.7	70	50	35	180	175×57×1.4 : HV 200×190×1.2 : LV	200	16	Yes	0	0	2.9
Z.19.7.2	70	50	35	180	175×57×1.4 : HV 200×190×1.2 : LV 220×346×1.2 : ground	200	16	Yes	0	0	2.9
Z.19.7.3	70	50	35	180	175×57×1.4 : HV 200×190×1.2 : LV 220×346×1.2 : ground	200	16	Yes	1000	1000	2.9
Z.19.7.4	70	50	35	180	175×57×1.4 : HV 200×190×1.2 : LV 220×346×1.2 : ground	200	16	Yes	500	500	2.9
Z.19.7.5	70	50	35	180	175×57×1.4 : HV 200×190×1.2 : LV 220×346×1.2 : ground	200	16	No	0	0	2.9

3.9 Realization of zig-zag RVD

In the first practical realization of the RVD, due to difficulties in the assembly and mounting of the HV shield the case Z.9 (without HV shield) has been realized, although the best results of the RVD are obtained when the HV shield is present (for example case Z.19). The realized RVD is shown in Fig. 3.135. The measurement set-up is shown in Fig. 3.136. The measurement is performed using the Agilent3458 digitizers configured in sub-sampling mode. Such configuration provides larger frequency bandwidth than the measurement set-up used in Fig. 2.5, that is based on DCV mode. The drawback of using DCV acquisition mode is that the internal input low- pass filter have different cut-off frequencies for different ranges and varies from 30 kHz (ranges 100 V and 1000 V) to 150 kHz (ranges 1 V and 10 V). This means that the result of DCV mode cannot be accurate for higher frequencies and needs to be corrected. In this measurement set-up, the calibrator is removed (compared to the measurement set-up in Fig. 2.5) and the signal generator FLUKE 397 is used as the primary supply. Then, the amplifier NF HSA 4012 is employed to amplify the signal produced by the FLUKE 397. Two digitizers Agilent 3548 read the input and out-put signals of the RVD. The measurement results are presented in Fig. 3.137.

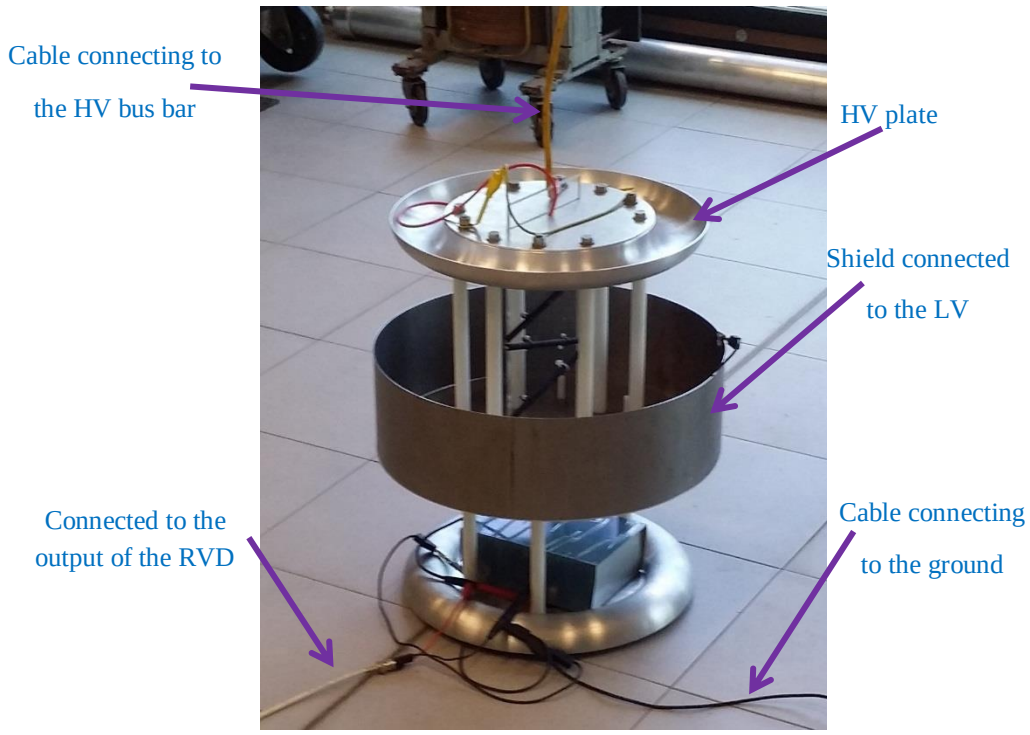


Fig. 3.135. The realized zig-zag RVD

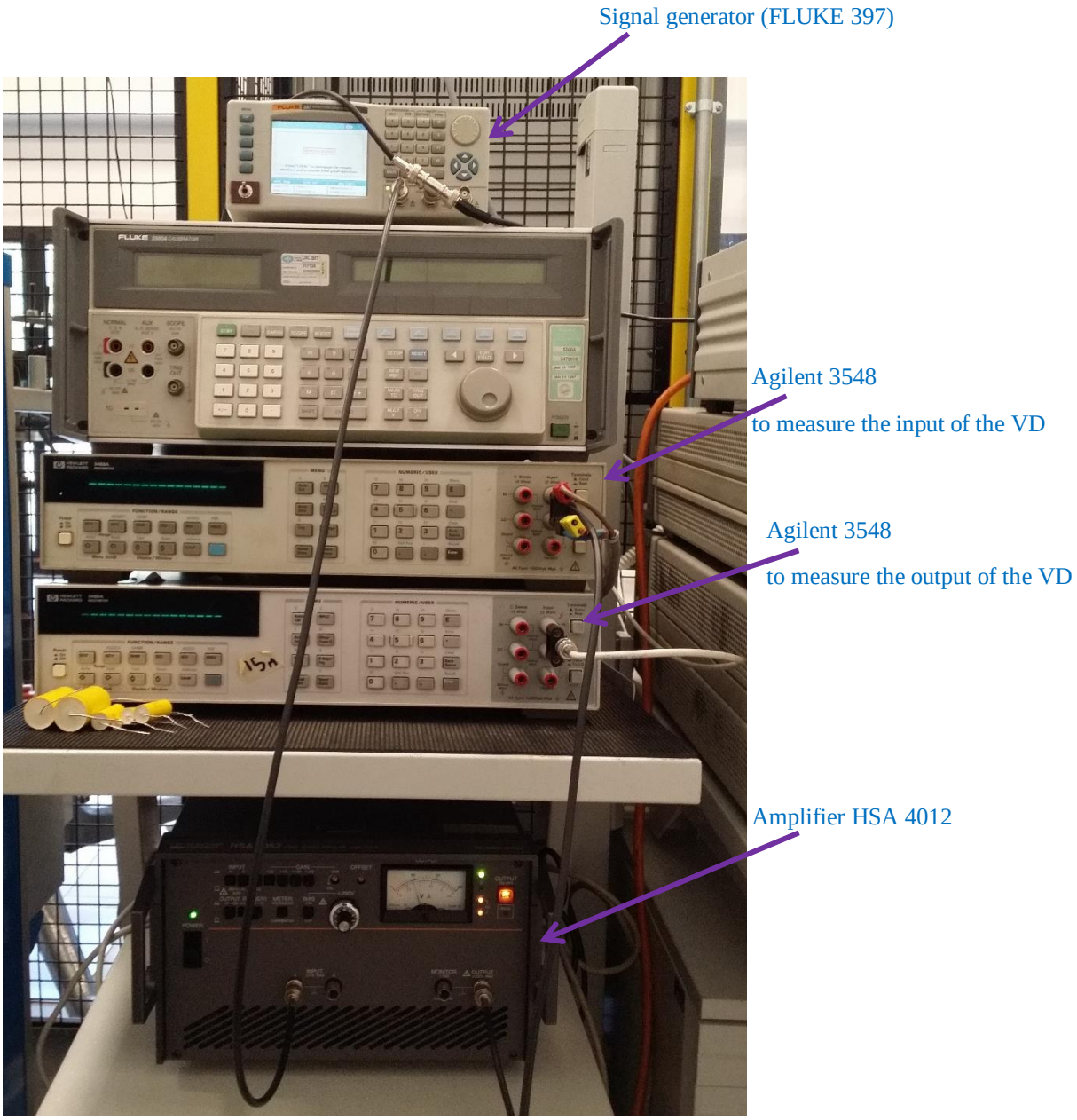


Fig. 3.136. The measurement set-up for digitizers used in subsampling mode

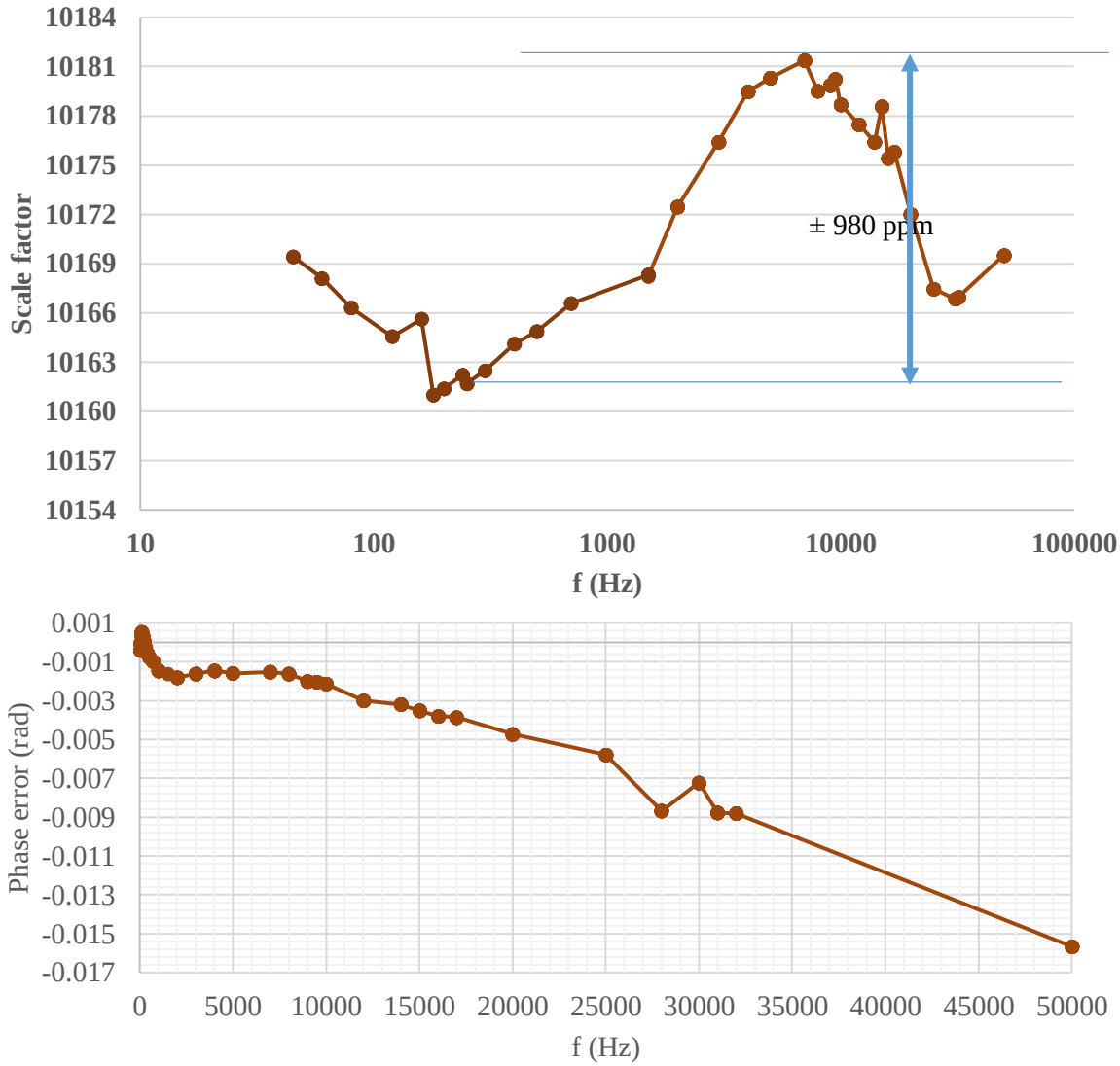


Fig. 3.137. Measurement results of the zig-zag RVD (similar to the simulated case Z.9)

As shown in Fig. 3.137, the maximum SF deviation is about ± 980 ppm up to 50 kHz which is a good response for the voltage transducer, with an accuracy 50 times better than the one required by the standards. The maximum phase error is -1.8 mrad up to 2.5 kHz (50^{th} harmonic), -2.1 mrad up to 10 kHz, and about -15 mrad up to 50kHz. It is worth to note that standard requires 18 mrad up to second harmonic and 90 mrad for the harmonics from 3^{rd} up to 50^{th}.

3.10 Resistive capacitive zig-zag VD

The maximum value of the stray capacitances in different RVD configurations is usually less than 1 pF. Then, the addition of HV capacitors (with much higher value than 1 pF) in parallel to each HV resistor reduces the effect of stray capacitances. Then, in order to decrease the proximity effect and having a better frequency behavior in comparison with the zig-zag RVD presented in previous sections, four series connected 1.2 nF capacitors are coupled to each HV resistor. In other words, each HV resistor is paralleled to 300 pF capacitance. In order to check the voltage applied to each capacitor in comparison to the rated voltage (3kV) the approximate voltage on each capacitor can be calculated as 1875 V (30 kV/16), neglecting the LV section and the stray capacitances. This value is sufficiently lower and then compatible with the rated voltage. The realized RCVD is shown in Fig. 3.138. A stranded copper wire is used in order to connect the HV capacitors to the resistors. However using the stranded wire, or soldering, causes sharp or semi-sharp edges increasing the risk of corona effect. To avoid this risk a semi-conductor paper shown in Fig. 3.139 is used to cover the stranded wire and the sharp edges.

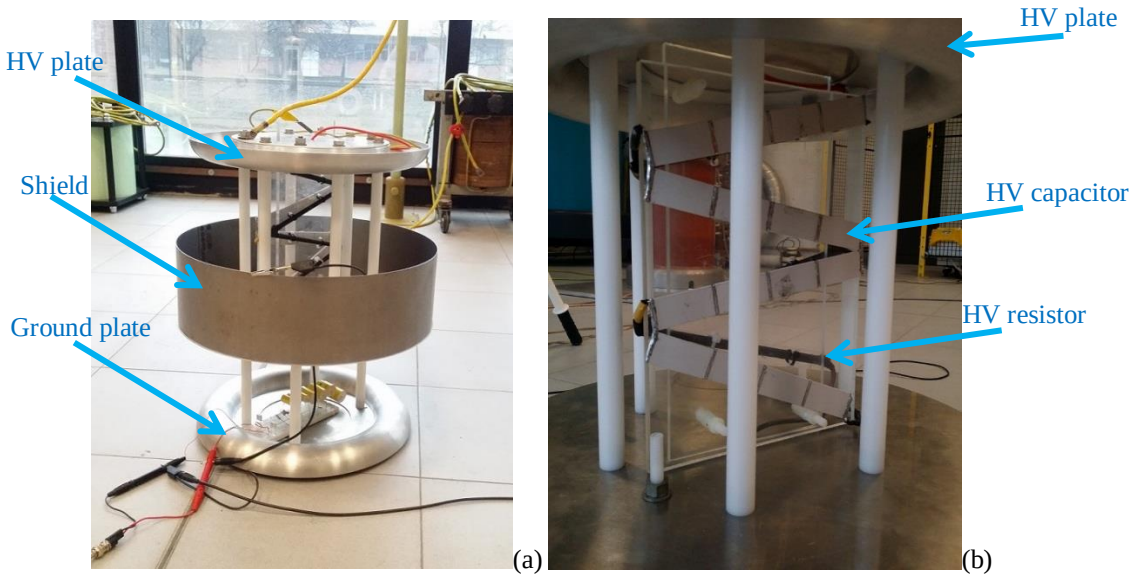


Fig. 3.138. Realized RCVD (a) general view (b) HV part (shield is not shown here)

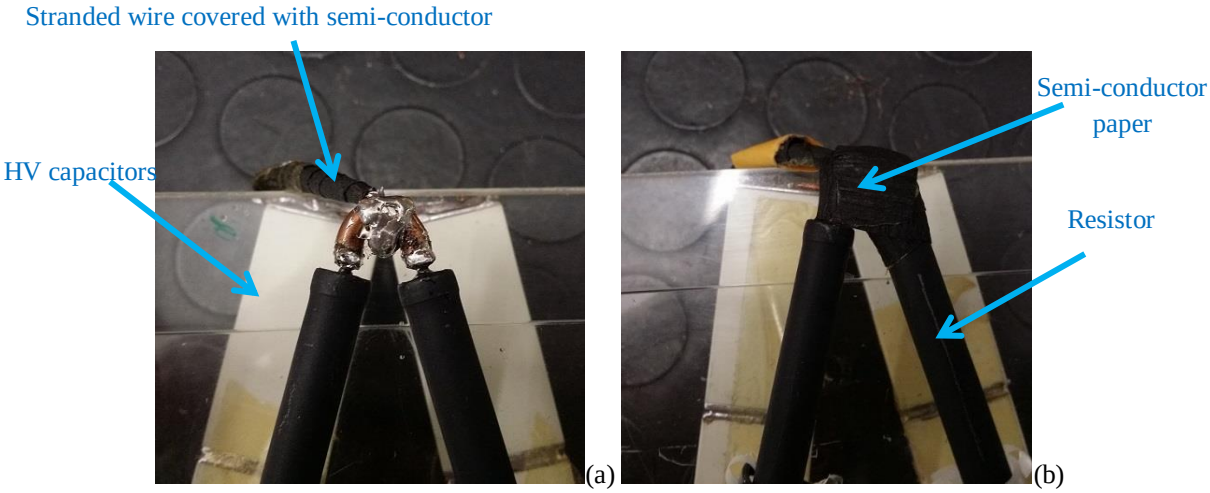


Fig. 3.139. Connection between HV capacitors and resistors (a) soldered with sharp edges (b)after using semi-conductor paper

3.10.1 The set-up used for frequency sweep measurement of the grounded

Two National Instruments (NI) digitizer modules (9225 and 9239) have been used in the frequency sweep measurement set-up of the zig-zag RCVD. The set-up is similar to the one described in Fig. 2.5. The input voltage of the RCVD is produced by the voltage calibrator FLUKE 5500. This voltage is measured by NI module 9225 (rated voltage 300 V_{rms}, 24 bit). The output voltage of the RCVD is measured by the NI module 9239 (maximum voltage: 10 V_{rms}, 24 bit). This set-up does not require an external synchronizer as these NI modules are integrated on the chassis CompactDAQ fitted by an internal trigger. The errors introduced by the use of two different NI modules is lower than 100 ppm for the SF ratio error [46]. However, these modules produce a considerable amount of the phase error specially at higher frequencies, as the NI module (9225) is 3 or 4 cycle is lagging from the NI module (9239). The time delay between two NI modules is defined as follows:

$$t_d = \frac{1}{f_c}(\mathrm{N_c}) \tag{3-4}$$

where t_d is the time delay between two NI modules, f_c is the clock frequency of the NI module (here is 12.8 MHz), and N_c is the cycle numbers that one NI modules lags. This time delay that makes a phase difference between two NI modules can be corrected in each frequency using the following formula:

$$phase\_correction = 2\pi f_s.t_d \tag{3-5}$$

where the f_s is the frequency of the signal (generated by the calibrator). For example, the phase error introduced by this effect is about 14.72 mrad (in case of 3 cycle lagging) or

19.63 mard (in case of 4 cycle lagging) at 10 kHz. The phase error (in case of 3 cycle lagging), which is only introduced by NI modules, is drawn in the Fig. 3.140.

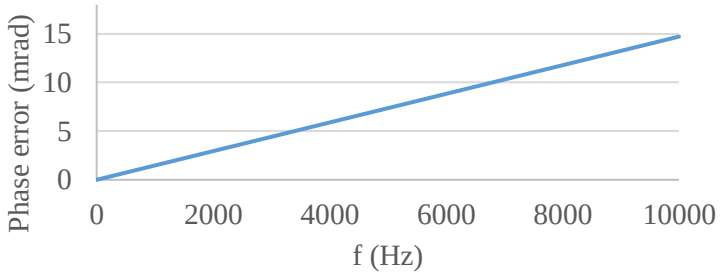


Fig. 3.140. Phase error introduced by the NI modules (in case of 3 cycle lagging)

3.10.2 Measurement results of RCVD with LV-connected shield

The DC scale factor of the RCVD under test is 10177. The best CBT should be increased up to the value to get a similar SF at higher frequencies. Initial result of the RCVD with LV-connected shield with a roughly chosen CBT is shown in Fig. 3.141. The maximum SF discrepancy from 45 Hz up to 10 kHz is about 500 ppm. This result shows that the CBT should be increased in order to reach a greater SF. However, it is important to know the proximity effect magniyude before increasing the CBT. The maximum phase error of the RCVD with LV-connected shield (shown in Fig. 3.141) is one order of magnitude lower than the requirement of standards for a voltage transducer.

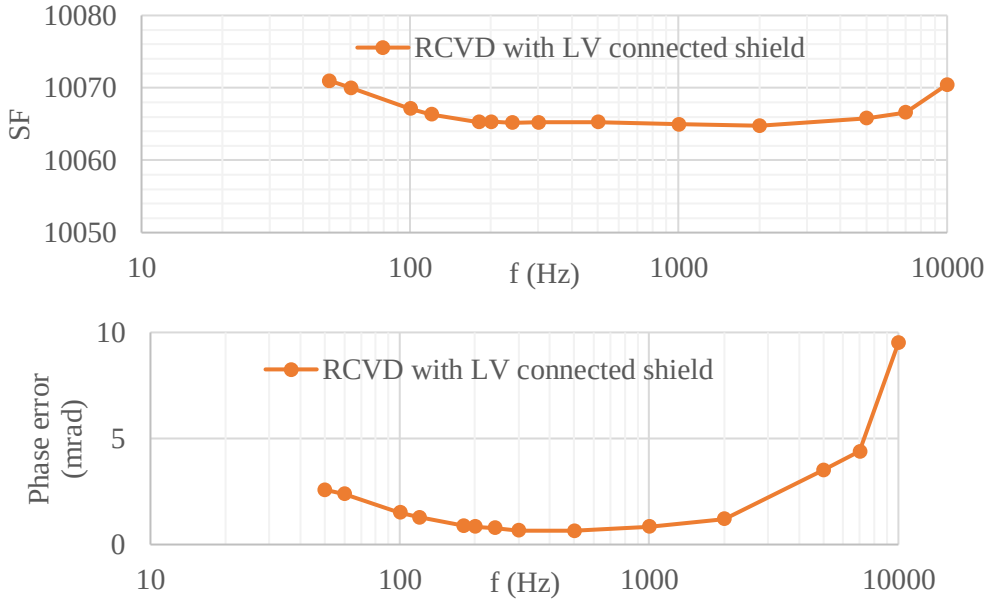


Fig. 3.141. Measurement results of the zig-zag RCVD with LV-connected shield

In spite of the satisfactory results provided by the zig-zag RCVD with LV-connected shield, the sensitivity to proximity effect of the divider remains an issue. Therefore a 40 cm × 50 cm rectangular plate (shown in Fig. 3.142) is placed at two distances (60 cm and 30 cm) from the RCVD in order to evaluate the proximity effect of a foreign object. The result is shown in Fig. 3.143.

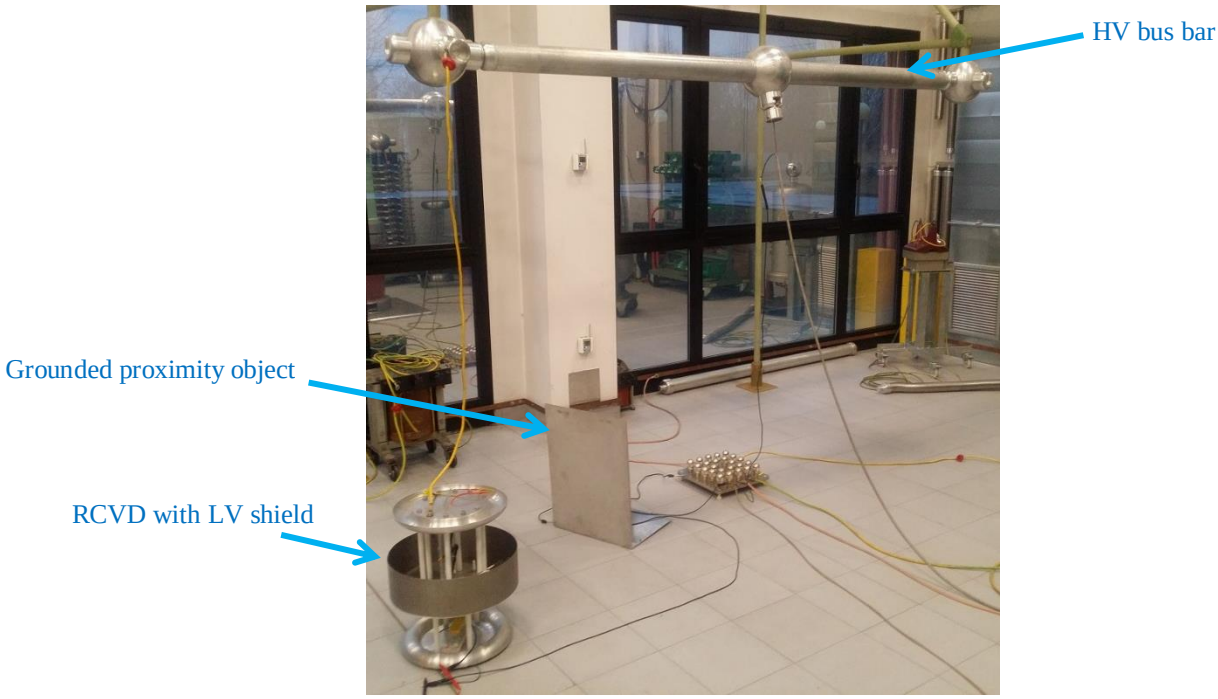
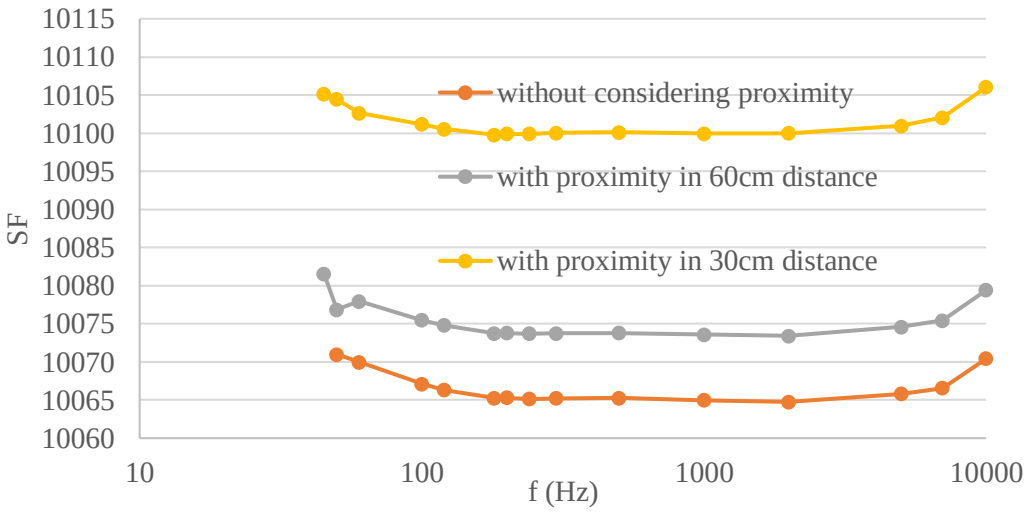


Fig. 3.142. Measurement set-up with the grounded plate as a proximity object



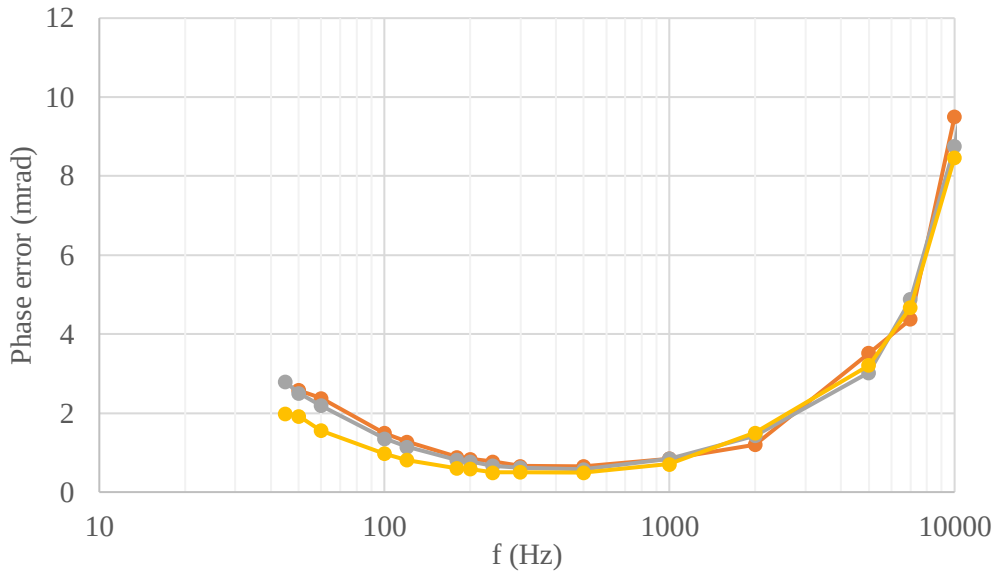


Fig. 3.143. Measurement results of the zig-zag RCVD with LV-connected shield including a proximity object in two different distances

The result shown in Fig. 3.143 illustrates that the proximity sensitivity of the RCVD with LV connected shield is not small and the SF increases up to 700 ppm and 3500 ppm for distances from the proximity object of 50 cm and 30 cm, respectively. This means that when the RCVD with the LV-connected shield is calibrated for an environment, whose layout is fixed such as an HV laboratory, it can be suitably calibrated and work well. However, if the proximity of the RCVD (with the LV-connected shield) or its position changes, it needs to be re-calibrated.

The shield potential has clearly an effect on stray capacitances and on proximity effect. To reduce the latter, the shield has been connected to the ground. In this way, the stray capacitances between the HV section and the ground will be higher. Then, if a nearby grounded object is moved towards the RCVD with grounded shield, it cannot affect significantly the stray capacitances.

To investigate this hypothesis, the frequency response of the RCVD with grounded shield was measured. Next, the effect of a proximity object (a plate with the size of 40 cm × 50 cm) on behavior of the RCVD (with grounded shield) is studied.

3.10.3 Measurement results of RCVD with ground connected shield

The best CBT has been chosen for the RCVD with ground-connected shield in order to reach the minimum deviation from the DC scale factor, which is about 10177. The results are shown in Fig. 3.144. In order to check out the proximity effect, a rectangular plate

having size of 40 cm × 50 cm is placed at a distance of 30 cm from the RCVD (with grounded shield) without modifying the CBT.

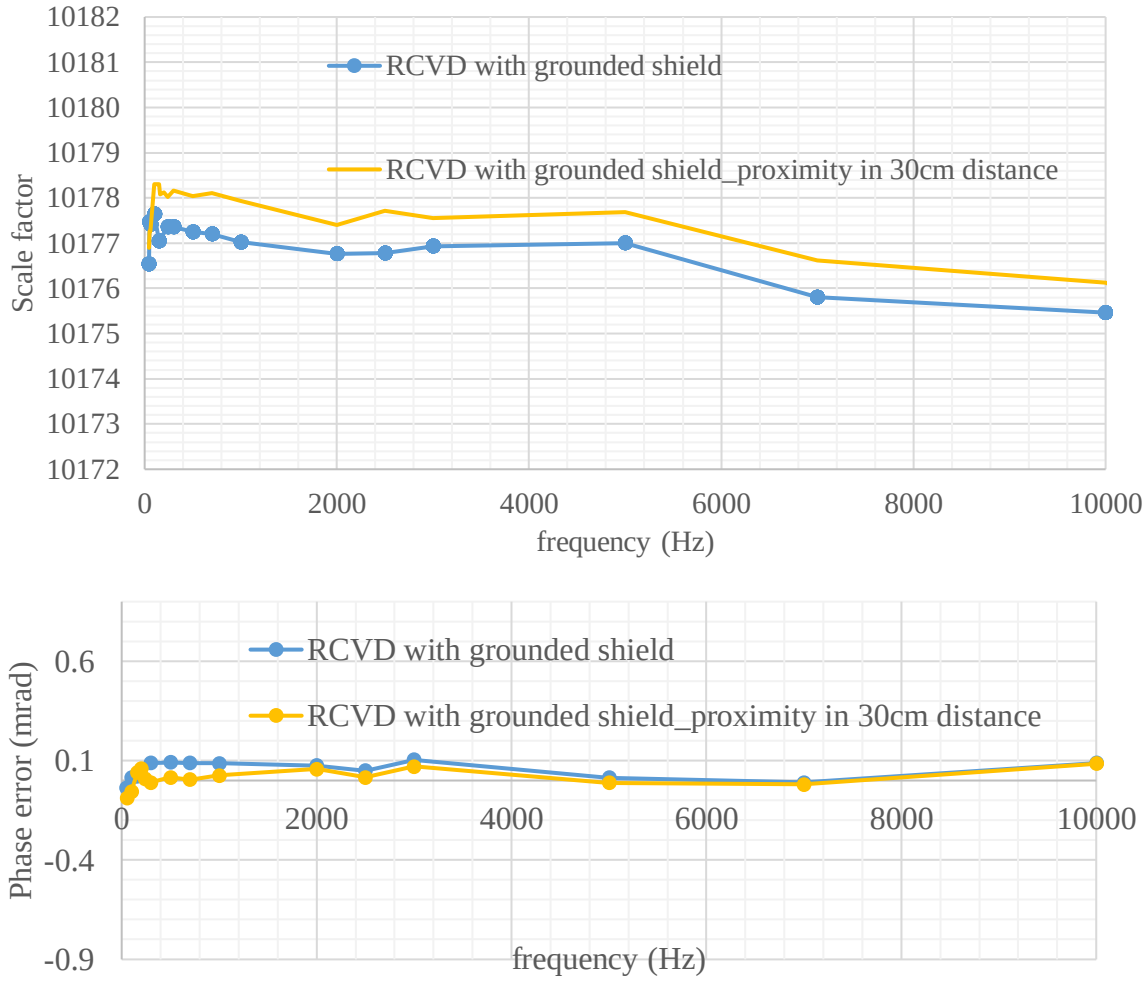


Fig. 3.144. Measurement results of the zig-zag RCVD (with ground connected shield) including a proximity object at 30 cm distance distances

The result shown in Fig. 3.144 demonstrates that the grounded shield RCVD has maximum SF deviation (from the DC scale factor) of 151 ppm which is very good for a reference voltage transducer designed for high voltage and large frequency bandwidth. The maximum phase error is also below 105 µrad, which could be considered as great result for a reference VT. Moreover, Fig. 3.144 most importantly shows a very limited proximity effect of foreign objects in presence of the grounded shield RCVD. The SF (and also the phase error) did not practically change in presence of grounded plate (40 cm × 50 cm) which is 30 cm distance from the VD. In presence of a grounded plate (40 cm × 50 cm) at 30 cm from the VD, the maximum SF and phase error variations are about 91.3 ppm and 89 µrad, respectively.

3.10.4 Linearity measurement of the RCVD with grounded shield

The linearity of the RCVD (with grounded shield) is measured at 50 Hz, for voltages starting from 2kV up to 30 kV. The measurement setup schematic is shown in Fig. 3.145. The realized set-up is also shown in Fig. 3.146 and Fig. 3.147. The signal generator Fluke 397 is used to synchronize two digitizers Agilent 3458. The voltage is provided by the voltage generator ELECTROTEST. The output of the ELECTROTEST (shown in Fig. 3.146) supplies the step-up voltage transformer (shown in Fig. 3.147) which allows one to reach even more than 30 kV. The output voltage of step-up transformer is connected to the input of RCVD and the reference measurement VT via HV bus bar (all four are shown in Fig. 3.147). The output signal of the RCVD is read directly by one of the digitizers Agilent 3458. The output voltage of the reference measurement VT is scaled down again by an inductive VD (Conimed), which has a measurement uncertainty lower than 25 ppm up to 400 Hz. The output signal of the IVD (Conimed) is measured by the second digitizer Agilent 3458. Using the accurate voltage ratio and phase error introduced by the measurement VT, the exact input voltage of the RCVD could be calculated. The out signal of the RCVD is also clear from the second digitizer. Then the correct SF and phase error of the RCVD (with ground shield) can be calculated.

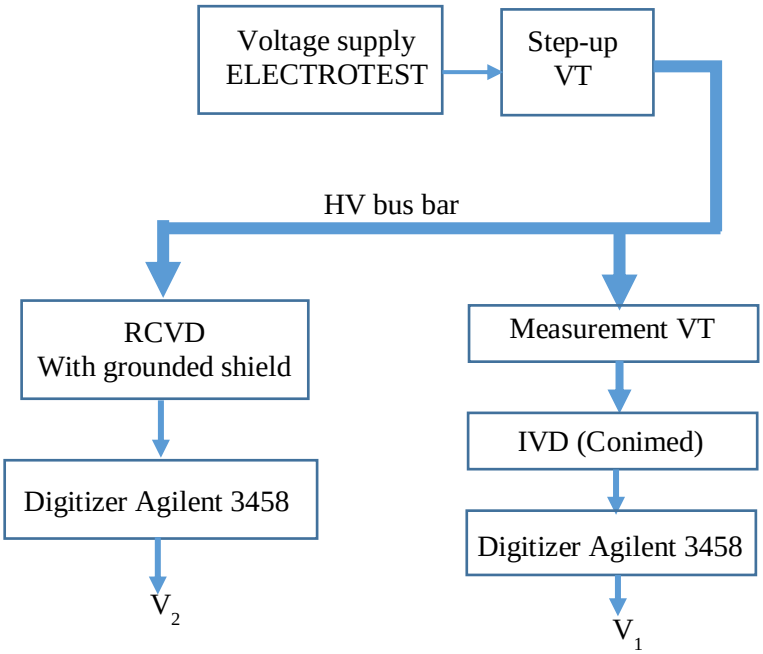


Fig. 3.145. Linearity measurement set-up schematic

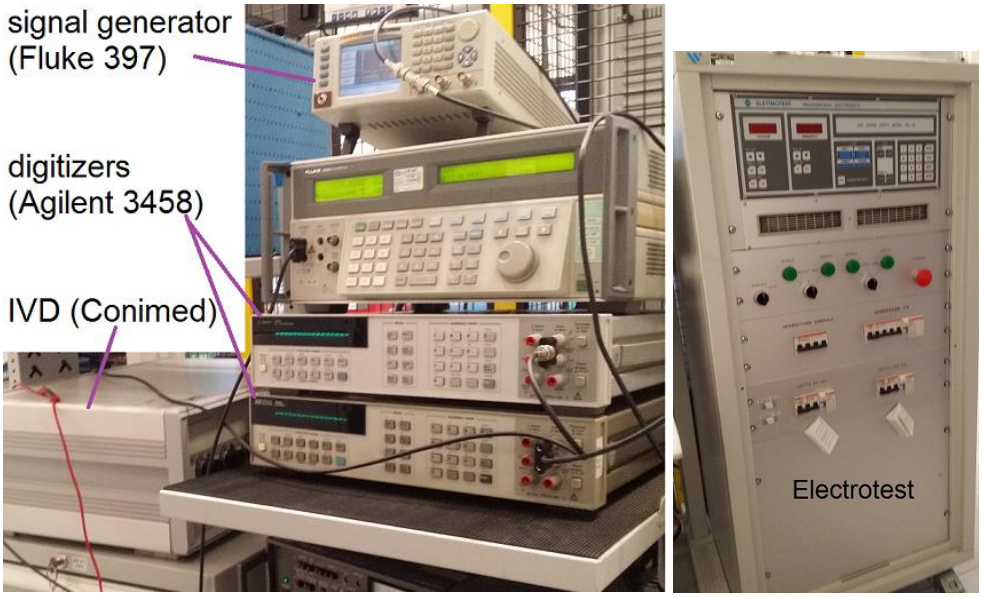


Fig. 3.146. Measurement set-up for linearity test of RCVD with grounded shield

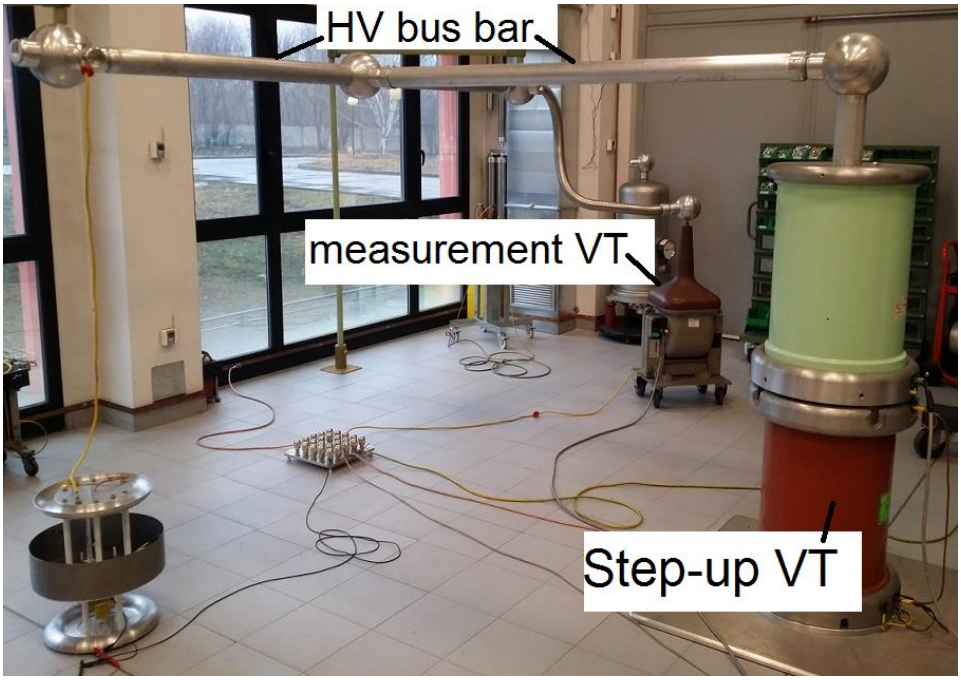


Fig. 3.147. Measurement set-up for linearity test of RCVD with grounded shield

The final results of linearity test at 50 Hz for different voltages are shown in Fig. 3.148.

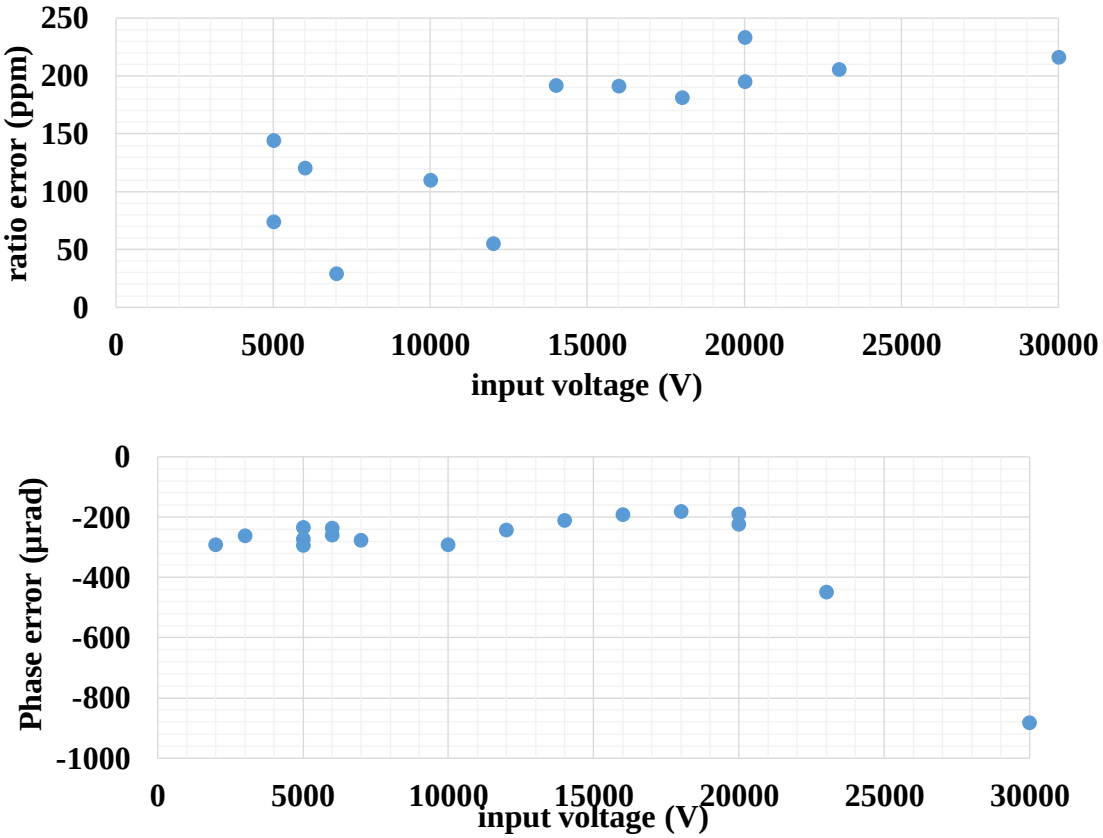


Fig. 3.148. Measurement result of linearity test

The results presented in Fig. 3.148, will be used in the uncertainty calculations as a correction factor besides an uncertainty due to complete voltage range up to 30 kV.

The results presented in Fig. 3.148, will be used in the uncertainty calculations to evaluate the correction factors and its uncertainty in the whole voltage range up to 30 kV.

3.10.5 Uncertainty of the RCVD with grounded shield

The measurement values to be assigned to the RCVD divider scale factor (SF_{ass}) and phase error $\Delta\varphi_{ass}$ can be respectively modelled as:

$$SF_{ass} = SF_{LV} \cdot k_{lin} \cdot k_{NI} \cdot k_{prox} \cdot k_{freq}$$
$$\Delta\varphi_{ass} = \Delta\varphi_{LV} - \delta\varphi_{NI} - \delta\varphi_{lin} - \delta\varphi_{prox} - \delta\varphi_{freq} \quad (3\text{-}6)$$

The model input quantities are described in Table 3.8 and a first uncertainty budget is given in Table 3.9. The standard uncertainties associated with the model input quantities are estimated considering the measurement chains and results obtained in the characterization tests carried out, which are described in the previous sections.

Table 3.8. Definition of the scale factor and phase error measurent model input quanties

Parameter	Description of the parameter
SF_{LV}	DC value of the SF measured at low voltage with ground connected shield and best CBT (Section 3.10.3)
k_{NI}	Correction factor due to NI modules accuracy and non -linearity (from already available characterization data) [46]
k_{lin}	Correction factor due to SF variation over its voltage operating range (Section 3.10.4)
k_{prox}	correction factor due to proximity effect (Section 3.10.33.10.3)
k_{freq}	correction factor due to variation of the scale factor during frequency sweep measurements (Section 3.10.3)
$\Delta\varphi_{LV}$	Phase error measured at 51 Hz (Section 3.10.3)
$\delta\varphi_{NI}$	Phase error correction due to NI non-linearity (from already available characterization data)
$\delta\varphi_{lin}$	Phase error correction due to variation of the phase error over its voltage operating range (Section 3.10.4)
$\delta\varphi_{prox}$	correction factor due to proximity effect (Section 3.10.3)
$\delta\varphi_{freq}$	Correction due to the variation of the phase error during frequency sweep measurements (Section 3.10.3).

The uncertainty budget and the associated correction due to different factors are presented in the following tables from Table 3.9 up to Table 3.14 for both SF and the phase error.

The Table 3.9 provides the maximum possible SF uncertainty in the presence of a rectangular object (with the size of 50 cm × 40 cm) in 30 cm distance from the RCVD.

Table 3.9. Uncertainty budget table for SF considering all factors

input quantities (Xi)	value	Relative standard uncertainty u_r (x_i) ($\cdot 10^{-6}$)	Sensitivity coefficient c_i	probability distribution	Relative standard uncertainty contribution $u_{ri} = c_i \cdot u_{r(}x_i)$
measured scale factor SF_{LV}	10177	18.21	1	rectangular	18.21
NI modules correction factors k_{NI}	1	28.87	1	normal	28.87
linearity k_{lin}	0.999867	58.31	1	rectangular	58.31
proximity k_{prox}	1	52.76	1	rectangular	52.76
Frequency response k_{freq}	1	87.18	1	rectangular	87.18
Expanded relative uncertainty (level of confidence 95%) ($\cdot 10^{-6}$): 244.54					

The data presented in Table 3.9 shows a good result ($244 \cdot 10^{-6}$ relative uncertainty) for a frequency bandwidth from DC to 10 kHz, and an input voltage up to 30 kV, The measurement conditions include the presence of a rectangular object (with the size of 50 cm × 40 cm), which may be positioned from an infinite distance to 30 cm far from the RCVD. Of course, in the actual laboratory condition there are no such big objects near to the RCVD and the actual relative uncertainty would be slightly less. The uuncertainty budget for the phase error considering all five different contributions is presented in the Table 3.10 (for input voltage up to 20 kV) and

Table 3.11 (for input voltage from 20 kV up to 30 kV), in the presence of a rectangular object (with the size of 50 cm × 40 cm) 30 cm distance from the RCVD.

Table 3.10. Uncertainty budget table for the phase error up to 20 kV

input quantities (x_i)	Values (µrad)	Standard uncertainty u_r (x_i) (µrad)	Sensitivity coefficient c_i	probability distribution	Standard uncertainty contribution $u_i = c_i.u_r(x_i)$
measured phase error $\Delta\varphi_{LV}$	0	34	1	rectangular	34
NI modules $\delta\varphi_{ni}$	0	75.06	1	normal	75.06
linearity $\delta\varphi_{lin}$	235	32.04	1	rectangular	32.04
proximity $\delta\varphi_{freq}$	0	47.34	1	rectangular	51.38
frequency response $\delta\varphi_{freq}$	70.5	19.63	1	rectangular	19.63
Expanded uncertainty (level of confidence 95%) (µrad): 204.38					

Table 3.11. Uncertainty budget table for the phase error from 20 kV up to 30 kV

input quantities (x_i)	Values (µrad)	Relative standard uncertainty u_r (x_i) (µrad)	Sensitivity coefficient c_i	probability distribution	Relative standard uncertainty contribution $u_i = c_i.u_r(x_i)$
measured phase error $\Delta\varphi_{LV}$	0	34	1	rectangular	34
NI modules $\delta\varphi_{ni}$	0	75.06	1	normal	75.06
linearity $\delta\varphi_{lin}$	536	143.18	1	rectangular	143.18
proximity $\delta\varphi_{freq}$	0	47.34	1	rectangular	51.38
frequency response $\delta\varphi_{freq}$	70.5	19.63	1	rectangular	19.63
Expanded uncertainty (level of confidence 95%) (µrad): 345.93					

As can be seen, the uncertainty of the phase error is about 205 μrad (for input voltage up to 20 kV) and around 346 μrad (for input voltage from 20 kV up to 30 kV). These data could be considered a very good result for the phase error while the uncertainty due to a rectangular object that reach from very far distance to the 30 cm distance of the RCV, is also considered.

Generally speaking, the foreign objects near the RCVD and the environmental conditions of the laboratory can be easily controlled. Therefore, the probability of having undesired objects near the VD can be considered negligible. Due to this reason, the uncertainty budget tables are also given without considering any effect from the proximity objects

Table 3.12. Uncertainty budget table for SF without considering proximity effect

input quantities (xi)	values	ur (xi) (ppm)	Ci	probability distribution	ui = Ci.u(xi)
measured SF (due to repeatability)	10177	18.21	1	rectangular	18.21
correction factor of NI modules	1	28.87	1	normal	28.87
linearity & heating effect	0.999867018	58.31	1	rectangular	58.31
Frequency response (biggest discrepancy of mean SF values from the DC SF)	1	186.48	1	rectangular	186.48
Expanded relative uncertainty (level of confidence 95%) ($\cdot 10^{-6}$): 220.6					

As can be seen. the uncertainty of the SF when there is no proximity around the RCVD is about 220 ppm which is more than two order of magnitude better than the requirement of a standard voltage transducer.

Table 3.13. Uncertainty budget table for the phase error up to 20 kV without considering proximity effect

input quantities (xi)	Values (µrad)	u (xi) (µrad)	Ci	probability distribution	ui = Ci.u(xi)
measured phase error (due to repeatability)	0	34.00	1	rectangular	70.5
correction factor of NI modules	0	75.06	1	normal	70.5
linearity & heating effect	235	32.04	1	rectangular	70.5
Frequency response (biggest discrepancy of mean phase error values)	70.5	19.63	1	rectangular	70.5
Expanded uncertainty (level of confidence 95%) (µrad): 181.12					

Table 3.14. Uncertainty budget table for the phase error from 20 kV up to 30 kV without considering proximity effect

input quantities (xi)	Values (µrad)	u (xi) (µrad)	Ci	probability distribution	ui = Ci.u(xi)
measured phase error	0	34.00	1	rectangular	34.00
correction factor of NI modules	0	75.06	1	normal	75.06
linearity & heating effect	536	143.18	1	rectangular	143.18
Frequency response (biggest discrepancy of mean phase error values)	70.5	19.63	1	rectangular	19.63
Expanded uncertainty (level of confidence 95%) (µrad): 332.72					

The uncertainty related to the phase error is about 181 μrad (for the input voltage up to 20 kV) and 333 μrad (for the input voltage from 20 kV up to 30 kV). This result, which has been obtained without any object near to the RCVD, could be considered another great result for a reference voltage transducer.

Chapter 4

Conclusion and suggestions

The aim of the thesis was to realize a reference voltage transducer for the calibration and characterization purposes of sensors for smart grid applications. Such a measurement tool can be also applied to smart meters in the grid.

The main achievements of this thesis work can be summarized as follows.

- At first, a numerical tool containing FEM and Matlab codes has been developed to accurately model and predict the frequency behavior of the VDs. The performance of the tool was validated by comparison between the results of the simulation and measurements on a two real RVDs (a prototype and also a 20 kV resin insulated RVD).
- The important role of the resistor body was highlighted in that tool which was, to the author knowledge, not fully investigated before in literatures and results have been published.
- The importance of a proper modeling of the ground floor has been proved and quantified by simulations and by the realization and characterization of a vertical 30 kV RVD.
- A comprehensive investigation including the study of different RVD configurations, the sensitivity analysis of different parameters (i.e. type of electrical connections, shield types and so forth) has been carried out providing useful data for literature and future investigations.
- Above of all, a 30 kV RVD with zig-zag component arrangement has been realized which shows a good result up to 50 kHz. It shows a relative uncertainty (only due to frequency response at low voltage) of ± 980 ppm (for the SF). Furthermore, the maximum phase error is -1.8 mrad up to 2.5 kHz (50^{th} harmonic), -2.1 mrad up to 10 kHz, and about -15 mrad up to 50kHz. This could be considered as a good result, 50 times better than a standard device. The analysis shows that when the application of the mentioned RVD is only for the calibration or

characterization of the measurement devices in laboratory conditions, it could be used as a reference voltage transducer.

- A specific study has been carried out concerning the introduction of a capacitive compensation in the RVD. By adding four 1.2 nF capacitors (3kV) parallel to each HV resistor, an RCVD was obtained from the RVD. The result of RCVD with introduction of a grounded shield are very great. The SF uncertainty (considering all uncertainties in laboratory condition) is 220 ppm, which is 225 times better than the standard requirements for a voltage transducer used for Power Quality measurement up to 10 kHz. The phase error uncertainty (after correction for systematic error) is also 181 µrad for voltages up to 20 kV (about 100 times better than the requirement for a measurement voltage transducer used in Power Quality voltage transducer) and 333 µrad for rms voltages from 20 kV up to 30 kV. The result of the RCVD with grounded shield proves that it is a more than satisfactory reference voltage transducer, with a very small sensitivity towards proximity effects and can be accurately used from DC up to 10 kV

4.1 Perspectives

The achievements here presented leave room for further studies. The RVD with three shields (with HV, LV, and ground connections) –like case Z.20– could be further investigated, optimized and then realized. Actually, the preliminary results obtained with such RVD envisage the possible realization of a cheap and qualified reference voltage transducer.

In addition, RCVD (with ground shield) can be considered superior to voltage measurement transformers for calibration and characterization applications, which involves wideband analysis. Besides, it could be considered a strong competitor for voltage measurement transformers in terms of both costs and accuracy. That is why a suitably designed, insulated and shielded version of the above two VDs should be optimized and realized in order to prepare them for the on-site applications as commercial voltage transducers.

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