POLITECNICO DI TORINO

VISHAY SEMICONDUCTOR ITALIANA

Thermal dissipation improvement by new technology approach: study, development and characterization

Department of Applied Science and Technology

PhD in Physics XXVIII Cycle

Isabella Para

Supervisors

Prof. C.F. Pirri

Dott. L. Merlin

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Chapter 1

INTRODUCTION

In this introductive Chapter, an overview of the semiconductor wafer and its thinning technique is reported. Afterwards it is presented an alternative approach to improve the performances of the electronic devices, which is the thesis' target. Finally, the last Section of the Chapter is dedicated to the description of the thesis structure and where it was conduct.

1.1 Semiconductor wafer

In electronics, a wafer (also called a slice or substrate) is a thin slice of semiconductor material, such as a silicon crystal, used in the fabrication of integrated circuits and other micro-devices.
The wafer serves as the substrate for microelectronic devices built in and over the wafer and undergoes many microfabrication process steps such as doping or ion implantation, etching, deposition of various materials and photolithographic patterning.
Front-end-of-line (FEOL) processing refers to the formation of devices directly in the substrate. In order to enhance the performance of electronic devices, the raw wafer is engineered by the growth of an ultrapure, virtually defect-free, silicon layer through epitaxy. Once the epitaxial silicon is deposited, the crystal lattice becomes stretched somewhat, resulting in improved electronic mobility. In addition, epitaxial wafers over

bulk wafers offer mean of controlling the doping profile and epitaxial layers are generally oxygen and carbon free.
Since the epitaxial silicon layer is the layer of device fabrication, its thickness choice depends largely on the intended application. Moreover, raw wafer thickness is determined by the mechanical strength of the material used and by the slice diameter; the important thing is that the wafer must be thick enough to ensure a minimum of mechanical stability to support its own weight without cracking during handling and to avoid warping during high-temperature processing steps.
Single crystal silicon wafers are utilized for essentially all integrated circuits and many other semiconductor devices. To permit common processing equipment to be used in multiple device fabrication lines, it is essential for the wafer dimensions to be standardized [1].

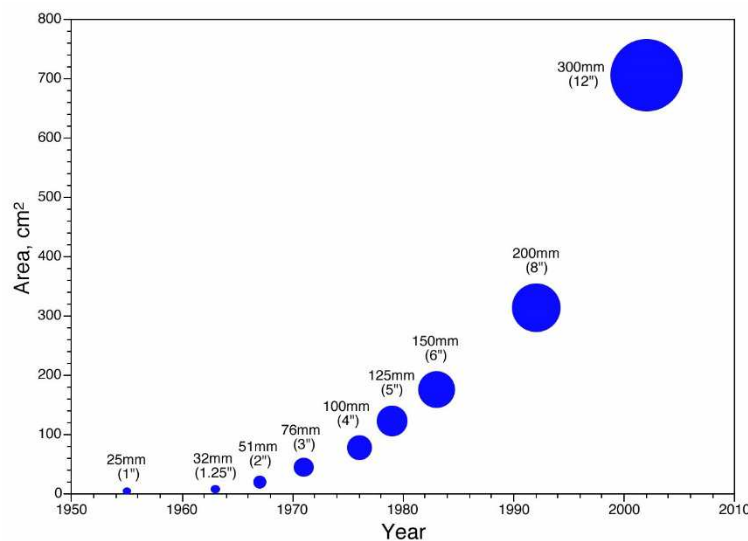

Fig. 1 Commercial silicon wafer size vs year trend [2].

Fig. 1 reports the time evolution in commercial silicon wafer size during last 60 years. The diameter has gradually increased to improve throughput and reduce cost but larger wafer diameters require thicker silicon to withstand wafer manufacturing.

Diameter [mm]	Diameter [inch]	Thickness [µ]
25	1	-
51	2	275
76	3	375
100	4	525
130	5	625
150	6	675

200	8	725
300	12	775
450	18	925

Tab. 1 Current commercial silicon wafer size [3].

Tab. 1 reports some values of production standard wafer sizes in case of silicon substrates.
On the other hand, the epitaxial layer thickness strictly depends on the desired device, thus, it is always thinner than the bulk substrate (Fig. 2). It ranges from a few hundred Angstrom to several tenth of Microns. This means that the active region of a semiconductor device is limited at the surface, thus there is a large amount of unused material. This silicon bulk material excess acts only as a mechanical support during manufacturing process steps and causes heat increasing during the device operation. Thermal dissipation is an important issue in semiconductor manufacturing because the operation of a semiconductor device is sensitive to temperature. When the junction temperature exceeds its functional limit, semiconductor performance, life, and reliability can be significantly reduced.

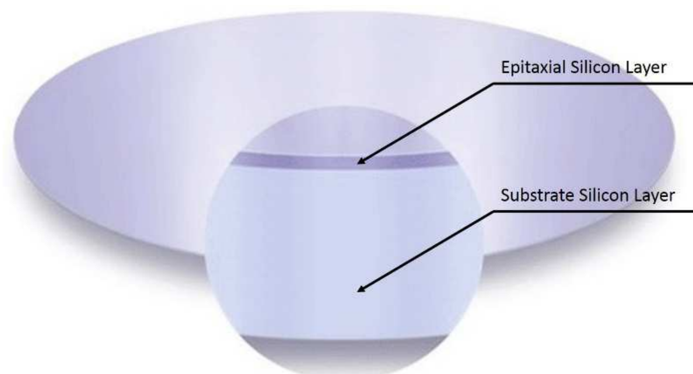

Fig. 2 Typical silicon wafer substrate with the epitaxial layer [4].

In electronic field, the thermal resistance is a simplified parameter characterizing the devices thermal performances and it depends strongly on the wafer thickness. As mentioned before, the substrate region has no major electrical function and the thermal resistance of nearly all power chips can be significantly improved by thinning the wafer. The lower the thermal resistance, the better the thermal dissipation, thus the better performing devices.
In order to improve the thermal resistance, the thinning of the whole wafer at the back end, i.e., after the complete device processing on the front side, is strongly required. The final thickness depends on the designed package, that depends itself on the final customer application.

1.2 Wafer thinning techniques overview

The requirement of an increasing thickness of the wafers during processing and the contrasting interest of thinner silicon in powerchip applications makes thinning techniques more and more important.
Wafer thinning is the process of removing material from the backside of a wafer to a desired final target thickness [5].
Because of its high thinning rate, mechanical grinding currently is the most common technique for wafer thinning especially in semiconductor and electronic manufacturing [6, 7, 8].
Conventional grinding is an aggressive mechanical process that utilizes a grind wheel to perform the material removal. These wheels are made by diamond grits embedded in a bonding matrix, which can be either metallic, vitrified or a resin. The main characteristic of a grinder wheel is its mesh, that is related to the density of diamond particles embedded and thus, with the size of these particles. The higher the mesh, the smaller the grit size, the smaller the roughness and the smaller the sub-surface damage (SSD).
The wafer is positioned on a porous ceramic rotating vacuum chuck with the backside of the wafer facing upwards (towards the grind wheel) (Fig. 3). Both the grind wheel and wafer chuck rotate during grind. Deionized water is jetted onto the work piece to provide cooling and wash away material particles generated during the grind. A grinding tape is applied to the front side of the wafer to protect the devices from being damaged during thinning.
The grind recipe dictates the spindle RPM, rate of material removal, and the final target thickness of the work piece.

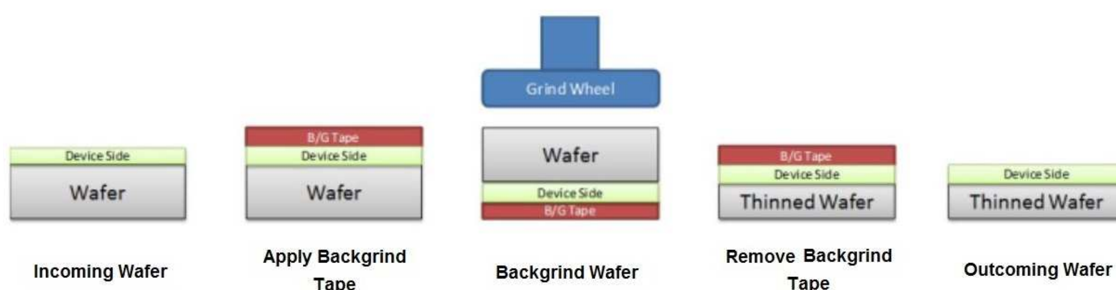

Fig. 3 Conventional mechanical wafer grinding process flow sketch [6].

All commercially available grinding systems use a two-step process including a coarse grinding that performs the bulk of the material removal and a subsequent fine grinding.
The first grinding step is performed with a rough grinding wheel (small mesh) in order to remove the bulk of the Si at high speed (in the order of a few µm per second). Yet, it causes deep SSD due to the brittle nature of the Si wafer in combination with the big grit size. This damage layer is typically confined to the first 30-20 µm below the ground surface (Fig 4) [8]. A fine grinding step is then performed to remove this damaged layer created by the coarse grinding step and reduce surface roughness by means of grids with smoothest roughness than that ones used for the first step. This step provides a mirror like surface that is the final finish of the wafer backside.
Fine grinding step provide the highest wafer and die strength as the high grit wheel removes the most subsurface damage. As a rule, as the grit increases, the wafer strength and smoothness improves, while the wafer warpage and subsurface damage decreases.
However, there is a remaining defect band near the surface. Although the fine grinding is used to remove the SSD from the rough grinding, it also introduces its own damage, though in a much smaller range, normally a few microns deep or even below 1µm.
The residual defects cause stress in the thinned wafer, leading to an additional bow and often broken wafers during handling or further processing. This means that additional thinning is necessary to remove the remaining defect layer and surface roughness after mechanical grinding. This can be done by either chemical mechanical polishing (CMP), dry etching (ADP) or wet chemical etching.

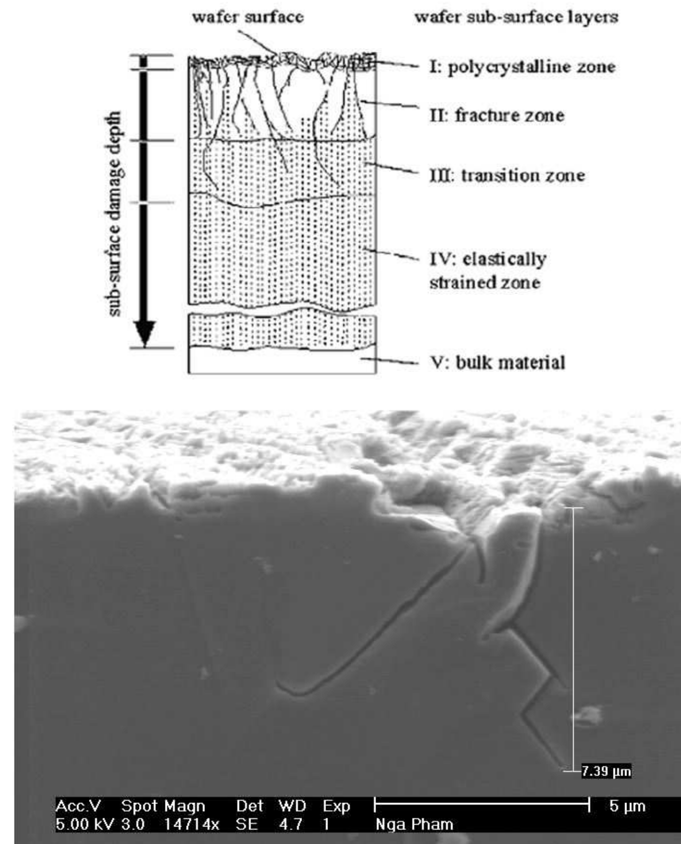

Fig. 4 Sub-Surface Damage stack (top) and SEM image of cracks (fracture zone) introduced because of the rough grinding process (bottom) [8].

In CMP, abrasive chemical slurry is used with a polishing pad to perform material removal [7, 9, 10]. During CMP processes, a wafer is rotated about its axis while being pressed face-down by a carrier and a carrier film against a rotating polishing pad covered with colloidal silica slurry with specific chemical properties (Fig. 5). The abrasive slurry, plays an important role in the material removal mechanism in CMP. Microscopic observations of polished surfaces have shown that material removal in CMP occurs as a consequence of a combination of chemical reaction of the slurry chemicals with the wafer surface materials and the repeated sliding, rolling, or indentation of the abrasive particles against the wafer surface.

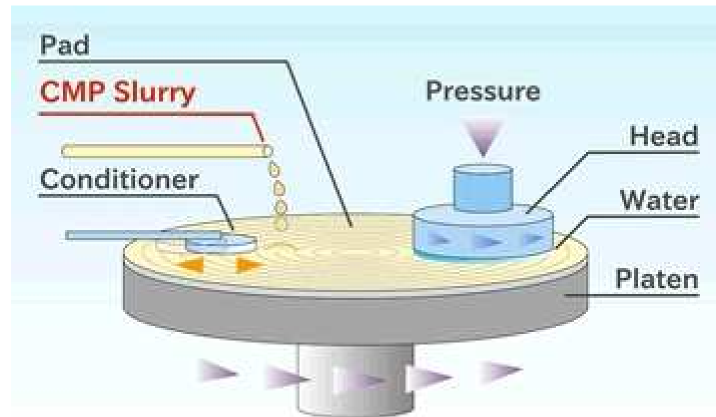

Fig. 5 Chemical Mechanical Polishing Process apparatus [10].

CMP provides greater planarization compared to mechanical grinding and low total thickness variation (TTV) values, however, it is considered a “dirtier” and more costly process. The thinning rate, however, reaches values of only a few micrometers per minute.

Atmospheric Downstream Plasma (ADP) processing utilize a magnetically controlled, inert gas, DC arc-plasma discharge [7, 11]. In the ADP source (Fig. 6a), two electrode units are directed upward and toward each other with an angle of about 90" between their axes. Each unit consists of an electrode placed inside a chamber with a water-cooled orifice. The orifice and electrode are located along the chamber axis so that the mainstream plasma gas (usually argon), when injected into the chamber, will exit through the orifice. When a dc field is applied between the two electrodes, a plasma arc is formed which exits the orifice of one electrode unit and enters the orifice of the other. The plasma is kept from the chamber walls by the flow of mainstream gas.

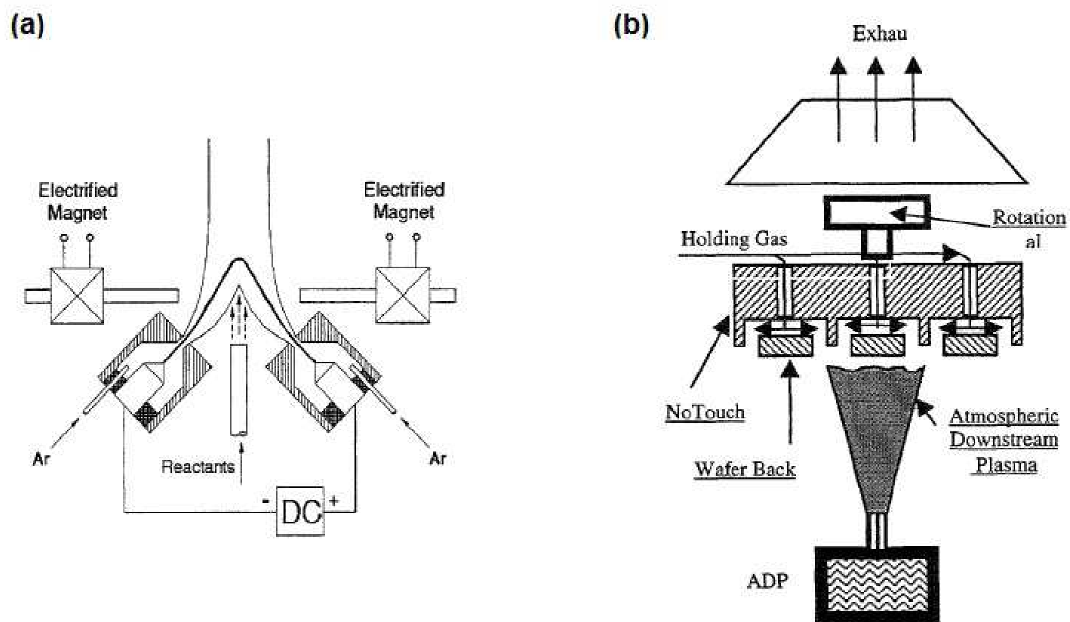

Fig. 6 (a) Schematic of the atmospheric downstream plasma source; (b) process chamber schematic of the Tru-Etch System [11].

External magnetic fields are used to direct the plasma jet parallel to the vertical symmetry axis of the combined electrode system. The vertical orientation of the plasma region creates a chimney effect and, when cold reactant gases are injected into the plasma region along its vertical axis, they are captured by the plasma. The reactant gases are heated, activated, and effectively decomposed in the plasma region which is far from the electrode units, therefore, chemical erosion of the plasma generators is eliminated. For silicon etching, tetrafluorocarbon (CF_4) is used as a reactant.

The ADP source has been incorporated into the Tru-Etch series of wafer treatment systems. The system schematic is shown in Fig. 6b.

The ADP flow is directed up and stabilized with the magnetic fields. Because of the atmospheric pressure in the process chamber, the effluent gases move up due to natural convection and are effectively removed by an exhaust located at the top of the process. The wafers are placed in holders so that the wafer side to be etched is oriented down. The wafer holders are attached to a process carousel precisely moved by a computer controlled rotational drive.

Another common thinning technique is wet chemical etching. The wafers can be immersed in a bath of etchant, which must be agitated to achieve good process control (Fig.7) [12,13]. The wafer front side must be protected by specific tape before the immersion. Megasonic agitation is commonly used with the chemical bath. An optical microscope serves as etching controller. This technique allows to simultaneously etching more than one wafer, thus it is the most widely used in mass production. KOH

is one the most commonly used silicon etch chemistry for micromachining silicon wafers. The KOH etch rate is strongly affected by the crystallographic orientation of the silicon and depends on the concentration of the KOH solution and temperature.

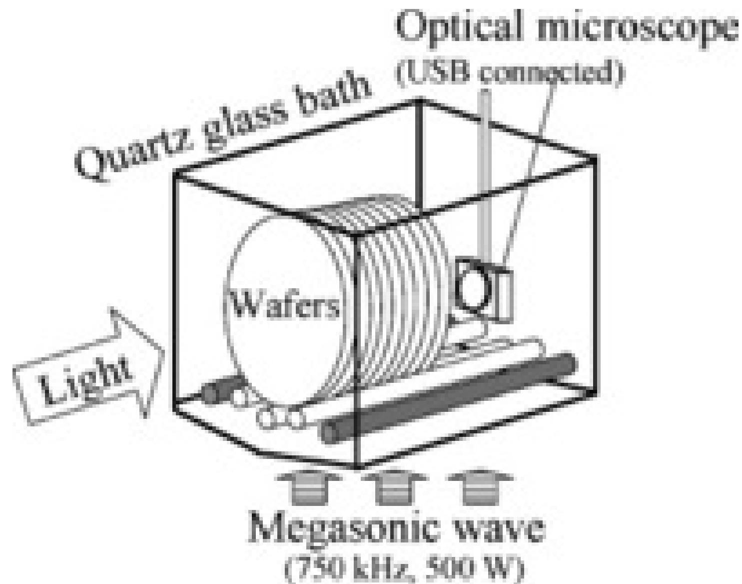

Fig. 7 Schematic drawing of a wet chemical etching bath [12].

As an alternative to immersion, to etch one side of the wafer, is spin etching, in which a thin stream of an etching agent is moved periodically over the surface of the rotating wafer (Fig. 8) [7, 14].

The front surface of the wafer is protected either by additional layers or by applying special chucks that allow the processing of thin wafers without surface protection layers or tapes. The etching agents for silicon are mostly mixtures of HF and HNO_3. The different mixtures allow different etching rates and are characterized by different selectivity, which may be important if different layers are involved.

The process chuck of the spin processor used to conduct the HF tests relies on Bernoulli's principle to fix the wafer at a constant distance from the chuck surface on a bed of nitrogen (N_2). The wafer is held in place by six edge-contact-only pins that make contact at the wafer bevel with sufficient force to center the wafer on the N_2 bed and hold it in place while the chuck rotates. The chuck rests in a process chamber, as depicted in the schematic drawing in Fig.8.

The process chamber can have up to four independent process levels, three of which dispense different process chemicals (or chemical blends) and one of which is dedicated to DI-water rinsing and nitrogen drying. The process chuck rotates clockwise or counterclockwise within the process chamber while the medium is dispensed. The

different chemistries are dispensed onto a spinning wafer at three dedicated process levels, allowing for tight process control and eliminating the risk of chemical cross-contamination.

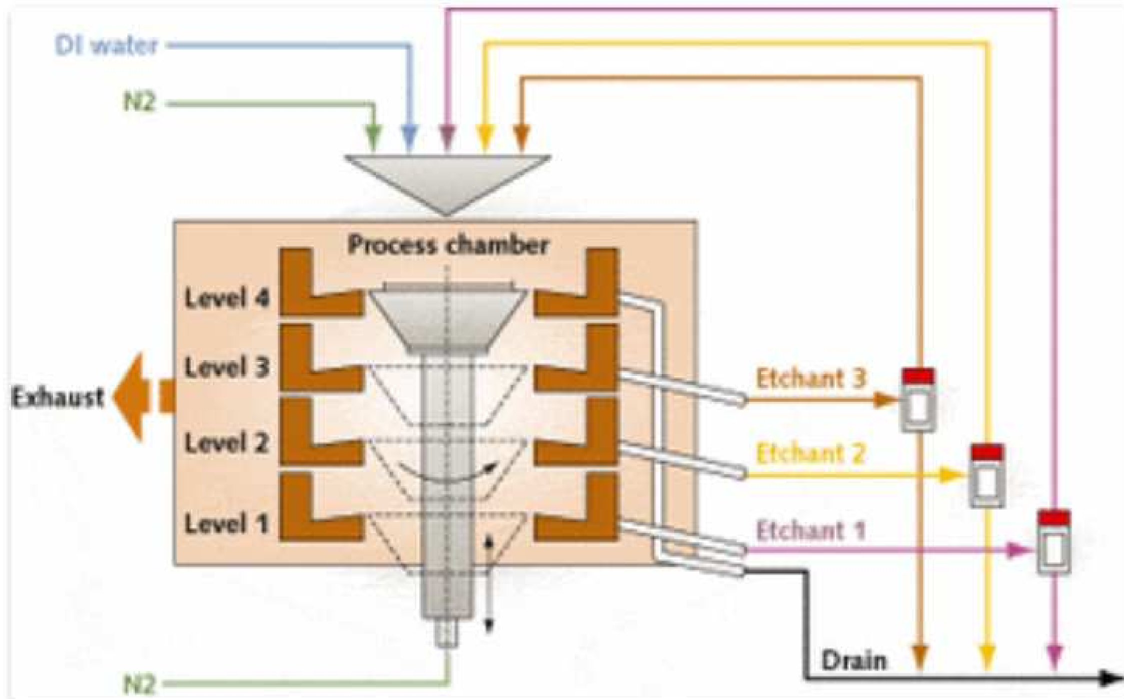

Fig. 8 Schematic drawing of the spin-processor chamber [7].

Once the wafer reached the desired thickness and surface finishing, further production steps, such as backside contact formation, are needed. All these steps are affected by the wafer history, i.e., the processes that result in a sequence of layers on the wafer front side that generate different internal stresses on the wafer. In addition, thin wafers are very flexible, which is the biggest problem for conventional handling tools.

1.1.1 Temporary bonding process and Taiko process

Nowadays, in order to overcome handling issues, wafer thinning process in mass production is carried out using mainly two approaches, the temporary bonding and the so-called Taiko processes.

Temporary bonding process is an EV Group (Electron Vision Group) invention covered by United States Patent and Trademark Office [15].

In the temporary bonding approach, the original thick and rigid device wafer is bonded onto a carrier wafer prior to the thinning step being performed.
The process for temporary wafer bonding is shown in Fig.9. The front side of the carrier wafer will be coated with the adhesive, and the wafer will undergo an initial bake to remove the solvent. The device wafer, after the application of a protective layer, will be brought into contact with the adhesive-coated carrier wafer under vacuum and pressure conditions [16, 17, 18, 19].

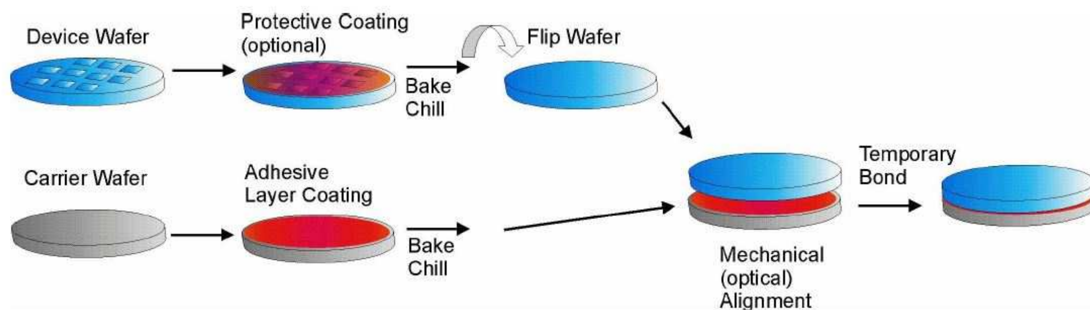

Fig. 9 Temporary bonding process flow [16].

Once the product wafer is temporarily bonded to the carrier wafer, which provides sufficient mechanical support, it is ready for mechanical grinding and next backside processing steps which generally may include, depending on the type of fabricated devices on the front side, lithography, DRIE etch, insulator/barrier deposition, CMP, metallization deposition, etc.
After completion of the backside processing steps, the thin device wafer can be released from the carrier wafer.
The most commonly used methods for debonding, depending on the kind of adhesive material employed, are represented in Fig.10. In the first method, the removable thermosets (the protecting coating of device wafer and the adhesive layer coating of the carrier wafer) can be completely decomposed at temperatures above 350ºC in nitrogen atmosphere within 15 minutes without leaving any residue. Then the thinned wafer can be carefully removed from the carrier using a wedge-off motion. The second method involves heating the substrates uniformly to the debonding temperature (in most cases, typically above 200ºC) while they are locked into a rigid frame with top and bottom heaters. Then, the wafers are slide apart in a controlled manner such that the wafers stay parallel to each other until completely apart.

Once the wafers are separated, the thin wafer is safety transferred to a single wafer-cleaning chamber, where the remaining adhesive is removed with an appropriate solvent.
This solvent is dispensed on the device wafer and allowed to soak for a period of time. During soaking, the solvent is agitated using a proprietary tool developed to better dissolve the polymer. As the polymer dissolves, the wafer is spun and sprayed with additional solvent to allow complete cleaning. A final high-speed spin is used to completely dry the wafer.

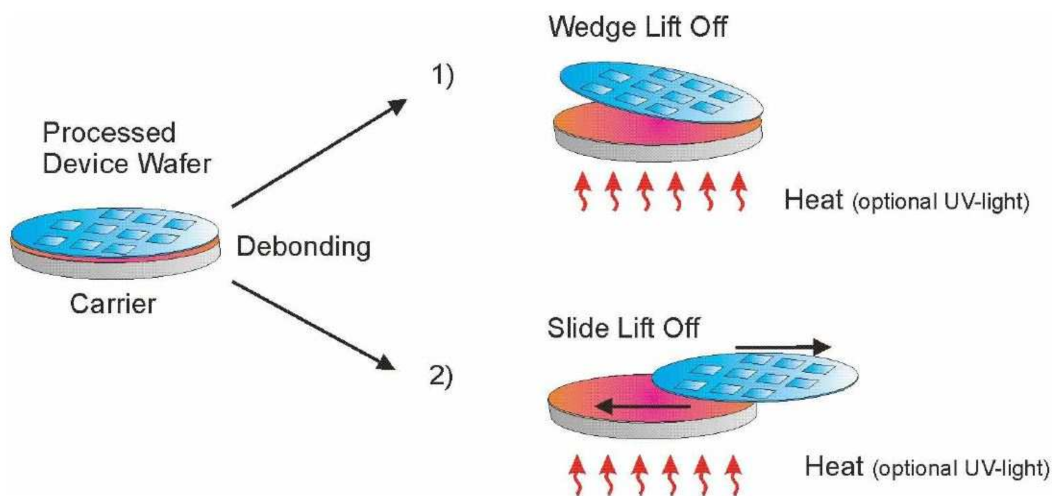

Fig. 10 Debonding methods [16].

The selection of a suitable temporary adhesive is the key to success. The major requirements of temporary adhesives are related to its process flow, thermal stability, chemical resistance, and mechanical strength.
Thermal stability of temporary adhesives relates to the ability of the material to resist decomposition and outgassing during exposure to high process temperatures over periods of time. The commonly reported modes of adhesive failure after exposure to high temperatures are the complete delamination of the thinned wafer from the carrier.
The adhesive must be resistant to a wide range of semiconductor chemicals that it will contact, from solvents and acids to plating solutions and cleaning agents.
Mechanical hardness and strength of the adhesive becomes important during the wafer thinning process and during permanent bonding, otherwise the thinned wafer will flex and prevent bonding.
Adhesives for the bonding process must have a good adhesion to a variety of semiconductor substrates and should possess adequate flow properties to flow into

structures on the front side of the device wafer to provide good bonding quality. In addition, the adhesives must be easy to apply and exhibit minimal total thickness variation (TTV) across wafers.

Finally, it must have a very gentle debond process imparting the least amount of stress on a fragile wafer.

The wafer carrier must also meet certain requirements like ability to align through the carrier and the adhesive and to be a non-contaminating material (the most diffused are silicon and glass). In addition, wafer carrier must have similar thermal expansion coefficient of device wafer, a diameter dimension able to support device wafer edge and it must have total thickness variation similar to the device wafer.

A temporary wafer bonding/debonding approach allows using standard wafer processing equipment for backside processing of thin wafers. A thin semiconductor wafer bonded to a carrier wafer resembles a thick semiconductor wafer in terms of geometrical and thermal properties. The bonded device wafer can be processed without the need for special thin wafer components.

The Taiko backgrinding process is a DISCO Corporation invention covered by United States Patent and Trademark Office [20].

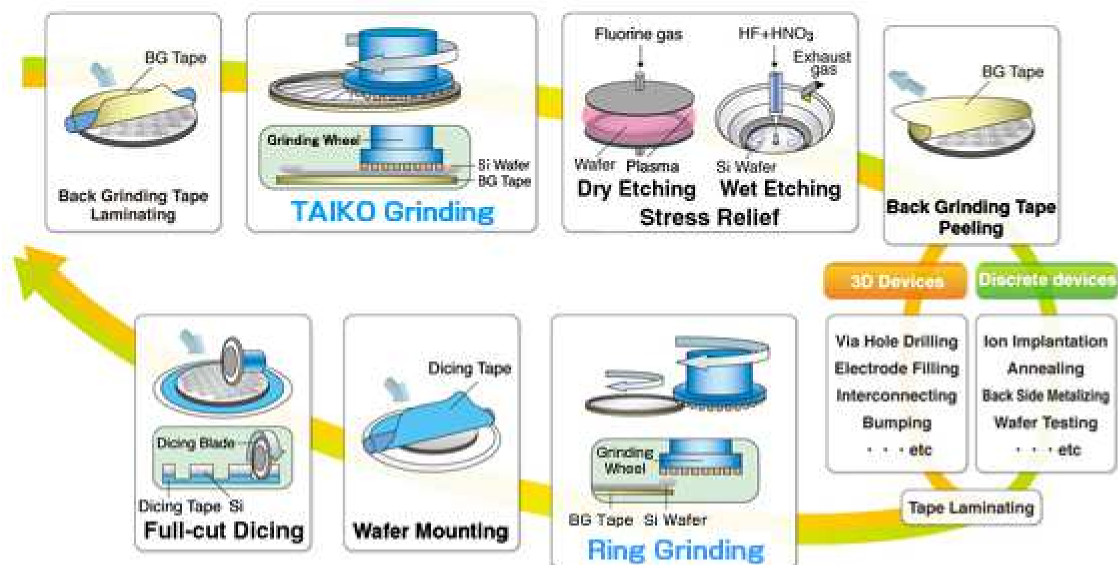

Fig. 11 Taiko Backgrinding process. [21]

In the Taiko approach, Fig.11, the front side of the wafer, with a plurality of devices, is covered with a proper material to protect the device front end during the subsequent processes. Then, the semiconductor backside is thinned removing the semiconductor material. However, the grinding wheel has a small diameter than the wafer one, and the

grinding process is done in a way that only the inner portion is thinned, whereas the rim edge of the background wafer has the original thickness of the wafer [22, 23].
Further backside processing steps, like wet and dry etching, can be performed and then the protective layer on the semiconductor wafer front end can be removed. Based on the semiconductor device typology the backside is processed to complete the device structure (implantation, thermal processes, metallization, etc…), managing the obtained thinner wafer.
Taiko approach allows to reduce the wafer thinning minimizing the wafer warpage and improving the semiconductor wafer strength. A comparison between conventional thinned wafer and Taiko grinded wafer, before edge removal, is shown in Fig.12. The thicker edge allows a self-support of the grinded wafer, while the conventional wafer shows a wide warpage. Different solutions for the removal of the thick ring are available, such as ring grinding, circle cut and direct dicing.

Fig. 12 Taiko wafer vs. conventional wafer. [23]

1.3 Thesis objectives

The main objective of this thesis project is to reduce the thermal resistance of the devices without reducing the wafer thickness but by exploiting the excess material as a heat sink.
The idea is to replace a large amount of silicon selectively removed by a local wafer thinning with a conductive material like copper. Therefore, the large amount of unused material, which would cause only heat increasing, becomes useful.

The first thesis goal is to develop a suitable process flow optimizing the parameters of each step and make it repeatable. The second thesis part is devoted to undergo the backside of the electrically good devices with the new process flow and hence compare thermal and electrical performances with those of standard good devices without a treated backside.

This new process flow offers the advantage of maintaining the wafer "self-support" and allow working with already existing technologies saving on both dedicated thinning technologies and handling technologies.

That concept is a completely new idea covered by United States Patent and Trademark Office [24]. Fig. 13 shows a drawing of a final new device section view compared with the final standard one. The front side structure belongs to a generic planar device and it is the same for new devices and the standard ones. The difference lies on the backside structure.

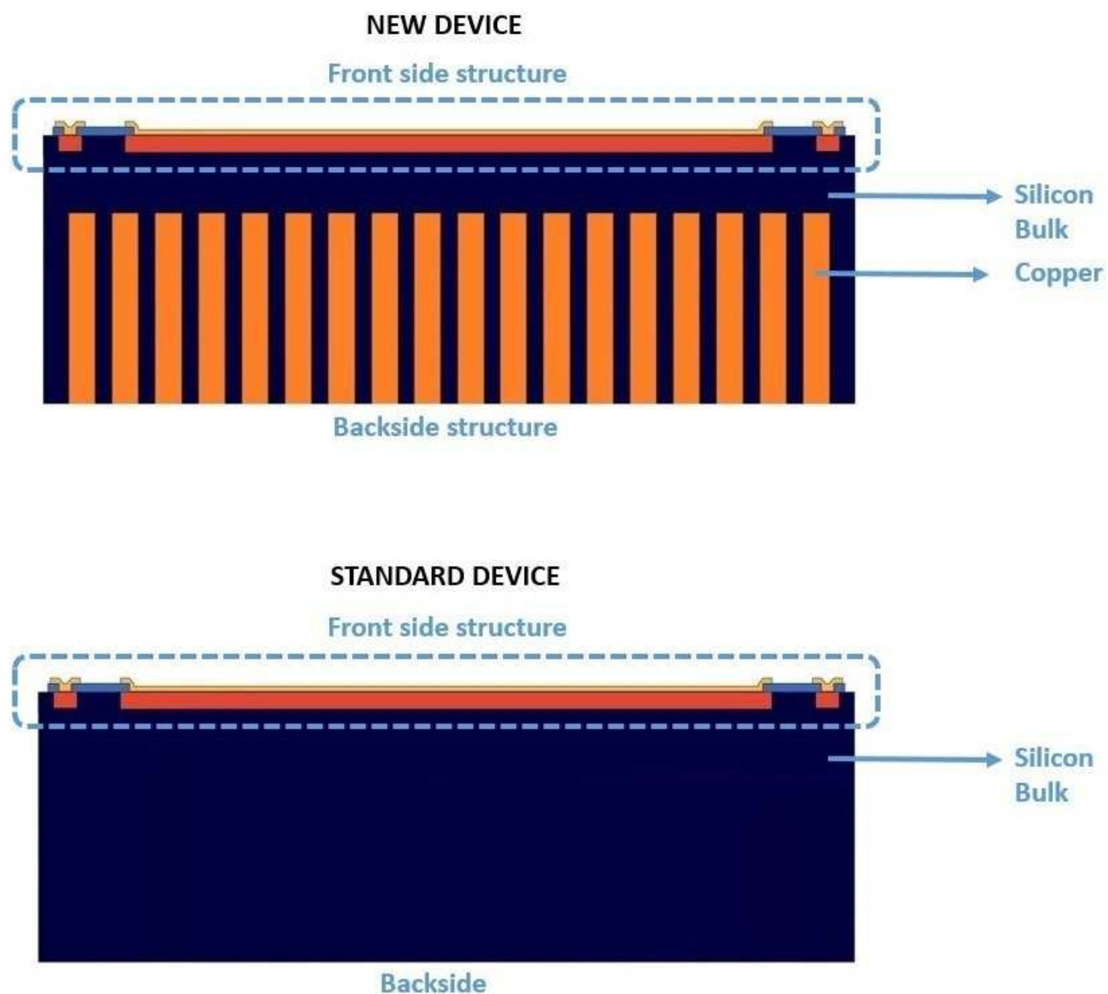

Fig. 13 Comparison between New and Standard devices' section view.

1.4 Thesis structure

The thesis is arranged into seven Chapters, the first one giving a brief introduction to the semiconductor wafers and thinning methods. This is followed by the purpose of the study as well as the outline of the thesis.
Chapter 2 deal with the environment in which the samples were processed, the cleanroom, and the description of the starting samples used during the thesis.
Chapter 3 presents the consolidated fabrication process flow in details.
Chapter 4 provides the section study characterization of the new process flow applied to semiconductor wafers.
Chapter 5 explains the assembly process flow of the manufactured devices.
Chapter 6 is devoted to the description of electrical and thermal characterization of new assembled devices.
Chapter 7 discusses the failure analysis results on new devices and the related root cause.
Chapter 8 presents the general conclusions together with a brief discussion of future work.
This work is the result of a collaboration among the Vishay Semiconductor Company of Borgaro Torinese (TO) and the Applied Science and Technology Department (DISAT) of the Politecnico di Torino.
All the process flow production and its characterization was performed mainly at Material and Microsystems Laboratory (Chilab) of the Politecnico di Torino, in Chivasso (TO) with the technological support of Trustech Innovation Technology at Techfab Laboratory, Chivasso (TO). The silicon wafers were supplied by Vishay Semiconductor Company of Borgaro Torinese (TO) as well as the back end processes, electrical and thermal characterization and failure analysis.

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Chapter 2

CLEANROOM AND SAMPLES

This Chapter gives an overview of the specific environment in which the thesis samples were built, the cleanroom. Moreover, the focus will move to the detailed description of the raw starting samples used during the thesis project.

2.1 Cleanroom

Product manufacturing takes place in a controlled environment called cleanroom. Cleanrooms are used in scientific research and practically every industry where small particles can adversely affect the manufacturing process. They vary in size and complexity, and are used extensively in industries such as semiconductor manufacturing, electronics, pharmaceuticals, biotech, medical device and life sciences, as well as critical process manufacturing common in aerospace, optics, military, department of energy and other critical manufacturing environments [1, 2].
A cleanroom is any given contained space where provisions are made to reduce particulate contamination and control other environmental parameters such as air flow rates and direction, pressurization, temperature, humidity and specialized filtration.
The concentration of pollutants such as dust, airborne microbes, aerosol particles, and chemical vapors must be under specified limits. People, process, facilities and

equipment inside a cleanroom also generate these contaminants, which must be continually controlled and removed from the air.
There are different kind of cleanrooms based on the kind of threated products and there are classified by how clean the air is.
The level to which these particles need to be removed depends upon the standards required [1, 3, 4].
The most frequently used standard is the U.S. General Service Administration's standards (known as Federal Standard 209E). The FS209E is a document that establishes standard classes of air cleanliness for airborne particulate levels in cleanrooms and clean zones.
In FS 209E, the number of particles equal to and greater than 0.5µm is measured in one cubic foot of air, and this count is used to classify the cleanroom.
However, as the need for international standards grew, the Internal Standard Organization (ISO) established a technical committee and several working groups to delineate its own set of standards.
The ISO 14644-1 standards classify a cleanroom by the number of particles per cubic meter equal to and greater than 0.1µm.
The two specifications does not match up because of the ISO 14644-1 is based on 0.1 µm whereas FS 209E was based on 0.5 µm (see Tab.1). FS 209E contains six classes, while the ISO 14644-1 classification system adds two cleaner standards and one dirtier standard. The "cleanest" cleanroom in FS 209E is referred to as Class 1; the "dirtiest" cleanroom is a class 100000. In ISO 14644-1 the "cleanest" cleanroom is a class 1 and the "dirtiest" a class 9. ISO class 3 is approximately equal to FS209E class 1, while ISO class 8 approximately equals FS209E class 100000.

FED STD 209E			0.1µm		0.2µm		0.3µm		0.5µm		1µm		5µm	
			m3	ft3	m3	ft3	m3	ft3	m3	ft3	m3	ft3	m3	ft3
SI	ENG	ISO CLASS 1	10	0.28	2	0.056								
		ISO CLASS 2	100	2.8	24	0.67	10	0.28	4	0.1				
M1.5	1	ISO CLASS 3	1000	28	237	6.7	102	2.8	35	0.9	8	0.2		
M2.5	10	ISO CLASS 4	10000	283	2370	67	1020	28	352	9	83	2		
M3.5	100	ISO CLASS 5	100000	2831	23700	671	10200	288	3520	99	832	23	29	0.8
M4.5	1,000	ISO CLASS 6	1000000	28316	237000	6711	102000	2888	35200	996	8320	235	293	8
M5.5	10,000	ISO CLASS 7							352000	9967	83200	2355	2930	82
M6.5	100,000	ISO CLASS 8							3520000	99674	832000	23559	29300	829
		ISO CLASS 9							35200000	996743	8320000	235593	293000	8296

Tab. 1 Comparison between cleanroom standards FS 209E and ISO 14644-1 [3].

In the last years, Federal Standard 209E has not been an active specification but its terminology is still around. The main reason is the ISO 14644-1 cleanroom classification does not do much to identity the class. The Federal Standard 209E is more intuitive. For example, an ISO Class 6 shows 35200 particles at 0.5 µm per cubic meter of air, whereas the Federal Standard class 1000 (which is the equivalent of ISO class 6)

means 1000 particles at 0.5 µm per cubic foot of air. Both FS 209E and ISO 14644-1 assume log-log relationships between particle size and particle concentration. For that reason, there is no such thing as zero particle concentration. Ordinary room air is approximately class 1000000 or ISO 9.

The key component to control the air cleaning is the High Efficiency Particulate Air (HEPA) filter that is used to trap particles that are 0.3 µm and larger in size [1, 3]. All of the air delivered to a cleanroom passes through HEPA filters, and in some cases where stringent cleanliness performance is necessary, Ultra Low Particulate Air (ULPA) filters are used.

HEPA (High Efficiency Particulate Air) filters have minimum efficiency of 99.97% at 0.3 µm the Most Penetrating Particle Size (MPPS). This type of filter is usually used in ISO Class 5 (100) to ISO Class 8 (100000).

ULPA (Ultra Low Penetration Air) filters have a minimum efficiency of 99.9997 at 0.12 µm MPPS. This type of filter is usually used in ISO Class 4 (10) to ISO Class 1.

In addition to the air filtration, the air flow should take into account too.

Two major types distinguish the methods of cleanroom ventilation: the turbulently ventilated flow and the unidirectional flow [3, 5]. Turbulently ventilated cleanrooms are also known as ‘non-unidirectional’. Unidirectional flow cleanrooms were originally known as ‘laminar flow’ cleanrooms. The unidirectional type of cleanroom uses very much more air than the turbulently ventilated type, and gives a superior cleanliness. These two types of cleanroom are illustrated in Fig.1.

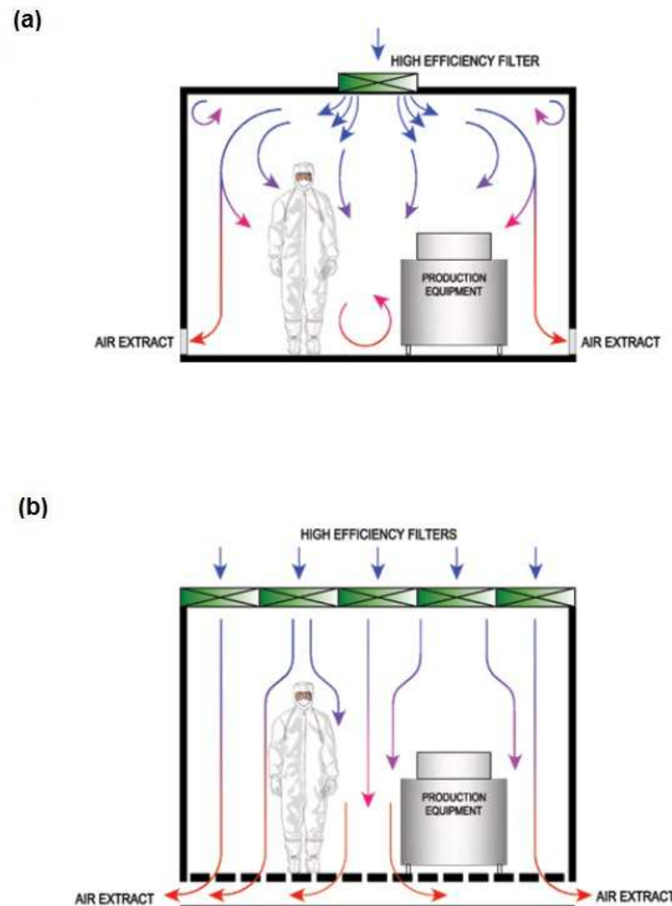

Fig. 2.1 Types of cleanroom; (a) Turbulently ventilated cleanroom; (b) Unidirectional flow cleanroom [5].

Figure 1a shows a turbulently ventilated room receiving clean filtered air through air diffused from the ceiling. This air mixes with the room air and removes airborne contamination through air extracts at the bottom of the walls. The air changes are normally equal to or greater than 20 per hour, this being much greater than that used in ordinary rooms, such as in offices. In this cleanroom, the contamination generated by people and machinery is mixed and diluted with the supply air and then removed.

Figure 1b shows the basic principles of the unidirectional flow room. High efficiency filters are installed across a whole ceiling (or wall in some systems) and they supply air. This air sweeps across the room in a unidirectional way at a speed of around 0.4 m/s (80 ft/min) and exits through the floor, thus removing the airborne contamination from the room. This system uses more air than the turbulently ventilated cleanroom, because of the directed air movement; it minimizes the spread of contamination about the room and sweeps it out through the floor.

Clean air devices, such as unidirectional benches or isolators, are used in both turbulently and unidirectional ventilated cleanrooms. These machines will give a localized supply of filtered air and enhances air conditions where required, e.g. at the area where the product is open to contamination.
ISO Class 1 through 5 are recommended to be unidirectional airflow designs, as well as ISO Class 6 through 9 are recommended to be non- unidirectional airflow designs.
Personnel selected to work in cleanrooms undergo extensive training in contamination control theory [1]. They enter and exit the cleanroom through airlocks, air showers and/or gowning rooms, and they must wear special clothing designed to trap contaminants that the skin and the body naturally generate. Depending on the room classification or function, personnel gowning may be as limited as lab coats and hairnets, or as extensive as fully enveloped in multiple layered bunny suits with self-contained breathing apparatus like the human represented in Fig. 1. Cleanroom clothing is used to prevent substances from being released off the wearer's body and contaminating the environment. The cleanroom clothing itself must not release particles or fibers to prevent contamination of the environment by personnel. This type of personnel contamination can degrade product performance in the semiconductor and pharmaceutical industries and it can cause cross-infection between medical staff and patients in the healthcare industry for example. Cleanroom garments include boots, shoes, aprons, beard covers, bouffant caps, coveralls, face masks, frocks/lab coats, gowns, glove and finger cots, hairnets, hoods, sleeves and shoe covers. The type of cleanroom garments used should reflect the cleanroom and product specifications. Low-level cleanrooms may only require special shoes having completely smooth soles that do not track in dust or dirt. However, shoe bottoms must not create slipping hazards since safety always takes precedence. A cleanroom suit is usually required for entering a cleanroom. Class 10000 cleanrooms may use simple smocks, head covers, and booties. For Class 10 cleanrooms, careful gown wearing procedures with a zipped cover all, boots, gloves and complete respirator enclosure are required.
A white area and a gray area compose the cleanroom [6]. The white area is the clean ambient in which all the processes take place. The gray area has a low-level cleanroom class than the white area one and refers to the interim space between the surroundings and the white area. The pressure cascade ensures that contamination is limited and that no exterior air enters the white area. The service area is located in the gray area i.e. changing rooms and the servicing and repair of technical systems. A wall or a curtain separates the white and gray areas.
Since this thesis project involves scientific research related to semiconductor manufacturing processes, all the production steps were conducted in cleanrooms. In particular, the whole process flow (see Chapter 3, Section 8) was carried out at Chilab

and Techfab cleanrooms [7, 8]. They are equipped with a yellow area because yellow lighting is necessary during photolithography process (see Chapter 3, Section 2), in order to prevent unwanted exposure of photoresist to light of shorter wavelengths.
Three different areas compose these cleanrooms:

- ISO 14644 Class 5 (U.S Fed-Std 209D Class 100) yellow area validated facility (15 m^2);
- ISO 14644 Class 6 (U.S Fed-Std 209D Class 1000) validated facility (45 m^2);
- not classified gray area, but approximately a ISO 14644 Class 7 (U.S Fed-Std 209D Class 10000) as measured (90 m^2).

During the sample transport from one cleanroom to another, the samples were properly sealed.

2.2 Samples

Starting thesis samples consists of a semiconductor wafers, as previously explained (Chapter 1 Section 1).
In order to test and subsequently fix the process flow settings, some monitor wafers were processed before the electrically good epi wafers. A monitor wafer is a slice of semiconductor for use in testing and controlling semiconductor fabrication lines and processes. Although monitor wafers are substantially the same as prime polished wafers with respect to cleanliness, and in some cases flatness, other specifications are generally less rigorous. The main difference between a monitor wafer and a prime polished wafer is the absence of the epi layer, thus without good devices on the front side. This allows a more cost-effective solution for non-critical wafer applications.
Prime polished epi wafers with front side devices were processed after the conclusion of the process flow settings.
Both monitor wafers and epi wafers used in the thesis project were 6-inch n-type silicon wafers with (100) lattice orientation. The bulk resistivity and the bulk doping were 0.0035 Ω.cm and 10^{21} cm^{-3} respectively.
Although the new process only involves the backside of a silicon wafer, any kind of electronic device can be present at the front side; it makes no difference if there is a diode, MOSFET, IGBT and other devices.
The electronic devices at the front side chosen as starting samples for the thesis project are standard planar power PiN diodes still in production. Standard planar power diodes availability and the related quantity of the electrical and thermal characterization data is the reason of this choice.

In power electronic circuits, planar power diodes are used mainly as power switches to regulate the duration of current flow; there are many types according to the desired application.
A diode is a two-terminal electronic component that conducts primarily in one direction thanks to the depletion process at the junction; it has low (ideally zero) resistance to the flow of current in one direction, and high (ideally infinite) resistance in the other. A power diode must be capable of controlling the flow of power to loads with low (ideally zero) power dissipation.
The three main electrical parameters that describe the diode behavior are the forward voltage drop, the leakage current and the breakdown voltage. The forward voltage drop is the voltage across the diode when it allows the current flow. The leakage current is the current value when the diode is inversely polarized. The breakdown voltage is the maximum reverse voltage that the diode can support before breaking.
An ideal diode should exhibit the current–voltage (i–v) characteristic shown in Fig. 2.2a. In the forward conduction mode, the first quadrant of operation in the figure, it should be able to carry any amount of current with zero on-state voltage drop. In the reverse blocking mode, the third quadrant of operation in the figure, it should be able to hold off any value of voltage with zero leakage current. An ideal device is able to sustain an infinite amount of potential in reverse bias, thus the breakdown voltage is infinite.

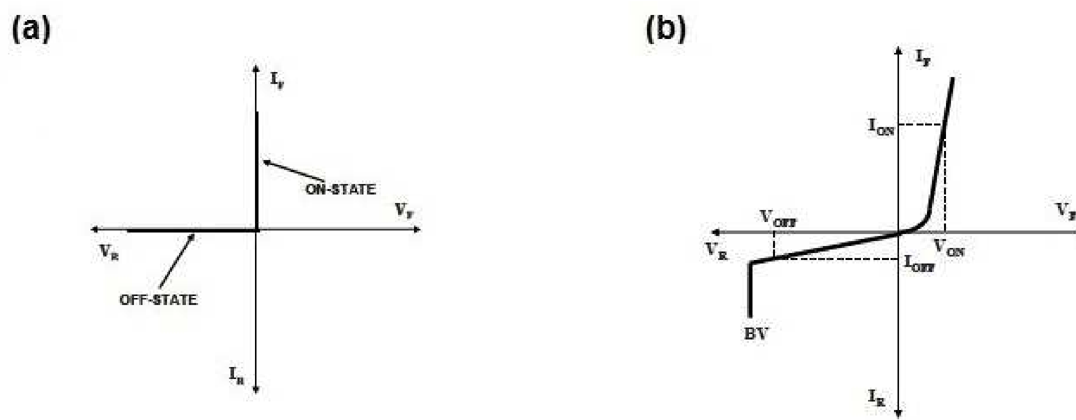

Fig. 2.2 Current-Voltage (I-V) characteristics (a) of an ideal diode and (b) of a typical real diode [9].

Further, the ideal rectifier should be able to switch between the on-state and the off-state, with zero switching time.
Neither of these components exhibits the ideal characteristics that are required in power circuits to prevent power dissipation.

Real diodes exhibit the i–v characteristics illustrated in Fig. 2.2b. They have a finite voltage drop (V_{ON}) when carrying current on the on-state, leading to power loss during the conduction. They also have a finite leakage current (I_{OFF}) when blocking voltage in the off-state, creating off-state power loss. Moreover, the breakdown voltage (BV) has a finite value.

The device must have a finite size in order to produce chips that go into packages, thus, it is necessary to surround the device cells with an edge termination. That area provides the transition from the interior of the chip to the edge of the die where it is separated from other chips by using a sawing operation. Cutting out the individual chips by using diamond-coated blades produces considerable damage to the semiconductor crystal. The damaged region must be kept separated from the active area of the chip where current flow transpires to avoid degradation of the device characteristics. This problem can be addressed by using special junction terminations around the edges of the power devices, so that the depletion regions of the high-voltage junctions do not intersect with the saw lanes where the damage is located.

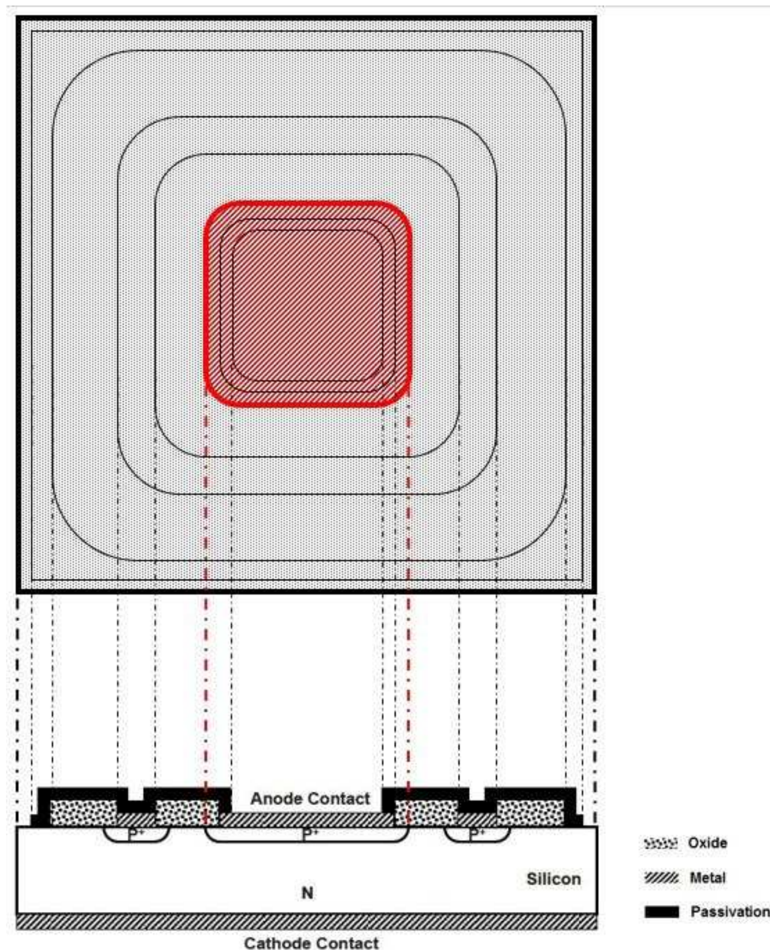

Fig. 2.3 Planar diode front view (upper) and section view (lower); active area and termination are highlighted respectively in red and grey.

In figure 2.3 a basic scheme of a generic planar PiN diode is presented; the upper square is the front view of a planar diode where have been highlighted two main areas: the active area (red) and the termination (grey). The sketch under the front view is the section view of a diode.
The active area is the central part of the device and is mainly responsible for the conduction of the device in direct bias polarization. The termination on the other hand works when the device is in reverse bias conditions. Its efficiency represents the ability of the device to reach the maximum breakdown voltage possible. The leakage current can originate both from the active area and from undesired effect in the termination.
The reverse blocking capability of a diode structure is limited by the design and performance of the edge termination. Many edge termination designs for power devices are still in use in semiconductor industries. The most common approach utilizes one or more floating field rings and field plates. In figure 2.3, there is illustrated an example with a generic planar power diode with singular ring configuration.
Numerical simulations have determined the optimum location of the floating field ring in a device. There are much kind of termination each one with its peculiar structure.
The external ring dimension and quantity depends on the desired electrical device performances. In fact, the major breakdown voltage is required; the major is the number of external rings. Depending on the desired and required Von, IOFF and BV the diode structure can change in active area dimensions, termination designs and so forth.

2.3 Samples Preparation

Once the whole front side process flow was accomplished, the wafers were taken from production line.
Before processing the epi wafers with the new process flow described in Chapter 3, the wafer front side was coated by a protective tape (Nitto BT-HR-100 [10]). This tape has a total 100µm thickness composed by 50µm thick adhesive layer and 50µm thick upper material. This material layer is able to resist to both high temperature (over 400°C) and chemicals used during the new process flow.
Further, the wafers have to be mechanically grinded and stress relief etched (see Chapter 1 Section 1) in order to start with a wafer thickness equal to standard wafer in production; this allows their direct comparison after the device assembly.
In figure 2.4 there is a typical front side view (a) and backside view (b) of the starting samples. Each small square distinguishable on the front side is a single device. The backside shows some surface staining due to chemical exposure during stress relief etching.

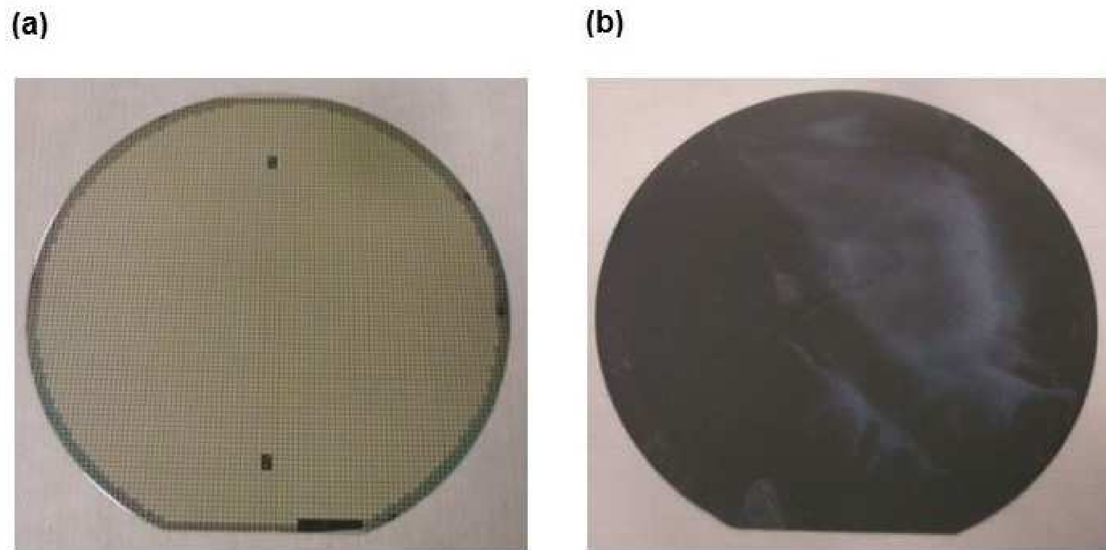

Fig. 2.4 (a) Wafer front side with multiple devices; (b) wafer backside view with a chemical polishing staining.

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Chapter 3

THE PROCESS FLOW

This Chapter is fully devoted to the detailed description of the whole final process flow designed in order to produce new and improved devices.
The next sections are each dedicated to an each step of the process in order to examine them in depth manner. The last session provides a summary of the set process flow.

3.1 Silicon Oxide Deposition

3.1.1 Introduction

Silicon dioxide (SiO_2) films have found applications in many areas, such as optics, electronics, tribology, etc [1, 2]. Silicon dioxide films are extensively used as low-index films in multilayer optical devices, scratch resistant coatings for plastic ophthalmic lenses and so on. In silicon microelectronics and power electronics, SiO_2 films are generally employed for diffusion masking and passivation or protection of silicon devices as well as gate oxide film formation in MOS capacitors [3].
The usual methods employed for forming silicon dioxide films involve oxidation of silicon at elevated temperatures ($T > 900°C$). However, the high-temperature processing

results in junction degradation. There are many low-temperature methods used in the preparation of SiO_2 films, such as evaporation, pyrolytic decomposition, plasma enhanced chemical vapor deposition, reactive sputtering and radio frequency (rf) magnetron sputtering. Film composition as well as deposition and post-deposition processing conditions strongly affect film microstructure, and, consequently, many of its macroscopic properties. A global optimization of the film properties and deposition conditions are necessary in preparing SiO_2 films for applications in a specific field [1, 2, 3]. The oxygen mixing confirms that the film properties of sputter-deposited films can be considerably improved to the same level as those of thermal oxide film [3].

3.1.2 Objective

In the present study, the first process flow step involves the deposition of a thin layer of silicon dioxide in order to electrically insulate the desired portion of the wafer surface during the final electroplating deposition. For this specific application, there is no need to have a silicon dioxide film with certain breakdown characteristics. In this case, this film must isolate selected parts of the underlying substrate in order to make effective the electroplating deposition and then it will be totally removed. Thus, it will not give any contribution to the final device working.

3.1.3 Sputtering basic principle

Silicon dioxide films were prepared by radiofrequency (rf) magnetron sputtering.
Sputtering is a physical vapor deposition (PVD) process used for depositing materials onto a substrate, by ejecting atoms from such materials and condensing the ejected atoms onto a substrate in a high vacuum environment.
The basic process is as follows [4] and is shown in figure 3.1. Electrically neutral Argon atoms are introduced into a vacuum chamber at a pressure of 10^{-5} to 10^{-6} Torr. A DC voltage is placed between the target and substrate which ionizes Argon atoms and creates a plasma, hot gas-like phase consisting of ions and electrons, in the chamber. This plasma is also known as a glow discharge due to the light emitted. These Argon ions are now charged and are accelerated to the anode target. The forceful collision of these ions onto the target ejects target atoms into the space. These ejected atoms then travel some distance until they reach the substrate and start to condense into a film. Electrons released during Argon ionization are accelerated to the anode substrate, subsequently colliding with additional Argon atoms, creating more ions and free electrons in the process, continuing the cycle. As more and more atoms coalesce on the

substrate, they begin to bind to each other at the molecular level, forming a tightly bound atomic layer. One or more layers of such atoms can be created at will depending on the sputtering time, allowing for production of precise layered thin-film structures.
There are a number of ways to enhance this process. One common way to do this is to use what is known as a magnetron sputtering system. The main difference between this and a basic DC sputtering system described above is the addition of a strong magnetic field near the target area. This field causes traveling electrons to spiral along magnetic flux lines near the target instead of being attracted toward the substrate. The advantage of this is that the plasma is confined to an area near the target, without causing damages to the thin film being formed. In addition, electrons travel for a longer distance, increasing the probability of further ionizing Argon atoms. This tends to generate a stable plasma with high density of ions. More ions mean more ejected atoms from the target, therefore, increasing the efficiency of the sputtering process. The faster ejection rate, and hence deposition rate, minimizes impurities to form in the thin-film, and the increased distance between the plasma and substrate minimizes damage caused by stray electrons and Argon ions. A way to measure the target deposition rate is the sputtering yield. The sputtering yield is defined as the number of target atoms released per incident Argon ion with certain kinetic energy. For example, if two target atoms are released per collision with an Argon ion, the sputtering yield is two.

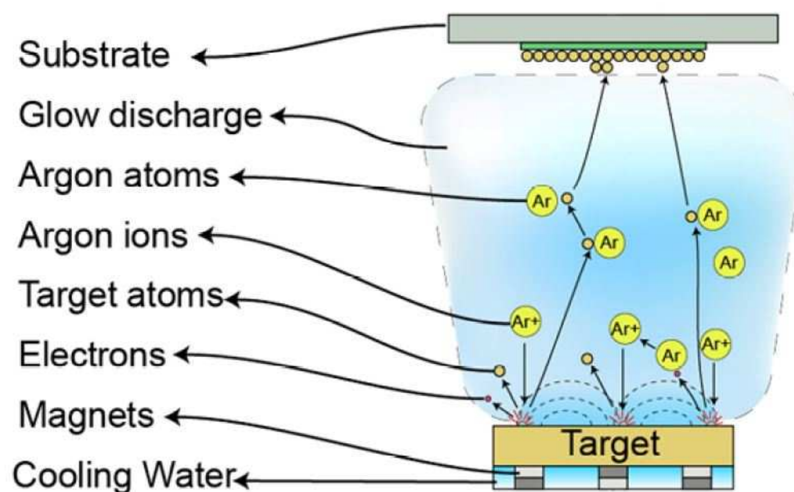


Fig. 3.1 The basic principles of a magnetron sputtering system [4].

To sputter conducting targets, a DC power supply is generally used. For insulating or semiconducting targets, an RF power supply is required with an automatic or manual impedance matching network between the power supply and the sputtering gun. The

magnetron sputtering guns are designed to work with any DC and RF power supplies for sputtering applications.

3.1.4 Equipment details and results

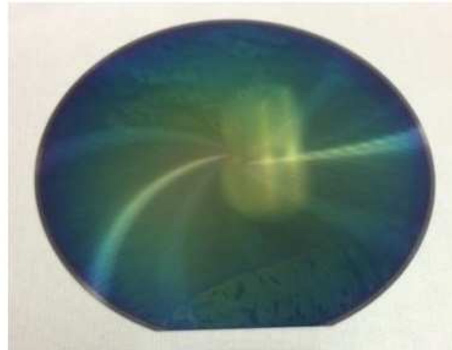
Silicon dioxide films were prepared by using a commercial RF magnetron sputtering system PVD 75 Pro Line Thin Film Deposition System (Kurt J. Lesker Company, England) available at TechFab, a Trustech Innovation Technology Laboratory, Chivasso (TO) (Fig. 3.2). The sputtering target was a 1 inch hot-pressed SiO_2 ceramic (99.995% purity) supplied by Superconductive Components, USA. The substrates employed were 6-inch n-type Si (100) 10^{21} cm^{-3} doped wafers supplied by Vishay Semiconductor Company of Borgaro Torinese (TO). The substrate was fixed directly above the target and a mechanical shutter was attached to it. An Argon/Oxygen (5%) gas mixture was introduced through a mass flow controller after the vacuum chamber was evacuated to about $2x10^{-6}$ Torr. The RF power supply was set at 150W. The growth rate was about 1.8nm/min. Before deposition, the target was usually pre-sputtered for some minutes to remove any contaminants and eliminate any differential sputtering effects with 100W RF power. The whole process duration is a bit more than 4 hours per wafer.

Fig. 3.2 Commercial RF magnetron sputtering system PVD 75 (Kurt J. Lesker Company, England) available at TechFab, Chivasso (TO) used for silicon dioxide deposition [5].

The final SiO_2 film thickness was 400nm. This thickness choice is due to the needed of an insulating layer that must also be thinner in order to permit a fast etching during DRIE process (see Section 3). The faster silicon dioxide plasma etching, the lower the damage at the hard mask. It is important that the hard mask will not be completely removed during DRIE etching. The reason will be understood in details in Section 3.5.

Figure 3.3 shows the six-inch wafer backside view after the deposition of 400nm of silicon dioxide layer and the correspondent drawing of the section view. This sketch will be useful throughout the third Chapter (to note that the drawing is not in scale).

(a) PHOTO OF THE FINAL WAFER BACKSIDE VIEW



(b) DRAWING OF THE FINAL WAFER SECTION VIEW

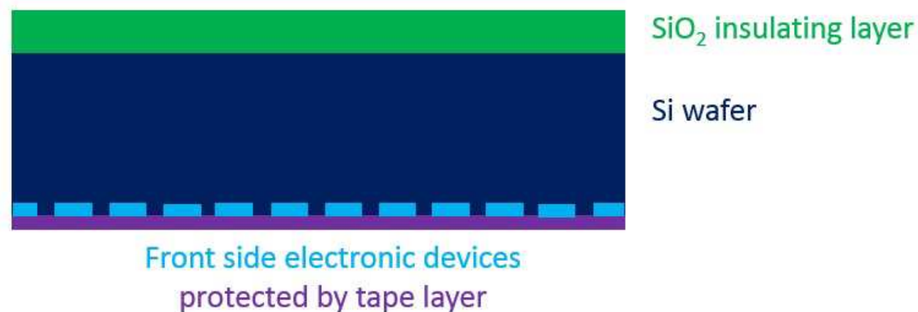


Fig. 3.3 6-inch silicon wafer after SiO_2 deposition; (a) Picture of the final wafer backside view; (b) Sketch of the final wafer section view not in scale.

3.2 Photolithography

3.2.1 Introduction

Photolithography is a fundamental process in modern semiconductor manufacturing to build the complex structures that make up a device, such as diodes and transistors, and the many wires that connect the millions of components of a circuit. Simple layers of thin films do not make a device. To create a device, layers of thin films have to be patterned, etched and coated. Photolithography combines these processes and can create millions of devices in batch [6, 7].
Photolithography steps are repeated at least 10 times, but more typically are done 20 to 30 times to make one circuit. Due to the large number of photolithography steps needed

in semiconductor manufacturing, this process typically accounts for about 30 percent of the cost of the total fabrication [6, 7].

Photolithography is an optical process of transferring geometric shapes on photomasks to the surface of a substrate. This technique generally involves stages as wafer cleaning, photoresist coating, soft backing, mask alignment, exposure, development, hard backing and post process cleaning.

A Photoresist useful for semiconductor device manufacturing, must exhibit several characteristics in addition to photosensitivity and acid resistance, they are listed below.

- Coating: must be able to form a thin, uniform, pinhole free film.
- Adhesion: adheres to the underlying substrate and does not lift off during subsequent processing.
- Sensitivity: must be sensitive to the wavelength of radiation utilized for exposure.
- Resolution: the ability to resolve the required minimum feature size being printed.
- Developing: must exhibit a significant difference in develop rate between the exposed and unexposed areas without pattern distortion.
- Process resistance: withstands plasma etch processes, high dose ion implantation, and wet etchants.
- Easy removal: must be removable by following processes.
- Thermal stability: must withstand bake processes without pattern distortion.
- Stability: the formulation must be stable enough to be stored for reasonable periods without requiring prohibitively difficult storage conditions.
- Safety: the material cannot present an acceptable health hazard.

Practical photoresists meeting above criteria are generally composed of three major components as follows.

- The polymer that is the backbone of the photoresist. Following exposure and developing the polymer is the major constituent of the patterned photoresist film.
- Photo active compound (PAC) which is the constituent of the photoresist that undergoes a reaction when exposed to light. The photoactive compound may be combined with the polymer.
- Solvent that keeps the photoresist in liquid form until after coating.

Photoresist may be classified as negative or positive photoresist.

- Negative photoresist: relatively developer soluble until exposed to light at which point the exposed portion exhibits decreased developer solubility.

- Positive photoresist: relatively developer insoluble until exposed to light at which point the exposed portion exhibits increased developer solubility.

Figure.3.4 illustrates negative and positive photoresist behavior during photolithography process. In case of negative photoresist, the light makes chemical bonds and the exposed parts will not be removed during developing. On the other hand, the light cause a bond breaking when a positive photoresist is exposed, thus the exposed parts will be removed during developing.

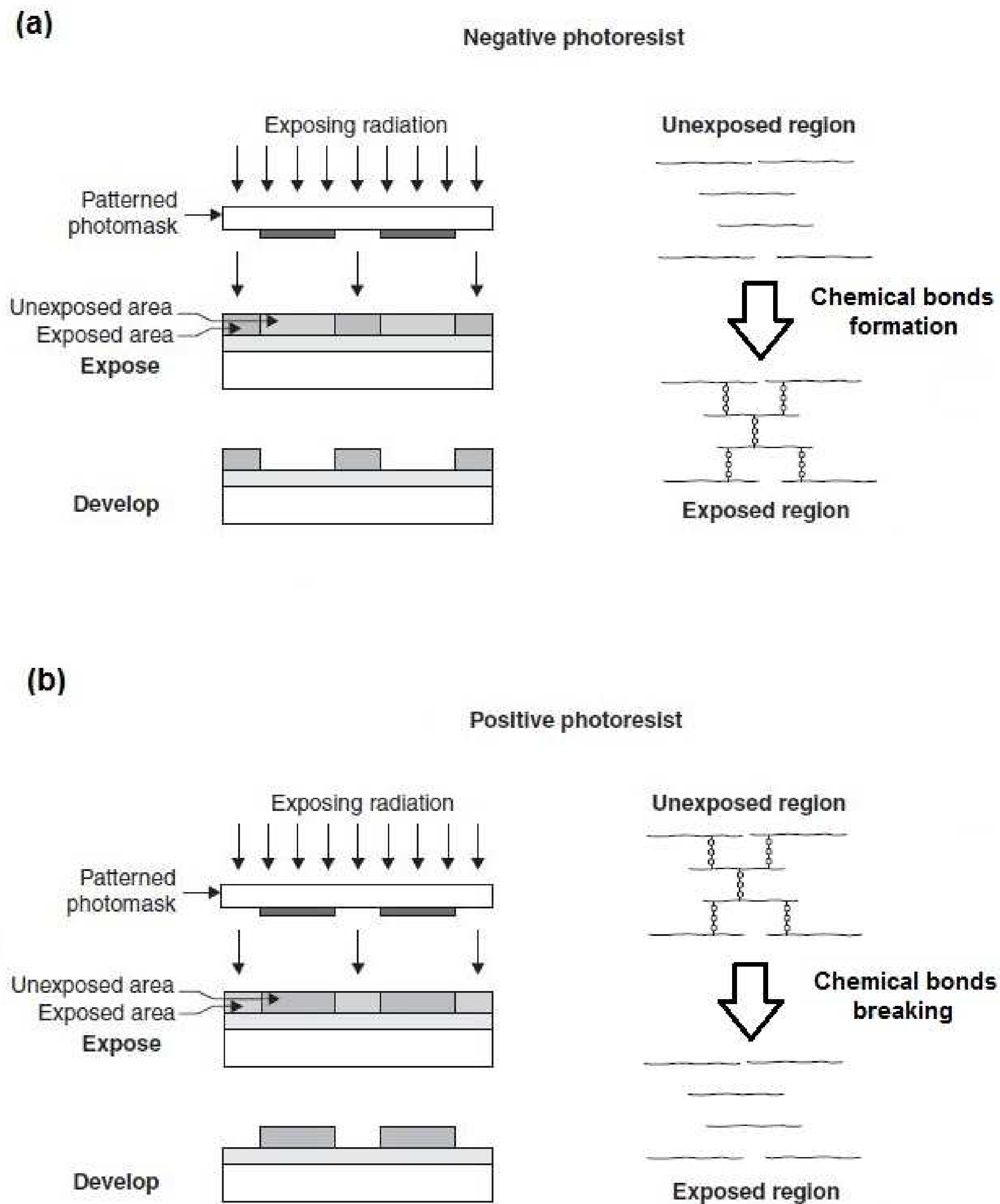


Fig. 3.4 Comparison between negative and positive photoresist; (a) photolithography process with a negative photoresist: only exposed parts survive; (b) photolithography process with a positive photoresist: only non-exposed parts remains on the substrate after developing [6].

3.2.2 Objective

The aim of this process step is to transfer the desired geometric pattern to a light sensitive thick polymer in order to further etch the silicon dioxide sputtered film and the below wafer substrate according to the chosen geometry.

The photoresist thickness required is related to the next etching step (described in next Section 3.3); in fact, this photoresist layer acts as a protective layer against subsequent plasma etching. During the plasma etching, it is important that the photoresist be not completely consumed.

3.2.3 Coating

During the spin coating process, a controlled photoresist volume is dispensed onto the wafer substrate; then the wafer is spun at a high speed to produce a uniform, partially dried, photoresist film.
Before the photoresist coating, a wafer dehydration is required on 120°C hot plate for 5 min. Thick positive photoresist AZ9260 [8] was employed for coating purpose by SPS Spin 150 Spin Coater (SPS Europe) [9]. The equipment and the basic coating process are illustrated in figure 3.5a and 3.5b respectively.
A controlled photoresist volume (about 20ml) was manually dispensed onto the center of the wafer. The coater offers a vacuum secured sample holder. The initial dispense was done with the wafer static. The photoresist is allowed to spread through the wafer rotating at a 500 RPM for 5s; then, the wafer is rapidly ramped up to a high spin speed, 2400 RPM, for 60s producing a uniformly layer with the desired thickness (from 7 up to 10 μm).
The spin coater bowl is properly designed to avoid the photoresist droplets splash back onto the wafer surface causing a non-uniform coat.
After the spin coating, the photoresist still contains too much solvent for a sufficient difference to exist in developing rates between the exposed and unexposed portion of the photoresist. In order to reduce the residual solvent level in the photoresist, a soft bake step is employed at 100°C hot plate for 10 min. Afterwards wafer hydration is required for about 1 hour – 1 hour and a half.

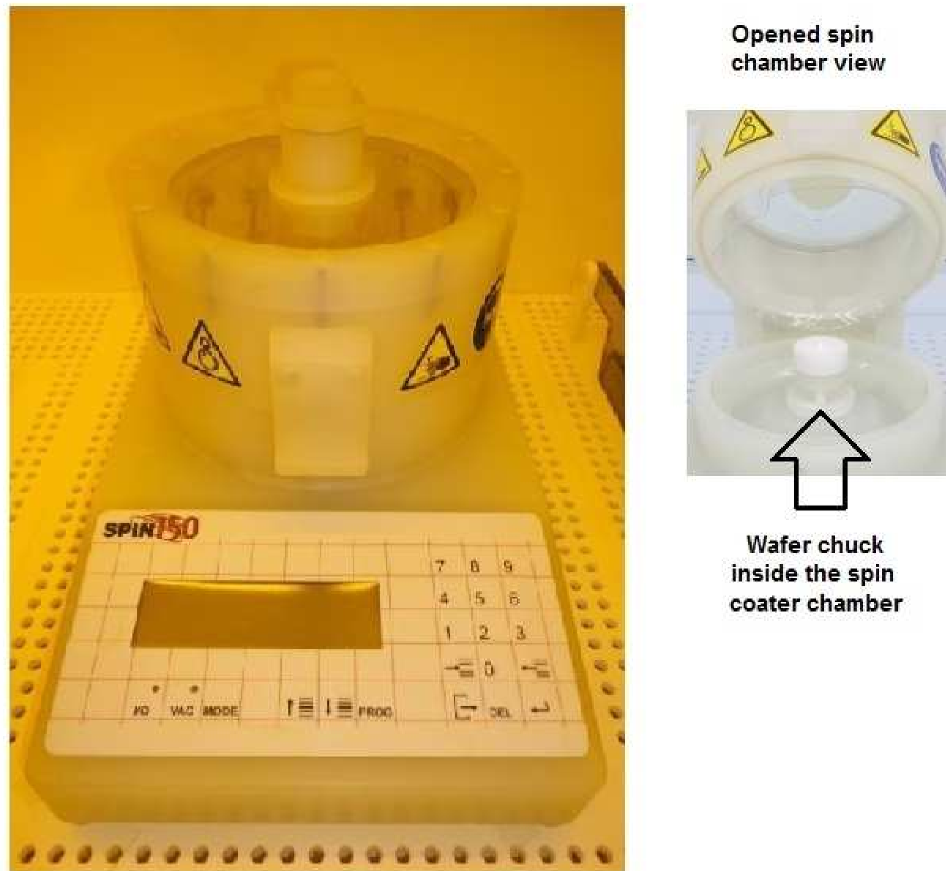
3.2.4 Exposure

3.2.4.1 Overview

Although photolithography experts have been predicting the end of optical lithography since the mid-eighties, optical lithography remains the methodology of choice for

patterning wafers in semiconductor manufacturing. The optical exposure of a wafer can occur through different techniques and tools.
The first commercially available exposure tool was the contact printer introduced in 1964.
A photomask containing a pattern for an entire wafer is brought into contact with the wafer to be patterned, hence the name contact printer.
Proximity printing system are very similar to contact printing systems with an illumination system that is typically more optimized for collimated light and a small gap introduced between the mask and wafer (5 up to 20 μm).

(a)



(b)

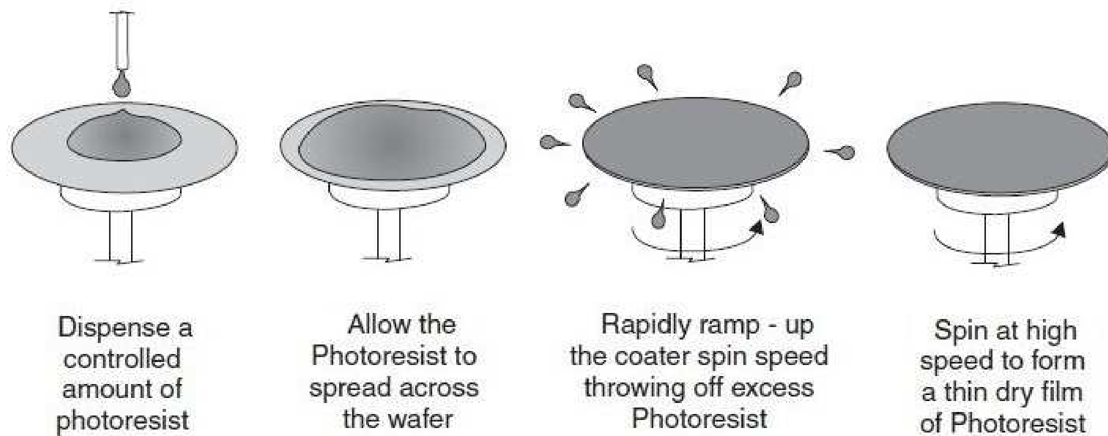


Fig. 3.5 (a) SPS Spin 150 Spin Coater used for photoresist coating with opened spin chamber view [10, 11]; (b) Photoresist spin coating process [6].

Projection printers have mask-wafer separation distances measured in centimeters and utilize lens systems to focus the mask image onto the wafer. The mask image is reproduced at the same size on the wafer, thus there is one-to-one systems (1:1).
In a step and repeat system a reticle is used that contains the patterns for one or more chips but does not contain enough chip patterns to pattern a whole wafer in one exposure. The reticle pattern is exposed onto the wafer and then the wafer stage “steps” the width of a patterned area and exposes the wafer again. By stepping and exposing multiple times the entire wafer area can be patterned.
The step and scan system is similar to step and repeat system with the difference that moves wafer and lenses contemporary. The basic principle of step and scan is that lens system is stepped to a location in the wafer and then a slit image through the lens scans the reticle image onto the wafer.
The step-and-scan approach uses a fraction of a normal stepper field (for example, 25mm x 8mm), then scans this field in one direction to expose the entire 4 x reduction mask. The wafer is then stepped to a new location and the scan is repeated.
There are some non-optical alternatives in lithography based on the utilized source used for exposure step. Extreme Ultraviolet (EUV), X-ray Lithography (XRL), Electron beam systems, Ion projection lithography (IPL). As long as economical optical lithography alternatives exist, the industry will make the safe choice and stay with optical lithography.
Of course, there are maskless lithographic techniques based either on a charged particle maskless or optical maskless methods like zone plate array lithography (ZPAL), dop-pen lithography (DPL), multiaxis electron beam lithography (MAEBL), scanning electron beam lithography (SEBL), focused ion beam lithography (FIBL), interference lithography (IL), maskless optical projection lithography (MOPL), and so on. Therefore, these endeavors require expensive instrumentation and or controlled experimental environments and none of them can be considered as a fast cost effective prototyping tool for microfabrication [14].

3.2.4.2 Experimental

The adopted lithography technique in the thesis project is the optical exposure by the contact printer. The contact printer system is illustrated in figure 3.6 and consists of the following elements.

- A mercury arc lamp centered in a parabolic or ellipsoidal reflector to collect the lamp light and direct the light into the aligner optics. The mercury lamp emits light from an area a few mms across so the lamp acts like a point source.

- A cold mirror to redirect the light and provide wavelength filtration.
- A shutter to control the time the wafer is exposed to light.
- An optical integrator creates multiple light images that are then recombined to improve uniformity.
- An aperture to block divergent light rays outside a controlled area.
- A turning mirror to turn the light towards the wafer.
- A condenser lens to create parallel light rays.
- The photomask.
- The photoresist coater wafer.

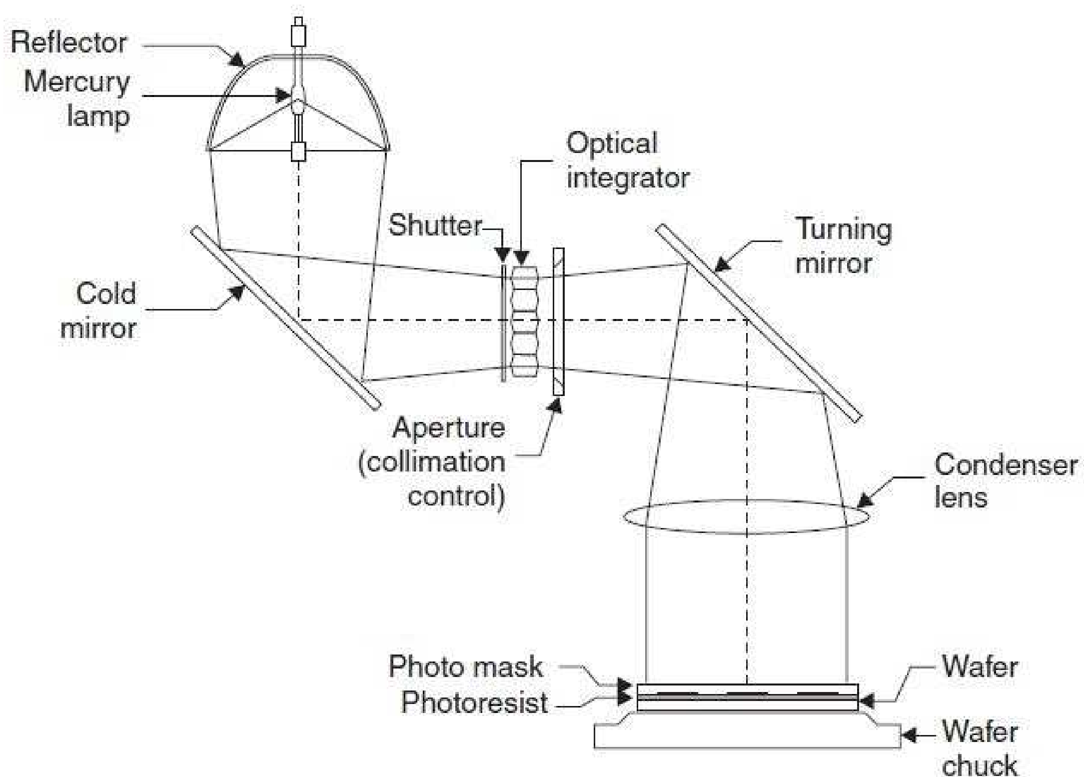


Fig. 3.6 Contact printer drawing [6].

A vacuum chuck may be moved in two horizontal directions and also move up and down a controlled distance to bring the mask and wafer in and out of contact.
In order to expose the wafer, the photomask is loaded and rotationally aligned looking through the microscope. The rotational alignment insures the mask edges are parallel to the front of the aligner. The wafer is then manually loaded onto specific chuck aligning its flat side parallel to the front of the aligner.

Since the wafer front side already has electrically good devices, there is a previous pattern on it, thus the alignment marks, which typically are crosses of boxes out toward both sides (see figure 3.7). It is necessary to pattern the back side of the wafer faithfully to the front side devices, hence the box crosses on the mask and the ones on the wafer will be properly designed. The cross set on the mask are smaller than the one on the wafer. If both crosses are centered in both sides of the wafer, the alignment is correct.
The wafer and mask must be separated during the alignment procedure so they may move independently. It is possible to put the mask and wafer in and out of contact several times during the alignment process.
Once alignment is achieved the wafer is brought up into contact with the mask and the shutter opens for a controlled time exposing the wafer.

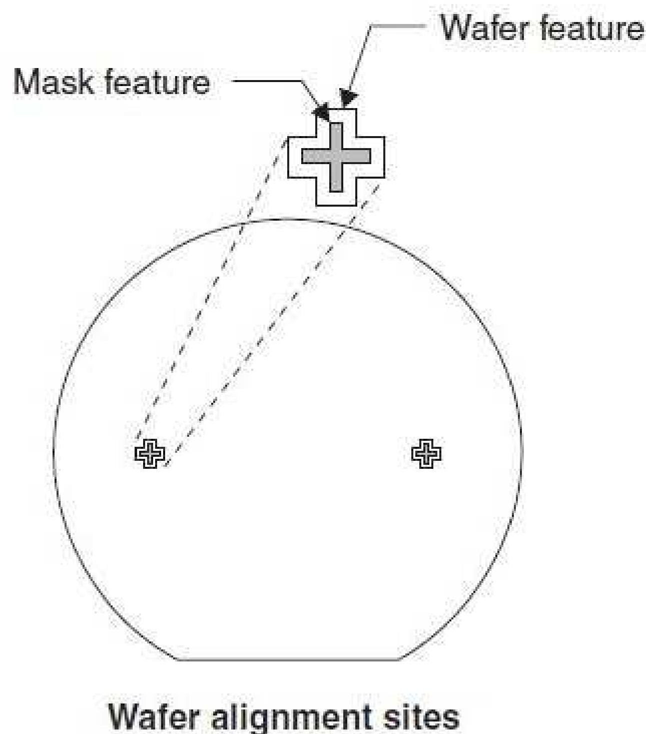


Fig. 3.7 Alignment marks [6].

Figure 3.8 shows the NXQ4006 mask aligner [12] used for the exposure of the previously coated substrate. It supports Soft/Hard pressure contact and Vacuum contact printing. The system can also print in Manual Proximity mode. It can process partial and whole substrates up to 200mm (8-inch) diameter and can be optionally equipped

with Backside Alignment and UV Nano Imprint Lithography. This aligner permits setting the pressure of the contact mode.

In order to avoid any misalignment between the front side devices and the related backside pattern, the equipment was adapted in backside alignment mode. Moreover, the exposure process was performed in contact mode with an exposure time of 180s.

During the exposure process, UV light shines through the mask, which blocks light in chrome patterned areas and lets it transmit to other transparent blanks. The transmitted light falls onto the photoresist where the exposed areas are modified distinctly than that of the unexposed areas by photochemical reactions.

The photomasks are hence an integral component in the entire procedure and manufactured by industrial companies using highly precise techniques like electron beam lithography. Quality masks are generally very expensive and depending on the complexities of intended structure, several lithographic steps with several masks are needed for fabricating one structure resulting in escalating mask costs per design to thousands of euro.

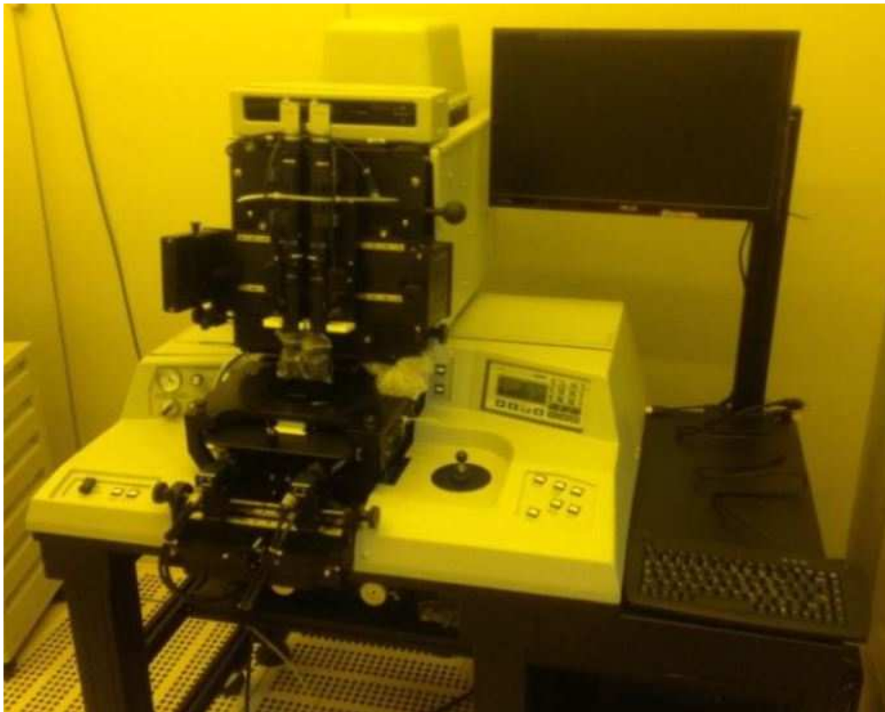


Fig. 14 The NXQ Mask Aligner Equipment [13].

The photomask allows selective irradiation of resist on the wafer surface by blocking irradiation in selected areas; consist of opaque (non-transparent to given wavelengths) and blank (transparent) parts; in photolithography chrome, and quartz respectively. These masks used in photolithography to block resist exposure to UV radiation in

selected areas; consists of chrome opaque areas supported by high quality quartz plate transparent to UV radiation.
If a particle lands on a mask or reticle (the term reticle will be used to include both masks and reticles from this point forward) and the particle is larger than the minimum resolution of the exposure system, the particle will print on every wafer exposed with the reticle in question. Reticles are typically manufactured by patterning a chrome layer on one side of a glass plate. Particles falling on the un-patterned side of the reticle will generally be out of focus and not printed, therefore only the patterned side of the reticles is susceptible to particle induced defects. If a thin film is stretched over a frame a small distance above the patterned side of the reticle, any particle falling towards the patterned side of the reticle will be blocked from reaching the pattern and will be out of focus, this is what a pellicle does. Every mask has a set of alignment windows based on the used aligning equipment thus under specific rules.

3.2.3 Development

The selective removal of exposed or unexposed photoresist is made possible by resist developers. Consequently, desired patterns are formed in photoresist after the resist development.
Once an image is exposed into a photoresist layer, depending on the tone (negative or positive) of the photoresist, the develop process either dissolves the photoresist that has been exposed or the photoresist that has not been exposed. The developer needs to remove photoresist where removal is desired and have a low attack rate on the photoresist where dissolution is not desired. The developing process must also be chosen to avoid distortion in the resulting photoresist pattern.
Once exposed, the photoresist must be developed. Most commonly used photoresists use aqueous bases as developers. Development is undoubtedly one of the most critical steps in the photoresist process. The characteristics of the resist-developer interactions determine to a large extent the shape of the photoresist profile and, more importantly, the linewidth control.
The method of applying developer to the photoresist is important in controlling the development uniformity and process latitude. In the past, batch development was the predominant development technique. A boat of some 10-20 wafers or more are developed simultaneously in a large beaker, usually with some form of agitation. With the push towards in-line processing, however, other methods have become prevalent. During spin development wafers are spun, using equipment similar to that used for spin coating, and developer is poured onto the rotating wafer. The wafer is also rinsed and dried while still spinning. Spray development has been shown to have good results

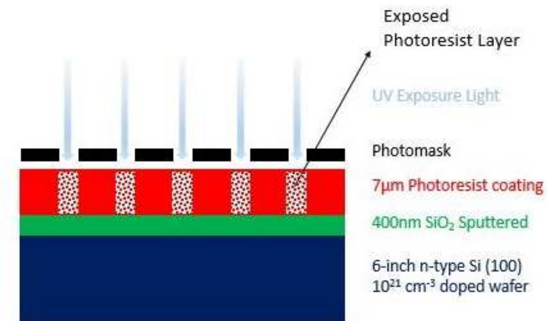
using developers specifically formulated for this dispense method. Using a process identical to spin development, the developer is sprayed, rather than poured, on the wafer by using a nozzle that produces a fine mist of developer over the wafer (Figure 1-8). This technique reduces developer usage and gives more uniform developer coverage. Another in-line development strategy is called puddle development. Again using developers specifically formulated for this process, the developer is poured onto a stationary wafer that is then allowed to sit motionless for the duration of the development time. The wafer is then spin rinsed and dried. Note that all three in-line processes can be performed in the same piece of equipment with only minor modifications, and combinations of these techniques are frequently used.
In this thesis project, the development was performed in a solution of about 1:4 of AZ400K developer and water, as suggested in the product datasheet. The support with the wafer is immersed in this prepared solution supplying some agitation for about 120s. The wafer was also rinsed and dried after developing.

3.2.4 Photolithography

The photolithography process of the starting wafer substrate previously deposited with silicon dioxide on the backside, is summarized in Fig.9 and briefly described above.
The photolithography serves to transfer the desired geometric pattern to a light sensitive polymer. The wafer is completely covered with positive photoresist by spin coating producing a uniformly layer with the desired thickness (from 7 up to 10μm).
Subsequently the wafer is exposed at UV Light which goes through the dedicated photomask. The exposure to light causes a chemical change in polymer so exposed parts become soluble in the developer and can be easily removed. After the developing, the remaining photoresist has exactly the final desired pattern.

Coating
Thick positive photoresist AZ 9260
Wafer dehydration: hot plate, 5' @ 120°C
Photoresist spinning: 1st step 500 RPM for 5 s;
2nd step 2400 RPM for 60 s.
Final Thickness: 7-8µm resist thickness
Wafer soft bake: hot plate, 10' @ 100°C
Wafer hydration: about 1-1.5h

Exposure
Quartz Mask for the backside alignment
Contac mode
Exposure time 120 s



Developing
Developer AZ 400K
Developer solution: about 1:4, AZ 400K : H_2O
Process time: about 120s
Rinse and drying after developing

Fig. 15 Photolithography process step summary.

The photomask has been designed according to both front device wafer structure and the mechanical stress simulations. The backside hole structure that causes minor wafer mechanical stress is the square geometry.
After the entire photolithography process, the wafers have been characterized at optical microscope, in order to evaluate the patterned geometry, and at profilometer in order to measure the surface profile and quantify the photoresist thickness.
Fig.10a shows a typical optical microscope image of the structure after the development and Fig.10b the correspondently typical photoresist profile.

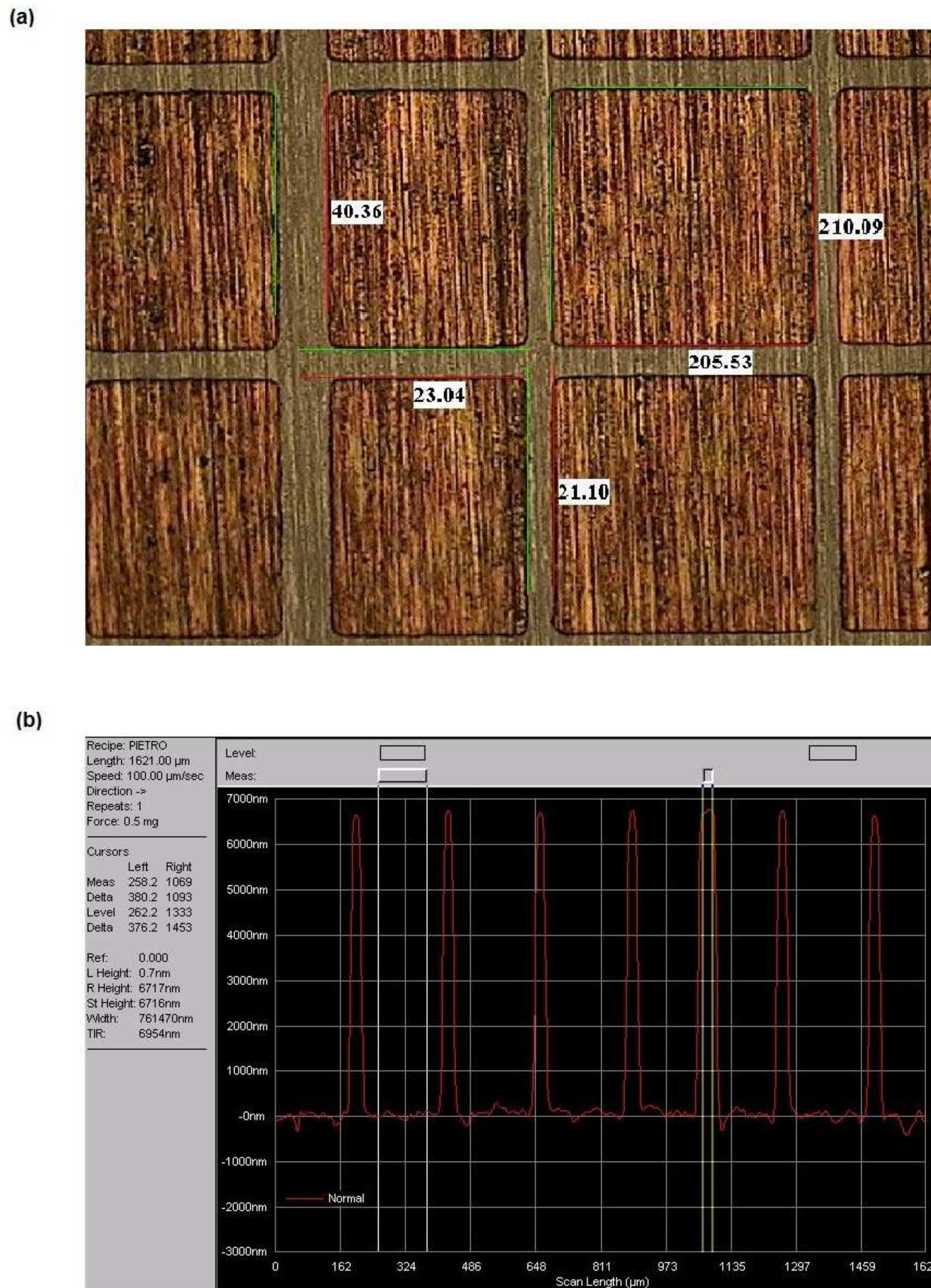


Fig. 16 Photolithography results; (a) optical microscope image with quotes in microns; (b) profilometer image.

The microscope image shows the final mask geometry that consists of larger squares according to the cutting street of the front device and the minor squares according to the mechanical simulation results (not a topic of this thesis).
The photoresist acts as a hard mask permitting to screen the wafer parts from the subsequent third process step, the Deep Reactive-Ion Etching (DRIE).

3.3 Deep Reactive-Ion Etching

The last decades have seen an ever-increasing use of plasma etching techniques, in particular for the fabrication of miniaturized devices based on silicon. Traditionally this development has been driven by the road maps in microelectronics industry, but during the last few years, the focus of the field is shifting toward the fabrication of microelectromechanical systems (MEMS). The main difference between the requirements of Integrated Circuit (IC) and MEMS fabrication is the desired structural definition: present and future IC's rely on submicron features, while, compared to structure depths of only microns in conventional ICs, MEMS structures may be several hundred microns deep, even up to the thickness of a silicon wafer [15]. MEMS applications require precise control of the widths of etched lines and spaces during pattern transfer processing. In particular, highly anisotropic etching has been required while at the same time maintaining high etch rates and high selectivity with respect to masking material.
The conventional etching techniques, like reactive ion etching (RIE), microwave plasma etching, electron cyclotron resonance (ECR) plasma etching, and magnetron-type RIE, have high plasma densities and a large number of active species, thus higher etch rates, but not high selectivity and anisotropy. A basic problem is the inability of these conventional etching methods to separately control reactions on bottom surfaces and sidewall surfaces.
The basic idea of all of the anisotropic reactive ion etching efforts today is to find a balance between trench side-wall passivation and trench bottom etching, the latter being activated through the bombardment of ions from the plasma discharge. Two main approaches can be distinguished.
The first method was introduced by Tachi et al. [16] and is based on cooling the wafer during plasma treatment, thereby greatly reducing the chemical reactions that occur on the sidewall of the sample. The main chemical reactions in plasma-assisted etching are spontaneous etching and ion-assisted reactions. The latter occurs on bottom surfaces. Energetic ions normally incident on the bottom enhance etching reactions between bottom surface atoms and adsorbed atomic species. Spontaneous etching takes place between long-lived radicals and surface atoms that exist on both the sidewall and the

bottom. This reaction produces isotropic profiles because of the random incidence and reflection of fragmented neutral atoms. Highly anisotropic etching requires dramatic suppression of this spontaneous reaction caused by the radicals. Either the reaction probability or the incident flux of atomic radicals to the sidewall surface must be reduced to obtain extremely small side etching. Controlling the substrate temperature directly suppresses this sidewall reaction. Since the reaction rate increases with the temperature of the sidewall, lower temperatures yield lower side etch rates. The bottom surface etching should only be slightly affected by this method, since the ion-assisted reaction dominates in RIE and microwave plasma etching. Hence, the low-temperature or cryogenic plasma-assisted etching should have extremely small side etching without reducing high etch rates and high selectivity. Low-temperature etching stands for plasma etching performed on a temperature-controlled electrode below 0°C. In particular, highly selective silicon etching with extremely small side etching and high etch rates are achieved by keeping the wafer temperature at -130°C to -100°C in sulfur hexafluoride (SF_6) gas RIE. Etching did not take place below -140°C because the sulfur hexafluoride (SF_6) gas, used for silicon etching, starts to freeze on the cold surface at this temperature [16].

The second is a method developed by Laermer and Schilp [17] and it is known as the "DRIE-Bosch Process" patented by Robert Bosch; this is an anisotropic dry etch process that gained popularity in high aspect ratio silicon etching for micro mechanical systems. Fluorine based inductively coupled plasma (ICP) using the Bosch process is superior in practically every aspect to wet chemical etching of silicon, except in the areas of the ability to preferentially follow crystallographic defined etch directions. The principle advantages include higher etching rates, compatibility with photo-resist masks, and the ability to produce vertical sidewalls on silicon substrates of any crystal orientation at room temperature [18].

DRIE Bosch process relies on many repetitions of alternating etch and passivation cycles.

The principle of DRIE process is shown in Fig. 3.11. The first cycle is ion-assisted etching of the silicon substrate by an etching gas (SF_6) and the second is a sidewall passivation step using a polymer-producing gas, the octafluorocyclobutane (C_4F_8). At first, passivation cycle coats the sidewalls with a protective polymer (poly-tetra-fluoro-ethylene PTFE), that prevents lateral etching. In successive etching step, a mixture of oxygen and SF_6 gas is passed. Oxygen ions etch the bottom polymer while fluoride ions etch silicon at the bottom of through-hole. Sidewalls of through-holes remain protected by polymer. The continuous repetition of such etching and passivation cycles results in high etching rate and highly anisotropic through-hole etching.

In this thesis project, the necessary deep silicon trenches are excavated by means of DRIE-Bosch process. Some testing was also done with Cryo-DRIE process, but it was notices a micrograss formation. Moreover, since the Cryo-DRIE process also requires cryogenic temperatures, the Bosch-DRIE process was the best candidate.

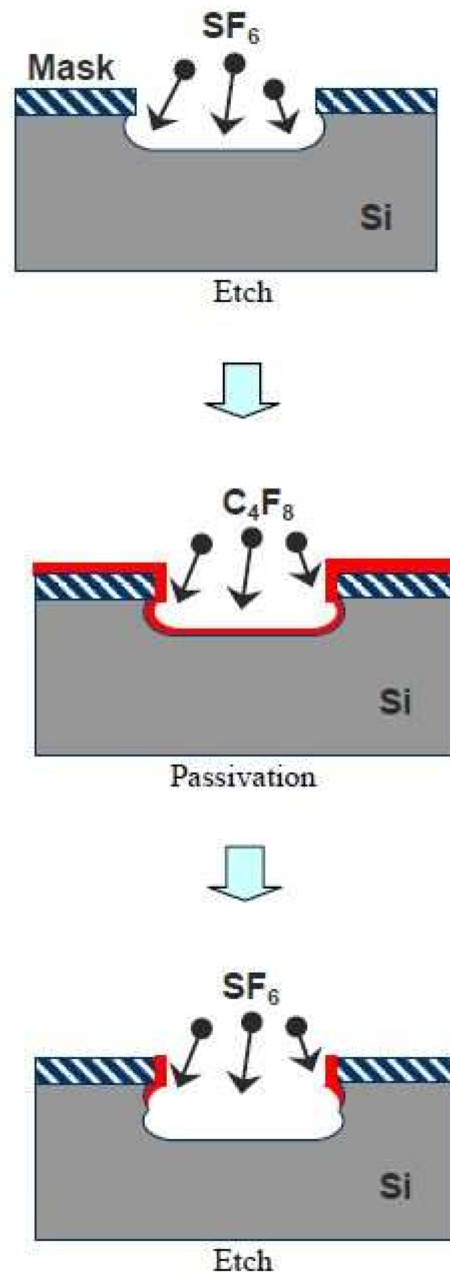


Fig. 3.11 Principle of deep reactive ion-etching (DRIE-Bosch) process [18].

In this type of DRIE system, the employed plasma is a combination of parallel plate and inductively coupled plasma (ICP). The ICP is employed as a high density source of ions which increases the etch rate, whereas a separate RF bias is applied to the silicon wafer

to create directional electric fields near the substrate to achieve more anisotropic etch profiles. An inductively coupled plasma (ICP) is a kind of plasma source where the energy is supplied by electric currents which are produced by electromagnetic induction, that is, by time-varying magnetic fields. The type of ICP geometry is cylindrical as shown in figure 3.12. The plasma is created in a medium vacuum chamber and the ions are accelerated with a nearly vertical direction. Very high plasma densities can be achieved, though etch profiles tend to be more isotropic. Gas pressure is typically maintained in a range between a few millitorr and a few hundred millitorr by adjusting both gas flow rates and the exhaust orifice. The pressure must be not too low to avoid impurity presence and at the same time not too high to allow etching gases to stay in the chamber. In order to achieve high etch rates, it is necessary to use high flows of process gases. This can only be achieved at the desired pressure by using high efficiency pumping. That means using a larger capacity turbomolecular pump, and backing this with an appropriate high capacity rotary pump.

The system is equipped with high efficiency helium backside wafer cooling to remove heat from the wafer generated by the use of higher ICP powers and higher etch rates.

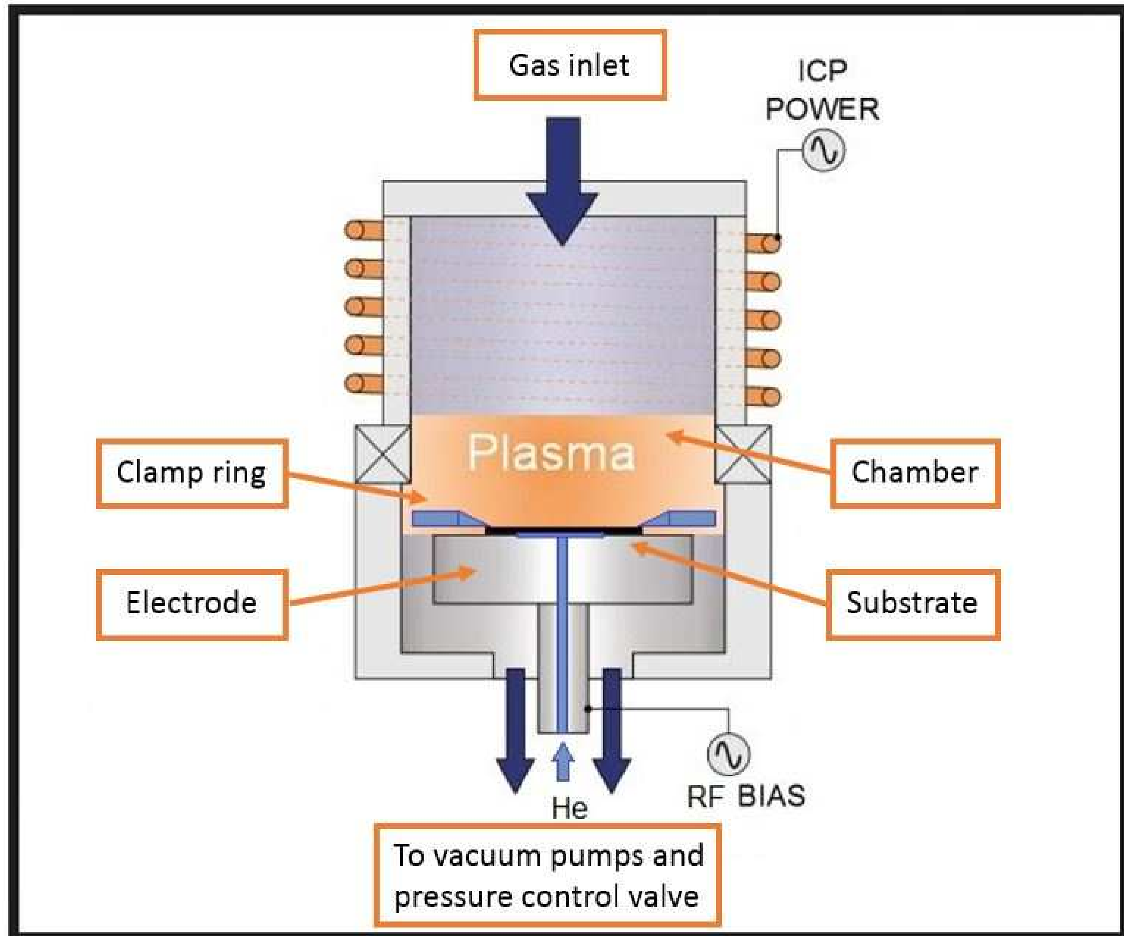


Fig. 3.12 The basic components of a ICP DRIE [19].

Silicon dioxide and silicon etching was performed by using a ICP-DRIE Oxford Plasmalab 100 system available at TechFab, a Trustech Innovation Technology Laboratory, Chivasso (TO) (Fig. 3.13). This equipment is composed by a double chamber reactor for wafer up to 6-inch (pre-loading chamber). There is the possibility of both Bosch attack and Cryogenic etching. The gases available are O_2, Ar, SF_6, CHF_3, C_4F_8.

Fig. 3.13 ICP-DRIE Oxford Plasmalab 100 system available at TechFab, Chivasso (TO) used for both silicon dioxide and silicon plasma etching [20].

Focusing the attention to the wafer processed during photolithography step in previous section, the residual photoresist acts as a hard mask during DRIE etching. This means that the SiO_2 and Si under the photoresist layer are protected from plasma etch.

The first etching involves a plasma consisting of Carbon Tetrafluoride (CF_4) and Oxygen mixture in order to remove the SiO_2 layer portion not protected by the photoresist [21].

The final detailed recipe is following:

- ICP: 1000W
- RF: 32W
- Pressure: 10mtorr
- Chamber temperature: 20°C
- He backside cooling system: 10sccm
- Gas mixture: 25 sccm C_4F_8 and 25 sccm O_2
- Time duration: 7 min
- Etch rate about 60nm/min
- 400nm SiO_2 to remove

After the silicon dioxide removal, the silicon etching is necessary. The previously illustrated Bosch process was used for the excavation of deep trenches with highly vertical sidewalls.
Below the final detailed recipe:

- ICP: 1500W
- RF: 50W
- Pressure: 15mtorr
- Chamber temperature: 18°C
- He backside cooling system: 15sccm
- Etching gas: 100 sccm SF_6
- Protective layer deposition gas: 50 sccm C_4F_8
- Time duration for each step: 7s etch and 4s protective layer deposition
- Total time duration about 1 hour
- Etch rate about 1.7µm/min
- 100µm Si to remove (about 330 SF_6+C_4F_8 steps)

Based on the etch rate, it is possible to establish the number of SF_6+C_4F_8 steps in order to obtain the trenches' desired deepness.
During the process, the plasma etches also the hard mask, but the photoresist has an etch rate 10-15 times smaller than the silicon one. The photoresist left after DRIE is important for the next processes, so the maximum possible deepness for a 10µm thick photoresist is at least 100-150µm.
Figure 3.14 summarizes the DRIE process of the starting wafer substrate previously photolithographed.

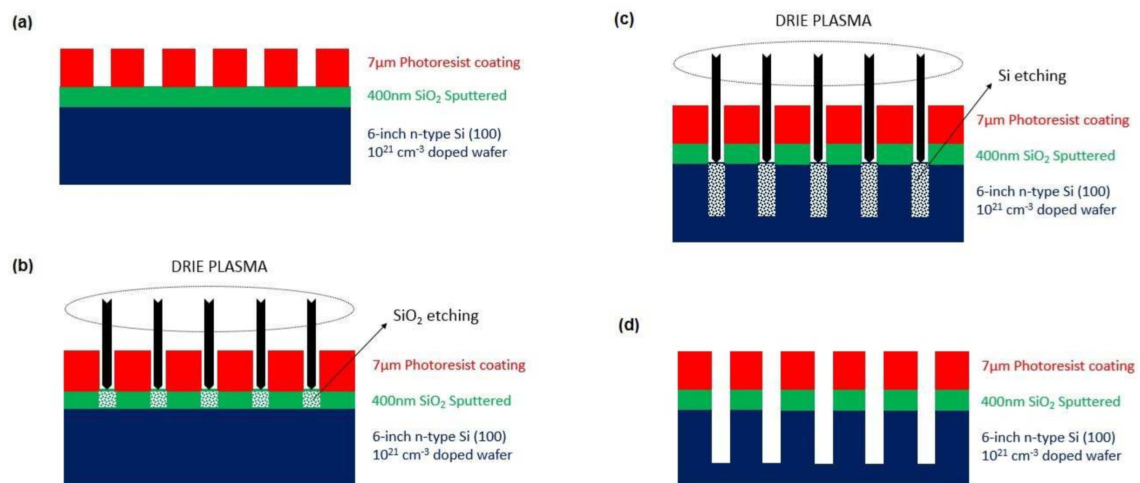


Fig. 3.14 Sketch of the DRIE process step; (a) wafer with patterned resist; (b) SiO_2 plasma etch; (c) Si plasma etch; (d) final plasma etched wafer.

After the whole DRIE process, the wafers have been characterized at optical microscope, in order to evaluate if the final geometry is faithful to the starting patterned geometry and at profilometer to verify if the real final trenches' depth corresponds to the expected one. Figure 3.15a shows a typical optical microscope image after the etching and figure 3.15b the correspondently typical profile.

The microscope image shows the final etched geometry according to the photolithography mask seen in Chapter 3 Section 2. The holes' deepness is about 110 µm.

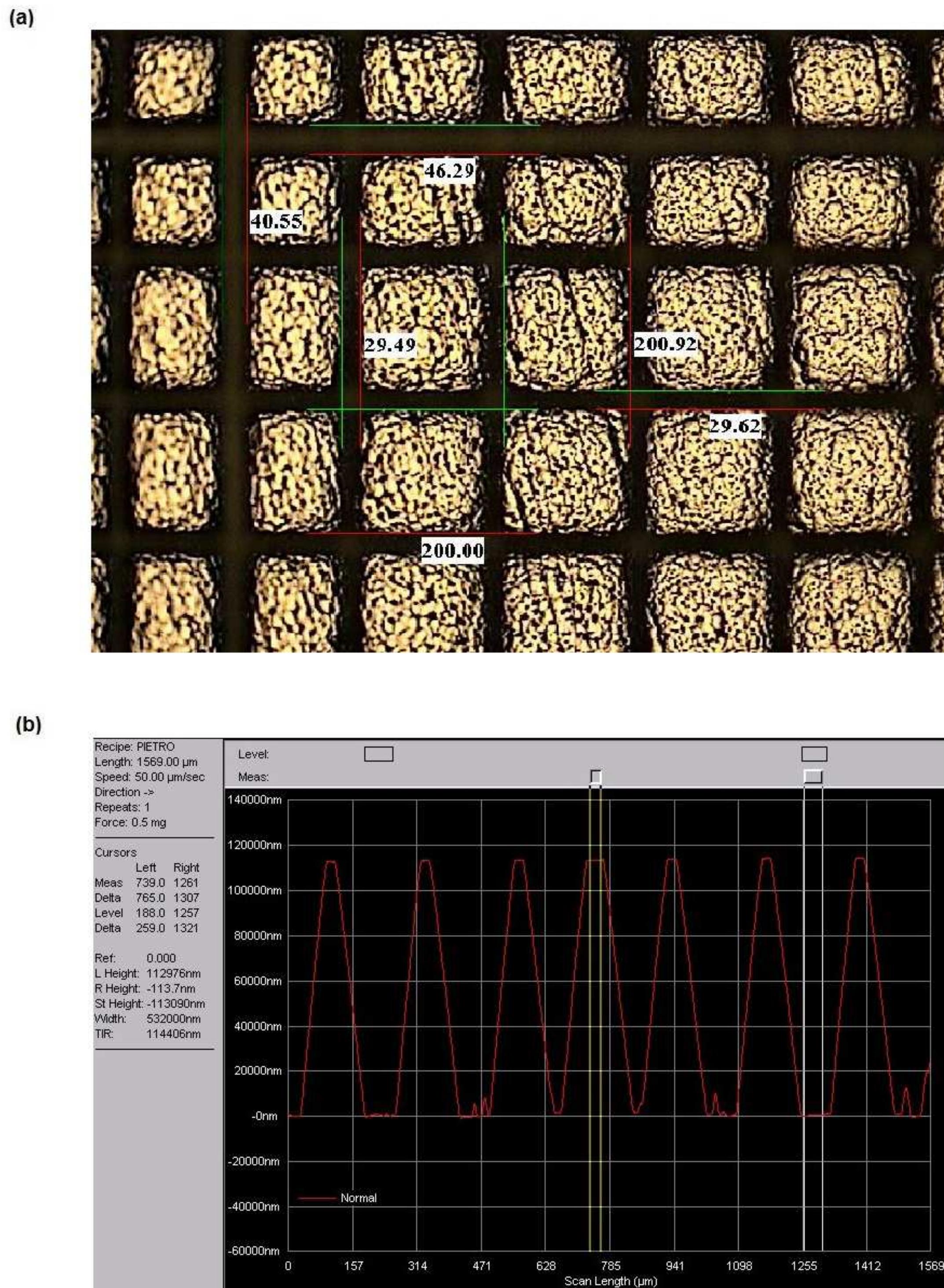


Fig. 3.15 DRIE results; (a) optical microscope image with quotes in microns; (b) profilometer image.

During DRIE process, the protective tape on the front side of the wafer deforms itself causing wafer warpage. This is probably due to thermal deformation: the etched side is heat by plasma reaction on the surface and the non-etched side is exposed to helium and nitrogen cooling.

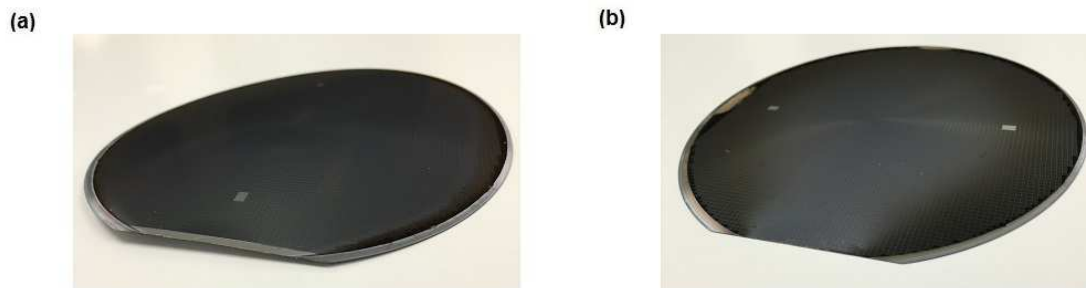


Fig. 3.16 Photo of the final wafer backside view; (a) wafer with protective tape; (b) wafer without protective tape.

3.4 Barrier Seed Layer Deposition

3.4.1 Introduction

Nowadays, the use of copper as the on-chip interconnect metal in semiconductor technology is widely diffused [22,23,24]. Every time copper is employed in integrated circuits, a barrier seed layer is required in order to both prevent the device degradation and promote metal deposition.

Copper has the highest diffusivity and solubility in silicon; it can be easily introduced into the bulk of silicon wafer during any heat treatment and diffuses very fast for significant distances even at room temperature [25]. Moreover, the diffusion barrier of 0.18eV is far lower than that of any other impurity in silicon [26].

The nature of these copper characteristics is primarily due to its electronic configuration. Copper belongs to the group of 3d transition metals, which are the elements with the numbers from 21 to 30 in the periodic table. The electronic structure of 3d transition metals in vacuum is $1s^1 2s^2 2p^6 3s^2 3p^6 3d^x 4s^2$, where x varies from 1 for ^{21}Sc to 10 for ^{30}Zn. ^{29}Cu is the only 3d element whose electronic structure violates this rule. Instead of the $3p^6 3d^9 4s^2$ configuration with an almost full 3d shell, one of the 4s electrons is moved to the 3d shell to complete it, leaving Cu in an irregular (compared to the other 3d metals) electron configuration: $3p^6 3d^{10} 4s^1$. Ionization of copper from Cu^0 to Cu_i^+ changes its electronic configuration in vacuum to the stable closed-shell configuration $3d^{10}$ [26].

Since a copper atom placed in a Si lattice interacts with the surrounding host atoms, its electron configuration may change compared to its state in vacuum. The simplest model is that the electron configuration of Cu_i in silicon is the same in a vacuum, thus $3d^{10}4s^1$ for the neutral charge state Cu_i^0, and $3d^{10}$ for the positively charged state Cu_i^+. Since interstitial Cu is a shallow single donor in silicon, it is always ionized Cu_i^+. The closed-shell $3d^{10}$ electron configuration of Cu_i^+ is the reason of the small ionic radius of Cu_i^+ in Si (it should be about 74 pm) and the weakness covalent interactions of Cu_i^+ with the silicon crystal lattice. That is why the diffusion of copper in silicon mainly proceeds via interstitial lattice sites [26].
Given that this metal diffuse very fast even at room temperature, they are not stable in the interstitial state and precipitate or form complexes or agglomerates during or shortly after the quench. All copper dissolved in the bulk of a silicon wafer during heat treatment will either precipitate, form stable complexes or agglomerates, or diffuse out after the wafer is removed from the furnace. Generally, the process of Cu precipitation is determined by the cooling rate, amount of copper present and already existing defects [26].
Another unusual feature of Cu in Si, which distinguishes it from the other 3d metals, is that it forms a Cu-rich silicide, Cu_3Si, with a much larger molecular cell volume than that of Si. It also interact with the other impurity present in silicon, one example is the CuB pairs formation [26].
Copper contamination is a serious issue in semiconductor technologies because it cause a deep level impurity that degrades the device performances. It has a detrimental effect on minority carrier lifetime and diffusion length; In fact, copper has been observed to reduce the minority carrier lifetime of electronic devices; one example is copper-related light-induced degradation (Cu-LID) in solar cell technologies [27]. Copper also reduces the breakdown strength of electronic devices causing, i.e. the degradation of the gate oxide integrity (GOI) in MOS capacitors [28, 29].
In order to avoid device degradation due to copper diffusion it is important to prevent any interaction between silicon and copper, thus a barrier layer is necessary. Currently, the most diffused barriers between silicon and copper are Ti, TiN, Ta or TaN (Nitrogen addition enhances the barrier performances) [24] even if several barrier layers have been tested in the past, i.e. Ta-W-N [30], Mo/Mo-N [31], and Cu/Co/Au [32].
A copper seed layer is always applied over the barrier layer in order to obtain an efficient charge transfer during the subsequent Cu electroplating.
Uniformity of seed layer is very important, since a poor seed layer can result in voids. It is also required a good adhesion to both Cu and Si and an adequate step coverage is required.

The barrier seed layer deposition method is by PVD i.e. thermal evaporation, sputtering, ion metal plasma process and so forth depending on the employed material.

3.4.2 Objective

In this thesis project, the fourth process flow step is the deposition of the barrier seed layer after the silicon trenches excavation by DRIE Bosch etch process.
The following layers compose the seed barrier layer used:

- Titanium to support the adhesion between silicon bulk and next metals
- Nickel to improve the metal contact between silicon bulk and next metals
- Gold to avoid copper diffusion in silicon
- Copper to promote copper deposition during the subsequent electroplating

3.4.3 Evaporation basic principle

The Ti/Ni/Au/Cu barrier seed layer film were deposited by thermal evaporation.
Thermal evaporation is a physical vapor deposition (PVD) technique that consists in heating until evaporation of the material to be deposited. The material vapor finally condenses in form of thin film on the cold substrate surface and on the vacuum chamber walls. Figure 3.17 shows an outline of the basic principle.

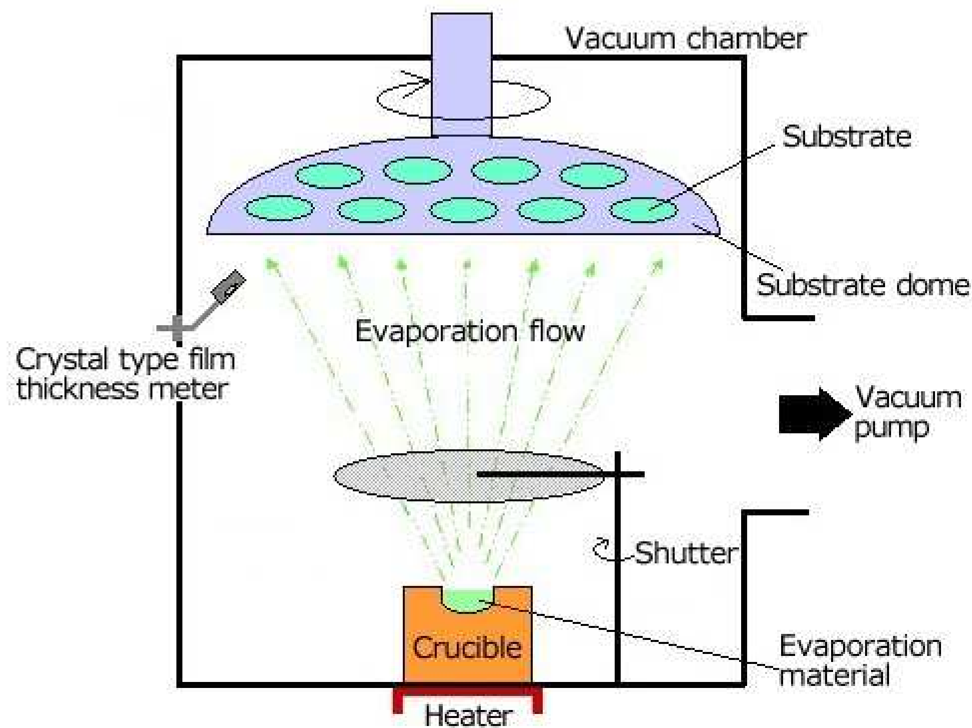


Fig. 3.17 The basic principles of a thermal evaporation system [33].

In thermal evaporation the materials to be evaporated is put on conductive (graphite or tungsten) crucibles, which are intensely heated by focusing an energetic electron beam. The heat melts the source material until its evaporation. This is done in a high vacuum with a long mean free path (10^{-5} to 10^{-6} Torr), both to allow the vapor to reach the substrate without reacting with or scattering against other gas-phase atoms in the chamber, and reduce the incorporation of impurities from the residual gas in the vacuum chamber. The evaporated particles travel directly to the sample (wafer substrate), where they condense back to a solid state.

Evaporated particles travel in straight lines from the evaporation source towards the substrate. This originates 'shadowing' phenomena with 3D objects, especially in those regions not directly accessible from the evaporation source (crucible). In order to overcome this problem, rotating substrate domes are generally employed as substrate support.

It is important to control the growth rate of the film and this is done thanks to an instrument called quartz microbalance, consisting of a piezoelectric quartz crystal placed in vibration at its background frequency and exposed to the flow of condensing material. The material deposited progressively adds to the weight of the quartz, lowering its background frequency. It is possible to see the instantaneous speed of

growth of the film and determine its thickness, measuring in real time the oscillation frequency of the quartz.
The deposition of multiple layers is easily possible because of the shutter; when the first layer reaches the desired thickness, the shutter interrupts the evaporation flow. Afterwards, the crucible rotates to completely expose the next material, which starts to melt and evaporate; then the shutter rotate again to permits the new evaporation flow to reach the substrate.

3.4.4 Equipment details and results

The barrier seed layer Ti/Ni/Au/Cu was deposited on the previously etched wafer by E-beam evaporator ULVAC EBX-14D system available at Material and Microsystems Laboratory (Chilab) of the Politecnico di Torino, in Chivasso (TO) (Fig.3.18).

Fig. 3.18 E-beam evaporator ULVAC EBX-14D system available at Material and Microsystems Laboratory (Chilab) of the Politecnico di Torino, in Chivasso (TO) [34].

The final film thicknesses are listed below:

- 200nm Ti thickness (3Å/s growth rate)
- 200nm Ni thickness (5Å/s growth rate)
- 50nm Au thickness (2Å/s growth rate)
- 200nm Cu thickness (10Å/s growth rate)

The total deposition takes about 2 hours because after the deposition of one layer, it is necessary to wait some time to cool the source before rotating the crucible support.
Figure 3.19 shows the six-inch wafer drawing of the section view after barrier seed layer deposition. To note that the drawing is not in scale.

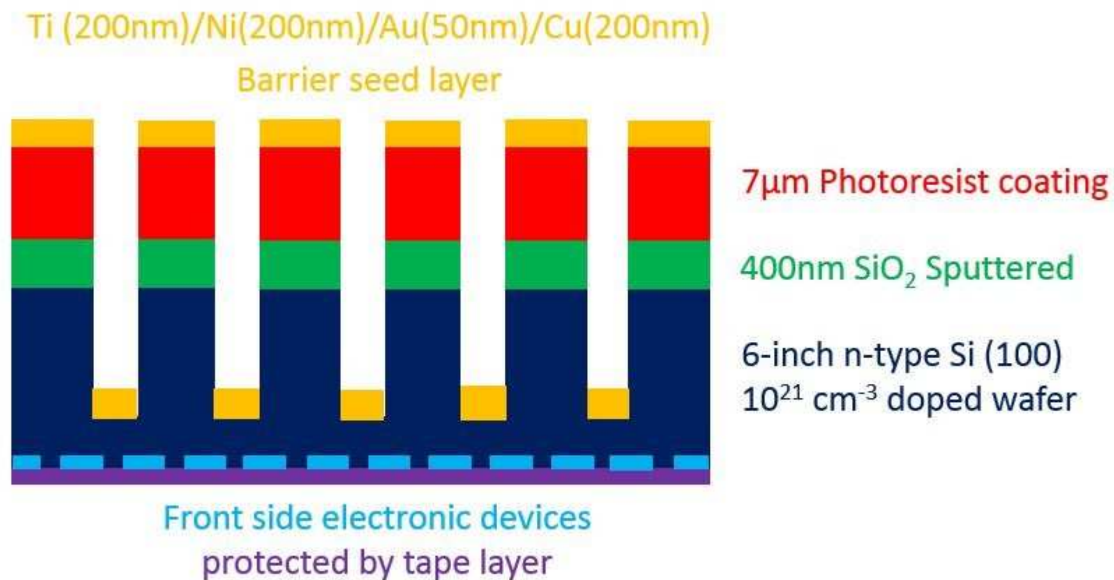


Fig. 3.19 Sketch of the wafer section view after barrier seed layer deposition not in scale.

3.5 Photoresist Lift-off

3.5.1 Introduction

Lift-off process is a method used in micron and submicron technology to create structures of a target material on the surface of a substrate using a sacrificial material. It is also an additive technique as opposed to more traditional subtracting technique, like etching, when films are difficult to dry etch.
Depending on the type of lift-off process, patterns can be defined with extremely high fidelity and for very fine geometries. Lift-off, for example, is the process of choice for patterning e-beam written metal lines, because film remains only where the photoresist has been cleared. The defect modes are opposite what one might expect for etching films since the defects may be in the underlying photoresist layer (for example, particles lead to opens, scratches lead to shorts in metal lift-off).

Any deposited film can be lifted-off, provided:

- during film deposition, the substrate does not reach temperatures high enough to burn the photoresist;
- the film quality is not absolutely critical. Photoresist will outgas very slightly in vacuum systems, which may adversely affect the quality of the deposited film;
- adhesion of the deposited film on the substrate is very good;
- the film can be easily wetted by the solvent;
- the film is thin enough and/or grainy enough to allow solvent to seep underneath;
- the film is not elastic and is thin and/or brittle enough to tear along adhesion lines.

3.5.2 Objective

The fifth process step of the thesis work is the lift-off of the photoresist previously patterned that was also used as hard mask during DRIE etching step (see Sections 2 and 3). The photoresist lift-off permits to contemporary remove the undesired portion of the barrier seed layer in order to promote a selective growth during the next electroplating process step.

3.5.3 Lift-off basic principle

Lift-off is a simple, easy method for patterning deposited films and the ones which are difficult to dry etch. A pattern is defined on a substrate using photoresist and standard photolithography. A film, usually metallic, is blanket-deposited all over the substrate, covering the photoresist and areas in which the photoresist has been cleared. During the actual lifting-off, the photoresist under the film is removed with solvent, taking the film with it, and leaving only the film which was deposited directly on the substrate. The procedure is represented in figure 3.20.

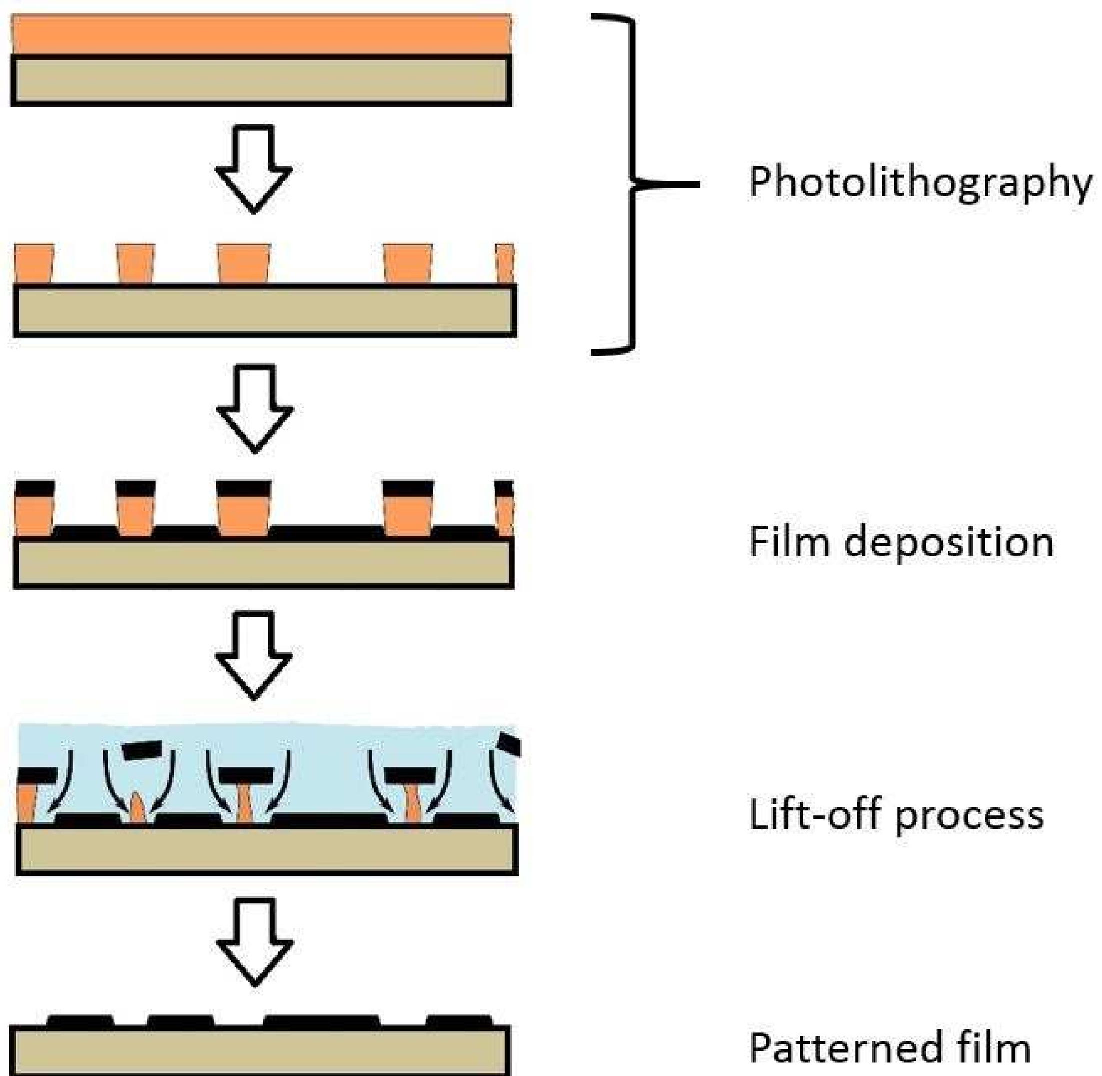


Fig. 3.20 Lift-off technique process [35].

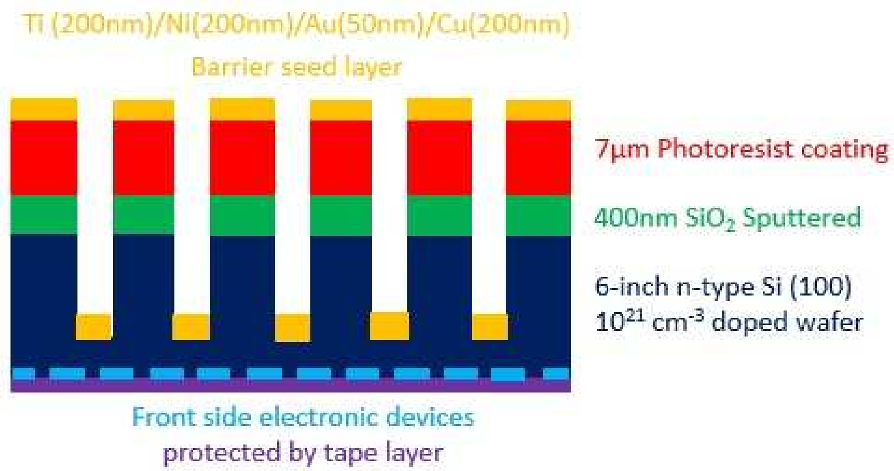
3.5.4 Equipment details and results

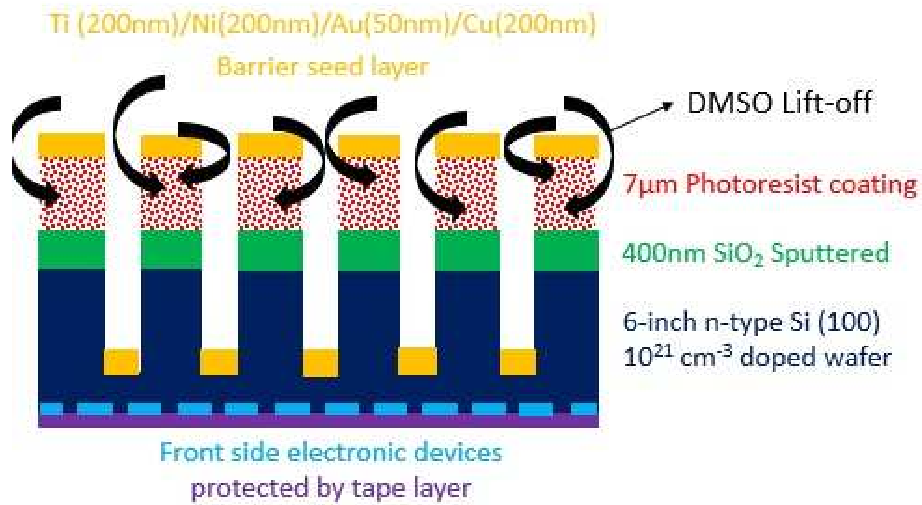
The residual photoresist was removed by wafer immersion in Dimethyl sulfoxide (DMSO). The wafer substrate and the DMSO were put in a glass Petri dish immersed in turn in an ultrasonic bath at 80°C for about 10 minutes. The ultrasonic bath equipment used was a Labsonic LBS2 -15 system available at Material and Microsystems Laboratory (Chilab) of the Politecnico di Torino, in Chivasso (TO) (Fig.3.21). It is provided with a digital timer, power regulation, possibility of choosing two KHz

frequencies, heating from 20° C to 80° C and acoustic alarm which starts when the temperature exceeds the set values [36].

Fig. 3.21 Labsonic LBS2 -15 system available at Material and Microsystems Laboratory (Chilab) of the Politecnico di Torino, in Chivasso (TO) [36].

Figure 3.22 shows the lift-off process drawing of the six-inch wafer section view. After the photoresist strip, the seed layer lies at the bottom of the silicon trenches and silicon oxide layer covers the top walls. The wafer substrate is now ready to the copper electroplating deposition step.


Ti (200nm)/Ni(200nm)/Au(50nm)/Cu(200nm)
Barrier seed layer
7µm Photoresist coating
400nm SiO2 Sputtered
6-inch n-type Si (100)
10^21 cm^-3 doped wafer
Front side electronic devices
protected by tape layer


Ti (200nm)/Ni(200nm)/Au(50nm)/Cu(200nm)
Barrier seed layer
DMSO Lift-off
7µm Photoresist coating
400nm SiO2 Sputtered
6-inch n-type Si (100)
10^21 cm^-3 doped wafer
Front side electronic devices
protected by tape layer

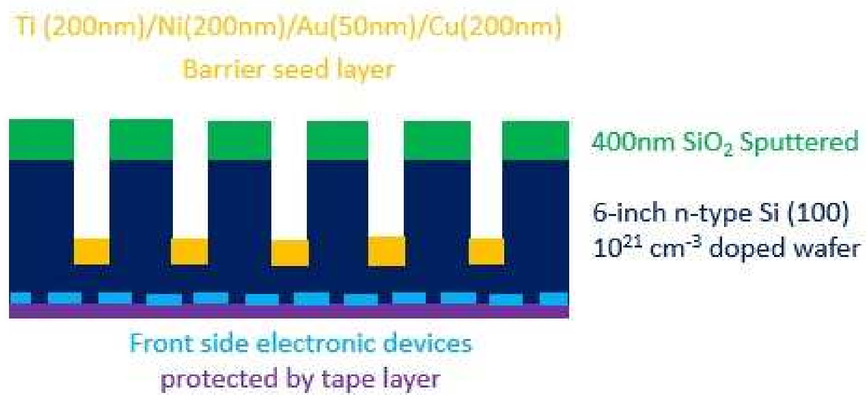

Ti (200nm)/Ni(200nm)/Au(50nm)/Cu(200nm)
Barrier seed layer
400nm SiO2 Sputtered
6-inch n-type Si (100)
10^21 cm^-3 doped wafer
Front side electronic devices
protected by tape layer

Fig. 3.22 Lift-off process step summary.

3.6 Copper Electroplating

3.6.1 Introduction

For several semiconductor technology generations, aluminum was used as the on-chip interconnect metal and silicon dioxide as the inter- and intra-level insulator. With the aggressive scaling of advanced integrated circuits (ICs) to deep submicron levels, the signal delay caused by the interconnect (that is, the resistance–capacitance [RC] delay) became increasingly significant compared to the delay caused by the gate. Either conductors with a lower electrical resistance or insulators with a lower dielectric constant, or both, were needed to reduce the interconnect RC delay. For metallic conductors with electrical resistivity lower than aluminum, the candidates were limited to silver, copper, and gold. Considering the integration feasibility and ‘‘friendliness’’ to silicon devices, copper became the natural candidate to replace aluminum [23].
The transition to copper as a conductor is one of the most significant changes in semiconductor manufacturing history. Manufacturers have long recognized the benefits of using copper interconnects, but switching to copper only became a priority in the late 1980s as feature sizes decreased. IBM made the first working microprocessor using copper in 1997. Motorola also published a paper on Cu interconnections [37].
Replacement of aluminum by copper was an enormous obstacle for semiconductor process engineers, since aluminum is deposited over the entire wafer surface and then patterned by reactive ion etching (RIE), and all efforts to apply RIE to copper failed. Copper cannot be patterned, and a new process had to be developed that could successfully fill a patterned dielectric. Various forms of PVD, including sputtering, deposition etch, electron cyclotron resonance, as well as CVD and electroless plating were examined initially [22].
Nowadays, copper is the dominant on-chip interconnect for advanced integrated circuits and the damascene process has emerged as the industry standard.

3.6.2 Objective

The purpose of this sixth step is the copper filling by the electrochemical deposition in order to fill the silicon trenches previously etched by DRIE Bosch process (see Section 3).

3.6.3 Electroplating basic principle

Electroplating is the application of a metal coating to a conductive surface by an electrochemical process.
The process of electrochemistry is the conversion between electrical and chemical energy, and these conversions take place in electrochemical cells.
In an electrolytic cell, electrical energy is converted to chemical energy, but this reaction is not spontaneous; it is promoted by a power supply.
The wafer to be plated is the electrical circuit cathode. The anode is made of copper bar to be deposited on the cathode. Both components are immersed in an electrolyte solution composed by copper sulfate $CuSO_4$ that permits the flow of electricity. Figure 3.23a shows a diagram of the electroplating tool and figure 3.23b schematically represent the electrochemical cell zoom.

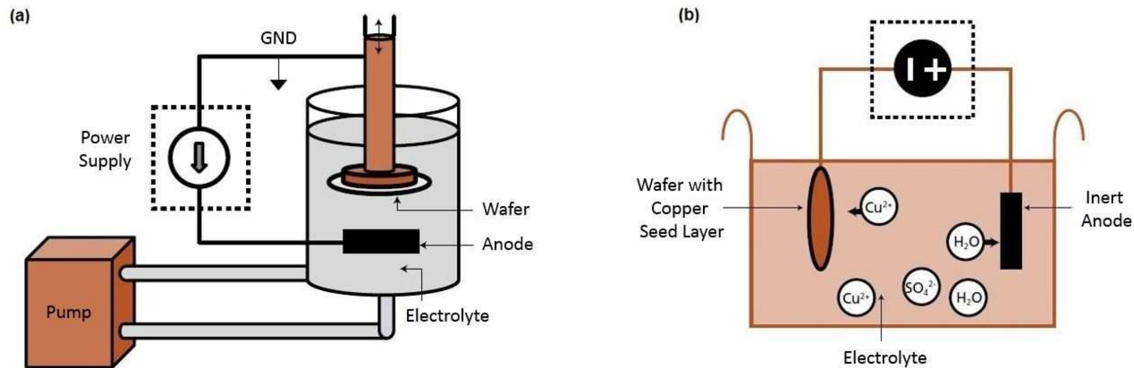


Fig. 3.23 (a) Diagram of the electroplating tool; (b) Copper electrochemical cell zoom [22].

There are two types of reactions in an electrochemical cell: oxidation and reduction (redox). In oxidation, electrons are lost; in a reduction, electrons are gained.
A power supply provides a direct current to the anode oxidizing the copper atoms to Cu^{2+} by losing two electrons. The Cu^{2+} associates with the anion SO_4^{2-} in the solution to form copper sulfate. At the cathode, the dissolved copper ions Cu^{2+} in the electrolyte solution are reduced at the interface between the solution and the cathode to metallic copper by gaining two electrons.
The redox reactions are summarized below.

- At the anode: Cu (solid) $\rightarrow$ $Cu^{2+} + 2e^-$
- At the cathode: Cu^{2+} (aqueous) + $2e^-$ $\rightarrow$ Cu (solid)

Faraday's laws of electrolysis govern the amount of metal deposited.
The rate at which the anode is dissolved is equal to the rate at which the cathode is plated; in this manner, the ions in the electrolyte bath are continuously replenished by the anode.
The result is the effective transfer of copper from the anode source to form a coherent metal coating on the substrate wafer.

3.6.4 Equipment details and results

The copper filling of the silicon trenches previously etched was performed by IKo Classic electroplating System available at Material and Microsystems Laboratory (Chilab) of the Politecnico di Torino, in Chivasso (TO) (Fig.3.24).
This equipment is a practical benchtop tool with the smallest footprint for up to 8-inch wafers on the market. It is designed simply to electroplate high-resolution interconnects and fine metallic feature on wafers and substrates. The tool components are fabricated with PVC and polypropylene and a minimum of metal parts to avoid potential contamination of electroplating solutions. Metal features are stainless and titanium. All parts can be easily disassembled for maintenance [38].

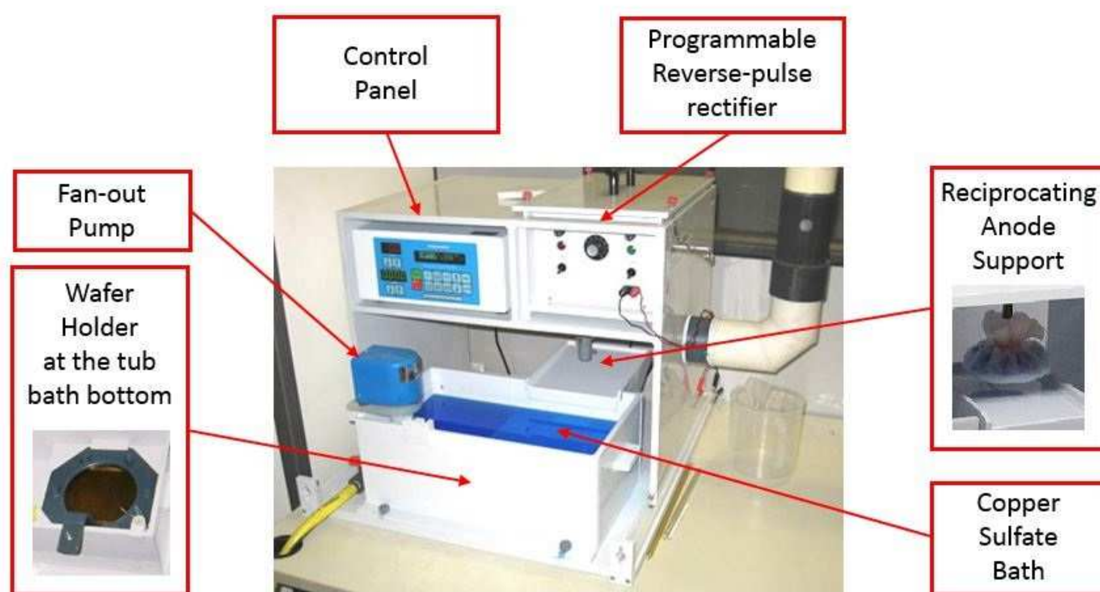


Fig. 3.24 IKo Classic Electroplating System available at Material and Microsystems Laboratory (Chilab) of the Politecnico di Torino, in Chivasso (TO) [39].

The equipment include the following components.

- Wafer holder that is ergonomically designed for easy processing and handling; it can accommodate various wafer sizes (up to 8-inch). A full-circle, elastic electric contact provides uniform current distribution resulting in uniform thickness features across the wafer.
- Reciprocating anode, which provides for an efficient exchange of matter and uniform electric field distribution.
- Programmable Reverse-pulse rectifier that contributes to equipment versatility. Reverse-pulse current during processing efficiently controls plating thickness distribution along the Z-axis.
- Fan-out pump with constant filtration (regardless of fine filter medium) which supply a constant flow of high-quality bulk solution.

Figure 3.25 shows the six-inch wafer backside view after the deposition of 100µm thick copper, a representative zoom microscope image (with quotes in microns) and the correspondent drawing of the section view (to note that the drawing is not in scale).

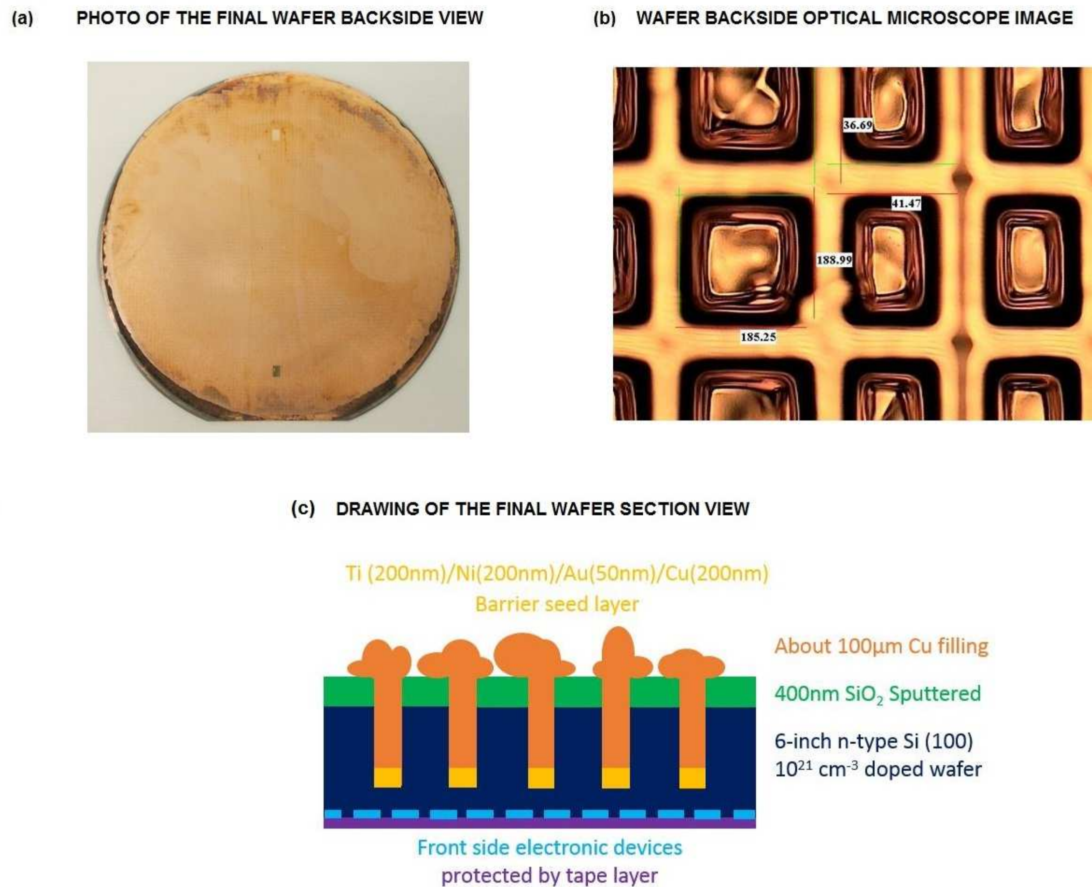


Fig. 3.25 6-inch silicon wafer after Cu deposition; (a) Picture of the final wafer backside view; (b) optical microscope image with quotes in microns; (c) Sketch of the final wafer section view not in scale.

After the electrodeposition step, the silicon trenches are completely filled by copper, indeed, it comes out from the holes covering the silicon dioxide layer on the top walls.
The profilometer results are not reliable because of copper overfilling. Moreover, the overfilling cause a visible increasing of the wafer warpage already noticed after DRIE process due to the protective tape presence on the front size (see Section 3).

3.7 Wafer Planarization

Wafer planarization is widely used in semiconductor industry at the end of the front side completion; it is performed by equipment and methods deeply described in Chapter 1 Section 2.
Mechanical fine grinding and chemical mechanical polishing (CMP) is required in order to remove both copper excess and silicon dioxide layer from the top of the silicon holes and to planarize the wafer surface.

DISCO Corporation performed this process step. DISCO is a based-Japan company engaged in the manufacture and sale of semiconductor manufacturing devices and precision processing tools.
Figure 3.26 shows the six-inch wafer backside view after the planarization, the respective microscope image (with quotes in microns) and the correspondent drawing of the section view (to note that the drawing is not in scale).

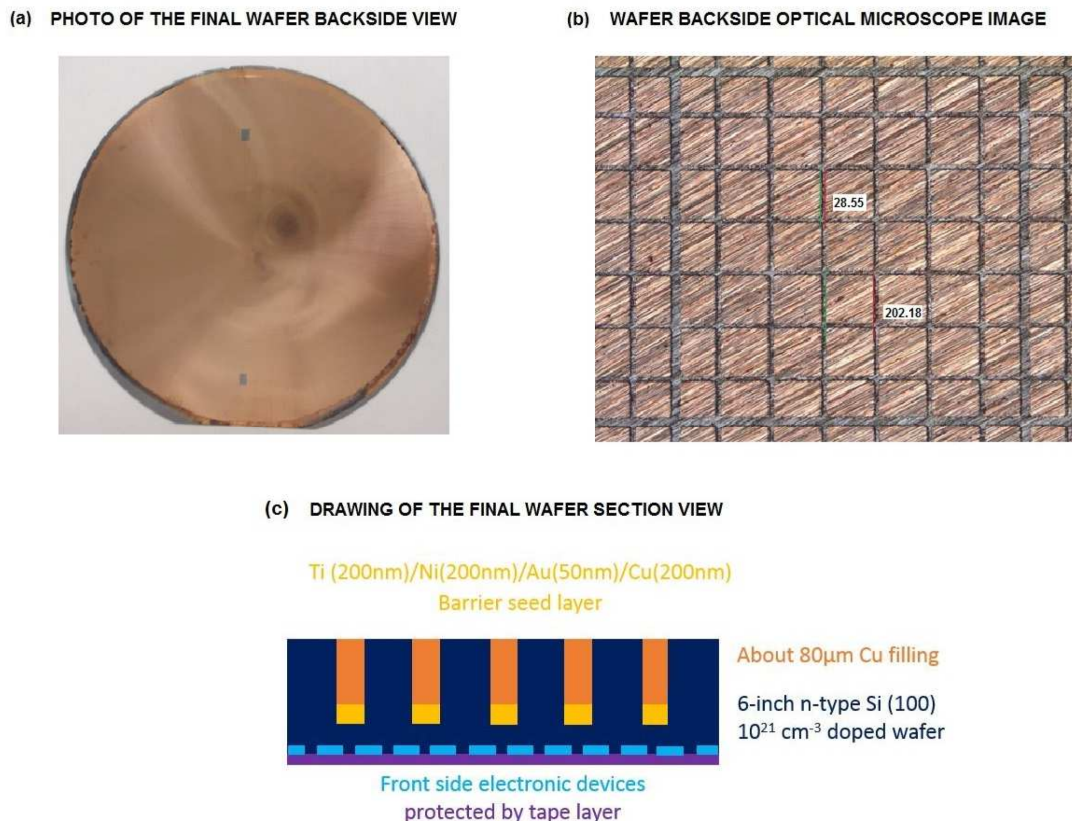


Fig. 3.26 6-inch silicon wafer after Cu deposition; (a) Picture of the final wafer backside view; (b) optical microscope image with quotes in microns; (c) Sketch of the final wafer section view not in scale.

The parallel scratches clearly visible in the optical microscope image (Fig.2.26b) are due to the wheel rotation during the material removal.
After the planarization, the wafer edges are thinner than other area due to wafer warpage after copper deposition.

3.8 Back Metal Deposition

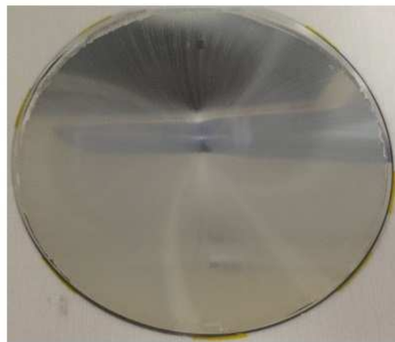
The back metal deposition is the final step in semiconductor manufacturing and it is necessary in order to realize the ohmic contact between the wafer bulk material and the

next packaging. Its deposition was performed by the E-beam evaporator ULVAC EBX-14D system described in details in Chapter 3 Section 4.
The following layers compose the back metallization:

- Titanium to support the adhesion between silicon bulk and next metals (100nm)
- Nickel to improve the metal contact between silicon bulk and next metals (300nm)
- Silver to promote the adhesion with the solder paste during the packaging (600nm)

Figure 3.27 shows the six-inch wafer backside view after the back metallization and the correspondent drawing of the section view (to note that the drawing is not in scale).

(a) PHOTO OF THE FINAL WAFER BACKSIDE VIEW



(b) DRAWING OF THE FINAL WAFER SECTION VIEW

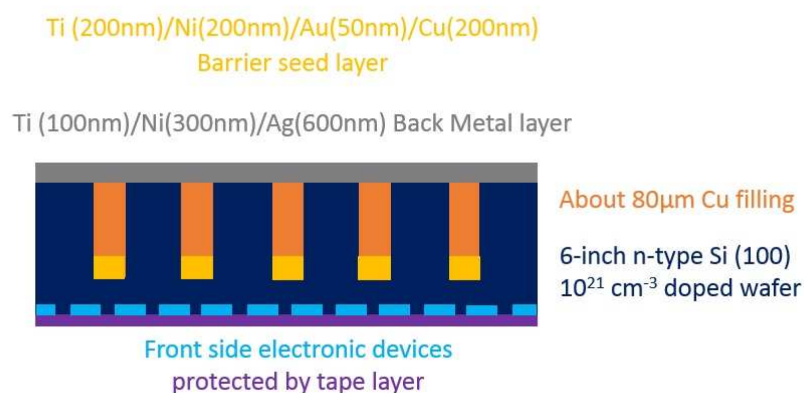


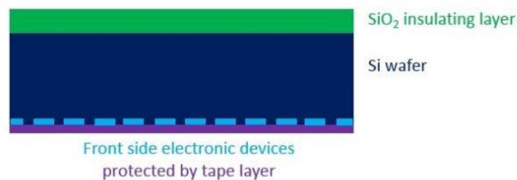
Fig. 3.27 6-inch silicon wafer after back metal deposition; (a) picture of the final wafer backside view; (b) sketch of the final wafer section view not in scale.

After the final back metal deposition, the protective tape layer was easily removed.

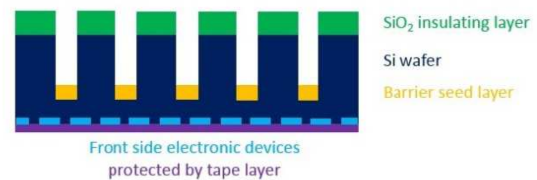
3.9 Process Flow Summary

The whole process flow threated in the previous sections is summarized in figure 3.28 in order to better understand each single process step.

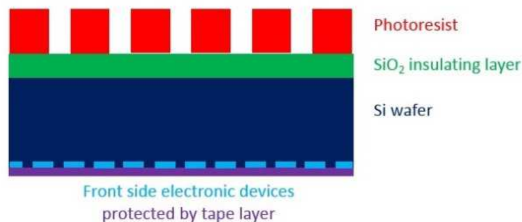
1) SILICON DIOXIDE DEPOSITION



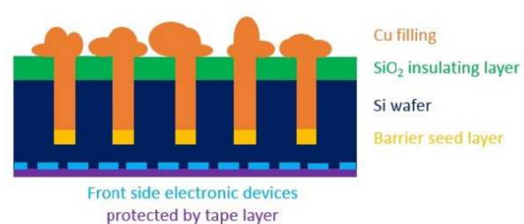
5) PHOTORESIST LIFT-OFF



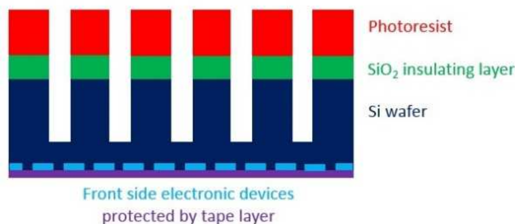
2) PHOTOLOTHOGRAPHY



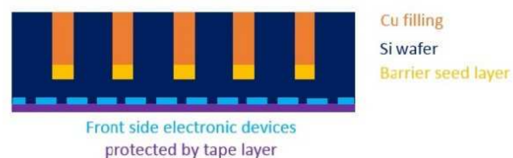
6) COPPER ELECTRODEPOSITION



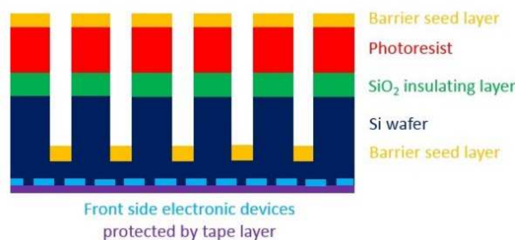
3) DRIE-BOSCH ETCHING



7) WAFER PLANARIZATION



4) BARRIER SEED LAYER DEPOSITION



8) BACK METAL CONTACT DEPOSITION

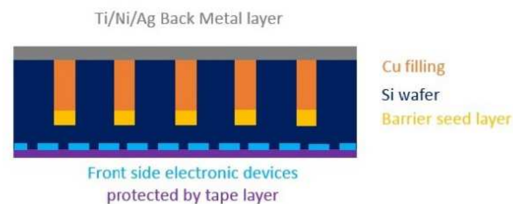


Fig. 3. 8 Process flow summary.

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Chapter 4

SECTION STUDY

This Chapter presents the section characterization by Field Emission Scanning Electron Microscopy (FESEM) of the manufactured wafers. The resin encapsulation is the adopted method to build appropriate samples in section and this technique is widely described in next sections.

4.1 Wafer Dicing

The dicing is the process by which wafer devices are separated from each other in order to assembly the single piece. From now on, the terms "die" refers to each single diode.
Dicing may be performed by sawing the wafer with blades, laser ablation methods, stealth-dicing technique, dicing before thinning and so forth.
The most diffused technique still in production is the dice cutting into individual chips by sawing the silicon wafer and this is the method adopted in this thesis work.
Firstly, the wafer is mounted on a specific blue tape, which has a sticky backing that holds the wafer on a thin sheet metal frame; this frame ring supports the whole structure.
A rotary high-speed blade saw the semiconductor wafer along the designed cutting streets. During the sawing process, a filtering water is dispensed along the blade

trajectory to carry out the mechanical residuals and the electrical charge generated during the process. The blade edge is made by diamond particles. The described process is shown in figure 4.1. Finally, each die is separated by the others.

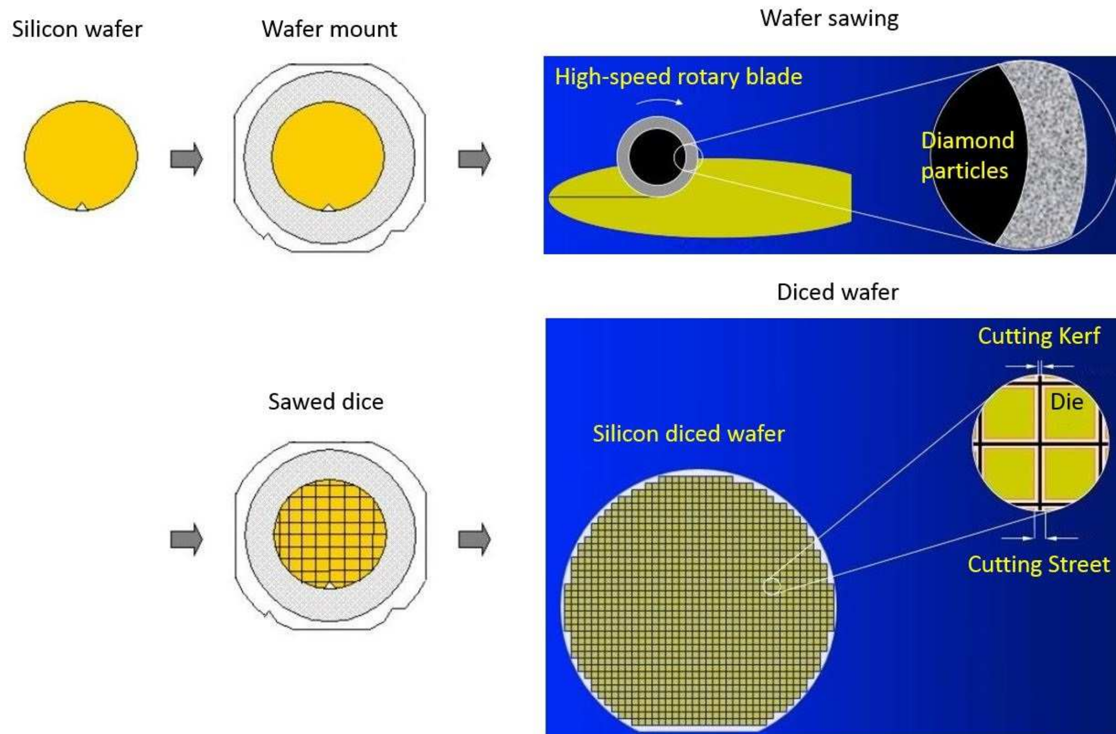

Fig. 4.1 Silicon wafer dice process steps [1, 2].

Figure 4.2 exhibits an optical microscope image of the backside view of the diced wafer; the blue color is due to the specific blue tape. Each bigger square corresponds to one diode while smallest square are the silicon holes filled by copper.

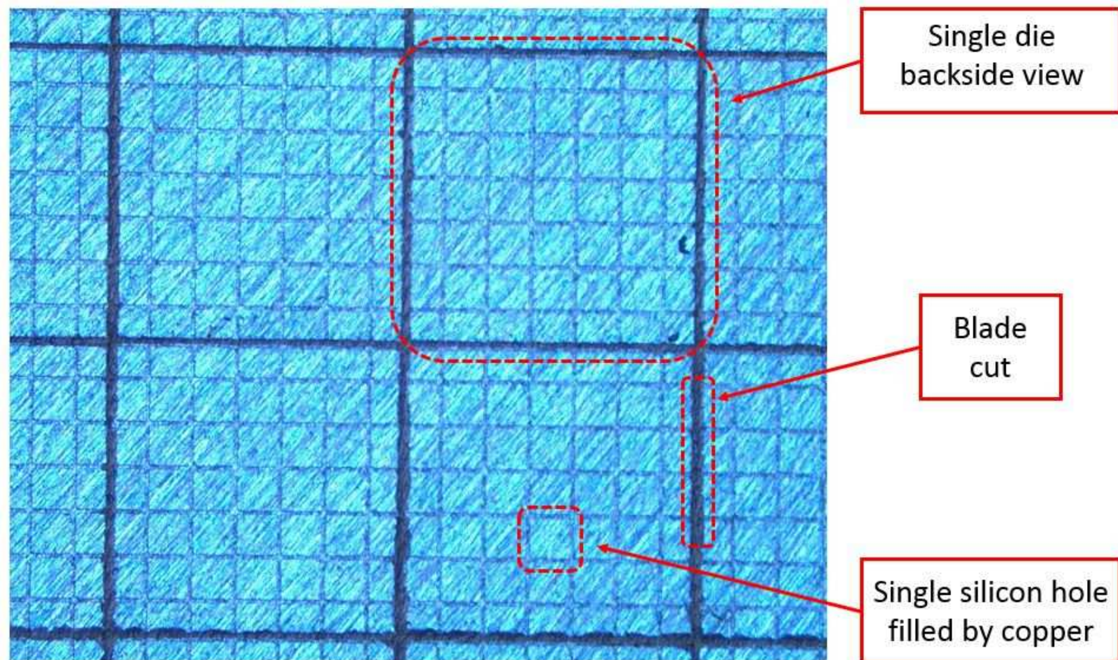

Fig. 4.2 Optical microscope image of the dice backside view after dicing.

4.2 Sample Choice Criterion

After dicing completion, some dice were collected from different wafer areas like shown in figure 4.3, in order to evaluate the process flow efficiency along the whole wafer.
To distinguish the different portions with respect to the wafer flat reference, the examined areas were from the one named as "A" until the one denoted as "I".

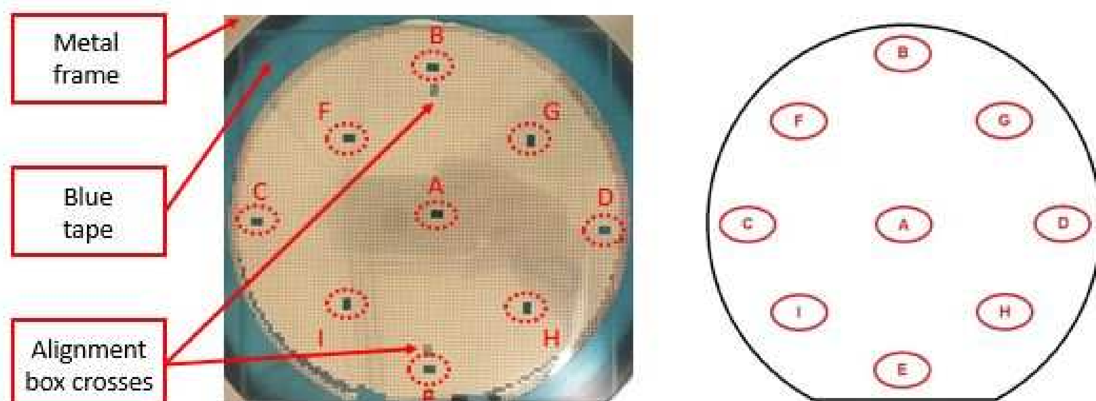

Fig. 4.3 Dice collection from different wafer areas.

4.4 Thickness Measurements

The thickness of each die was measured by means of digital thickness gauge. This tool consists of a metal tip and a digital display (see figure 4.4).

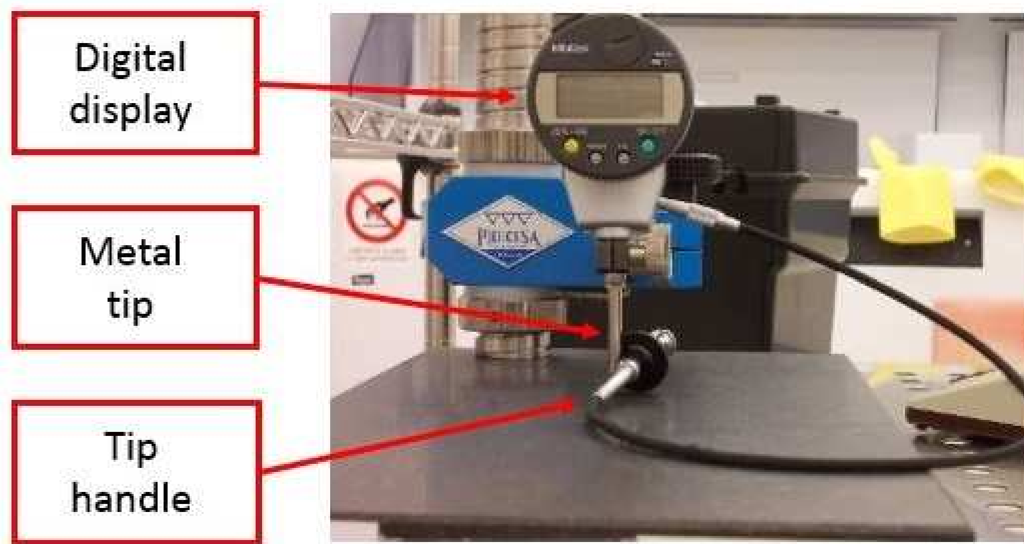

Fig. 4.4 Digital thickness gauge available at Vishay Semiconductor Company.

The die thickness is given by the difference between the final position with the die under the tip and the initial one without the die.

4.5 Resin Encapsulation

The resin encapsulation is necessary in order to avoid copper removal from silicon holes. Figure 4.5 shows the optical microscope image comparison between dice section without and with the resin encapsulation.

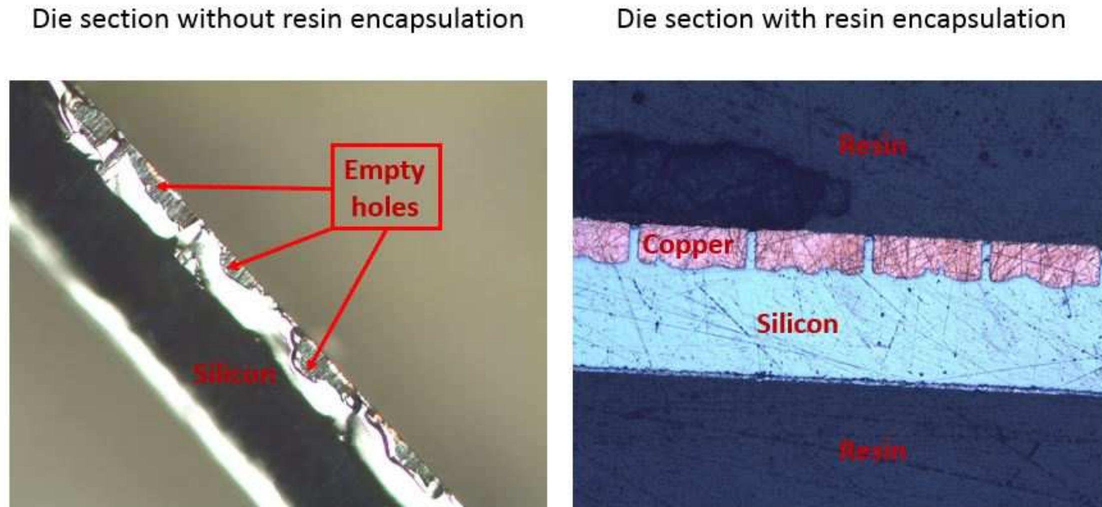

Fig. 4.5 Optical microscope image comparison between die section with and without resin encapsulation.

The resin encapsulation is needed in order to maintain the copper inside the silicon holes during the mechanical section.

The dice were fixed inside a sample holder (see figure 4.6) in vertical position for convenience, thus, the resin and hardener mix was pour into the holder incorporating all the samples. The solution is composed by 7.5 resin parts and 1 hardener part and must stand for at least 12 hours.

The resin and the correspondent hardener employed were the Buehler EpoKwick Epoxy resin 20-8136-128 and the Epoxy hardener 20-8138-032 [3].

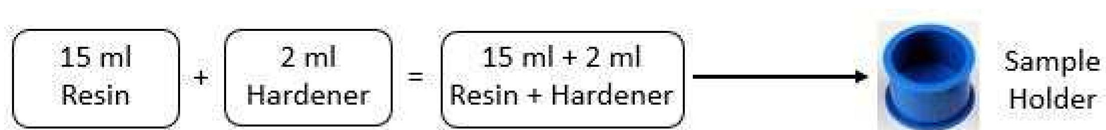

Fig. 4.6 The resin and hardener solution details and sample holder.

4.6 Mechanical Grinding and Polishing

The incorporated samples were grinded by sheets of sandpaper with Silicon Carbide as abrasive material (see figure 4.7). Different grit dimensions were employed in order to remove the material and then smaller grits were used to gradually polish the sectioned surface.

The greater amount of material was removed by the 320 grit, then were used the 600, 800, 1000, 1200, 2500, 4000 grits consecutively making as smoother as possible the sample surfaces. The final polishing step was performed by means of the diamond abrasive polishing paste containing micro particles.

Fig. 4.7 Sheets of Silicon Carbide sandpapers with different grain size.

4.7 FESEM Samples preparation

FESEM requires a sample size lower than one cubic centimeter, hence the resin excess must be removed. The samples were cut by oil-lubricated high-speed blade, shown in figure 4.8a, obtaining suitable resin squares like the one in figure 4.8b.

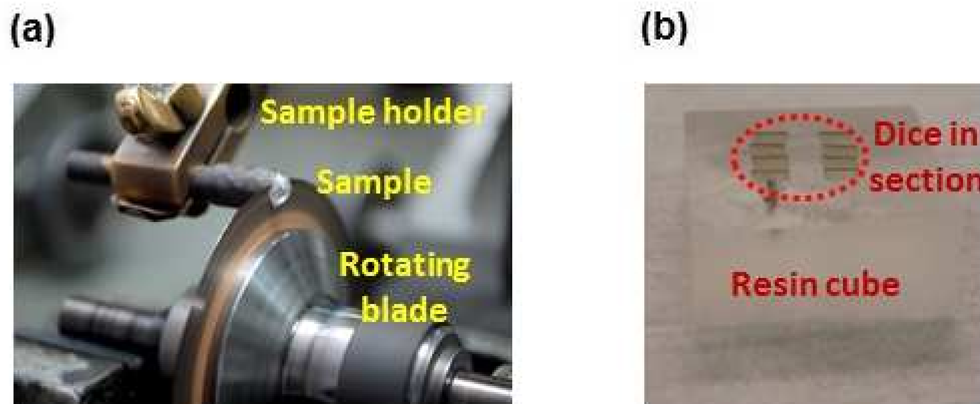

Fig. 4.8 (a) Oil-lubrificated rotating blade; (b) resin sample after cutting.

Since for FESEM imaging specimens must be electrically conductive, some chromium tens of nanometers were sputtered at the front surface samples.

Then samples must be also electrically grounded to prevent the accumulation of electrostatic charge at the surface, which causes scanning faults and other image artifacts.

4.8 Results and discussion

Field emission scanning electron microscopy (FESEM) provides topographical and elemental information of the samples by scanning the surface with a focused beam of electrons.

Two different semiconductor wafers were completely processed and characterized by FESEM analysis. The section images related to the first and the second wafer are collected in figure 4.9 and 4.10 respectively. Each letter at the corner of each image refers to the wafer areas specified in Section 2 figure 4.3.

Table 4.1 contains a summary of all section and thickness measurements of each wafer area.

Fig. 4.9 FESEM images of the die cross sections of the first wafer.

Fig. 4.10 FESEM images of the die cross sections of the second wafer.

W#	Zone	Thickness [μm]	Hole Deepness [μm]	Hole Width [μm]	Wall Width [μm]
First Wafer	A	288	65.01	212.3	19.83
	B	292	101.00	206.8	23.14
	C	289	90.35	209.4	19.47
	D	293	78.60	207.9	22.04
	E	296	88.15	213.0	16.16
	F	289	80.80	213.0	18.00
	G	291	80.44	210.8	19.83
	H	295	81.17	211.2	19.47
	I	291	87.78	213.0	18.36
Second Wafer	A	298	82.27	210.8	19.47
	B	296	87.78	211.6	18.36
	C	301	88.52	211.9	17.63
	D	299	89.99	207.9	19.83
	E	302	103.90	212.3	18.36
	F	300	87.78	208.3	18.73
	G	290	84.11	206.8	22.40
	H	303	69.42	213.4	18.00

Tab. 4.1 Summary of die thicknesses and FESEM measurements for each area.

After the comparison between the values of the first and second wafer, the DRIE process does not depend on the considered wafer zone, i.e. the B area of the first wafer is the deepest, while, for the second wafer, the deeper area is the E.

Table 4.2 presents a statistic summary of all previous measurements by wafer.

		W#2	W#3
Dice Thickness [µm]	Median	300	291
	Mean	299	292
	Std Dev	4	3
FESEM Hole Deepness [µm]	Median	88	81
	Mean	87	84
	Std Dev	10	10
FESEM Hole Width [µm]	Median	211	211
	Mean	210	211
	Std Dev	2	2
FESEM Wall Width [µm]	Median	19	19
	Mean	19	20
	Std Dev	2	2

Tab. 4.2 Statistic summary by wafer.

The values for the first and the second wafer are almost the same, so the process is reproducible.
The high standard deviation value related to the hole deepness means low homogeneity in DRIE excavation process.
Figure 4.11 shows the defects found during section characterization.

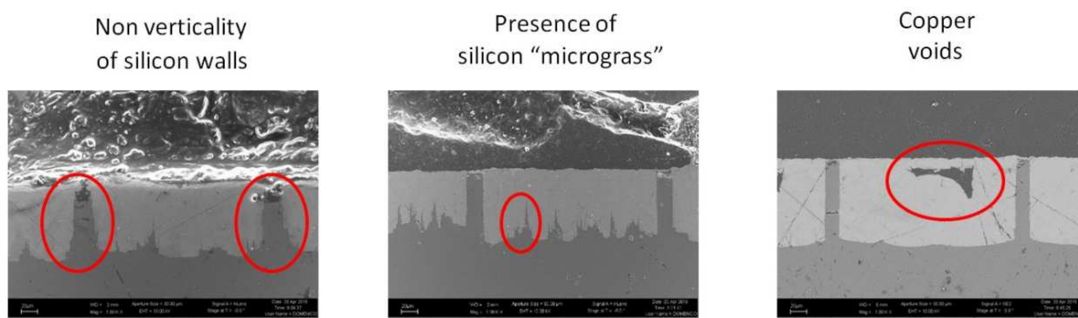

Fig. 4.11 Defects summary.

As regards the non-verticality of silicon walls, it was only found in the area B of the first wafer and in areas D and G of the second.
Concerning the presence of the "micrograss", this defect was found in almost all areas except in areas B and F of the first wafer. This defect is probably related to the starting wafer roughness after the first backgrinding.

Copper void was only seen in the area E of the second wafer. The area was limited and probably due to external reasons not related to the process flow.

It is possible to conclude that the process flow has good repeatability, the minor defects found are not tightly due to the process flow and they could be overcome improving the starting surface roughness and cleanness.

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Chapter 5

DICE ASSEMBLY

This Chapter explains the fundamental steps of the dice assembly process flow to obtain the final pieces.

5.1 Assembly overview

Nowadays, there are several packages in which semiconductor devices are assembled and each different package requires its process flow. Moreover, each semiconductor company employ its own technique. However, even if the methods differ, they have common basics that will be briefly explained below.
Mount wafer on film: the wafers are mounted on a backing tape that adheres to the back of the wafer. The mounting tape provides support for handling wafer saw and die attach process.
Dicing: the wafer saw process cuts the individual die from the wafer leaving the die on the backing tape. The wafer saw equipment consists of automated handling equipment, saw blade and an image recognition system. The image recognition system maps the wafer surface to identify the areas to be cut, known as the saw street. DI water is dispensed on the wafer during the saw process to wash away particles (silicon dust) and

to provide lubrication during the dicing process. Wafers are dried by spinning the wafer at a high RPM before going to the die attach process.
Die attach: the die attach process provides the mechanical support between the silicon die and the substrate, i.e,. leadframe, plastic or ceramic substrate. The die attach is also critical to the thermal and, for some applications, the electrical performance of the device. The die attach equipment is configured to handle the incoming wafer and substrate simultaneously. An image recognition system identifies individual die to be removed from the wafer backing/Mounting tape, while die attach material is dispensed in controled amounts on to the substrate. A non pierce through plunge up needle/s assists to separate an individual die to be picked by the collet on the pick-up head of the die attacher. Finally, the die is aligned in the proper orientation and position on the substrate. The type of material used for die attach is a function of the package type and performance requirements. The epoxy and cyanate ester are two types of polymers used as a die attach between the die and the leadframe. Depending on the leadframe design, adhesion may be directly to copper, silver plating, or palladium plating. Die attach materials are filled with silver particles to increase the thermal dissipation properties. Material is dispensed from syringes in controlled amounts. These materials have defined shelve lifes and, therefore, the recommended guidelines must be followed when handling in a manufacturing environment. After placement of the die, the die attach is cured; typical cure temperatures are in the 125-175°C range.
Wire bond: wire bonds are the most common means of providing an electrical connection from the IC device to the substrate/Leadframe. The wire bond process must achieve high throughputs and production yields to be acceptable on a cost basis. High-speed wire bond equipment consists of a handling system to feed the substrate/leadframe into the work area. Image recognition systems ensure the die is orientated to match the bonding diagram for a particular device. Wires are bonded one wire at a time. Thermosonic bonding is used with gold and copper wire. The wire is fed through a ceramic capillary. A combination of temperature and ultrasonic energy forms the metallic wire bond. The mechanical properties and diameter of the wire are important wire attributes that impact the bonding process and yield. Gold wire is 99.99% pure with 100 ppm dopant level. The dopants impart the desired mechanical properties without severely limiting the electrical conductivity. Copper wire requires an inert gas environment to prevent oxidation.
Molding: mold compound protects the device mechanically and environmentally from the outside environment. Transfer molding is used to encapsulate most plastic packages. Mold compounds are formulated from epoxy resins containing inorganic fillers, catalysts, flame retardants, stress modifiers, adhesion promoters, and other additives. Fused silica, the filler most commonly used, imparts the desired coefficient of thermal

expansion, elastic modulus, and fracture toughness properties. Most resin systems are based on an epoxy cresol novolac (ECN) chemistry though advanced resin systems have been developed to meet demanding requirements associated with moisture sensitivity and high temperature operation. Filler shape impacts the loading level of the filler. Transfer molding is used to encapsulate leadframe based packages and some PBGA packages. This process involvesthe liquidification and transfer of pelletized mold compound in a mold press. The liquidification results in a low viscosity material that readily flows into the mold cavity and completely encapsulates the device. Shortly after the transfer process into the mold cavity, the cure reaction begins and the viscosity of the mold compound increases until the resin system is hardened. A further cure cycle takes place outside the mold in an oven to ensure the mold compound is completely cured. Process parameters are optimized to ensure the complete fill of the mold cavity and the elimination of voids in the mold compound. Also critical to the mold process is the design of the mold tool. Runners and gates are designed so the flow of mold compound into the mold cavity is complete without the formation of voids. Depending on the wire pitch, the mold process is further optimized to prevent wire sweep that can result in electrical shorts inside the package. Process parameters that are controlled are the transfer rate, temperature, and pressure. The final cure cycle (temperature and time) determines the final properties and, thus, the reliability of the molded package.
Dejunk and deflash: the dejunk process removes excess mold compound that may be accumulated on the leadframe from molding. Media deflash bombards the package surface with small glass particles to prepare the leadframe for plating and the mold compound for marking.
Trim and form: trim and form is the process where the individual leads of the leadframe are separated from the leadframe strip. First, the process involves the removal of the dambar that electrically isolates the leads. Second, the leads are placed in tool-ing, cut, and formed mechanically to the specified shaped. The lead forming process is critical to achieve the coplanar leads required for surface mount processes. Tool cleaning during maintenance is crucial to ensure the quality of the process.
Marking: marking is used to place corporate and product identification on a packaged device. Marking allows for product differentiation. Either ink or laser methods are used to mark packages. Laser marking is preferred in many applications because of its higher throughput and better resolution.
Figure 5.1 shows an assembled discrete device sketch in section.
The diodes used for the thesis work were assembled at Vishay assembly sites in China.

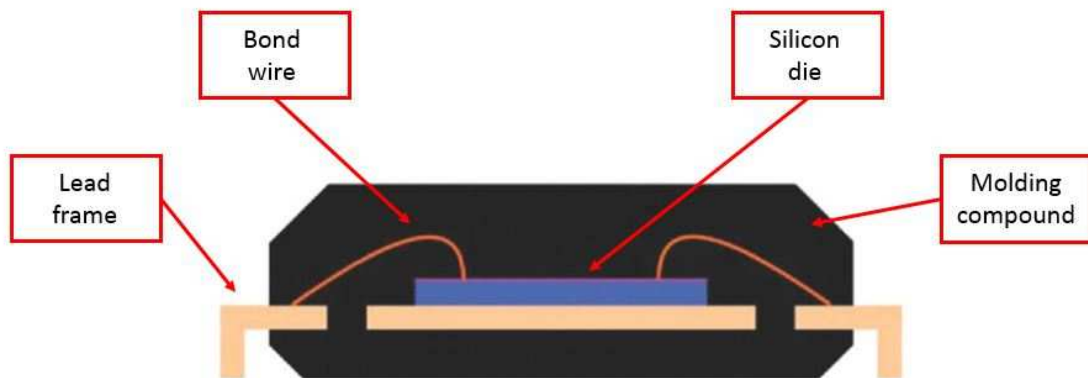

Fig. 5.1 Sketch of an assembled discrete device [1].

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Chapter 6

ELECTRICAL AND THERMAL CHARACTERIZATION

This Chapter shows the electrical and thermal results of the assembled dice in comparison with the standard devices.

6.1 Electrical Characterization

The main electrical parameters that characterize a diode are the forward voltage drop, the leakage current and the breakdown voltage as seen in Chapter 2 Section 2.
Both standard and new devices were evaluated in forward polarization at different forward currents. The obtained median values are plotted in figure 6.1 giving the median I-V diode characteristics.
The forward performances of the new devices are better than the standard ones especially at higher forward current values. This means that the new devices has better thermal dissipation than the standard ones.
The devices were also characterized in reverse polarization and the results are shown in the variability charts in figures 6.2 and 6.3. The leakage current and the breakdown

voltage are aligned with the standard requirements, in fact the breakdown voltage exceeds the 200V and the leakage current does not exceeds 1μA.

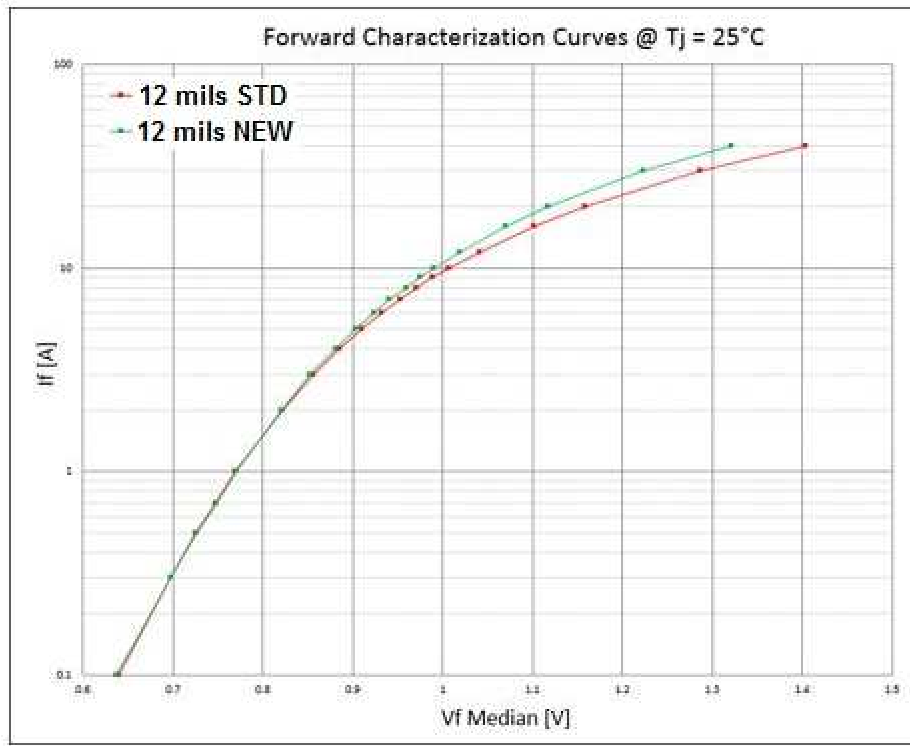

Fig. 6.1 Forward characterization curve comparison between standard and new devices.

Leakage Current @ 200V

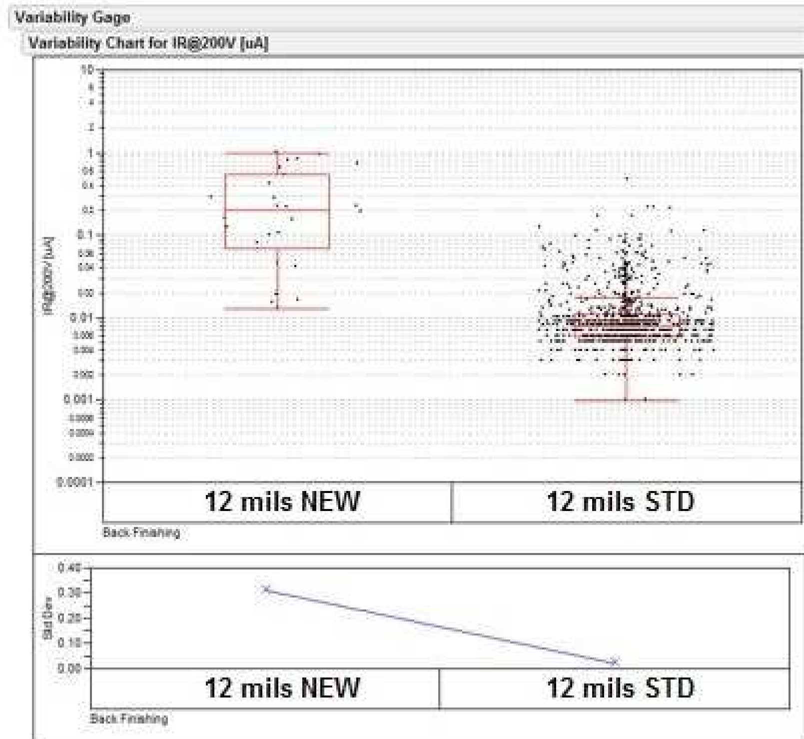

Fig. 6.2 Leakage current variability chart comparison between standard and new devices.

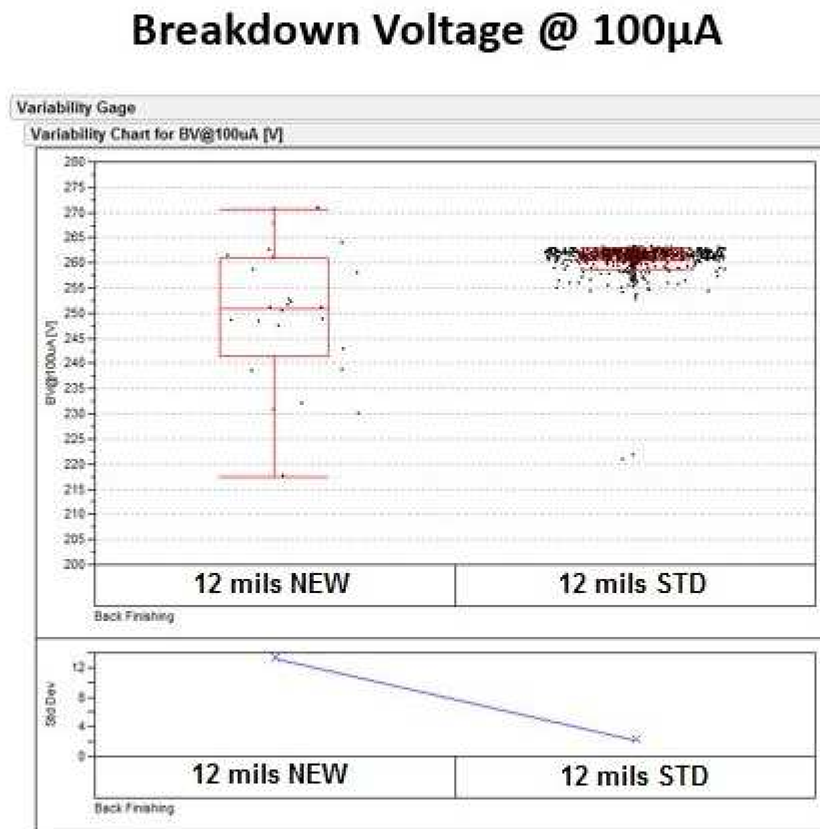

Fig. 6.3 Breakdown voltage variability chart comparison between standard and new devices.

6.2 Thermal Characterization

The thermal resistance is a simplified parameter characterizing the thermal performance of a device and his package. Generally, the internal structure of a discrete device is composed by different components. Depending on the choice of temperature detection points, distinctions are made as illustrated in figure 6.4. The total thermal resistance depends on the sum of the thermal resistances between the device junction and the ambient environment, which is the ultimate heat sink. In particular, it is given by:

$$Rth_{tot} = Rth_{j-c} + Rth_{c-s} + Rth_{s-a} \qquad (1.1)$$

where:

$Rth_{tot} =$ total thermal resistance

Rth_{j-c} = junction to case thermal resistance

Rth_{c-s} = case to heat sink thermal resistance

Rth_{s-a} = heat sink to ambient thermal resistance

Thermal resistance between the semiconductor junction and the junction's external case is an internal function of the design and manufacturing methods used by the device manufacturer. Because this resistance occurs within the device, the use of heat sinks or other heat-dissipating devices does not affect it. The semiconductor manufacturer decides upon this resistance by weighing such factors as the maximum allowable junction temperature, the cost of the device, and the power of the device.
The thermal impedance is defined as a quotient of the time function of a temperature difference divided by the impressed power dissipation. The static upper range value is the actual thermal resistance.

$$Zth(t) = \frac{T_1(t) + T_2(t)}{P} \quad (1.2)$$

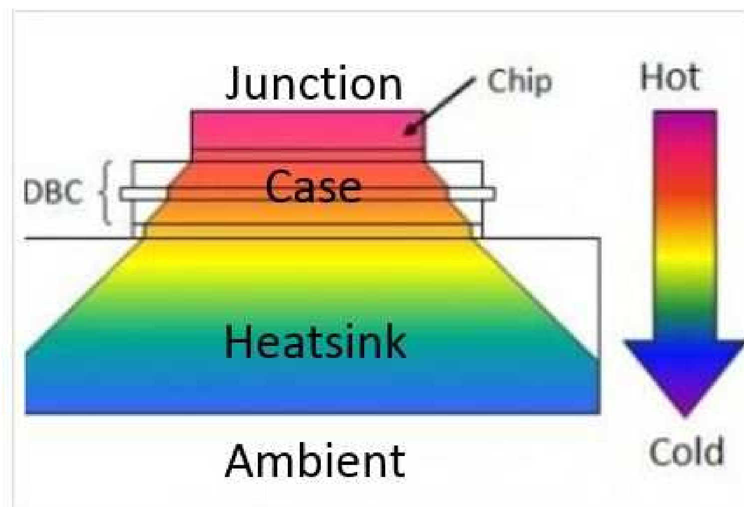

Fig. 6.4 Thermal heating distribution through the chip [1].

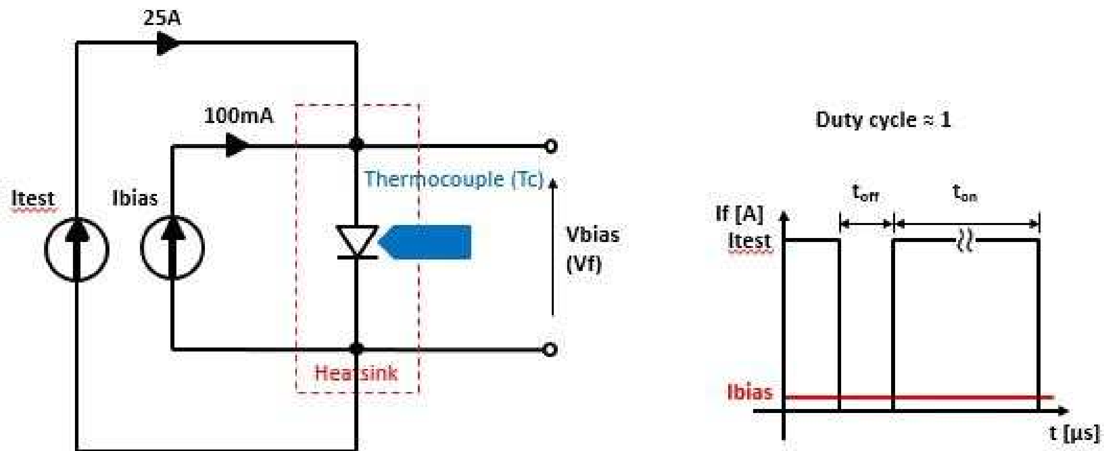

Fig. 6.5 Thermal measurements apparatus.

Thermal measurements were performed with the electronic circuit illustrated in figure 6.5. A thermocouple measures the case temperature during the direct diode polarization, thus the thermal resistance can be directly calculated.

Table 6.1 summarizes the thermal resistance values of both standard devices and the new ones. Moreover, the thermal impedance graph in figure 6.6 gives the thermal dynamic behavior.

THERMAL RESISTANCE RESULTS		
Samples	**12 mils STD**	**12 mils NEW**
N Rth j-c	6	6
Median Rth j-c	3.19	2.87
Mean Rth j-c	3.17	2.89
Std Dev Rth j-c	0.09	0.11

Tab. 6.1 Thermal resistance values summary.

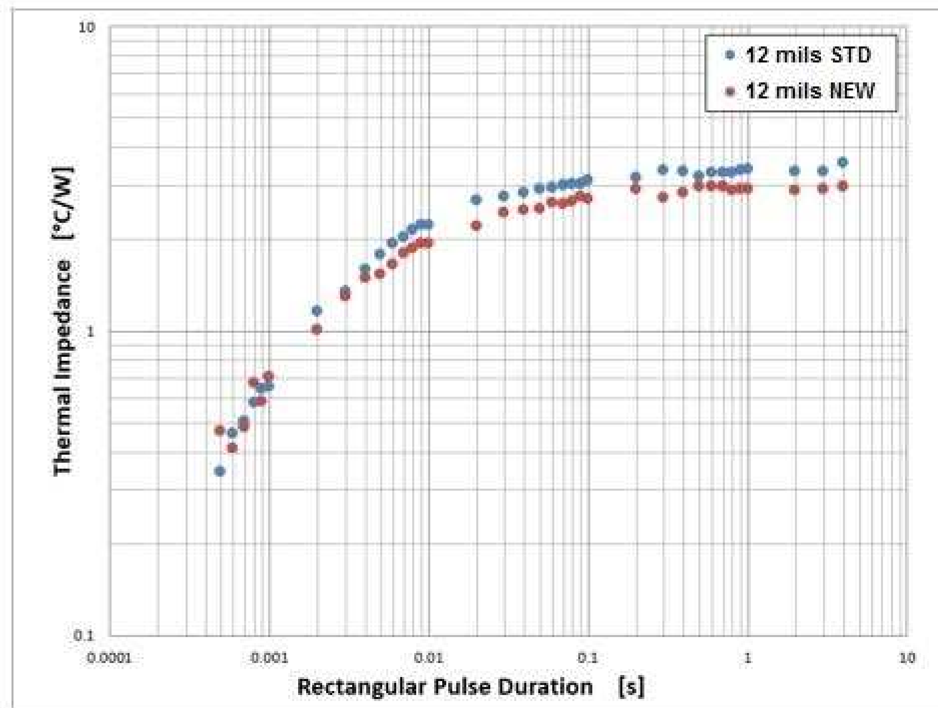

Fig. 6.6 Thermal impedance trend of standard devices and the new ones.

The results show that the new devices reach a thermal improvement of about 10% if compared to standard devices.

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Chapter 7

FAILURE ANALYSIS

This Chapter discusses the failure analysis results on new devices and the related root cause.

7.1 Failure analysis on assembled dice

The assembly process had a low yield, about 5-10% in reverse mode, thus the leakage was very high and the breakdown very low.
In order to understand the root cause, some failure analysis were performed.
After chemical decapsulation some cracks were found on both good and failed devices (see figure 7.1).

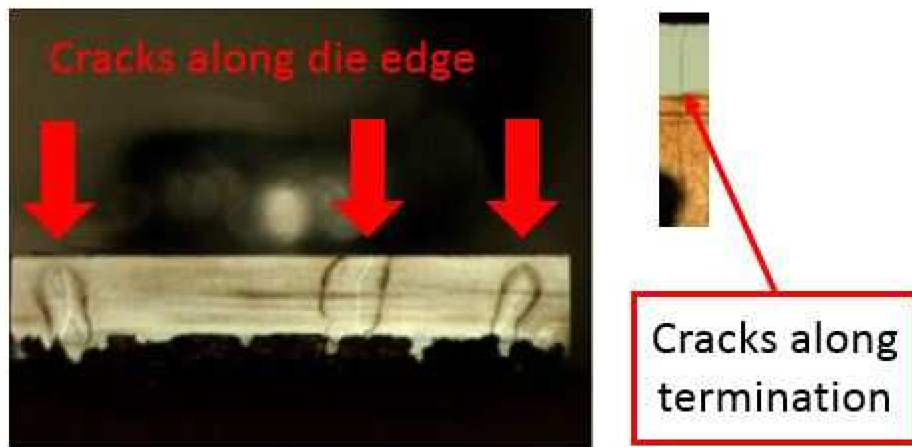

Fig. 7.1 Silicon cracks after chemical decapsulation.

Even after die section study on assembled devices, silicon cracks were found on both good and failed devices (see figure 7.2).

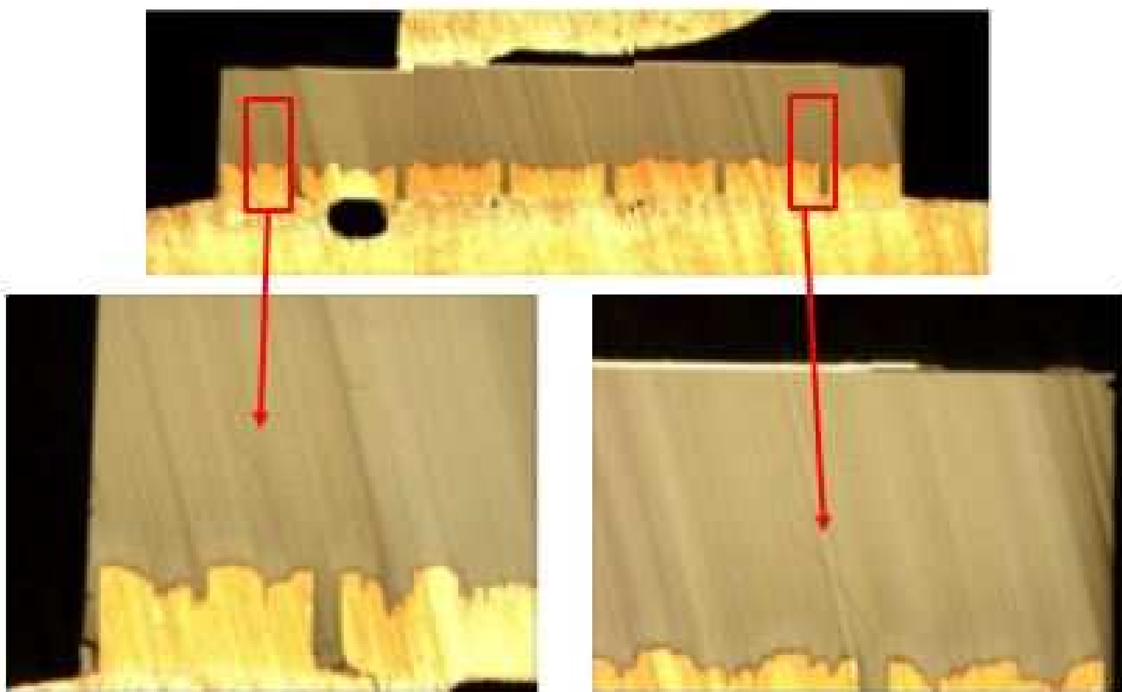

Fig. 7.2 Silicon cracks after mechanical chip section.

This cracks starts at the interface between the copper/silicon interface and then they spread until the device surface causing the termination degradation. Thus, the device is not more able to work in reverse conditions.

Before the assembly process, the dice did not show this kind of defect (see Chapter 4). The most critical assembly process step is the die attach (see Chapter 5) because of the high temperature peak (about 400°C) reached in a couple of minutes.

7.2 Forced dice degradation

The die attach profile is given in figure 7.3 (orange). Repeating this temperature profile in the laboratory (the blue one in figure 7.3), some non-assembled dice were heated with this thermal cycle.

Figure 7.4 shows the section analysis comparison between a non-heated dice and a dice after one thermal cycle.

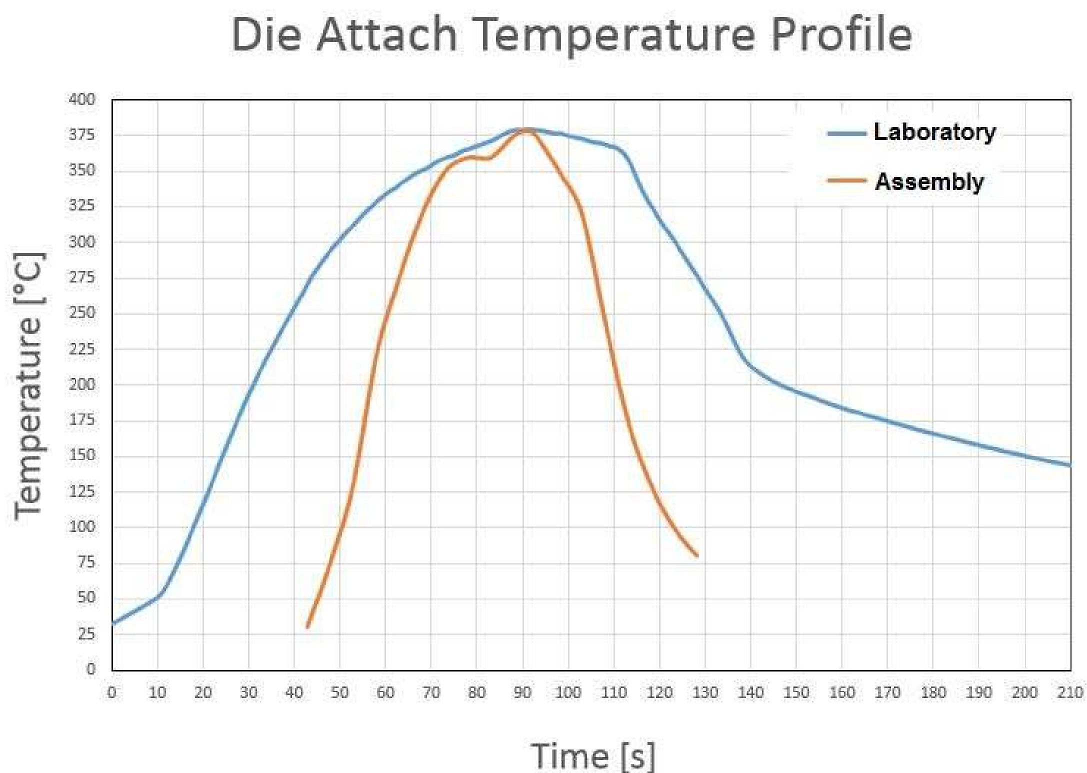

Fig. 7.3 Die attach assembly profile (orange) and temperature cycle repeated at the laboratory.

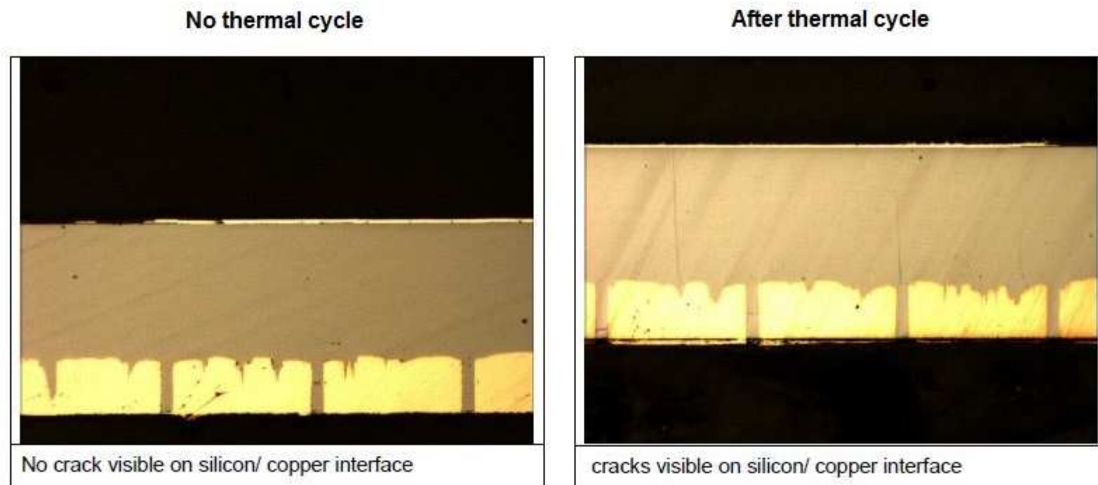

Fig. 7.4 Section study comparison between dice after thermal cycle and die without thermal cycle.

It was found that the root cause is the heat treatment. The copper expansion during heat treatment breaks the silicon bulk.

Chapter 8

CONCLUSIONS

The objective of this thesis work was to obtain a thermal resistance improvement in power electronic devices.
Nowadays, semiconductor manufacturing world adopts different thinning techniques to reduce the amount of material and hence the heat generation. These techniques are focused on silicon bulk material reduction with all the related handling issues.
The thesis project adopted an alternative way to achieve thermal resistance reduction overcoming handling issues and saving costs.
The development of an intrinsic heat sink by replacing silicon bulk material with copper, which has a higher conductivity, offers the advantage of maintaining the wafer "self-support" and allow working with already existing technologies saving on both dedicated thinning technologies and handling technologies.
With the goal of realizing this material replacement, a new process flow was designed, developed, optimized and applied to standard devices.
The cross sectional FESEM characterization showed a good adhesion between the different materials involved in the process flow: the silicon bulk material, the seed barrier layer composed by a stack of different metals, the thick electroplated copper and the back metal contact also made up of more metal layers.

Sample total thickness, hole deepness, hole width and wall width were the physical parameters quantitatively evaluated for different wafer areas suitably chosen along the whole wafer surface.
Holes and walls width had the lower standard deviation, meaning that the photolithography process reproduced a good homogeneous pattern on the substrate surface and that the photoresist hard mask survived the Bosch-DRIE plasma etch.
Hole deepness and sample total thickness had the higher standard deviation, especially the hole deepness. This two physical quantities are related each other to the final wafer planarization that was affected on both the wafer warpage and the non-homogeneous copper growth, thus the copper filling excess.
However, the high standard deviation value related to the hole deepness could mean a low homogeneity on Bosch-DRIE etching process.
Comparing all the aforementioned dimension values of the two processed wafer substrates, there is no relationship between the considered wafer area.
Since the median, mean and standard deviation calculated for each wafer are almost equal each other, the process flow is repeatable and overall homogeneous.
The most diffused defect is similar to “silicon micrograss” probably related to the starting wafer roughness because the Bosch-DRIE process does not create this kind of defect.
The non-verticality of silicon walls and copper voids are rare; even copper voids were founded only in one zone of one wafer, thus it could be due to cleanness.
The new devices exhibited good electrical parameters comparing to the standard device ones; in fact, the I-V diode characterizations were overlaid at low forward current. The higher the current, the lower becomes the forward voltage drop. It means that at higher current, the backside structure starts to do one’s duty.
The reverse electrical data of these new devices showed a higher standard deviation of both the leakage current and the breakdown voltage compared to the standard ones. However, the new standard devices data satisfied the upper and lower limits fixed by the standard devices. The difference between the distributions is due to the mechanical wafer stress.
Thermal characterization gave a thermal improvement of 10% compared to the standard device ones.
The electrical characterization after the wafer assembly gave a low reverse electrical yield because of silicon bulk cracks. These cracks forms during the dicing assembly process in which the diodes are subjected to high temperature gradient in a short period (400°C in $t = 0s$). Silicon cracks formation happens at the interface between silicon and copper, then thermally propagate until the surface of the substrate. In this way, the termination area degrades and the diode is no longer able to block the reverse voltage.

RINGRAZIAMENTI

Ringrazio la Vishay ed in particolare il gruppo R&D composto da L. Merlin, G. Richieri, C. Sanfilippo, M. Naretto, N. El-Baradai, R. Carta, L. Bellemo, P. Mercaldi, F. Crudelini, M. Nebiolo, E. Trentin. Grazie per avermi dato l'opportunità di intraprendere questo percorso e per avermi sostenuta ed aiutata durante il lavoro.

Ringrazio i ragazzi del laboratorio del Chilab, in particolare D. Perrone, S. Marasso, A. Tommasi, D. Mombello, S. Benetto per la preziosa collaborazione ed il lavoro svolto durante il progetto.

Ringrazio i professori del politecnico in particolare C.F Pirri, S. Ferrero, L. Scaltrito per avermi seguita ed indirizzata durante il progetto.

Un grazie speciale ai miei più cari amici Irene, Mattia e Natale che mi hanno dato un aiuto enorme sia dal punto di vista tecnico sia morale in questi anni di duro lavoro.

Un grazie altrettanto speciale alla mia famiglia ed ai miei amici Marco ed Elisa per avermi sempre sostenuta e creduto in me.

Grazie a Tommaso per aver sopportato insieme a me momenti molto duri ed avermi aiutato ad uscirne nel migliore dei modi.