

Foreword: Special Section on Addressing Signal and Power Integrity in Future Generation Systems—Part I: Technology and Design Considerations

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Foreword: Special Section on Addressing Signal and Power Integrity in Future Generation Systems. Part 1: Technology and Design Considerations

Ensuring Signal and Power Integrity (SPI) is a primary concern for the Electronic Packaging community. The continuous increase of operating frequencies, combined with more and more aggressive miniaturization and integration strategies, pose tremendous challenges to designers. Every transistor must receive power with reduced noise, and all signals must be received properly, despite the plethora of signal and power degradation effects due to crosstalk and electromagnetic interaction, losses and dispersion due to material non-idealities, reflections due to mismatches and discontinuities, just to name a few. Proper handling of such effects require precise characterization through modeling, suitable design strategies to minimize them, and the technological ability to realize the design.

This Special Section is the first of two Special Sections collecting a number of contributions that highlight some of the main directions that researchers from academia and industry are heading for managing SPI in future generation systems. The Authors for these two Special Sections were selected from the best papers presented at two major IEEE conferences dedicated to SPI topics that are held annually in the United States (EPEPS2015, San Jose, CA) and Europe (SPI2016, Torino, Italy). The first part has eight papers in two main categories: four focusing on the technological aspects of SPI and four on the design aspects. There will be another six papers in a forthcoming Special Section that will discuss advanced modeling aspects.

Four papers address technological aspects of SPI. K. Dieng *et al.* compare two different (axial and radial) architectures of Through Silicon Capacitors (TSC) in silicon interposers. TSCs are aimed at co-integration within Through Silicon Via (TSV) arrays for future power delivery network decoupling applications. A. Maffucci *et al.* demonstrate the theoretical feasibility of obtaining a resistance that decreases with increasing temperature in Carbon NanoTubes (CNT) interconnects up to a scale of fractions of millimeters. A technique for self-assembly of short CNTs is also proposed, together with experimental validation. N. G. Weimann *et al.* introduce a chip mounting technology suitable for low-cost assemblies for sub-mm-wave operation in the 300-500 GHz range. This technology is compatible with standard chip and submount fabrication techniques and achieves very low radiation losses through suitable thin-film shielded waveguide topologies. H. Oh *et al.* discuss heterogeneous microsystem integration by means of non-traditional TSV technologies. The latter include microflu-

idic heat sink and TSV integration, coaxial-shielding through multiple-ground TSVs, and partial air isolation for reducing TSV loss and capacitance at high frequencies.

Four papers address design topics. P-J Li *et al.* document a novel common-mode filter concept for suppressing radiation from cables attached to PCB structures. The filter relies on resistive materials for absorbing CM noise, differently from more standard reactive filters, CM chokes or EBG structures that may be band-limited and thus ineffective over a broad frequency band. E. A. Engin *et al.* also propose a filter concept, but targeting power plane noise in the GHz frequency range. Noise is rejected by arrays of quarter-wave resonators, suitably arranged as to create a virtual ground fence. H. Braunisch *et al.* describe an effective technique for reducing crosstalk, based on matching the characteristic impedance or admittance matrix. Significant Signal Integrity improvements are achieved for various on-package interconnect structures. D. Zhang *et al.* combine Low DropOut (LDO) voltage regulators with Power Transmission Lines (PTL) structures, with the aim of improving bandwidth and efficiency of power supply noise rejection. Measurements confirm a drastic reduction in power supply noise with respect to traditional plane-based design approaches.

These eight papers provide a great sampling of technology being considered to improve the SPI performance of future systems and design techniques to maximize the performance the technology can provide.

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