Demonstration of a Partially Integrated Silicon Photonics ONU in a Self-Coherent Reflective FDMA PON

Demonstration of a Partially Integrated Silicon Photonics ONU in a Self-Coherent Reflective FDMA PON

(Invited Paper)

S. Straullu, P. Savio, G. Franco, R. Gaudino, *Senior Member*, *IEEE,* V. Ferrero, S. Bernabé, M. Fournier, V. Muffato, S. Menezo, B. Charbonnier, E. Temporiti, D. Baldi, G. Minoia, M. Repossi, L. Carroll, J. Lee, P. O'Brien, R. Marchetti, G. Duan, F. Saliou and S. Abrate, *Senior Member*, *IEEE*

***Abstract* — We report about the final results of the FABULOUS European project, demonstrating the feasibility of real-time Ethernet transmission on a self-coherent reflective Passive Optical Network, using an Optical Network Unit whose main optical functions are performed by a silicon-photonics device; 500 Mbps per user with a power budget of 24 dB in off-line processing and 21 dB in real-time is shown. We also report details about the packaging process and the special technique developed for the flip-chipping of a CMOS electrical driver, used for driving the ONU with low voltage, onto a Silicon Mach Zehnder Modulator.**

***Index Terms* — Passive Optical Network, Reflective Modulation, Self-coherent detection.**

I. Introduction

Optical access networks are evolving to provide higher capacities to the end users. For residential, business and mobile networks, the main driver to replace copper by fibre is the feasibility to support large broadband services. G-PON (Gigabit capable Passive Optical network) has been now deployed for more than a decade. The standardisation entities FSAN (Full Service Access Network) and ITU-T had defined a first renewal PON generation working at 10 Gbps and 2.5 Gbps for up- and down-stream, which is named XG-PON (the former XGPON1), and the deployment of this 10 Gbps generation is ramping up. In order to provide symmetrical line bitrates at lower costs, the most recent PON standard proposed to remain with fixed wavelength solutions and defined the G.9807.1 [1] standard named XGS-PON offering symmetrical 10 Gbps. The same standardisation entities had also defined a second renewal generation which is named Next Generation PON 2 (NG-PON2), then standardized as G.989 [2]; two multiplexing options are then available: a Time and Wavelength Division Multiplexing (TWDM) PON and a Point to Point Wavelength Division Multiplexing (P2P WDM) PON. Whereas the previous PON standards used fixed pair of wavelength for both upstream and downstream transmissions, NG-PON2 relies on colourless optics at the ONU (Optical Network Unit) in order to save on inventory and operational complexity and to provide more flexibility for other operational advantages as load balancing between wavelength, protection mechanism, and power saving; however, the cost of tunability could be a challenge: technology maturity and high volumes are the expected solution to help the deployment of NG-PON2.

Recently, the optoelectronic technology inside Small Form factor Pluggable (SFP) transceiver became compatible with 25 Gbps line rates; then, next steps in standardization should be to introduce the 25 Gbps over fixed wavelength, by proposing a 25 Gbps PON and/or over multiple wavelengths, by proposing a 100 Gbps PON. Going even beyond, future optical access standards will certainly be open to be designed on disruptive photonic technologies which will give the possibility to re-attribute or reuse parts of the optical spectral bands already occupied by all the legacy PON generations.

The FABULOUS European Project [3], concluded in June 2016, was conceived when XG-PON2 was mostly a wish-list and XGS-PON not even under consideration, and proposed a Frequency Division Multiple Access (FDMA) self-coherent reflective PON suitable for the full realization of the optical part of the Optical Network Unit (ONU) on silicon-photonics platform, targeting capacities greater than the ones achieved by G.989 equipment while trying to keep the cost lower. To date, we have already demonstrated:

- the potential of the architecture with discrete optical components and the off-line processing approach: using a 11 GHz $LiNbO_3$ modulator, we achieved an aggregate

This work was supported by the EU FP7 project FABULOUS under contract 318704.

S. Straullu, P. Savio, G. Franco and S. Abrate are with Istituto Superiore Mario Boella, 10138 Torino, Italy (e-mail: straullu@ismb.it).

R. Gaudino and V. Ferrero are with Politecnico di Torino, Dipartimento di Elettronica e Telecomunicazioni, 10129 Torino, Italy (e-mail: gaudino@polito.it).

S. Bernabé, M. Fournier, V. Muffato, S. Menezo and B. Charbonnier are with CEA-Leti, 38000 Grenoble, France, (e-mail: stephane.bernabe@cea.fr).

E. Temporiti, D. Baldi, G. Minoia and M. Repossi are with STMicroelectronics, 27100 Pavia, Italy (e-mail: enrico.temporiti@st.com).

L. Carroll, J. Lee and P. O'Brien are with Tyndall National Institute, Cork, Ireland (e-mail: lee.carroll@tyndall.ie).

R. Marchetti is with Università degli Studi di Pavia, 27100 Pavia, Italy (e-mail: riccardo.marchetti02@universitadipavia.it).

G. Duan is with III-V Lab, 91767 Palaiseau, France (e-mail: guanghua.duan@3-5lab.fr).

F. Saliou is with Orange, 22307 Lannion Cédex, France (e-mail: fabienne.saliou@orange.com).

capacity of 32 Gbps per wavelength and per direction over an Optical Distribution Network (ODN) loss of 31 dB [4, 5, 6], compatible with XG-PON ODN class N2;

- the feasibility of a partially integrated version of the ONU having a silicon reflective MZM with an electrical driver flip-chipped on top [7], with preliminary off-line constellations demodulation.

We claimed that the FABULOUS approach, being based on silicon-photonics, is conceived for achieving mass-market electronics volumes and prices, but the credibility of this statement is also related to the feasibility of the Digital Signal Processing (DSP) implementation for real-time transmission on ASIC platforms; we already estimated that the needed DSP, if implemented on 65 nm CMOS technology, would require a 7 mm^2 chip with a power consumption lower than 4.2 W, but in this paper for the first time we demonstrate real-time transmission with the partially integrated silicon photonics ONU and Field Programmable Gate Arrays (FPGA) to implement the DSP and the Ethernet protocol.

II. Assembly of Packaged Module

The core of the FABULOUS ONU consists of a Silicon Photonic Integrated Circuit (Si-PIC) with a bidirectional Reflective Mach Zehnder Modulator (R-MZM), onto which a CMOS Electronic Integrated Circuit (EIC), to drive the modulator, is flip-chip bonded, as depicted in Fig. 1(a) and (b). The R-MZM [7] is made up of a Si-PIC comprising a 2D Grating Coupler (GC) acting as a Polarizing Beam Splitter (PBS) and a segmented Mach-Zehnder intensity modulator with its flip chipped CMOS Electronic Integrated Circuit (EIC) driver. The segmented electrodes correspond in total to a doped electrode length of 3 mm. It was then pigtailed, packaged and integrated on a test board for system experiments. A first generation of the R-MZM device (EIC excluded) exhibited a $V_\pi \cdot L_\pi$ of 4 V·cm and an E/O bandwidth of 20 GHz when biased at −1 V [7]. A new generation run of this device, that we used for the experiments described in this paper, provided better performances in terms of $V_\pi \cdot L_\pi$ product (2 V·cm) leading to a V_π = 7 V. Reflective polarization independent optical carrier suppressed modulation was demonstrated with both devices.

Flip-chipping the EIC onto the R-MZM was a challenging packaging aspect and much activity on the optimization of such process has been carried out to achieve high yield and, possibly, low cost. The electrical and thermal connection between the PIC and EIC is made through 484 discrete Copper-Pillar-Bumps (CPBs), as shown in Fig. 1(c). The CPBs have a diameter of ≈25 µm, and are formed by Cu electro-plating of the under-bump metal-pads on the PIC and EIC, followed by the deposition of a lead-free Sn-Ag-Cu solder-cap. This solder-cap is quickly coated by a native-oxide layer that must be removed during the flip-chip bonding, to ensure good electrical and mechanical connection between the PIC and EIC. Initial flux-free thermo-compression tests gave poor bonding results - systematic misalignment of the EIC- and PIC-CPBs, solder-squeezing that could lead to electrical shorts, etc. Instead, the ONU was assembled with a new "no clean" flux solder-reflow process, using a VOC-free (Volatile Organic Compounds) flux that activates and then evaporates at the melting-temperature of the solder-cap [8]. This means that no post-bonding solvent-rinse is needed, minimizing the risk of displacing contaminants onto the grating-couplers on the surface of the PIC [9, 10]. As shown in Fig. 1(d), after solder-reflow bonding for 250 ºC for 30 s, the alignment of the PIC- and EIC-CPBs is excellent, and there is no evidence of solder-squeezing. We speculate that the surface tension from the 480 molten solder-caps is sufficient to "self-align" the matched pairs of CPBs. Electrical resistance measurements, destructive tear-off tests and X-ray microscopy were all used to verify the quality of the CPBs. Once optimized, the yield of the "no clean" flux solder-reflow bonding was 100% for the small number of samples (≈20) prepared within the FABULOUS project.

The ONU uses a single 2D-GC as a combined input and output interface with a standard single mode telecom fiber (SFM-28). To facilitate optical alignment to this main coupler, a pair of widely-spaced 1D-GCs are included on the PIC, to form an "optical shunt". The spacing between the 2D-GC and 1D-GCs on the integrated device (250 µm) is chosen to exactly match the nominal spacing of the individual fibers in the SMF-28 multi-channel Fiber-Array (FA) block used to bring optical signals to/from the ONU, as represented in Fig. 2(a)-(d).

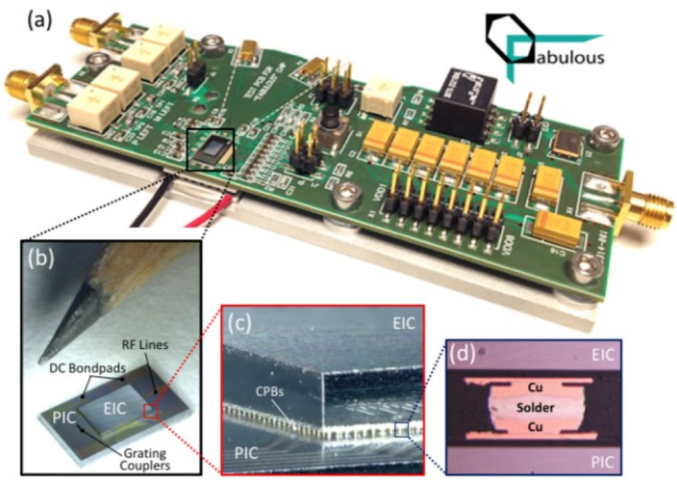

Fig. 1(a) Image of FABULOUS module consisting of the ONU mounted in a PCB with front-end electronics, and with temperature stabilization provided by a thermo-electric cooler. (b) Zoom-in of the ONU, consisting of a Si-PIC bonded to a EIC, with a pencil tip for scale. (c) Further zoom-in of the ONU, showing the many discrete copper pillar bumps used to form the electrical, thermal, and mechanical connection between the PIC and EIC. (d) Microscope image of the solder-reflow flip-chip bond formed between a pair of CPBs on the PIC and EIC. This image was created by destructively grinding-down and then polishing-back a bonded ONU that had been mechanically stabilized by an epoxy under-fill.

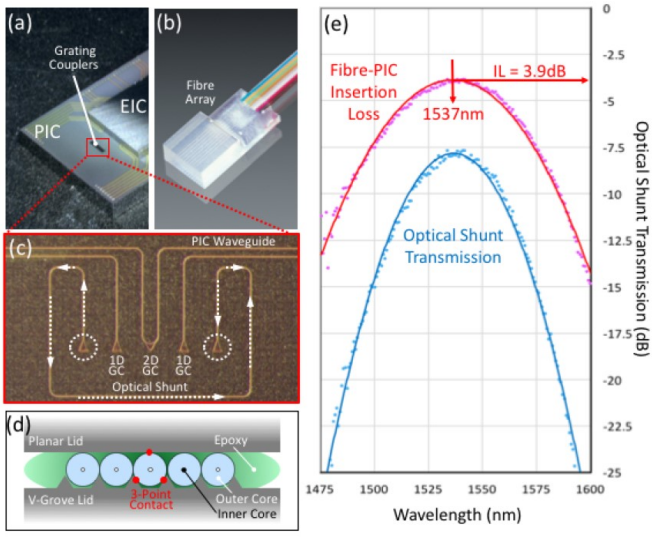

Fig. 2(a) Location of grating-couplers on the PIC surface. It is necessary to have an "exclusion zone" around the grating-couplers, to ensure the fiber-array does not overlap with the EIC or delicate wire-bonds. (b) Image of the multi-channel fiber-array used to transport the optical signal to/from the ONU. One channel is used for the signal, and other channels to support the optical alignment (and other on-PIC diagnostics). (c) Microscope image of the optical interface on the PIC, including an optical shunt between two 1D-GCs. The optical signal to/from the ONU passes through the central 2D-GC, while the Fiber-PIC alignment is optimized by maximizing transmission through the optical shunt. (d) Schematic of the precision alignment of individual fibers in the multi-channel fiber-array block. (e) The optical shunt transmission spectrum (blue markers), fitted by a Gaussian curve (blue line). Given that the shunt should have no appreciable waveguide losses, the Fiber-PIC insertion loss (-3.9 dB) of the 1D-GC can be estimated as half the dB value of the shunt transmission.

Since the concentricity tolerances of the individual fibers in the FA-block (±0.5 µm) are significantly tighter than the 1 dB Fiber-GC alignment tolerance (±2.5 µm), an active-alignment procedure that maximizes the transmission through the optical shunt also aligns a fiber-channel to the 2D-GC, ensuring a low Insertion Loss (IL) to the ONU. Figure 2(e) illustrates the transmission through the optical shunt, which shows a maximum of -7.8 dB at 1537 nm, as well as the implied Fiber-PIC IL of the 1D-GC, i.e. 3.9 dB (=7.8 dB/2). The 1 dB and 3 dB coupling bandwidths of the 1D-GC are 40 nm and 70 nm, respectively.

III. Experimental Setup and Characterization

The experimental setup for the upstream (US) direction is shown in Fig. 3; downstream (DS) is not shown as it is a straightforward point-to-multipoint communication with an avalanche photodetector (APD) at the ONU receiver side. A continuous wave (CW) optical seed (N7714A model from Agilent) at 1550.92 nm and +9 dBm launch power is generated at the Optical Line Terminal (OLT) and sent to the ODN, which is composed by 25 km of Single Mode Fiber (SMF), a variable optical attenuator (VOA) to act on the ODN loss and a 1x4 optical splitter. The CW seed, after going along the ODN, reaches the input of two active reflective ONUs: ONU1, composed by optical discrete components [5], and ONU2, where the R-MZM is integrated on a Si-PIC. At each ONU, the optical signal is amplified by a Semiconductor Optical Amplifier (SOA), reflected back by the R-MZM (discrete or integrated) and modulated with the upstream signal.

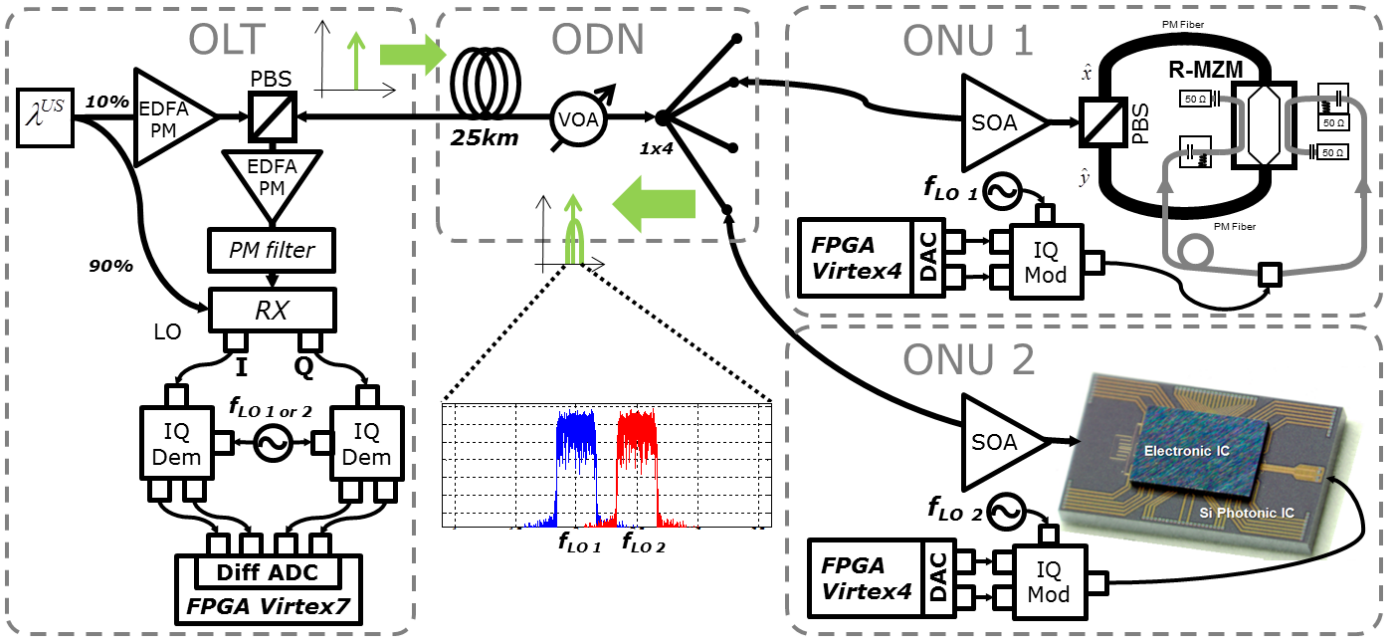

Fig. 3 FABULOUS real-time experimental setup (ADC: Analog-to-Digital Converter; DAC: Digital-to-Analog Converter; EDFA: Erbium-Doped Fiber Amplifier; PBS: Polarizing Beam Splitter; PM: Polarization Maintaining; SOA: Semiconductor Optical Amplifier; R-MZM: Reflective Mach-Zehnder Modulator; VOA: Variable Optical Attenuator).

We characterized the integrated R-MZM when installed in the ONU 2 using the setup depicted in Fig. 4. An optical circulator was placed in front of the ONU, in order to separate the bidirectional optical signals; an Optical Spectrum Analyzer (OSA) was used in order to compare the peak power of the optical signal at the input and the output of the ONU (port 2 and port 3 of the optical circulator, respectively), thus obtaining the full ONU optical gain (or insertion loss). The same measurement was performed removing the SOA, thus obtaining the insertion loss of the R-MZM. The results are summarized in Fig. 5 as a function of the optical power of the signal at the ONU input, from which it can be seen that the R-MZM fiber-to-fiber insertion loss is about 30 dB, while the overall ONU gain (Si-PIC + SOA) is more than 6 dB for input power levels lower than -15 dBm.

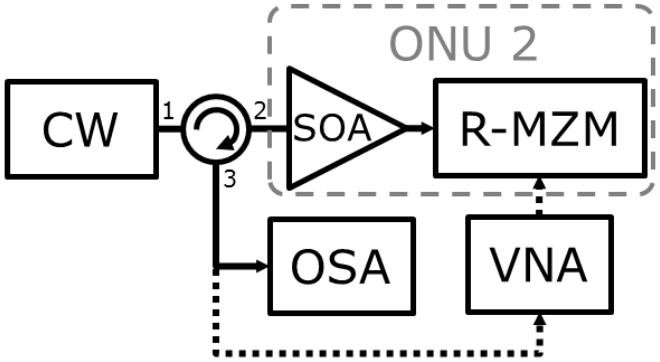

Fig. 4 Integrated ONU characterization setup (OSA: Optical Spectrum Analyzer; SOA: Semiconductor Optical Amplifier; R-MZM: Reflective Mach-Zehnder Modulator; VNA: Vector Network Analyzer).

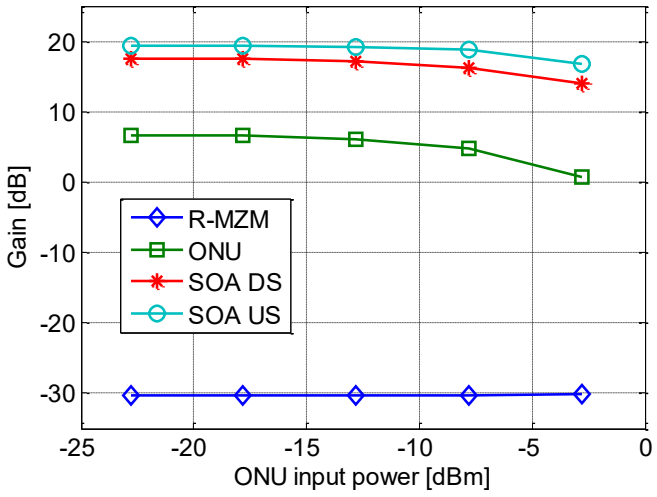

Fig. 5 R-MZM, SOA and overall ONU optical gain vs. the optical power of the signal at the integrated ONU input.

We also evaluated the electrical bandwidth of the ONU under test by means of a 20 GHz Vector Network Analyzer (VNA). As reported in Fig. 6, we measured a 3 dB bandwidth of about 6 GHz for the full R-MZM + EIC device.

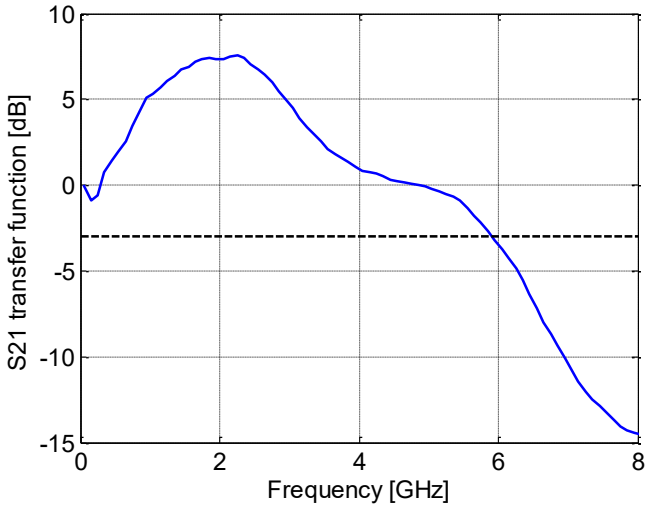

Fig. 6 Integrated ONU (R-MZM + EIC) electrical bandwidth measured by means of a 20 GHz Vector Network Analyzer.

The proposed FDMA architecture requires DSP at both the ONU and OLT sides in order to adapt an Ethernet digital data stream to the specific FABULOUS physical layer. ONU and OLT units have been implemented on FPGA cards equipped with high speed Analog-to-Digital (ADC) and Digital-to-Analog (DAC) converters chipsets. As the ONU is expected to be a low cost device, we decided to implement it on a FPGA board with relatively limited computational resources, so that we selected a Bitsim UHAB board equipped with two Virtex4 SX35 FPGAs and two Analog Devices AD9736 DAC, running at 1200 MSps.

The DAC baseband two outputs are connected to an external electrical I/Q modulator and a local oscillator selects the appropriate upstream FDMA carrier frequency. At the OLT, the upstream signals pass through a pre-amplifier and an optical filter before being demodulated by means of a single polarization optical coherent receiver, where the transmitted CW signal is also used as local oscillator in a homodyne self-coherent setup. The single polarization operation is made possible by the ONU 90° polarization rotation that is intrinsic in the structure of the reflective ONU [5]. The coherent detection process requires a more intensive DSP to be implemented at the OLT side; therefore, it is built around a higher performances Xilinx VC707 evaluation board, equipped with a Virtex7 XC7VX485T FPGA, connected to a Texas Instruments ADC12D2000RF evaluation board, running at 1200 MSps. The coherent receiver's two outputs are demodulated by means of two electrical I/Q demodulators, whose local oscillator can be set to the carrier frequency of the US signal to be detected. The four resulting I and Q signals are combined by the ADC input differential buffers and sampled by the dual channel 1200 MSps ADC, in order to process them with our low speed DSP [11].

IV. System Results

The characteristics of the FDM signal and of the DSP used for the set of experiments were widely described in previous literature [5, 6] about the activity we carried out with discrete components, and the main features are briefly reported in the following for sake of clarity only:

- the baud-rate for each electrical carrier considers a 20% overhead to allow long Forward Error Correction (FEC) and eventual signaling;
- the channel spacing is equal to the baud-rate plus roll-off factor of 0.1 (yielding for example to a spacing of 330 MHz for a line-rate of 300 MBaud);
- the real-time DSP consists of a 64 complex taps FIR filter, updated according to a Constant Modulus Algorithm (CMA) stage, followed by a Radius Directed Estimator (RDE) stage and a 16 taps memory Carrier-Phase Estimator (CPE).

We first tested the integrated R-MZM by modulating it with a 300 MBaud, 16-QAM upstream signal centred at 2 GHz. As reported in Fig. 7 (left), the received constellation is very noisy even in back-to-back, as demonstrated by the resulting BER = $2 \cdot 10^{-3}$. Therefore, we switched to a more robust 300 MBaud QPSK, Fig. 7 (right), thus halving the resulting bit-rate to 500 Mbps per user, but achieving an error-free transmission over more than 10^6 samples. The use of QPSK provides also more robustness with respect to the laser linewidth, that can be a sensitive parameter in this system: in [6], for example, we have shown that, with the ECL unit used in our setup (nominal linewidth <100 kHz, measured ~20 kHz), it was not possible to transmit 64-QAM signals with a bandwidth of 330 MHz.

Using QPSK modulation and targeting a transmission link of 25 km, we then evaluated the stability of our system, by monitoring the BER over more than 24 hours: the instant BER never overcame the value of 10^{-9} for all the observation time, with several error-free transmission periods, as reported in Fig. 8.

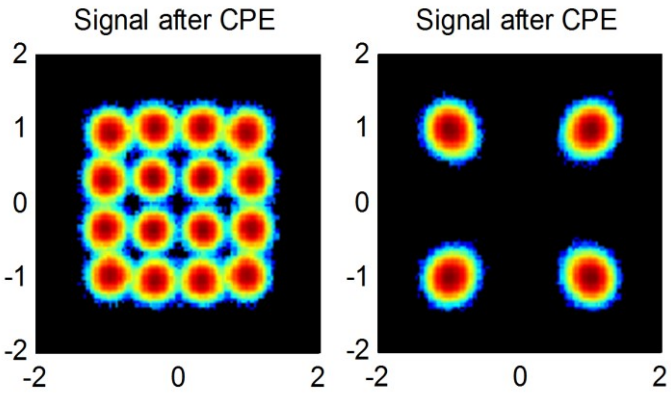

Fig. 7 US 16-QAM (left) and QPSK (right) back-to-back constellations generated by the integrated ONU.

We also evaluated how the BER changes when increasing the ODN loss, acting on the VOA placed at the end of the fiber. As reported in Fig. 9, the system supports 21 dB of ODN loss considering a FEC with 10^{-4} outage threshold, that is the one we have been able to implement on FPGA.

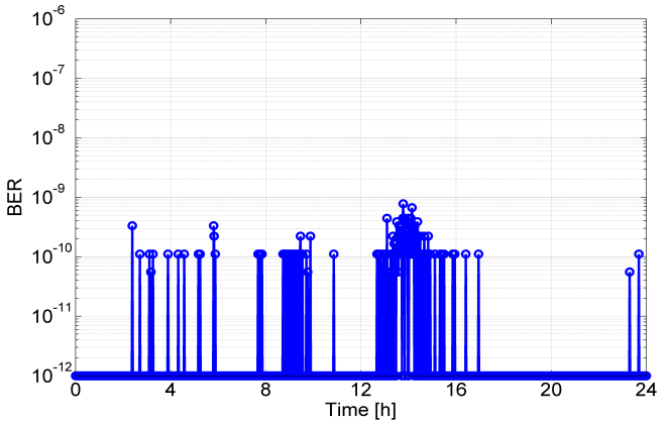

Fig. 8 Real-time BER of the US QPSK signal generated by the integrated ONU after 25 km vs. time.

We then repeated the same measurement in post-processing, replacing the FPGAs with a 12 GSps arbitrary waveform generator at the ONU and with a 50 GSps real-time oscilloscope at the OLT, and implementing in Matlab© the same DSP (imposing to the software the limitations due to hardware), obtaining the same BER curve but now being able to extend it to higher values, in order to compare with the benchmark we obtained with discrete components (to the point of considering a FEC capable of correcting up to an incoming threshold of 10^{-2}) [5, 6]. Clearly, the ODN loss values achieved with the partially integrated ONU (up to 24 dB in off-line processing) are lower than with the discrete ONU, and this is mostly due to the high insertion loss of the R-MZM. It also has to be highlighted that for the full off-line experiments we considered a FEC capable of correcting up to 10^{-2}, as FDMA allows to increase at will the complexity of the processing (no burst mode transmission needed), while we didn't have the related FPGA IP available for real-time implementation, thus lowering the achievable ODN loss in real-time operation with respect to the post-processing performance.

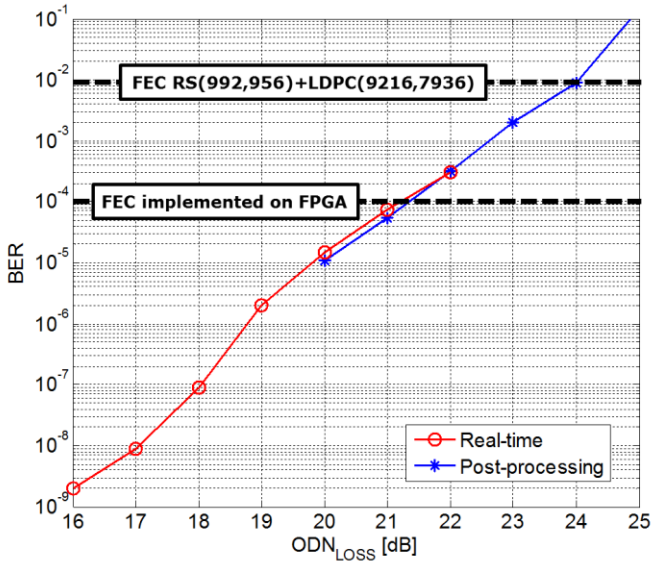

Fig. 9 Real-time and post-processing BER of the US QPSK signal generated by the integrated ONU vs. ODN loss.

Finally, we switched on both ONUs in order to verify how the two adjacent FDM-QPSK upstream channels interfere to each other. In particular, we observed how the BER of the signal generated by the integrated ONU changes when reducing the frequency spacing Δ_f between the FDMA carriers assigned to the two ONUs. As expected, until the frequency spacing is higher than each channel bandwidth (330 MHz), the interfering ONU does not affect the ONU under test performance, as reported in Fig. 10. This result is consistent with what we already demonstrated with discrete components in [6], highlighting then good linearity in the integrated R-MZM behavior.

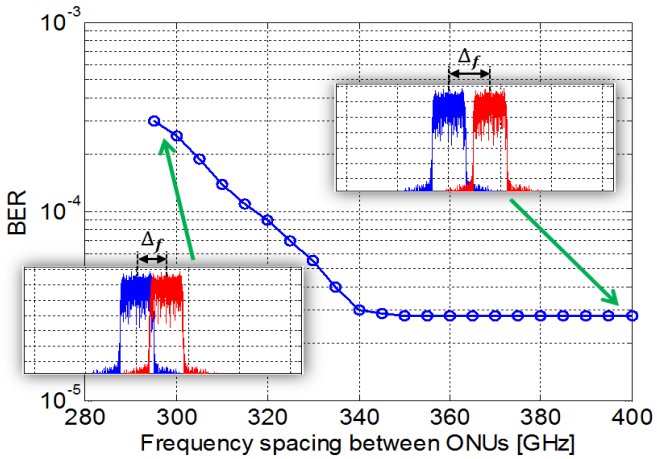

Fig. 10 Real-time BER of the US QPSK signal generated by the integrated ONU vs. frequency spacing between ONUs.

V. Conclusions

We demonstrated the feasibility of a reflective ONU with an unprecedented level of optical integration allowing to achieve interesting performances in terms of bit-rate and ODN loss in a reflective PON, thanks to massive employment of DSP; we also demonstrated the real-time feasibility of such DSP, that can be implemented on ASIC for realizing an integrated ONU with consumer-electronics target prices. To summarize, for the first time, an integrated Silicon MZM is operated in real time over the FDMA PON proving that the different important features demonstrated with discrete components (reflective polarisation insensitive carrier suppressed modulation) can be obtained at low cost and high production volume with a fully integrated silicon ONU.

Even though the project was officially concluded, the partners are committed to keep working on the architecture, as the overall concept is quite promising, also in sight of the standardization process described in the introduction, and we also believe that improving the performances of the ONU integrated circuit is fundamental to finally boost the adoption of SiP in the access segment; therefore, a further SiP circuit is on its way comprising the PBS (2D-GC), a travelling wave MZM and two InP over Si optical amplifiers [12], and prototypes for full system tests are expected to be available in spring 2017.

References

[1] ITU-T Recommendation G.9807.1 (06/2016) "10-Gigabit-capable symmetric passive optical network (XGS-PON)"
[2] ITU-T Recommendation G.989 (10/2015) "40-Gigabit-capable passive optical networks (NG-PON2): Definitions, abbreviations and acronyms"
[3] Project web site: www.fabulous-project.eu.
[4] S. Straullu et al., "Single-Wavelength Downstream FDMA-PON at 32 Gbps and 34 dB ODN Loss", IEEE Photonics Technology Letters, vol. 27, no. 7, pp. 774–777, Apr. 2015.
[5] S. Straullu et al., "Optimization of reflective FDMA-PON architecture to achieve 32 Gb/s Per upstream wavelength over 31 dB ODN loss," J. Lightw. Technol., vol. 33, no. 2, pp. 474–480, Jan. 2015.
[6] S. Abrate et al., "Overview of the FABULOUS EU Project: Final System Performance Assessment With Discrete Components," J. Lightw. Technol., vol. 34, no. 2, pp. 798–804, Oct. 2015.
[7] S. Menezo et al., "Transmitter Made up of a Silicon Photonic IC and its Flip-Chipped CMOS IC Driver Targeting Implementation in FDMA-PON", J. Lightw. Technol., vol. 34, no. 10, pp. 2391–2397, May 2016.
[8] Multicore MF210 VOC-free No Clean Flux - http://www.henkel-adhesives.com
[9] A. Horibe, K-W Lee, K. Okamoto, H. Mori, and Y. Orii, "No Clean Flux Technology for Large Die Flip Chip Packages," IEEE Electronic Components & Technology Conference, 2013.
[10] Serene Lee Choon Mei, Carlo Marbella, Tan Ai Min, "No-clean Polymer Flux Evaluations and its Impact on BGA Solder Joint Quality and Board Level Reliability," 34th International Electronic Manufacturing Technology Conference, 2010.
[11] B. Charbonnier et al., "Demonstration of Low DSP Requirements for FDMA PON", *ECOC 2014*, P7.4, Cannes, France.
[12] P. Kaspar et al., "Hybrid III-V/Silicon SOA in Optical Network Based on Advanced Modulation Formats", Photonic Technology Letters, Vol. 27, No. 22, 2015