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# Reliability Estimation at Block-Level Granularity of Spin-Transfer-Torque MRAMs

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***Abstract*— In recent years, the Spin-Transfer-Torque Magnetic Random Access Memory (STT-MRAM) has emerged as a promising choice for embedded memories due to its reduced read/write latency and high CMOS integration capability. Under today aggressive technology scaling requirements, the STT-MRAM is affected by process variability and aging phenomena, making reliability prediction a growing concern. In this paper, we provide a methodology for predicting the reliability of an STT-MRAM based memory (assuming high thermal stability). The reliability estimation is performed at block level for different block sizes and access rates. The proposed methodology also allows for an exploration of required error correction capabilities as function of code word size to achieve desired reliability target for the memory under study.**

***Keywords-Emerging memories, STT-MRAM, Memory Reliability***

## I. INTRODUCTION

Due to the rapid development of smartphones, netbooks and tablets, the need for high density, low power, high performance SoCs has pushed the well-established embedded memory technologies (e.g., SRAM, DRAM, Flash) to their limits. To overcome this issue, emerging technologies are being developed and implemented.

A promising candidate for next generation embedded memories is the Spin-Transfer Torque Magnetic Random Access Memory (STT-MRAM) [1]. STT-MRAM offers faster read and write access time (nanoseconds) and better CMOS integration than other available technologies with similar features. With scaling, the STT-MRAM cell is facing a set of challenges that strongly impact performance and reliability, severely affecting the yield of the memory array. These issues are mainly related to process variations of MOS and MTJ devices ([2], [3], [4], [5]), to the high write power consumption ([6], [7]), and to the thermal fluctuations in the MTJ switching ([8]).

The main degradation mechanism known to affect the MTJ element is the *breakdown mechanism* (hard or soft). The hard breakdown is caused by dielectric breakdown of the tunneling barrier and it is a sudden phenomenon which annihilates the tunneling effect. The soft breakdown is a gradual degradation of the MTJ device due to repetitive voltage stressing causing a gradual degradation of the resistive characteristics of the storage element [9], [10], [11], [12].

The MOSFET transistors are deteriorated by aging mechanisms like hot-carrier injection (HCI), radiation induced damage, and bias temperature instability (BTI). With the introduction of high-k transistor gates, the nMOS transistor becomes sensitive to the PBTI (positive BTI) effect [13], [14]. Several works have studied the effects of PBTI on the reliability of the SRAM cell – [15], [16] among others – but limited publications are available on evaluating its effect on STT-MRAMs.

To assure highly reliable embedded memory, the behavior of a memory block has to be studied in detail in all the operation modes, under different environmental conditions to assure a highly reliable embedded memory.

In this paper, we present a methodology for memory reliability prediction at block level (as function of block size, and block access rate), given the failure distribution of a single cell. It is important to note here that the characterization of a single cell is out of scope of this paper and therefore the cell failure distribution here considered is based on data retrieved from the literature. Without loss of generality, the proposed reliability estimation methodology is based on a 1T-1MTJ STT-RAM cell.

As an application example, the proposed methodology is used to select the necessary error correction code capability to satisfy imposed reliability targets in a given STT-MRAM memory block.

Given the current trend on cell designs with high magnetic bit thermal stability [17], this paper is focused on this class of STT-MRAM cells. In this way the behavior of the memory cell and block in data retention is stable [18].

This paper is organized as follows. In Section II, the operation principles of an STT-MRAM cell are briefly described. The third section describes the proposed methodology for block reliability estimation. Section IV includes a discussion on the required error correction capabilities, as function of code word size, for achieving different reliability targets for the memory under study. Finally, Section V concludes the paper.

## II. STT-MRAM CELL: OPERATION PRINCIPLE AND ELECTRICAL MODEL

In this section, the STT-MRAM cell operation principle and corresponding electrical model are described.

### A. Operation Principle

In an STT-MRAM memory, information is stored into a magnetic tunneling junction (MTJ) device. Typically, an MTJ element consists of one oxide barrier layer sandwiched between at least two ferromagnetic layers (FLs), characterized by their own magnetic orientation. One of the two magnetic layers, referred to as fixed layer, has a fixed magnetic orientation set during fabrication time, whereas the other, called free layer, has a freely rotating magnetic orientation that can be dynamically changed by forcing sufficient tunneling currents across the device (Fig. 1). The conductance of such a tunneling junction can vary depending on whether the magnetizations of the FLs have parallel or antiparallel orientations. This effect is called *tunneling magnetoresistance* effect (TMR) and it is characterized by means of the *TMR ratio*, given by the ratio between the conductances (resistances) of both orientations.

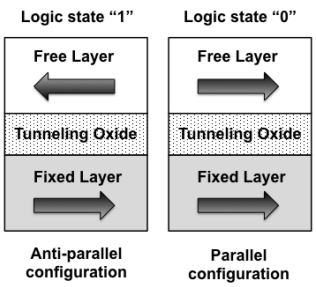


**Figure 1:** MTJ Configurations

### B. Electrical Model of STT-MRAM

The data stored is charged by applying a sufficiently large spin-polarized current through the MTJ device [19], long enough to switch the magnetization direction of the free layer. When both fixed and free layer feature the same magnetic orientation (parallel state), the MTJ exhibits a low resistance ($R_{MTJ}=R_L$). When, on the other hand, they have opposite magnetic orientation (anti-parallel state) MTJ exhibits a high resistance ($R_{MTJ}=R_H$). The logic value '0' is associated with the parallel state and the logic value '1' is associated with the anti-parallel state (see Fig. 1). The TMR ratio is therefore defined as: $TMR= (R_H - R_L)/R_L$.

Without loss of generality, the proposed block reliability estimation methodology is described for a 1T-1MTJ STT-MRAM, the smallest STT-MRAM topology. In this topology, the access to the MTJ element is done through an access nMOS transistor (Fig. 2a).

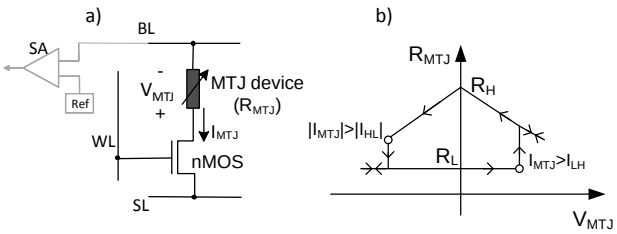


**Figure 2**: 1T1MTJ STT-MRAM Cell: a) the electrical model; b) Piecewise linear model of $R_{MTJ} - V_{MTJ}$ hysteresis characteristic

The voltage-resistance dependence of the MTJ device exhibits a hysteresis behavior [20], as shown in Fig. 2b).

## III. STT-MRAM BLOCK RELIABILITY ESTIMATION

An accurate quantification of STT-MRAM based memory array failure probability under process variability and aging effects could render designers able to leverage ad- hoc system-level fault tolerance strategies to meet application dependent reliability targets.

It is well known that the aging of a memory block is strongly dependent on the usage scenario. To quantify this statement in the case of STT-RAM based memory arrays, a block reliability model is hereafter presented.

### A. Block reliability estimation methodology

The model is designed to assess the impact of aging and process variability on the reliability of a memory block given the failure probability of a single cell and the access rate of each word with the assumption that the block is written one word at a time. Moreover, a block is considered failed when one or more bits fail.

Let $N$ be the number of bits in a word and $B$ the number of words in a block. The following assumptions are considered:

- The stress lifetime of the block is measured in block cycles $n_{BC}=B{\cdot}nc$ where $nc$ is determined by the memory access time and indicates the time to access a single cell of the block. The stress lifetime indicates the number of block cycles elapsed before the first failure.
- The block usage is stationary, i.e., word access rates do not change with time.
- The reliability of a single cell after $nc$ access cycles is $R_{cell}(nc)$.
- The aging of the block words is modelled assuming that, the activity spread throughout the memory block is known.
- The access rate ($\gamma_i$) of each word ($w_i$) with $i=1:B$ is a fraction of the block cycle. This access rate coefficient can take values between 0 and 1 (0 means that the $w_i$ word is never accessed, while 1 means that $w_i$ is the only word accessed during the block cycle).

According to the aforementioned assumptions, the reliability of a memory block ($R_{block}$) composed of $B$ words can be evaluated as follows:

$$R_{block}(n_{BC}) = \prod_{i=1}^{B}[R_{cell}(\gamma_i \cdot n_{BC})]^N \qquad (5)$$

where $[R_{cell}(\gamma_i\ n_{BC})]^N$ is the reliability of word $w_i$ after $n_{BC}$ block cycles, $\gamma_i$ is the rate at which the $w_i$ word is accessed, N is the number of bits in a word, and $R_{cell}$ is the cell reliability.

Therefore, given a number of block cycles ($n_{BC}$), the $\gamma_i$ coefficients can be used to perform a fine-grained evaluation of the impact of different usage scenarios on the aging of the memory block under random variability.

Two extreme cases are derived using the proposed mathematical model:

- *maximum localized access* (worst case aging): all access during any block cycle is done on the same

word. In this case, $\gamma_1=1$ and $\gamma_j=0$, with $j=2:B$, hence the expression (5) becomes

$$R_{block}(n_{BC}) = \\ = [R_{cell}(\gamma_1 \cdot n_{BC})]^N \cdot \prod_{j=2}^{B}[R_{cell}(\gamma_j \cdot n_{BC})]^N \quad (6)$$

Since $\gamma_j=0$, the second term of (6) can be replaced as $R_{cell}(\gamma_j \cdot n_{BC}) = R_{cell}(0)$ where $R_{cell}(0)$ is the reliability of the fresh cell. Therefore the reliability of each $w_j$ word can be approximated to be 1, since regardless the actual reliability of the concerned cells they will not affect the block reliability.

- *minimum localized access* (best case aging): all words in the block are equally accessed at the same rate. In this case $\gamma_i=1/B$, the expression (5) thus becomes:

$$R_{block}(n_{BC}) = [R_{cell}\left(\frac{1}{B} \cdot n_{BC}\right)]^{B \cdot N} \quad (7)$$

Different intermediate usage scenarios, between the considered extreme cases, are expected.

### B. Simulation Results

Using the block level reliability estimation methodology, we discuss the reliability of STT-MRAM memory blocks designed with 1T-1MTJ cells with MTJ element characterized by typical nominal $R_L=1k\Omega$ and $R_H=2k\Omega$ values at ambient temperature and write and read access times are *30ns*. The following assumptions are made regarding to variability induced parameter distributions

- The reliability of the cell is obtained by statistically integrating the joint *probability density function* of the electrical parameters of the cell (in this case $R_L$, $R_H$, and $V_{TH}$) after different cumulative stress periods. We use statistical data presented in [22], [23], [24] where above parameters follow normal distributions. The reliability curve obtained in this scenario is in Fig. 3.

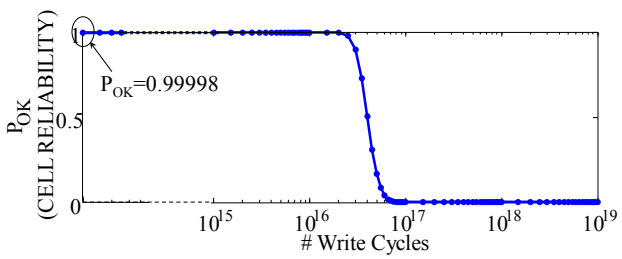


**Figure 3** – STT-RAM cell reliability as a function of the stress cycles under random variability and aging effects for the cell under evaluation

The reliability of the "fresh cell", when no aging is assumed and the cell performance is degraded by fabrication induced variability, is 0.9998. This value is similar to the values reported in literature [26]. Another important observation is that the cell reliability degradation is almost insignificant during a large number of operation cycles (~$10^{16}$ under our assumptions) and then it is fast falling to zero.

The discussion targets the effect of access scenario and block size on the memory reliability.

We start by analyzing the access rate effect on block reliability. For this aim we assume a memory block for which $N=32$ (number of bits in a word) and $B=64$ (number of words in the block).

For illustration and analysis purpose only, we consider 3 intermediate cases, obtained by using 3 access rate distributions of memory usage. The histograms of the 3 distributions, obtained for 2000 blocks, are shown in Fig.4. We assume that the same access rate be maintained over a large number of block cycles (in our case $10^{19}$ block cycles). The access rate histograms for the extreme cases are also included in Fig. 4 (the green and red bars).

The block reliability for the 5 cases (3 intermediate and 2 extreme) has been evaluated, and the results are plotted in Fig. 5. As expected, the usage scenario that guarantees the longest life span is when all words in the block are equally accessed, while the shortest lifespan is obtained when all access is concentrated on one word of the block.

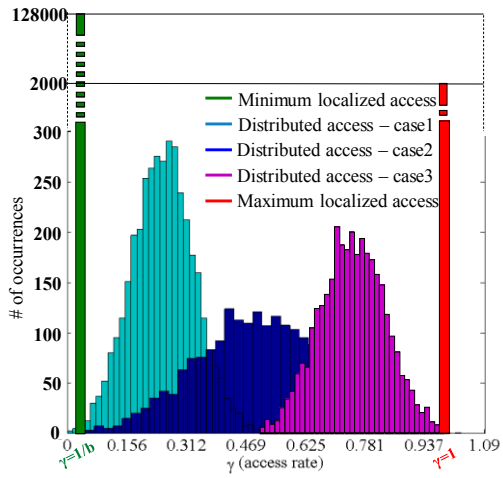


**Figure 4** – Histograms of the access rate distributions

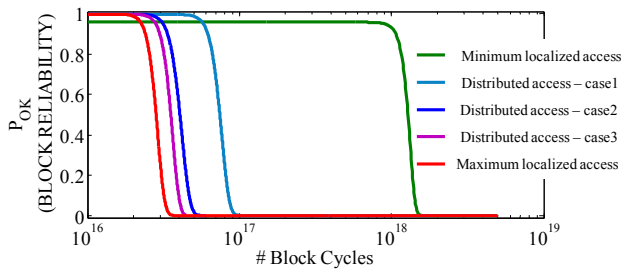


**Figure 5** – Block reliability assuming different access rates (for a block size of 256B).

It should be noted that, by controlling the rate at which a memory block is accessed, the lifespan of the block can be significantly increased. In our particular case, the block lifespan is almost 2 orders of magnitude larger under the minimum localized access scenario when comparing the maximum localized access scenario. Another observation analyzing the results is that, regardless the memory access rate, the block reliability curves follow the same trend as the cell reliability curve.

Using the proposed methodology, we analyze the effect of block size on memory reliability. For this, we assume 4 block sizes, with the same $N=32$ (number of bits in a word) and

*B=[32 64 128 256]* (number of words in the block). For all blocks, the minimum localized access scenario is assumed (best lifespan). The results are shown in Fig. 6. It should be noted that increasing the block size results in increased lifespan when the same access scenario is assumed. On the other hand, the same conditions lead to reduced reliability ($P_{OK}$). This decrease can be substantial: for instance, in our case study, the reliability of a 'fresh' 1MB block (*B=256*) is *0.8175* while the reliability of a 'fresh' 128B block (*B=32*) is *0.9752*.

To satisfy today's reliability requirements (i.e., a working memory is expected to meet a reliability target of $10^{-18}$) system-level fault tolerance strategies, such as error correcting codes, are required.

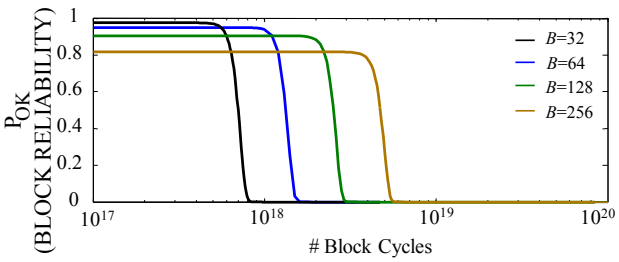


**Figure 6** – Block reliability assuming different block sizes (for minimum localized access scenario) where B is given by the number of 32-bit words in the block.

In the next section, we present an exploration of error correction capabilities as function of code word size to achieve the desired reliability target for the memory under study.

## IV. Discussion on STT-MRAM Block Reliability Improvement

As previously stated, the inherent reliability of STT-MRAM memories is not sufficient to satisfy the reliability targets commonly required in nowadays applications. For instance, considering a typical usage of STT-MRAM as main system memory, the probability of failure has to be below $10^{-18}$ [9]; whereas, for storage memory, the probability of failure has to be below $10^{-13}$ [27]. For this reason, the implementation of mitigation and fault tolerant techniques is required. In this work, we discuss the impact of using Error Correction Codes (ECCs) to improve the reliability of the whole memory system, ensuring that each codeword in a memory block achieves the reliability target and hence data integrity. The choice of the most suitable error correcting scheme depends on the target application. For this reason, practical ECC solutions are typically market segment-specific and range from derivatives of the Hamming code [28] to the BCH [29] or the Reed-Solomon code [30].

The choice of the most suitable ECC technique depends on several parameters (e.g., code complexity, latency, code word size). The proper correction capability is crucial for determining the reliability and the performance of the whole STT-MRAM memory.

For this reason, we define the codeword probability of failure when ECCs are used, to correlate the desired reliability target with the number of errors the code is able to correct. We assume that the failure probabilities of all bits in a codeword are known. The failure probability of an N-bit codeword ($P_{word}$) is defined as the probability to have more than *t* errors in the codeword. This probability is computed using the joint probability of failure of the bits in the codeword. Without loss of generality we assume statistical independence:

$$P_{word}(errors > t) = \sum_{i=t+1}^{N} \binom{N}{i} \cdot p_{cell}^{i} \cdot (1 - p_{cell})^{N-i} \qquad (8)$$

where *t* is the correction capability of the ECC, N the word size, and $p_{cell}=1-R_{cell}$ represents the probability that a single cell fails.

Nevertheless, the error correction capability *t* is not the only parameter to be taken into account when designing the most suitable ECC for a target application. Codeword size must be considered as well, since it strongly impacts the latency of memory operations and the amount of code bits required by the ECC.

Figure 11 shows the boundaries given by (8) between codeword sizes and ECC correction capabilities w.r.t. different target reliabilities. Each curve, obtained by interpolation, represents a reliability contour (more precisely its logarithm to base 10) computed by means of (8), where the considered $p_{cell}$ value is $2 \cdot 10^{-4}$ according to Figure 3. An important fact to be considered is that the values in this plane are discreet, since the error correction capability is an integer and codeword size is usually a power of 2: $2^n$, with *n* an integer.

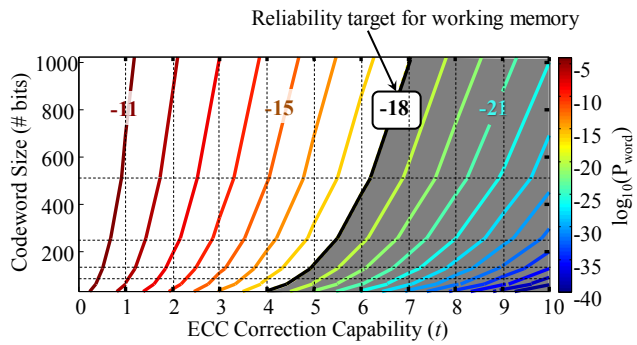


**Figure 7** – ECC design space; shaded area represents the combination of ECC parameters required to achieve the reliability target

A small codeword size makes it difficult to handle high concentrations of errors and require a high number of code bits and higher hardware complexity, whereas the impact on the latency of memory operations is minimized. Larger codeword sizes, instead, better handle higher concentrations of errors, providing more protection using fewer code bits, while increasing the latency of memory access.

It is worth noticing that the same reliability target can be achieved with different combinations of these parameters. For instance, let's assume the reliability target is $10^{-18}$ (black line in Fig. 7), typical requirement when the STT-MRAM is used as working memory. In this specific case, ECCs with the capability to correct 5 errors on a 128-bits codeword or 7 errors on a 1024-bits codeword may be equally used to achieve such a reliability target. Anyway, considering a standard 32-bit memory interface, in the first case the system requires 4 words be read at once to apply the ECC schema, whereas in the latter case 32 words are required. In the second case reading more words than needed could exacerbate aging effects as a word could be accessed many times before being

actually used. Therefore cache memory architecture must be properly designed to mitigate this problem.

More generally, the reliability target will be satisfied by using any combination of ECC parameters (with the restrictions that the code capability is an integer, and codeword size is a power of 2) in the shaded area in Fig. 7. Cache and main memories are typically expected to reach high performances by resorting to cost-effective solutions. In this case, the required ECC should work on smaller blocks with a consequent lower impact in terms of latency. On the contrary, if STT-MRAM memories as secondary storage device are targeted, the current trend is to enlarge the block size over which ECC operations are performed, to handle a higher number of errors minimizing the portion of the memory required to store the code bits.

So far, we have shown that using the proposed methodology, by properly choosing the parameters of error correcting codes, a desired codeword reliability target can be achieved. Also, in the previous section, we have used the methodology to show that the memory lifespan varies significantly depending on the memory block size and the access rate scenario.

In continuation, we show how the proposed methodology can be used to optimize memory block size and error correction capability in order to simultaneously achieve desired memory reliability and lifespan targets. For this, several steps have to be followed.

### A. Application Example

Let's assume that the ECC most suited for our application is the one with the capability to correct 6 errors in a 256-bit codeword (yellow mark on Fig. 8a). The block reliability is evaluated for different memory block size and access rate scenarios. For sake of simplicity, and illustration purpose only, we focus this discussion on a single access rate scenario (the *minimum localized access*). The block reliability is evaluated using a modified version of (5):

$$R_{block}(n_{BC}) = \prod_{i=1}^{B}[1 - P_{word}(\gamma_i \cdot n_{BC})]^B \qquad (9)$$

where $P_{word}(\gamma_i \cdot n_{BC})$ is the metric in (8) obtained for a $t$ error correction capability (6 in our example) on a N-bit codeword (256-bit in our example) accessed at a rate $\gamma_i$ after $n_{BC}$ block cycles; $B$ is the number of codewords in the memory block. The values of $P_{word}(\gamma_i \cdot n_{BC})$ are obtained by using $p_{cell}(\gamma_i \cdot n_{BC})=1-R_{cell}(\gamma_i \cdot n_{BC})$ and $R_{cell}(\gamma_i \cdot n_{BC})$ is the cell reliability after time $\gamma_i \cdot n_{BC}$ and its value is obtained from the data in Fig 3.

Eq. (9) is evaluated for different codeword sizes and memory block sizes. From the obtained reliability curves (similar to the ones shown in Fig 10), the lifespan of the memory block ($B_{life}$) is evaluated as the number of block cycles after which the memory reliability drops to 99% from its 'fresh' value:

$$B_{life} = n_{BC} \mid R_{block}(n_{BC}) = 0.99 \cdot R_{block}(0) \qquad (10)$$

The lifespan of the memory block with different block size and codeword size (assuming the minimum localized access scenario) is depicted in Fig. 8b). Here, each dotted line represents a specific lifespan contour (more precisely, its logarithm to base 10). A target is imposed for memory block lifespan and the region for which this target is achieved is identified (shaded in Fig. 8b).

This is just an example of how the presented methodology can be used. Depending on the specific restrictions, a user can modify the targets and/or size constraints to achieve the desired STT-MRAM memory specifications.

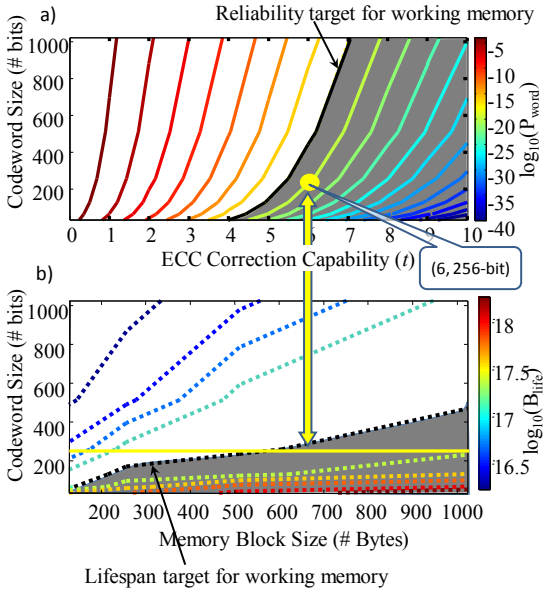


**Figure 8** –a) ECC design space b) memory block design space; shaded areas represent the regions in the design spaces where the targets are achieved.

## V. Conclusions

In this paper, we provided a methodology for predicting the reliability of an STT-MRAM based memory designed with cells of high thermal stability. The reliability estimation is performed at block level.

The memory reliability at block level is estimated for different block sizes and access rates. It has been shown that carefully controlling the rate at which a memory word is accessed, the lifespan of the entire memory block can be substantially increased. For our case study we have observed a block lifespan increase of 2 orders of magnitude when comparing maximum localized access with minimum localized access scenarios. Also, we have shown that the larger the block size, the longer its lifespan, but with continuously decreasing reliability.

As an application of the proposed methodology, an exploration of required error correction capabilities as function of code word size to achieve desired reliability target for the memory under study has been performed.

The proposed method is general; it can be used for different STT-RAM topologies, sizes and cell failure distributions. At block level, based on the estimated cell reliability, the method allows for adjusting the block size, the codeword size, and the access rate of the memory under study for target memory reliability.

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