Integrated Circuit Modeling for Noise Susceptibility Prediction in Communication Networks

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Michele Fontana, FlavioG.Canavero, and Richard Perraud

***Abstract*—This paper addresses an integrated circuit (IC) modeling procedure for mixed-signal immunity simulations of communication networks. The procedure is based on a gray-box approach, modeling (IC) ports with a physical circuit and the internal links with a behavioral block. The parameters are estimated from time and frequency domain measurements, allowing accurate and efficient reproduction of nonlinear device switching behaviors. The effectiveness of the modeling process is verified by applying the proposed technique to a controller area network (CAN) transceiver, involved in a direct power injection (DPI) immunity test on a data communication link. The obtained model is successfully implemented in a VHDL-analog mixed-signal (AMS) solver to predict both the functional signals and the RF noise immunity at component level.**

***Index Terms*—CAN transceiver, conducted susceptibility, controller area network (CAN), electromagnetic compatibility (EMC), mixed-signal integrated circuit, RF noise immunity, signal integrity, VHDL-analog mixed-signal (AMS).**

I. Introduction

THE first step required to understand the electromagnetic susceptibility of a complex electronic equipment is to analyze the behavior of its integrated circuits (IC) when affected by disturbances. In particular, the IC electromagnetic immunity is of paramount importance in communication system networks in noisy environments. Today, in automotive, avionic or industrial environments, well-designed network standards are able to provide data integrity and performance requirements of safety critical systems at a reasonable effort. These network-based systems offer a significant weight reduction, lower development cost, and substantial procurement and maintenance savings compared to dedicated communication systems. This is mainly achieved using a network backbone which serves as a shared resource for the communication between multiple modules. Every module communicates using a transceiver as an interface between the local digital information and the signaling through the network. Hence, the performance of the IC transceiver when affected by disturbances is one of the main factors guaranteeing the electromagnetic (EM) immunity of the whole equipment. The IC noise susceptibility needs to be addressed with the IEC direct power injection (DPI) test [1] and an accurate immunity model has to be generated in order to simulate the operation of communication networks for design-phase assessment of signal integrity and electromagnetic compatibility (EMC) problems.

In literature, several susceptibility analyses on IC were carried out. In [2] a time-domain analysis of RF immunity is carried out on a digital circuit using the original IC netlist, which is not always supplied by the manufacturer. A different approach is proposed in [3], where artificial neural networks (ANN) are used to build a frequency-domain susceptibility model of an inverter, based on data acquired through a DPI test. In [4], an accurate immunity model of a voltage regulator is based on surrogates, constructed using ANNs, replacing the real netlist and concealing the IP of the manufacturer. Data are collected by means of harmonic balance simulations, allowing to model both the functional and the noisy behavior of the nonlinear circuit in the frequency domain. Another frequency-domain model is described in [5], where a local interconnect network (LIN) transceiver is modeled according to integrated continuous improvement methodology [6], based on S-parameters with an IC port linearity assumption.

In order to evaluate the IC noise susceptibility in communication networks, the functional behavior has to be assessed in time-domain, since immunity criteria are often defined as deviation from standard signal timing [7]. Furthermore, during a data transmission a transceiver displays a digital switching behavior between high and low logic states, nonlinearly varying its electrical characteristics. Taking into account these features, this paper proposes a modeling framework based on an analog mixed-signal (AMS) block structure for the generation of immunity models of transceivers from real measured data, aiming at reproducing the nonlinear electrical behavior of switching device ports and simulating noise injection on a bus network in time-domain. The step-by-step modeling procedure and the setup required to collect the responses for parameter estimation from time and frequency domain measurements are thoroughly described.

A controller area network (CAN) transceiver [8] was chosen as device under test. Since generally no transistor-level models are publicly supplied by the IC manufacturer, the model parameters have to be extracted from measurements or taken from the datasheet. Furthermore, to the authors best knowledge, the behavioral models available in literature are inadequate to account for the IC susceptibility to RF noise. Several mixed-mode models of a CAN transceiver were developed to evaluate complex network topologies, signal integrity [9], transceiver finite state behavior, CAN network fault analyses [10], and verification of internal vehicle networks [11]. An analysis of the ESD diodes impact on differential signaling was carried out in [12], when sinusoidal noise is injected in an automotive network. However, the growing complexity of CAN networks operating in a noisy

M. Fontana and F. G. Canavero are with the Dipartimento di Elettronica, Politecnico di Torino, 10129 Torino, Italy (e-mail: michele.fontana@polito.it; flavio.canavero@polito.it).

R. Perraud is with the Airbus Group Innovations, 92152 Suresnes, France (e-mail: richard.perraud@eads.net).

environment demands for a refinement of transceiver models, including noise immunity features; nonidealities on transmitter/receiver differential signaling have to be included in the model to correctly evaluate noise effects on the CAN communication system. It is relevant to remark that the outlined procedure is not restricted to CAN transceivers, but may be applied to any IC used in a communication network, as different automotive or avionic transceivers such as MOST, LIN, or Flexray can be modeled taking into account their susceptibility to RF or transient noise.

The paper is organized as follows. Section II summarizes the procedure for noise immunity measurements on CAN networks. Section III introduces the proposed AMS model for a generic transceiver and it provides the details of the measurement procedure in order to estimate model parameters. Section IV validates the proposed model simulating transient analog waveforms and digital signals on a CAN network where RF noise is injected. Finally, in Section VI an immunity simulation at component level is carried out predicting the resulting immunity graph of a DPI test.

II. EMC Evaluation of CAN Transceivers

CAN is a network protocol that allows multiple processors in a system to communicate efficiently with each other, using high-speed analog circuit techniques to provide data transfers up to 1 Mbps. CAN is a multimaster network where any network node can act as transmitter or receiver, sending messages through a serial bus. Every CAN node includes a CAN transceiver, whose task is to implement the physical layer specifications [13], transforming a digital signal into the physical bus waveforms and vice versa. CAN bus is highly immune to electromagnetic interference due to the differential nature of the transmission; in fact, both bus lines are equally affected by the noise, thus leaving the differential signal unaffected. However, nonidealities of the transceiver and asymmetries in bus topology may affect ideal differential signaling and, therefore, noise immunity. The operation of CAN transceivers can be affected by electromagnetic interference because cables that connect network nodes behave like unintentional antennas, so that the signals at CAN ports are affected by conducted interferences leading to potential failures.

In order to investigate noise effects, an immunity analysis to conducted disturbances is carried over according to IEC/TS 62228 test method [7]; the test standard is used as a standardized common scale for EMC evaluation of CAN transceivers, where failures can be analyzed by means of the IEC 62132-4 DPI test method [1], directly injecting an RF disturbance into the CAN ports and characterizing the susceptibility in terms of the incident power of the EM disturbance causing the failure.

To test the EMC behavior of a transceiver, a simple CAN network consisting of two powered nodes is used, as shown in Fig. 1, where a communication test function is run and analog and digital port signals are observed to verify send-and-receive functionality and to detect any errors. The bus central termination consists of a resistor $R = 60\ \Omega$ to comply with CAN physical layer specification [13], while the cable length is kept as short as possible to minimize the propagation delay between

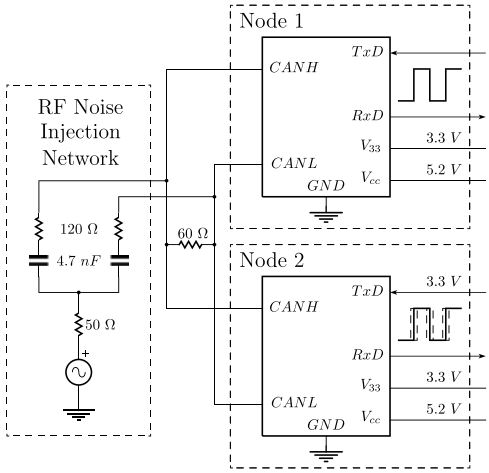

Fig. 1. Schematic view of DPI test for evaluation of transceiver susceptibility to RF disturbances in CAN networks.

transceivers. The disturbance source is constituted by a RF continuous wave signal generator with an output impedance of $50\,\Omega$ and interferences are injected in the network with a pair of RC-serial circuits ($R = 120\,\Omega$, $C = 4.7$ nF) which symmetrically couples the RF signal on CAN ports as common-mode noise.

With reference to Fig. 1, Node 1 operates as a transmitter for a bit pattern, which simulates a CAN message to be received and monitored at the RxD output ports of all nodes in the configured network. A test communication signal with 0-1-0-1 data alternation is sent to Node 1 TxD port, with a bit rate equal to 1 Mbps ($T_{\mathrm{Bit}} = 1\ \mu$s), equivalent to a square wave signal with a frequency of 500 kHz, the maximum possible bit rate on a CAN network. To determine the immunity of the transceiver against RF narrow-band disturbances for single frequencies in the 1 MHz-1 GHz bandwidth, disturbances are injected in the network increasing the noise power level up to 36 dBm until a fault is detected. Although the noise power level is defined by the forward power generated by the disturbance source [1], only a fraction of it is transferred to the transceiver, depending on the IC port impedances at the corresponding noise frequency. As a fault criterion for immunity evaluation, the maximum voltage variation on the RxD signal of every transceiver is checked: if a voltage variation equal or higher than 0.9 V is detected, a glitch occurred and an error event for this test is recorded. The bit period T_{Bit} is also monitored: a time variation equal or higher than $10\%\ T_{\mathrm{Bit}}$ (0.1 μs) fulfills the susceptibility criterion.

III. IC Modeling Procedure

The proposed approach to the modeling of active devices is via simplified equivalent circuit representations, in which the information on the internal structure of the device is used to derive a simplified equivalent circuit for each analog I/O port. The equivalent circuit is composed of various blocks, accounting for specific static or dynamic effects and delays between digital ports. The model is developed to be used in time-domain simulation, as the I/O ports of ICs are highly nonlinear and the electrical properties are linked to their switching behavior. Furthermore, the immunity criteria for communication networks

are defined on time-domain signals, looking at failures related to glitches and jitter [7], that make a purely frequency-domain approach clearly unsuitable.

The models are implemented in VHDL-AMS language [14], as it provides both continuous-time and event-driven modeling semantics, particularly well suited for verification of mixed-signal IC.

The IC modeling procedure can be divided into four steps described in the following sections:

1) *Block structure identification:* identify components of critical circuit blocks for each port and internal connections from datasheet to model nonlinear logic state switching structure.
2) *Logic state static characterization:* evaluate DC port *I-V* characteristics for every logic state to fit component parameters.
3) *Port parasitic element evaluation:* estimate *LC* parasitic elements in port circuit blocks from frequency-domain impedance measurements.
4) *Internal block behavioral modeling:* estimate a behavioral model to take into account internal links from IC switching and DPI measurements in time domain.

The procedure is validated on the TLE6250GV33 CAN transceiver [15], whose evaluation procedure of noise immunity was described in the previous section. The developed model must be able to estimate analog noise effects on CAN transceiver ports according to its logic state and evaluate noise impact on digital output in time domain according to IEC immunity criteria [7]. The presented CAN transceiver model can be used for immunity testing at frequencies up to 300 MHz, as explained in the next sections.

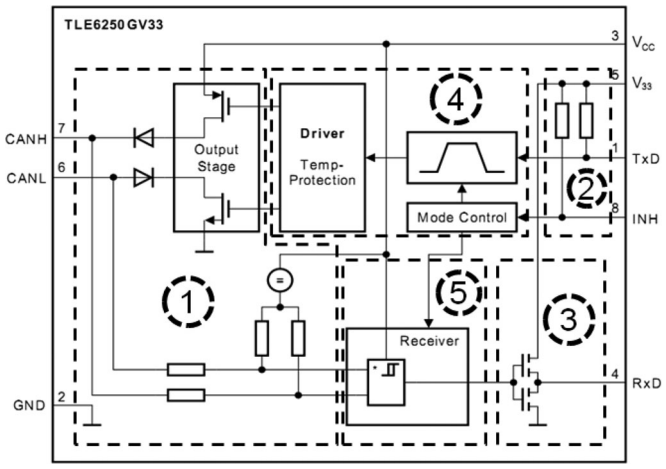

Fig. 2. Transceiver TLE6250GV33 block structure [15].

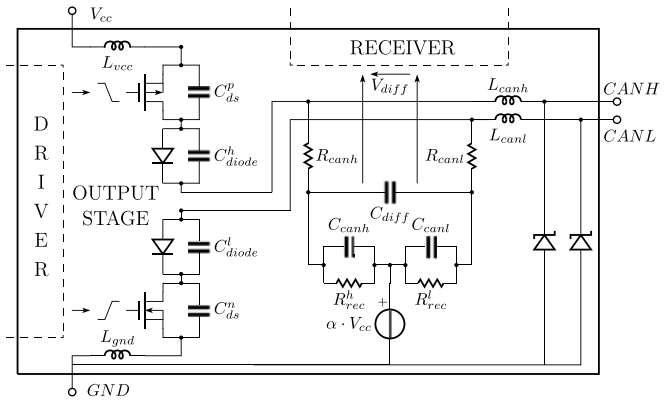

Fig. 3. TLE6250GV33 output stage block schematic.

A. Block Structure Identification

The first step of the modeling procedure is to identify the critical ports for the immunity behavior of the IC. In a CAN communication system, disturbances are typically injected on the bus network or through power supply, therefore in VHDL-AMS modeling environment the transceiver ports that could be affected by noise are modeled as analog ports, while other pins carrying control signals for the IC can be defined as digital ports. A block circuit library is created to describe the IC behavior; the blocks can be divided in two types:

1) *Port circuit block:* it physically describes the electrical connection between the corresponding analog I/O port and the local ground and power supply pins. It is composed only by analog linear (resistors, capacitors, inductors) and nonlinear circuit elements (transistors, diodes, TVS), whose behavior is described by their relevant physical equations and their relevant parameters [16]. The port schematic is usually taken from the IC datasheet or from literature; it has to be able to describe the port impedance in every IC logic state and any nonlinear effect in order to correctly assess the noise coupling in a system-level EM analysis.
2) *Internal connection block:* it describes the IC inner structure and the link between different I/O ports. The characterization of the internal switching structure is done using a behavioral model, as the physical structure of the IC logic core is protected by intellectual property of the producer and not disclosed. The block is composed of AMS elements, such as comparators, filters, and digital delays, and it has to model the internal propagation delay between different I/O ports. Features like the input signal setup time and the voltage threshold have to be taken into account to correctly assess the switching behavior in presence of a noisy signal.

For the TLE6250GV33 CAN transceiver chosen as a reference, the block diagram of the AMS model is depicted in Fig. 2 and is inspired from the device datasheet [15]. Ground (GND), power supply (VCC, V33), digital I/O (TXD, RXD), and CAN signaling (CANH, CANL) are modeled as analog ports, while control ports connected to external systems (INH) are defined as digital ports. With reference to Fig. 2, the block library includes:

1) *CAN output stage (port circuit block):* it defines the output impedance and takes into account the nonlinear behavior of CAN ports due to the MOS transistors switching between different operating regions. The circuit model shown in Fig. 3 is made of two branches between VCC-CANH and CANL-GND ports, respectively. Each branch

is composed of a diode in series with a MOSFET transistor, of type n-channel and p-channel if connected to VCC and GND ports respectively. The diodes limit the current flowing through the transistor when they are reversely polarized by external signals. Controlled by a signal from the driver, the transistors work as switches set by the transceiver state; for dominant state, they are both turned on and CANH-CANL voltage levels are primarily determined by MOSFET nonlinear equations and corresponding parameters, such as the voltage threshold $V_{\rm th}$ and the transconductance k [16]. On the other hand, in recessive state, both transistors are turned OFF and the voltage level on CAN ports is set by the voltage regulator. This voltage divider is connected to CAN ports through series resistances with a nominal value of $R_{\rm rec} = 20\ \mathrm{k}\Omega$, defining a bias voltage level as a fraction α of power supply, nominally 0.5 VCC. When all CAN transceivers in the network are in recessive state, no current flows through the transistors, hence CANH and CANL port voltages are weakly driven by this block. Two ESD protection diodes are used to protect CANH and CANL from high-voltage transient and discharge to ground any current that could damage the logic core. The nonlinear behavior of diodes and MOSFETs is implemented using basic Shockley and Shichman-Hodges equations [16], respectively. Due to the relatively low number of parameters involved in the equations, the model capability to estimate high-frequency distortion effects has to be validated, as illustrated in Section IV. Furthermore, parasitic elements such as package port inductances ($L_{\rm vcc}$, $L_{\rm gnd}$, $L_{\rm canh}$, $L_{\rm canl}$), diode, MOS drain-source and package capacitances ($C_{\rm diode}$, $C_{\rm ds}$, $C_{\rm can}$, and $C_{\rm diff}$) and recessive state series resistances $R_{\rm can}$ have to be included in the model to define correctly port impedances and switching behavior between states. It is relevant to remark that the output stage block is directly connected to VCC port and, therefore, the transceiver voltage dependency from power supply is integrated in the model electrical equations.

2) *TXD (port circuit block):* it is composed of a pull-up resistor $R_{\rm pull}$ connecting TXD port to VCC, in order to put the transceiver in a recessive state unless a dominant bit is received by the port. Series resistance $R_{\rm TXD}$, package capacitance $C_{\rm TXD}$ and inductance $L_{\rm TXD}$ are added to represent the port impedance.
3) *RXD (port circuit block):* a CMOS output stage, driven by the receiver internal block, connects the RXD output port to GND and VCC. MOSFET drain-source capacitances ($C^n_{\rm RXD}$, $C^p_{\rm RXD}$), series resistance $R_{\rm RXD}$ and package inductance $L_{\rm RXD}$ are added to model the port impedance.
4) *Driver (internal circuit block):* after processing the TXD input waveform through a high-impedance comparator, the block transforms the digital signal to analog waveforms driving gate-source voltage of MOSFET transistors. Several parameters, like the comparator voltage threshold, the rise and fall time of transistor driving signal and asymmetric digital delays between ports and driver, can be set to accurately model transitions between states.

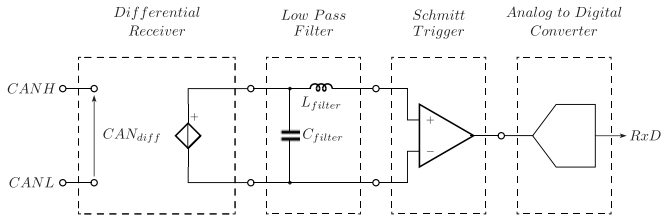

Fig. 4. Receiver block layout.

5) *Receiver (internal circuit block):* the differential analog signal from CANH and CANL ports is processed by the receiver and sent to RxD output port. The receiver is composed of a Schmitt trigger (a comparator with hysteresis), which compares the differential signal with specified voltage levels and sends a digital bit through the transceiver logic core to RxD selecting between recessive and dominant state. In the model shown in Fig. 4, the logic core behavior is modeled as an *LC* circuit filtering the signal before it is processed by the Schmitt trigger; the transceiver internal delay is taken into account by an asymmetrical delay in the A/D block to correctly address signal timing between CAN and RxD ports. The net effect is that the RxD output moves to a new logic state only after the filtered differential signal crosses the voltage thresholds; even if the Schmitt trigger output is prone to spurious switching due to noise from the environment, the filter should suppress high-frequency interferences and fast transient pulses, ensuring that the output swaps only when a state switching actually occurred in the network. As the filter cutoff frequency is set high enough to not affect the functional CAN signal bandwidth and to filter only higher frequencies, the RxD output swap caused by a noisy signal will be influenced by the behavioral filter and a time variation on RxD bit period $T_{\rm Bit}$ will occur, as shown in Section III-D. Instead, if the state switching is determined by a CAN waveform not affected by the filter, the internal delay will be determined only by the asymmetrical delay and by the rise/fall time of the signals driving the RXD block CMOS output stage.

B. Logic State Static Characterization

A first estimation of the port circuit parameters is done by measuring the dc voltage on the relevant pins in every logic state of the IC. Furthermore, dc resistance port values are measured with a multimeter or taken from the IC datasheet. In a real CAN network, a transceiver is connected through a wire stub to the main CAN bus which is terminated by two $120\ \Omega$ resistors at both ends to ensure impedance matching in the transmission line and to minimize reflection effects. Hence, a differential impedance of $60\ \Omega$ is found between CAN ports on every node. The electrical behavior of a transceiver is evaluated by the measurement setup shown in Fig. 5.

During the measurements, a logic signal on the input port drives the IC in high and low logic state while the other ports are loaded in their usual operating conditions defined in [7].

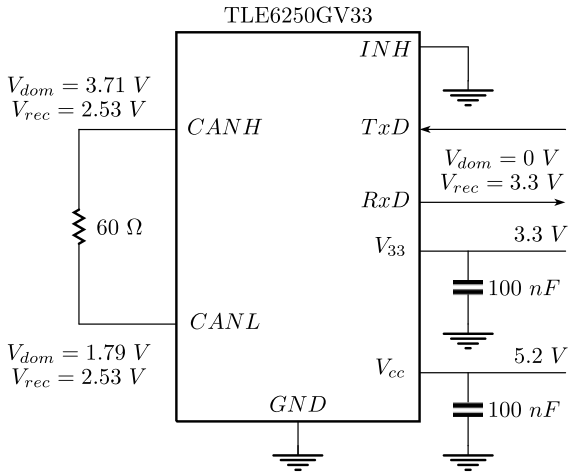

Fig. 5. Transceiver test circuit for static and dynamic behavior with relevant voltage levels in dominant and recessive state.

VCC and V33 ports are supplied with their relevant voltage levels and a 100 nF decoupling capacitor is placed between the supply pin and the ground. RXD digital output port is connected to a high impedance load and the INH control port is grounded [15]. It has to be noted that all measurements are done between the relevant port and the local ground pin, which has to be connected to the global ground of the test setup.

Voltage levels in dominant state on CANH and CANL are used to estimate the parameters of output stage transistors, being in the triode region of operation. In order to calculate the voltage threshold $V_{\rm th}$ and the transconductance k for both MOSFETs, two separate DC voltage measurements are carried out on the CAN pins varying the differential impedance between the ports from 60 Ω to high impedance ($Vth_n = Vth_p = 0.1$ V, $k_n = 7.8$ mA/V^2, $k_p = 9.5$ mA/V^2). When the transceiver is in recessive mode, MOSFETs are in cutoff region, CANH and CANL port are at the same voltage levels and no current flows through the output stage and the 60 Ω resistor; therefore the voltage regulator parameter α can be estimated from recessive voltage levels and found equal to $\alpha = 0.487$, lower than the nominal value of 0.5. Voltage divider resistance values are set to $R^h_{\rm rec} = R^l_{\rm rec} = 20\,{\rm k}\Omega$, while the TXD pull-up resistance is equal to $R_{\rm TXD} = 25\,{\rm k}\,\Omega$.

C. Port Parasitic Element Evaluation

In order to assess in a DPI test the amount of noise power actually transferred to the transceiver, port impedances need to be correctly modeled in both logic states. To extract the port impedance, the component is mounted on a printed circuit board (PCB) with the IC ground pin linked to its solid copper ground plane and a S-parameter measurement is performed with a vector network analyzer (VNA) on the pins to measure the impedance. As the IC ports are loaded with the $50\ \Omega$ VNA input impedance, it performs a small signal measurement testing the behavior of the port circuit around its operating point; therefore the parameters of any nonlinear components have to be characterized in other modeling steps.

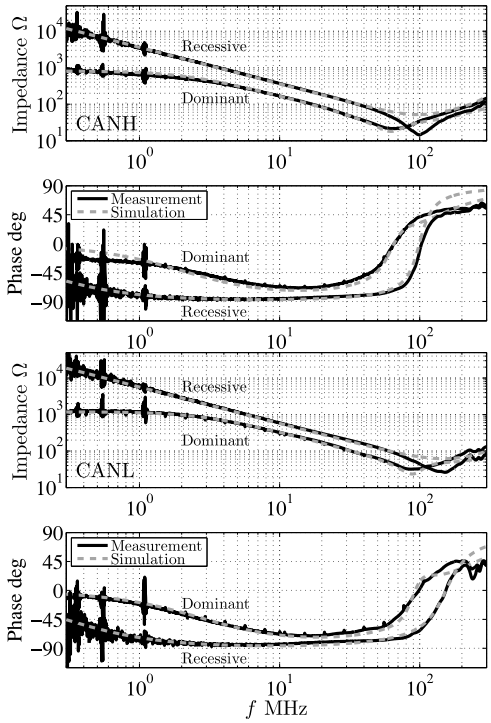

Fig. 6. CANH (top two panels) and CANL (bottom two panels) port impedances in dominant and recessive state. Solid lines: real measurement carried out on the transceiver of Fig. 5; dashed lines: prediction obtained via the equivalent circuit of Fig. 3.

TABLE I
ELEMENT VALUES OF PORT CIRCUIT BLOCKS

Block	Element	Value	Element	Value	Element	Value
CAN	$R^h_{\rm rec}$	20 kΩ	$R^l_{\rm rec}$	20 kΩ	$R_{\rm canh}$	50 Ω
CAN	$R_{\rm canl}$	50 Ω	$C_{\rm canh}$	50 pF	$C_{\rm canl}$	25 pF
CAN	$L_{\rm canh}$	40 nH	$L_{\rm canl}$	40 nH	$L_{\rm vcc}$	40 nH
CAN	$L_{\rm gnd}$	40 nH	$C_{\rm diff}$	5 pF	$C^p_{\rm ds}$	20 pF
CAN	$C^n_{\rm ds}$	10 pF	$C^h_{\rm diode}$	50 pF	$C^l_{\rm diode}$	20 pF
TXD	$C_{\rm TXD}$	10 pF	$L_{\rm TXD}$	20 nH	$R_{\rm TXD}$	20 Ω
RXD	$C^{n-p}_{\rm RXD}$	10 pF	$R_{\rm RXD}$	20 Ω	$L_{\rm RXD}$	20 nH

Fig. 6 shows the impedances seen at CANH and CANL ports, recorded with the transceiver set in dominant and recessive state. Across the bandwidth of the DPI test, the device structure shows a smooth capacitive behavior, up to 80–100 MHz where a parasitic inductive load due to bonding wires and IC frame package is detected. Considering the PCB ground and short traces as ideal, Fig. 6 compares the measurements with the responses of the lumped equivalent circuits of Fig. 3, whose parasitic element values have been estimated via simple fitting and shown in Table I. Impedance curves measured in recessive state are preliminary employed to estimate capacitances and inductances belonging to the voltage regulator block, while parasitic elements of the output stage are determined afterward from dominant state impedance. The measurement procedure is valid to characterize the IC port impedance up to 300 MHz; at higher frequencies the parasitic elements of the PCB and of the SMA connector are no longer negligible, thus requiring to be de-embedded. It

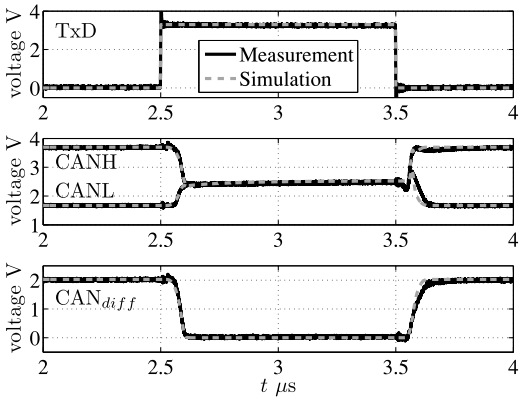

Fig. 7. Port voltage responses (solid black curves) and model predictions (dashed gray curves) of the transceiver state transition driven by 1 Mb/s input signal.

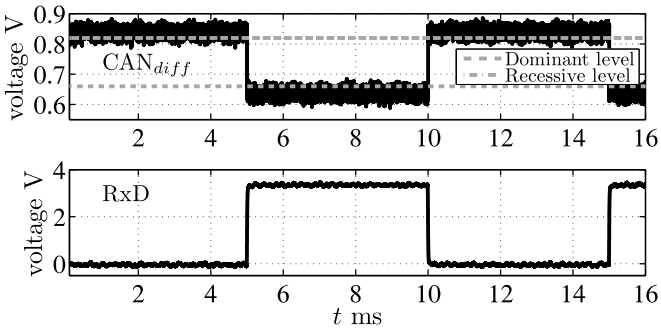

Fig. 8. Square wave differential input signal for voltage level estimation of receiver hysteresis.

is relevant to remark that the parasitic elements detailed in this section and the proposed values of their electrical parameters represent only a good fit of the impedance measurements, as it is not possible to accurately determine the exact values of each component only from external measurements. The uncertainty on parasitic elements could be strongly reduced using informations on the IC provided by the manufacturer, not available as it is covered by Intellectual Property.

D. Internal Block Behavioral Modeling

In a mixed-signal model construction, the interaction between ports has to be correctly assessed. A square wave signal is sent on the input port to estimate the switching voltage thresholds of I/O signals. Then, DPI susceptibility measurements are carried out on the IC signal ports usually affected by noise. The recorded waveforms are used as input for the complete IC model to fit the parameters of the behavioral internal connections.

The measurement setup shown in Fig. 5 is used to verify the proper functionality of the transceiver when state transitions occur, driven by a 1 Mb/s switching digital signal on TxD port. The transceiver internal delay from a TxD digital event to the corresponding CANH and CANL signal change, is evaluated from the measured waveforms shown in Fig. 7; the delay (30–40 ns), the rise and fall time of transistor driving signals (80–90 ns) are taken into account in the model together with the switching voltage threshold on TXD port obtained from the datasheet (2 V, [15]), fitting the driver block parameters and, thus, estimating the transient waveform of MOSFETs gate-source voltages. The good agreement between measurements and simulations confirm that the model properly represents I/O timing and may correctly validate signal integrity for CAN systems operating at the highest bit rate possible.

Since the susceptibility criterion used in the immunity test relies on RxD signal analysis, the characterization of the receiver functionality is of paramount importance to correctly predict noise influence on bus lines. With reference to the receiver block represented in Fig. 4, the differential analog signal from CANH and CANL ports is the input for the Schmitt trigger; recessive-to-dominant and dominant-to-recessive transitions on the bus line are detected on different voltage levels due to the comparator inherent hysteresis. A differential square wave signal is applied to CAN ports and its high and low voltage levels are reduced until glitches and spurious commutations are found on RxD signal in both logic states; a low frequency (100 Hz) signal is preferred, as shown in Fig. 8, to avoid measurement errors from parasitic capacitance discharge during transitions. The receiver characterization is done on a transceiver in recessive state fixed to a "1" logic level on TxD port, as the IC is set in this condition while not transmitting any data on the bus.

Additionally, the low-pass response of the logic core has to be assessed. The receiver behavior affected by sinusoidal noise is evaluated in the DPI test setup shown in Fig. 1. Several faulty transmissions in the CAN network, along with a set of noiseless waveforms, are reported in Fig. 9 with various noise frequency and injected power level; it is worth noting that high power level noise (35 dBm) induces spurious commutations on RxD output in the 1–10 MHz bandwidth, while at higher frequencies only errors due to jitter are detected. The measured waveforms of CAN differential signal are used in simulation as an input for the receiver block model and the resulting simulated RxD output is compared with the measured signal on the RxD port to fit the model parameters. First, the noiseless CAN waveform shown in the top graph of Fig. 9 is used to estimate the receiver block delay (5–10 ns) and the rise and fall time of transistor driving signals (10 ns). Subsequently the noisy CAN signals are used to determine the filter order and the parameters of the behavioral logic core model observing the timing characteristic of the faulty transmissions; a good accuracy level is obtained in simulation environment by modeling the transceiver low-pass behavior as a Bessel second order *LC* filter ($C = 950$ pF, $L = 6276$ nH) with a cutoff frequency of $f_c = 2.5$ MHz.

The implementation of the AMS model in the simulator is shown in Fig. 10, without showing the *LC* parasitic elements for picture readability. The IC ports are linked to the port circuit blocks (TXD, RXD, CAN output stage), while the internal circuit blocks (Driver, Receiver) model the connection between ports components, driving the gate signal of the MOSFET transistors. The schematic is used as a subcircuit in all immunity simulations.

IV. IC Model Validation

The proposed modeling approach is validated on several examples, predicting transient analog waveforms and digital I/O

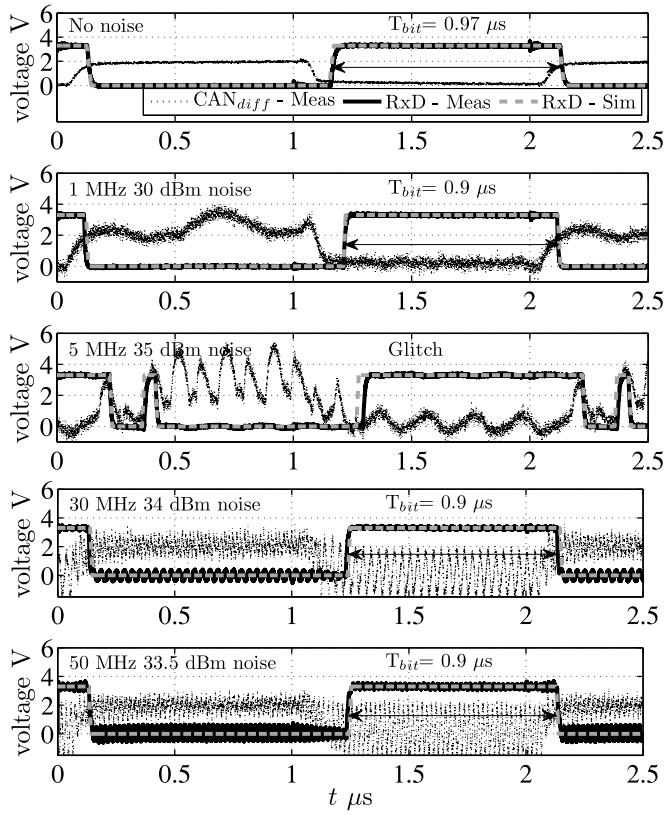

Fig. 9. Noisy CAN port voltages and corresponding digital output signals for receiver characterization; noise frequency and power level corresponding to the susceptibility criterion are indicated in each panel; dotted black lines: measured noisy differential CAN signal; solid black lines: measured RxD signal; dashed grey lines: predicted RxD signal.

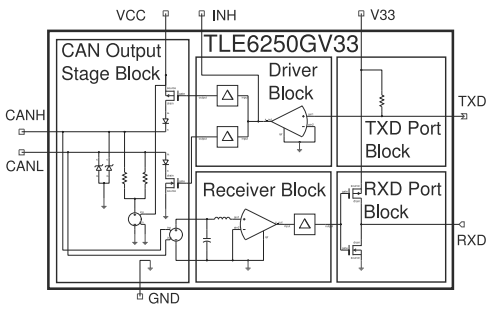

Fig. 10. TLE6250GV33 Transceiver AMS model.

signals of the transceiver affected by common mode RF noise; the DPI test described in Section II is reproduced also in simulation. Measurements are carried out for all examples and the measured signals are used as reference waveforms in the validations.

The first test case is the injection of a RF signal with constant power level (30 dBm) at several frequencies up to 300 MHz, to correctly assess the transfer function between the noise generator and CAN ports, when Node 1 transceiver is on recessive or dominant state. Several waveforms reported in Fig. 11 confirm the capacitive behavior of the port impedances in recessive state, because the sinusoidal amplitude is reduced

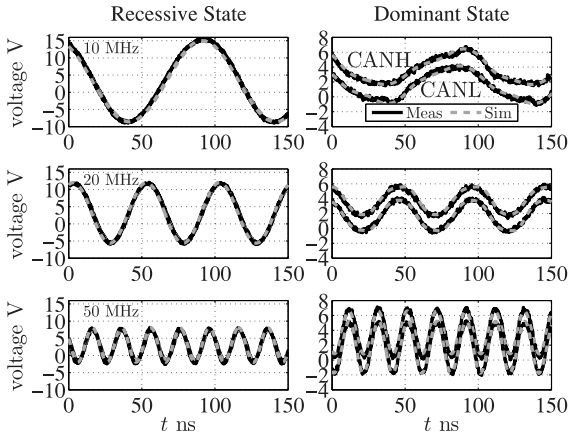

Fig. 11. Noise injection with constant 30 dBm power level on CAN transceiver ports in recessive and dominant state. Solid black lines: reference. Dashed gray lines: prediction.

as the noise frequency increases. On the other hand, in dominant state the noise triggers a nonlinear behavior: varying the voltage amplitude on CAN ports leads to a shift of the transistor operating region, from triode to saturation regime and viceversa, thus producing a distortion of the sinusoidal waveforms. The proposed model is able to handle the nonlinear effects caused by RF noise when the transceiver is in dominant state, as shown in Fig. 11, thus validating the noise injection simulations in the whole frequency bandwidth.

The second test case is the simulation of a complete DPI test on the transceiver at a single frequency. A 1 Mbps CAN communication between nodes is stressed injecting RF noise at 5 MHz. The resulting waveforms are shown in Fig. 12, and a 27.5 dBm noise power is required to record a failure on RxD signal. The asymmetries deriving from nonidealities of the CAN ports are correctly assessed in simulation, since the common mode noise is not symmetrically coupled to both bus lines. This asymmetry slightly influences the differential signal and modifies the transitions between bus states. Hence, a square wave signal transmitted over the network is seen by the receiver with a modified duty cycle, since the dominant state period lasts longer than the recessive one; this behavior leads to a digital output signal affected by jitter, whose amplitude can give rise to system susceptibility, according to [7]. The good agreement of the reported curves confirms the model capability to describe RF noise effects on the transceiver and highlights the importance of taking into account the complex relation between the noisy differential signal and the digital output. The simulation time required to obtain these waveforms is 6.2 s, proving a good computational efficiency.

V. Immunity Simulation at Component Level

As an application example, the TLE6250GV33 transceiver immunity model is used to reproduce a real DPI test at component level. Time-domain simulations are carried out for the schematic shown in Fig. 1 to generate an immunity graph according to the test procedure defined in [7]. As a test of the

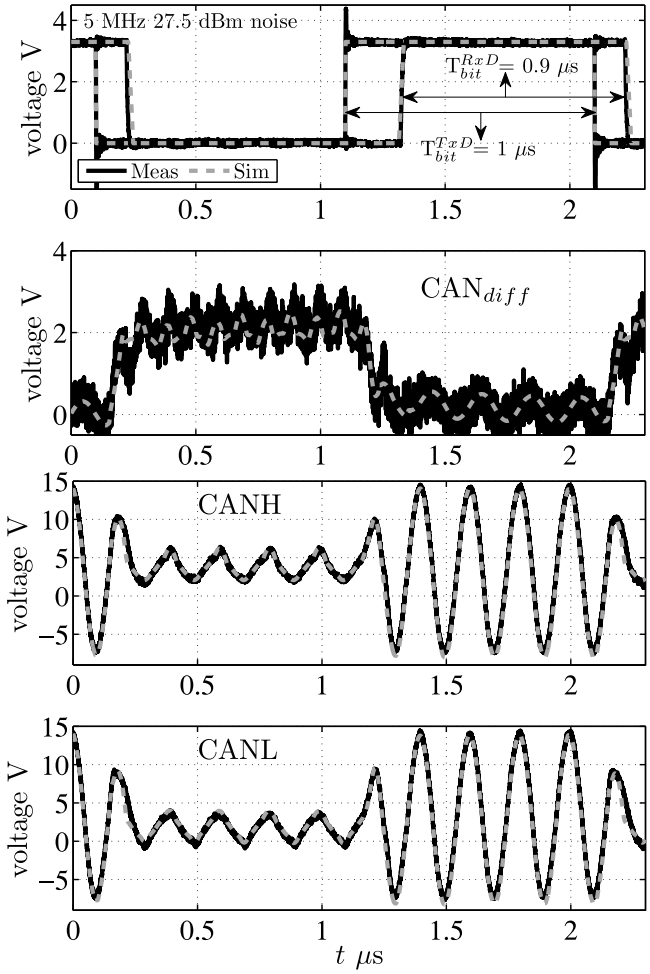

Fig. 12. Node 1 TxD and Node 2 RxD digital signals and analog CAN waveforms for the network depicted in Fig. 1, with 5 MHz noise injection; solid black lines: reference; dashed gray lines: prediction.

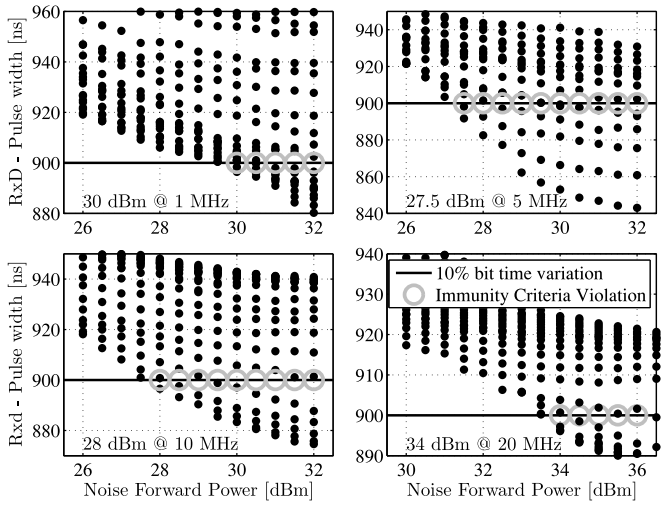

Fig. 13. Pulse width jitter of the Node 2 RxD signal, as obtained in DPI simulation of a TLE6250GV33 transceiver for different noise frequencies, power level and phase.

communication channel, a 1 Mbps signal with a 0-1-0-1 pattern was sent from the Node 1 TxD port. For each frequency point starting from 1 MHz onwards, disturbances are injected in the network increasing the noise power level up to 36 dBm; the RXD signal of Node 2 is monitored until a fault is detected according to the susceptibility criteria (glitches or 10% jitter). The parameters of the RF noise source are varied in the DPI circuit to obtain a complete immunity graph, therefore time-domain simulations are run in three nested loops:

1) *Noise frequency:* the RF frequency of the noise source is the parameter varied in the outer loop, in order to scan the whole frequency bandwidth required by the immunity test.
2) *Noise amplitude:* in the middle loop the forward noise power is set to a value (20 dBm) low enough to not cause any immunity criteria violation in the whole bandwidth. The noise power level is then increased in steps of 0.5 dB until a fault is found on the monitored signal. In simulation, the RF noise forward power has to be converted to an open-circuit peak value of the RF voltage source according to the following equation:

$$V_{\mathrm{RF}} = 2\sqrt{2 * 10^{\left(\frac{P_{dBm}-30}{10}\right)} * 50.}$$

3) *Noise phase:* the last parameter to be set in the inner loop is the phase of the RF noise. While the transceiver transmits data at 1 Mbps during the DPI test, the CAN ports vary their impedance depending on the logic state; thus in time domain the peak of the sinusoidal noise waveform can be coupled with the transceivers during a transition or in dominant or recessive state. In a real measurement, the noise phase is randomly generated by the voltage source and every possible combination of RF phase and transceiver state is evaluated by running the test for the 1-s dwell time specified in [7]. However, in simulation this condition is not true, therefore several simulations haves to be run varying the phase angle between 0 and 360°.

The simulation results of the DPI test on the TLE6250GV33 transceiver are shown in Fig. 13. On each graph the pulse width of the positive bit of the node 2 RxD signal is plotted with the corresponding RF noise power: an immunity criteria violation is found when the pulse width is lower than 900 ns, as the node 1 TxD input signal has a $T_{\mathrm{Bit}} = 1$ μs and therefore a 10% variation is detected. The effect of the noise phase on the test results can be clearly seen as different pulse width values are recorded for the same noise frequency and power. The lowest noise power value provoking a failure is then recorded for each frequency as the minimum level required to fail the immunity test. To obtain a jitter simulation graph, a number of 340 time-domain simulations are run for a single frequency, varying noise power and phase at each step by 0.5 dBm and 18°, respectively; the total simulation time is about 25 minutes.

The results are then collected into the immunity graph shown in Fig. 14 demonstrating an excellent agreement between the data obtained by measurements and the simulated immunity model. At 1 MHz, the IC withstands 30.5 dBm and still operates

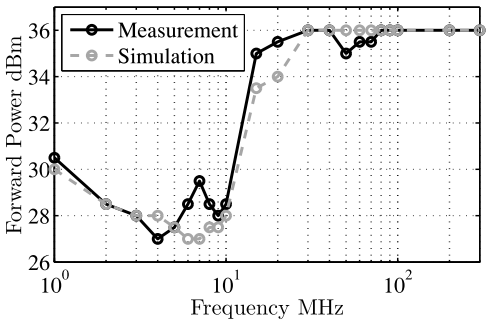

Fig. 14. TLE6250GV33 transceiver immunity graph: measurement and prediction.

correctly, while the model returns 30 dBm as a maximal acceptable value of the RF noise power. For the frequency range from 2 MHz until 10 MHz this value decreases according to both setups, with a maximum error of 2.5 dB at 7 MHz between the two curves. Between 10 and 80 MHz, the IC is clearly more immune to interferences and it fully passes the DPI test on frequencies up to 300 MHz, being able to tolerate a noise power level of 36 dBm both in measurement and simulation. The test simulation time is about 10 h on a common laptop, which is deemed an acceptable time for industrial needs.

The precision of the virtual susceptibility test results depends on how accurate the state-switching port impedance and the circuit internal connection are modeled. While the former factor can be easily assessed by direct measurements, the latter element can only be estimated by indirect means and its behavior is clearly dominated by nonlinear analog and digital elements; therefore, the use of proposed behavioral model avoids the difficulty to determine the physical behavior of the internal link, leading to a maximum error of 2.5 dB at 7 MHz. A more accurate physical model, built using informations covered by Intellectual Property, should reduce the error magnitude.

The modeling procedure detailed in the paper provides a solid framework that can be exploited to address noise immunity problems requiring a time-domain analysis. While collecting the required data could be challenging compared to modeling procedures based on frequency-domain approach [3]–[5], the model flexibility allows to consider both strong analog nonlinearities and state switching behaviors often found in digital ICs. Furthermore, the immunity graph of the measured DPI test is not employed in the modeling procedure and only used as a reference to validate the simulated immunity curve. If the IC immunity criterion is modified for industrial needs, the model is still valid and can be used to estimate an immunity curve according to the new susceptibility functions.

VI. Conclusion and Future Work

An IC modeling procedure is proposed for mixed-signal immunity simulations of communication networks. The procedure is based on the use of schematic blocks, whose parameters are estimated from time and frequency domain measurements, allowing accurate and efficient reproduction of port circuits and IC internal links. A representative test case of a CAN transceiver was selected, for which the model construction parameters have been calculated and optimal settings have been selected ensuring high precision and efficiency. The model was integrated into an AMS circuit simulator and its immunity behavior was correctly predicted at component level, confirming the effectiveness of the modeling process. The obtained models may handle RF noise up to 300 MHz and can adequately reproduce the noise effects on both analog and digital signals for SI and EMC investigations.

As the immunity model described in this paper is based on a time-domain modeling approach, it could be theoretically extented to simulate the transient noise impact on a IC. Regarding the CAN transceiver AMS model previously detailed, ESD protection diodes have to be characterized and included in the IC model for immunity prediction toward transient noise. The *I-V* diode characteristic can be extracted with a transmission line pulse measurement carried out on the CANH and CANL ports [17]. The ESD protection diode model are usually implemented in VHDL-AMS using a behavioral formulation based on a state machine model [18], where each operating region is associated with an equation reproducing the measured *I-V* curve. Thus, the measurement setup to test transient noise on a IC could bd reproduced in a virtual environment and immunity test results can be extracted from simulations. The feasibility of this approach to model the transient noise impact on a IC is a topic for future study.

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