# POLITECNICO DI TORINO


# Oxide Memristive Devices

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# Abstract

Resistive switching in metal oxide materials has recently renewed the interest of many researchers due to the many application in non-volatile memory and neuromorphic computing. A memristor or a memristive device in general, is a device behaving as nonlinear resistor with memory which depends on the amount of charges that passes through it. A novel idea of combining the physical resistive switching phenomenon and the circuit-theoretic formalism of memristors was proposed in 2008. The physical mechanism on how resistive switching occurs is still under debate. A physical understanding of the switching phenomenon is of much importance in order to tailor specific properties for memory applications. To investigate the resistive switching in oxide materials, memristive devices were fabricated starting from materials processing: low-pressure chemical vapor deposition of ZnO nanowires (NWs), low-temperature atomic layer deposition (ALD) of $TiO_2$ thin films and micro-pulse ALD of $Fe_2O_3$ thin films. The distinct geometry of ZnO NWs makes it possible to investigate the effect of the electrode material, surface states and compliance to the memristive properties. A simpler method of fabricating $TiO_2$-based devices was explored using low-temperature atomic layer deposition. This approach is very promising for device application using photoresist and polymeric substrates without thermal degradation during and after device fabrication. ALD of pure phase $Fe_2O_3$ thin films was demonstrated using cyclic micro-pulses. Based on the performance of the fabricated devices, the oxide materials under this study have promising properties for the next-generation memory devices.

# Summary

This dissertation is organized as follows:

- **CHAPTER 1**. This chapter provides an overview in the field of memristor and memristive devices. A background on the circuit-theoretic and recent development in device application are given. A survey of different memristive materials is discussed in detail. The current state-of-the-art technology and application of memristors is also given emphasis.
- **CHAPTER 2**. This chapter focuses on the methodology and materials processing techniques utilized in this study. Emphasis is given in science behind low-pressure chemical vapor deposition (LPCVD) and atomic layer deposition (ALD) techniques.
- **CHAPTER 3**. This chapter presents all the oxide materials and device characterization. Results showing the effect of interface layer in ZnO NWs memristive behavior are discussed. Results of low-temperature ALD and fabrication of $TiO_2$ thin film devices are also tackled. Finally, results of micro-pulse ALD and fabrication of $Fe_2O_3$ thin film devices are presented.
- **CHAPTER 4**. Summary and conclusion are given based on the results presented. Suggestions regarding future development in the materials processing and device characterization aspect are also presented.

# Table of Contents

# 1. Review

This Chapter will discuss the concept of memristor and the recent advances in the study of memristive materials and devices. Details about the circuit-theoretic formulation of memristor and the physics of memristive switching in various materials and devices will be presented.

## 1.1. Background

System complexity in biological systems, memory networks and learning processes are observed to possess brain-like features. This poses a great challenge in terms of emulating neuromorphic processes like pattern recognition, adaptive learning and memory. Neuromorphic system and information processing are two emerging technology trends that require sophisticated microelectronic devices and circuitry for fast, reliable, high-density computing. Downscaling is very important in device fabrication especially now that low dimensional device architecture equates to physical device miniaturization, efficient material resource management and low power consumption.

Different electronic devices offer alternative solution to conventional type of computing including memristors, memristive systems and spintronic devices. The idea of memristor was first theorized by Chua[1] in 1971 in an attempt to find a circuit-theoretic relation between electric charge q and magnetic flux Φ. Memristors and memristive systems offer potential use in neuromorphic processes, learning systems, parallel computing and non-volatile memory devices. The state of the device depends on its current charge history and its memory is retained. Thus, memristor can retain memory even if the power is switched off.

In the vast selection of materials to be used for such applications, metal oxides like ZnO, $TiO_2$ and $Fe_2O_3$ are excellent choices because of abundance, ease of processing and versatility. The recent discovery of the $TiO_2$-based memristor by HP Labs[2] stirs much interest in the field of nanoelectronics. This simple device consists of a switchable insulating layer sandwiched between two metal electrodes. These devices operate through stable switching from high to low resistance states caused by the changes in the filament resistance.

## 1.2. Memristor Fundamental

Basic circuit theory describes passive circuit elements as two-terminal devices that relate fundamental circuit variables – voltage ($v$), current ($i$), charge ($q$) and magnetic flux ($\phi$). Six mathematical relations can be formulated relating two of the four circuit variables. Two relations arise from the concept of current (charge flow) and voltage (electromotive force). Charge is the time integral of current. Conversely, flux is the time integral of voltage. These relations can be written as,

$$dq = i\,dt \tag{1}$$

and

$$d\phi = v\,dt \tag{2}$$

The three equations describing the three basic circuit elements are:

voltage and current relation links with resistance $R$,

$$dv = R\,di \tag{3}$$

charge and voltage relation associates with a capacitor with capacitance $C$,

$$dq = C\,dv \tag{4}$$

and current and flux relation describes an inductor with inductance $L$.

$$d\phi = L\,di \tag{5}$$

The last equation linking flux and charge describes a quantity $M$ with units of resistance.

$$d\phi = M\,dq \tag{6}$$

The memristor equation can be deduced to Ohm's Law when the device response becomes linear. Based on the theoretical formulation, a memristor operates under sinusoidal input wherein the voltage changes with time.

## 1.3. Memristive Devices

There is a remarkable progress in computer and mobile telecommunication in the past decade due to improvement of memory and processor technologies. With the emergence of big data opportunities for industry and research alike, the demand for memory devices increased rapidly. Memory devices can be divided into two groups – non-volatile and volatile memories. The current platform in memory storage mechanism is based on floating gate (flash) devices – charge storage.[3,4] Due to scaling limits encountered by this system, alternative memory storage mechanisms are already being developed.[5–9] The most promising alternatives include ferroelectric switching, magnetic switching, phase-change and resistive switching[10]. Resistive switching has been demonstrated since the late 1960s.[11,12] Band model interpretation of such phenomenon is less applicable as new experimental results indicate high field in localized regions of the device after electroforming.

### 1.3.1. Electroforming

Electrical phenomena in many oxides are described by a nonlinear transport mechanism[13–15] based on the bulk, surface states and oxide-electrode interface. The insulator-conductor transition that occurs prior to obtaining a stable switching has to be surpassed by electroforming. IV measurements show that the device becomes more conductive after the electroforming process. A typical IV measurement is performed by applying electrical stress to the device. In a symmetric device, when a gradually increasing positive voltage is applied to the top electrode, oxygen vacancies drift toward the bottom electrode. This high-field induced charge transport in some cases results to phase transition[16] to a more conductive state of the bulk or in localized regions. For an asymmetric device on the other hand, metallic filaments are also observed to form as ion channels using active electrodes like Ag[17,18] and Cu.[19–21] Either oxygen vacancies or metallic ions forming the conducting filaments are believed to be responsible for the abrupt decrease in resistance of the insulator.

Some issues are encountered during electroforming using voltage bias in particular. As mentioned above, this process can alter the stoichiometry, phase or charge distribution within the insulator. Initial field bias applied to the device is usually higher than the operating field. It is necessary to limit the current or to set a compliance current $I_{cc}$ in

order to prevent irreversible dielectric breakdown. Another approach to completely avoid setting the compliance current is to apply current bias (instead of voltage bias) during electroforming. Nauenheim et al.[22] observed stable transition into the bipolar switching without shifting to a permanent conductive state or unipolar switching mode. Moreover, it is determined that the use of low-level current ($10^{-9}$ A) or low scan rate prevents the cell device from overcharging. Device geometry and operating current are important factors that affect memristive property because they are correlated to the changes in local inhomogeneity during switching. Yanagida et al.[23] investigated the scaling effect of unipolar and bipolar switching in crossbar junction devices. They investigated the transition of non-memory, unipolar and bipolar switching based on device geometry or cell area.

### 1.3.2. Resistance States

The initial resistance of a memristive device called pristine state (PRS) exhibits rectifying behavior. This is because the interface between Pt and Au (typically used as inert electrodes) and most oxides form a Schottky contact.[13] After electroforming, the device exhibits stable resistive switching characterized by two states - high resistance state (HRS or OFF state) to low resistance state (LRS or ON state). When the device switches from HRS to LRS, it is said to have undergone SET process. On the other hand when it switches from LRS to HRS the device it called RESET process. The switching can be bipolar (BRS) or unipolar (URS) depending on the nature of electrical stress and device asymmetry related to fabrication.[5] In the BRS mode, the SET and RESET processes occur on different voltage polarity while in the URS mode the SET and RESET processes occur on the same polarity and the RESET depends on the current intensity. In terms of device performance, bipolar is more reliable than unipolar switching in terms of endurance as the former is influenced by applied field while the latter is dominated by thermal effects. The ON/OFF current ratio influences the power consumption and switching speed. The transition between resistance states can be a smooth curve or an abrupt jump in the current in a given threshold voltage. Several reports indicate that it is possible to obtain more than two resistance state which the memristive device can switch. Multiple filament formation, stoichiometry, surface

states, compliance current and source frequency[24] are some factors mentioned that influence the transition to multiple resistance states.

### 1.3.3. Switching Mechanism

Early work of Dearnaley et al.[13] , Oxley[25] and Petersen et al.[26] give detailed description of the physical mechanism of resistive switching in oxides and chalcogenide thin film devices. The irreversible process of electroforming proceeded by stable switching thereof are shown to be due to filament formation across the insulating layer. Structural and conductivity studies of electroformed $TiO_2$ devices give strong evidence of the localized channel formation[27–29]. Switching dynamics is classified into three categories based on whether redox reaction or ionic conduction happens during switching[30]. This includes thermochemical mechanism (TCM), valence change mechanism (VCM) and electrochemical metallization (ECM)[30–32]. The first category is associated with thermal effects wherein current-driven increase in temperature results to filaments formation and rupture. This category best explains unipolar resistive switching. The second category is linked to oxygen vacancy migration which causes changes in oxide stoichiometry. In this mechanism, a nonstoichiometric or multilayer oxide layer is introduced in the MIM device in order to alter the vacancy transport. The chemical control in this case is confined in the interface suggesting the dominant contribution of thin layers instead of localized filaments. Lastly in ECM mechanism, the switching depends on the metal ion diffusion from the active electrode (Ag or Cu) to the inert electrode. During the switching process, the conducting filaments can be composed of ions and vacancies.

The linearity or nonlinearity of the transport properties of MIM devices serves a clue about the nature of the charge carriers responsible for the switching. Nonlinear behavior can be accounted by ion transport or by electrode-insulator interface reaction[30]. It is important to note that once ion transport is taken into account, the channel length has to be of the order of atomic scale length – i.e. lattice constant or nearest neighbor distances.

## 1.4. Memristive Materials

Memristive effect have been observed in various metal oxides like transition metal oxides (TMOs), perovskites, multiferroics, ferroelectrics, wide band gap (high-*k*) dielectrics, organic-based materials like graphene oxide and polymers. On the other hand, non-oxide materials which exhibit similar effect include chalcogenides like selenides and tellurides. This suggests a wide range of material selection as building blocks of devices for memory applications[33].

Several switching mechanisms were proposed for particular materials to explain the phenomenon. For example, tunneling in high-k dielectrics is widely used to explain the low current and low power transport. Metal-insulator phase transition is very much studied using $VO_2$[34–36] as model material.

### 1.4.1. Oxide Thin Films

Titanium dioxide ($TiO_2$) thin film development has been of much interest because of its potential use in many practical applications. There is also a need to find an alternative material to replace $SiO_2$ for memory cells and field effect transistors (FET). $TiO_2$ – based memristive devices are well investigated in the literature. Recently, Strukov et. al.[2,37] proposed an empirical model of $TiO_2$ resistive switching and memristance in general. In this phenomenological approach, they described the $TiO_2$ layer consisting of doped and undoped regions. The boundary between these two regions is like a "moving wall" depending on the state variable $w(t)$ associated with the size of the doped region. When $w(t) \to D$, the device becomes more conducting ($R \to R_{ON}$) and when $w(t) \to 0$, it becomes more insulating ($R \to R_{OFF}$). Thus, such system was modeled as two variable resistors connected in series. The memristance equations are written as[2],

$$V(t) = \left( R_{ON} \frac{w(t)}{D} + R_{OFF} \left[ 1 - \frac{w(t)}{D} \right] \right) I(t), \qquad (7)$$

$$\text{where} \qquad \frac{dw(t)}{dt} = \mu \frac{R_{ON}}{D} I(t). \qquad (8)$$

It is clear that the state variable w(t) is dependent on the ion mobility μ such that

$$w(t) = \mu \frac{R_{ON}}{D} q(t). \qquad (9)$$

When we put equation (9) to equation (7), the memristance becomes

$$M(q) = R_{OFF}\left(1 - \mu \frac{R_{ON}}{D^2} q(t)\right). \qquad (10)$$

Equations (7) and (10) describe current-controlled memristive switching. The memristance equation (10) explicitly depends on the internal state of the device. Although this model fits the available experimental data, one has to argue that its universality is quite limited. This linear drift description encounters unavoidable nonlinear effects as one approaches the boundaries. Pershin and Di Ventra [38] suggested that description of current-controlled drift and ion mobility should also account for such boundary conditions. Further refining of this model has been done with the inclusion of a window function F which ensures zero drift at the boundaries.[39] Other models have also been developed and implemented to accommodate other material systems.[32,40–42]

Direct physical evidence of oxygen vacancy generation due to $TiO_2$ reduction during device operation has been reported. Amorphous, anatase and magneli phases are found to coexist in a working $TiO_2$ device.[28,43,44] The magneli phase is the reduced $TiO_{2-x}$ phase which exhibit metallic behavior. This reduced region predominantly carries the current across the oxide, thereby creating localized increase in temperature. Although this occurred only during high-field bias or electroforming process. High resolution x-ray photoelectron spectroscopy (XPS) results[45] of $TiO_2$ bilayer devices consisting of oxygen-rich ($TiO_x$) and oxygen-deficient ($TiO_y$) layers show evidence of oxygen drift across the interface region. Changes in the chemical binding states of $Ti^{2p}$ peaks are measured in the three oxide regions namely: $TiO_x$ layer, $TiO_y$ layer and $TiO_x$-$TiO_y$ interface. The oxygen-deficient $TiO_y$ layer did not exhibit significant changes in the Ti sub-oxide phases measured in the three resistance states. On the other hand, the $TiO_x$ layer and the interface region show increase in the metallic phases $Ti^{3+}$ peak intensity in the low resistance state.[45] Clearly, the $TiO_y$ layer acts as the charge reservoir during

switching. The $TiO_x$ layer and the interface region become more conducting as conducting filaments are formed during electroforming and SET processes.[46,47]

Much effort has also been done to investigate the role of intentional doping or the presence of nanoparticle interstitials in the switching behavior of several oxides. Defects have been crucial assisting field localization thereby suppressing further potential build up during bias. The presence of well-separated nanocrystals in the oxide facilitates the formation of polar charges which affects the hysteresis in the IV curve.[48] $Al_2O_3$ MIM devices have been studied on its memory performance by embedding metal nanocrystals on the $Al_2O_3$ matrix. The advantage of Ru on $Al_2O_3$ is that the high-dielectric property of $Al_2O_3$ accommodates trap-rich regions which act as charge storage layers.[49] This results in direct tunneling effect in the $Al_2O_3$ bulk during bias programming.

Qin et al.[50] suggested that modification of the oxide-electrode interface using Ag nanoparticles enhances the memristive behavior of $Al_2O_3$ devices. During bias in a MIM device, oxygen vacancies are influenced by a uniform electric field which enables the formation of cylindrical-shaped conducting channels parallel to the applied field. The SET and RESET processes show fluctuations in their values and this can be attributed to the random channel rupture and recovery. This is because no filament was more favored to rupture, as this is the nature of how the ensemble of filaments is initially formed. On the other hand, the presence of Ag nanoparticles alters the electric field distribution. This creates localized fields which facilitate the growth of conducting filaments while suppressing the random nature of this process. The results show minimized resistance state dispersion and lower SET and RESET voltages which translate to more stable (both endurance and retention) devices and lower power operation.[50] Similar improvement in the endurance has also been observed in Al-$AlO_x$ multilayer devices. Song et al. proposed that by increasing the number of Al-$AlO_x$ layers, the number of active regions for the filament growth and rupture also increases.[51]

### 1.4.2. Oxide Nanostructures

The localized nature of filament generation during resistive switching suggests the possibility of fabricating nanostructure-based memristive devices. Moreover, surface

effects and carrier dynamics can be conveniently investigated in such systems as compared to the study of filaments sandwiched in bulk devices[52]. Among the nanostructured memristive oxide devices reported in literature include nanowires (NW)[52–61] nanotube (NT)s,[62] nanobelts (NB)[63], quantum dots (QD)[64] and nanoparticles (NP).[65–70] Due to size effect, charge localization, field distribution and impurity, the diffusion in nanostructures behave differently in comparison to bulk materials. NW-based memristive devices are of much interest because of the ease of synthesis and the possibility of fabrication of individual NW devices. This entails much more sophisticated methods in conducting detailed study of charge transport mechanism and other nanoscale physical phenomena.

Nagashima et al.[52] demonstrated bipolar resistive switching in fabricated single MgO/$TiO_2$ NW devices. The memristive switching of these devices was found to be affected by the different gas environments. Moreover, the nature of the transport carriers was n-type which was in contrast to the p-type character of carriers normally concentrated in conducting filaments. One particular observation was the decrease of low resistance state (LRS) when the device was exposed to oxidizing environment.[52] They concluded that such behavior could be due to the effect of electron compensation through NW surface oxidation with the environment. Huang et al.[55] utilized ZnO NW-thin film junction diodes (1D) and memristive devices (1R) to show rectifying and resistive switching behaviors in one device (1D1R). One advantage of this configuration was the mitigation of sneak path currents which arose in crossbar devices. The presence of NW layer creates device asymmetry (non-symmetry Schottky barriers) as well as vacancies or surface states which facilitate stable switching.[71] The ZnO NW layer acts as a reservoir for oxygen vacancies readily accessible during filament formation and rupture[55]. Similarly, Qi et al.[57] reported self-rectification and self-compliance behavior during switching of single Na-doped ZnO NW devices. The fabricated device had the Pt electrode connected to the ground while the active Ag electrode connected to a voltage bias. It was observed that a chain of Ag nanoislands formed on the NW surface during electrical characterization. High spatial resolution Auger electron spectroscopy (HSR-AES) map of the Ag distribution along the NW length showed the highest concentration of Ag in the biased electrode (Ag) while the lowest concentration was found in the

middle. Self-compliance enhancement was attributed to the asymmetry of electrodes and Na-doping. It was also inferred that Na-doping facilitates the segregation of Ag atoms during bias.[57] Dendritic Ag NP cluster formation was also observed in ultrathin devices of $SiN_x$ membranes.[72] However, it has to be considered that in 1D nanostructures, the fractal behavior of the filament is now limited to the axial confinement as compared to 2D systems.[60] Controlling such filaments was dependent on the programming current owing to the reduction of Ag ions within the switching layer through electron capture.[18,73] Moreover, it was shown that by changing the SET voltage in Sb-doped ZnO NW devices, multilevel resistance values could be obtained.[61] This was due to the fact that Sb-doping increased resistivity and thereby narrowing the voltage distribution during SET process.

Another approach implemented to obtain enhanced resistive switching was to utilize the piezoelectric property of ZnO NW. Wu and Wang[59] demonstrated from a piezoelectrically modulated resistive memory (PRM) device that the applied strain (tensile and compressive) drastically influenced the hysteretic I-V characteristics. The absence of central symmetry of the ZnO crystal[74] meant that mechanical perturbation on the crystals had effect on the ionic polarization. This gave birth to a new phenomenon called piezotronic effect. It was described as the tuning of the barrier height at the electrode-oxide interface by the strain-induced charge polarization.[59] They also showed that the conductance ratio was stable ($\sim 10^5$) with different values of applied strain. These results offer large potential for the fabrication of flexible ZnO NW-based memory devices.

### 1.4.3. Application

In this section the overall performance of memristive devices based on particular application is discussed. It is important to consider that some device characteristics are of much importance while others can be compromised up to a certain extent. Switching properties which arise as some electrical parameter-dependent are highlighted and evaluated in relation to specific device applications.

Crossbar device architecture is now used for the fabrication of high-density nonvolatile memories.[75–78] The feasibility of memory devices to be implemented in the existing chip

technology is to put small-size cells into densely-packed configuration (for more scalability). Crossbar array configuration enables the selection and programming of individual memory cell. However, there are challenges that have to be addressed like sneak path current to avoid incorrect selection of memory cells during read/write process. In fact the signal from unselected devices in the crossbar array can contribute noise during operation.

Yanagida et al.[79] studied the effect of cell area in the resistive switching characteristics of crossbar devices. They proposed threshold lines highlighting the boundaries between unipolar, bipolar and no switching regimes. The coverage of these regimes are mapped according to the applied electric field or forming current as a function of cell area. Fig. 1a shows the area dependence of switching with applied electric field while Fig. 1b shows the dependence with forming current.

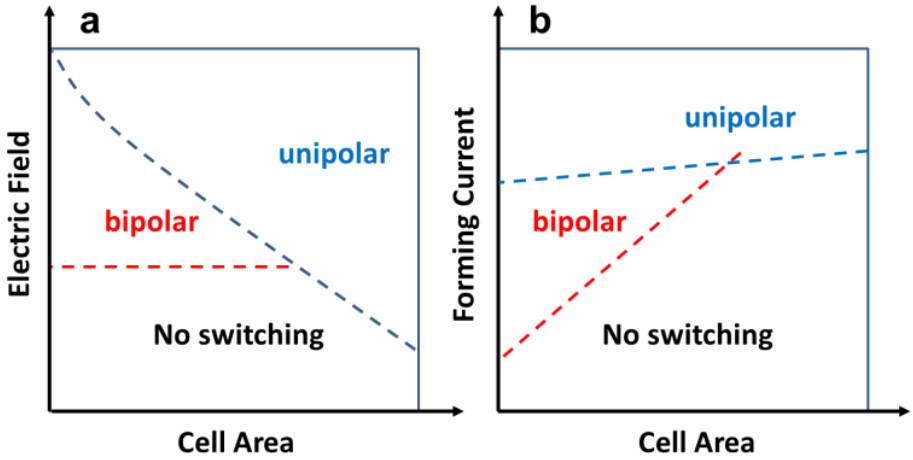


FIG. 1. Area dependence of the different switching regimes with the applied electric field (a) and forming current (b).

Devices commonly exhibit no resistive switching when biased with low electric field or low forming current regardless of cell area. The threshold electric field necessary for bipolar switching is not much affect by the cell area. In fact, there is no noticeable effect (~$10^6$ V/cm) with a wide range of cell area ($10^2$ to $10^6$ $nm^2$).[79] As presented in Fig. 1a, the electric field required for unipolar switching is influenced by the cell area. The smaller the cell area, the larger the electric field necessary for unipolar switching and vice versa. The forming current for unipolar switching is not that affected with the wide range of cell area being measured. On other hand, this is not the same with bipolar

switching. There is a noticeable increase in the threshold current from $10^{-9}$ to $10^{-4}$ A when the cell area is increased in the range $10^2$ to $10^6$ $nm^2$. The crossover of the two threshold lines in both diagrams supports the commonly observed unipolar switching in devices with large cell area.

Another way of connecting memristive devices in crossbar array is by stacking complementary devices.[80] Linn et al.[78] suggested that connecting two devices anti-serially solves sneak path problems. Their device is composed of Cu bottom electrode and Pt top electrode with GeSe sandwiched layer. The complementary devices have the same mechanism as that of CMOS inverters wherein one of the transistors is always turned OFF, so the operating current is greatly minimized. Moreover, they also mentioned that the memory resistance has no dependence on the stored bit of information but in the pre-defined state during the write process.[78]

Adding nonlinearity feature to the Pt/ $TaO_x/TiO_{2-x}$/Pt devices in a crossbar array has been shown to simplify the crossbar implementation by avoiding extrinsic device selection and by operating at low current around $10^{-6}$ A.[76] It has been reported that the nonlinearity arises from the $TaO_x/TiO_{2-x}$ bilayer and the resistive switching happens in the Pt/$TaO_x$ interface.[76]

Another switching characteristic that needs to be emphasized is the switching speed of memory devices. Volatile memory applications require several hundred picoseconds to nanoseconds of switching to accommodate fast data processing. Pulse-induced switching is usually performed to determine the high speed switching characteristics.[81] Lee et al.[82] obtained high speed switching of about 5 ns. The device, composed of $HfO_2$ switching layer and Ti buffer layer, exhibits high resistance ratio and reliable retention (about 10 years) even at 200 °C temperature. Zhang et al.[83] reported similar response time in Pt/$STiO_3$:Nb junction devices. It is also reported the possibility to obtain multi-valued memory states with similar switching characteristics in $TiO_2$-based devices.[84] Sub-ns time response was also observed using GHz pulse generator. It has been demonstrated[85] that a 300 ps pulse of 1.4 V amplitude provides enough energy for switching a $HfO_x$ based device. Torrezan et al.[86] also reported sub-ns switching behavior of Ta oxide memristor in the 100 ps timescale. Utilizing the ultrafast switching characteristics of memristive devices shortens the programming time during write

process. Moreover, this device capability offers the possibility of competing with the DRAM performance.[87]

Neuromorphic process is also a rich area of application where fast memristive dynamics can be exploited. Although it has also direct application in digital logic, research interest has not been reinforced due to the success of CMOS technology in this application. Early work of Widrow[88] in the 60s used the concept of memistor (resistor with memory) to describe and mimic the firing of the neuron. It is necessary to have electronic control over the neural output by storing the negative or positive gain values depending on how the input signals are temporally introduced.[88,89] In electronic devices the neural firing is generated by artificial synapses or spikes. The amplitude of such signal can be varied according to the timing of pulse namely pre-synaptic or post-synaptic spike.[90–92] Since this system is asynchronous, which does not require a clock like in digital logic, information processing can be done in parallel.[89]

Spike-timing-dependent plasticity (STDP) learning mechanism is one area of study being explored apart from the resistive switching phenomenon on various materials. The comprehensive overview of the STDP process can be found in the suggested references.[93–95] Ultrafast STDP was implemented in chalcogenide memristors to mimic the synaptic weight modification during pulsing.[96] Potentiation (increase in device conduction) and depression (decrease in device conductance) were observed when negative and positive pulses were applied, respectively. It was found out that the pulse width upper limit for the chalcogenide memristor to undergo phase change from crystalline to amorphous state is 30 ns with 1.4 V amplitude. However, this is still 5 orders of magnitude faster than that of normal synapses in biological processes (milliseconds).[89] Many phase-change memory devices exhibit the potentiation and depression behavior during pulsing.[97–99] In oxide devices, the initial pulse generates the largest change in the conductance either during potentiation or depression. The succeeding pulses tend to create saturation in the conductance values. This jump in conductance can be attributed to charge trapping and de-trapping processes which normally happen in very short time scales.[100,101] The conductance saturation is the effect of leakage current due to additional stress-induced defects formed after many pulsing

cycles. Detailed studies of STDP variations due to device-specific implementation have been previously reported.[102,103]

The potential application of memristor and memristive system is wide and a lot of areas have not yet been explored in detail. The immediate application in non-volatile memories promises fair alternative to DRAM technology. Neuromorphic and STDP application utilize device properties like fast switching dynamics, multistate and analog switching in various materials systems. Full realization of these applications relies on the fundamental science i.e. better understanding of the filaments dynamics, charge transport and defect formation in memristive materials. Thus, it is imperative to provide thorough investigation of the materials processing and device fabrication of memristive system.

# 2. Materials Processing

This chapter will discuss the growth of ZnO nanowires and $TiO_2$ thin films as starting materials for the fabrication of memristive devices. First, low-pressure chemical vapor deposition (LPCVD) of ZnO nanowires will be described. Next, atomic layer deposition of $TiO_2$ thin films will be discussed in detail. It will be important to also mention the dependence of materials preparation to the material properties. Therefore, this will the focus of most of the discussion here. Lastly, device fabrication methods used in this study will also be discussed.

## 2.1 Chemical vapor deposition

Interest in ZnO nanostructure studies have been growing since the development of nanoscience and technology. Sophisticated techniques were developed and improved for nanoscale processing and characterization. ZnO received much interest in areas of electronics, photonics and opto-electronics due to its unique defect chemistry. There are a variety of deposition techniques routinely used for the production of different ZnO nanostructures.[104–108] This includes hydrothermal technique,[109–112] vapor phase transport (carbo-thermal),[113–118] thermal oxidation[119–121] and chemical vapor deposition (CVD).[122–125]

Among the above-mentioned NW growth methods, hydrothermal technique requires the lowest growth temperature (90 °C) while other techniques need higher temperature at least 300 °C. However, post-heat treatment is normally required to minimize the unnecessary impurities in hydrothermally-grown NWs. CVD has more advantages in terms of controlling growth parameters, crystallinity, intentional doping and homogeneity of ZnO NWs. CVD requires only moderate growth temperature and more control in the growth environments. It is well known that different preparation parameters affect the ZnO nanowire properties. Seed-layer has been known to enhance the epitaxial orientation of the grown ZnO NWs. Prior to the NW growth, it is required to perform the initial deposition of metal catalyst or acetated-seedlayer.[122,126,127] The crystal orientation of the seed-layer is independent of the substrate used.[126] Some reports demonstrated that surface roughness assists ZnO NW growth even in a catalyst-free substrate.[118,128] Yu et al.[113] reported the synthesis of ZnO NWs in a substrate without metal catalyst in a double-tube configuration. The purpose of using a smaller

tube is to confine the Zn vapor during reaction. This results to larger Zn-rich region in the tube thereby increasing the length of grown ZnO NWs up to 6 μm. However, the vertical growth of nanowires is impeded due to the absence of catalyst or seedlayer for epitaxial growth.

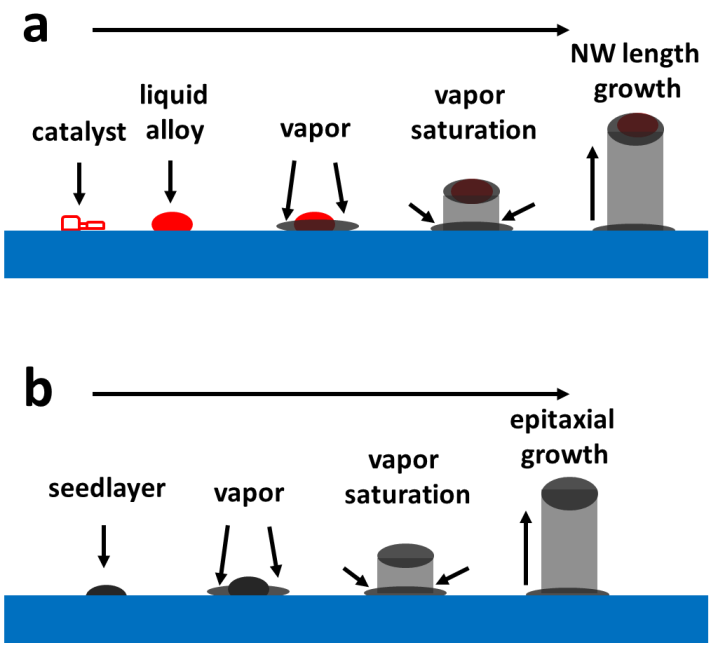


FIG. 2. Nucleation and nanowire growth process in the presence of catalyst (a) and seedlayer (b).

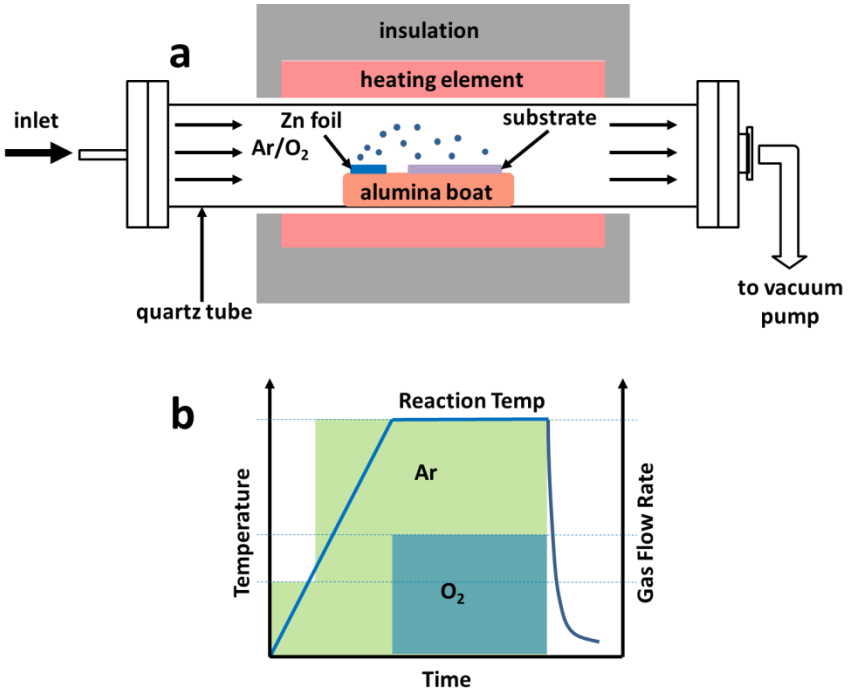


FIG. 3. Schematic diagram of the horizontal tube furnace used (a) and reaction temperature profile (b) for low-pressure chemical deposition (LPCVD) of ZnO NWs.

In this study, a 27 mM solution of zinc acetate di-hydrate was spin-coated on Pt-coated Si/SiO2 substrates, rinsed with ethanol and blown dry with $N_2$ gas. After covering the substrate with several layers of the solution, it was annealed in air at 350 °C for 20 minutes. This procedure was repeated to have a film consisting of 10 layers.

LPCVD was performed in a typical thermal CVD system consisting of a horizontal quartz tube furnace. The tube was evacuated to about $10^{-3}$ mTorr base pressure. Zn foil was used as Zn source. The substrate was positioned toward the downstream direction as illustrated in Fig. 3. The standard LPCVD process was done at a temperature of 650 °C for 20 minutes. The system was maintained under vacuum and Ar gas was used a carrier gas with 300 sccm flow rate during the whole process. $O_2$ gas was introduced with 50-150 sccm flow rate during the growth process.

Several LPCVD trials were made to determine the parameters affecting the growth of ZnO NW. The deposition temperature was varied from 650 to 800 °C. Homogeneous and dense growth of ZnO NWs was observed in the deposition temperature of 650 and 700 °C. The growth ZnO NW also exhibit high c-axis orientation. Previous study in our research group shows single crystal properties of an individual nanowire. Growth of

ZnO NW at 800 °C was not successful. It is possible that the Zn source was completely consumed even before $O_2$ gas was introduced to the reaction. Adding more Zn source in the chamber and shortening the ramp up time for heating the furnace are possible remedies of the problem. However, this approach seems to be impractical and not cost-effective.

Repeatability of ZnO NW growth is very important for device application. It has been practiced that during sample preparation all the equipment has to be clean ultrasonically cleaned with ethanol. Noticeable differences in the morphology of synthesized ZnO NWs have been observed. The quartz tube is regularly cleaned to maintain the base pressure for each LPCVD process. The successive LPCVD process leaves ZnO deposits on the inner wall of the tube. This also degrades the ZnO NW growth quality and uniformity. Thus, it is imperative to always use a freshly cleaned tube to minimizes the factors that affect the variability of NW growth.

Patterned seedlayers are also used for the NW synthesis. After the spin-coating of seedlayer, standard photolithography and wet etching were done. Circular and rectangular strip patterns are used. It is also demonstrated the possibility of NW growth in sputtered ZnO thin films. These initial experiments are very important in stablishing a standard recipe for the growth of ZnO NWs.

## 2.2. Atomic Layer Deposition

Atomic layer deposition (ALD) is a vapor phase deposition technique which utilizes surface kinetics during thin film deposition. ALD is a versatile technique of growing crystalline, polycrystalline and amorphous coatings. The early development of atomic layer epitaxy (ALE) started with a need of a robust thin film technology for electroluminescent display devices.[129] Recently, ALD is gradually integrated in semiconductor technology for the production of gate oxides in transistors and dielectric layers in capacitors for memory applications. The metal oxide dielectrics used include $TaO_x$, $Al_2O_3$,[130] $HfO_2$ and $TiO_2$. In the case of $TiO_2$ various metal organic precursors are used Ti source namely titanium tetrachloride ($TiCl_4$),[131] titanium ethoxide ($Ti(OEt)_4$)[132] and titanium isopropoxide ($Ti(O^iPr)_4$)[133] among others. Moreover, the typical co-

reactant used as oxidizing precursors are water ($H_2O$), hydrogen peroxide ($H_2O_2$), oxygen gas ($O_2$), ozone ($O_3$) and other oxygen-containing organic compounds.

In a typical ALD, the substrate is exposed to gaseous chemical species that are introduced alternately and separately. This process is said to be self-limiting because the ideal ALD cycle is purely surface reactions in nature. In order to grow a sub-monolayer for each cycle, it is necessary to always have active sites on the substrate surface.[134] There are four steps that take place in one ALD cycle: (1) reactant A dose, typically a metal-organic ligands, (2) purge and pump step, (3) reactant B dose, typically an oxidizing compound and finally (4) purge and pump step. During the dosing of reactant A, the chemical species are chemisorbed onto the substrate. When the substrate is already saturated with reactant A, there will be no more chemisorption and the excess reactants are purged and pumped out of the chamber. This is followed by reactant B exposure. Normally, $H_2O$ or $O_3$ is used as co-reactant. Reactant B undergo chemisorption to the A sites until all the sites reacted. The reaction products and excess reactants are purged and pumped out of the chamber in preparation for the next ALD cycle. Substrate saturation during chemisorption is dictated by the reaction temperature.

The ALD window is achieved in a temperature range where self-limiting growth occurs. If the reaction temperature is too low or too high, condensation, gas-phase reactions or decomposition may occur. This means that incomplete reactions or some CVD-like reactions due to temperature affect the growth rate. The ideal growth rate per cycle (GPC) is not influenced by the reaction temperature in the ALD window. The figure below (Fig. 4) shows the possible reactions beyond the ideal ALD window. At lower temperature, condensation or low reaction may happen. When precursor vapor is subjected to temperature lower than the temperature of vaporization, there is a possibility of condensation and physisorption of precursors even beyond saturation. This results to an increase in the ALD growth rate. One the other hand, low growth rate occurs during the reaction when the thermal energy (due to low temperature) is not high enough to activate surface reaction. At temperature higher than the ALD window, decomposition or desorption may occur. If the thermal energy is high enough, thermal decomposition of precursors on the substrate happens thereby increasing the GPC. The

reverse effect of desorption occurs when the chemisorbed molecules do not stay on the substrate which limit saturation. This results to an uncontrolled decrease of GPC.

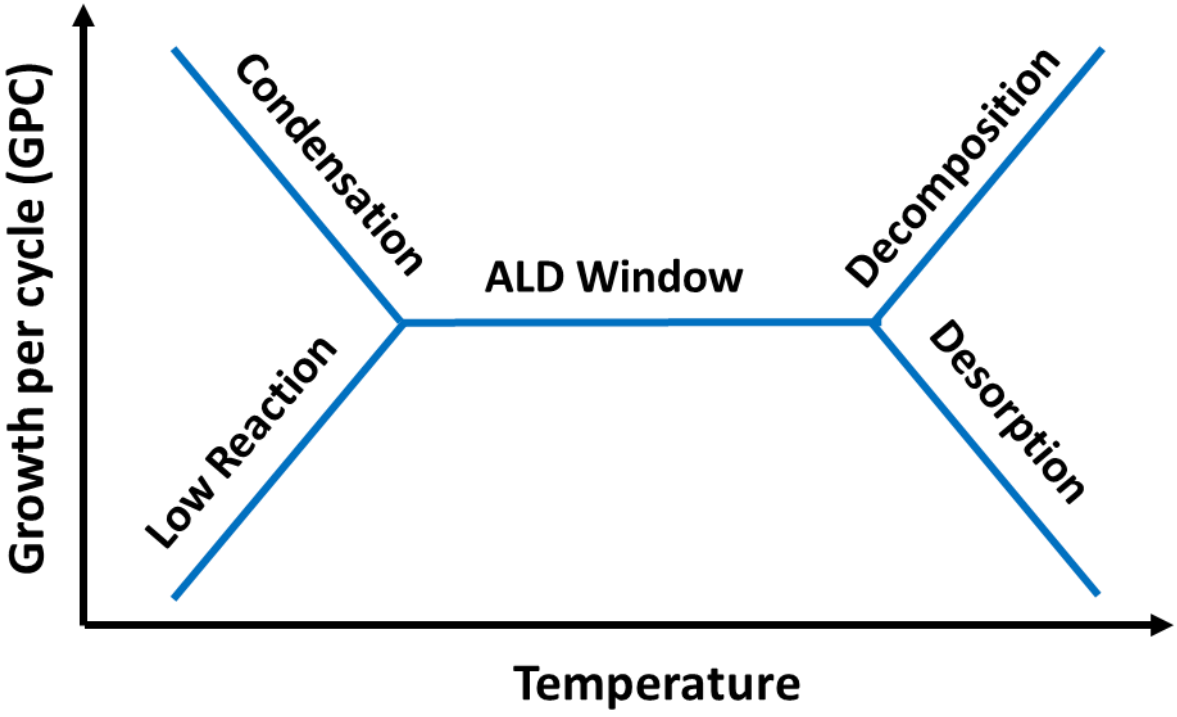


FIG. 4. Ideal ALD window and temperature dependence of growth rate.

Most ALD reactors are similar to CVD systems. The precursor reactions dictate how the system is built. In designing an ALD system, one has to consider the cyclic ALD steps. As described previously, the precursor flow is not continuous unlike in CVD. Moreover, the wide range of deposition pressure has to be considered. The exposure and purge sequence has to be optimized in any type of ALD reactor. A background discussion is given for the different types of ALD reactors namely, flow-type, showerhead, batch, plasma-enhanced and spatial ALD.[135–141]

**Flow-type ALD**. This reactor design is composed of a heated deposition chamber similar to a furnace. The precursor species are directly delivered to the main chamber using a carrier gas. The fluid transport during deposition is maintain to be laminar by controlling the flow rate, pulsing time and purging rate. In most cases, the precursor delivery line is also heated to avoid condensation. The main chamber can only accommodate a full wafer. This is sometimes a limitation considering large-scale manufacturing.

**Showerhead type ALD**. Precursor species delivered to the chamber are evenly distributed using a showerhead. This design prevents CVD-like reactions because it minimizes pressure gradient across the substrate area. A double-chamber design is typical in showerhead type ALD to have uniform temperature close to the substrate. The inner chamber should be of higher temperature than the outer chamber to avoid unnecessary reaction far from the substrate. This is implemented by attaching the outer wall to a cooling system.

**Batch ALD**. A large volume reactor design can accommodate multiple wafer samples for batch ALD processing. This design increases the manufacturing yield for each deposition process. This is beneficial in large-scale manufacturing because ALD is characterized as a slow deposition process for optimum thickness control. Modifications should be implemented regarding the exposure and purging rates. The precursor diffusion is much slower in batch ALD. Thus, the residence time and purging time for each half-cycle should be longer than in a single wafer reactor to maintain the optimum ALD conditions.

**Plasma-enhanced ALD**. Some precursor species require higher thermal energy to activate ALD reaction. The use of plasma energy to activate reaction is implemented without requiring high temperature. This is advantageous for thermally-sensitive precursors and substrates. Co-reactant species do have short lifetimes. Thus, the integrated plasma reactor should be optimized such that the created radicals reside very close to the substrate. PEALD is also advantageous in single reactant ALD for metal thin films.

**Spatial ALD**. In this reactor design, instead of sequential pulsing of precursors the substrate or the substrate holder is moved in the different zones in the chamber. There is continuous flow of precursors in different spatial zones in the chamber. Each spatial zone is considered as a half-reaction region. This can be implemented using a rotary reactor. Multiple flanges can be used to prevent the precursors from mixing once they are introduced to the chamber. This has an advantage in roll-to-roll deposition of flexible substrates or even textiles.

The above-mentioned reactor designs are mostly combined in a single ALD reactor to obtain optimal advantages like film uniformity, low temperature processing and high ALD throughput. For a research-grade ALD system, the integration of in situ thin film and ALD reaction diagnostics is also considered.

The high thickness control and self-limiting characteristics of the ALD process make it possible to deposit thin films in any type of substrate. Conformal ALD coating in high aspect ratio nanostructures for electronic and energy applications was demonstrated.[142–145] Moreover, ALD has much advantage in low-temperature thin film processing especially in self-assembled monolayers (SAMs) and polymeric substrates.[146–150]

In this study, the ALD tool used was a Beneq TFS-200 model. The schematic diagram is depicted in Fig. 5. The hot wall, flow-through type ALD reactor can accommodate an 8'' substrate. The reactor is enclosed in the larger main chamber. The uniformity of deposition is guaranteed also on high aspect-ratio structures (up to 1/50).

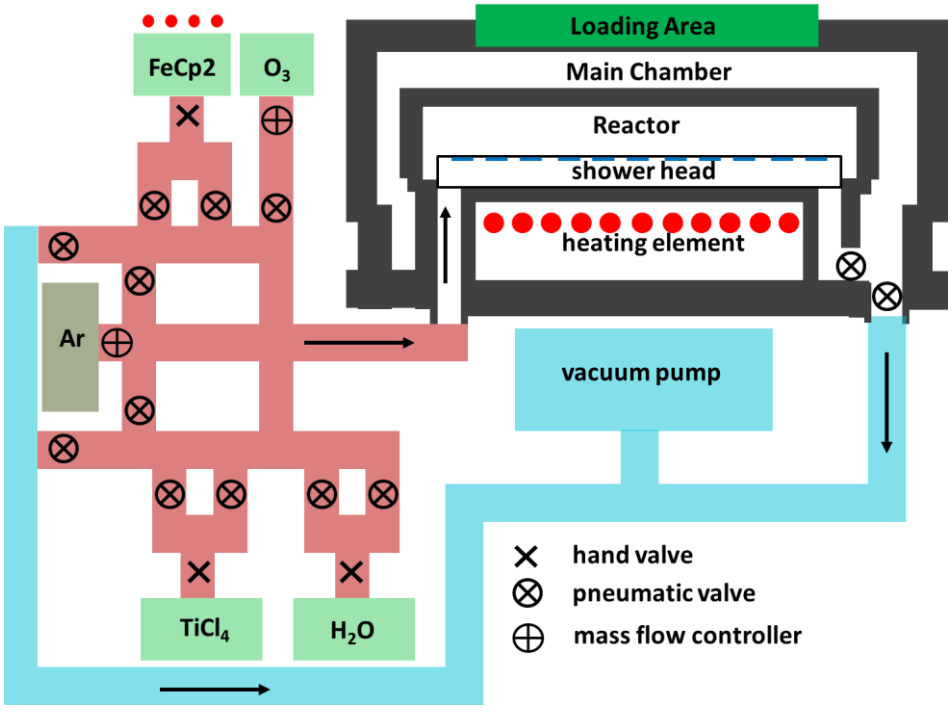


FIG. 5. Schematic diagram of the ALD reactor used for the deposition of $TiO_2$ thin films.

## 2.3. Device Fabrication

The effect of the ZnO NW interface to the memristive behavior of ZnO NW-based memristive device was investigated in this of the study. Two types of top electrodes were used: Pt and Cu. Pure ZnO NW and polymer-coated ZnO NW were used as insulating layer. A total of four types of devices were prepared.

For the fabrication of ZnO NW memristive devices, a thin Pt layer (200 nm) was deposited on top of ZnO NW layer by sputtering using a hard mask to obtain circular patterns for the top electrode. Fig. 6 shows the steps of the fabrication process.

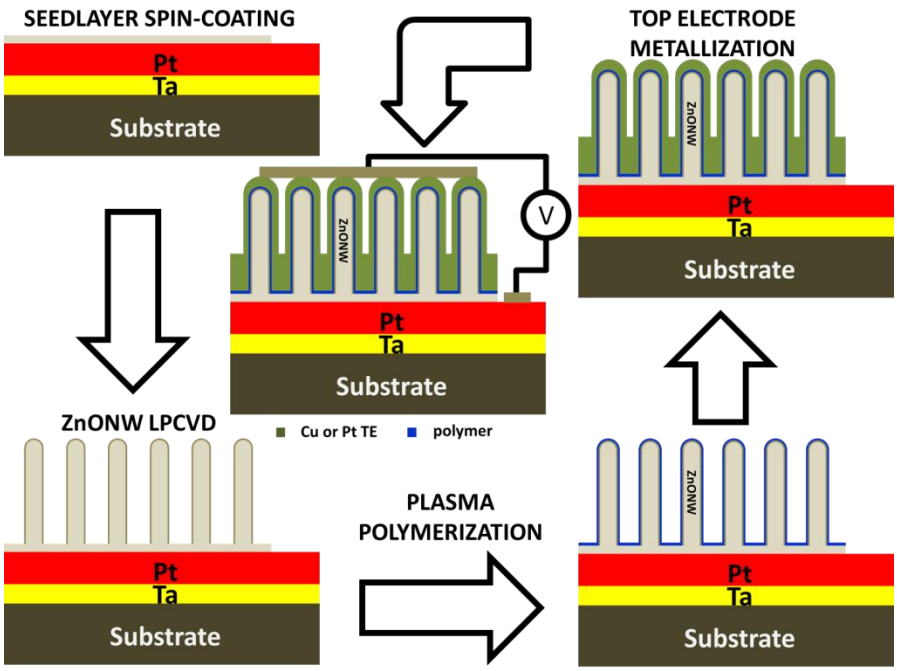


FIG. 6. Fabrication procedure for Pt/ZnO NW/Pt memristive devices.

After the deposition of the top electrode, wet etching process was performed to expose the bottom electrode (Fig. 7). A dilute solution containing 1 g of HCl (37%) and 100 mL of distilled water was prepared for the etching process. A portion of the substrate was immersed to the etching solution for 30 s. Then, the etched area was washed with distilled water and dried with $N_2$ gas. This process was repeated until the optimum continuity of the bottom electrode was obtained.

For the ZnO NW-polymer (ZnO NW/PP) core-shell, plasma polymerization of acrylic acid (PPAA) was done in a PECVD system. [151] The ZnO NW was coated conformally with polymer as seen in Fig. 8. Cu electrode was deposited by thermal evaporation and a three-step photolithography procedure was performed to fabricate circular-patterned devices.

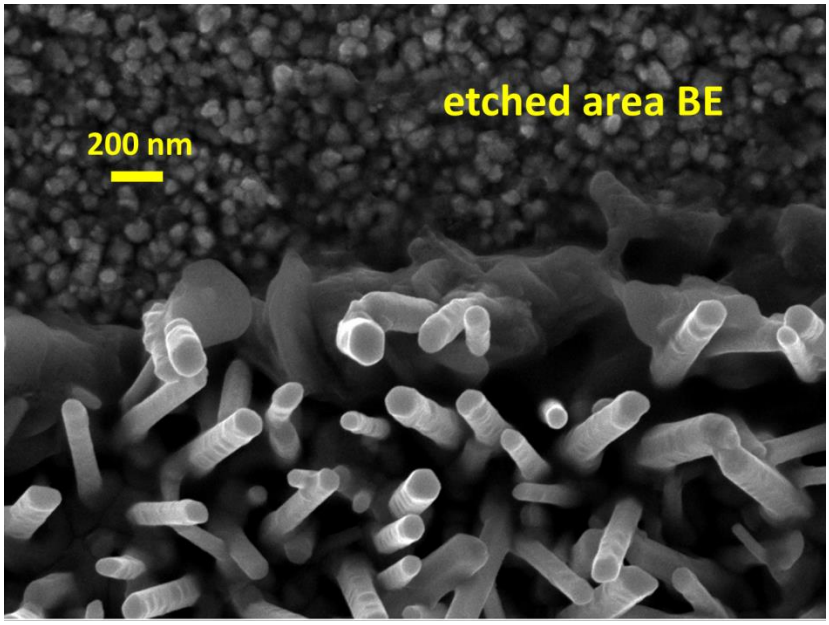


FIG. 7. FESEM of ZnO NW array showing the etched area exposing the bottom electrode.

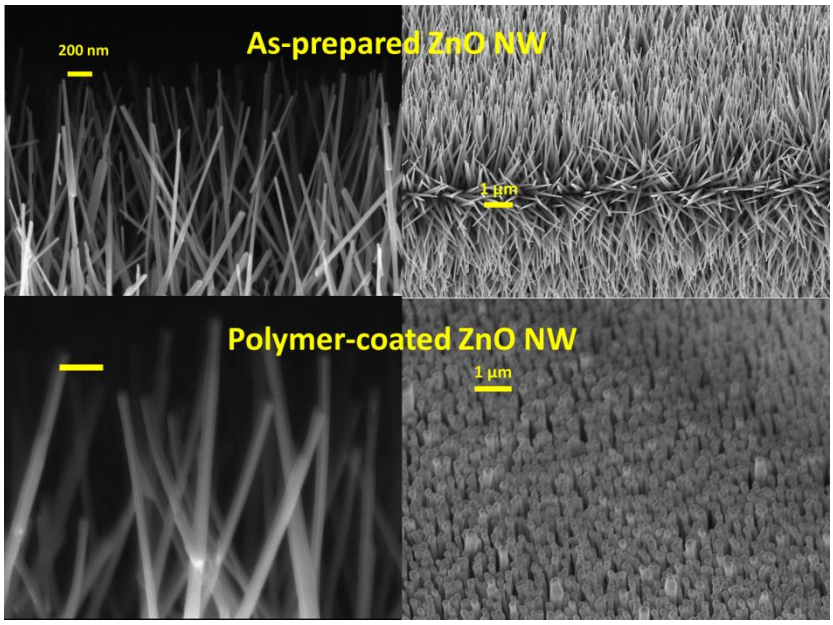


FIG. 8. FESEM of as-prepared and polymer-coated ZnO NW array.

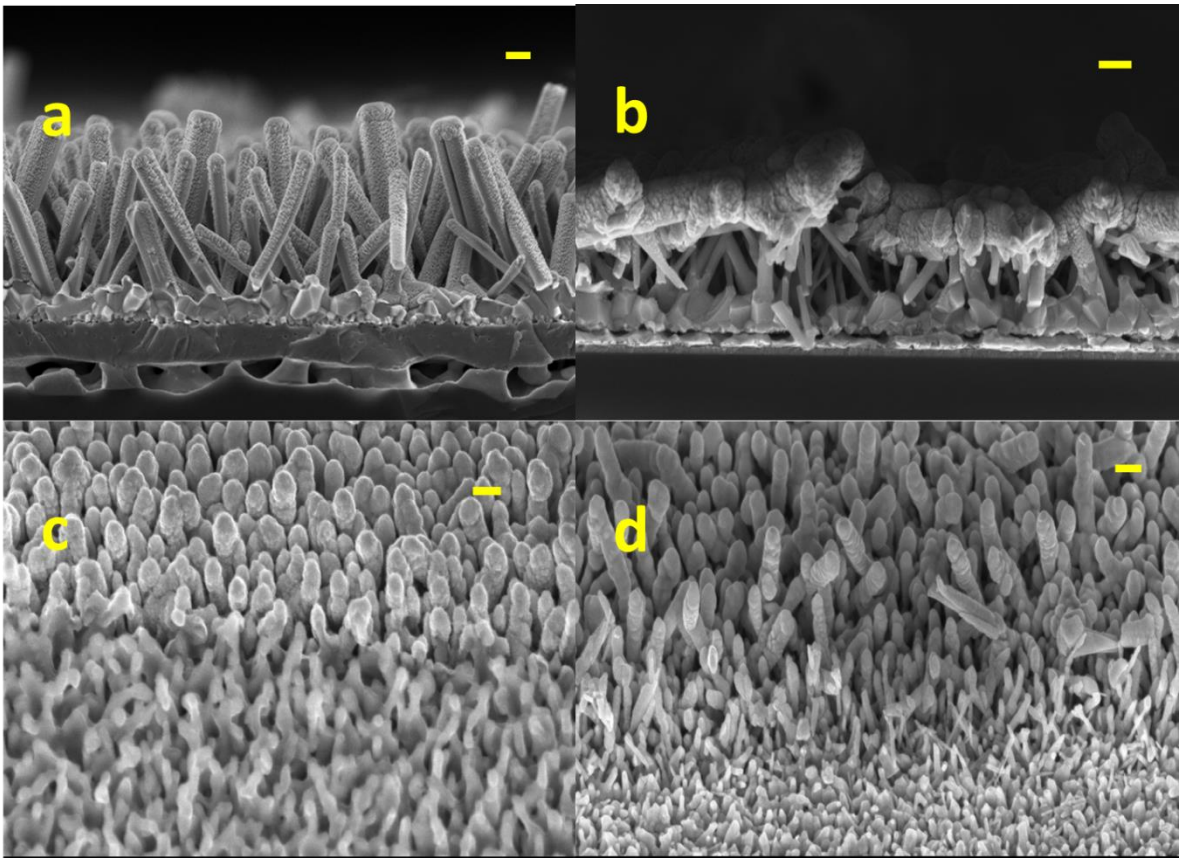


FIG. 9. FESEM of ZnO NW memristive devices: Pt/ZnO NW/Pt (a), Pt/ZnO NW/PP/Pt (b), Cu/ZnO NW/Pt (c) and Cu/ZnO NW/PP/Pt (d). scale bar = 200 nm

Conformal coating of the top electrode on the array of ZnO NWs is shown in Fig. 9. The top electrode coverage reaches the bottom part of the individual NW. It can be assumed that the whole length of the NW is fully covered with the top electrode. This means that the effective thickness of the device is equivalent to the thickness of the film at the bottom of the NW.

The pointed electrical probe is not directly used in contact with the top electrode to avoid excessive scratching during measurement. To measure the IV characteristics of these devices a tungsten coated metal cylinder (D = 1 mm). Few hundred NWs are in contact with the metal cylinder for every measurement. The measured IV characteristics is the average response of the ZnO NWs in contact with the metal cylinder. The current density can be easily calculated based on this set up. Another advantage of using the cylinder is the reduced mechanical pressure on each NW when contacting the top electrode. However, there is a limitation on how to control the contact pressure due to

the mechanical nature of the probe station in use. The use of a flexible probe solves this problem preventing damage on the device prior to electroforming.

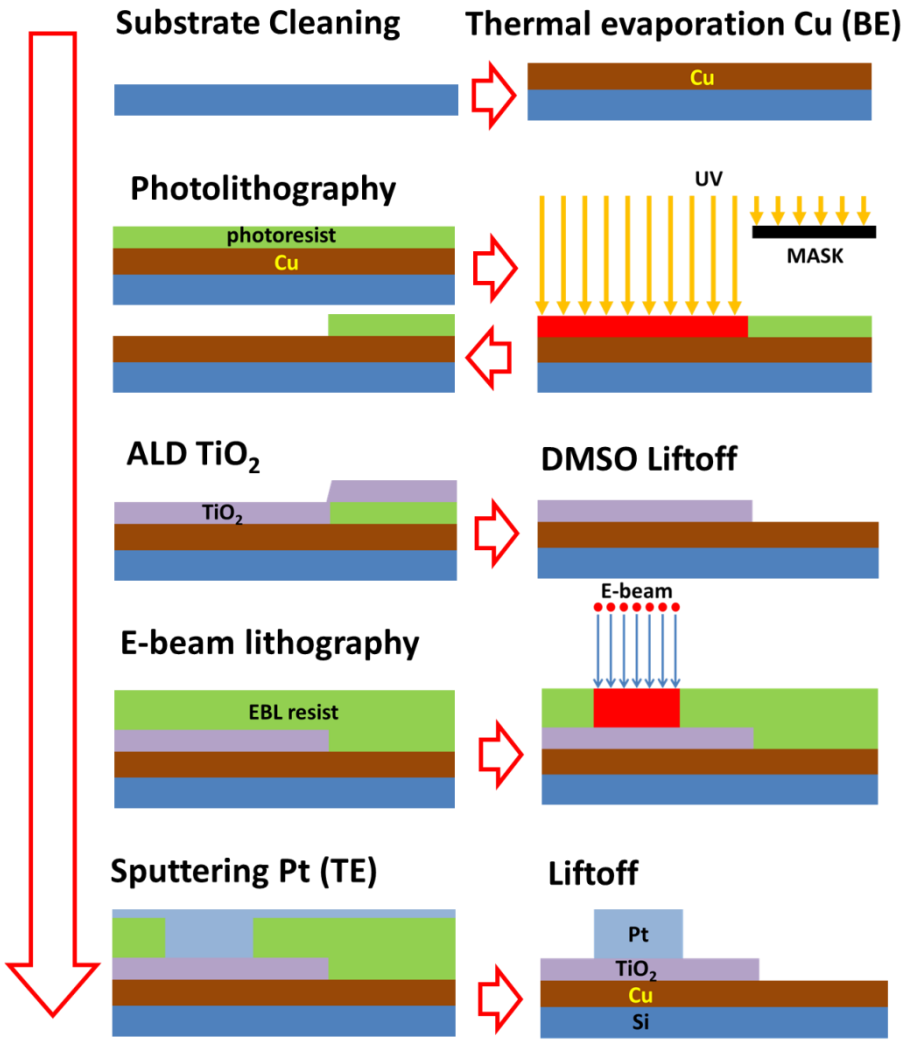


FIG. 10. Fabrication procedure for Cu/TiO2/Pt memristive devices.

Memristive devices based on $TiO_2$ switching thin layers were fabricated using standard UV photolithography and liftoff wet etching. Standard 4" Si wafers (100, p-type) were used as substrates and washed in piranha cleaning and deionized water.

Electron beam deposition of Cu onto Si provides a continuous layer for the bottom electrode with no further patterning required. A thin Ti interlayer (20 nm) provides the adhesion of the Cu thin film on Si. This prevents portion of the Cu layer from being detached (due to poor adhesion) from the Si wafer during liftoff. The mechanical liftoff

process makes the patterning of the $TiO_2$ thin layer more straight-forward. The procedure includes deposition of the photoresist (PR), patterning of the PR by photolithography, ALD of the $TiO_2$ thin films and mechanical liftoff. The details of the procedure[148] are described below:

- **Spincoating**. A thin layer of PR was spincoated on the Cu bottom electrode.
- **Patterning**. A circular mask of 1.2 mm diameter was used for the standard UV photolithography.
- **Atomic layer deposition**. Deposition of $TiO_2$ thin film (30 nm) was performed using low temperature ALD using Ar as the carrier gas. The precursor used are $TiCl_4$ and $H_2O$.
- **Liftoff**. Etching of the $TiO_2$ thin layer on the patterned PR was done in ultrasonic bath at 50 °C using dimethyl sulfoxide (DMSO) until the pattern definition was clearly visible. Subsequent rinsing DMSO and deionized water was done followed by drying in $N_2$ gas.

In order to optimize the liftoff procedure for patterning of $TiO_2$ layers, several ALD tests at relatively low temperatures were achieved varying the substrate temperature between 80 and 150°C, while carrier gas flow rate (250 sccm), precursor pulse (100 ms), $H_2O$ pulse (250 ms), purging times (2000 ms) and number of ALD cycles (400) were held constant. A sample processed at 230 °C was used as a standard reference sample. Field-emission scanning electron microscopy (FESEM) was performed on the samples for the morphology and thickness measurement. The FESEM analysis results were used to determine the film growth rate at different temperature. Samples for growth rate calibration were obtained on bare Si substrates by ALD tests using different number of cycles, using the growth conditions described above. To investigate the structure of $TiO_2$ layers, Raman spectroscopy was performed using a Renishaw inVia Reflex micro-Raman spectrophotometer equipped with a cooled CCD camera. $TiO_2$ samples (50 nm) for Raman analysis were deposited using the same growth conditions described above on Si substrates with an interlayer made of e-beam evaporated Pt (100 nm) in order to avoid the presence of Si Raman scattering from the substrate, which may interfere with the $TiO_2$ signal. Samples were excited with a 785 nm wavelength

solid state laser source using 1 sec exposures with 20 iterations and a 10% power filter to avoid $TiO_2$ crystallization due to prolonged and/or high power laser exposure.

The fabricated memristive devices are made of 30 nm thick $TiO_2$ layers deposited at 120 and 140°C and patterned using the liftoff technique described above, and on a reference $TiO_2$ sample deposited at 230°C and patterned by standard photolithography using reactive ion etching. The Pt top electrode (100 nm) was deposited via sputtering following a liftoff procedure similar to the one described above, to obtain circular electrodes of diameter 1 mm. The use of electron beam lithography provides the capability to develop smaller features for microscale (nanoscale) top electrode patterns. The I-V electrical measurements were performed in a two-point contact probe station at room temperature, while maintaining the top (Pt) electrode electrically grounded and the bottom (Cu) electrode under DC voltage sweep.

# 3. Materials and Device Properties

This chapter discusses the growth, characterization and performance of synthesized ZnO nanowires and $TiO_2$ thin film devices. The distinct structure of ZnO NWs has been utilized for more guided and localized filaments. This results to less dispersion between resistance states. The low temperature processing using ALD has been utilized for $TiO_2$ thin film devices. This approach has posed promising advantages as far as minimizing the fabrication steps is concerned. Moreover, optimization of low temperature processing via ALD allows the use of polymeric and other thermally-sensitive substrates.

## 3.1. ZnO Nanowires

Resistive switching in ZnO NW devices is described in this section. Most of the description on device performance were based on the thin films. The typical IV characteristics of memristive devices show resistance change with change in bias polarities. As described above, this phenomenon is dominated by the formation and dissolution of conducting filaments across the sandwich oxide. However, there are still ambiguities about the origin of the switching and the description of the filament dynamics. Individual switching cycles are said to be of random behavior because the filament dimension is highly localized. The unique configuration of ZnO NWs allows the formation of nanostructure-guided filaments which translates to lesser variation in the IV characteristics.

### 3.1.1. Nanowire Synthesis and Properties

The synthesis of ZnO nanowires starts by preparing seedlayers by spin coating a 27 mM zinc acetate-ethanol solution on $Si/SiO_2/Ta/Pt$ substrate and annealing the seed layer at 350 °C for 20 minutes. LPCVD was performed in a typical thermal CVD system consisting of a horizontal quartz tube furnace.[122] The tube was evacuated to about $10^{-3}$ mTorr base pressure. Zn foil was used as Zn source. The substrate was positioned toward the downstream direction as illustrated in Fig. 3. The standard LPCVD process was done at a temperature of 650 °C for 20 minutes. The system was maintained under vacuum and Ar gas was used as a carrier gas with 300 sccm flow rate during the whole

process. $O_2$ gas was introduced with 50-150 sccm flow rate during the growth process at 650 °C. To determine the electrical property of ZnO NWs, Pt top electrodes (200 nm) were deposited via magnetron sputtering using a hard mask (1 mm diameter). The Pt/ZnO NW/Pt devices were measured in a two-point probe configuration using Keithley 4200-SCS parameter analyzer.

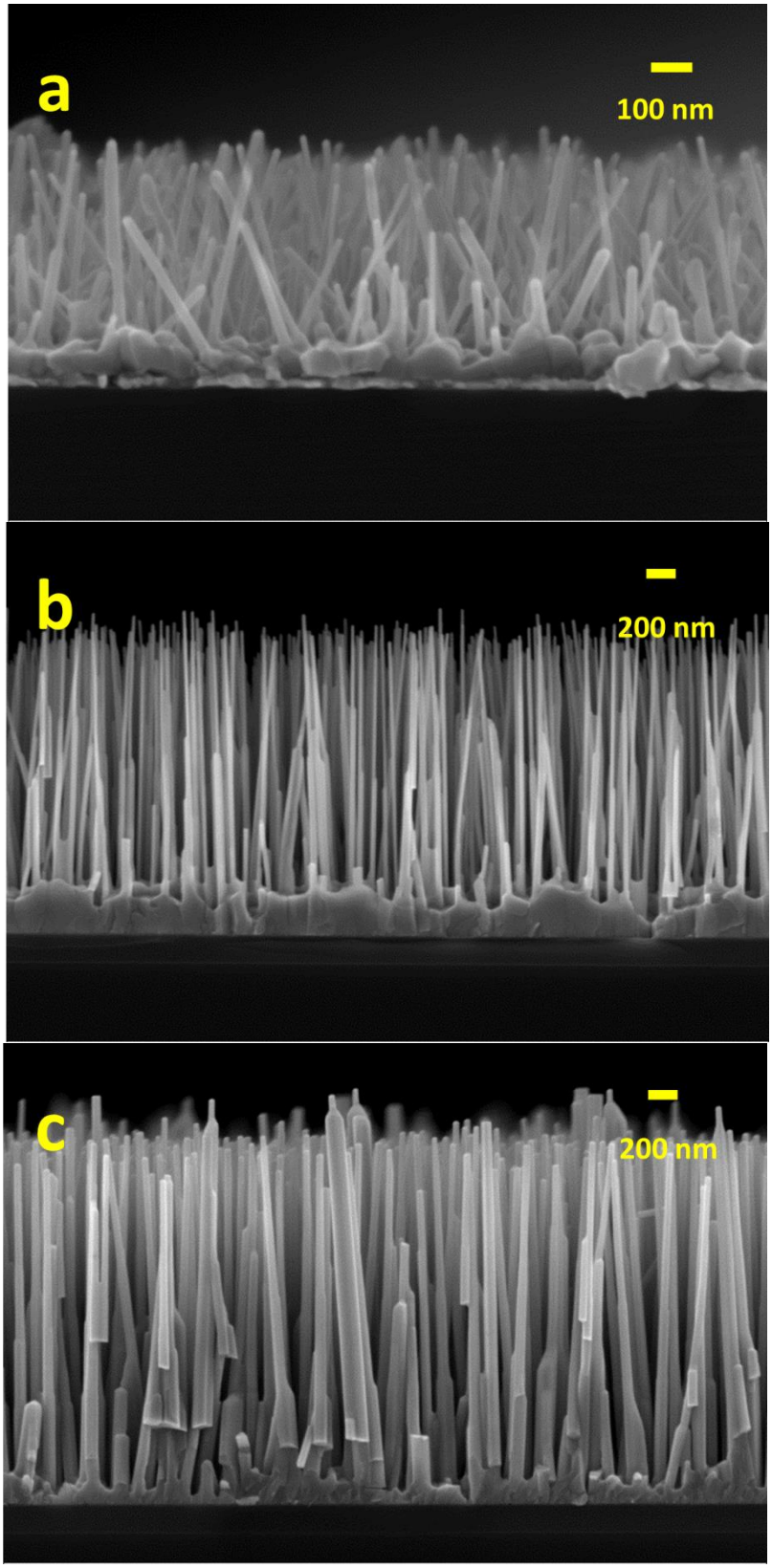


FIG. 11. Cross-section image of ZnO NWs grown with 50 sccm (a), 100 sccm (b) and 150 sccm (c) $O_2$ flow rates.

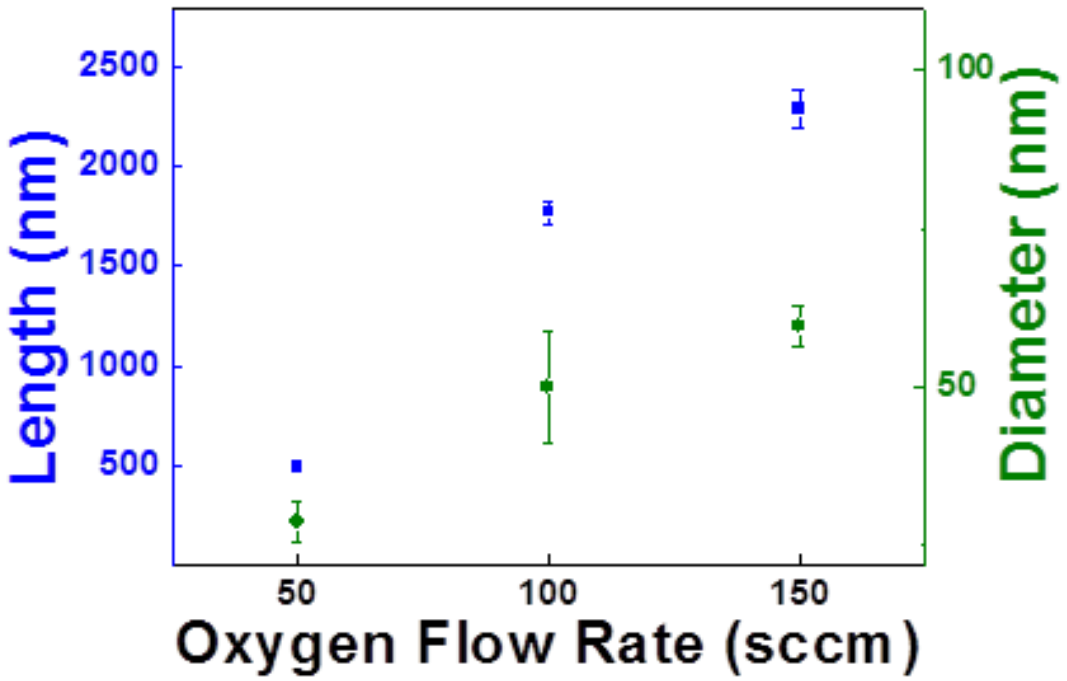


FIG. 12. ZnO NW dimensions (length and diameter) with different oxygen flow rates.

The FESEM cross-section images of the as-grown ZnO NWs with different oxygen flow rates are reported in Fig. 11. The typical length and diameter of the ZnO NWs with 50, 100 and 150 sccm flow rate are 500 nm and 30 nm, 1800 nm and 50 nm, and 2300 nm and 100 nm, respectively. The ZnO NW arrays can be described as having uniform growth in a 1cm x 1 cm substrate. A thin film of thickness about 100 nm is observed at the bottom of the ZnO NW arrays. This is much thicker than the observed features of the ZnO seed layer. It seems that this layer was formed prior to ZnO NW growth as the number of nucleation sites increases with time. The increasing trend in the ZnO NW dimension as shown in Fig. 8 has been the typical feature in $O_2$ rich CVD growth. This is also consistent with the kinetic and thermodynamic model reported previously.[114,152,153]

It was also demonstrated that by changing the $O_2$ concentration inside the tube furnace, one can determine the optimal condition for the onset of nucleation and ZnO NW growth.[152] It is also interesting to note that by increasing the $O_2$ flow rate, the deposition pressure significantly increases from 1 to 1.4 Torr. Several set of samples were prepared

to determine the optimal condition for NW growth. Considering the non-viscous flow of Ar-Zn system, the fluid transport can be described by the equation below:

$$\frac{\partial \rho \phi}{\partial t} + \boldsymbol{\nabla} \cdot (\rho \boldsymbol{v} \phi) = \boldsymbol{\nabla} \cdot (D \boldsymbol{\nabla} \phi) + S \qquad (11)$$

$\rho$ is the density of the fluid mixture, $v$ is the fluid velocity field vector, $\phi$ is the concentration, $D$ is the diffusivity and S is the source term.[114]

### 3.1.2. Device Characterization

The set of devices prepared was composed of symmetric Pt electrodes. Pt is a stable metal and it does not easily oxidize. Due to the high work function of Pt (5.65 eV) and large electron affinity of ZnO, the Pt-ZnO interface creates a Schottky barrier (0.75 eV).[154,155] Fig. 13 reports the bipolar resistive switching of ZnO NW devices. The resistive switching in one DC cycle was measured using the following steps:

- (1) OFF: Increase positive bias starting from 0 to $V_{max}$
- (2) SET: Transition from HRS to LRS
- (3) ON: Decrease positive bias starting from $V_{max}$ to 0
- (4) ON: Decrease negative bias starting from 0 to $V_{min}$
- (5) RESET: Transition from LRS to HRS
- (6) OFF: Increase negative bias starting from $V_{min}$ to 0

In a typical cycle, the compliance current was set to 5 mA to prevent permanent breakdown. It can be seen in Fig. 13a that in the positive bias, the device is SET (ON state) around 0.7 V. When the voltage bias is turned off during the ON state, the device remains in the LRS. The device resistance state transitions from LRS to HRS during the negative bias at a RESET voltage around -0.7 V.

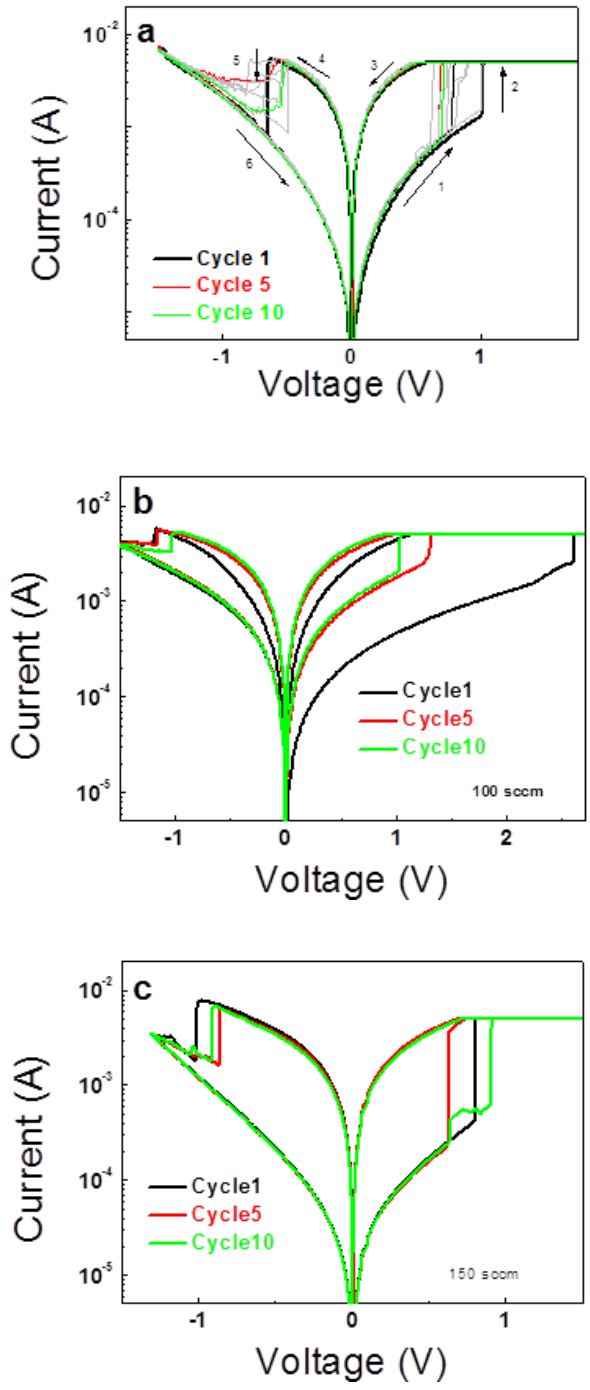


FIG. 13. A series of DC sweep plotted in semi-logarithmic IV shows the bipolar resistive switching characteristics of Pt/ZnO NW/Pt devices with different $O_2$ flow rates: 50 sccm (a), 100 sccm (b) and 150 sccm (c).

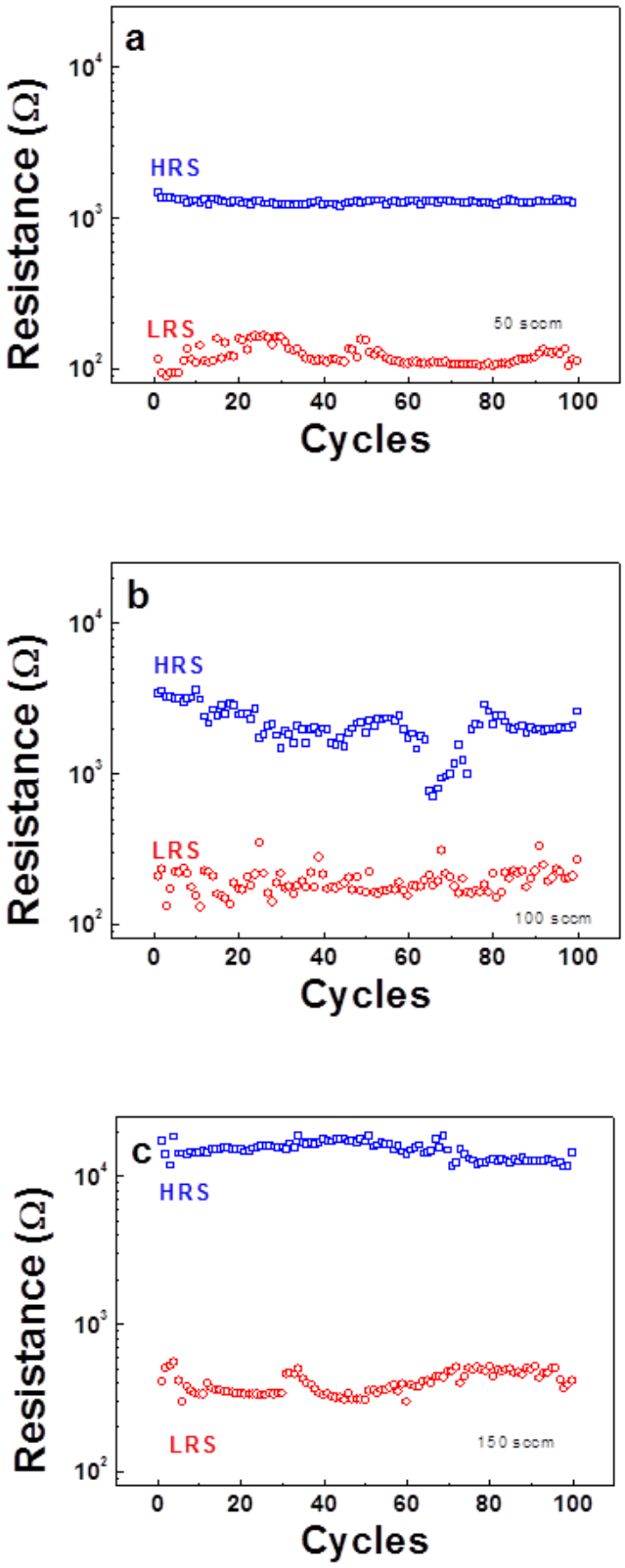


FIG. 14. Resistance characteristics of Pt/ZnO NW/Pt devices for 100 cycles measured at 0.1 V.

The first cycle in Fig. 13b shows that the SET voltage occurs at a higher value around 2.5 V. Although it can be seen that in the succeeding cycles the SET threshold decreases to 1 V, the RESET voltage is found to be around -1 V. Similarly, the device in Fig. 13c has SET voltage around 0.7 V and RESET around 0.8 V.

The stability of resistive bipolar switching of all the devices is also evaluated. The endurance plot presented in Fig. 14 shows the devices in HRS and LRS for 100 cycles. The mean values of HRS for 50, 100 and 150 sccm, respectively are 1.3 kΩ, 2.1 kΩ and 15 kΩ while the mean values of LRS are 120 Ω, 190 Ω and 400 Ω. Some variations in the resistance states can be observed especially in the LRS. There is no significant variation in the HRS values of the 50 and 150 sccm devices while noticeable fluctuation is observed in the 100 sccm device.

The resistance states variation is also investigated in relation to the current compliance. Fig. 15 reports the variation in LRS and HRS values for a set compliance from 5 mA to 15 mA. The value of LRS decreases with the increase in current compliance. On the other hand, there is no noticeable trend in the value of HRS with current compliance. As shown in Fig. 16, the reset current increases in magnitude with the increase in current compliance. Considering a cylindrical structure of the conducting filament, the decrease value of LRS can be attributed to a larger filament cross-section resulting to lower resistivity.[156] This means that the reset current required should be higher to switch the device back to HRS. The compliance-controlled LRS shows that ZnO NW-based device has potential for multistate memristive application.

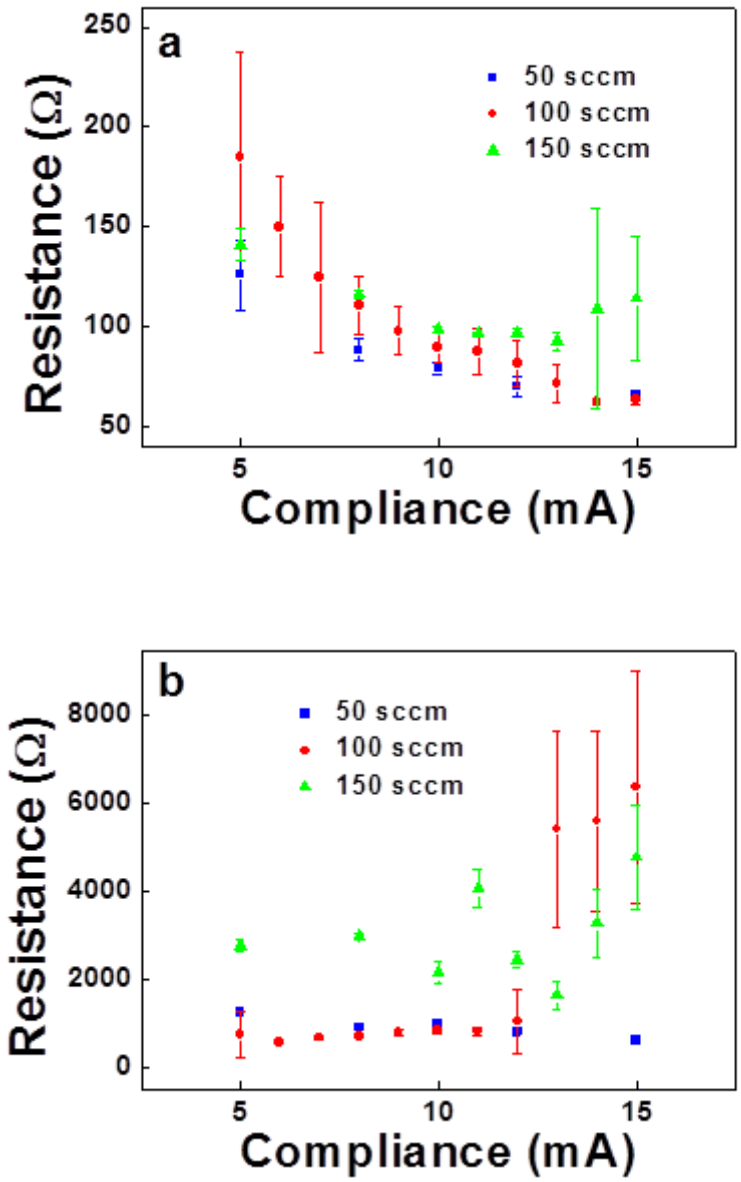


FIG. 15. Variations in devices' resistance states: LRS (a) and HRS (b) with different compliance.

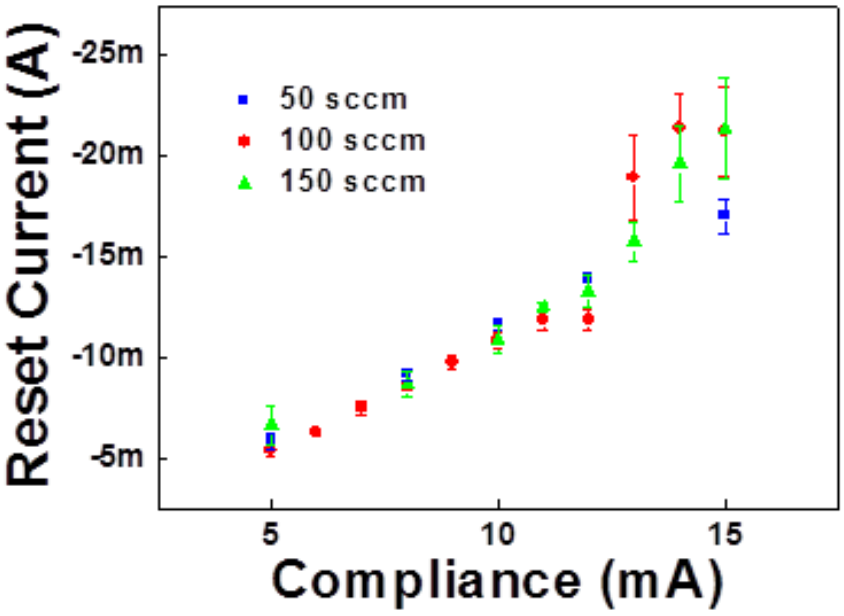


FIG. 16. Linear relation of compliance and reset current.

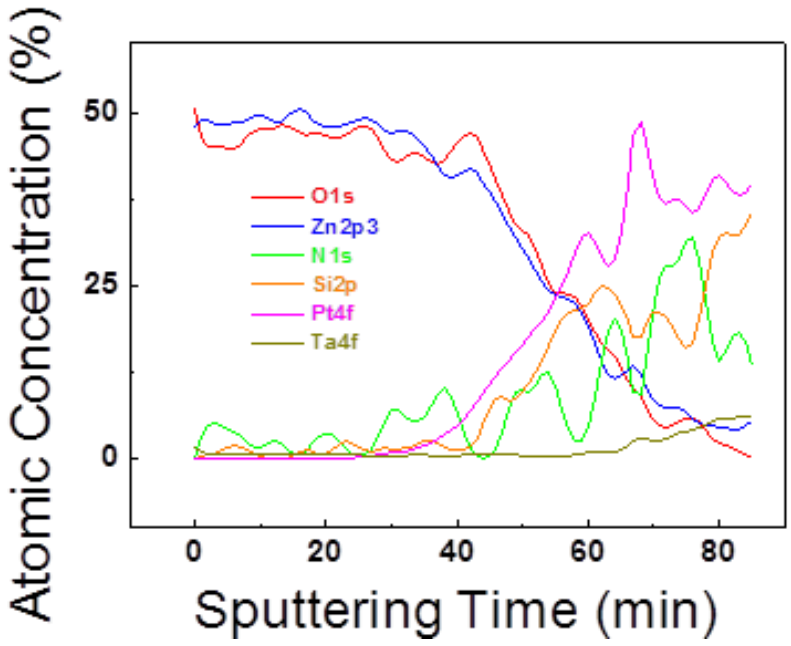


FIG. 17. XPS depth profile of ZnO NW arrays deposited on Si substrate with 150 sccm flow rate.

Fig. 17 reports the XPS depth profile of a representative ZnO NW sample processed at 150 sccm. The approximate surface composition (Zn/O in at. %) of the ZnO NW on Pt/Ta/Si is 51:49. There is a bit more oxygen than Zn content after 40 min of sputtering.

For the next set of devices 150 sccm $O_2$ flow rate is used as the standard recipe. The Pt/ZnO NW/PP/Pt device is reported in Fig. 18. There is an abrupt increase in the conductivity from the pristine state around -2 V voltage bias. The current compliance (CC) is fixed at 10 mA to prevent Joule heating which can permanently damage the device. In order to obtain reversible switching, the voltage sweep range is set to a lower value of ± 1 V and the CC is increased. It can be observed that when the positive voltage sweep has reached about 0.9 V the device is switched OFF or RESET. The device stays in the OFF state until the voltage sweep changes polarity and has reached a value of about -0.5 V wherein the SET process occurs. The OFF state of the device is of lower resistance value compared to the device's pristine state. This can be the result of the irreversible forming process that happened prior to the RS measurement. The bipolar switching endurance reaches up to 25 cycles.

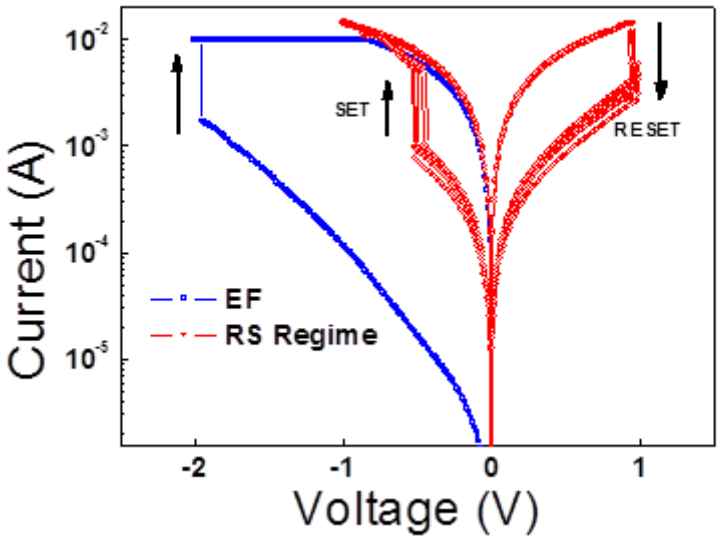


FIG. 18. The bipolar resistive switching characteristics of Pt/ZnO NW/PP/Pt device plotted in semi-logarithmic scale.

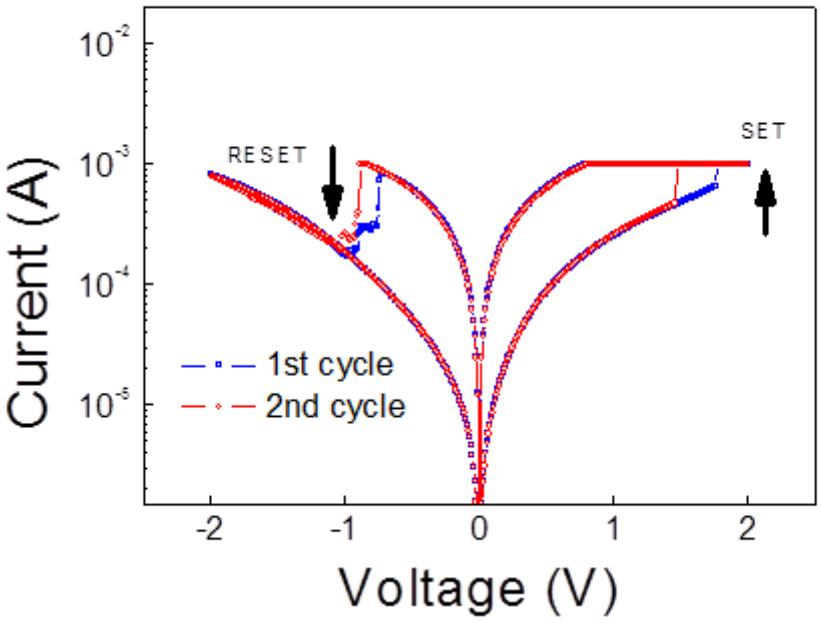


FIG. 19. The bipolar resistive switching characteristics of Cu/ZnO NW/Pt device plotted in semi-logarithmic scale.

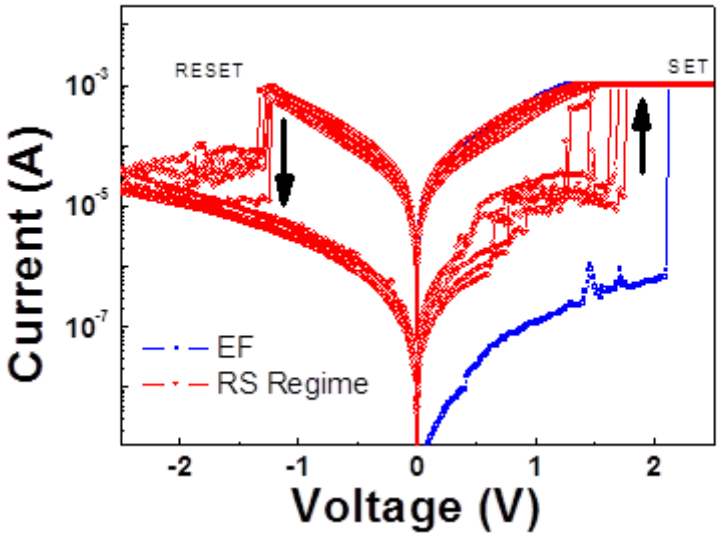


FIG. 20. The bipolar resistive switching characteristics of Cu/ZnO NW/PP/Pt device plotted in semi-logarithmic scale.

The IV characteristics of Cu/ZnO NW/Pt and Cu/ZnO NW/PP/Pt are reported in Fig. 19 and Fig. 20, respectively. Fig. 19 shows the bipolar switching from HRS (7 kΩ) to LRS

(800 Ω) without electroforming process. It can also be observed that the RESET voltage variance for successive cycles is lower when compared to the SET voltage. In Fig. 20, the Cu/ZnO NW/PP/Pt device has a very high resistance in its pristine state ($10^7$ Ω). The CC is set to 1 mA accordingly. Unlike the Pt/ZnO NW/PP/Pt device, the electroforming process here happens in the positive bias around 2 V and the RESET voltage is around -1.3 V. After this process, the device is observed to exhibit stable switching from the high resistance state (700 kΩ) to low resistance state (3 kΩ). Both sets of devices exhibit reversible bipolar switching.

The ON/OFF ratio of the devices are ~$10^2$ (Cu/ZnO NW/PP/Pt) and ~$10^1$ (Cu/ZnO NW/Pt), ~$10^1$ (Pt/ZnO NW/PP/Pt) and ~$10^1$ (Pt/ZnO NW/Pt). The sharp transition from HRS (OFF state) to LRS (ON state) by voltage bias and from LRS to HRS by opposite voltage bias suggests the formation of filaments across the active layer – ZnO NW and core-shell. The current measured through these filaments can be due to Zn interstitials, oxygen vacancies and/or metallic ions. The nature of the dominant carriers for the conduction depends on the electrochemical property of the biased electrode and can be determined based on the polarity of the SET and RESET voltages.

The nonlinear behavior of I with V is also investigated to understand the conduction mechanism in different resistance states. This behavior can have potential application in the neuromorphic processes and learning systems [89]. The double-log scale plots (Fig. 21 and 22) show that at low voltage bias of HRS and LRS, the conduction (slope ~1) obeys Ohm's Law ($I \alpha V$) which suggests the formation of conducting filaments. For the rest of the devices, the HRS conduction exhibit Schottky emission or thermionic emission (linear log I vs $V^{1/2}$). Cu/ZnO NW/PP/Pt device on the other hand, shows a steep portion of the conduction in the high resistance state. This conduction behavior (Fig. 23) can be best described by space charge limited conduction (SCLC) which consists of three parts: Region I (trap-filled limited), Region II (steep slope) and Region III (Child's Law). This mechanism relies on the sub-bands exponentially distributed within the ZnO bandgap. The nonlinearity observed can be attributed to the presence of PPAA layer by: (i) altering the surface states of ZnO NW[157,158] and (ii) forming a high barrier between Cu and ZnO NW as shown by the high PRS value of this device [159–161].

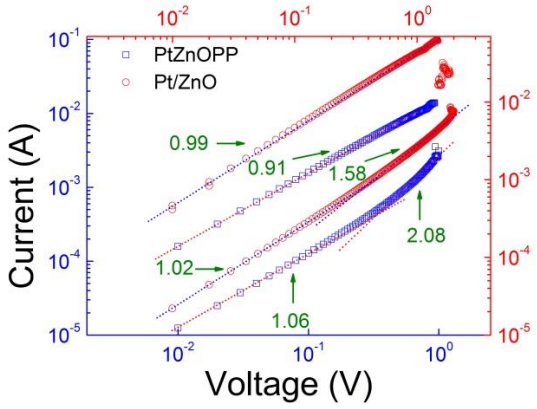


FIG. 21. Line fitting in log-log scale IV characteristics of pure and polymer-coated ZnO NW memristive devices with Pt TE.

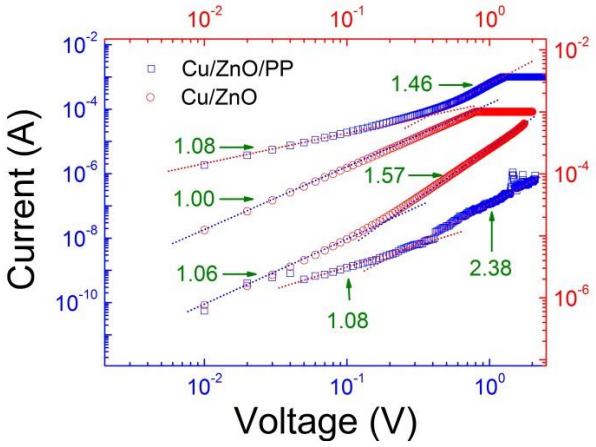


FIG. 22. Line fitting in log-log scale IV characteristics of pure and polymer-coated ZnO NW memristive devices with Cu TE.

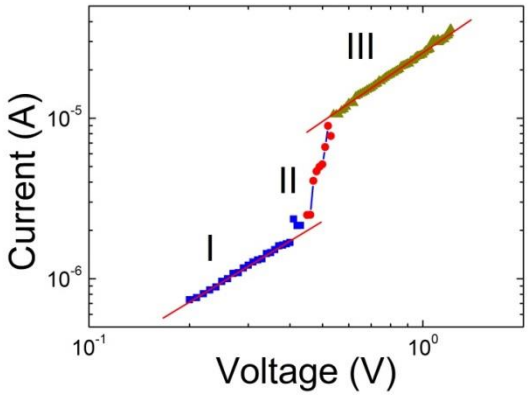


FIG. 23. Three regions of high-field conduction in Cu/ZnO NW/PP/Pt device describing space-charge limited conduction (SCLC) mechanism.

For the Cu/ZnO NW/Pt device, hole injection through the top electrode is more favorable than electron injection. Cu and ZnO NW surface contact has lower barrier height (0.45 eV) than Pt/ZnO NW due to lower work function of Cu (4.65) [155,162]. This indicates that when the top electrode is under positive bias, $Cu^{Z+}$ (Z = 1 or 2) ions diffuse from the top electrode and migrate through the ZnO NW grain boundaries towards the Pt bottom electrode [163]. The conduction is highly field-dependent because the probability that $Cu^{Z+}$ ions recrystallize in the ZnO NW/Pt interface and build up into a chain of conducting filament relies on the polarity, magnitude and duration of the applied bias [30]. The device is now switched to LRS (SET) and it can only be switched to HRS (RESET) under negative bias sufficient enough to dissolve the Cu filaments. This diffusion of $Cu^{Z+}$ ions is totally reversible such that there is no need for electrofoming process. We also use a higher CC (10 mA) on other devices for the first switching cycle and we observed the same value for HRS. The only difference that we observed is the higher RESET current requirement for higher CC. Under this circumstance, the larger area of filament formed needs larger current to dissolve during RESET [164].

The conduction in the ZnO NW-polymer devices is observed to have nonlinear behavior in the high voltage bias. As discussed above, thermionic emission is the dominant conduction mechanism in pure ZnO NW devices regardless of the top electrode used. On the other hand, in Cu/ZnONW/PP/Pt devices the conduction is dominated by SCLC. With the large energy gap between the lowest unoccupied molecular orbital (LUMO) and the highest occupied molecular orbital (HOMO), PPAA becomes a charge blocking layer for $Cu^{Z+}$ ions injection through the ZnO NW layer. If a positive bias is applied to the Cu electrode, the ZnO layer becomes less negative due to screening effect of the PPAA polarization. Thus, the filament formed are expected to be thinner and growing on both in PPAA and ZnO NW layers. This may be the reason why electroforming is still necessary and nonlinearity is observed even in the LRS. There may be differences in the filament growth rate in PPAA and ZnO NW layers due to the differences in the conductivity of the two layers. This can be the reason of the large voltage variance at the onset of trap-filled limited conduction for multiple switching cycles. The operating current (1 mA CC) of these devices is enough that possible modification in the PPAA happens and its insulating property enhances the RS behavior of the device. For the

Pt/ZnO/PP/Pt device, we have not observed the same behavior seemingly because of the higher operating current (10 mA CC) to form vacancies.

## 3.2. $TiO_2$ Thin Films

The discussion on this section is based on the published article cited in the reference.[148] Low temperature ALD processing of $TiO_2$ thin films is explored for the fabrication of memristive devices. ALD can be used for the deposition of amorphous films of high quality and conformal coating. There is a wide selection of substrates where ALD is compatible in terms of area, surface roughness and porosity. The ALD growth conditions can be tuned in a way to accommodate polymeric photoresists prior to the ALD process. This approach eliminates additional patterning techniques by doing the liftoff process immediately after the ALD of $TiO_2$ films. The use of asymmetric electrode namely Pt and Cu, provided another approach of understanding the electrochemical metallization mechanism in the formation of filaments during resistive switching.

### 3.2.1. Thin Film Synthesis and Properties

The layer-by-layer deposition $TiO_2$ is described by the two surface reactions below.[165]

$$n\,(-OH)(s) + TiCl_4(g) \rightarrow (-O-)_n TiCl_{4-n}(s) + HCl(g) \quad (12)$$

$$(-O-)_n TiCl_{4-n}(s) + (4-n)H_2O\,(g) \rightarrow (-O-)_n Ti(OH)_{4-n}(s) + (4-n)HCl(g) \quad (13)$$

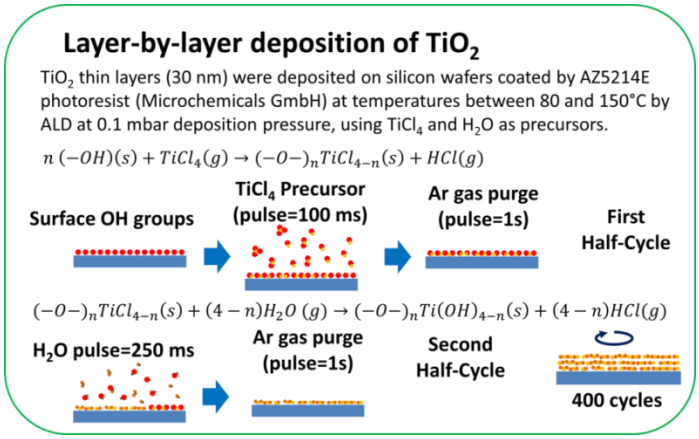


Fig. 24. Typical surface reactions during one ALD cycle of $TiCl_4$ and $H_2O$ pulsing.

In the first-half cycle, $TiCl_4$ reacts with the surface OH molecules releasing HCl after the reaction. In the second half-cycle, $H_2O$ vapor is introduced to the reaction. Surface $TiCl_{4-n}$ reacts with $H_2O$ molecules releasing another HCl molecule as by-product. At the end of the second-half cycle, OH species are now readily available for the next ALD cycle. Moreover, it takes several ALD cycles to completely achieve fully-coated substrate and constant ALD cycle.

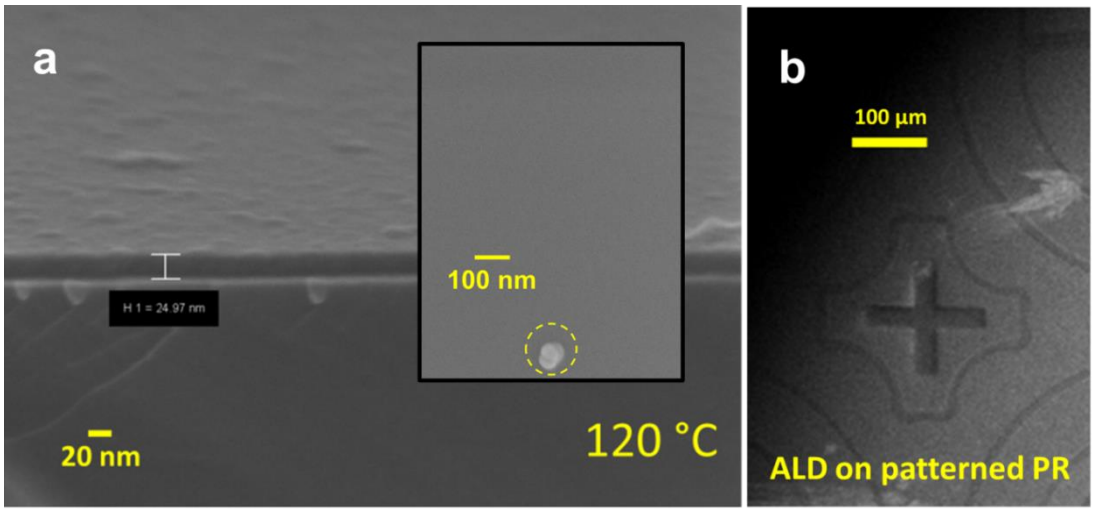


FIG. 25. FESEM image of ALD $TiO_2$ thin film on Si substrate deposited at 120 °C (a) and effective DMSO liftoff of ALD $TiO_2$ thin films on patterned PR (b).

$TiO_2$ films by ALD showed continuous and smooth morphology in the deposition temperature selected for this study. Fig. 25a shows a cross-section image of a film deposited at 120 °C on Si. It shows uniform thickness and homogeneous morphology from the initial ALD cycles (bottom) up to the end of the ALD process. All films deposited from 80 to 140 °C show smooth surface morphology. Excellent mechanical liftoff process is also possible in this process temperature range. This is shown by the well-defined patterns on the $TiO_2$ films after the lift off (Fig. 25b). It can be inferred from these results that in this ALD window, the polymeric PR does not degrade during the ALD process.

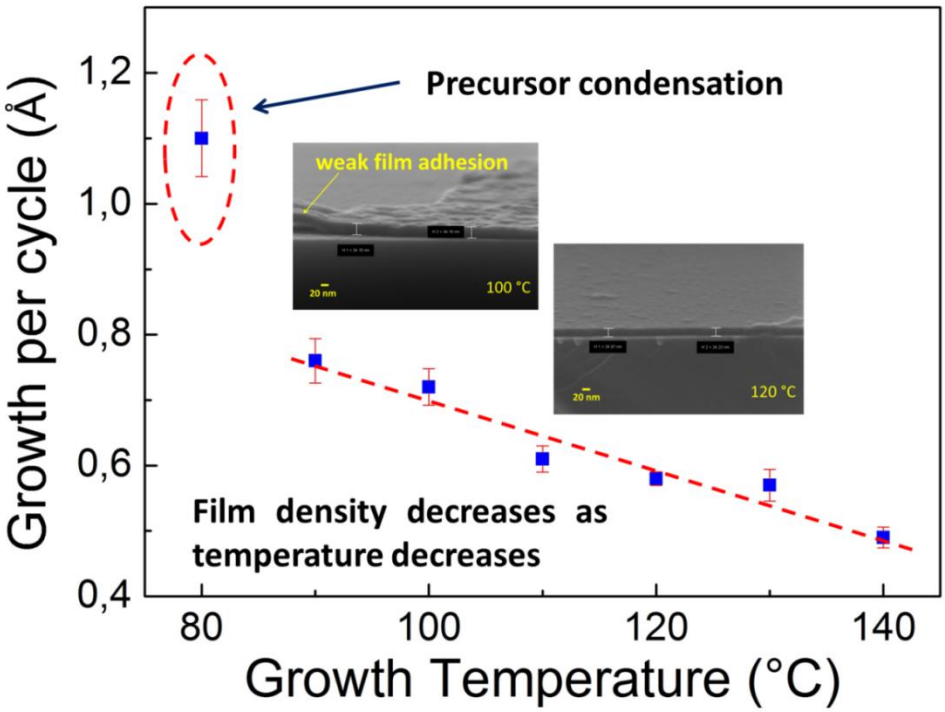


FIG. 26. Growth rate of $TiO_2$ films shows decreasing trend as temperature increases.

The growth rate per cycle (GPC) for a particular ALD process temperature was also calculated. Thickness was measured in the acquired FESEM images and divided it by number of ALD cycles. In Fig. 26, the GPC value from 90 to 140°C is less than 0.8 Å/cycle. The GPC for 80 °C is 1.1 Å/cycle. This value is much higher than what is expected in a typical ALD. There are two possible reasons for the observed increase in GPC: (i) condensation and (ii) incomplete surface reaction. During low temperature ALD processing, H-bonded OH groups dominate the surface exchange reaction. Condensation of H-bonded OH occurs, thereby increasing the number of reactive sites. In this situation there is a possibility that more precursor species participate in the ALD half-reaction beyond the surface saturation. Moreover, the presence of $H_2O$ vapor at 80 °C depends solely on the partial pressure and not on the reactor temperature. Considering these observations, only thin films prepared at 120 °C or higher were considered for device fabrication.

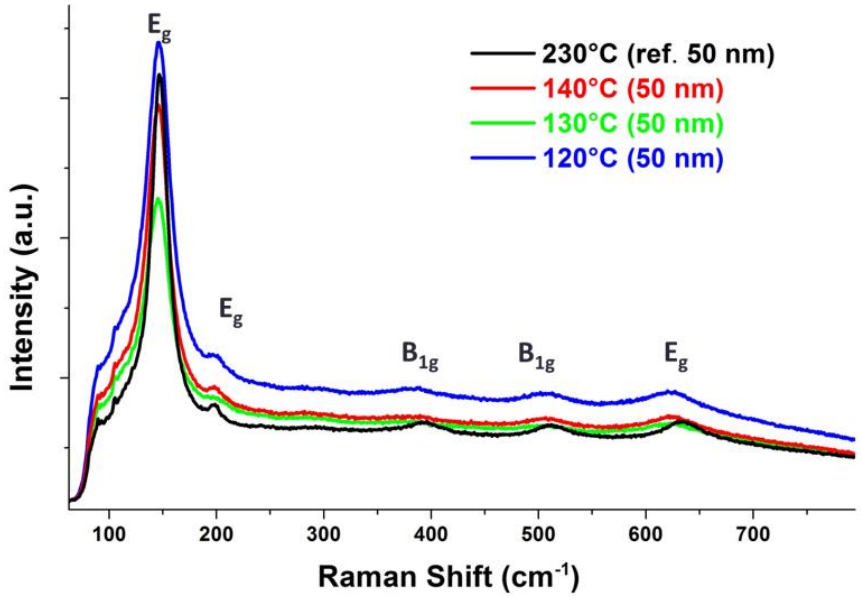


FIG. 27. Raman spectra of TiO2 thin layers on Pt deposited at 120 °C to 230 °C.

Raman spectroscopy was performed on 50-nm $TiO_2$ thin layers deposited at 120, 130, 140 and 230 °C (Fig. 27). The prominent peaks at 144, 197 and 639 $cm^{-1}$ are assigned to $E_g$ mode. The peaks at 399 and 519 $cm^{-1}$ are assigned to the $B_{1g}$ mode. All the peaks seen in the spectra corresponds to the anatase phase of $TiO_2$. The peak at 144 $cm^{-1}$ is significantly sharper than the rest of the peaks. It is worthwhile to note that we can obtain such a sharp peak even at a very low process temperature. Previous work reported weak signal from this Raman line for films grown at 150 °C and 175 °C and it is only expected to increase around 200 °C.[166] Raman peaks (not shown) observed from thicker samples (500 nm) exhibit sharper features. This can be correlated to the formation of larger grains and higher surface roughness of the film.

### 3.2.2. Device Characterization

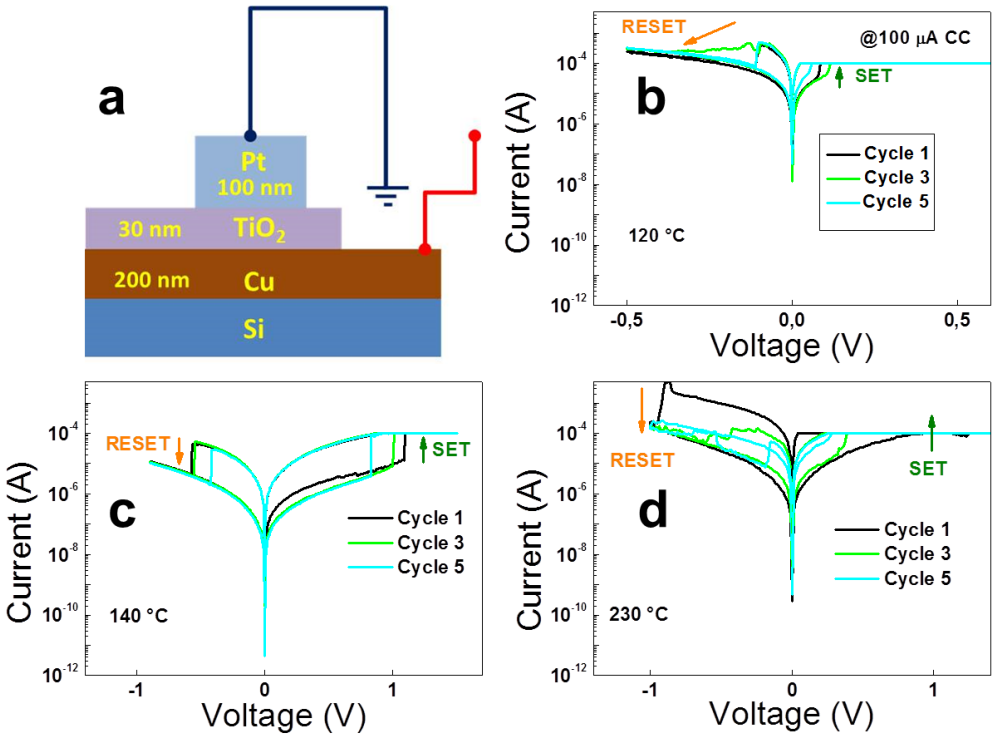


FIG. 28. Schematic diagram of the Cu/$TiO_2$/Pt devices (a) semi-logarithmic I-V curves of devices with $TiO_2$ grown at 120 (b), 140 (c) and 230°C (d), showing the first 5 memristive cycles. The devices work in bipolar resistive switching.

Electrical characterization of the fabricated Cu/$TiO_2$/Pt devices was conducted in dc sweep configuration (Fig. 28a). The Cu electrode is connected to the dc bias while the Pt electrode is grounded. The scan rate and current compliance were fixed at 10 mV/s and 100 µA, respectively. Fig. 28b-28d shows the bipolar switching characteristics of the Cu/$TiO_2$/Pt devices. The pristine resistance state of the devices was measured to be around $10^6$ to $10^7$ Ω. After device electroforming was performed in the positive bias, successive SET and RESET processes were done. From the IV curve, the resistance state values were extracted from the voltage regime by taking the current at 10 mV. The ON/OFF ratio of the devices are 9, 23 and 17 for 120, 140 and 230 °C, respectively.

These values do not differ much with each other. Device-to-device resistance state values may vary but the ON/OFF ratio has no significant change.

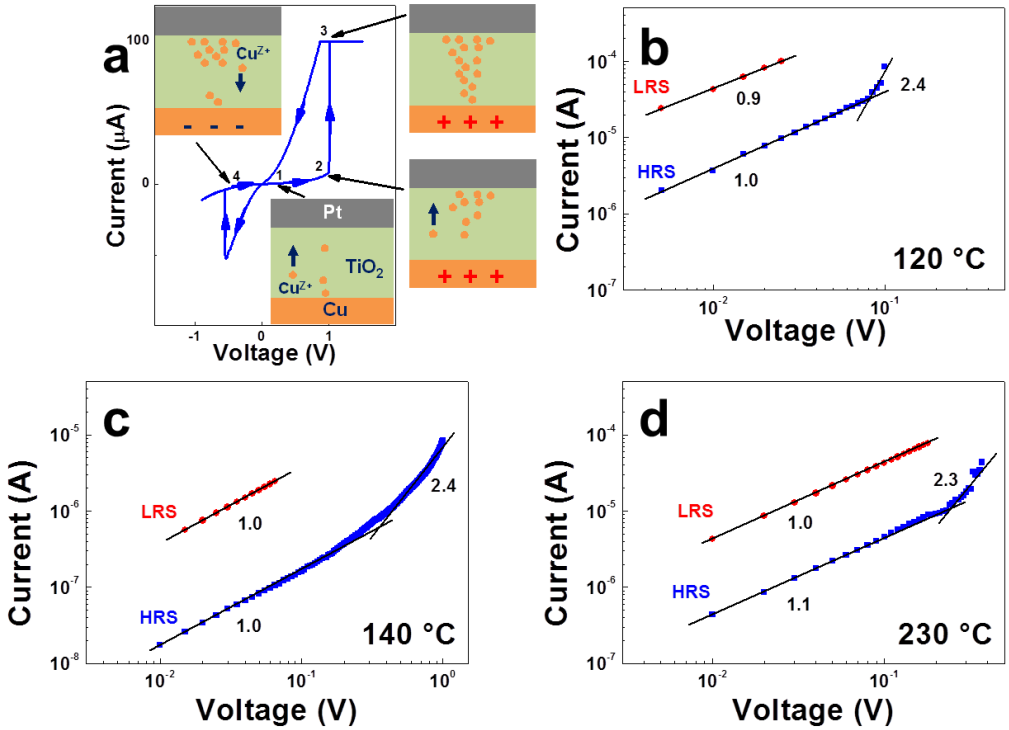


FIG. 29. Schematic diagram of the Cu/$TiO_2$/Pt devices showing the filament formation and rupture that happens in one cycle (a) double-logarithmic I-V curves of devices with $TiO_2$ grown at 120 (b), 140 (c) and 230°C (d) showing the two resistance states.

The use of an active metal as an electrode for the memristive devices alters the possible concentration of ions during filament formation. Cu ions can migrate through the $TiO_2$ layer toward the Pt electrode with sufficient electric field applied. This results to the accumulation of Cu ions until the threshold voltage ($V_{EF}$) induces the creation of continuous ion channel connecting the two electrodes (Fig. 29a). It can be observed that the HRS has a lower value than the pristine resistance state. This indicates that the RESET process is not able to completely dissolve the conducting filaments.

The double-logarithmic plots show linear relation of I and V for LRS of all the devices (Fig. 29b-29d). In this case, the conduction is mostly from the conducting filaments. Since the filaments contain metallic Cu ions, the conduction obey Ohm's Law ($I \alpha V$).[20,167] In a similar manner, the double-log plot of HRS describes nonlinear relation of I and V. When the device is in the OFF state, the behavior obeys space charge-limited

conduction (SCLC) mechanism. SCLC is described by two conduction mechanisms namely: (a) Ohmic conduction in the low voltage regime and (b) Schottky emission ($I \alpha V^2$) in the high voltage regime.

More simple device fabrication process can now be done by performing direct ALD of $TiO_2$ on pre-patterned polymeric photoresist and subsequent liftoff process. $TiO_2$ films grown by low-temperature ALD using $TiCl_4$ and $H_2O$ exhibit smooth and uniform layers suitable for memristive device fabrication. The growth rate below the ALD window increases with decreasing ALD reaction temperature. High film growth rate results in less dense films and more possible local defects. The Raman spectra of $TiO_2$ films deposited at low temperature show features of $TiO_2$ in the anatase phase. XPS analysis shows similar composition and stoichiometry of the $TiO_2$ layers at different ALD temperatures. Fabricated memristive devices show stable bipolar resistive switching. The LRS obeys Ohmic behavior suggesting the presence of metallic filaments. On the other hand, HRS follows SCLC mechanism as shown by the nonlinear IV at higher voltage. Some deviations in the device resistance states are affected by the applied voltage bias but the ON/OFF is not significantly changed. This means that the low-temperature ALD $TiO_2$ devices perform very well when compared to the standard ALD devices. The advantage of performing low-temperature ALD on pre-patterned polymeric substrates is the possibility of fabricating multilayer devices composed of layers with different etching rates where conventional etching process cannot be done.

## 3.3. $Fe_2O_3$ Thin Films

Iron oxide ($\alpha$-$Fe_2O_3$) thin films were fabricated on Pt/Ta/$SiO_2$/Si substrate by atomic layer deposition (ALD) technique using ferrocene and ozone as precursors. As-prepared thin films have shown smooth morphology and good crystallinity owing to the excellent control of ALD precursors by using micro-pulses. The film crystallinity was affected by post-deposition annealing due to the formation of new oxide phases. The resistive switching of fabricated $\alpha$-$Fe_2O_3$ thin film devices showed bipolar mode with good stability and endurance. Multistate switching was achieved via current and voltage control. It was found that the ON state regime can be tuned by changing the current compliance while the OFF state can be changed to intermediate levels by decreasing the maximum voltage during reset.

### 3.3.1. Thin Film Synthesis and Properties

This section will report the synthesis and characterization ALD $Fe_2O_3$ thin films on $Si/SiO_2/Ta/Pt$ substrate and their memristive application. Using ferrocene ($FeCp_2$) as iron (Fe) precursor and ozone ($O_3$) as oxygen source, pure $Fe_2O_3$ phase thin film is obtained. Electrical characterization was performed to determine the effect of voltage and compliance current to the multilevel resistance states. This section will also present a description of the filament dynamics during switching to assess the feasibility of using Fe-O material system for memristive application.

Standard Si with $SiO_2$ native oxide layer were used. Ta/Pt (100 nm) electrodes were deposited by sputtering and used as growth interlayer for ALD. Ferrocene ($Fe(C_5H_5)_2$ or $FeCp_2$) and ozone ($O_3$) were used as iron precursor and oxidation source, respectively. The $FeCp_2$ hot source was heated prior to deposition and all the ALD processes were conducted at a substrate temperature of 250°C. Due to low growth rate of ALD for $Fe_2O_3$, $FeCp_2$ dose was introduced to the reactor using micro-pulses as described in the reference.[144] The ALD reactor is maintained at 1.8 mbar under constant flow of inert gas before starting the ALD process. During the precursor dosing, the feeding pressure readings are 75 mbar and 6 mbar for $FeCp_2$ and $O_3$ half-cycles, respectively. For each ALD cycle, the total precursor dose is 30 s for $FeCp_2$, 10 s for $O_3$ and 20 s for $N_2$ purging in between to avoid precursor overlap and to remove excess gaseous by-products. It takes 400 ALD cycles (100 micro-pulses/cycle) to achieve a film thickness of 30 nm. The morphology of the samples was evaluated using FESEM ZEISS Auriga. The chemical composition of the samples was determined by x-ray photoelectron spectroscopy (XPS). For the structural characterization, two sets of samples were analyzed by Raman spectroscopy as-prepared and annealed samples. The samples were annealed in vacuum with constant flow of Ar gas at 400 °C for 3 h. For the fabrication of memristive devices, a thin Pt layer (200 nm) was deposited on top of $Fe_2O_3$ layer by sputtering using a hard mask to obtain circular patterns for the top electrode. Finally, wet etching was done to expose the bottom electrode for electrical contact. The electrical measurement of the devices was conducted in a two-point contact probe station connected to Keithley 4200-SCS parameter analyzer.

SEM images of as-deposited samples are depicted in Fig. 30. In Fig 30a, the film shows uniform growth with grain dimension about 15 nm. Fig. 30b shows the film morphology near the substrate edge suggesting non-uniform growth. However, secondary electron analysis image (inset) shows homogeneous and smooth topography throughout the film surface. Fig 30c reports the cross-section image of the different layers of the substrate coated with $Fe_2O_3$. From thickness measurement, the $Fe_2O_3$ growth rate is about 0.78 Å/cycle which is typical with standard ALD processes. We also conducted another set of experiments by decreasing the number of micro-pulses to 5 cycles while increasing the pulse duration to 1.5 s and maintaining the same number of ALD cycles. The results show the deposition of nanoparticles instead of homogeneous thin film coverage of the substrate. Although the original micro-pulse recipe takes a longer time than other conventional deposition techniques, the precursor reaction inside the ALD chamber is more controllable. Substrate exposure to precursors using short pulses (100 ms) provides longer residence time and more homogeneous diffusion all throughout the substrate surface.

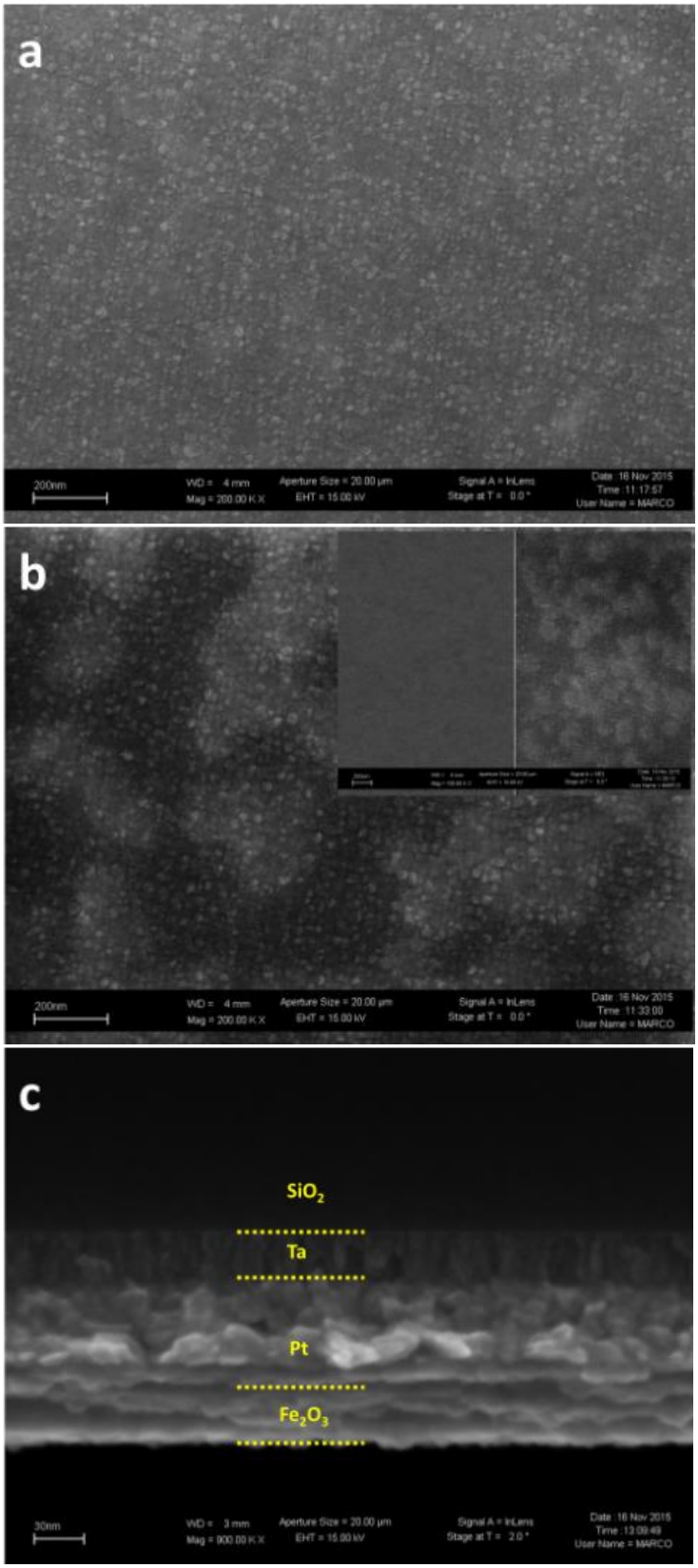


FIG. 30. SEM top view at the center (a) and edge (b) of the sample, and cross-section view (c) of $Fe_2O_3$ thin films deposited on Pt/Ta/$SiO_2$/Si substrate for 400 cycles.

The as-prepared samples exhibit good crystallinity based on the sharp peaks of the Raman measurements. Fig. 31a shows peaks for $E_{1g}$ vibrational modes at 247, 295, 405, 603 and 1305 $cm^{-1}$ for hematite ($\alpha$-$Fe_2O_3$). Another set of samples was annealed at 400°C in vacuum (300 sccm Ar flow) for 3 h. In Fig. 31b, the Raman peak at 668 $cm^{-1}$ is typical for $A_{1g}$ vibrational mode of magnetite ($Fe_3O_4$) phase and the peak at 350 $cm^{-1}$ for $\gamma$-$Fe_2O_3$ phase.[168,169] There is a noticeable peak broadening in the 630-800 $cm^{-1}$ and 1510-1650 $cm^{-1}$ regions where the $\gamma$-$Fe_2O_3$ peak contribution can be considered, namely 720 $cm^{-1}$ and 1580 $cm^{-1}$. The asymmetry observed at 1305 $cm^{-1}$ peak can be due to another $\gamma$-$Fe_2O_3$ peak located at 1420 $cm^{-1}$. This means that the decrease in the overall crystal quality of the as-prepared film as shown in the Raman spectra may be due to the formation of $\gamma$-$Fe_2O_3$ at the expense of $\alpha$-$Fe_2O_3$. There is also a slight shift of the Raman peaks of the annealed compared to as-prepared sample which can be attributed to the stress present in the film due to the formation of other Fe-O phases.

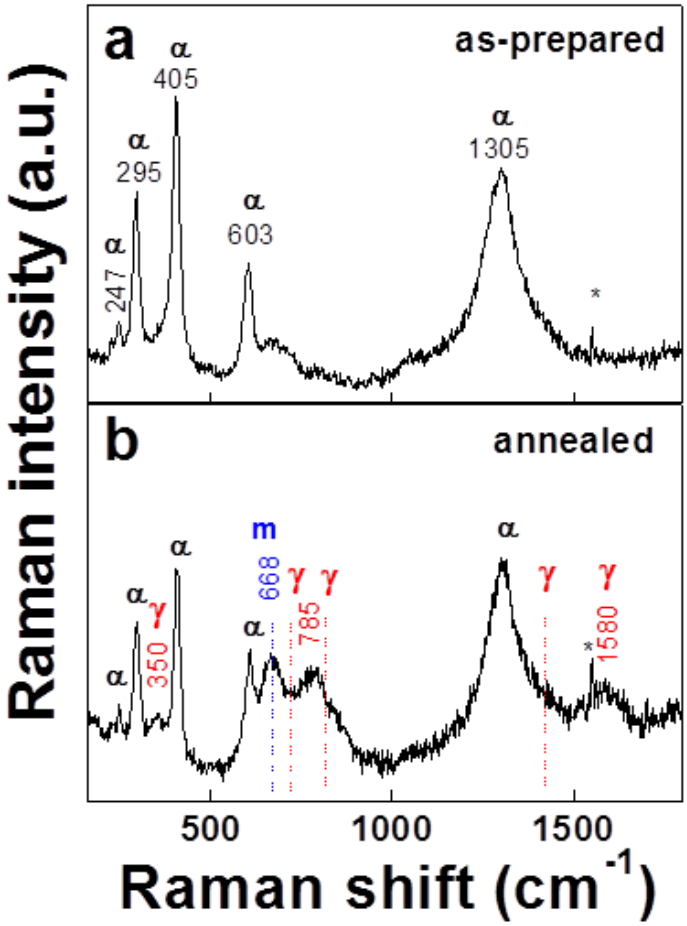


FIG. 31. Raman spectra of as-prepared (a) and annealed (b) $Fe_2O_3$ thin films deposited by 400 ALD cycles.

The chemical composition of $Fe_2O_3$ thin film was investigated via XPS technique to determine the oxide phases present in the samples. Fig. 32a shows the XPS survey spectrum of as-prepared sample. The XPS spectrum has sharp peaks assigned typically to iron and oxygen. C contamination is also evident as this can't be avoided in the sample preparation. The depth profile analysis of the film (Fig. 32b) shows approximately a 40:60 ratio of Fe and O for the Fe oxide layer at the surface. Fig. 32c and 32d show the high resolution scans for O1s and Fe2p core levels. From the Gaussian fitting of O1s spectra, two peaks are observed at 530 and 531 eV. On the other hand, high resolution scan between 707 and 737 eV presents stronger peak for $Fe2p_{3/2}$ at

~710 eV than that of $Fe2p_{1/2}$ at ~724 eV. The satellite peaks assigned for $Fe2p_{3/2}$ and $Fe2p_{1/2}$ can be seen at ~724 and ~732 eV, respectively. The peak characteristics of the core levels are consistent with what is in the literature[170,171]. This also confirms the presence of $Fe_2O_3$ phase in the film and the absence of other iron oxide phases.

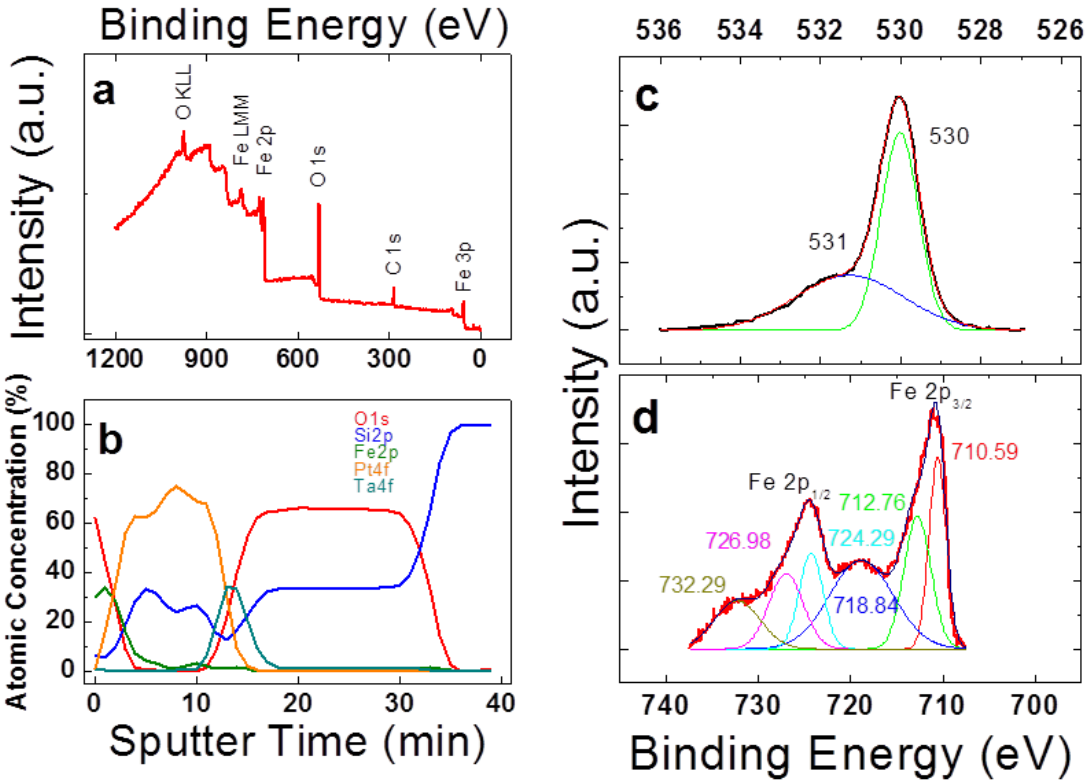


FIG. 32. XPS spectra of $Fe_2O_3$ thin films: survey spectrum (a), depth profile (b) and high resolution spectra of O1s (c) and Fe2p (d).

### 3.3.2. Device Characterization

Memristive devices were fabricated in order to investigate the electrical properties and to demonstrate other potential applications of the developed $Fe_2O_3$-based thin films. Based on the device architecture shown in Fig 33a, cyclic DC sweep was performed on the devices. The pristine state of the device is about $10^4$ Ω. The device was formed in the negative bias. Hundreds of dc cycles were performed for each device to test the write/erase endurance before performing measurement for different compliance. The

measured resistive switching was stable for many cycles as represented by the switching endurance in Fig. 33b. The hysteretic I-V loops measured in cycles 1, 15 and 20 are reported in Fig. 33c. The ON/OFF ratio is around 10 which is normally expected for a thin oxide layer having a large electrode. The observed resistive switching in oxide thin films is best explained by the mechanism involving growth and rupture of conductive filaments during SET and RESET, respectively. The compliance current was varied from 500 µA to 10 mA to determine its effect on the device resistance states. For each compliance value, 20 dc sweep cycles were performed and the resistance state value was read at 0.1 V. Fig. 33d shows that the compliance does have a slight effect in the high resistance state (HRS) especially in lower compliance current values, while it has a more significant influence in the low resistance state (LRS). Moreover, the reset current also tends to increase in magnitude with compliance. The apparent decrease in the LRS could be due to the increase of filament cross-section with compliance. Thus, once the device is in the ON state, and one tries to do a device reset, a larger amount of current is needed in order to rupture the filament.

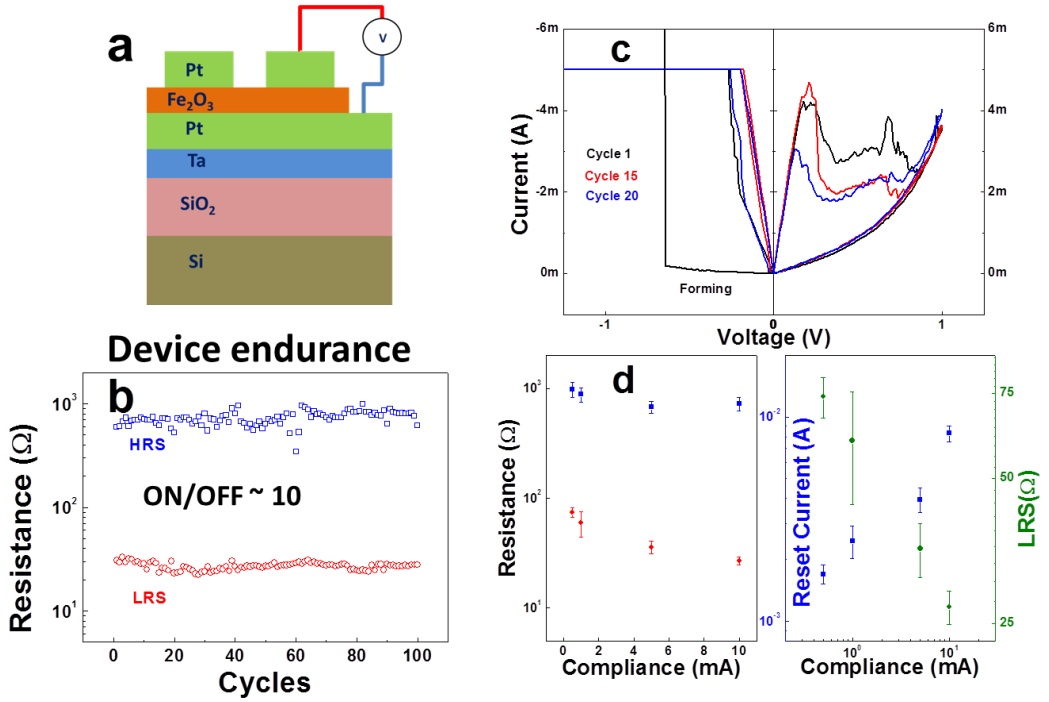


FIG. 33. Device diagram (a), cyclic I-V characteristics (b), switching endurance (c) and resistance states vs compliance current plot of $Fe_2O_3$ device.

It can be observed that there is a smooth transition from LRS to HRS during reset. There are no noticeable changes in HRS between 0.9 V and 1 V. In order to determine the effect of reset voltage with the HRS value, the bias voltage is varied from 300 mV to 900 mV while maintaining the current compliance at -5 mA. Fig. 34 reports the I-V characteristics of the device during reset. Starting from 300 mV, the HRS value increases with the reset voltage. The LRS value does not change that much as the HRS value with voltage. The gradual reset process facilitates the possibility of obtaining a resistance value different from the HRS in bipolar switching. This value depends on the chosen maximum voltage in the positive bias. The voltage-dependent reset process is mainly due to the rupture of the conducting filament by Joule effect and redox reaction. This phenomenon depends on the strength and duration of the applied bias.[42,172] The resistance obtained during the reset depends on how much the filament has been ruptured. Fig. 34c and 34d show the nature of the filament during set and reset processes, respectively. It appears that by increasing (decreasing) the compliance current during set process, the amount of vacancies increases (decreases), thus a larger filament cross-section. On the other hand, by decreasing (increasing) the maximum bias during reset, the rupture length decreases (increases). Intermediate LRS can be obtained by choosing the appropriate compliance, while intermediate HRS can be obtained by setting the maximum voltage. By taking into consideration that Joule heating happens when high current is reached (electroforming), we can infer that some modification of the $\alpha$-$Fe_2O_3$ structure occurs. Although not as significant to detect Raman signal as the new Fe-O phases shown in Fig. 19b, it is a possibility that the localized heating effect may form nano-phases of $\gamma$-$Fe_2O_3$ or $Fe_3O_4$, which is more conductive than $\alpha$-$Fe_2O_3$.[173] Similarly, Raman spectroscopy study of planar devices[174] suggests the localized redox reaction of $Fe_3O_4$ to $\gamma$-$Fe_2O_3$ in the oxide-electrode interface during resistive switching.

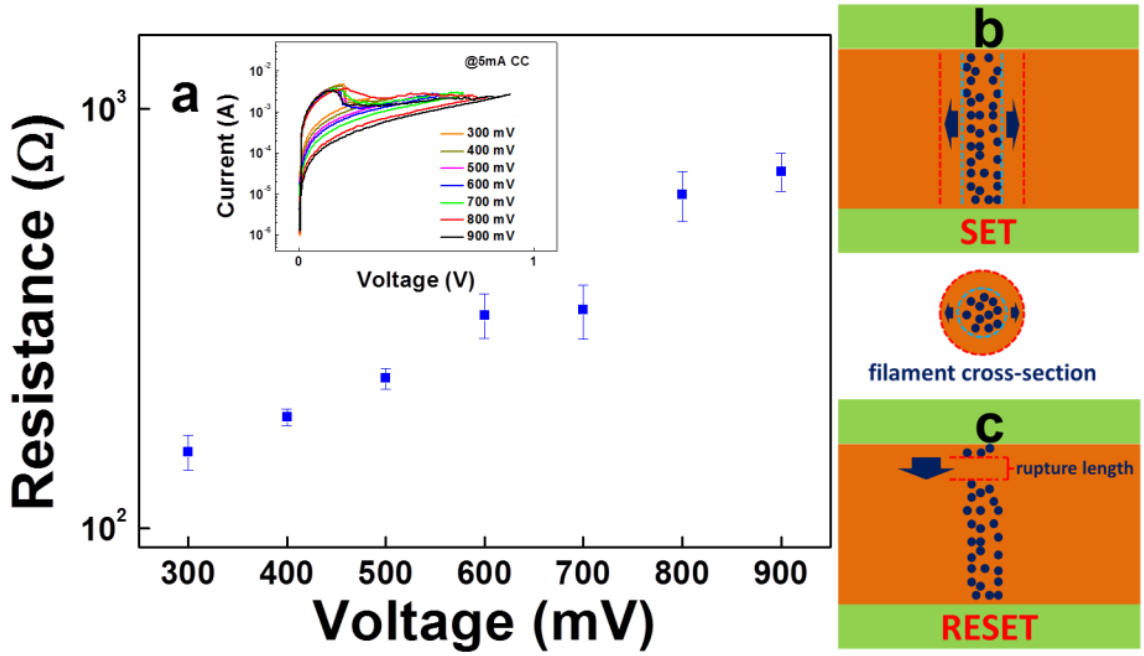


FIG. 34. HRS vs voltage (a) and I-V characteristics (inset) of the device, filament dynamics during set (b) and reset (c) processes.

$Fe_2O_3$ thin films of homogeneous and smooth surface morphology can be obtained by ALD using cyclic micro-pulses of $FeCp_2$ and $O_3$ precursors. Although the process takes a longer time than conventional deposition techniques, the growth rate is much more controlled which is very advantageous for high aspect ratio deposition. Introducing precursors in short pulses provides longer residence time and more homogeneous diffusion throughout the substrate. Also, this approach prevents CVD-like reaction because of more favorable surface absorption. The ALD process temperature as low as 250°C can easily produce phase pure $Fe_2O_3$ thin films with good crystallinity. It was demonstrated that at low ALD process temperature pure phase iron oxide can be obtained as confirmed by XPS. Based on the Raman measurement results of annealed samples, the formation of other phases of $Fe_2O_3$ seems to degrade the crystal quality of as-prepared samples.

# 4. Conclusion

In this thesis, three oxide materials were studied for memristive device applications. LPCVD and ALD were used for the growth of ZnO NW, $TiO_2$ and $Fe_2O_3$ thin films. Device fabrication and characterization were done to determine the memristive behavior of each oxide material.

**ZnO NW**. LPCVD has been shown to be an effective deposition technique for the synthesis of vertically ZnO NW with good repeatability and controllability. The unique configuration of ZnO NW allows structure-dependent growth of filaments along the NW geometry resulting in a more stable resistance state variation. The formation-annihilation of conducting filaments is the dominant mechanism of switching. In pure ZnO NW memristive devices, the LRS changes inversely with compliance owing to the widening of the filament cross-section. This is also compensated by the larger reset current during LRS to HRS transition. The Cu electrode used for the asymmetric devices provides lower operating current mainly because of the lower barrier height as compared to Pt electrode devices. Coating ZnO NWs with PPAA (polymer) enhances the nonlinearity of the IV characteristics by modifying the surface states of ZnO NW. As a consequence, operating power of the device is lower. Such device has lesser susceptibility to heating.

**$TiO_2$ thin films**. The low-temperature ALD on pre-patterned polymeric substrates allows the possibility of fabricating memristive devices using simpler methods where conventional etching process cannot be done. It was demonstrated that performing direct ALD of $TiO_2$ on pre-patterned polymeric photoresist and subsequent liftoff process does not affect the overall performance of the fabricated devices. Although the ideal ALD has the possibility of being compromised at extremely low temperature processing, standard thin film treatments like post annealing and plasma exposure are readily available once a better film quality is desired for specific application.

**$Fe_2O_3$ thin films.** Micro-pulsing technique in ALD is another approach in coating high aspect ratio substrates. Utilizing this technique in $Fe_2O_3$ thin film processing enables us to obtain homogeneous thin films of high phase purity. The ease of obtaining phase pure oxide films by ALD together with localized redox reaction to induce stable resistive

switching makes fabrication of Fe-O based memristive devices more feasible and scalable. Considering the device performance of $Fe_2O_3$ devices, the compliance current affects the reset current and LRS of the device owing also to the increased effective cross-section of the conducting filament. Similarly, the maximum voltage for the reset process alters the HRS of the device depending on the partial dissolution or rupture of the conducting filament.

The sharp transition observed SET and RESET process shows that the filament dynamics is the dominant mechanism responsible for the memristive behavior of the fabricated oxide memristive devices. We conclude that resistance states can be controlled based on the input current or voltage during DC sweep characterization. This approach can be utilized for multilevel resistance switching applications.

Further investigation is recommended in the following aspects of this study:

- The role of ZnO thin film in the resistive switching of ZnO NW devices
- In situ characterization of memristive effect in single ZnO NW devices
- Implementation of low temperature ALD in flexible substrates
- Implementation of memristive networks using crossbar architecture
- Pulsed IV characterization of memristive devices

## Bibliography


1. Chua, L. Memristor-The missing circuit element. *IEEE Transactions on Circuit Theory* **CT-18,** (1971).

2. Strukov, D. B., Snider, G. S., Stewart, D. R. & Williams, R. S. The missing memristor found. *Nature* **453,** 80–3 (2008).

3. Baldi, L. & Sandhu, G. Emerging memories. *2013 Proceedings of the European Solid-State Device Research Conference (ESSDERC)* **102,** 30–36 (2013).

4. Riggert, C., Ziegler, M., Schroeder, D., Krautschneider, W. H. & Kohlstedt, H. MemFlash device: floating gate transistors as memristive devices for neuromorphic computing. *Semiconductor Science and Technology* **29,** 104011 (2014).

5. Yang, J. J., Strukov, D. B. & Stewart, D. R. Memristive devices for computing. *Nature nanotechnology* **8,** 13–24 (2013).

6. Thomas, A. Memristive devices. *Semiconductor Science and Technology* **29,** 100301 (2014).

7. Fröhlich, K. TiO2-based structures for nanoscale memory applications. *Materials Science in Semiconductor Processing* **16,** 1186–1195 (2013).

8. Lu, W. & Lieber, C. M. Nanoelectronics from the bottom up. *Nature Materials* **6,** 841–850 (2007).

9. Massimiliano, B., Ventra, D., Pershin, Y. V & Chua, L. O. Circuit Elements With Memory : and Meminductors. *Proceeding of the IEEE* **97,** 1717–1724 (2009).

10. Sawa, A. Resistive switching in transition metal oxides. *Materials Today* **11,** 28–36 (2008).

11. Verderber, R. R., Simmons, J. G. & Eales, B. Forming process in evaporated SiO thin films. *Philosophical Magazine* **16,** 37–41 (1967).

12. Simmons, J. G. & Verderber, R. R. New Conduction and Reversible Memory Phenomena in Thin Insulating Films. *Proceedings of the Royal Society A: Mathematical, Physical and Engineering Sciences* **301,** 77–102 (1967).

13. Dearnaley, G., Stoneham, A. M. & Morgans, D. V. Electrical phenomena in amorphous oxide films. 1129–1191 (1970).

14. Simmons, J. G. Generalized Formula for the Electric Tunnel Effect between Similar Electrodes Separated by a Thin Insulating Film. *Journal of Applied Physics* **34,** 1793–1803 (1963).

15. Simmons, J. Poole-Frenkel Effect and Schottky Effect in Metal-Insulator-Metal Systems. *Physical Review* **155,** 657–660 (1967).

16. Yang, J. J. *et al.* Memristive switching mechanism for metal/oxide/metal nanodevices. *Nature Nanotechnology* **3,** 429–33 (2008).

17. Hu, W. *et al.* Bipolar and tri-state unipolar resistive switching behaviors in Ag/$ZnFe_2O_4$/Pt memory devices. *Applied Physics Letters* **101,** 63501 (2012).

18. Waser, R. & Aono, M. Nanoionics-based resistive switching memories. *Nature Materials* **6,** 833–40 (2007).

19. Liu, T., Verma, M., Kang, Y. & Orlowski, M. Volatile resistive switching in Cu/TaOx/δ-Cu/Pt devices. *Applied Physics Letters* **101,** 073510 (2012).

20. Tsuruoka, T., Terabe, K., Hasegawa, T. & Aono, M. Forming and switching mechanisms of a cation-migration-based oxide resistive memory. *Nanotechnology* **21,** 425205 (2010).

21. Rahaman, S. *et al.* Excellent resistive memory characteristics and switching mechanism using a Ti nanolayer at the Cu/$TaO_x$ interface. *Nanoscale Research Letters* **7,** 345 (2012).

22. Nauenheim, C., Kuegeler, C., Ruediger, a. & Waser, R. Investigation of the electroforming process in resistively switching $TiO_2$ nanocrosspoint junctions. *Applied Physics Letters* **96,** 122902 (2010).

23. Yanagida, T. *et al.* Scaling effect on unipolar and bipolar resistive switching of metal oxides. *Scientific Reports* **3,** 1657 (2013).

24. Chua, L. O. & Sung Mo Kang. Memristive devices and systems. *Proceedings of the IEEE* **64,** 209–223 (1976).

25. Oxley, D. P. Electroforming, Switching and Memory Effects in Oxide Thin Films. *ElectroComponent Science and Technology* **3,** 217–224 (1977).

26. Petersen, K. E. On state of amorphous threshold switches. *Journal of Applied Physics* **47,** 256 (1976).

27. Borghetti, J. *et al.* Electrical transport and thermometry of electroformed titanium dioxide memristive switches. *Journal of Applied Physics* **106,** 124504 (2009).

28. Strachan, J. P. *et al.* The switching location of a bipolar memristor: chemical, thermal and structural mapping. *Nanotechnology* **22,** 254015 (2011).

29. Joshua Yang, J. *et al.* The mechanism of electroforming of metal oxide memristive switches. *Nanotechnology* **20,** 215201 (2009).

30. Valov, I., Waser, R., Jameson, J. R. & Kozicki, M. N. Electrochemical metallization memories--fundamentals, applications, prospects. *Nanotechnology* **22,** 254003 (2011).

31. Valov, I. & Kozicki, M. N. Cation-based resistance change memory. *Journal of Physics D: Applied Physics* **46,** 74005 (2013).

32. Valov, I. *et al.* Nanobatteries in redox-based resistive switches require extension of memristor theory. *Nature Communications* **4,** 1771 (2013).

33. Jeong, D. S. *et al.* Emerging memories: resistive switching mechanisms and current status. *Reports on Progress in Physics* **75,** 076502 (2012).

34. Ha, S. D. & Ramanathan, S. Adaptive oxide electronics: A review. *Journal of Applied Physics* **110,** 071101 (2011).

35. Yang, Z., Ko, C. & Ramanathan, S. Oxide Electronics Utilizing Ultrafast Metal-Insulator Transitions. *Annual Review of Materials Research* **41,** 337–367 (2011).

36. Radu, I. P. *et al.* Switching mechanism in two-terminal vanadium dioxide devices. *Nanotechnology* **26,** 165202 (2015).

37. Strukov, D. B., Borghetti, J. L. & Williams, R. S. Coupled Ionic and Electronic Transport Model of Thin-Film Semiconductor Memristive Behavior. *Small* **5,** 1058–1063 (2009).

38. Pershin, Y. V. & Di Ventra, M. Memory effects in complex materials and nanoscale systems. *Advances in Physics* **60,** 145–227 (2011).

39. Joglekar, Y. N. & Wolf, S. J. The elusive memristor: properties of basic electrical circuits. 1–24 (2008). doi:10.1088/0143-0807/30/4/001

40. Pershin, Y. V., La Fontaine, S. & Di Ventra, M. Memristive model of amoeba learning. *Physical Review E - Statistical, Nonlinear, and Soft Matter Physics* **80,** 1–6 (2009).

41. Bersuker, G. *et al.* Metal oxide resistive memory switching mechanism based on conductive filament properties. *Journal of Applied Physics* **110,** (2011).

42. Puglisi, F. M., Larcher, L., Bersuker, G., Padovani, A. & Pavan, P. An empirical model for RRAM resistance in low-and high-resistance states. *IEEE Electron Device Letters* **34,** 387–389 (2013).

43. Kwon, D.-H. *et al.* Atomic structure of conducting nanofilaments in $TiO_2$ resistive switching memory. *Nature Nanotechnology* **5,** 148–53 (2010).

44. Kim, G. H. *et al.* Improved endurance of resistive switching TiO2 thin film by hourglass shaped Magnéli filaments. *Applied Physics Letters* **98,** 2–4 (2011).

45. Bae, Y. C. *et al.* Transition of metallic and insulating Ti sub-oxides in bipolar resistive switching $TiO_x$ /$TiO_y$ frameworks due to oxygen vacancy drifts. *Applied Physics A* **102,** 1009–1013 (2011).

46. Yang, J. J. *et al.* Dopant control by atomic layer deposition in oxide films for memristive switches. *Chemistry of Materials* **23,** 123–125 (2011).

47. Joshua Yang, J. *et al.* The mechanism of electroforming of metal oxide memristive switches. *Nanotechnology* **20,** 215201 (2009).

48. Sekhar, K. C. *et al.* Effect of bi-layer ratio in ZnO/$Al_2O_3$ multilayers on microstructure and functional properties of ZnO nanocrystals embedded in Al2O3 matrix. *Applied Physics A* **115,** 283–289 (2013).

49. Zhang, M. *et al.* Physical and electrical characterization of atomic-layer-deposited Ru nanocrystals embedded into $Al_2O_3$ for memory applications. *Journal of Physics D: Applied Physics* **41,** 032007 (2008).

50. Qin, S.-C., Dong, R.-X. & Yan, X.-L. Memristive behavior of $Al_2O_3$ film with bottom electrode surface modified by Ag nanoparticles. *Applied Physics A* (2014). doi:10.1007/s00339-014-8765-9

51. Song, J. *et al.* Effects of Ultrathin Al Layer Insertion on Resistive Switching Performance in an Amorphous Aluminum Oxide Resistive Memory. *Applied Physics Express* **3,** 091101 (2010).

52. Nagashima, K. *et al.* Switching Properties of Titanium Dioxide Nanowire Memristor Switching Properties of Titanium Dioxide Nanowire Memristor. *Japanese Journal of Applied Physics* **51,** 9–13 (2012).

53. Nagashima, K. *et al.* Resistive switching multistate nonvolatile memory effects in a single cobalt oxide nanowire. *Nano Letters* **10,** 1359–1363 (2010).

54. Huang, Y. *et al.* Logic gates and computation from assembled nanowire building blocks. *Science (New York, N.Y.)* **294,** 1313–7 (2001).

55. Huang, C.-H. *et al.* $ZnO_{1-x}$ nanorod arrays/ZnO thin film bilayer structure: from homojunction diode and high-performance memristor to complementary 1D1R application. *ACS Nano* **6,** 8407–14 (2012).

56. Song, J., Zhang, Y., Xu, C., Wu, W. & Wang, Z. L. Polar charges induced electric hysteresis of ZnO nano/microwire for fast data storage. *Nano Letters* 0–5 (2011). doi:dx.doi.org/10.1021/nl2011966

57. Qi, J. *et al.* Current self-complianced and self-rectifying resistive switching in Ag-electroded single Na-doped ZnO nanowires. *Nanoscale* **5,** 2651–4 (2013).

58. Younis, A., Chu, D. & Li, S. Stochastic memristive nature in Co-doped $CeO_2$ nanorod arrays. *Applied Physics Letters* **103,** 0–5 (2013).

59. Wu, W. & Wang, Z. L. Piezotronic nanowire-based resistive switches as programmable electromechanical memories. *Nano Letters* **11,** 2779–85 (2011).

60. In Kim, S. *et al.* Scaling behaviors for resistive memory switching in NiO nanowire devices. *Applied Physics Letters* **104,** 023513 (2014).

61. Wang, B. *et al.* Resistive switching in Ga- and Sb-doped ZnO single nanowire devices. *J. Mater. Chem. C* **3,** 11881–11885 (2015).

62. Bachmann, J. *et al.* Ordered iron oxide nanotube arrays of controlled geometry and tunable magnetism by atomic layer deposition. *Journal of the American Chemical Society* **129,** 9554–9555 (2007).

63. Tan, Z.-H., Yin, X.-B. & Guo, X. One-dimensional memristive device based on MoO3 nanobelt. *Applied Physics Letters* **106,** 023503 (2015).

64. Younis, A. *et al.* High-performance nanocomposite based memristor with controlled quantum dots as charge traps. *ACS Applied Materials and Interfaces* **5,** 2249–2254 (2013).

65. Younis, A., Chu, D., Mihail, I. & Li, S. Interface-engineered resistive switching: CeO2 nanocubes as high-performance memory cells. *ACS Applied Materials and Interfaces* **5,** 9429–9434 (2013).

66. Qi, J. *et al.* Resistive switching in single epitaxial ZnO nanoislands. *ACS Nano* **6,** 1051–1058 (2012).

67. Lee, J.-Y. *et al.* Voltage-dependent resistive switching characteristics in mixed layer consisting of $\gamma$-$Fe_2O_3$ and Pt-$Fe_2O_3$ core-shell nanoparticles. *Applied Physics Letters* **104,** 093514 (2014).

68. Zhao, L. *et al.* Current rectifying and resistive switching in high density $BiFeO_3$ nanocapacitor arrays on Nb-SrTiO3 substrates. *Scientific Reports* **5,** 9680 (2015).

69. Verbakel, F., Meskers, S. C. J. & Janssen, R. a J. Electronic memory effects in diodes of zinc oxide nanoparticles in a matrix of polystyrene or poly(3-hexylthiophene). *Journal of Applied Physics* **102,** 1–9 (2007).

70. Verbakel, F., Meskers, S. C. J., Leeuw, D. M. D. & Janssen, R. a J. Resistive switching in organic memories with a spin coated metal oxide nanoparticle layer. *Journal of Physical Chemistry* **112,** 5254–5257 (2008).

71. Lai, J. H., Su, S. H., Chen, H.-H., Huang, J. C. a. & Wu, C.-L. Stabilization of ZnO polar plane with charged surface nanodefects. *Physical Review B* **82,** 155406 (2010).

72. Yang, Y. *et al.* Observation of conducting filament growth in nanoscale resistive memories. *Nature Communications* **3,** 732 (2012).

73. Waser, R., Dittmann, R., Staikov, C. & Szot, K. Redox-based resistive switching memories nanoionic mechanisms, prospects, and challenges. *Advanced Materials* **21,** 2632–2663 (2009).

74. He, J. H., Hsin, C. L., Liu, J., Chen, L. J. & Wang, Z. L. Piezoelectric Gated Diode of a Single ZnO Nanowire. *Advanced Materials* **19,** 781–784 (2007).

75. Shenoy, R. S. *et al.* MIEC (mixed-ionic-electronic-conduction)-based access devices for non-volatile crossbar memory arrays. *Semiconductor Science and Technology* **29,** 104005 (2014).

76. Joshua Yang, J. *et al.* Engineering nonlinearity into memristors for passive crossbar applications. *Applied Physics Letters* **100,** 113501 (2012).

77. Lee, M.-J. *et al.* A fast, high-endurance and scalable non-volatile memory device made from asymmetric $Ta_2O_{(5-x)}/TaO_{(2-x)}$ bilayer structures. *Nature materials* **10,** 625–30 (2011).

78. Linn, E., Rosezin, R., Kügeler, C. & Waser, R. Complementary resistive switches for passive nanocrossbar memories. *Nature Materials* **9,** 403–6 (2010).

79. Yanagida, T. *et al.* Scaling effect on unipolar and bipolar resistive switching of metal oxides. *Scientific Reports* **3,** 1657 (2013).

80. Strukov, D. B. & Kohlstedt, H. Resistive switching phenomena in thin films: Materials, devices, and applications. *MRS Bulletin* **37,** 108–114 (2012).

81. Ignatiev, a. *et al.* Resistance switching in oxide thin films. *Phase Transitions* **81,** 791–806 (2008).

82. Lee, H. Y. *et al.* Low power and high speed bipolar switching with a thin reactive ti buffer layer in robust $HfO_2$ based RRAM. *Technical Digest - International Electron Devices Meeting, IEDM* 3–6 (2008). doi:10.1109/IEDM.2008.4796677

83. Zhang, X. T., Yu, Q. X., Yao, Y. P. & Li, X. G. Ultrafast resistive switching in $SrTiO_3$:Nb single crystal. *Applied Physics Letters* **97,** 222117 (2010).

84. Yoshida, C., Tsunoda, K., Noshiro, H. & Sugiyama, Y. High speed resistive switching in Pt/$TiO_2$/TiN film for nonvolatile memory application. *Applied Physics Letters* **91,** 223510 (2007).

85. Lee, H. Y. *et al.* Evidence and solution of Over-RESET Problem for $HfO_x$ Based Resistive Memory with Sub-ns Switching Speed and High Endurance. 7–10 (2010).

86. Torrezan, A. C., Strachan, J. P., Medeiros-Ribeiro, G. & Williams, R. S. Sub-nanosecond switching of a tantalum oxide memristor. *Nanotechnology* **22,** 485203 (2011).

87. Burr, G. W. *et al.* Phase change memory technology. *Journal of Vacuum Science & Technology B: Microelectronics and Nanometer Structures* **28,** 223 (2010).

88. Widrow, B. An Adaptive "Adaline" Neuron Using Chemical "Memistors." in *Stanford Electronics Laboratories Technical Report* 1553–2 (1960).

89. Serrano-Gotarredona, T., Masquelier, T., Prodromakis, T., Indiveri, G. & Linares-Barranco, B. STDP and sTDP variations with memristors for spiking neuromorphic learning systems. *Frontiers in Neuroscience* **7,** 1–15 (2013).

90. Gerstner, W., Kempter, R., van Hemmen, J. L. & Wagner, H. A neuronal learning rule for sub-millisecond temporal coding. *Nature* **383,** 76–81 (1996).

91. Bi, G. Q. & Poo, M. M. Synaptic modifications in cultured hippocampal neurons: dependence on spike timing, synaptic strength, and postsynaptic cell type. *The Journal of neuroscience : The Official Journal of the Society for Neuroscience* **18,** 10464–10472 (1998).

92. Bichler, O., Querlioz, D., Thorpe, S. J., Bourgoin, J. P. & Gamrat, C. Extraction of temporally correlated features from dynamic vision sensors with spike-timing-dependent plasticity. *Neural Networks* **32,** 339–348 (2012).

93. Bi, G. & Poo, M. SYNAPTIC M ODIFICATION BY C ORRELATED A CTIVITY : Hebb ' s Postulate Revisited. *Annual Review of Neuroscience* **24,** 139–166 (2001).

94. Caporale, N. & Dan, Y. Spike timing-dependent plasticity: a Hebbian learning rule. *Annual Review of Neuroscience* **31,** 25–46 (2008).

95. Feldman, D. E. The Spike-Timing Dependence of Plasticity. *Neuron* **75,** 556–571 (2012).

96. Li, Y. *et al.* Ultrafast synaptic events in a chalcogenide memristor. *Scientific Reports* **3,** 1619 (2013).

97. Kuzum, D., Jeyasingh, R. G. D., Lee, B. & Wong, H. P. Nanoelectronic Programmable Synapses Based on Materials for Brain-Inspired Computing. *Nano Letters* **12,** 2179–2186 (2012).

98. Xiong, F., Liao, A., Estrada, D. & Pop, E. Low-power switching of phase change materials with carbon nanotube electrodes. *Science* **332,** 568–570 (2011).

99. Loke, D. *et al.* Breaking the speed limits of phase-change memory. *Science* **336,** 1566–1569 (2012).

100. Evangelou, E. K., Rahman, M. S. & Dimoulas, a. Correlation of Charge Buildup and Stress-Induced Leakage Current in Cerium Oxide Films Grown on Ge (100) Substrates. *IEEE Transactions on Electron Devices* **56,** 399–407 (2009).

101. Mandal, S., El-Amin, A., Alexander, K., Rajendran, B. & Jha, R. Novel synaptic memory device for neuromorphic computing. *Scientific Reports* **4,** 5333 (2014).

102. Rajendran, B. *et al.* Specifications of nanoscale devices and circuits for neuromorphic computational systems. *IEEE Transactions on Electron Devices* **60,** 246–253 (2013).

103. Zamarreño-Ramos, C. *et al.* On Spike-Timing-Dependent-Plasticity, Memristive Devices, and Building a Self-Learning Visual Cortex. *Frontiers in Neuroscience* **5,** 1–22 (2011).

104. Wang, Z. L. Zinc oxide nanostructures: growth, properties and applications. *Journal of Physics: Condensed Matter* **16,** R829–R858 (2004).

105. Djurišić, A. B., Chen, X., Leung, Y. H. & Man Ching Ng, A. ZnO nanostructures: growth, properties and applications. *Journal of Materials Chemistry* **22,** 6526 (2012).

106. Hsu, Y. F., Xi, Y. Y., Djurišić, a. B. & Chan, W. K. ZnO nanorods for solar cells: Hydrothermal growth versus vapor deposition. *Applied Physics Letters* **92,** 2006–2009 (2008).

107. Greene, L. E., Yuhas, B. D., Law, M., Zitoun, D. & Yang, P. Solution-grown zinc oxide nanowires. *Inorganic Chemistry* **45,** 7535–7543 (2006).

108. Pearton, S. J., Norton, D. P., Ip, K., Heo, Y. W. & Steiner, T. Recent progress in processing and properties of ZnO. *Superlattices and Microstructures* **34,** 3–32 (2003).

109. Xu, S. & Wang, Z. L. One-dimensional ZnO nanostructures: Solution growth and functional properties. *Nano Research* **4,** 1013–1098 (2011).

110. Greene, L. E. *et al.* Low-temperature wafer-scale production of ZnO nanowire arrays. *Angewandte Chemie (International ed. in English)* **42,** 3031–4 (2003).

111. Baruah, S. & Dutta, J. Hydrothermal growth of ZnO nanostructures. *Science and Technology of Advanced Materials* **10,** 013001 (2009).

112. Joo, J., Chow, B. Y., Prakash, M., Boyden, E. S. & Jacobson, J. M. Face-selective electrostatic control of hydrothermal zinc oxide nanowire synthesis. *Nature Materials* **10,** 596–601 (2011).

113. Yu, D., Trad, T., McLeskey, J. T., Craciun, V. & Taylor, C. R. ZnO Nanowires Synthesized by Vapor Phase Transport Deposition on Transparent Oxide Substrates. *Nanoscale Research Letters* **5,** 1333–9 (2010).

114. Subannajui, K. *et al.* ZnO Nanowire Growth: A Deeper Understanding Based on Simulations and Controlled Oxygen Experiments. *Crystal Growth & Design* **10,** 1585–1589 (2010).

115. Zhou, Z. *et al.* Rapid mass production of ZnO nanowires by a modified carbothermal reduction method. *Materials Letters* **65,** 832–835 (2011).

116. Byrne, D. *et al.* A Study of Drop-Coated and Chemical Bath-Deposited Buffer Layers for Vapor Phase Deposition of Large Area, Aligned, Zinc Oxide Nanorod Arrays. *Crystal Growth & Design* **10,** 2400–2408 (2010).

117. Huang, M. *et al.* Catalytic Growth of Zinc Oxide Nanowires. *Advanced Materials* **13,** 113–116 (2001).

118. Ho, S. Te *et al.* Catalyst-free surface-roughness-assisted growth of large-scale vertically aligned zinc oxide nanowires by thermal evaporation. *Chemistry of Materials* **19,** 4083–4086 (2007).

119. Koshy, O. & Khadar, M. a. Superparamagnetism in undoped ZnO nanorods. *Applied Surface Science* **346,** 528–533 (2015).

120. Zhao, C. X. *et al.* Large-Scale Synthesis of Bicrystalline ZnO Nanowire Arrays by Thermal Oxidation of Zinc Film: Growth Mechanism and High-Performance Field Emission. *Crystal Growth & Design* **13,** 2897–2905 (2013).

121. Zappa, D., Comini, E. & Sberveglieri, G. Thermally oxidized zinc oxide nanowires for use as chemical sensors. *Nanotechnology* **24,** 444008 (2013).

122. Podrezova, L. V., Porro, S., Cauda, V., Fontana, M. & Cicero, G. Comparison between ZnO nanowires grown by chemical vapor deposition and hydrothermal synthesis. *Applied Physics A* **113,** 623–632 (2013).

123. Pung, S.-Y., Choy, K.-L. & Hou, X. Tip-growth mode and base-growth mode of Au-catalyzed zinc oxide nanowires using chemical vapor deposition technique. *Journal of Crystal Growth* **312,** 2049–2055 (2010).

124. Cheng, A.-J. *et al.* Thermal chemical vapor deposition growth of zinc oxide nanostructures for dye-sensitized solar cell fabrication. *Applied Physics Letters* **92,** 092113 (2008).

125. Chang, P. *et al.* ZnO Nanowires Synthesized by Vapor Trapping CVD Method. *Chemistry of Materials* **16,** 5133–5137 (2004).

126. Greene, L. E. *et al.* General route to vertical ZnO nanowire arrays using textured ZnO seeds. *Nano Letters* **5,** 1231–1236 (2005).

127. Xu, S. *et al.* Patterned growth of vertically aligned ZnO nanowire arrays on inorganic substrates at low temperature without catalyst. *Journal of the American Chemical Society* **130,** 14958–14959 (2008).

128. Liu, F. *et al.* Well-aligned zinc oxide nanorods and nanowires prepared without catalyst. *Journal of Crystal Growth* **274,** 126–127 (2005).

129. Suntola, T. Atomic layer epitaxy. *Materials Science Reports* **4,** 261–312 (1989).

130. Groner, M. D., Elam, J. W., Fabreguette, F. H. & George, S. M. Electrical characterization of thin $Al_2O_3$ films grown by atomic layer deposition on silicon and various metal substrates. *Thin Solid Films* **413,** 186–197 (2002).

131. Aarik, L. *et al.* Atomic layer deposition of $TiO_2$ from $TiCl_4$ and $O_3$. *Thin Solid Films* **542,** 100–107 (2013).

132. Sammelselg, È., Uustare, T., Ritala, M. & Leskela, M. Characterization of titanium dioxide atomic layer growth from titanium ethoxide and water. *Thin Solid Films* **370,** 163–172 (2000).

133. Ritala, M., Leskela, M., Niinisto, L., Haussalo, P. & Niinist, L. Titanium Isopropoxide as a Precursor in Atomic Layer Epitaxy of Titanium Dioxide Thin Films. *Chemical Material* **5,** 1174–1181 (1993).

134. Puurunen, R. L. Growth Per Cycle in Atomic Layer Deposition: A Theoretical Model. *Chemical Vapor Deposition* **9,** 249–257 (2003).

135. Pakkala, A. & Putkonen, M. *Atomic Layer Deposition*. *Handbook of Deposition Technologies for Films and Coatings* 364–391 (Elsevier B.V., 2010). doi:10.1016/B978-0-8155-2031-3.00008-9

136. Selvaraj, S. K., Jursich, G. & Takoudis, C. G. Design and implementation of a novel portable atomic layer deposition/chemical vapor deposition hybrid reactor. *Review of Scientific Instruments* **84,** 095109 (2013).

137. Longrie, D., Deduytsche, D., Haemers, J., Driesen, K. & Detavernier, C. A rotary reactor for thermal and plasma-enhanced atomic layer deposition on powders and small objects. *Surface and Coatings Technology* **213,** 183–191 (2012).

138. Levrau, E. *et al.* In situ IR Spectroscopic Investigation of Alumina ALD on Porous Silica Films: Thermal Versus Plasma Enhanced ALD. *The Journal of Physical Chemistry C* **118,** 29854–29859 (2014).

139. Aghaee, M. *et al.* Low temperature temporal and spatial atomic layer deposition of TiO2 films. *Journal of Vacuum Science & Technology A: Vacuum, Surfaces, and Films* **33,** 041512 (2015).

140. McCormick, J. a., Cloutier, B. L., Weimer, a. W. & George, S. M. Rotary reactor for atomic layer deposition on large quantities of nanoparticles. *Journal of Vacuum Science & Technology A: Vacuum, Surfaces, and Films* **25,** 67 (2007).

141. George, S. M. Atomic layer deposition: An overview. *Chemical Reviews* **110,** 111–131 (2010).

142. Guan, C. *et al.* Hollow core–shell nanostructure supercapacitor electrodes: gap matters. *Energy & Environmental Science* **5,** 9085 (2012).

143. Guan, C. *et al.* Highly stable and reversible lithium storage in $SnO_2$ nanowires surface coated with a uniform hollow shell by atomic layer deposition. *Nano Letters* **14,** 4852–4858 (2014).

144. Li, X., Fan, N. C. & Fan, H. J. A Micro-pulse Process of Atomic Layer Deposition of Iron Oxide Using Ferrocene and Ozone Precursors and Ti-Doping. *Chemical Vapor Deposition* **19,** 104–110 (2013).

145. Martinson, A. B. F. *et al.* Atomic Layer Deposition of $Fe_2O_3$ Using Ferrocene and Ozone. *The Journal of Physical Chemistry C* **115,** 4333–4339 (2011).

146. Lee, J. P. & Sung, M. M. A new patterning method using photocatalytic lithography and selective atomic layer deposition. *Journal of the American Chemical Society* **126,** 28–9 (2004).

147. Lee, J. P., Jang, Y. J. & Sung, M. M. Atomic layer deposition of $TiO_2$ thin films on mixed self-assembled monolayers studied as a function of surface free energy. *Advanced Functional Materials* **13,** 873–876 (2003).

148. Porro, S. *et al.* Low-temperature atomic layer deposition of $TiO_2$ thin layers for the processing of memristive devices. *Journal of Vacuum Science & Technology A: Vacuum, Surfaces, and Films* **34,** (2016).

149. Seo, E. K., Lee, J. W., Sung-Suh, H. M. & Sung, M. M. Atomic Layer Deposition of Titanium Oxide on Self-Assembled-Monolayer-Coated Gold. *Chemistry of Materials* **16,** 1878–1883 (2004).

150. Ras, R. H. a, Sahramo, E., Malm, J., Raula, J. & Karppinen, M. Blocking the lateral film growth at the nanoscale in area-selective atomic layer deposition. *Journal of the American Chemical Society* **130,** 11252–11253 (2008).

151. Rivolo, P., Severino, S. M., Ricciardi, S., Frascella, F. & Geobaldo, F. Protein immobilization on nanoporous silicon functionalized by RF activated plasma

polymerization of Acrylic Acid. *Journal of Colloid and Interface Science* **416,** 73–80 (2014).

152. Menzel, A. *et al.* Role of carrier gas flow and species diffusion in nanowire growth from thermal CVD. *Journal of Physical Chemistry C* **116,** 5524–5530 (2012).

153. Gardner, P. J., Pang, P. & Preston, S. R. Binary gaseous diffusion coefficients of mercury and of zinc in hydrogen, helium, argon, nitrogen, and carbon dioxide. *Journal of Chemical & Engineering Data* **36,** 265–268 (1991).

154. Mohammad, S. N. Contact mechanisms and design principles for (Schottky and Ohmic) metal contacts to semiconductor nanowires. *Journal of Applied Physics* **108,** 034311 (2010).

155. Brillson, L. J. & Lu, Y. ZnO Schottky barriers and Ohmic contacts. *Journal of Applied Physics* **109,** 121301 (2011).

156. Chang, W.-Y., Lin, C.-A., He, J.-H. & Wu, T.-B. Resistive switching behaviors of ZnO nanorod layers. *Applied Physics Letters* **96,** 242109 (2010).

157. Jasmin, A., Porro, S., Chiolerio, A., Pirri, C. F. & Ricciardi, C. Polymer coated ZnO nanowires for memristive devices. *Proceedings of IEEE Nano 2015,* 496–498 (2015).

158. Jasmin, A. *et al.* Multistate switching in ZnO NW-based memristive devices. *In preparation.*

159. Chiu, F. C. A review on conduction mechanisms in dielectric films. *Advances in Materials Science and Engineering* **2014,** (2014).

160. Son, D. I., You, C. H., Jung, J. H. & Kim, T. W. Carrier transport mechanisms of organic bistable devices fabricated utilizing colloidal ZnO quantum dot-polymethylmethacrylate polymer nanocomposites. *Applied Physics Letters* **97,** 013304 (2010).

161. Hussain, I., Soomro, M. Y., Bano, N., Nur, O. & Willander, M. Interface trap characterization and electrical properties of Au-ZnO nanorod Schottky diodes by conductance and capacitance methods. *Journal of Applied Physics* **112,** (2012).

162. Rahaman, S. Z. *et al.* Repeatable unipolar/bipolar resistive memory characteristics and switching mechanism using a Cu nanofilament in a $GeO_x$ film. *Applied Physics Letters* **101,** 073106 (2012).

163. Peng, S. *et al.* Mechanism for resistive switching in an oxide-based electrochemical metallization memory. *Applied Physics Letters* **100,** (2012).

164. Long, B., Li, Y., Mandal, S., Jha, R. & Leedy, K. Switching dynamics and charge transport studies of resistive random access memory devices. *Applied Physics Letters* **101,** 113503 (2012).

165. Leem, J. *et al.* Role of HCl in Atomic Layer Deposition of $TiO_2$ Thin Films from Titanium Tetrachloride and Water. *Bulletin of the Korean Chemical Society* **35,** 1195–1201 (2014).

166. Niilisk, A. *et al.* Structural study of $TiO_2$ thin films by micro-Raman spectroscopy. *Central European Journal of Physics* **4,** 105–116 (2006).

167. Prakash, A., Maikap, S., Banerjee, W., Jana, D. & Lai, C.-S. Impact of electrically formed interfacial layer and improved memory characteristics of $IrO_x$/high-κx/W structures containing $AlO_x$, $GdO_x$, $HfO_x$, and $TaO_x$ switching materials. *Nanoscale Research Letters* **8,** 379 (2013).

168. Lübbe, M., Gigler, A. M., Stark, R. W. & Moritz, W. Identification of iron oxide phases in thin films grown on Al2O3(0001) by Raman spectroscopy and X-ray diffraction. *Surface Science* **604,** 679–685 (2010).

169. Slavov, L. *et al.* Raman spectroscopy investigation of magnetite nanoparticles in ferrofluids. *Journal of Magnetism and Magnetic Materials* **322,** 1904–1911 (2010).

170. Yamashita, T. & Hayes, P. Analysis of XPS spectra of $Fe^{2+}$ and $Fe^{3+}$ ions in oxide materials. *Applied Surface Science* **254,** 2441–2449 (2008).

171. Biesinger, M. C. *et al.* Resolving surface chemical states in XPS analysis of first row transition metals, oxides and hydroxides: Cr, Mn, Fe, Co and Ni. *Applied Surface Science* **257,** 2717–2730 (2011).

172. Strachan, J. P. *et al.* State dynamics and modeling of tantalum oxide memristors. *IEEE Transactions on Electron Devices* **60,** 2194–2202 (2013).

173. Jasmin, A., Porro, S., Chiolerio, A., Pirri, F. & Ricciardi, C. Memristive properties of atomic layer deposited iron oxide thin films. *In preparation.*

174. Odagawa, A. *et al.* Electroforming and resistance-switching mechanism in a magnetite thin film. *Applied Physics Letters* **91,** 2007–2009 (2007).