Design of an Advanced Portable System for High Density Surface EMG Recording with Wireless Control of Signal Quality

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Summary

High density surface EMG (HD-sEMG) is a technique for evaluating and recording the electrical activity produced by muscles by placing a 2-dimensional (2D) grid comprising many closely spaced electrodes (3~10 mm center-to-center), instead of just a few electrodes, on the muscles. The advantage of HD-sEMG over intramuscular EMG, apart from the non-invasiveness and the relative ease of obtaining spatial distributions of electrical muscle activity, is its high reproducibility in follow up studies.

Despite the importance of HD-sEMG in many fields such as a valuable aid in discovering and diagnosing abnormalities not only in the muscles but also in the motor system as a whole, the development of HD-sEMG detecting and recording system is considered to be quite behind technology nowadays. It is necessary to develop a new generation HD-sEMG detecting and recording device in order to meet the requirements in more channels, higher resolution and portable, which is why the design of an advanced portable system for high density surface EMG recording with wireless control of signal quality (HD-sEMG RSWC) is proposed.

In the first chapter of this thesis, state of the art of related technologies to design the HD-sEMG RSWC is studied. These technologies include: 1) electrode system for HD-sEMG; 2) front end amplifiers; 3) A/D conversion; 4) data acquisition system; 5)

wireless communication network; 6) wireless communication solution.

The state of the art of the electrode system for HD-sEMG RSWC is studied as described in **SECTION1.2**. Moreover, the selected 64-channel flexible electrode grid for HD-sEMG detection is presented in **SECTION1.2**.

The state of the art of analog front end (AFE) is investigated as described in **SECTION1.3**. Normally, raw sEMG can range between ±5 mV and typically the frequency content ranges between 6 and 500 Hz, showing most power between 10 and 250 Hz. An AFE is a set of analog signal conditioning circuitry that uses operational amplifiers, filters as well as application-specific integrated circuits to provide more "pure" EMG signals. Two possible AFE solutions (HY-2 dual channel EMG hybrid front-end and 64-channel WEMG AFE), both available at LISiN are discussed in **SECTION 2.3.2**. The 64-channel WEMG AFE designed by Dr U.Barone (2013) is selected for its advantages in lower power consumption and higher common-mode rejection ratio (CMRR).

The state of the art of analog digital converter (ADC) is discussed in **SECTION1.4.** An ADC is used to digitize EMG signals after conditioning by the AFE. Successive-approximation-register (SAR) ADCs are frequently the choice for medium-to-high-resolution applications with sample rates under 5 Msps. Resolution for SAR ADCs most commonly ranges from 8 to 16 bits. SAR ADC provides low power consumption as well as a small size. This combination of features makes SAR ADCs ideal for the HD-sEMG RSWC. Two possible ADC solutions (LTC2368-16 and LTC2370-16) are discussed in **SECTION2.3.3**. In addition, LTC2368-16 is selected for its advantages in less integral linearity error (INL) and lower power consumption comparing to LTC2370-16.

The state of the art of data acquisition system (DAQ) is discussed in **SECTION1.5.** DAQ is a combination of AFE, ADC and other application-specific integrated circuits processes. A non-multiplexed DAQ system is discussed in **SECTION1.5.2** and a multiplexed DAQ system is discussed in **SECTION1.5.3.** The multiplexed DAQ solution is selected for the advantage in savings power, size, and cost. However, it also introduces a disadvantage: system delay between two channels, although these system delay can be somehow compensated by adding system delay time into the computing of conduction velocity (CNV).

The state of the art of wireless networks is discussed in **SECTION1.6.** Various wireless networks are discussed in **SECTION1.6.1**. In addition, a previous prototype for implementing data link solution for HD-sEMG DAQ system based on ultra-wideband (UWB) wireless connection by Z. Babaie (2011) at LISiN is discussed in **SECTION1.6.2**. Analyzing the failure of the previous prototype based on UWB, we found that: 1) an internal printed circuit board (PCB) antenna is apparently not suitable for a stable wireless communication. A high gain external antenna must be adopted in the future wireless communication solution to make the wireless communication more stable and less vulnerable to obstacles. 2) Wireless network only using a pair of low power consumption sender and receiver limits the radio range of the wireless communication therefore should not be used in further wireless communication system. In addition, Wi-Fi wireless network has the advantages in higher throughput and more stability compared to point-to-point network (e.g. Bluetooth), is selected as wireless communication network for the design of the HD-sEMG RSWC as discussed in **SECTION 1.6.3**.

The state of the art of Wi-Fi communication solutions is discussed in **SECTION1.7.** Two different Wi-Fi communication solutions are investigated, including: 100% Wi-Fi

solution and 10% Wi-Fi solution. In addition, by comparing in stability, the influence introduced by wireless packet loss and power consumption (described in **SECTION1.7.4**), the solution that transmit only a portion (10% of every second) of data wirelessly for on-line visualization with all data recorded in a SD memory card for off-line analysis at the same time is selected for the HD-sEMG RSWC.

In the end of the first chapter, the objectives of the work are presented in **SECTION1.8**, which includes: 1) the design of a portable system for high density surface EMG recording with wireless control of signal quality; 2) the implementation and technical testing of a prototype (including hardware, firmware and control panel) to verify the design; 3) two physiological applications using this prototype; 4) the analysis of the technical advantages/disadvantages, the limitations and the future technologies that may be useful for further design.

The second chapter of this thesis describes the methodologies to design the HD-sEMG RSWC. The design criteria of this system are studied and defined in **SECTION2.2.1** &**2.2.2**. A system block diagram of the proposed design that satisfied these defined criteria is presented in **SECTION2.2.3.** The HD-sEMG RSWC is divided into serval subsystems, which include: 1) data acquisition system; 2) data recording system; 3) Wi-Fi communication system; 4) power supply unit. Furthermore, technical investigation about the solutions, the chips or the modules for the design of each subsystem is discussed in **SECTION2.3-6**.

The third chapter of this thesis is focus on the implementation (including hardware, firmware and control panel) and the technical testing of a prototype to verify the proposed design as described in **SECTION2**. First of all, the criteria to design a printed circuit board (PCB) for placement of all components selected is described in **SECTION**

3.2.1. Technical investigation of more components (such as aluminum enclosure, power socket bulkhead and power plug) to enhance electromagnetic compatibility (EMC) and safety of the prototype is described in **SECTION3.2.2**. Moreover, user panels that help user to follow correct connection of the external connectors (such as charger, patient reference and so on) and check the work state are descried in **SECTION3.2.3.**

The second part of chapter 3 is focus on the firmware that was developed for the prototype. Information about the integrated development environment (IDE) for firmware is described in **SECTION3.3.1**. The software structure of the firmware is depicted in **SECTION3.3.2.** Multi-thread application is described in **SECTION3.3.3**. Data flow of the multi-thread application is specified in **SECTION3.3.4**. File system and specific format to organize the data recorded in SD memory card is described in **SECTION3.3.5**.

The third part of chapter 3 describes three technical tests performed on the prototype to verify the design. The first test is about gain mismatching of the 64-channel WEMG AFE, which is used to amplify 64-channel single-end analog inputs. Test bench setup, test procedure and test results of the first test are described in **SECTION3.4.1**. The second test is about the performance of multiplexers and ADC in the DAQ without AFE. Test bench setup, test procedure and test results of the second test are described in **SECTION3.4.2**. The third test is about throughput and stability of Wi-Fi communication system. Test bench setup, test procedure and test results of the third test are described in **SECTION3.4.3**.

System characteristics, including data acquisition characteristics, timing characteristics, electrical characteristics, physical characteristics and RF characteristics, are described in **SECTION3.5**. Moreover, how to perform calibration of the prototype as technical

support is described in **SECTION3.6.**

In the fourth chapter of this thesis, the procedure of off-line signal processing (with Matlab) of HD-sEMG signals acquired by this system is discussed. First of all, EMG signals recorded in a SD memory card are loaded to Matlab (version 2010a or higher) as 16-bit data with big endian encoding format (machine code) as described in **SECTION4.1-2**. Secondly, a channel remapping is performed according to the placement of electrode grid as described in **SECTION4.3**. Moreover, pre-processing is performed to remove (or reduce) electrode offset, artefact and noises of each signal as described in **SECTION4.4**. Root mean square (RMS) of the amplitude of monopolar surface EMG signals is computed and the results are plot in a 2D RMS map as described in **SECTION4.5.** In the end, the procedure to find the centroid of the 2D RMS map, which is commonly used to estimate the position of the EMG source during each contraction, is described in **SECTION4.6**.

In the fifth chapter of this thesis, two physiological applications using this prototype are described. In the first application (see **SECTION5.2**), EMG signals are acquired by placing a 64-channel electrode grid (IED=1cm) on the biceps brachii muscle of two subjects. Single differential EMG signals along muscle fiber direction column by column (7 single differential signals per column) are plotted. The propagation of motor unit action potentials (MUAPs) along the fibers of motor units (MUs) of the biceps brachii of two subjects is presented in **SECTION5.2.5**. Information concerning innervation zone (IZ) and conduction velocity of the MUAP can be obtained from all columns showing MUAP as described in **SECTION5.2.5**.

In the second application, EMG signals are acquired by placing a 64-channel electrode grid (IED=1cm) on the proximal portion of dorsal forearm of three subjects. Spatial

distribution of monopolar surface EMG amplitude on the forearm is used to estimate the most active muscle area during the following different specific biomechanical actions: wrist extension (WRIST EXT), ulnar deviation (ULN DEV), middle finger extension (MID), ring finger extension (RING) and little finger extension (LIT). Whether the spatial properties of the monopolar EMG amplitude distribution (RMS) over the proximal portion of dorsal forearm can be used to discriminate different contractions or not is studied and the results are presented in **SECTION5.3.7**.

The last chapter of this thesis is focus on a discussion about the technical advantages /disadvantages and the limitations of the prototype of HD-sEMG RSWC as well as the future technologies that may be useful to a new design. The technical advantages and disadvantages of the prototype is described in **SECTION6.2.** The limitations discovered in the prototype are discussed in **SECTION6.3**. The future technologies that may be useful for a new design are discussed in **SECTION6.4**.

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Contents

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List of Acronyms

ADC	Analog Digital Converter
AFE	Analog Front End
AHB	Advanced High-performance Bus
BAN	Body Area Network
CDMA	Code Division Multiple Access
CMRR	Common-Mode Rejection Ratio
CNV	Conduction velocity
CPU	Central Processing Unit
DAQ	Data Acquisition module
DMA	Direct Memory Access
DRS	Data Recording System
DSP	Digital Signal Processor
EMG	Electromyography
FIFO	First in First out
GPDMA	General Purpose Direct Memory Access
HD-sEMG	High Density Surface EMG
HSDPA	High-Speed Downlink Packet Access
HSPA	High-Speed Packet Access
HSUPA	High-Speed Uplink Packet Access
I2C	Inter-Integrated Circuit
I2S	Integrated Inter-chip Sound
IDE	Integrated Development Environment
IED	Inter Electrode Distance

INL	Integral Linearity Error
IZ	Innervation Zone
JTAG	Joint Test Action Group
LAN	Local Area Network
LDO	Low Drop-Out
LSB	Least Significant Bit
LTE	Long Term Evolution
MA	Multiplexers Array
MAN	Metropolitan Area Network
M2M	Machine To Machine
M2E	Machine To Enterprise systems
MAC	Media Access Control
MCU	Micro-Controller Unit
MIMO	Multiple-input Multiple-output
MSB	Most Significant Bit
MUAP	Motor Unit Action Potential
NVIC	Nested Vectored Interrupt Controller
OS	Operating System
PAN	Personal Area Network
PC	Personal Computer
PCB	Printed Circuit Board
PHY	Physical Layer Protocol
PSD	Power Spectral Density
RAM	Random-access memory
RTOS	Real-time Operation System

SAR	Successive Approximation Register
SD	Secure Digital
SIM	Subscriber Identity Module
SDK	Software Development Kit
SMT	Surface Mount technology
SoC	System-on-Chip
SPI	Serial Peripheral Interface
SPS	Sample Per Second
TCP	Transmission Control Protocol
THT	Through-Hole technique
WAN	Wide Area Network
WAP	Wireless Access Point
WiMAX	Worldwide Interoperability for Microwave Access
WCDMA	Wideband Code Division Multiple Access
WLAN	Wireless Local Area Network
WSN	Wireless Sensor Network
UART	Universal Asynchronous Receiver/Transmitter
UDP	User Datagram Protocol
USB	Universal Serial Bus
UWB	Ultra-WideBand

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List of Figures

dimension) to 2D (two-Dimension) described in Figure4.3. In “pre-processing”, the electrodes offset, artefacts and other noises outside the EMG bandwidth [20Hz, 500Hz] are removed (or reduced) from raw signals by the program described in Figure4.5,. After pre-processing, Power-Spectral-Density (PSD) analysis is used to check whether 50Hz power line interference exists or not. If exists, spectrum interpolation is performed to reduce 50Hz power line interference and its harmonics (up to 10th harmonics) by the program described in Figure4.8. In “bad channel detection”, channel interpolation will be performed to update the RMS map if bad channels are detected. Finally, the centroid of the updated map (replacing the values below threshold with zero) is found and marked with white cross by the program described in section4.6. 114

Figure4.2: Monopolar (upper) and single differential (lower) EMG signals acquired from column 3 of the 64-channel electrode grid (see Figure5.2) of subject 1 (S1) contracting with holding 3kg weight. EMG signals acquired originally were monopolar and were computed to single differential by software. In single different mode, motor unit action potential (MUAP) produced by motor units of biceps brachii is easy to be detected with an inter-electrode distance (IED) of 1cm. The red lines indicate the propagation of MUAPs along muscle fiber direction. 115

Figure4.3: (a) Structure of the raw data loaded into MATLAB is an array that consists of recorded samples in a specific ordering. (b)The structure of reshaped data is a 64xNsamples (Number of samples) matrix. After reshaping, each row of the 64xNsample matrix contains all the samples acquired from the same channel. ‘CH1S1, CH1S2, …, CH1SN-1,CH1SN’ indicate the 1st, 2nd, …, (N-1)th, Nth sample of channel one. ‘CH2S1, CH2S2, …, CH2SN-1,CH2SN’ indicate the 1st, 2nd, …, (N-1)th, Nth sample of channel two. ‘CH63S1, CH63S2, …, CH63SN-1,CH63SN’ indicate the 1st, 2nd, …, (N-1)th, Nth sample of channel sixty-three. ‘CH64S1, CH64S2, …,

at 2000 S/s (0.5ms between samples). A 64-channel electrode grid (see Figure5.2) is placed on the biceps brachii of subject 1 holding 3kg weight in isometric condition. EMG signals are initially acquired in monopolar configuration and are converted to SD later. The propagation of MUAPs is marked with red line. Different MUs are also marked with number in a circle. The anatomical model to explain phenomena detected in this figure is presented in Figure5.10. No propagation MU is detected in column 1 and column 2, which is marked with red dashed rectangle. These no propagation MU may be due to cross talk from its neighbour muscle (triceps) or motion artefacts. CNVs estimated (with the method presented in Figure5.7) from each column are more or less the same. 147

Figure5.10: Anatomical model to explain the phenomenon detected in Figure5.9. The model consists of bone, muscle tissue, a subcutaneous layer and skin. MUs are marked with number. MU1 (marked with 1) has the largest territory so that can be detected in all columns. MU2 also has a large territory and can be detected in column 2-7. MU 3-7 are small MUs located more superficial to skin and can only be detected in fewer columns of the electrode array. C1 is column 1 and C8 is column 8 of the electrode array.....147

Figure5.11: Time course (over 250ms) of the longitudinal single differential (LSD) EMG signals detected from each column (columns 1-8, 7 channels per column). By visual analysis, innervation zone is detected under rows 3-4. The LSD signals are sampled at 2000 S/s (0.5ms between samples). A 64-channel electrode grid (see Figure5.2) is placed on the biceps brachii of subject 2 holding 3kg weight in isometric condition. EMG signals are initially acquired in monopolar configuration and are convert to SD later. The propagation of MUAPs is marked with red line. Different MUs are also marked with number in a circle. The anatomical model to explain phenomena

List of Tables

PCBs can be single sided (one copper layer), double sided (two copper layers) or multi-layer. Conductors on different layers are connected with plated-through holes called vias. Advanced PCBs may contain components - capacitors, resistors or active devices

1

State of the Art and Objectives of the Work

1.1 General

Myoelectric signals are formed by physiological variations in the state of muscle fiber membranes. Electromyography (EMG) is the recording of the electrical activity of muscles, and therefore constitutes an extension of the physical exploration and testing of the integrity of the motor system [1] [2]. EMG is used for the study of muscle function through the inquiry into the myoelectric signal the

muscles emanate. When pathological conditions arise in the motor system, whether in the spinal cord, the motor neurons, the muscles, or the neuromuscular junctions, the characteristics of the electrical signals in the muscle change. Careful registration and study of electrical signals in muscle (electromyograms, EMG) can thus be a valuable aid in discovering and diagnosing abnormalities not only in the muscles but also in the motor system as a whole [3].

A motor unit (MU) is the functional unit of a muscle consisted of a motor neuron and the muscle fibers it innervates. The EMG signal is composed of the action potentials from groups of MUs, which can be detected with sensors placed on the surface of the skin or with needle or wire sensors introduced into the muscle tissue. There are two main kinds of EMG in widespread use: intramuscular (needle and fine-wire) EMG and surface EMG (sEMG). To acquire intramuscular EMG, a needle electrode or a needle containing two fine-wire electrodes is inserted through the skin into the muscle tissue. A trained professional (such as a neurologist, physiatrist, chiropractor, or physical therapist) observes the electrical activity while inserting the electrode. Certain places limit the use of needle EMG by non-physicians.

Traditionally, neuromuscular disorders have been diagnosed with intramuscular (needle) EMG, often in combination with motor-nerve conduction studies [4][5][6]. However, needle EMG has disadvantages, the most prominent being the invasiveness and the lack of spatial information. In the latter, surface electrodes are widely used to record the compound muscle action potentials.

Normally, raw sEMG can range between ±5 mV and typically the frequency content ranges between 6 and 500 Hz, showing most power between 10 and 250 Hz. In the example given below (**Figure1.1**), a raw surface EMG recording (sEMG) was done

for three static contractions of the biceps brachii muscle [7].

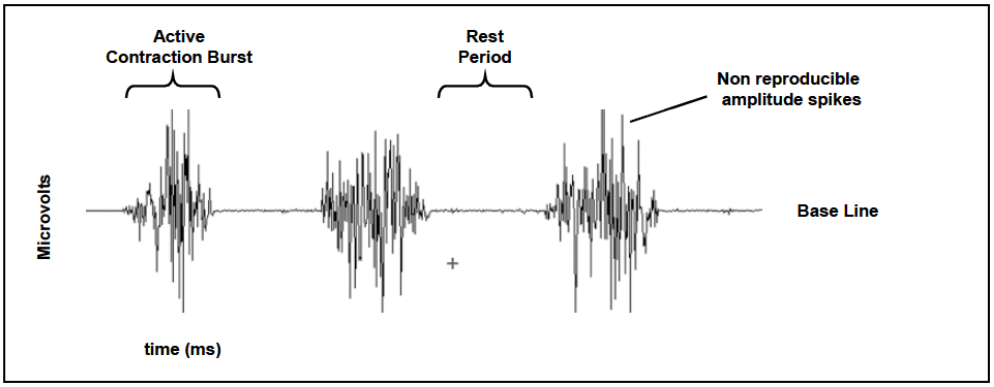

Figure1.1: Raw sEMG recording of three contraction bursts of the biceps brachii muscle. When the muscle is relaxed, a more or less noise-free EMG baseline can be seen. Non-reproducible amplitude spikes are recorded during every active contraction burst. Reproduced by courtesy of [8].

In many cases it is desirable to study and/or use the information contained in the timing of the discharges of individual motor units, such as in investigations for furthering the understanding of how motor units are controlled by the central nervous system (CNS) in generating force or for assessing the degree of dysfunction in upper motoneuron diseases such as cerebral palsy, Parkinson's disease, amyotrophic lateral sclerosis (ALS), stroke, and other disorders. This may be achieved by "decomposing" the EMG signal. The concept is depicted in **Figure1.2**.

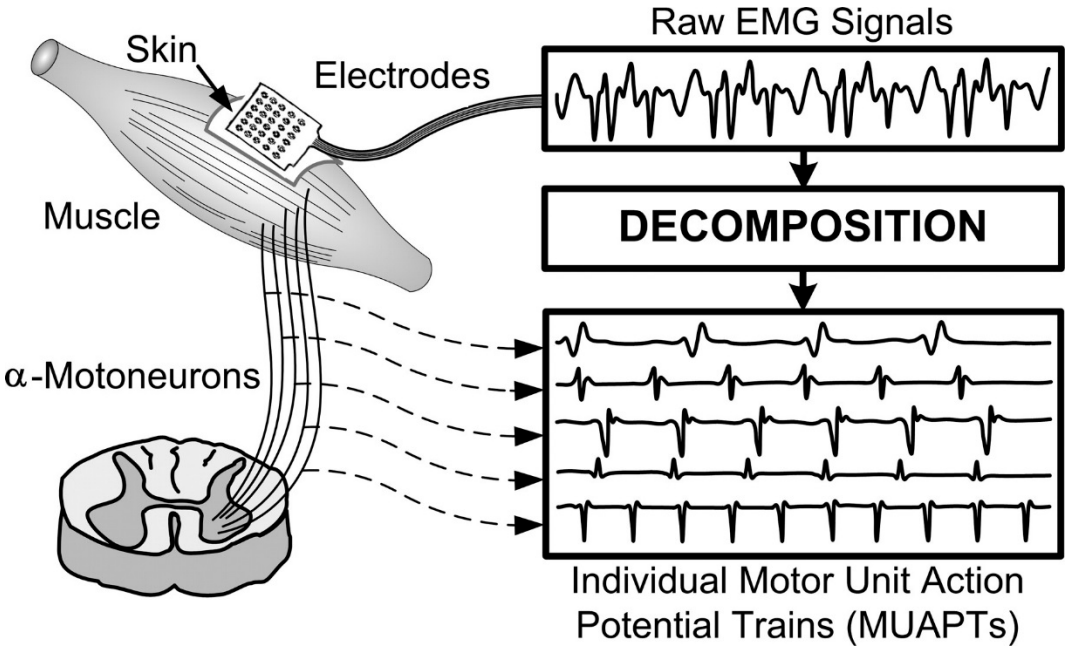

Figure1.2: Pictorial outline of the decomposition of surface EMG signal into its constituent motor unit action potentials. Reproduced by courtesy of [9].

A decomposed EMG signal provides some of the information "hiding" in the EMG signal. The timing information provides a complete description of the interpulse interval, firing rate, and synchronization characteristics. The morphology of the shapes of the MU action potentials provides information concerning the anatomy and health of the muscle fibers.

However, the development of HD-sEMG detecting and recording system is considered to be quite behind technologies nowadays. It is necessary to develop a new generation HD-sEMG detecting and recording device in order to meet the requirement in more channel, higher resolution and portable, which is why the design of an advanced portable system for high density surface EMG recording with wireless control of signal quality is proposed.

State of the art of key technologies and solutions related to the design the advanced portable system for high density surface EMG recording with wireless control of signal quality (HD-sEMG RSWC) is presented in **Figure1.3**.

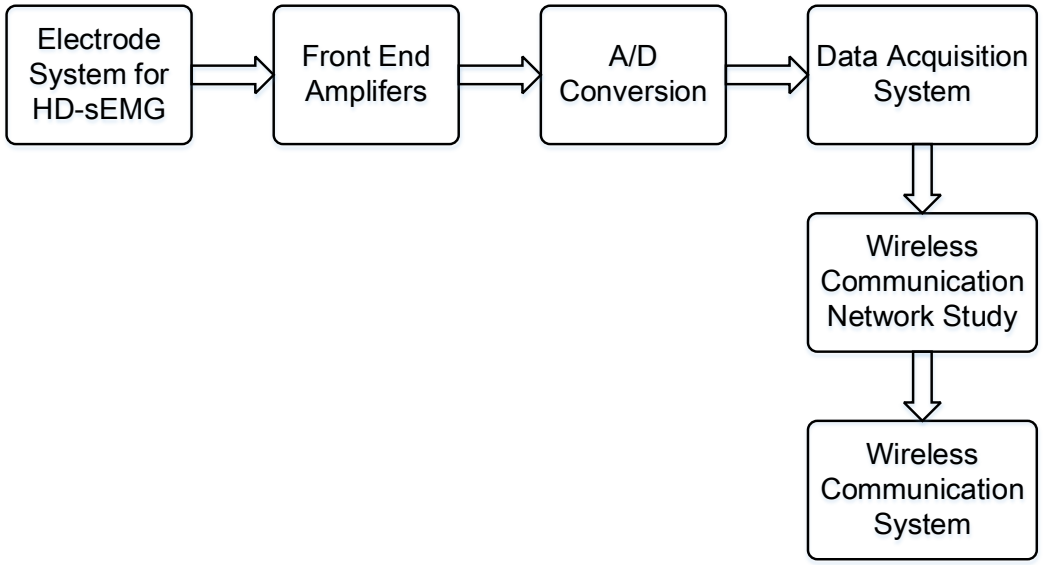

Figure1.3: Diagram of key technologies and solutions that are related to the design of the advanced portable system for high density surface EMG recording with wireless control of signal quality (HD-sEMG RSWC)

1.2 Electrode System for HD-sEMG

HD-sEMG is a technique for evaluating and recording the electrical activity produced by muscles by placing a 2-dimensional (2D) grid comprising many closely spaced electrodes (3~10 mm center-to-center), instead of just a few electrodes, on the muscles. This information is sometimes overlapping, but often complementary to the information extracted by needle EMG. Such 2D electrode grid principle was first described by Masuda et al [10].

Advantage of HD-sEMG over intramuscular EMG, apart from the non-invasiveness

and the relative ease of obtaining spatial distributions of electrical muscle activity, is its high reproducibility in follow up studies.

There are mainly two categories of 2D electrodes grid which are widely used for HD-sEMG detection: dry electrodes grid and flexible electrodes grid [11]. The advantages of dry electrodes grid are a fast application and, related to that, the ease of replacing the grid to find an optimal recording position. However, dry electrode grids are somewhat uncomfortable during longer use or when used in sensitive areas such as the face. Furthermore, absence of electrode gel may cause less optimal or even failing contacts. And flexible electrodes grid are dependent on a good contact via electrode gel application and can even be used in the more sensitive skin areas even with uneven contours [12][13]. Their signal to noise ratio is improved compared to dry electrodes and these grids can even be used in dynamic conditions [14]. The selected 64-channel flexible electrode grid with 10mm Inter-Electrodes Distance (IED) for HD-sEMG detection is depicted in **Figure1.4**.

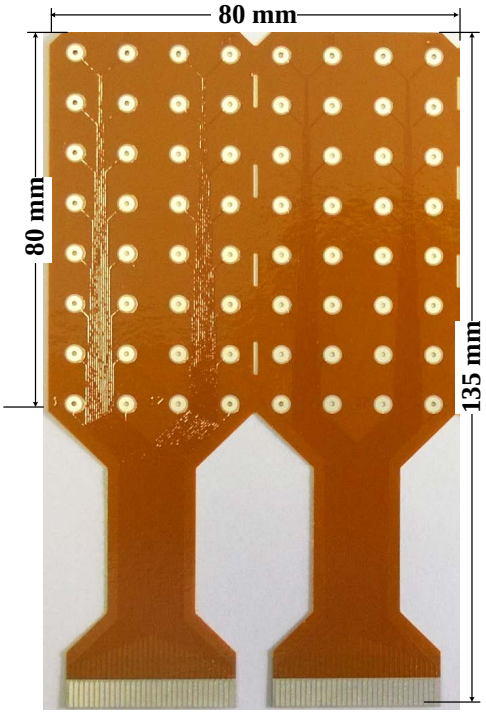

Figure1.4: Dimension of the 64-channel flexible electrode grid for HD-sEMG detection (designed at LISiN). This grid is organized in 8 by 8 matrix (IED=10mm) and can cover an area of 80x80 mm^2. The vertical light lines between the first (from left to right) and the second columns represent the wire connections to 32-channel pins (bottom). These 32-channel pins are connected to connector (designed at LISiN) with 32-wire cable as analog inputs to HD-sEMG detection system.

The number of electrodes and their IED of a flexible electrodes grid used for HD-sEMG detection is varied and depended on the targeted muscles and applications. Considering a fixed IED = 10mm, the areas that different number of electrodes can cover, are presented in **Table1.1**.

Table1.1: Areas covered by different flexible electrode grids. A 16-channel flexible electrodes grid with 4 by 4 array can cover an area of 40 x 40 mm^2, or cover an area of 20 X 80 mm2 with 2 by 8 array. A 64-channel flexible electrodes grid with 8 by 8 array can cover an area of 80 x 80 mm^2.

Flexible Electrodes Grid	Array	Area (mm^2)
16-channel	4 by 4 2 by 8	40 x 40 20 x 80
32-channel	4 by 8	40 x 80
64-channel	8 by 8	80 x 80

As shown in **Table1.1**, a 64-channel flexible electrodes grid with 8 by 8 array (IED=10mm) can cover an area of 80 x 80 mm^2. And this area can cover more than one muscle in the forearm, e.g. extensor carpi ulnaris (ECU), extensor digitorum communis (EDC) and extensor carpi radialis brevis (ECRb) and extensor carpi radialis longus (ECRl), if placed from 10% to 40% of the forearm length (see **Figure5.11**).

1.3 Front End Amplifiers

Original HD-sEMG signals are contaminated by various noises. Two important types of these noise are ambient noise and transducer noise [15]. Ambient noise is generated by electromagnetic devices such as computers, force plates, power lines etc. Essentially any device that is plugged into the wall A/C (Alternating Current) outlet emits ambient noise. This noise has a wide range of frequency components, however, the dominant frequency component is 50Hz or 60Hz, corresponding to the frequency of the A/C power supply (i.e. wall outlet). Transducer noise is generated at the electrode-skin junction. Electrodes serve to convert the ionic currents generated in muscles into an electronic current that can be manipulated with electronic circuits and stored in analog form as a voltage potential. There are two types of noise sources that result from this transduction from an ionic to an electronic form [16][17].

- D/C (Direct Current) Voltage Potential. It is caused by differences in the impedance between the skin and the electrode sensor, and from oxidative and reductive chemical reactions taking place in the contact region between the electrode and the conductive gel.
- A/C (Alternating Current) Voltage Potential. It is generated by factors such as fluctuations in impedance between the conductive transducer and the skin. One

effective method to decrease impedance effects is to use Ag-AgCl electrodes. This electrode consists of a silver metal surface plated with a thin layer of silver chloride material.

An AFE is a set of analog signal conditioning circuitry that uses operational amplifiers, filters as well as application-specific integrated circuits to provide analog outputs. Technological developments have decreased the level of noise in the EMG signal. The most important development was the introduction of the bipolar recording technique. Bipolar electrode arrangements are used with a differential amplifier, which functions to suppress signals common to both electrodes. Essentially, differential amplification subtracts the potential at one electrode from that at the other electrode and then amplifies the difference.

Two possible AFE solutions to design the HD-sEMG RSWC are discussed in **SECTION 2.3.2**.

1.4 A/D Conversion

An analog digital converter (ADC) is used to digitize the output (voltage) of AFE into digital values. Successive-Approximation-Register (SAR) analog-to-digital converters (ADCs) are frequently the architecture of choice for medium-to-high-resolution applications with sample rates under 5 Msps. Resolution for SAR ADCs most commonly ranges from 8 to 16 bits, and they provide low power consumption as well as a small size. This combination of features makes SAR ADCs ideal for a multiplexed DAQ system.

As the name implies, the SAR ADC basically implements a binary search algorithm. Therefore, while the internal circuitry may be running at several MHz, the ADC

sample rate is a fraction of that number due to the successive-approximation algorithm. Although there are many variations for implementing a SAR ADC, the basic architecture is quite simple [18] (see **Figure1.5**).

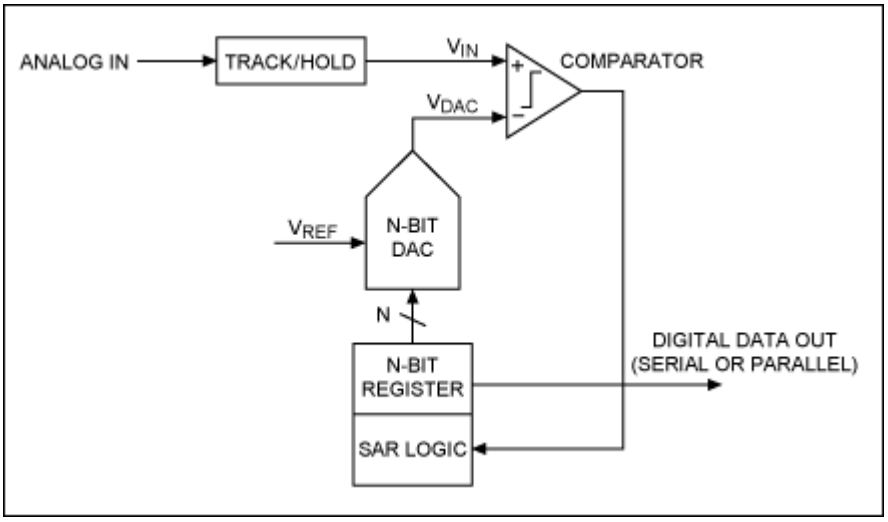

Figure1.5: Simplified N-bit Successive-Approximation-Register (SAR) ADC architecture. The analog input voltage (V_{IN}) is held on a track/hold. To implement the binary search algorithm, the N-bit register is first set to midscale (that is, $(100... .00)_2$, where the MSB is set to 1). This forces the DAC output (VDAC) to be $V_{REF/2}$, where V_{REF} is the reference voltage provided to the ADC.

As shown in **Figure1.5**, a comparison is then performed to determine if V_{IN} is less than, or greater than, V_{DAC}. If V_{IN} is greater than V_{DAC}, the comparator output is a logic high, or 1, and the MSB of the N-bit register remains at 1. Conversely, if V_{IN} is less than V_{DAC}, the comparator output is a logic low and the MSB of the register is cleared to logic 0. The SAR control logic then moves to the next bit down, forces that bit high, and does another comparison. The sequence continues all the way down to the LSB. Once this is done, the conversion is complete and the N-bit digital word is available in the register.

Figure1.6 shows an example of a 4-bit conversion. The y-axis (and the bold line in the figure) represents the DAC output voltage. Notice that four comparison periods

are required for a 4-bit ADC.

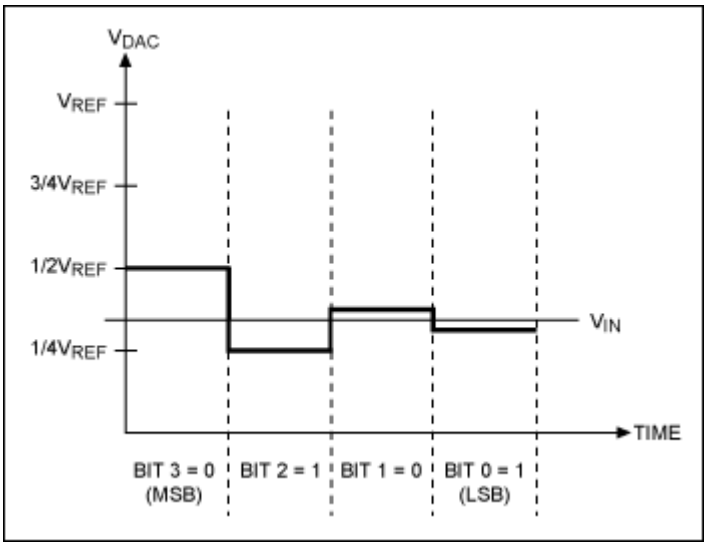

Figure1.6: Successive-approximation-register (SAR) ADC operation (4-bit example), redrawn from [18][15]. In the example, the first comparison between V_{IN} and V_{DAC} shows that $V_{IN} < V_{DAC}$. Thus, bit 3 is set to 0. The DAC is then set to $(0100)_2$ and the second comparison is performed. As $V_{IN} > V_{DAC}$, bit 2 remains at 1. The DAC is then set to $(0110)_2$, and the third comparison is performed. Bit 1 is set to 0, and the DAC is then set to $(0101)_2$ for the final comparison. Finally, bit 0 remains at 1 because $V_{IN} > V_{DAC}$.

Generally speaking, an N-bit SAR ADC will require N comparison periods and will not be ready for the next conversion until the current one is complete. This explains why these ADCs are power- and space-efficient, yet are rarely seen in speed-and-resolution combinations beyond a few Msps at 14 to 16 bits.

Two possible SAR ADC solutions to design the HD-sEMG RSWC are discussed in **SECTION 2.3.3**.

1.5 Data Acquisition System

1.5.1 General

Raw HD-sEMG signals collected with electrodes is of small amplitude (range between ±5mV) and typically the frequency content ranges between 20 and 500 Hz are contaminated by noise e.g. 50Hz power line interference. The Data acquisition system (DAQ) consisting of analog front end (AFE), analog digital converter (ADC) and other application-specific integrated circuits processes (amplification, analog signal filtering and conditioning) is used to acquire EMG signals.

1.5.2 Non-multiplexed DAQ Solution

Non-multiplexed DAQ system consists of multi-channel AFE and multi-channel ADCs, without multiplexer (see **Figure1.7**). Each channel of multi-channel Analog Front End (AFE) is connected to one input channel of analog digital converter (ADC).

A typical example is the WEMG DAQ system described in [19] (Barone, 2013). This DAQ solution consists of a 64-channel AFE and 8 chips of 8-channel ADC (ADS1278, 24-bit Δ - Σ ADC manufactured by Texas Instruments). In that design, 64-channel are sampled simultaneously so that no settling time among channel-to-channel. 64 chips of rail-to-rail driving amplifiers are implemented before 24-bit Δ - Σ ADC, provide an accurate LSB (Least Significant Bit) level 596nV with 10V Full Scale Range (FSR) under 1V/V gain.

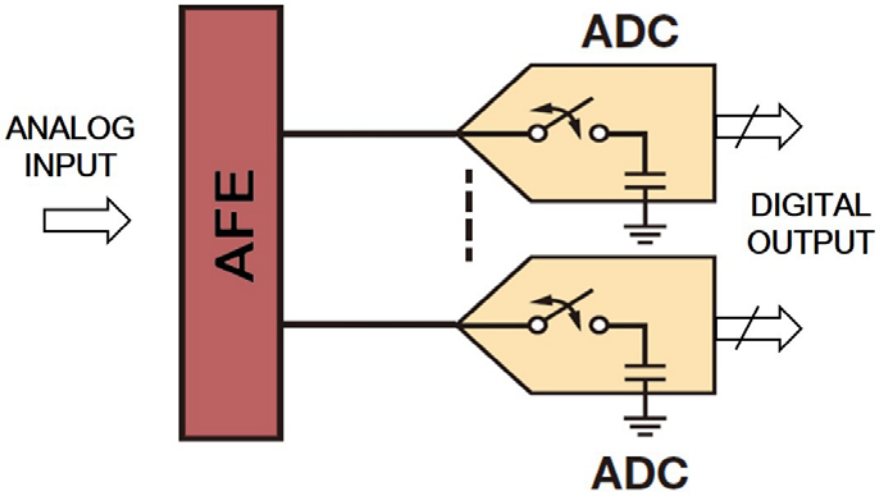

Figure1.7: Block diagram of non-multiplexed data-acquisition system. Each channel of multi-channel Analog Front End (AFE) is connected to one input channel of analog digital converter (ADC).

The advantages of a non-multiplexed DAQ system are: 1) Adopting high accuracy (24-bit resolution) low speed ADCs for signal digitizing, more bits acquired in each sample provides additional information for further analysis. 2) non-multiplexed DAQ system provides less signal distortion and has not influence of settling time introduced by a multiplexer.

1.5.3 Multiplexed DAQ Solution

Multiplexed DAQ system consists of multi-channel AFE, high speed multiplexer and ADCs. **Figure1.8** shows a block diagram of a data-acquisition system that includes an Analog Front End (AFE), a multiplexer and a successive-approximation-register (SAR) ADC.

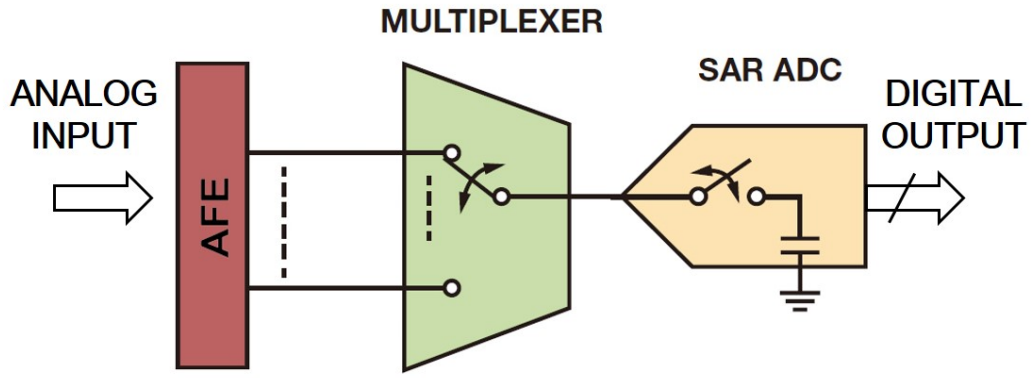

Figure1.8: Block diagram of a multiplexed data-acquisition system (DAQ). Each channel of multi-channel Analog Front End (AFE) is connected to one input channel of a high speed multiplexer. Only one channel of multiplexer is selected at one time, and other channels are switched off. Theoretically, when sample rate of a high speed Successive-Approximation-Register (SAR) ADC is able to be set 64 times faster than the sample rate of single channel, the multiplexed DAQ system is able to sample 64-channel with only one chip of single channel SAR ADC.

1.5.4 Solution Selection

The advantage of the non-multiplexed DAQ system is that it offers more information (by more bits achieved from higher resolution ADCs) and less signal distortion. However, it also has some disadvantages: first of all, the hardware cost to implement a non-multiplexed DAQ system is too high. Considering the unit price of ADS1278 chip is 38.06 euro (quoted price from RS Components Ltd, Italy), the total price of eight chips of ADS1278 (to implement a sixty-four channel DAQ system) achieved is 304.48 euro. More ADCs in the system also introduced problems like high power consumption and large physical size.

Conversely, the multiplexed DAQ solution has significant advantage in savings power, size, and cost. Meanwhile, it also has a disadvantage: it introduces system

delay between different channels. However, the system delay can be somehow compensated by adding system delay time into the computing of conduction velocity (CNV).

Consider all advantages and disadvantages of these two solutions, the multiplexed DAQ solution is selected for the design of HD-sEMG RSWC. Small (±5mV) differential voltage in raw EMG signal (without amplification) between adjacent inputs makes data acquisition system not prone to channel-to-channel crosstalk. Furthermore, a delay between the two channels is introduced by multiplexer (see **SECTION 2.3.3**), which makes the calculation of conduction velocity different from the non-multiplexed DAQ solution.

1.6 Wireless Communication Network Study

1.6.1 Wireless Communication Networks

A wireless network refers to any network not connected by cables, which is what enables the desired convenience and mobility for the user. In these networks, radio communication is usually the medium of choice. However, even within the radio-powered subset, there are dozens of different technologies designed for use at different scales, topologies, and for dramatically different use cases. One way to illustrate this difference is to partition the use cases based on their “geographic range”.

Table1.2: Types of wireless communication networks, revised from [20].

Type	Range	Applications	Standards
Personal area network (PAN)	Within reach of a person	Cable replacement for peripherals	Bluetooth, ZigBee, NFC (Near Field Communication), UWB (Ultra Wide Band)
Local area network (LAN)	Within a building or campus	Wireless extension of wired network	IEEE 802.11 (Wi-Fi)
Metropolitan area network (MAN)	Within a city	Wireless inter-network connectivity	IEEE 802.15 (WiMAX)
Wide area network (WAN)	Worldwide	Wireless network access	Cellular (UMTS, WCDMA, LTE, etc.)

The preceding classification in **Table1.2** is neither complete nor entirely accurate. Many technologies and standards start within a specific use case, such as Bluetooth for personal area network (PAN) applications and cable replacement, and with time acquire more capabilities, reach, and throughput. In fact, the latest drafts (Bluetooth 4.0) of Bluetooth now provide seamless interoperability with IEEE 802.11 (Wi-Fi) for high-bandwidth use cases. Similarly, technologies such as WiMAX have their origins as fixed-wireless solutions, but with time they acquired additional mobility capabilities, making them a viable alternative to other Wide area network (WAN) and cellular technologies.

Wide Area Network (WAN)

High-Speed Downlink Packet Access (HSDPA) and CDMA 1X EV-DO-B (Evolution-Data Only, version B) belong to Wide Area Network (WAN). HSDPA is an enhanced 3G (third-generation) mobile-telecommunications protocol in the High-Speed Packet Access (HSPA) family, which allows networks based on Universal Mobile Telecommunications System (UMTS) to have higher data speeds and capacity. The first phase of HSDPA has been specified in the 3rd Generation

Partnership Project (3GPP) release 5. Phase one introduces new basic functions and is aimed to achieve peak data rates of 14.0 Mbit/s. And further speed increases are available with HSPA+, which provides speeds of up to 42 Mbit/s downlink and 84 Mbit/s with Release 9 of the 3GPP standards [21]. CDMA2000 is a family of 3G mobile technology standards, uses CDMA (Code Division Multiple Access) channel access, to send voice, data, and signaling data between mobile phones and cell sites. CDMA 1X EV-DO-B (Evolution-Data Only, version B) can reach a throughput of 8.8Mbit/s download and 5.36 Mbit/s upload, with a target speed of 14.7 Mbps [22].

Metropolitan Area Network (MAN)

Worldwide Interoperability for Microwave Access (WiMax) belongs to Metropolitan area network (MAN). WiMAX standards provide an aggregate raw bandwidth up to about 70 Mbps per base station (BS), although the throughput is much less due to overhead, as well as issues of LOS, link distance, air quality, electromagnetic interference (EMI), radio frequency interference (RFI), and other signal impairments. Mobile network deployments described in 802.16e are expected to provide up to 15 Mbps of aggregate raw bandwidth within a cell radius of up to 3 kilometers [23].

Local Area Network (LAN)

IEEE 802.11 is a set of media access control (MAC) and physical layer (PHY) specifications for implementing wireless local area network (WLAN) computer communication in the 2.4, 3.6, 5 and 60 GHz frequency bands. Wi-Fi 802.11g works in the 2.4 GHz band (like 802.11b), but uses the same OFDM (Orthogonal Frequency-Division Multiplexing) based transmission scheme as 802.11a. It operates at a maximal physical layer bit rate of 54 Mbit/s exclusive of forward error correction codes, or about 22 Mbit/s average throughput [24]. 802.11n is an

amendment which improves upon the previous IEEE 802.11 standards by adding multiple-input multiple-output antennas (MIMO). IEEE 802.11n operates on both the 2.4 GHz and the lesser used 5 GHz bands, although support for 5 GHz bands is optional. It operates at a maximal net data rate from 54 Mbit/s to 600 Mbit/s with the use of four spatial streams at a channel width of 40 MHz [25].

Personal Area Network (PAN)

Bluetooth (Version 3.0 + HS) was adopted by the Bluetooth SIG on April 21, 2009 [26]. The High-Speed (HS) part of the specification is not mandatory, and hence only devices sporting the "+HS" will actually support the Bluetooth over Wi-Fi high-speed data transfer. A Bluetooth 3.0 device without the HS suffix will not support High Speed. Bluetooth 3.0+HS with AMP (Alternate MAC/PHY Manager) technique supports theoretical data transfer speeds of up to 100Mbit/s.

UWB, also called ultra-wide band, is a radio technology that can be used at very low energy levels for short-range high-bandwidth communications by using a large portion of the radio spectrum. UWB is a technology for transmitting information spread over a large bandwidth (>500 MHz) that should, in theory and under the right circumstances, be able to share spectrum with other users [27].

ZigBee is based on an IEEE 802.15 standard, including a suite of high-level communication protocols used to create personal area networks built from small, low-power digital radios. ZigBee has a defined rate of 250 Kbit/s which is best suited for intermittent data transmissions from a sensor or input device. However, 108 Kbit/s is the maxim throughput that in the test done by Burchfield, T.R et.al [28].

1.6.2 Previous Approach and Experience

A prototype for implementing data link solution for HD-sEMG DAQ system based on Ultra-wideband (UWB) wireless connection was designed by Zeinab Alipour Babaie in 2011 [29]. The prototype is a point-to-point solution, which consists of a sender and a receiver. The sender was implemented by one of a pair of UWB USB dongles (adapters) from Olidata S.p.A. (Italy) and a DLP-FPGA Module from DLP Design, Inc. (Texas, USA). The receiver was implemented by another UWB USB dongle and a laptop, functioning as the wireless data receiver. During the evaluation and testing of the prototype, at least two deficiencies were detected: 1) Wireless link between two UWB USB dongle was only stable in short range. Test result for 4.8 meter at 4 Mbit/s bit rate in 50 seconds showed the longest time that received valid data was only 13 seconds (between 11 and 24 second) and resets happened frequently (every 3 to 5 seconds). 2) Even working under short range (1.5 meter), data link was still too vulnerable to obstacles. During the test, a human being walking between the transmitter and the receiver would block the data link (reset happened).

Analyzing the failure of the solution based on UWB, two conclusions are: 1) Internal printable circuit board (PCB) antenna is apparently not suitable for a stable wireless communication. A high gain external antenna MUST be adopted in the future wireless communication solution to make the wireless communication more stable and less vulnerable to obstacles. 2) The wireless network including a pair of low power consumption sender and receiver limits the radio range of the wireless communication, and should not be considered as an ideal wireless solution.

1.6.3 Wireless Network Selection

As mentioned in the previous section, there are mainly four kinds of wireless communication solution: personal area network (PAN), local area network (LAN), metropolitan area network (MAN) and wide area network (WAN).

Obviously, the most advantageous criteria to select a WAN or MAN is the characteristics of ubiquitous connectivity in deploying the DAQ system inside the network's radio range. However, the quality of such wireless network depends intensively on the service provided by local mobile operator and is very likely to be influence by the obscuration of buildings, if implemented as an indoor wireless communication solution. Furthermore, such wireless networks need a subscriber identity module (SIM) card, which increases developing time as well as developing cost if employing WAN or MAN network for our DAQ system.

Conversely, deploying of the PAN network is much simpler. Like UWB, Bluetooth and Zigbee, the deploying method is usually a point-to-point method: a sender and a receiver. Obviously, those point-to-point networks have less deploying cost both in time and in price. However, ultra-low power wireless networks like UWB, Bluetooth and Zigbee, have disadvantage in less stable and shorter radio range. The wireless network that only including a pair of low power consumption sender and receiver itself limits the radio range of the wireless communication, and should not be considered as an ideal wireless solution to design our system.

Furthermore, **Figure1.9** depicts a comparison of LAN (Wi-Fi) wireless network over point-to-point wireless network (e.g. Bluetooth) in radio range. Assumed that the radio ranges of sender and receiver are fixed at 5 meter radius, the maxim distance between a sender and a receiver is only 5 meter in point-to-point wireless network.

However, by introducing an access point in the middle of a Wi-Fi wireless network, the distance between a sender (such as HD-sEMG RSWC) and a receiver (such as a laptop) increases to 10 meter.

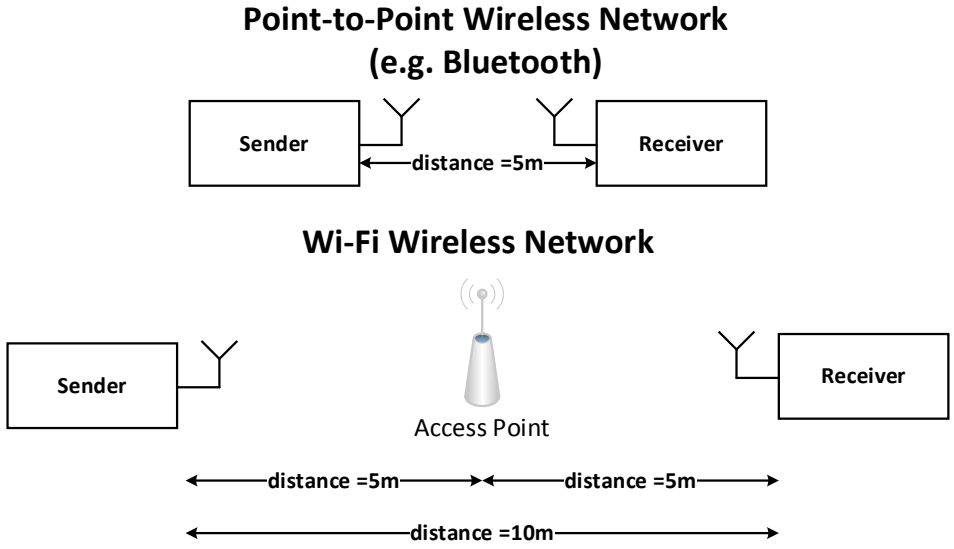

Figure1.9: A comparison between Point-to-Point wireless network and Wi-Fi wireless network with an access point. Assumed that the radio range of sender and receiver are 5 meter radius, the maxim distance between a sender and a receiver is only 5 meter in point-to-point wireless network. Conversely, by introducing an access point (radio radius= 5m) in the middle of a Wi-Fi wireless network, the radio distance between a sender and a receiver increases to 10 meter maximal.

In practical, the radio range covered by an AP is larger compared to Bluetooth devices. Furthermore, Wi-Fi 802.11network has more advantages as following: 1) Wi-Fi networking cost is relatively low as the price of an Access Point (AP) is around 200 euro, which is sufficient to establish a simple wireless Local Area Network (LAN). 2) AP provides a high performance wireless network between a sender and a receiver both in throughput and stability. Typically, a wireless AP equipped with a high-gain antenna (Wi-Fi 802.11b/g/a) or multiple-input multiple-output antennas (Wi-Fi 802.11n), can significantly increase the stability of the wireless link and radio range. From both theoretical and practical point of view, Wi-Fi wireless network can reach higher throughput with more stability compared to

point-to-point network (e.g. Bluetooth) and is selected as wireless communication network in the further design of our system.

1.7 Wireless Communication System

1.7.1 General

Digitalized surface EMG signals from DAQ can be transferred wirelessly through a wireless communication system (WCS) for visualization. Visualization of HD-sEMG signal gives us a feedback which can be used to control signal quality by detecting: 1) strong noise source e.g. 50Hz power line interference; 2) bad contact of electrode-gel-skin interface during measurement.

To design our wireless communication solution, preliminary investigation and literature review some of the commercial available wireless network is done. Furthermore, two different solutions are investigated in this section, including: 100% wireless solution and 10% wireless solution. Requirement of the wireless throughput depends on the number of channels, sample rate, the resolution of an ADC and also the solution selected.

1.7.2 Solution A: 100% Wireless Solution

In Solution A (100% wireless solution), 100% of the digitalized surface EMG signals acquired from DAQ will be transferred wirelessly. The throughput of this solution is computed by the following equation.

$$\text{Througput} = \text{NCH} \times \text{NBIT} \times \text{Sample Rate} \qquad (1\text{-}1)$$

Where, NCH is the number of channels and NBIT is the resolution of an ADC.
The results of throughput according to different NCH and NBIT under 2000 SPS sample rate under equation 1-1 are presented in **Table1.3**.

Table1.3: Raw data throughput depends on the number of channels (NCH), the resolution of ADC (NBIT) as well as sample rate, see equation (1-1). With 16-bit resolution and 2000 SPS (Sample per Second) sample rate, the approximate estimation of required bit rate for data samples retrieving of one surface EMG electrode array (sixty-four channels) is 2.048 Mbit/s, and for 512 channels is 16.384 Mbit/s.

NBIT / NCH	12-bit	16-bit	24-bit	Unit
32	0.768	1.024	1.536	Mbit/s
64	1.536	2.048	3.072	Mbit/s
128	3.072	4.096	6.144	Mbit/s
256	6.144	8.192	12.288	Mbit/s
512	12.288	16.384	24.576	Mbit/s

As shown in **Table1.3**, the minim throughput is 0.768 Mbit/s (32-channel, 2000 SPS sample rate and 12-bit) and the maxim throughput is 24.576 Mbit/s (512-channel, 2000 SPS sample rate and 24-bit).

1.7.3 Solution B: 10% Wireless Solution

The target of displaying of HD-sEMG signal online through wireless communication system is to check the signal quality before and during acquisition. From the experience of off-line analysis, surface EMG signals are usually displayed in a zoom in manner, which takes 100ms as the full time scale, to check the signal quality. The information inside 100ms is already able to detect: 1) whether the electrodes or device is too close to a strong noise source (e.g. 50Hz power line interference); 2) whether the electrodes placed on the skin of subject have bad contact of electrodes-gel-skin interfaces. So that 10% wireless solution was proposed as Solution B, in which only 10% (first 100ms of every second) of the digitalized surface EMG signals acquired from DAQ will be transferred wirelessly.

The throughput required by solution B (10% wireless solution) is computed by the following equation.

$$\text{Througput} = 10\% \times \text{NCH} \times \text{NBIT} \times \text{Sample Rate} \quad (1\text{-}2)$$

Where, NCH is the number of channels and NBIT is the resolution of an ADC.

The results of throughput according to different NCH and NBIT under 2000 SPS sample rate under equation 1-1 are presented in **Table1.4**.

Table1.4: Wireless data throughput (10% of raw data throughput) depends on the number of channels (NCH), the resolution of ADC (NBIT) as well as sample rate, see equation(1-2). With 16-bit resolution and 2000 SPS (Sample per Second) sample rate, the approximate estimation of required bit rate for data samples retrieving of one surface EMG electrode array (sixty-four channels) is 0.2048 Mbit/s, and for 512 channels is 1.6384 Mbit/s.

NBIT / NCH	12-bit	16-bit	24-bit	Unit
32	0.0768	0.1024	0.1536	Mbit/s
64	0.1536	0.2048	0.3072	Mbit/s
128	0.3072	0.4096	0.6144	Mbit/s
256	0.6144	0.8192	1.2288	Mbit/s
512	1.2288	1.6384	2.4576	Mbit/s

As shown in **Table1.4,** the minim throughput achieved is 0.0768 Mbit/s (32-channel, 2000 SPS sample rate and 12-bit resolution) and the maxim throughput achieved is 2.4576 Mbit/s (512-channel, 2000 SPS sample rate and 24-bit resolution). Although the requirement of throughput decreased significantly in this solution, low power wireless device like Bluetooth USB Adapter is NOT recommended and should not be used in our application. Low power Bluetooth device has limitation in transmitter power such as Bluetooth Power Class 2 (maximum output power: 2.5 mW in maximum; nominal output power: 1 mW; minimum output power: 0.25 mW) and

usually only equipped with an internal PCB antenna, resulting in unstable and low speed in practical test [30]. Check section 1.6.3 for more advantages of Wi-Fi over Bluetooth.

1.7.4 Wireless Solution Selection

Key criteria to select a proper solution for our application include: 1) Stability; 2) the influence introduced by wireless packet loss and 3) power consumption requirements.

Stability. The way that a wireless communication system dealing with continuous data make a wireless communication system less stable compare to a wireline communication system. A simplified procedure how a wireless communication system dealing with continuous data is depicted in **Figure1.10**.

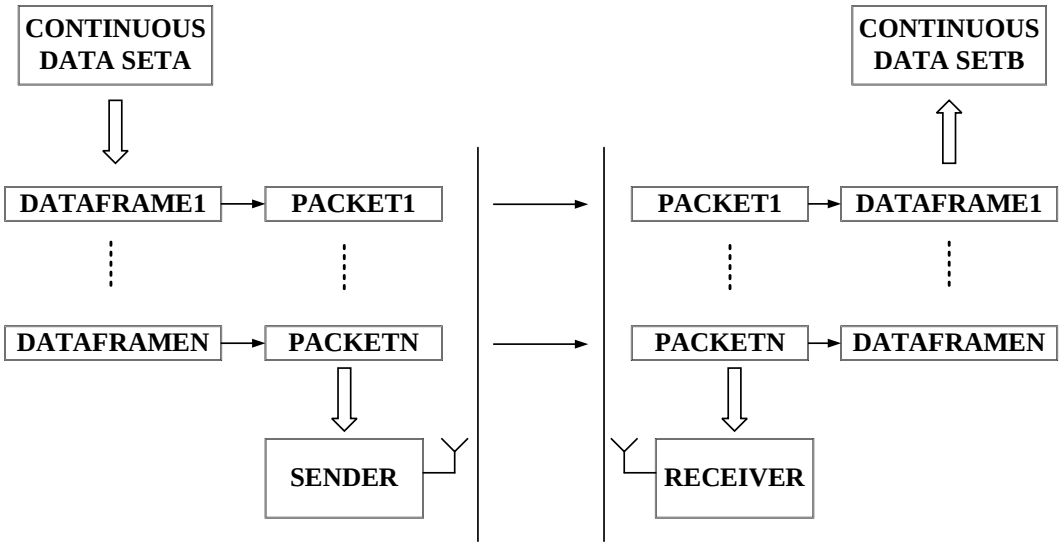

Figure1.10: Block diagram of a simplified (unidirection) wireless communication system dealing with continuous data. As shown in the left side, CONTINUOUS DATA SETA first divided into data frames (the maxim size of data frame depends on the protocol implemented by wireless communication system. E.g. The maxim size of data frame of Wi-Fi 802.11 b/g is 1400 bytes). And one data frame plus packet header and packet footer form one packet (e.g. PACKET1, … PACKETN). A sender transmits data wirelessly packet by packet, while a

receiver (at the right side) also receives the data packet by packet. Receiver extracts raw data dataframe by dataframe from packets (by removing the header and footer of each packet) and those dataframes compose of CONTINUOUS DATA SETB. In an ideal environment without packet loss, CONTINUOUS DATA SETA and CONTINUOUS DATA SETB should be the same.

Figure1.10 demonstrates how continuous data transceived in an ideal environment which has only a pair of sender and receiver and not be contaminated by noise. However, this ideal environment never exists in practical application. **Figure1.11** depicts how packet collisions and packet loss happen in a three pair of transceiver environment.

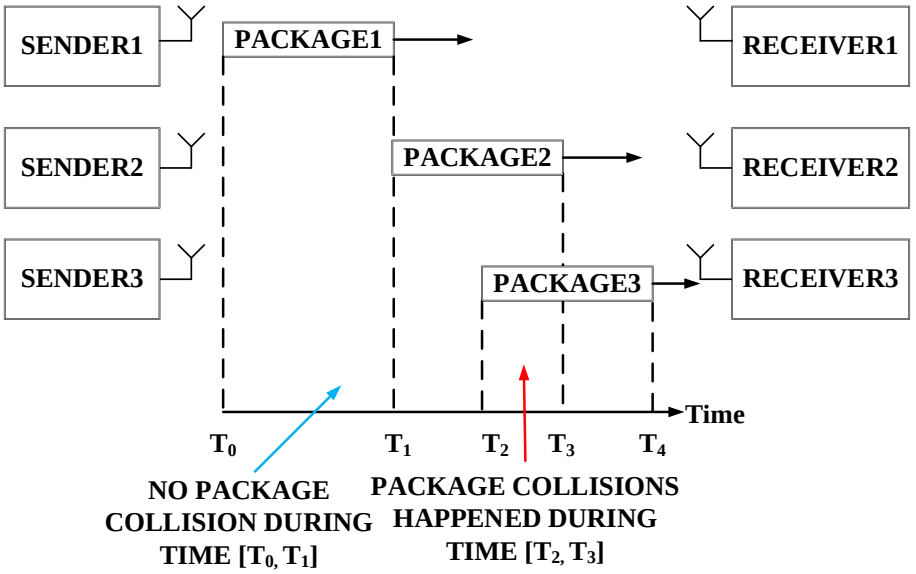

Figure1.11: Block diagram that shows how packet collisions and packet loss happen in a three pair of transceiver environment. PACKET1 transmitted by SEND1 during time [T_0, T_1], PACKET2 transmitted by SEND1 during time [T_1, T_3], PACKET3 transmitted by SEND1 during time [T_2, T_4]. No collision should happen during time [T_0, T_2], since only PACKET1 existing in the entire environment. However, packet collisions was bound to happen during time [T_2, T_3], since PACKET2 and PACKET3 are using the same radio frequency. Furthermore, packet loss should be detected by RECEIVER2 and RECEIVER3.

Because more than a pair of sender and receiver are working in the same time at same radio range and radio environment always be contaminated by noise in practical application, packet collision and packet loss in wireless communication system is almost inevitable. Furthermore, the more packets traveled (in the same

time duration at the same radio range), the greater possibility packet collision and packet loss happened. In this way, solution A is less stable than solution B, since solution requires ten times more packets than solution B.

Influence introduced by wireless packet loss. Influence that introduced by packet loss only affects a wireless solution. All data received by receiver without data loss in wireless communication level is mandatory to the wireless solution, since wireless communication system is the only way for recording data. Although packet loss is not equal to data loss (because packet loss in the wireless communication is detectable and lost packet can be re-transmitted again and again until received successfully by receiver), the influence introduced by wireless packet loss is still significant: packet loss detection and data recover protocol consume some wireless bandwidth which reduce wireless throughput at the end. In the worst case, data loss still happens, if all wireless bandwidth runs up. Obviously, the packet loss in wireless phase has no influence to the data recorded locally in memory.

Power consumption requirements. Wireless communication system is a part of the new advanced battery-powered multi-channel HD-sEMG recording system and power consumption is a key criteria in solution selection as well.

The power consumption of 100% wireless solution (solution A) and 10% wireless solution (solution B) is calculated by the following equation.

$$P_{SOLUTION\ A} = P_{COMMON} + P_{WIRELESS\ A} \quad (1\text{-}3)$$

$$P_{SOLUTION\ B} = P_{COMMON} + P_{WIRELESS\ B} + P_{SD} \quad (1\text{-}4)$$

Where, P_{COMMON} is a sum of power consumption of common modules (e.g. data acquisition system and micro control unit). $P_{WIRELESS\ A}$ and $P_{WIRELESS\ B}$ is the average power consumption of wireless module working in transfer mode and

standby mode of solution A and solution B. P_{SD} is the power consumption of SD memory card.

Power consumption of SD cards varies by its speed mode, manufacturer and model. During transfer it may be in the range of [66,330] mW ([20,100] mA at a supply voltage of 3.3 V) [31]. Standby current is much lower, less than 0.2 mA for one microSD card [32].

$P_{SOLUTION\ A}$ and $P_{SOLUTION\ B}$ depends on which type of wireless module as well as SD memory card using in the system. The wireless module selected is XBee S6B (manufactured by iDigi International) and the SD memory card selected is SanDisk micro-SD (type class10, 16Gbyte capacity), which is discussed in section 2.3 and 2.4 of this thesis. Considering the approximate estimation of $P_{COMMON,}$ $P_{WIRELESS\ A}$, $P_{WIRELESS\ B}$ and P_{SD} is 1.6W, 0.7W, 0.37W and 0.03W, the power consumption $P_{SOLUTION\ A}$ is at least 15% higher than $P_{SOLUTION\ B}$.

Conclusion. Considering stability, the influence introduced by wireless packet loss as well as power consumption, solution B (that a portion [10% of every second] of data transferred wirelessly for on-line visualization and all data set recorded in a SD memory card for off-line analysis) is better than solution A (all data set transferred wirelessly for both on-line visualization and off-line analysis) in our application. Since solution B (10% wireless solution) is adopted in the design of HD-sEMG RSWC, a data recording system (DRS) that recording all data in a local memory for off-line analysis is necessary and is discussed in **SETION 2.4.** Furthermore, more details about the investigation of stand-alone Wi-Fi modules are discussed in **SETCION 2.5.**

1.8 Objectives of the Work

Despite the importance of HD-sEMG in many fields such as a valuable aid in discovering and diagnosing abnormalities not only in the muscles but also in the motor system as a whole, the development of HD-sEMG detecting and recording system is considered to be quite behind technology nowadays. It is necessary to develop a new generation HD-sEMG detecting and recording device in order to meet the requirements in more channels, higher resolution and portable, which is why the design of an advanced portable system for high density surface EMG recording with wireless control of signal quality (HD-sEMG RSWC) is proposed.

In this thesis, the methodologies to design the HD-sEMG RSWC is going to be studied. The design criteria of this system will be studied and be defined firstly. A system block diagram of the design that satisfied these defined criteria is going to be proposed. The subsystems, including data acquisition system, data recording system, Wi-Fi communication system and power supply unit, will be designed.

A prototype will be implemented to verify the design and its performances will be tested. The criteria to design a printed circuit board (PCB) for placement of all components selected will be studied and be defined. In addition, more components (including aluminum enclosure, power socket bulkhead and power plug) to enhance electromagnetic compatibility (EMC) and safety of the prototype will be studied. Moreover, user panels that help user to follow correct connection of the external connectors (charger, patient reference and so on) and check the work state will be studied. A firmware for the prototype will be developed.

Off-line signal processing of HD-sEMG signals acquired by the prototype will be studied. Furthermore, two physiological applications using this prototype are going

to be studied.

In the end, the technical advantages /disadvantages, the limitations and the future technologies of the prototype of HD-sEMG RSWC are going to be investigated and be presented.

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2

Design of an Advanced Portable System for High Density Surface EMG Recording with Wireless Control of Signal Quality

2.1 General

This section describes the methodologies to design the HD-sEMG RSWC. The design criteria of this system will be studied and defined firstly. A system block diagram of the design that satisfied these defined criteria is going to be proposed. The subsystems, including data acquisition system, data recording system, Wi-Fi communication system and power supply unit, will be designed.

2.2 Design Criteria and System Block Diagram

2.2.1 Characteristics of HD-sEMG

Main characteristics of sEMG signals [1] for designing the HD-sEMG RSWC are presented in **Table 2.1**.

Table 2.1: Main characteristics of sEMG signals

SYMBOL	DESCRIPTION	Value		UNITS
		MIN	MAX	
$V_{EMG\ AC}$	sEMG peak-to-peak voltage	5	5000	μV
$V_{EMG\ DC}$	sEMG electrode DC offset voltage		0.5	V
BW_{EMG}	Bandwidth of sEMG	10	500	Hz
Z_{EMG}	Input Impedance within sEMG bandwidth (10~500Hz)		100	MΩ
V_{nEMG}	RMS noise voltage with EMG bandwidth*	1	10	μV_{rms}
f_s	Sample frequency per each channel	1024		Hz

Note*: V_{nEMG} is make reference from [1].

2.2.2 System Requirements

The technical requirements of the HD-sEMG RSWC based on the main characteristics of sEMG signals are presented in **Table 2.2**.

Table 2.2: Technical requirements of the HD-sEMG RSWC.

SYMBOL	DESCRIPTION	Value			UNITS
		MIN	TYP	MAX	
N_{CH}	Number of EMG channels	32	64	512	number
ΔV_{EMG}	The EMG Voltage Accuracy	0.5[1]		1	μV
NBIT	The resolution of the ADC	12		24	bit
FSR	The full scale range of ADC	3.3		10	V
Gain	The voltage gain of Analog Front End (AFE)	100		1000	V/V
$CMRR_{50Hz}$	The Common Mode Rejection Ratio (CMRR) under 50Hz	85			dB
BW_{EMG}	Bandwidth of sEMG	10		500	Hz
f_s	Sample frequency (each channel)	1024			SPS
DR_{SYSTEM}	Raw data rate (from ADC)	0.768[2]		24.576[3]	Mbit/s
$DR_{WIRELESS}$	Raw data rate (for wireless communication module)	0.0768[4]		24.576[5]	Mbit/s

Note1: The minimum ΔV_{EMG} is calculated as 10% of the minimum value of sEMG peak-to-peak voltage (5μV).
Note2: The minimum DR_{SYSTEM} is 0.768 Mbit/s, which is calculated by 32 (channel) x 12 (bit) x 2000 (SPS).
Note3: The maximal DR_{SYSTEM} is 24.576 Mbit/s, which is calculated by 512 (channel) x 24 (bit) x 2000 (SPS).
Note4: The minimum $DR_{WIRELESS}$ is 0.0768 Mbit/s, which is calculated by 32 (channel) x 12 (bit) x 2000 (SPS) x 10%.
Note5: The maximal $DR_{WIRELESS}$ is 24.576 Mbit/s, which is calculated by 512 (channel) x 24 (bit) x 2000 (SPS).

2.2.3 System Block Diagram

Block diagram of the HD-sEMG RSWC is depicted in **Figure2.1**.

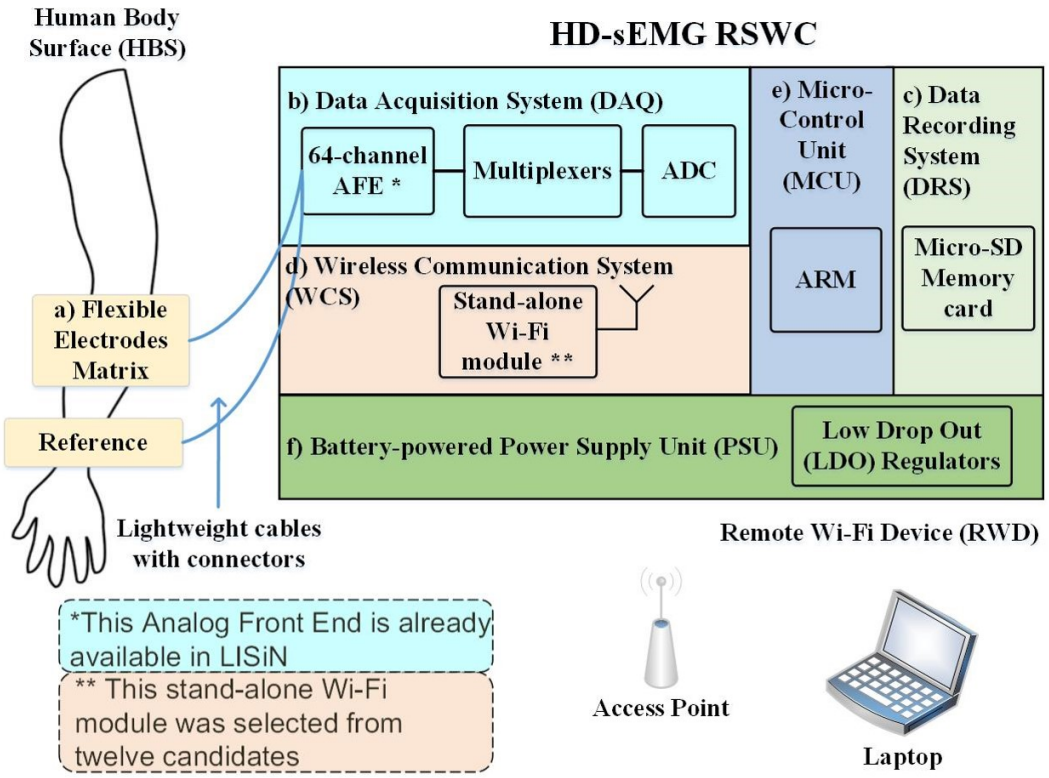

Figure2.1: Block diagram of HD-sEMG RSWC. This system could be described as the following blocks: a) Flexible electrodes matrix (FEM) is the interface placed on the human body surface (HBS) which detects EMG activities; b) data acquisition system (DAQ) consists of AFE, multiplexers and ADC, which performs surface EMG signals conditioning and A/D conversion; c) data recording system (DRS) records data acquired from DAQ with a SD memory card for off-line analysis; d) wireless communication system (WCS) transfers 1/10th of every second (first 100 ms) signals with a stand-alone Wi-Fi module for on-line visualization; e) micro-control unit (MCU) provides clocks and control signals to other sub-system e.g. DAQ, DRS and WCS; f) battery-powered power supply system provides power to all other blocks. Remote Wi-Fi devices such as laptop with real-time visualization software installed can be used to signal quality checking when linking to same access point (AP) in a simple network configuration (as presented).

2.3 Data Acquisition System

2.3.1 General

As discussed in **SECTION 1.3**, the multiplexed DAQ solution is selected for

advantage that multiplexing allows the use of fewer ADCs per system, offering significant savings in power, size, and cost. Furthermore, a high speed Successive approximation register (SAR) ADC with much lower latency (compare to ∑-Δ ADC) is adopted in the design of multiplexed systems because its fast response to a full-scale input step (in worst case) without any settling time issues. This multiplexed DAQ solution composes of Analog Front End (AFE), multiplexers and ADC (see **Figure2.1** block (b)). The requirement for delay between channel 1 and channel 64 should less than 500μs, if sampling at 2000 sample per second.

2.3.2 Analog Front End

An AFE is a set of analog signal conditioning circuitry that uses operational amplifiers, filters as well as application-specific integrated circuits to provide analog outputs to an ADC.

After investigation of available AFEs at LISiN, two AFE modules are considered suitable to implement a sixty-four channel AFE: HY-2 dual channel EMG hybrid front-end and 64-channel WEMG AFE.

HY-2 is a dual channel analog front-end featuring differential input, bandpass filtering and amplification, embedded on a tiny 20 mm x 10 mm hybrid module. All the components are housed on an alumina substrate, and the resistors are printed with thick film technology and are laser trimmed to 0.5% accuracy. Each of the two channels is designed to implement a complete single differential (SD) front-end for surface EMG signals detection [2]. Thirty-two HY-2 dual channel analog front-ends are achieved to implement a 64-channel AFE. And the technical data of HY-2 is presented in **Table 2.3**.

Table 2.3: Technical specification of the HY-2 dual channel Analog Front End module [2].

Parameter	Description	Value			Unit
		MIN	TYP	MAX	
N_{CH}	Number of channels		2		number
CMRR	Common Mode Rejection Ratio	74	90		dB
Z_{IN}	Input impedance		10^9 // 4		Ω // pF
$V_{n,\ RTI}$	Total noise voltage, referred to input			1	μV
G	Gain		-1000		V/V
f_{HP}	High-pass frequency, +40dB/dec roll-off		10		Hz
f_{LP}	Low-pass frequency, -40dB/dec roll-off		400[1]		Hz
V_{cc}	Power supply	±2		±15	V
L	Length of a single HY-2 module		20		mm
H[2]	Height of a single HY-2 module		10		mm
W	Width of a single HY-2 module		3		mm

Note1: If set low pass frequency to 400Hz, some information above 400Hz will lose.
Note2: Dimension H does not include the stand-off of the pins, which is 1mm.

The 64-channel WEMG AFE [3] is a multichannel AFE featuring differential input, bandpass filtering and amplification for sEMG, which was also developed by LISiN (2013). All the components are housed on two PCB boards. Each of the 64-channels is designed to implement both in monopolar (MP) mode and differential (SD) mode for surface EMG signals detection. Only one 64-channel WEMG AFE is achieved to implement 64-channel DAQ system for sEMG, instead of using thirty-two of HY-2 dual channel analog front-ends. The technical data of 64-channel WEMG AFE is presented in **Table 2.4**.

Table 2.4: Technical specification of the 64-channel WEMG Analog Front End [3].

Parameter	Description	Value			Unit
		MIN	TYP	MAX	
N_{CH}	Number of channels		64		number
CMRR	Common Mode Rejection Ratio	86	93	101	dB
V_{OFFSET}	The offset voltage of AFE output		2.5		V
Power Supply	5V 2.5V -2.5V			100 50 50	mA
G	Gain		+100 -100		V/V
f_{HP}	High-pass frequency, +40dB/dec roll-off		2[1]		Hz
f_{LP}	Low-pass frequency, -40dB/dec roll-off		3500[1]		Hz
L	Length		160		mm
H[2]	Height		10		mm
W	Width		145		mm

Note1: The bandwidth of 64-channel WEMG AFE is set to [2, 3500] Hz, and make the variation of the gain of different frequency inside the bandwidth [10, 500Hz] as little as possible.
Note2: Dimension H does not include the plastic protector, which has 10 mm thickness.

Two AFE modules were considered suitable to implement a sixty-four channel AFE: HY-2 dual channel EMG hybrid front-end (HY-2) and 64-channel WEMG AFE. However, the low pass cut-off frequency of the HY-2 is set to 400Hz, resulting in the loss of information inside the EMG bandwidth between 400Hz and 500Hz. Furthermore, the datasheet of 64-channel WEMG AFE (developed at 2013) indicates that it has higher performance (Common Mode Rejection Ratio, CMRR), less power consumption comparing to HY-2. So that the 64-channel WEMG AFE was selected to design the new DAQ system. The diagram of the 64-channel AFE is presented in **Figure2.2**.

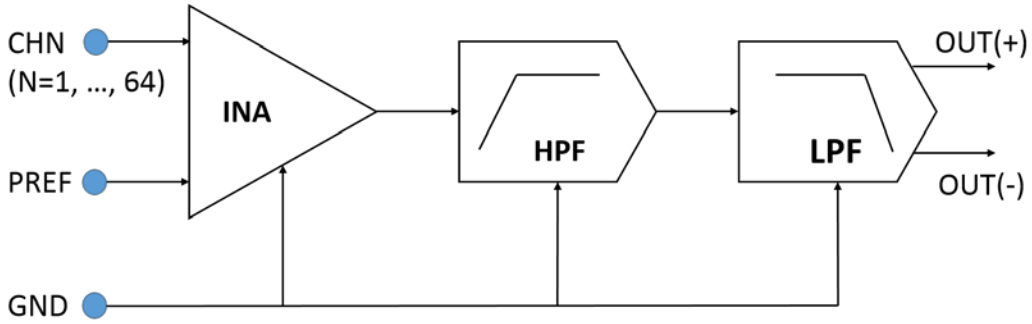

Figure2.2：AFE block diagram description, redrawn from [3]. The three stages highlight the basic features of the signal conditioning chain. The first block (INA, Instrument Amplifier) collects the differential signals between CHN (N=1, …, 64) and PREF (Patient Reference) by using INA333 from Texas Instrument. The second stage implements a Sallen-Key HPF (High Pass Filter) with 2Hz cut-off frequency by using OPA333 from Texas Instrument. The third stage implements a third order Bessel LPF (Low Pass Filter) with 3500 cut-off frequency by using THS4521 from Texas Instrument.

2.3.3 Multiplexer

High speed multiplexers are used to select each channel of AFE as the input of high speed SAR ADC at one time in order (from 1st channel to 64th channel) within the sampling time. **Figure2.3** describes main operations of the multi-channel HD-sEMG recording system with wireless communication (HD-sEMG RSWC) and its time requirements, which offers an approach to select a proper multiplexer for our application.

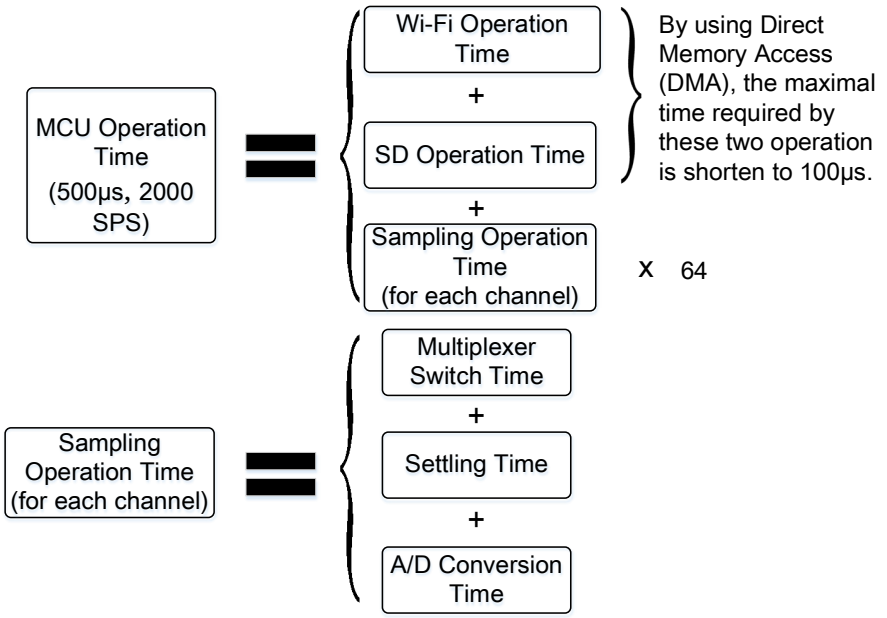

Figure2.3: Diagram of main operations of the HD-sEMG RSWC and their time requirements. The data acquisition system adopts 2000 SPS (sample per second) as its sample rate and leaves 500μs for a series of Micro-Control Unit (MCU) operation. These MCU operations include Wi-Fi operation, SD (memory card) operation and sampling operations (64 times). By using direct memory access (DMA), the maximal time required except sampling operation is shorten to 100μs. The average sampling operation time for each channel is around 6μs. The time required by sampling operation consists of multiplexer switching time, settling time and A/D conversion time.

In our application, multiplexer switching time and settling time as well as ADC conversion time are the shorter the better. Settling time is the time required for an instrument to provide a reading, within a given degree of accuracy (see **Figure2.4**). Multiplexer switching time should be more than 2.5μs (half of the max sampling operation time) and the shorter the better. Besides multiplexer switching time, R_{ON} (turn on resistor) is another critical standard to select a proper multiplexer for our application. The R_{ON} is the smaller the better.

After investigation some commercial available multiplexers (manufactured by Texas Instruments, Maxim Integrated, Linear Technology and Analog Devices) three high speed multiplexers that meet with the requirement of delay (see **Table2.5**)

MAX14661 (Maxim Integrated), LTC1380/LTC1393 (Linear Technology) and ADG726/732 (Analog Devices) were selected for further comparison

MAX14661 [4] is a serially controlled, dual-channel analog multiplexer allowing any of the 16 pins to be connected to either common pin simultaneously in any combination. The device features Beyond-the-Rails capability so that ±5.5V signals can be passed with any single supply between +1.6V and +5.5V. The serial control is selectable between I^2C and SPI. Both modes provide individual control of each independent switch so that any combination of switches can be applied. Its SPI mode includes a D_{OUT} pin that can be used to chain multiple devices together with a single select signal. The IC is available in a 28-pin (4mm x 4mm) TQFN packet and is specified over the -40ºC to +85ºC extended temperature range.

LTC1380 [5] is CMOS analog multiplexers with SMBus® compatible digital interface. The LTC1380 is a single-ended 8-channel multiplexer. The supply current is typically 10mA. Both digital interface pins are SMBus compatible over the full operating supply voltage range. The LTC1380 analog switches feature a typical R_{ON} of 35Ω (±5V supplies), typical switch leakage of 20pA and guaranteed break-before-make operation. The LTC1380 is available in 16-lead SO and GN packets.

ADG726 [6] is monolithic CMOS dual 16-channel analog multiplexer. It switches one of 16 inputs as determined by the 4-bit binary address lines A0, A1, A2, and A3. On-chip latches facilitate microprocessor interfacing. It may also be configured for differential operation by tying CSA and CSB together. An EN input is used to enable or disable the devices. When disabled, all channels are switched OFF. It operate from a single supply of +1.8 V to +5.5 V and a ±2.5 V dual supply, making them ideally suited to a variety of applications. On resistance is in the region of a

few ohms and is closely matched between switches and very flat over the full signal range. These parts can operate equally well as either multiplexers or demultiplexers and have an input signal range that extends to the supplies. In the OFF condition, signal levels up to the supplies are blocked. All channels exhibit break-before-make switching action, preventing momentary shorting when switching channels. They are available in either 48-lead CSP or TQFP packets.

Table 2.5: Technical data comparison of MAX14661 [4], LTC1380 [5] and ADG726 [6].

Multiplexer / **Parameter**	**MAX14661**	**LTC1380**	**ADG726**
Channels	16-Channel	8-Channel	16-Channel
Manufacturer	Maxim Integrated	Linear Technology	Analog Devices
Bandwidth (Max) (MHz)	60		34
Ron typical[1] (Ohms)	5.5	35	4
Supply voltage range	Single 1.6~5.5V/ Dual ±5.5V	Single 2.7V / Dual ±5V	Single 1.8~5.5V/ Dual ±2.5V
Turn-on time[2]	13µs	850ns	30ns
Power Requirements	I_{CC} (max) =200µA, while V_{CC}=3.3V	I_{CC} (max) =20µA, while V_{CC}=5V	I_{CC}(max) = 20µA, while V_{CC}=5.5V

Note1: The value of Ron typical is reference from datasheet [4][5][6].
Note2: The value of turn-on time is reference from datasheet [4][5][6].

In conclusion, ADG726 has the fastest turn-on (switching) time and the lowest power consumption comparing to other two products and is selected as the multiplexer for the further design.

Calculate settling time of ADG726 multiplexer

As mentioned in **SECTION 1.4**, the multiplexed DAQ solution allows use of fewer ADCs per system, offering significant savings in power, size, and cost. However,

the trade-off of multiplexed DAQ solution is the introducing of settling time. Settling time is the time required for an instrument to provide a reading, within a given degree of accuracy, when a monitored parameter varies [7]. Settling time includes a very brief propagation delay, plus the time required for the output to slew to the vicinity of the final value, recover from the overload condition associated with slew, and finally settle to within the specified error (see **Figure2.4**).

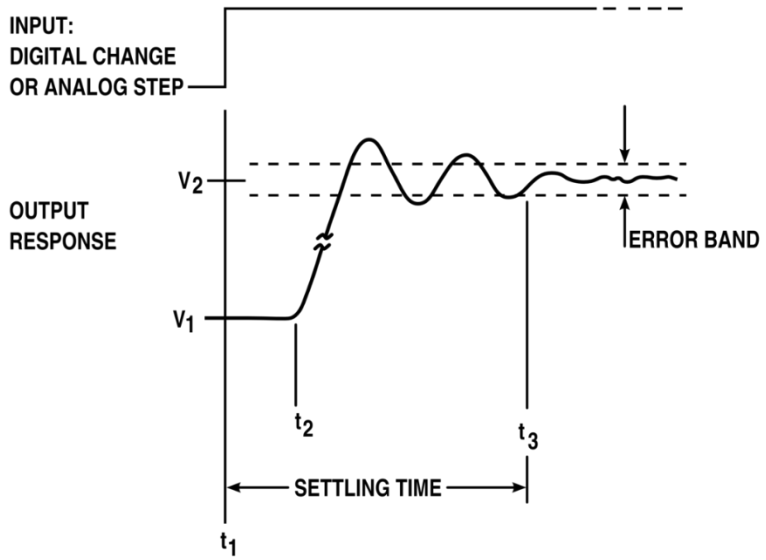

Figure2.4: Settling time is the time required for an output to reach and remain within a given error band following some input stimulus.

The error band (see **Figure2.4**) that set for settling time depends on the resolution of ADC (LSB). A rudimentary way of calculating how long a switch or multiplexer takes to settle can be estimated by calculating the RC for the device, that is, R_{ON} x C_D, and multiplying by the number of time constants for required system accuracy. This is added to the switch timing, T_{ON}, T_{OFF}, or $T_{TRANSITION}$, for the switch or multiplexer [8].

Time to Settle = Switching Timing + (R_{ON} x C_D x No. of Time Constants) (2-1)

Where, R_{ON} is the switch on resistance. C_D is the switch drain capacitance. No. of

Time Constants = −ln (% error/100). **Table 2.6** presents the number of time constants required to settle to 1 LSB accuracy for a single-pole system.

Table 2.6: Number of Time Constants [defined by equation (2-1)] required to settle to 1 LSB accuracy for a single-pole system [9].

Resolution, No. of Bits	LSB (%FS)	No. of Time Constants = −ln (% Error/100)
6	1.563	4.16
8	0.391	5.55
10	0.0977	6.93
12	0.0244	8.32
14	0.0061	9.70
16	0.00153	11.09
18	0.00038	12.48
20	0.000095	13.86
22	0.000024	15.25

Furthermore, a more convenient way to calculate the settling time of a multiplexer is by online calculator. **Figure2.5** presents the calculating results of settling time with the online tool provided by Analog Devices [9].

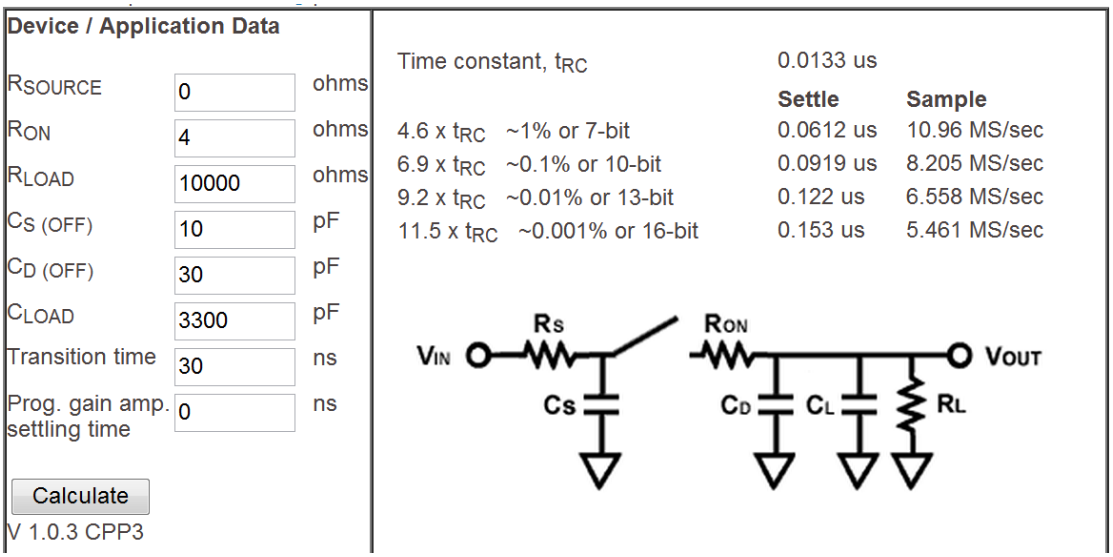

Figure2.5: Calculating settling time for ADG726 by online tool [9] with C_{LOAD} = 3300pF, Transition time =30 ns, R_{ON} =4 Ω. For 16-bit resolution ADC, the settling time introduced by multiplexer and load resistor (1MΩ) as well as load capacitor (3300pF) is 0.153μs.

Sampling of the channels

Sampling of the channels in the 64-channel multiplexed DAQ is presented **Figure2.6**. The delay between each channel is set to 5μs, in order to:

1) Eliminate the influence of setting time introduced by multiplexer;
2) Provide enough MCU operation time inside T (T= 500μs, when sample frequency is 2000) for Wi-Fi module and SD memory card.

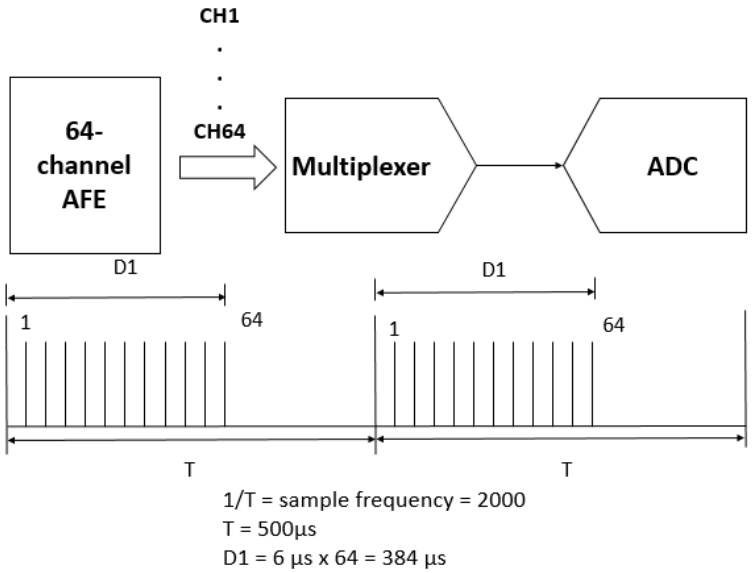

Figure2.6: Diagram of channels sampling in the 64-channel multiplexed DAQ. The delay between each channel is 5μs, so that only 384μs is required by 64-channel and more than 100μs is left to MCU for controlling Wi-Fi module and SD memory card.

2.3.4 Analog-to-Digital Converter

After investigation some commercial available multiplexers manufactured by Texas Instruments, Maxim Integrated, Linear Technology and Analog Devices, two high speed SAR ADC were selected for comparison: LTC2368-16 and LTC2370-16.

LTC2368-16 is a low noise, low power, high speed 16-bit successive approximation register (SAR) ADC [10]. Operating from a 2.5V supply, the LTC2368-16 has a 0V to VREF pseudo-differential unipolar input range with VREF ranging from 2.5V to 5.1V. The LTC2368-16 consumes only 13.5mW and achieves ±0.75LSB INL maximal, no missing codes at 16 bits with 94.7dB SNR. The LTC2368-16 has a high speed SPI-compatible serial interface that supports 1.8V, 2.5V, 3.3V and 5V logic while also featuring a daisy-chain mode. The fast 2Msps throughput with no cycle latency makes the LTC2368-16 ideally suited for a wide variety of high speed applications. An internal oscillator sets the conversion time, easing external timing considerations. The LTC2368-16 automatically powers down between conversions, leading to reduced power dissipation that scales with the sampling rate.

LTC2370-16 is a low noise, low power, high speed 16-bit successive approximation register (SAR) ADC [11]. Operating from a 2.5V supply, the LTC2370-16 has a 0V to VREF pseudo-differential unipolar input range with VREF ranging from 2.5V to 5.1V. The LTC2370-16 consumes only 19mW and achieves ±0.85LSB INL maximal, no missing codes at 16 bits with 94dB SNR. The LTC2370-16 has a high speed SPI-compatible serial interface that supports 1.8V, 2.5V, 3.3V and 5V logic while also featuring a daisy-chain mode. The fast 2Msps throughput with no cycle latency makes the LTC2370-16 ideally suited for a wide variety of high speed applications. An internal oscillator sets the conversion time, easing external timing considerations. The LTC2370-16 automatically powers down between conversions, leading to reduced power dissipation that scales with the sampling rate.

Table 2.7: Technical data comparison between two high speed Successive-Approximation-Register (SAR) ADC: LTC2368-16 [10] and LTC2370-16 [11].

ADC / Parameter	LTC2368-16	LTC2370-16
Channel	1 differential channel	1 differential channel
Sample rate (Max)	1Msps	2Msps
Resolution	16-bit	16-bit
Supply voltage	2.5V	2.5V
Input Range	0V to V_{REF}	0V to V_{REF}
V_{REF} Input Range*	2.5V to 5.1V	2.5V to 5.1V
I/O Voltages	1.8V to 5V	1.8V to 5V
Integral Linearity Error (Max)	±0.75LSB**	±0.85LSB
Power Requirements	13.5mW at 1Msps, 13.5μW at 1ksps	19mW at 2Msps, 19μW at 2ksps

Note*: This range must be higher than the max output (5.0V) of selected analog front end.
Note: LSB (Least Significant Bit) is the smallest unit of analog digital convertor.**

In conclusion, LTC2368-16 is selected as the ADC for implementing the DAQ system of the prototype, because it has less Integral Linearity Error (INL) as well as lower power consumption comparing to LTC2370-16, and 1Msps sample rate is sufficient for a 64-channel DAQ system with 2Ksps sample rate for each channel.

2.4 Data Recording System

2.4.1General

Functionality of data recording system (DRS) is to read sampled data (16-bit each sample) from DAQ through SPI bus and record them with a standard SD memory card through Secure Digital Input/Output (SDIO) bus (see **Figure2.1 block (c)**).

2.4.2 Evaluation and Testing of SD Card

An SD Card is a small flash memory card designed to provide high-capacity memory in a small size. SD cards are used in many small portable devices such as digital video camcorders, digital cameras, handheld computers, audio players and mobile phones. The technical data of some commercial available SD memory card are presented in **Table 2.8**.

Table 2.8: Technical Data of SD/SDHC/SDXC memory card, revised from [12]. Normal Speed (NS: 12.5MB/s); High Speed (HS: 25MB/s); Ultra High Speed-I (UHS-I: 50MB/s).

Standard / Parameter	SD Standard	SDHC Standard	SDXC Standard
Capacity	up to 2GB	more than 2GB up to 32GB	more than 32GB up to 2TB
File System	FAT 12, 16	FAT 32	exFAT
SD Memory Cards	SD	SD HC	SD XC
Card form factor	Full: 32 x 24 x 2.1 mm, Approx. 2g miniSD: 20 x 21.5 x 1.4 mm, Approx. 1g microSD: 11 x 15 x 1.0 mm, Approx. 0.5g		
Bus Speed	NS,HS	NS, HS UHS-I	NS, HS UHS-I

The binary file size of the raw data that generated by the 64-channel DAQ system is calculated by the following equation:

$$\text{Binary File Size (Raw Data)} = \text{NCH} \times \text{NBIT} \times \text{Sample Rate} \times \text{Sample Time} \quad (2\text{-}2)$$

Where, NCH is the number of channel; NBIT is the resolution of ADC; Sample Rate is the sample rate for each channel; Sample Time is the total time of sampling.

Table 2.9 shows the raw data capacity according to different sample time that achieved by storing all sampled data from DAQ system without any data

compression, while the 64-channel DAQ system running at 2000 SPS sample rate for each channel.

Table 2.9: Raw data capacity generated by the 64-channel DAQ system (at 2000 SPS sample rate for each channel and 16-bit resolution ADC).

Parameter / Time	The size of raw data	Unit
1s	0.256	Mbytes
1min (60s)	15.6	Mbytes
0.5h (1800s)	460.8	Mbytes
1h (3600s)	921.6	Mbytes

As presented in **Table2.9**, the capacity that generated in an hour measurement is 921.6 Mbytes. Furthermore, four commercial available SD memory cards with minim1GB capacity are investigated and the testing results are presented in **Table2.10.**

Table 2.10: Throughput testing results of four commercial available SD memory cards.

Throughput Test	**SD card using SPI[1]**	**Micro SD card using SDIO[2]**
Kingston 1G (SD card, class 4)	16 Mbps (Write) 20 Mbps (Read)	
Transcend 16G (SDHC card, class 10)	12 Mbps (Write) 20 Mbps (Read)	
Kingston 4G (micro SDHC card, class 4)		18 Mbps (Write) 25 Mbps (Read)
SanDisk 16G (micro SDHC card, class 10)		24 Mbps (Write) 30 Mbps (Read)

Note1: The test bench was built with Arduino Due board run at 84MHz SPI clock.
Note2: The test bench was built with MCU STM32F407 4-bit SDIO run at 42MHz clock.

As presented in **Table2.10**, the SanDisk 16G (micro SDHC card, class 10) had the highest writing speed under testing and selected as the SD card for further prototype.

2.4.3 File System

A file system is used to control how data is stored and retrieved. Without a file system, information placed in a storage area would be one large body of data with no way to tell where one piece of information stops and the next begins.

There are many kinds of file system, more than fifty, according to the list in [13]. FAT16 and FAT32 are two of them widely used in the most popular operation systems (Windows, UNIX and Linux). There are differences between FAT32 and FAT16 [14]: 1) FAT32 allows finer allocation granularity (approximately 4 million allocation units per volume). 2) FAT32 allows the root directory to grow (FAT16 holds a maximum of 512 entries, and the limit can be even lower due to the use of long file names in the root folder).

FAT16 can be used in MS-DOS, Windows 95, Windows 98, Windows NT, Windows 2000, and some UNIX operating systems. There are many tools available to address problems and recover data. It is efficient, both in speed and storage, on volumes smaller than 256 MB. Disadvantages of FAT16 are: The root folder can manage a maximum of 512 entries. FAT16 is limited to 65,536 clusters, but because certain clusters are reserved, it has a practical limit of 65,524. To maintain compatibility with MS-DOS, Windows 95, and Windows 98, a FAT16 volume should not be larger than 2 GB. FAT16 can waste file storage space in larger drives as the size of the cluster increases. The space allocated for storing a file is based on the size of the cluster allocation granularity, not the file size. A 10-KB file stored in a 32-KB cluster wastes 22 KB of disk space.

FAT32 belongs to the family of File Allocation Table (FAT) file systems, which is supported by almost all operating systems for personal computers, including all

versions of Windows [15]. The FAT file systems are therefore well-suited as a universal exchange format between computers and devices of most any type and age.FAT32 uses space more efficiently than FAT16. FAT32 uses smaller clusters (4 KB for drives up to 8 GB), resulting in 10 to 15 percent more efficient use of disk space relative to large FAT16 drives. FAT32 also reduces the resources necessary for the computer to operate. FAT32 is more robust than FAT16. FAT32 has the ability to relocate the root directory and use the backup copy of the FAT instead of the default copy. In addition, the boot record on FAT32 drives has been expanded to include a backup of critical data structures. This means that FAT32 volumes are less susceptible to a single point of failure than FAT16 volumes.

The file system that was adopted for SDHC card is FAT32 (see **Table 2.8**). The file size limit of FAT32 is close to 4 GB, and its file name has a limit of eight characters for a file name, and three characters for the extension (such as ".sig"). This is commonly referred to as the 8.3 filename limit [14]. For example, "XQ123456.sig" is a correct file name, while "XQ12345678.sig" will not be recognized as a correct file name because "XQ12345678" has ten letters which exceeds the limit of eight according to 8.3 filename limit.

An example of the configuration file is as following:

This file name is: QX0115; sample time in second is:5;
The name of abstract file. Abstract file is a file that used in LISiN to record the information of device, subject and measurement (such as which muscle).

This file is comprise of three parts, separated by semicolon. The first part ("**This file name is: QX0115"**) is the content before the first semicolon. It configures the file name of binary files stored the recording data in a standard: the first letter of name and surname of a subject (QX) and the data of the recording (0115 indicates

January 15). The second part (“**sample time in second is:5”**) is the content between the first and second semicolon. It configures the sample time of each acquisition in 5 seconds. In fact, it only have a length of 4.9 s, because the last 100ms will not be stored in SD memory card. The last part is the content after the second semicolon, which is used to add user define information for explanation of this file such as an abstract file describing the level of contraction, the muscle etc. The final part has not effect to acquisition itself and the length of this part is limited to 500 characters.

Finally, this configuration generates a series of recording file with file name started from “QX011501.sig” storing the data acquired during 5 seconds measurement. Where, “Q” is the first letter of the name of the subject; “X” is the first letter of the surname of the subject; “01” is the month; “15” is the date; “01” is the first measurement.

2.5 Wi-Fi Communication System

2.5.1 General

Wireless Communication System (WCS) transfers 10% of every second (first 100 ms) through a stand-alone Wi-Fi module for on-line analysis (see **Figure2.1 block (d)**).

Some commercial available Wi-Fi modules were investigated in this section, in order to implement a wireless communication system for transferring a portion (10% of every second) of acquired data set to another Wi-Fi powered device e.g. a laptop for online visualization. The Wi-Fi modules under investigation were low-power consumption modules, since the system is battery-powered.

2.5.2 Investigation of Wi-Fi Module

A list of commercially available low-power Wi-Fi modules, investigated, is presented in **Table2.11.**

Table2.11: List of the twelve commercial available Wi-Fi modules investigated. The Wi-Fi modules can be classified in two main groups, on the basis of integrating integrated TCP/IP protocol or not. The module integrated TCP/IP protocol within itself is called stand-alone Wi-Fi module. And another type of Wi-Fi module without integrated TCP/IP protocol is called "normal" Wi-Fi module, which requires an external MCU to implement TCP/IP protocol.

Item	Part Name	Manufacturer	
		MCU	Wi-Fi Module
1	Atmel Wi-Fi [17]	Atmel	H&D wireless
2	XBee Wi-Fi S6B [18]	Stand-alone	Digi International
3	Inventek Systems [19]	ST Microelectronics (STM32F205 @120MHz)	Broadcom 4319
4	WiFi Comm Demo Board [20]	Microchip 32-bit PIC32 microcontroller (PIC32MX695F512H @80MHz)	MRF24WB0MA
5	RTX4100 [21]	Energy Micro EFM32 Gecko Cortex-M3 MCU	Qualcomm Atheros AR4100
6	AM3517 SOM-M2 [22]	TI AM3517 (600 MHz)	TI WL1271

(Table is continued on the next page)

Table2.11: List of commercial available Wi-Fi modules investigated includes twelve modules in total. The Wi-Fi modules can be classified to two main group, on the basis of integrating integrated TCP/IP protocol or not. The one with integrated TCP/IP protocol within the Wi-Fi module called stand-alone Wi-Fi module. And another type of Wi-Fi module without integrated TCP/IP protocol cab be called as "normal" Wi-Fi module, which require an external MCU to implement TCP/IP protocol.

(Table continued from the previous page)

Item	Part Name	Manufacturer	
		MCU	Wi-Fi Module
7	Marvel Smart Energy Platform Solutions [23]	Marvel 88MC200 (ARM-M3) @ 200MHz	Marvel Avastar 88W878x
8	Qualcomm Atheros's SP137 development kit [24]	EFM32 Gecko (ARM-M3) from Energy Micro	Qualcomm Atheros AR4100P
9	WF121 Development Kit [25]	Microchip 32-bit PIC32 microcontroller (PIC32MX695F512H @80MHz)	Bluegiga
10	W2CBW0015 Dev Kit [26]	Wi2Wi WiFi/802.11 Development Tools	Marvel 8787
11	RS-WC-201/301[27]	Stand-alone	Redpine Signals
12	Nano WiReach [28]	CO2144 (ARM 7 by Connect One)	Marvel 8686

Since some solutions (solution 3, 6, 7, 8, 10 and 11) were discarded due to too long time (more than two months) in availability or delivery and some solutions (solution 1, 4 and 9) were proved to have low throughput (less than 1Mbps) in practical environment testing through technical consulting from their manufacturers, only solution 2 and 12 are selected for further evaluation.

Testing results of solution 12, Nano WiReach (manufactured by Connect One),

shown that throughput higher than 1Mbps could not be reach through UART (Universal Asynchronous Receiver/Transmitter) interface but only through RMII (Reduced Media Independent Interface) bus (with the support of windows operation system).

In the end, Xbee Wi-Fi S6B (stand-alone Wi-Fi module manufactured by Digi International) is selected. More details about the evaluation and the testing of this module is discussed in **SETCTOIN 2.5.3.**

2.5.3 Stand-alone Wi-Fi module

XBee Wi-Fi S6B Module is a stand-alone Wi-Fi module manufactured by Digi International Inc., which is used to transfer 10% of every second (first 100ms) to Wi-Fi device such as laptop, in a speed of 204.8 Kbit/s. The specification of XBee Wi-Fi S6B module is presented in **Table 2.11**.

Table 2.11: Specification of XBee Wi-Fi S6B module, revised from [16].

Features	Description
Serial Data Interface	UART[1] up to 1 Mbit/s, SPI[2] up to 6 Mbit/s
Frequency Band	ISM (Industrial Scientific Medical Band) 2.4GHz
Antenna Options	PCB (Embedded), external connector
Operating Temperature	-30 °C to +85°C
Dimension (LXW)	Through-Hole: 0.960 inch x 1.297 inch (2.438 cm x 3.294 cm)
Security	WPA-PSK[3], WPA2-PSK and WEP[4]
Channels	13 channels (wireless)
Standard	802.11 b/g/n
Supply Voltage	3.14~3.46 VDC
Transmit Current	up to 309 mA

Receive Current	100mA
Power-Down Current	<6µA ~25 °C
Transmit Power	up to +16 dBm
Receive Sensitivity	-93 to -71 dBm

Note1: Universal Asynchronous Receiver/Transmitter (UART).
Note2: Serial Peripheral Interface (SPI).
Note3: WPA-PSK and WPA2-PSK are IEEE 802.11i standard Pre-Shared Key security algorithm.
Note4: Wired Equivalent Privacy (WEP) is a security algorithm for IEEE 802.11 wireless networks.

As shown in **Table 2.11**, the maximal SPI speed to read data from external MCU through SPI interface is up to 6 Mbit/s. However, the SPI speed for stable continuous data transmitting can only reach up to 2Mbit/s in our test and it limited the wireless throughput to a lower value closed to 1Mbit/s. And the test bench is depicted in **Figure2.7** and its test results are presented in **Figure2.8**.

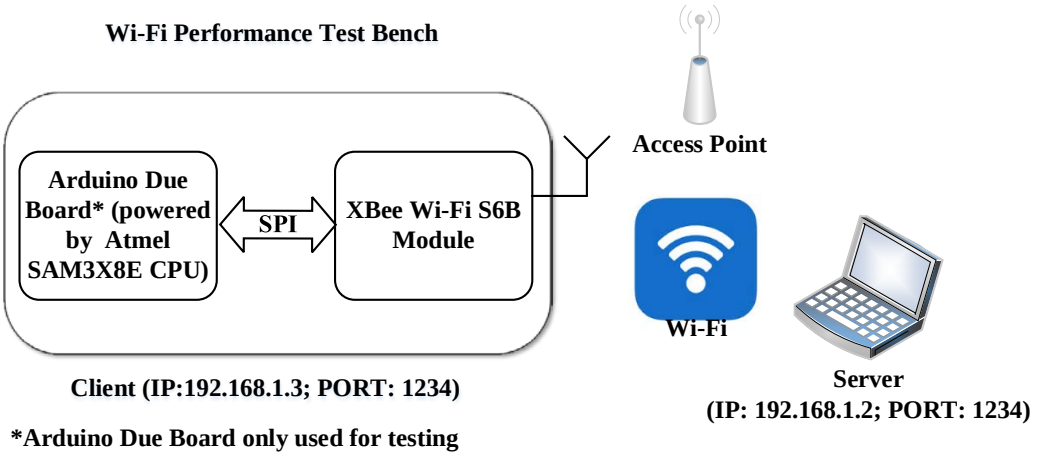

Figure2.7: Diagram of Wi-Fi performance test bench for XBee Wi-Fi S6B module. The laptop was assigned an IP (192.168.1.2) by Access Point (AP) and acted as a TCP/UDP server (with port 1234). Arduino Due (a 32-bit microcontroller board based on the Atmel SAM3X8E ARM Cortex-M3 MCU [27]) was connected to XBee Wi-Fi S6B module through Serial Peripheral Interface (SPI) bus. During testing, XBee was assigned an IP 192.168.1.3 by the same AP and acted as TCP/UDP client (with port 1234).

Wi-Fi performance testing follows the following procedures.

1) A digital data set was generated (ASCII codes from “A” to “Z” with the size of

1024 bytes) and buffered in the Random Access Memory (RAM) of Arduino Due.

2) Arduino Duo board wrote the data buffered in RAM to XBee Wi-Fi S6B module through SPI bus packet by packet (each packet contains 1024 bytes raw data) in the speed of 2Mbit/s.

3) Arduino Duo read “Receive Data Confirmation” packet from XBee Wi-Fi S6B through SPI interface at a speed of 3M bit/s, if set to Transmission Control Protocol (TCP) protocol. If the information inside of the packet indicated “successful”, then continue to implement from **STEP 2)** otherwise resend the same packet. This step can be ignored, if set to User Datagram Protocol (UDP) protocol.

5) A laptop (Thinkpad R61i with Windows 7 OS in our testing) ran throughput monitor software “Wireshark” and reported wireless throughput during the testing.

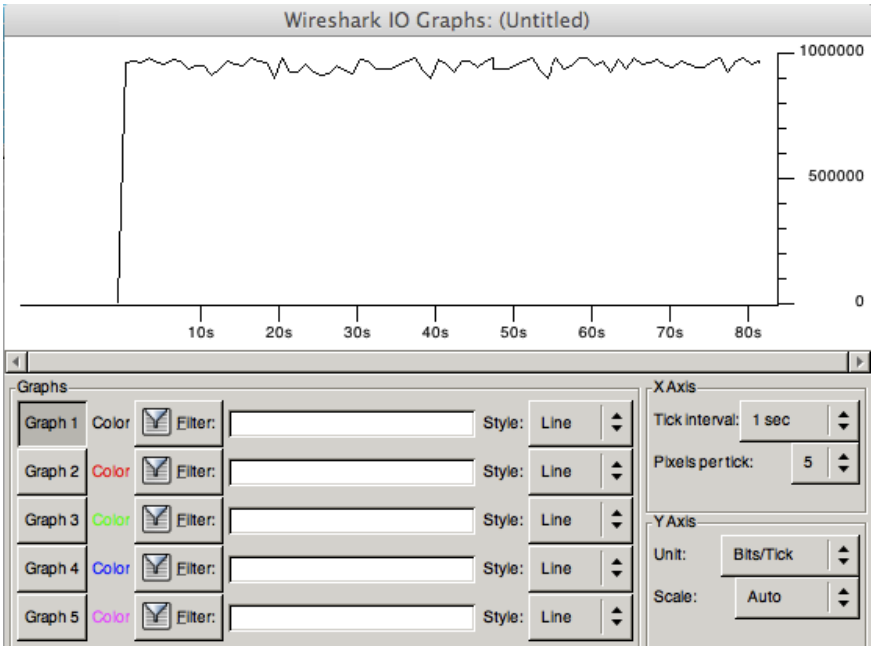

Figure2.8： Throughput test results plotted by Wireshark (throughput monitor software) shown that throughput of XBee S6B was around 1 Mb/s with the SPI (Serial Peripheral Interface). The unit of Y axis was set to “Bits/Tick” so that 1,000,000 in Y axis indicated a throughput up to 1Mbit/s.

2.6 Power Supply Unit

2.6.1 General

Power supply unit of the HD-sEMG RSWC consists of a high capacity rechargeable Li-ion battery and several low drop out regulators (LDOs), see **Figure2.9**, supplies power to all modules listed in **Table2.12.**

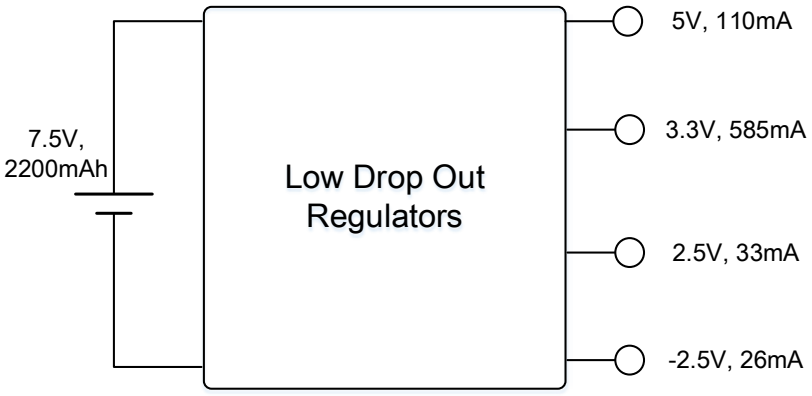

Figure2.9: Diagram of power supply unit and its output voltages. More details about these output voltages are presented in Table2.12

Table 2.12: Requirements of the power supply unit, in order to power all the modules of the HD-sEMG RSWC.

Item	Name	Descriptions
1	64-channel AFE (WEMG, LISiN)	+5V, I_{DD} < 100mA (typ. required up to 80mA); -2.5V, I_{DD} < 100mA (typ. required up to 26mA); +2.5V, I_{DD} < 100mA (typ. required up to 26mA); +3.3V, I_{DD} < 100mA (typ. required up to 26mA).
2	64-channel multiplexers (ADG726, Analog Devices)	+5V, I_{DD} < 60mA (typ. required up to 30mA)

3	ADC (LTC2368-16, 16bits resolution, Linear Technology)	V_{DD} =2.5V, I_{VDD} (max) = 6.3 mA; V_{REF} = 5V, I_{REF} (max)= 0.7 mA
4	MCU (STM32F407, ST Electronics)	V_{DD} = 3.3V, I_{VDD} (max) = 150mA.
5	SD card (16GB, class 10, SanDisk)	3.3V, up to 100mA for writing operation
6	XBee Wi-Fi S6B (iDigi International)	3.3V, up to 309 mA current in continuous transfer

2.6.2 Power Supply Unit Design

The high capacity rechargeable battery is a 7.5V, 2200mAh Li-ion battery (No.800052 Li-ion rechargeable 7.5V, 2200mAh, ENIX Energies) and its technical specification is presented in **Table 2.13**. The LDOs adopted by this power supply unit as well as batter are is presented in **Table 2.14**.

Table 2.13: Technical specification of the Li-ion rechargeable battery (No.800052) 7.5V, 2200mAh, ENIX Energies, revised from [27].

Electrical Details:	**UNIT**	**NOMINAL**	**MINIMUM**	**MAXIMAL**
Charge Current	A	1.0	0.1	2.0
Charge Voltage	V	8.4	8.3	8.5
Charging Temperature	ºC	+20	0	+45
End of charge detection: By timer[1]				
By low current	hours	3		
	mA	100		
Discharge Current[2]	A	0.4		3.0
Cut-off Voltage[3]	V	6.0	5.0	
Discharge Temperature[4]	ºC	+20	-20	+60
Storage:				
Temperature	ºC	+20	-20	+30
Duration	months			12
Store at 50% state of charge for optimum life. **Do NOT store in a discharged condition.**				
Mechanical Details:				
Length:	70.0 mm	Weight:	100 g	

Depth:	37.5 mm	Covering:	PVC Heat Shrink
Height:	19.0 mm	Labelling:	Standard
Leads:	120 mm UL1007	Connector:	None

Table 2.14: List of all components adopted by the power supply unit of the HD-sEMG RSWC.

Item	Name	Descriptions	Part Number
1	Battery	Li-ion rechargeable 7.5v 2200mAh, ENIX Energies	530-6331 (RS Components code)
2	LP38692MP-5.0	1A LDO regulator, Texas Instruments (fixed output at 5.0V)	LP38692MP-5.0
3	TPS73633	400mA Low-Dropout Regulator with Reverse Current Protection, Texas Instruments (fixed output at 3.3V)	TPS73633-DBV-5
4	TPS73625	400mA Low-Dropout Regulator with Reverse Current Protection, Texas Instruments (fixed output at 2.5V)	TPS73625-DBV-2.5
5	MAX889T	High-Frequency (2M Hz), Regulated, 200mA, Inverting Charge Pump, Maxim	MAX889TESA
6	TPS72325	200mA Negative Output Low-Dropout Linear Regulators, Texas Instruments (fixed output at -2.5V)	TPS72325-DBV-2.5
7	LTC6655-5	5V, 0.25ppm Noise, Low Drift Precision References	LTC6655BHMS8-5#PBF

As shown in **Table 2.14**, the 5V voltage for the 64-channel AFE and four chips of multiplexers are driven by LP38692MP-5.0 (5V 1A Low Dropout CMOS Linear Regulators, Texas Instrument [29]). LP38692MP-5.0 provide tight output tolerance (2.5% typical), extremely low dropout voltage (450mV@1A load current, V_{OUT}=5V), and excellent AC performance utilizing ultra low ceramic output capacitors.

The 5V voltage for ADC LTC2368-16 is driven by 5V reference LTC6655-5 [30]. The LTC6655-5 is a complete family of precision voltage references from Linear Technology, offering exceptional noise and drift performance. This low noise and drift is ideally suited for the high resolution measurements required by our application. Advanced curvature compensation allows this bandgap reference to achieve a drift of less than 2ppm/°C with a predictable temperature characteristic and an output voltage accurate to ±0.025%, reducing or eliminating the need for calibration.

The 2.5V voltage of the 64-channel AFE is driven by TPS73625, and the 3.3V voltage of the 64-channel AFE is driven by TPS73633. TPS73625 and TPS73633 are both in the TPS736xx family [31] (Texas Instruments). The TPS736xx family low-dropout (LDO) linear voltage regulators provides high reverse blockage (low reverse current) and ground pin current that is nearly constant over all values of output current. The TPS736xx uses an advanced BiCMOS process to yield high precision while delivering very low dropout voltages and low ground pin current. Current consumption, when not enabled, is under 1µA and ideal for portable applications. These devices are protected by thermal shutdown and foldback current limit.

The negative 2.5V for the 64-channel AFE is driven by MAX889 [32] and TPS72325 [33] together. The MAX889 (Maxim Integrated) inverting charge pump delivers a regulated negative output voltage at loads of up to 200mA. The device operates with inputs from 2.7V to 5.5V to produce an adjustable, regulated output from -2.5V to $-V_{IN}$. The MAX889 is available with an operating frequency of 2MHz (T version), 1MHz (S version), or 0.5MHz (R version). The higher switching frequency devices allow the use of smaller capacitors for space-limited applications. The lower frequency devices have lower quiescent current. The MAX889 also

features a 0.1μA logic-controlled shutdown mode and is available in an 8-pin SO packet. The output of MAX889 connected as the input of TPS72325. TPS72325 is a low drop out (LDO) negative voltage regulator offers an ideal combination of features to support low noise applications, from Texas Instruments. TPS72325 is stable with small, low-cost ceramic capacitors, and include enable (EN) and noise reduction (NR) functions. Thermal short-circuit and over-current protections are provided by internal detection and shutdown logic.

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3

System Prototyping and Performance Analysis

3.1 General

This section describes the design, assembling and testing of a prototype of HD-sEMG recording system with wireless communication (HD-sEMG RSWC). Components selected for our system are listed in **Table3.1** and a printed circuit board (PCB) is designed for the placement of those components (see SECTION3.2). After assembling, a HD-sEMG RSWC prototype is tested as described in SECTION3.4, calibrated and then used for acquisition and recording of sixty-four channel electric signals generated by muscles during voluntary contractions and detected by surface electrode arrays applied on the skin. All data acquired during the acquisition are recorded in a micro-SD memory card for off-line analysis, while a portion (10% of every second, first

100ms) of those data are transferred wirelessly to another Wi-Fi 802.11g device for online visualization. The main features of this prototype are:

- Multi-channel EMG detection with maximal 64 channel simultaneously.
- Battery-powered power supply system.
- End of the differential AFE [differential AFE has two ends, one positive end (+) and one inverse end (-)] output has a gain fixed at 96V/V. The gain of this AFE provides proper accuracy (1LSB with 0.76μV) to EMG signals and makes the system are not susceptible to saturation.
- Data Acquisition (DAQ) system samples sixty-four channel surface EMG with 2000 Sample Per Second (SPS) sampling rate and 16-bit resolution.
- On-board Data Recording System (DRS) to record data with SD memory card under FAT32 file system in a speed of 2048 Kbit/s.
- Wireless Communication System (WCS) transfers 0.1s of every second with a stand-alone Wi-Fi module with a speed of 102.4 Kbit/s using IEEE 802.11g.

3.2 System Prototyping

3.2.1 PCB Design of the Prototype

3.2.1.1 PCB Design Criteria

A PCB is a printed circuit board, also known as a printed wiring board [1]. It is used in electronics to build electronic devices. A PCB starts out as a thin, non-conducting sheet of material (e.g. glass fiber epoxy laminate material) and a thin layer of copper is chemically deposited on each side of this material. The connection diagram is "printing" onto the PCB for wiring required to connect the components. The "printing" is usually done by photographically transferring the image to the board. A PCB serves two purposes in the construction of an electronic device; it is a place to mount the components and it provides the means of electrical connection between the components.

Hardware components that are adopted in the design of HD-sEMG recording system with wireless communication (HD-sEMG RSWC) prototype are presented in **Table3.1**.

Table3.1: List of main components that are adopted by HD-sEMG RSWC prototype.

Module	Name	Descriptions
1	Micro-Control Unit (MCU)	STM32F407 (ARM-M4 core, 168MHz, LQFP100 14 x 14 mm^2 packet, from ST Electronics)
2	Analog Digital Convertor (ADC)	LTC2368-16 (16bits resolution, 5V reference voltage, 2.5V power supply, 1M SPS, from Linear Technology)
3	Multiplexer	ADG726 (16-channels, Analog Multiplexers, from Analog Devices)
4	Analog Front End (AFE)	64-channel WEMG AFE (64-channel single-end input; 64-channel differential output; 100 V/V voltage gain; Low pass filter with 3.5KHz [3dB cutoff]; High pass filter with 2Hz [3dB cutoff])
5	SD memory card	micro SD card (16GB, class 10, from SanDisk)
6	Wi-Fi module	XBee S6B Wi-Fi module
7	Power Supply Unit	TPS73633 (3.3V Low-Dropout Regulator from Texas Instruments) TPS73625 (2.5V Low-Dropout Regulator from Texas Instruments) MAX889TESA (200mA, Inverting Charge Pump, from MAXIM) LP38690-5 (5V Low-Dropout Regulator from Texas Instruments) TPS72325 (-2.5V Low-Dropout Regulator from Texas Instruments)

PCBs can be single sided (one copper layer), double sided (two copper layers) or multi-layer. Conductors on different layers are connected with plated-through holes called vias. Advanced PCBs may contain components - capacitors, resistors or active devices - embedded in the substrate as well. Since the sum of the main components is less than

fifty as presented in **Table3.2**, a double sided PCB (see **Figure3.1**) is sufficient to design the prototype of HD-sEMG Recording System with Wireless Communication.

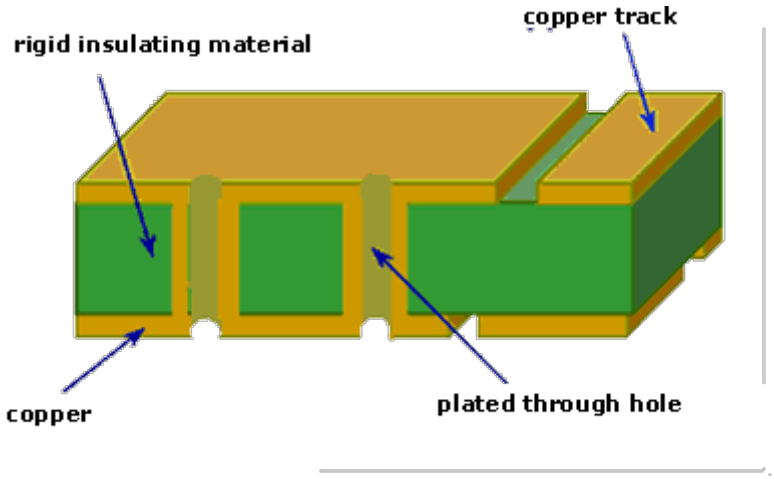


Figure3.1: Diagram of a double-sided printed circuit board (PCB) with copper for interconnection use. Plated through hole also called via, provides interconnection between top layer and bottom layer of this double-sided PCB.

The components listed in **Table 3.1** are placed on a two-layer PCB and follow the criteria of PCB arrangement as following:

1) The regulators of the power supply unit are sources of noise so that the arrangement of those regulators must be separately from other components. These regulator must be apart from each other at least 5mm and be placed together closed to input of analog front end. The back of these regulators must be kept blank as well.
2) Wi-Fi module is a source of high frequency noise and the arrangement of it must be separately from other components. The PCB has two layers with one layer assembled with Wi-Fi module, the area of another layer under the Wi-Fi module must be left blank.
3) Four chips of multiplexers must be apart from each other as far as possible to avoid cross talk.
4) In order to reduce the influence of noise, we adopt large area for grounding of components on board and star-connection ground between AFE board and our PCB.

Details about the two-layer PCB are presented in **Table3.3**.

Table3.3: Technical Information of the PCB manufacturing for the HD-sEMG RSWC.

PCB-layer	Parameter Description	Value
Top layer	Copper thickness	1.4mil
Bottom layer	Copper thickness	1.4mil
Dielectric layer	Material	FR-4
	Thickness	12.6mil
	Dielectric constant	4.8
Machanical 1	Dimension	138.9 x 127.0 mm^2 (LxW)

3.2.1.2 Assembling

There are mainly two kinds of assembling methods adopted by industry: Through-Hole technique (THT) and Surface Mount technology (SMT). The difference between THT and SMT is depicted in **Figure3.2**. All components that were using THT are presented in **Table3.5** and the layouts of the bottom PCB layer to assemble them are depicted in **Figure3.4**.

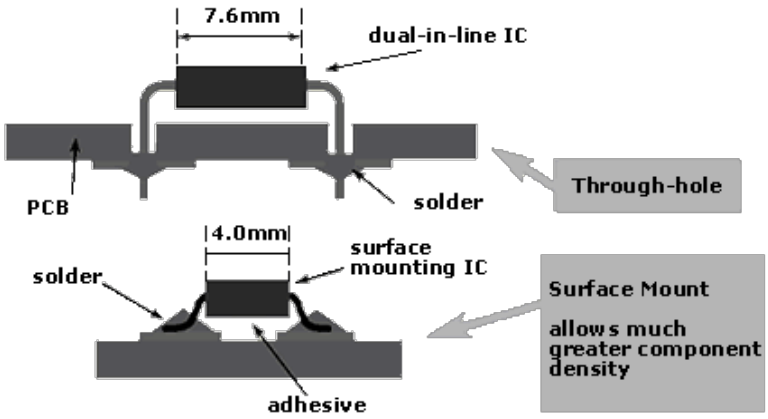


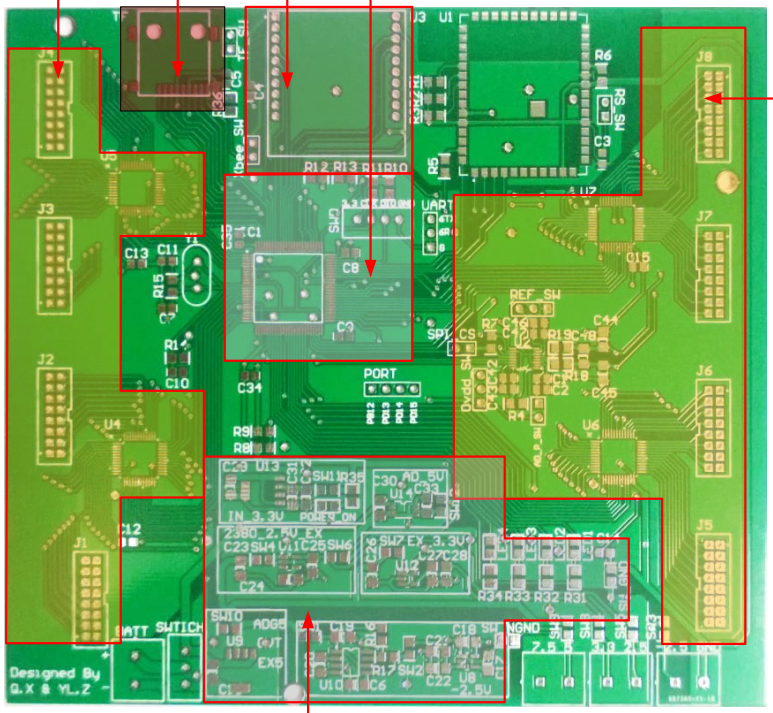
Figure3.2: Diagram that shows the difference of through-hole technique (THT) and surface mount technology (SMT).

b) Data Acquisition System

c) Data Recording System

d) Wireless Communication System

e) Micro-Control Unit



1cm

1cm

f) Battery-powered Power Supply Unit

Figure3.3: PCB (top side) of HD-sEMG RSWC prototype. All pads for Surface Mounted Devices (SMDs) with surface mount technology are designed in this side. The outline dimensions of the smallest two-terminal components (resistors or capacitors) are 0.3 mm x 0.6 mm. Fine pitch multi-terminal components (ICs) have a pitch down to 0.3 mm.

Table3.4: List of components that were assembled on the top side of printed circuit board of HD-sEMG RSWC prototype (see Figure3.3) with surface mount technology.

Comment	Description	Designator	Footprint	Quantity
Cap	Capacitor	C1, C2, C3, C4, C5, C6, C7, C8, C9, C10, C11,C12, C13, C14, C15, C16, C17, C18, C19, C20, C21, C22, C23, C24, C25, C26, C27, C28	0805[1]	28
STM32F40x-VG	Micro-Control Unit (MCU)	IC1	LQFP100[2]	1
SD_Card	SD memory card slot	P7		1
Res	Resistor	R1, R2, R3, R4, R5, R6, R7, R8, R9, R10, R11, R12, R13, R14, R15, R16, R17, R18, R19, R20, R21	0805[1]	21
RS9110-N-11-22	Wi-Fi module (option)	U1		1
LTC2368-16	ADC	U2	MSOP-16	1
Xbee-S6B	Wi-Fi module	U3		1
ADG726BSUZ	Multiplexer	U4, U5, U6, U7	SU_48	4
LTC6655-8	5V reference	U8	MSOP-8	1
TPS72325_DBV_5	2.5V LDO	U9, U12	DBV5	2
LP38692_NDC_5	5V LDO	U10	MP05A	1
MAX889S	Negative charge pump	U11	SO-G8	1
TPS73633_DBV_5	3.3V LDO	U13	DBV5	1

Note1: The dimension of footprint "0805" is 2.0 mm × 1.3 mm (0.08 inch x 0.05 inch).

Note2: The dimension of footprint "LQFP100" is 14mm × 14mm.

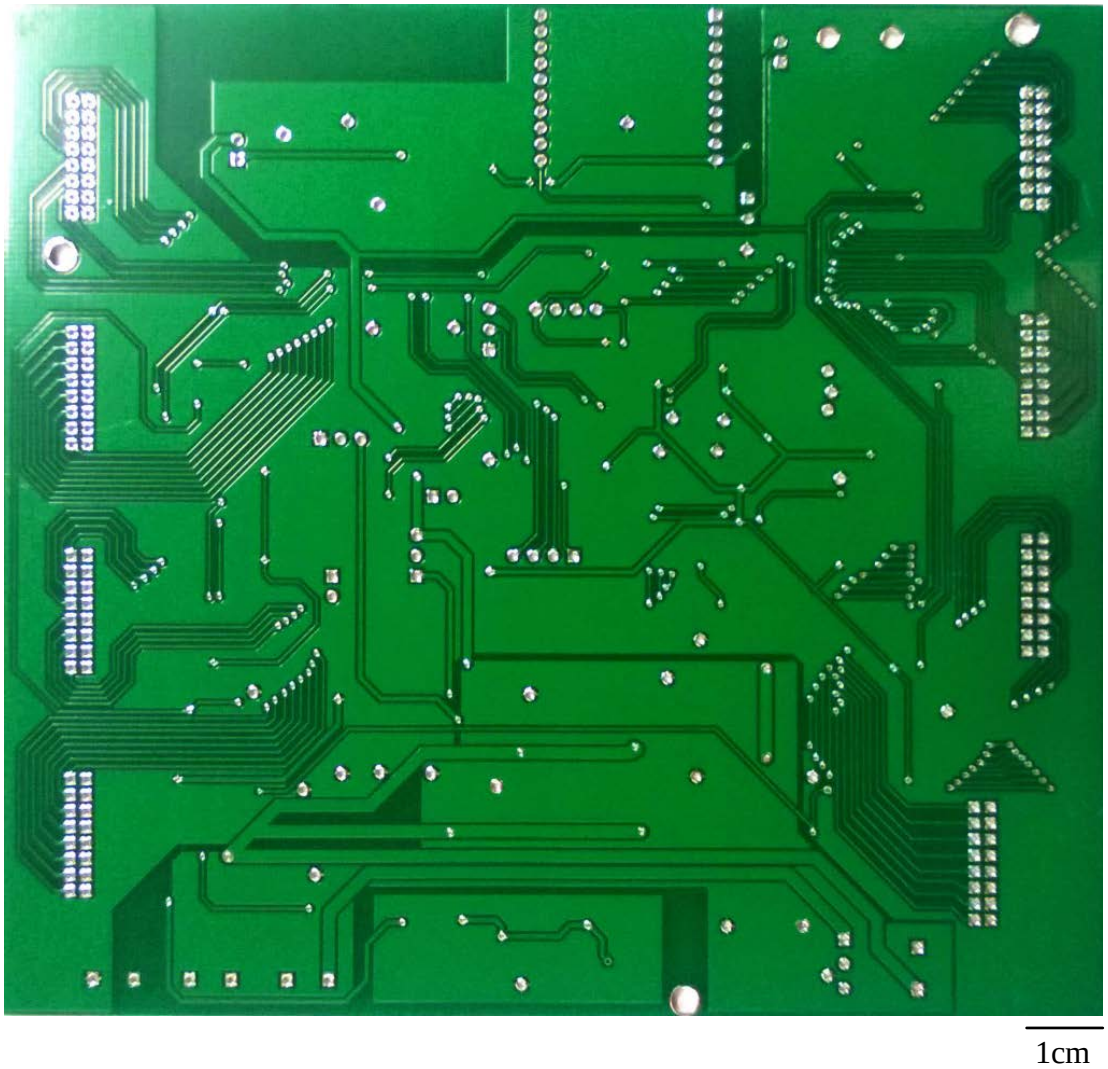


Figure3.4: PCB (bottom side) of HD-sEMG RSWC prototype. All pads for through-hole mount components are indicated in this side.

Table3.5: A list of components mounted on the bottom side of printed circuit board of HD-sEMG RSWC prototype (see Figure3.4) with through-hole mount technology. However, the indicators (see Figure3.3) are printed only in top side of the PCB.

Comment	Description	Indicators	Footprint	Quantity
Header 8x2	Header, 8-Pin, Dual row	J1, J2, J3, J4, J5, J6, J7, J8	Male-16	8
Header 2	Header, 2-Pin	P1 (TF_SW), P4 (Xbee_SW), P6(SPI_CS), P8 (AD_SW), P9 (RS_SW)	HDR1X2	5
Header 3	Header, 3-Pin	P2 (REF_SW), P3 (0vdd)	HDR1X3	2
JTAG	Joint Test Action Group debugger	P5 (SWD)		1
Xbee-S6B	Wi-Fi module	U3		1
8M	Crystal Oscillator	Y1	XTAL	1

Top side of the assembled PCB board is presented in **Figure3.5**.

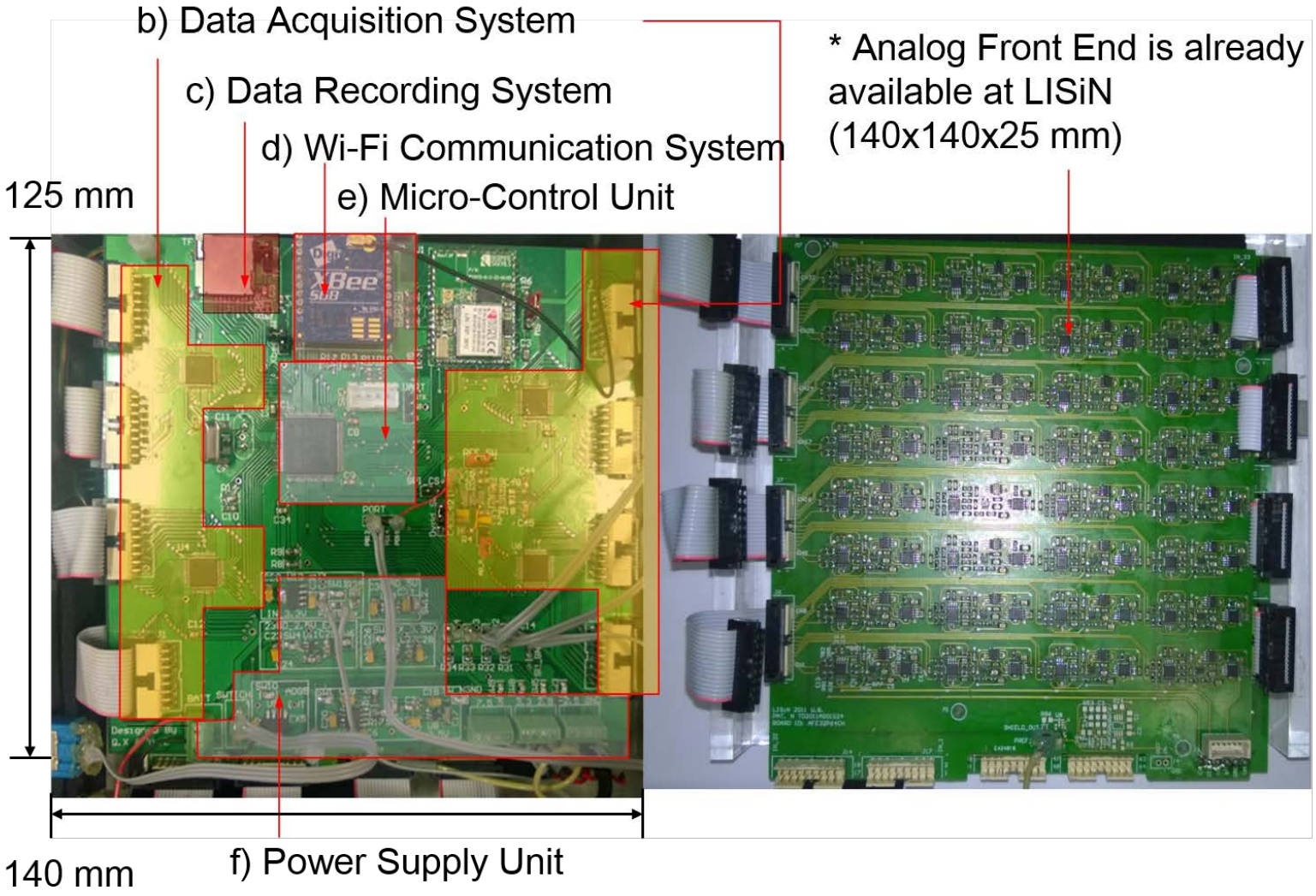

b) Data Acquisition System
c) Data Recording System
d) Wi-Fi Communication System
e) Micro-Control Unit
* Analog Front End is already available at LISiN (140x140x25 mm)
125 mm
140 mm
f) Power Supply Unit

Figure3.5: PCB (top side) of HD-sEMG RSWC prototype with all components mounted. Four connectors on the left side and four connectors on the right side are connected to the output of analog front end (AFE).

3.2.2 EMC and Safety

In order to enhance EMC (Electromagnetic Compatibility) as well as safety of the HD-sEMG recording system with wireless communication (HD-sEMG RSWC) prototype, more components (including aluminum enclosure, power socket bulkhead and power plug) are required.

EMC specification define the maximal emissions allowed from a system and the maximal interference the system must withstand while still functioning properly. Shielding is one of many ways can control a system's emissions and minimize immunity issues. The amount of reduction of the radio waves passing through the surface is generally referred to as enclosure's shielding effectiveness (SE). An existing EMC compatible aluminum enclosure (see **Figure3.6**) is adopted to reduce both the emissions leaving the product and the interference trying to enter the product.

HD-sEMG RSWC prototype is powered by a rechargeable battery and must not turn on during recharge. Furthermore, a power socket bulkhead (lumberg 1614 15) [2] and a power plug (lumberg XNES/J 250) [3] are adopted to disconnect one end (ground) of the prototype board from battery (-) during charging for safety. HD-sEMG RSWC prototype must not be connected to patient during recharge for safety.

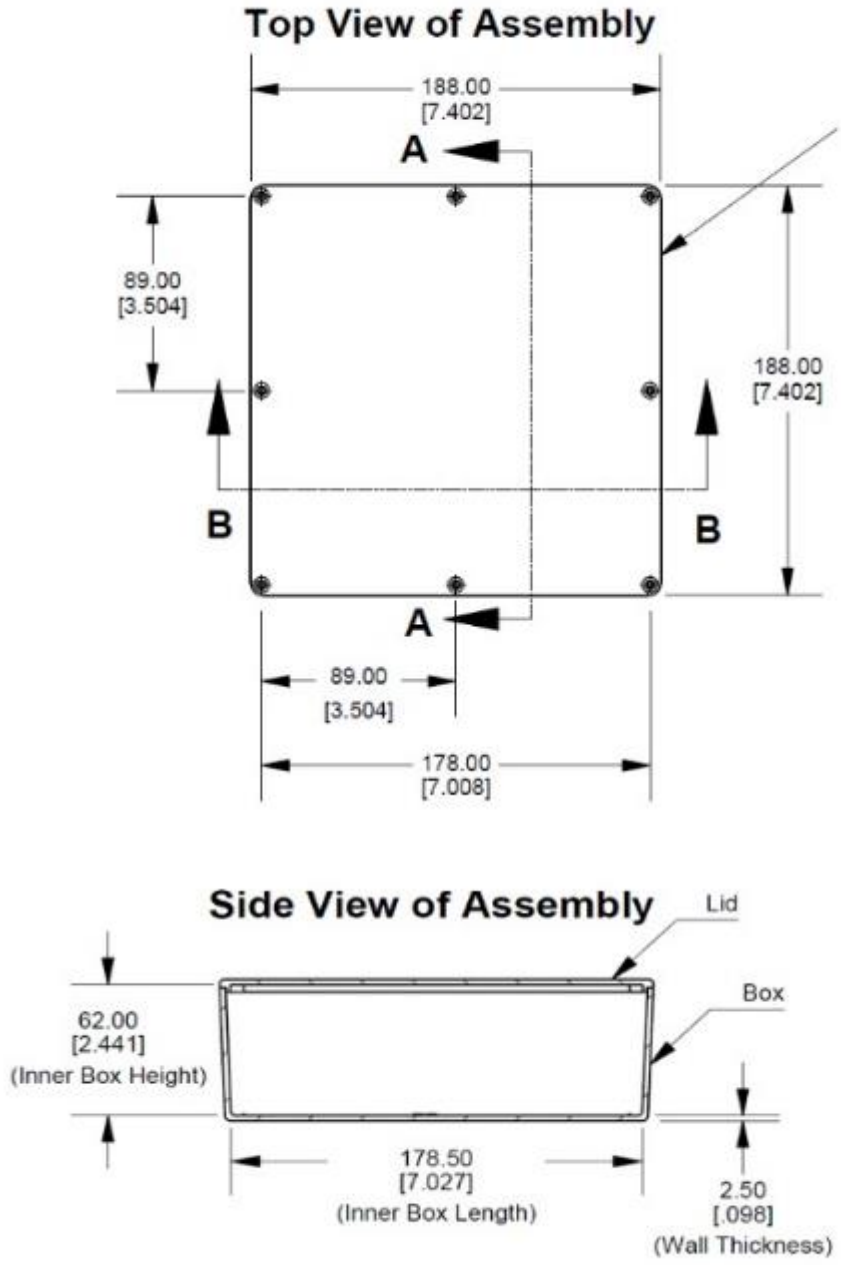


Figure3.6: Top view (upper) and side view (lower) of the aluminum enclosure (1590F, manufactured by HAMMOND MANUFACTURING) adopted for the HD-sEMG recording system with wireless communication (HD-sEMG RSWC) prototype. The dimension is presented as well, take 188.00 [7.402] for example, which indicates 188.00mm [7.402 inch] in length.

3.2.3 User Panel Design

User panels are where the external connectors, power switch, LEDs as well as instructions etc. are placed. Panels help user to follow the correct connection of the external connectors (charger, reference and so on) and check the work state of the HD-sEMG recording system with wireless communication (HD-sEMG RSWC) prototype as well. The schematic of the designed panels is depicted in **Figure3.7**.

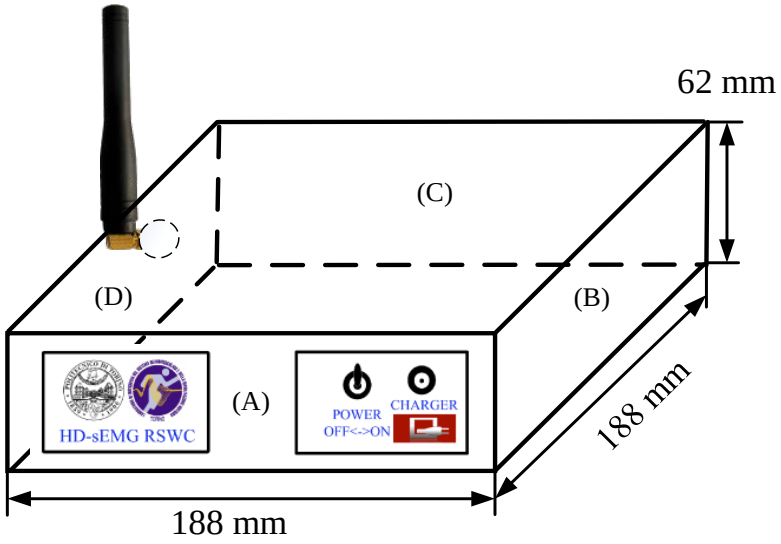


Figure3.7: Schematic of the HD-sEMG recording system with wireless communication (HD-sEMG RSWC) prototype panels. Totally four panels are designed, include: Panel A (front panel, see Figure3.8), Panel B (right panel, see Figure3.9), Panel C (rear panel, see Figure3.10) and Panel D (left panel, see Figure3.11).

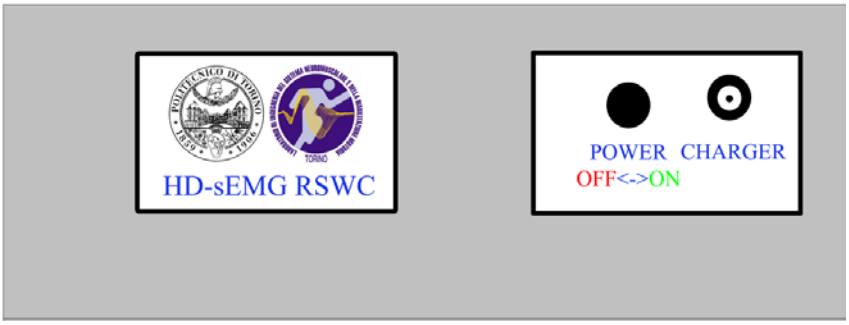


Figure3.8: Front panel (Panel A) of the HD-sEMG recording system with wireless communication (HD-sEMG RSWC) prototype. This panel includes the logo of HD-sEMG RSWC unit, power on/off switch and charger connector.

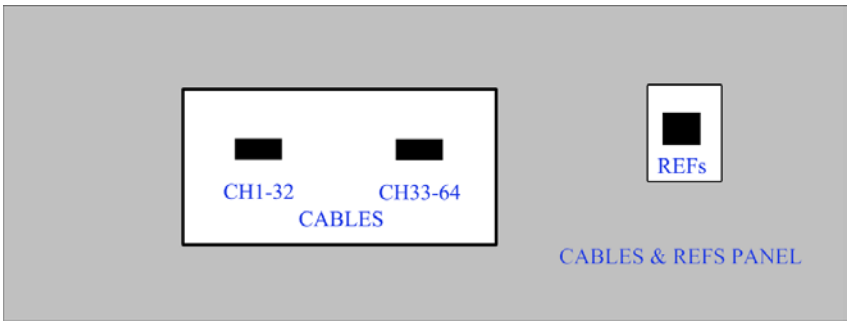


Figure3.9: Cables and refs connectors panel (Panel B) of the HD-sEMG recording system with wireless communication (HD-sEMG RSWC) prototype. This panel includes two thirty-two connector (CH1-32 for channel 1 to 32, CH33-64 for channel 33 to 64) for collecting EMG signals from sixty-four electrodes and connector (REFs) for patient reference.

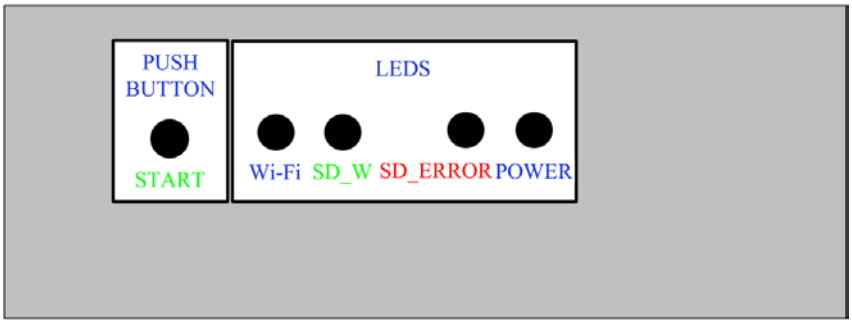


Figure3.10: Rear panel (Panel C) of HD-sEMG RSWC unit. This panel includes a push button and four LEDs. The push button starts an acquisition. The LED labeled with "Wi-Fi" indicates the state of Wi-Fi module: it blinks at the beginning when searching for access point and becomes off if ready for wireless communication. The LED labeled with "SD_W" indicates the state of SD card writing operation: this LED is on during SD card writing operation. The LED labeled with "SD_ERROR" indicate the state of a SD writing operation: if it is on after a SD writing operation, indicates error happened during this operation and a new acquisition is need. The LED labeled with "Power" indicates the state of power: LED on (power on) and LED off (power off).

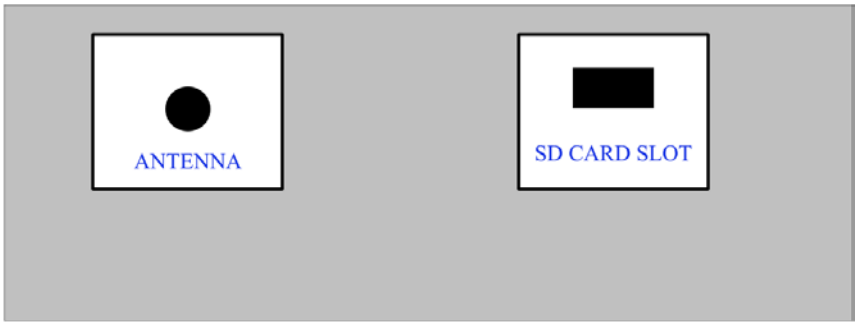


Figure3.11: Left side panel (Panel D) of HD-sEMG RSWC unit. This panel includes an external antenna connector and a SD card slot.

3.3 Real-Time Firmware Design

Firmware is software program that is etched into a hardware device. Firmware was originally designed for high level software and could be changed without having to exchange the hardware for a newer device [4]. Firmware also retains the basic instructions for hardware devices that make them operative. Without firmware, a hardware device would be non-functional. Firmware is typically stored in the flash ROM (read only memory) of a hardware device. It can be erased and rewritten.

According to the requirement of the multi-channel HD-sEMG Recording System with Wireless Communication (HD-sEMG-RSWC) discussed in **SETCTION 3.1**, a real-time firmware is adopted. Furthermore, there are mainly two types of real-time firmware: hard real time firmware and soft real-time firmware. Hard real time firmware is firmware program that cannot tolerate any delay or if delay happens the whole system will be worthless. Conversely, a real-time firmware that can usually or generally meet a deadline is a soft real-time firmware.

Our firmware is designed as a soft real-time firmware. It has not strict time requirement on each small operation (e.g. an operation that writes 512 bytes block inside a SD memory card) but a cluster of small operations must meet a deadline. For instance, a buffer must be empty for reuse after 100ms so that data recording system must write all 25600 bytes [calculated by 16-bit, 64-channel and 200 samples (100ms with 2000 sample per second)] to a SD memory card inside 100ms.

The following instruction are to optimize the code to design our soft real-time firmware:
1) All the codes (include the drivers and libraries) were written in C program language or Assemble language. The information of the compilers used is presented in **Table3.6**.
2) Internal (inside the drivers) delay functions such as “void ASM_delay_10ns(void)”,

“void ASM_delay_50ns(void)”, “void ASM_Delay_1us(void)” and so on are only written in Assemble Language.

3.3.1 Integrated Development Environment

Integrated development environment (IDE) is a set of programming tools for writing applications (source code editor, compiler, debugger, etc.), all activated from a common user interface and menus. IDEs are necessary standard procedure for program development. The IDE adopted for our application is µVersion 4.7. The µVision IDE from Keil combines project management, make facilities, source code editing, program debugging, and complete simulation in one powerful environment [7]. The µVision development platform is easy-to-use and helping you to quickly create embedded programs that work. The µVision editor and debugger are integrated in a single application that provides a seamless embedded project development environment. More details are presented in **Table3.6**.

Table3.6: Main tools (software) adopted by the Integrated Development Environment (IDE) µVision (V4.72.10.0) for the development of the firmware for the HD-sEMG RSWC. All these tools and software are provided together with the µVision IDE itself under Windows operation system.

Item	Description	Version
Toolchain	MDK-ARM Standard	V4.72.1.0
C Compiler	Armcc.Exe	V5.03.0.76
Assembler	Armasm.Exe	V5.03.0.76
Linker/Locator	ArmLink.Exe	V5.03.0.76
Librarian	ArmAr.Exe	V5.03.0.76
Hex Converter	FromElf.Exe	V5.03.0.76
CPU DLL	SARMCM3.DLL	V4.72.1.0
Dialog DLL	DCM.DLL	V1.10.0.0
Target DLL	Segger\JL2CM3.dll	
Dialog DLL	TCM.DLL	V1.14.1.0

3.3.2 Software Structure Diagram

Structure of the design of soft real-time firmware is depicted in **Figure3.12**.

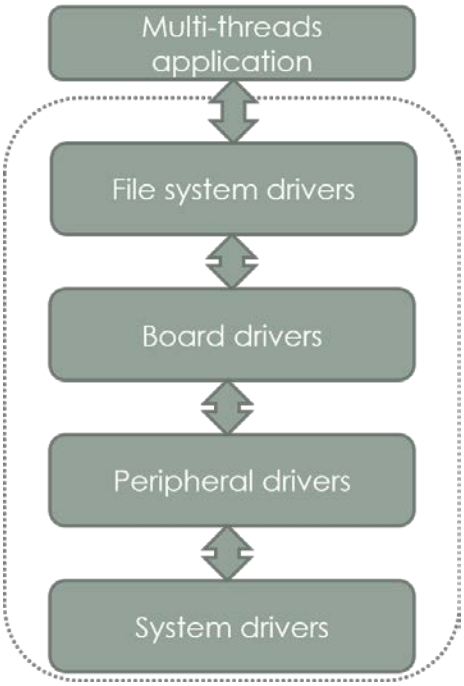


Figure3.12: software structure diagram of the firmware developed for the HD-sEMG RSWC. Multi-thread application runs on the top above a four-level drivers (see Table3.7), which including system driver (at the bottom-1st level), peripheral drivers (2nd level), board drivers (3rd level for user defined device) and file system driver (4th level for file system).

As shown in **Figure3.12**, multi-thread application runs on the top above a four-level drivers (see **Table3.7**). This four-level driver structure separates system functions and user-defined functions with different level to make source code of the firmware easier for maintain and modification.

- 1st level system drivers, are drivers that deal with system management. E.g. “startup_stm32f4xx.s” in assembly language (manager system clock) and “stm32f4xx_it .c” (manage interrupt).
- 2nd level peripheral drivers, are drivers that deal with communication between system and peripheral [e.g. SPI (Serial Peripheral Interface), SDIO (Secure Digital Input/Output) and so on]. E.g. “stm32f4xx_spi.c” (manage the

communication of SPI peripheral) and “stm32f4xx_sdio.c” (manage the communication of SDIO peripheral). All second level drivers are organized in folder “stm32f4xx_peripheral driver”.

- 3rd level board drivers, are drivers that deal with the communication between all user-defined on-board components and MCU. E.g. “led.c” (manage the LEDs), “usart.c” (manage the Universal Asynchronous Receiver/Transmitter interface), “MUX.c” (manage the ADC).
- 4th level file system driver are the driver manage the file system for SD memory card. The file system adopted for our application is FAT32 (File Allocation Table 32) file system.

These four-level drivers together with the multi-thread application (described in SECTION3.3.3) is compiled with the IDE (described in **SECTION3.3.1**) to generate the firmware. The compiled firmware will be written to the prototype of HD-sEMG recording system with wireless communication (HD-sEMG RSWC) through a JTAG debugger.

Table3.7: Information about the four-level drivers and multi-thread application for the firmware developed for the HD-sEMG RSWC. This multi-thread application runs on the top above the four-level drivers.

Level	Name	Description
1st level system drivers	system_stm32f4xx.c	This file contains the system clock configuration for STM32F4xx devices, and is generated by the clock configuration tool stm32f4xx_Clock_Configuration_V1.0.1.xls
	startup_stm32f4xx.s	This file provides STM32F4xx devices vector table for MDK-ARM toolchain.
	stm32f4xx_it.c	This file manages the interrupts.
2nd level peripheral drivers	stm32f4xx peripheral driver	Those files (total thirty-one files) manage external timer, communication with peripheral (through standard peripheral protocol such as SPI, SPIO, CAN, ADC and so on), watch dog and so on.
3rd level board drivers	led.c	This file provides driver for LEDs.
	delay.c	This file contains internal delay function, which are mainly written in Assemble Language. E.g. "void ASM_delay_10ns (void)" function, provide a 10 nano-second delay.
	sdio_sd.c	This file implements a high level communication layer for read and write from/to a SD memory card through SDIO interface.
	usart.c	This file contains function to print debug information with USART interface.
	mux.c	This file provides driver for multiplexers.
	button.c	This file provides driver for push button.
	adc.c	This file provides driver for analog digital convertor.
	xbeewifi.c	This file provides driver for Xbee Wi-Fi module
4th level file system driver	fat	Those two files (ff.c and diskio.c) provide driver for managing the file system (FAT32) write to/from a SD memory card.
multi-thread application	main.c	This file implements mainly three threads simultaneously in order to acquire, record 64-channel HD-sEMG and transfer 1/10th of every second wirelessly.

3.3.3 Multi-Thread Application

As shown in **Table3.7**, multi-thread application runs above the four-level drivers and manages three main threads simultaneously.

- Thread one: MUX – ADC – SPI1. This thread acquires 64-channel HD-sEMG signals and make analog digital conversion. Four chips of 16-channel multiplexers (MUX) requires twenty-eight control signals and address signals [each multiplexer requires three control signals (chip select, enable, write address) and four address signals (A_0, A_1, A_2 and A_3)]. One ADC requires one control signal (CNV, Convert Input. A rising edge on this input powers up the part and initiates a new conversion) and requires one SPI (SPI1, Serial Peripheral Interface 1) port. One SPI port requires two data signals [MOSI (Master Output Slave Input) and MISO (Master Input Slave Output)] and two control signals [CS (Chip Select) and CLK (clock)].
- Thread two: SDIO – SD memory card. This thread records all the data from thread one with a SD memory card. With 4-bit SDIO (Secure Digital Input/Output) model, four digital pins (DAT0, DAT1, DAT2 and DAT3) as well as three control pins [CMD (command), CLK (clock) and SD_DET (SD Detection)] are required by this thread.
- Thread three: SPI3 – XBee Wi-Fi. This thread transfers $1/10^{th}$ of every second wirelessly. XBee Wi-Fi module requires three control signals [DOUT (Digital Out, output), RESET, SPI_ATTN (SPI_ Attention)] as well as one standard SPI port. One SPI port requires two data signals [MOSI (Master Output Slave Input) and MISO (Master Input Slave Output)] and two control signals [CS (Chip Select) and CLK (clock)].

3.3.4 Data Flow

Data acquired by ADC in thread 1 needs to be buffered first for other operation done by thread 2 and thread 3 as well. The data flow among those three threads are depicted in **Figure3.13**.

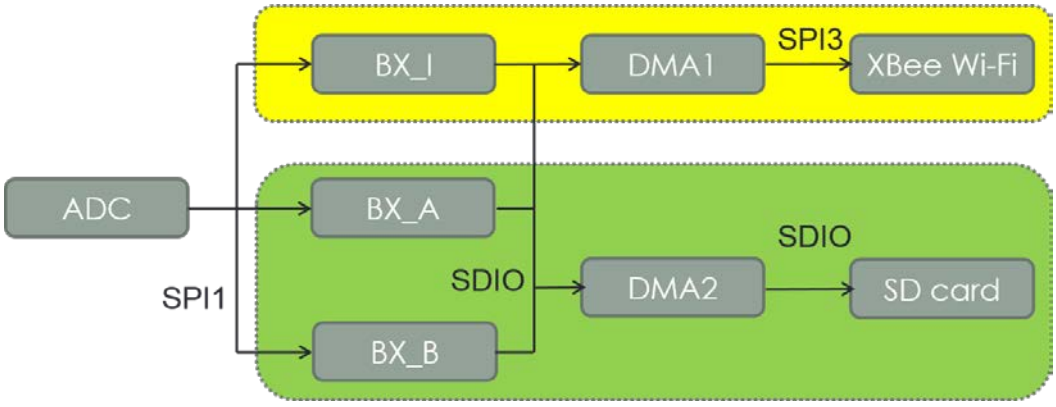


Figure3.13: Data flow diagram of the firmware developed for the HD-sEMG RSWC. Data read from ADC (Analog Digital Converter) through SPI1 (Serial Peripheral Interface 1) buffered in three different internal buffers (BX_I, BX_A and BX_B). The size of those three buffers are the same and can manage a portion of sampled data [25600 bytes, calculated by 16-bit, 64-channel and 200 samples (100ms with 2000 sample per second)]. In every second, data acquired in [0, 100ms) are buffered in BX_I; data acquired in [100ms, 200ms), [300ms, 400ms), [500ms, 600ms), [700ms, 800ms), [900ms, 1000ms) are buffered in BX_A; data acquired in [200ms, 300ms), [400ms, 500ms), [600ms, 700ms), [800ms, 900ms) are buffered in BX_B. The data buffered in BX_I are read twice: first time through SPI3 (Serial Peripheral Interface 3) bus to XBee Wi-Fi module with DMA1 (Direct Memory Access1) and second time through SDIO (Secure Digital Input/Output) bus to SD memory card with DMA2 (Direct Memory Access2).

As shown in **Figure3.13**, direct memory access (DMA) is an unit inside MCU that allows certain hardware subsystems within the computer to access system memory independently of the central processing unit (CPU).

3.3.5 File System and Specific Format

3.3.5.1 File System

In computing, a file system is used to control how data is stored and retrieved [5]. Without a file system, information placed in a storage area would be one large body of data with no way to tell where one piece of information stops and the next begins. By separating the data into individual pieces, and giving each piece a name, the information is easily separated and identified. Taking its name from the way paper based information systems are named, each piece of data is called a "file". The structure and logic rules used to manage the groups of information and their names is called a "file system". FAT32 (File Allocation Table 32), is an improvement to the original FAT (File Allocation Table) system, that was introduced by Microsoft in 1996 with its Windows 95 OEM Service Releases 2 (OSR2) operating system [6]. Since it uses more bits to identify each cluster on the disk, this helps the computer locate files easier and allows for smaller clusters, which improves the efficiency of your hard disk. Cluster values are represented by 32-bit numbers, of which 28 bits are used to hold the cluster number. The boot sector uses a 32-bit field for the sector count, limiting the FAT32 volume size to 2 TiB for a sector size of 512 bytes. The maximal possible size for a file on a FAT32 volume is 4 GiB minus 1 byte or 4,294,967,295 ($2^{32}-1$) bytes.

3.3.5.2 Specific Format

Each byte of data in SD memory has its own address and big-endian ordering systems store the most significant byte of a word in the smallest address and the least significant byte is stored in the largest address (Most Significant Bit) [8]. **Figure3.14** describes the difference between big-endian ordering and little-endian ordering when storing same data “0A0B0C0D” from register.

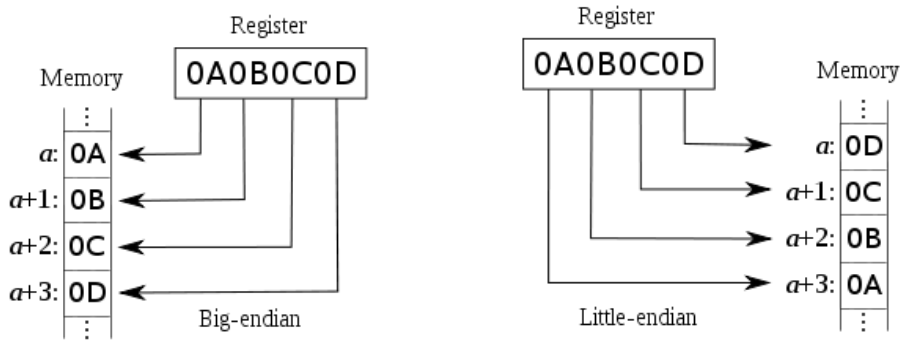


Figure3.14: Diagram shows the difference between big-endian ordering and little-endian ordering when storing same data "0A0B0C0D" from register. Big-endian systems store the most significant byte of a word in the smallest address and the least significant byte is stored in the largest address (Most Significant Bit). Little-endian systems, in contrast, store the least significant byte in the smallest address. Furthermore, the "a" points to the address of data stored in memory.

The orders of bytes are following big-endian ordering while the orders of the samples acquired from sixty-four channel are specified in **Figure3.15**.

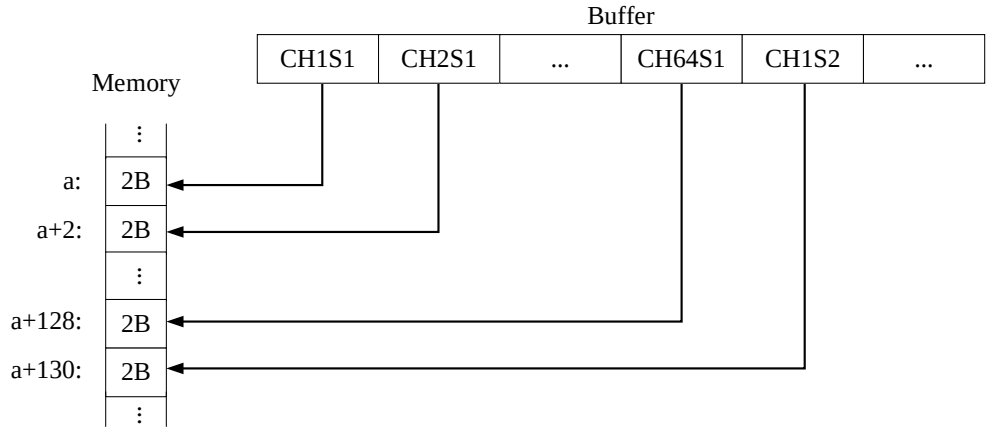


Figure3.15: Ordering of samples that are recorded in the HD-sEMG RSWC. Samples firstly are buffered by internal buffer of micro-control unit and written to the memory of SD card in big-endian ordering. Each sample occupies two bytes (2B) in memory while "a, a+2, …, a+130" (left side) point to the address of memory. CH1S1 indicates the first sample of channel one, CH2S1 indicates the first sample of channel two, CH64S1 indicates the first sample of channel sixty-four and CH1S2 indicates the second sample of channel one.

3.4 Performance Analysis

3.4.1 AFE Gain Measurements

The 64-channel WEMG Analog Front End (AFE) [9], designed at LISiN, is used to amplify 64-channel single-end analog inputs from electrodes with 96V/V single end voltage gain and provide 64-channel analog outputs after filtering. The bandwidth of 64-channel WEMG AFE is set to [3Hz, 3500Hz], and make the variation of the gains at different frequency inside the bandwidth [10Hz, 500Hz] as little as possible.

3.4.1.1 Objective

The objective of this evaluation is to investigate the mismatch of voltage gain among sixty-four AFE channels and its influence on accuracy of Data Acquisition System (DAQ).

3.4.1.2 Method

To perform this evaluation, sinusoid waves (with various frequencies in the range of sEMG bandwidth [10Hz, 500Hz]) by signal generator (Agilent 33210A) were taken as the input to 64-channel WEMG AFE through a 1-to-64 connector. A digital multimeter (Agilent Multimeter 34410A) measured the root mean square (RMS) of the output voltages of AFE one channel by one channel (see **Figure3.16**).

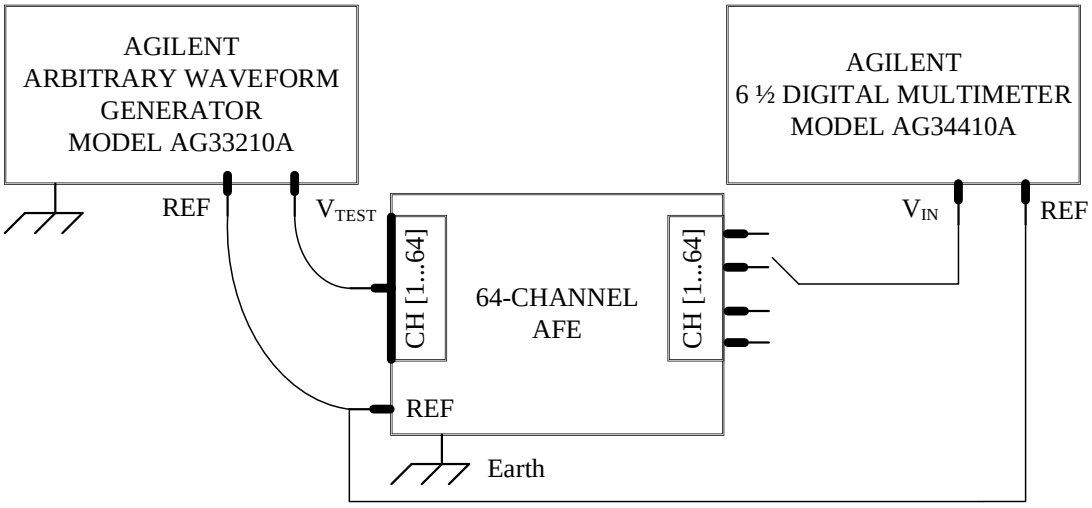


Figure3.16: Test bench block diagram for Analog Front End (AFE) gain measurements. The input of AFE was sinusoid wave (with various frequencies inside EMG bandwidth [10Hz, 500Hz]) produced by signal generator. During measurements, two references [PREF (Person Reference) and GND (Ground)] of AFE were connected to REFs (references) of AG33210A and AG34410A as well. The root mean square (RMS) of output voltages of AFE (one channel by one channel) responded to different frequency of input sinusoid wave were measured by multimeter AG34410A. The bandwidth of digital multimeter (AG34410A) is [10 Hz, 20 kHz].

Mismatching of the Analog Front End (AFE) is calculated by the following equation:

$$\text{Mismatching} = \frac{(\text{Gain}_{MAX} - Gain_{MIN})}{Gain_{MIN}} \times 100\% \qquad (3\text{-}2)$$

Where: Gain_{MAX} is the maximal measured gain of 64-channel AFE and Gain_{MIN} is the measured minimal gain of 64-channel AFE.

3.4.1.3 Results

Due to the tolerance of components [e.g. resistors (±1%), capacity (±10%) and so on], the gain [calculated by equation (3-2)] of 64-channel WEMG AFE shows mismatching of monopolar gain among sixty-four channels. **Table3.8** presents the statistic of Analog Front End gain mismatching, while V_1 in equation (3-2) is 7.07 mV_{RMS}.

Table3.8: Results of Analog Front End gain (single end) mismatching test. Due to the tolerance of component [e.g. resistors (±1%), capacity (±10%)], the gain [calculated by equation (3-2)] of 64-channel WEMG AFE shows mismatching among sixty-four channels. This mismatching also influenced by the frequency of input signals according to the testing results. The left side of the table indicates some frequencies tested inside sEMG bandwidth [10, 500] Hz.

Frequency (Hz)	Minimal Monopolar Gain of the 64 Channel (V/V)	Maximal Monopolar Gain of the 64 Channel (V/V)	Mismatch* between Monopolar Gain of the 64 channel (%)
10	77.5	78.2	0.9
15	86.4	87.1	0.8
20	90.7	90.9	0.3
25	92.4	92.9	0.6
30	93.5	94.1	0.6
40	94.8	95.3	0.6
50	95.0	95.8	0.7
60	95.3	96.2	0.9
70	95.8	96.3	0.6
80	96.0	96.5	0.4
90	96.0	96.5	0.4
100	96.2	96.5	0.3
200	95.6	96.6	1.0
300	95.3	96.6	1.3
400	95.3	96.5	1.2
450	95.0	96.2	1.2
500	94.8	96.0	1.3

Note*：The accuracy of signal generator (AG33210A) is ±2% of reading. The accuracy of digital multimeter (AG34410A) is ±0.04% [true RMS AC voltage (10 Hz, 20 kHz)].

As shown in **Table3.8**, the plot shown that the gain of the 64-channel AFE raise fast at [10, 60] Hz, become stable at [60, 400] Hz, then reduce at [400, 500] Hz. Considering the accuracy of signal generator (AG33210A) is ±2% of reading and the accuracy of digital multimeter (AG34410A) is ±0.04% [true RMS AC voltage (10 Hz, 20 kHz)], the maximal measured mismatching is only 1.3%, less than 2% (accuracy of the signal generator), is quite good.

These mismatching of 64-channel monopolar gain introduces an error in computing single differential signal by software. Consider that a 50Hz power line interference as the common input to all 64 channel, the difference cause by the mismatching between 2 channels will appear as background noise of EMG signals. Obviously, the mismatching of 64-channel monopolar gain is the smaller the better.

3.4.2 Multiplexer and ADC Performance Measurements

3.4.2.1 Objective

The performance of multiplexers and analog digital converter (ADC) in the data acquisition system (DAQ) without Analog Front End was estimated in this section. The function of multiplexer is to select from 1st channel to 64th channel one by one as input to ADC. ADC is used to convert analog input (0~5V) to digital value (16-bit resolution).

3.4.2.2 Method

To perform this evaluation, a ramp (triangular) wave generated by signal generator (Agilent 33210A) was taken as input to 64-channel multiplexers through a 1-to-64 connector and be digitized by ADC. The frequency of the ramp wave was set to 12Hz in order to have enough samples (166 samples) for sample loss detection. The sample loss can be easily detected by a method that subtracting a sample from the previous one (see **Figure3.17**). The test bench is depicted in **Figure3.18**

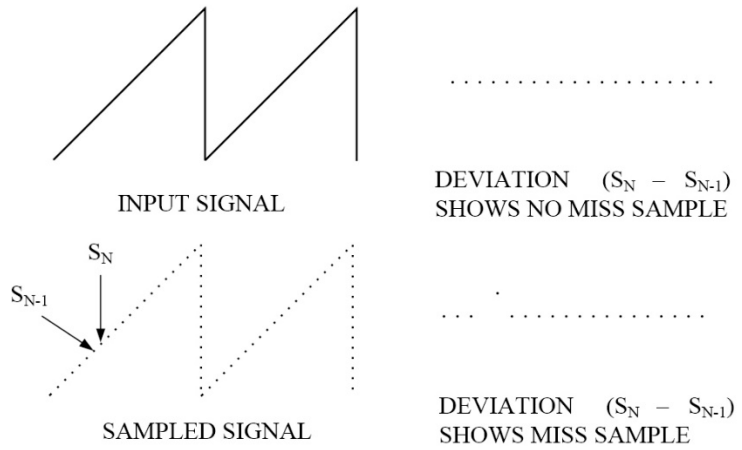


Figure3.17: Diagram shows how to use a ramp (triangular) wave with 12Hz (to have 166 samples for each ramp under 2000 sample frequency) to examine sample loss. The sample loss can be detected by plotting the deviation ($S_N - S_{N-1}$) of digitized signal (ramp wave). S_N and S_{N-1} are the digital value of the N^{th} sample and $(N-1)^{th}$ sample. Deviation plot (upper right) is almost a straight line so that no sample is missed. Another deviation plot (lower right) shows the position of one point twice higher than the other points, indicates one sample is missed.

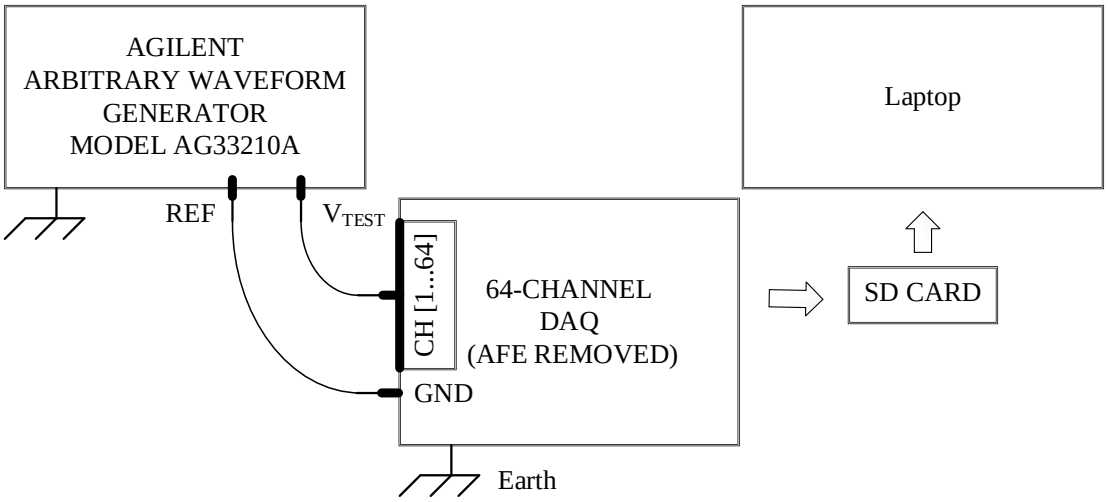


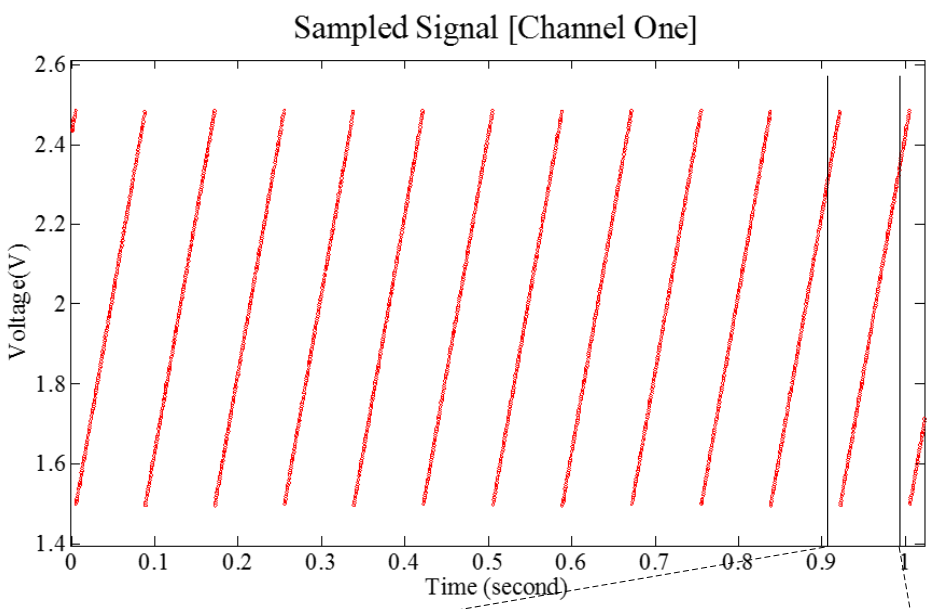
Figure3.18: Test bench block diagram for multiplexer and ADC performance measurements. The input of the 64-channel Data acquisition system (DAQ) is a ramp wave signal (12Hz, 2Voffset, 1Vpeak-to-peak) produced by signal generator (AG33210A). During measurements, the Analog Front End (AFE) was removed from DAQ during the measurements while the GND (Ground) of DAQ was connected to the REF (reference) of AG33210A. The signal was digitized by ADC and recorded in a SD memory card as the results of measurements.

3.4.2.3 Results

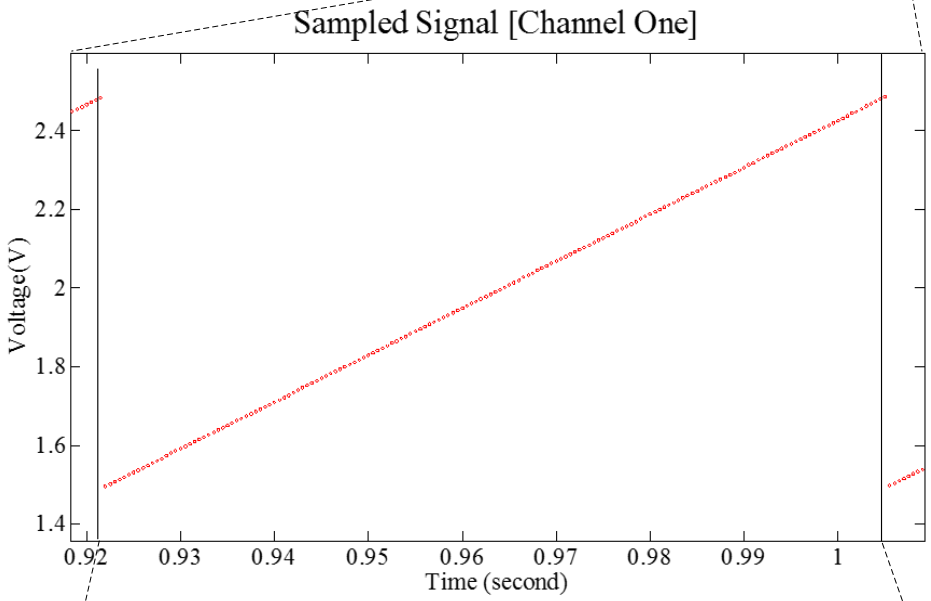
According to the datasheet of signal generator (Agilent 33210A 10MHz Function/

Arbitrary Waveform Generator) [14], the linearity of generated ramp wave is <0.1% of peak output. The linearity error introduced by signal generator is ±1mV (when output of signal generator set to 12Hz, 2Voffset, 1Vpeak-to-peak). **Figure3.19** reports the off-line analysis results by plotting the digitized signals [input signal was a ramp (12Hz, 2Voffset, 1Vpeak-to-peak, nonlinearity ±0.1%)] of channel one under software (Matlab2010a). The expected ΔV is 6mV, if no sample is skipped, as shown in **Figure3.19 (c).** If one sample was skipped, the expected ΔV should be 12mV.

a)


Sampled Signal [Channel One]
Voltage(V)
Time (second)

b)


Sampled Signal [Channel One]
Voltage(V)
Time (second)

c)

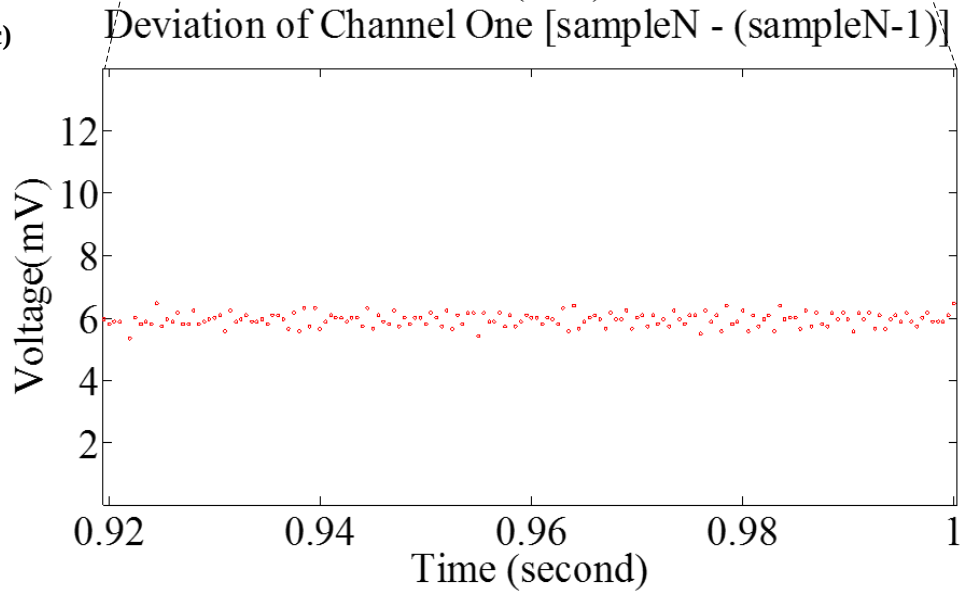

Deviation of Channel One [sampleN - (sampleN-1)]
Voltage(mV)
Time (second)

Figure3.19:Signals acquired by the test bench for multiplexer and ADC performance measurements were plotted channel by channel with Matlab, while the input signal is a ramp wave signal (12Hz, 2Voffset, 1Vpeak-to-peak) generated by signal generator. The sample rate was set to 2000 SPS (sample per second). In (a), twelve ramp waves were detected in a second with amplitude [1.5V, 2.5V], as expected. In (b), the region [0.92s, 1s] of (a) was zoomed in which displayed the last one of the twelve ramp wave in (a). In (c), the deviation [$Sample_N$ – $Sample_{N-1}$: the N^{th} sample value minus the $(N-1)^{th}$ sample value] of the same region of (b) was plotted, which shown that no sample was missed inside that region. The expected ΔVis 6mV, if no sample is skipped.

3.4.3 Wireless Performance Measurements

3.4.3.1 Objective

Wireless Communication System (WCS) supports IEEE 802.11b/g/n and transfers $1/10^{th}$ of every second (first 100ms) data wirelessly through Wi-Fi module with a speed of 204.8 Kbits/s. The performance of WCS along with multi-channel HD-sEMG recording system with wireless communication (HD-sEMG RSWC) prototype was estimated in this section.

3.4.3.2 Method

To perform this evaluation, a sinusoid wave, within the range of sEMG bandwidth [10Hz, 500Hz] generated using signal generator (Agilent 33210A), was taken as the input of the HD-sEMG RSWC prototype. Both the HD-sEMG recording system with wireless communication (HD-sEMG RSWC) prototype and a laptop were linked to the same Access Point (AP).

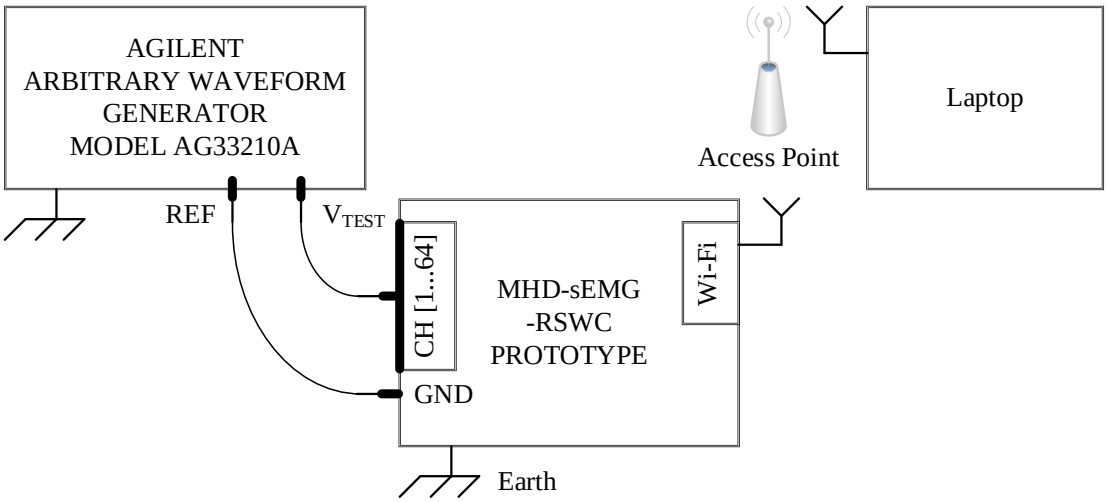


Figure3.20: Test bench block diagram of wireless performance measurements of multi-channel HD-sEMG recording system with wireless communication (HD-sEMG RSWC). The input of the HD-sEMG-RSWC prototype is a sinusoid wave signal (80Hz, 500mVoffset, 20mVpeak-to-peak). During the measurement, the GND (Ground) of HD-sEMG RSWC was connected to the REF (reference) of AG33210A. Both the HD-sEMG-RSWC prototype and the laptop were linked to the same Access Point (AP). The signals were digitized by ADC and 1/10th of every second (first 100ms) data transferred to a laptop with a speed of 204.8 Kbit/s.

3.4.3.3 Results

As shown in **Figure3.20**, the signals were digitized by ADC and 1/10th of every second (first 100ms) data transferred from the HD-sEMG RSWC prototype to a laptop with the speed of 204.8 Kbit/s. The wireless communication in the speed of 204.8 Kbits/s actually was achieved by the following procedures: 1) The HD-sEMG RSWC prototype transmitted twenty packets (and the length of raw data inside each packet is 1280 bytes) in every second; 2) The laptop received data through access point packet by packet and plotted those data sample by sample. If the number of total packets that are transmitted by the HD-sEMG-RSWC prototype and the number of total packets that are received by the laptop are different, packet loss happened. Packet loss rate and radio distance are two important criteria in analysis the performance of wireless communication system, and the results are presented in **Table3.9**.

Table3.9: Wireless performance measurements results from the test bench described in Figure3.20. The radio distance is composes of two parts: 1) the distance between HD-sEMG RSWC prototype and Access Point (AP); 2) the distance between the laptop and AP. The No. Transmitted is the number of transmitted packets (each packet contains 1280 bytes raw data) by the HD-sEMG-RSWC prototype, while the No. Received is the number of received packets (1280 bytes per packet) by laptop. Packet lose rate is calculated by: (No. Transmitted - No. Received/ No. Transmitted) x 100%.

Item	Walking Distance respect to Access Point (meter)	No. Transmitted (packet)	No. Received (packet)	Packet Loss Rate (%)
1	3	1200	1200	0
2	6	1200	1200	0
3	10	1200	1200	0
4	14	1200	1116	0.33

As shown in **Table3.9**, no packet loss happened if the radio distance was less than ten meters (five meters between prototype and AP as well as five meters between laptop and AP). Packet loss happened if the radio distance became more than ten meters. However, the influence of packet loss in 14 meter distance is still less than 1% and that is acceptable when only using wireless signals to check the signal quality. Furthermore, no significant influence was noticed when one person walking as obstacle during the testing.

3.5 System Characteristics

Data acquisition characteristics of the HD-sEMG recording system with wireless communication (HD-sEMG RSWC) prototype are presented in **Table3.10**. **Table3.11** describes timing characteristics of the HD-sEMG recording system with wireless communication (HD-sEMG RSWC) prototype. **Table3.12** describes the electrical characteristics and physical characteristics of HD-sEMG recording system with wireless communication (HD-sEMG RSWC) prototype.

Table3.10: Data acquisition characteristics of the HD-sEMG RSWC prototype. With the multiplexed data acquisition solution (see Figure1.8), one single channel high speed Analog Digital Convertor (ADC) is able to sample as many as sixty-four EMG channels.

SYMBOL	PARAMETER	Value			UNITS
		MIN	TYP	MAX	
N_{CH}	Number of EMG channels		64		number
LPF	3dB cut-off frequency of the low-pass filter[1]		3500		Hz
HPF	3dB cut-off frequency of the high-pass filter[1]		2		Hz
$CMRR_{50Hz}$[2]	Common Mode Rejection Ratio (CMRR) under 50Hz	86		101	dB
Gain	Voltage gain of data acquisition system		96		V/V
f_s	Sample frequency per each channel		2000		SPS
1LSB[3]	1LSB (least significant bit) of data acquisition system for EMG signals	0.76			μV
R_{ADC}	Resolution of ADC[4]		16		bits
D	Walking distance respect to access point		5		m
Delay[4]	Sample delay between two adjacent channels	5		400	μs

Note1: The bandwidth of 64-channel WEMG AFE is set to [2, 3500] Hz, and make the variation of the gain of different frequency inside the bandwidth [10, 500Hz] as little as 2%. However, the mismatching between 2 channels will appear as background noise of EMG signals due to the influence of V_{CM} (common mode voltage).

Note2: This value is a test value in [9].

Note3: LSB (Least Significant Bit). With 100V/V gain amplifier, the accuracy (1 LSB level) of DAQ can reach as small as 0.76μV for sEMG signals with V_{REF}=5V.

Note4: The sample delay between two adjacent channels is caused by not implementing S/H in data acquisition system.

Table3.11: Timing characteristics of the HD-sEMG RSWC prototype. The system clock of the prototype adopts the maxim clock of its MCU (Micro-Control Unit), in order to achieve the highest performance [48MHz SPI1 (Serial Peripheral Interface 1) clock, 10MHz GPIO (General Purpose Input/Output) clock].

SYMBOL	PARAMETER	Value			UNITS
		MIN	TYP	MAX	
Clk_{SYSTEM}	System clock of MCU[1]	1	168	168	MHz
Clk_{SPI1}	Clock of SPI1[2] (Serial Peripheral Interface 1) bus	1	48	48	MHz
Clk_{SPI3}	Clock of SPI3[2] (Serial Peripheral Interface 3) bus	1	2	24	MHz
Clk_{SDIO}	Clock of SDIO (Secure Digital Input/Output) bus[2]		48	48	MHz
Clk_{GPIO}	Clock of GPIO (General Purpose Input/Output)[3]			10	MHz
$T_{A/D}$	A/D conversion time[4]		2	2.5	μs
$T_{SETTLING}$	Settling time after channel switching[5]	0.153	4	4	μs
T_{Delay}	Time delay between samples[6]		6	6.5	μs
S_{SDIO}	Writing throughput of Secure Digital Input Output (SDIO) bus[7]		2,048		Kbit/s
S_{Wi-Fi}	Transmit throughput of the on-board Wi-Fi module[8]		204.8		Kbit/s

Note1: The MCU is STM32F407 (ARM-M4 core, 168MHz, LQFP100 packet, ST Microelectronics) [10].

Note2: SPI1, SPI3 and SDIO interface or bus are all on STM32F407 MCU.

Note3: This 10MHz value is the testing value, which is only 1/5th of maxim 50MHz according to the datasheet.

Note4: A/D conversion time is a tested value of LTC2368-16 by us.

Note5: T_{SWITCH} is a test value that offers sufficient time for 64-channel multiplexed DAQ with ADC LTC2368-16 and is set to a little higher than the calculated safe settling time of ADG726 (0.153μs).

Note6: Time delay between samples is a sum of multiplexer switching time (T_{SWITCH}), settling time and A/D conversion time.

Note7: The SD memory card used for testing is micro-SD SanDisk class 10 16GB.

Note8: The Wi-Fi module used for testing is XBee S6B working under 802.11g standard.

Table3.12: Electrical characteristics and physical characteristics of the HD-sEMG RSWC prototype.

SYMBOL	PARAMETER	Value			UNITS
		MIN	TYP	MAX	
V_{DD}	Supply voltage	5.0	7.5[1]	9.0	V
$V_{CHARGER}$	Battery charger voltage		8.4[2]		V
$I_{CHARGER}$	Battery charger current			1.3[2]	A
Size	Dimension of the prototype	188(L)x188(W)x67(H)[3]			mm
Weight	Weight of the prototype (including enclosure)	1200			g

Note1: The prototype adopts a Li-ion rechargeable battery with nominal ratings 7.5 V and 2.2 Ah [11].

Note2: The type of the charger is 2240 Li-Ion batteries charger (Mascot Group) [12].

Note3: The prototype is placed in an enclosure box with the size of 188(L) x 188(W) x 67(H) mm^3 [13].

Table3.13 describes the power consumption of the HD-sEMG recording system with wireless communication (HD-sEMG RSWC) prototype. The power consumption of HD-sEMG RSWC is a sum of power consumption of its sub-systems, which include MCU, DAQ and WCS. And the battery used in HD-sEMG RSWC is Li-ion rechargeable battery (No.800052 manufactured by Enix-energies). Its nominal ratings is: 7.5 V, 2.2 Ah or 7.5V, 16.5Wh (consider that 1Wh=1mAh÷1000×1V and 16.5Wh = 2200mAh÷1000×7.5V). Note: Actual voltage and capacity in use will be affected by various factors, including temperature, discharge rate, charge rate and method (if applicable), end point voltage, history (e.g. past use, storage) etc.

Table3.13: Power consumption of the HD-sEMG RSWC prototype.

Symbol	Description	Value	
		V_{DD} (V)	**I_{DD} (mA)**
P_{MCU}	Power consumption of Micro-Control Unit (MCU), including the power that drive SD memory card.	3.3	109
DAQ	Power consumption of DAQ system, include Analog Front End (AFE), multiplexers and ADC.	5[1] 2.5[1] -2.5[1] 5[2] 2.5[3]	100 50 50 0.8 6.3
WCS	Power consumption of Wireless Communication System (WCS).	3.3	225

Note1: analog front end (AFE) requires 5V and ±2.5V power supply.

Note2: multiplexers (four chips of ADG726) require 5V power supply.

Note3: analog digital converter (ADC) requires 2.5V power supply.

Consider that Li-ion rechargeable battery should not be discharged completely (to keep the state of battery in a good condition) and the conversion efficiency of DC-DC regulator is less than 100%, we add a 50% ratio in the calculation of working hours of battery after full charged:

7.5V x 2200mAh x 50% =
(3.3Vx109mA+5Vx100mA+2.5Vx100mA+5Vx0.8mA+2.5Vx6.3mA+3.3Vx225mA)
x Working Time (hour) (3-3)

According to equation (3-3), the working time of the battery could reach as much as four hours after fully charged. And this value should be verified in real measurement.

Table3.14 describes RF characteristics of the HD-sEMG recording system with wireless communication (HD-sEMG RSWC) prototype. User Datagram Protocol (UDP) is one

of the core members of the Internet protocol suite [15]. It uses a simple connectionless transmission model with a minimum of protocol mechanism. It has no handshaking dialogues, and thus exposes any unreliability of the underlying network protocol to the user's program. There is no guarantee of delivery, ordering, or duplicate protection. UDP provides checksums for data integrity, and port numbers for addressing different functions at the source and destination of the datagram. Transmission Control Protocol (TCP) is one of the core protocols of the Internet protocol suite (IP), and is so common that the entire suite is often called TCP/IP [16]. TCP provides reliable, ordered and error-checked delivery of a stream of octets between programs running on computers connected to a local area network, intranet or the public Internet. It resides at the transport layer. The protocol that used in our system is UDP, which emphasizes low-overhead operation and reduced latency rather than error checking and delivery validation.

Table3.14: RF characteristics of the HD-sEMG RSWC prototype. This prototype is powered by XBee S6B Wi-Fi module (manufactured by iDigi International).

Items	Descriptions
Frequency	ISM (Industrial Scientific Medical) 2.4-2.5GHz
Number of Radio Channels	13
Adjustable Power	Yes
Wi-Fi Standards	802.11 g
Transmit Power Output (Average)	up to +16 dBm
RF Data Rates	1 Mbit/s to 72.22 Mbit/s[1]
Receiver Sensitivity	-93 to -71 dBm
Transmission Protocol	UDP[2] TCP[3]

Note1: 1Mbit/s and 72.22Mbit/s are only the radio frequency (RF) data rates, the data throughput is much lower than RF Data Rates.
Note2: UDP (User Datagram Protocol).
Note3: TCP (Transmission Control Protocol).

3.6 System Calibration

This section describes how to perform calibration of the HD-sEMG recording system with wireless communication (HD-sEMG RSWC) prototype. The diagram of the test bench to implement testing and calibration of HD-sEMG RSWC prototype is presented in **Figure3.21**. The positions of these test points are depicted in **Figure3.22**.

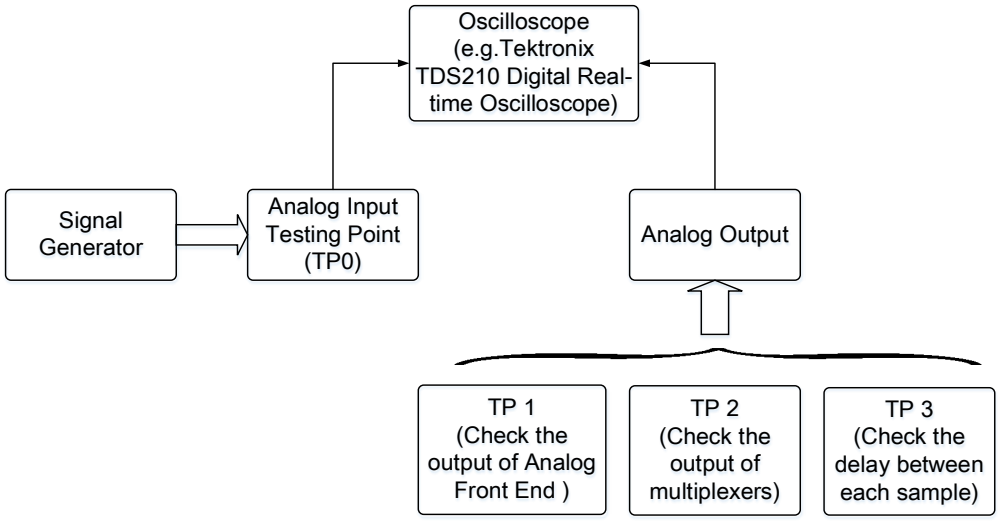


Figure3.21: Test bench for the calibration of the HD-sEMG RSWC prototype. The method is to monitor different outputs at different testing points (TPs) with an oscilloscope (e.g. Tektronix TDS210) and check whether we can get the expected results or not. Test point 0 (TP0) is 1 point, which is set to the 64-channel input connector of analog front end (AFE); test point 1 (TP1) is 64 points, which are set to each of 64-channel output connector of AFE; test point 2 (TP2) is 1 point, which is set to the common output point of multiplexers; test point 3 (TP3) is 1 point, which is set to the conversion trigger signal (CNV) of ADC.

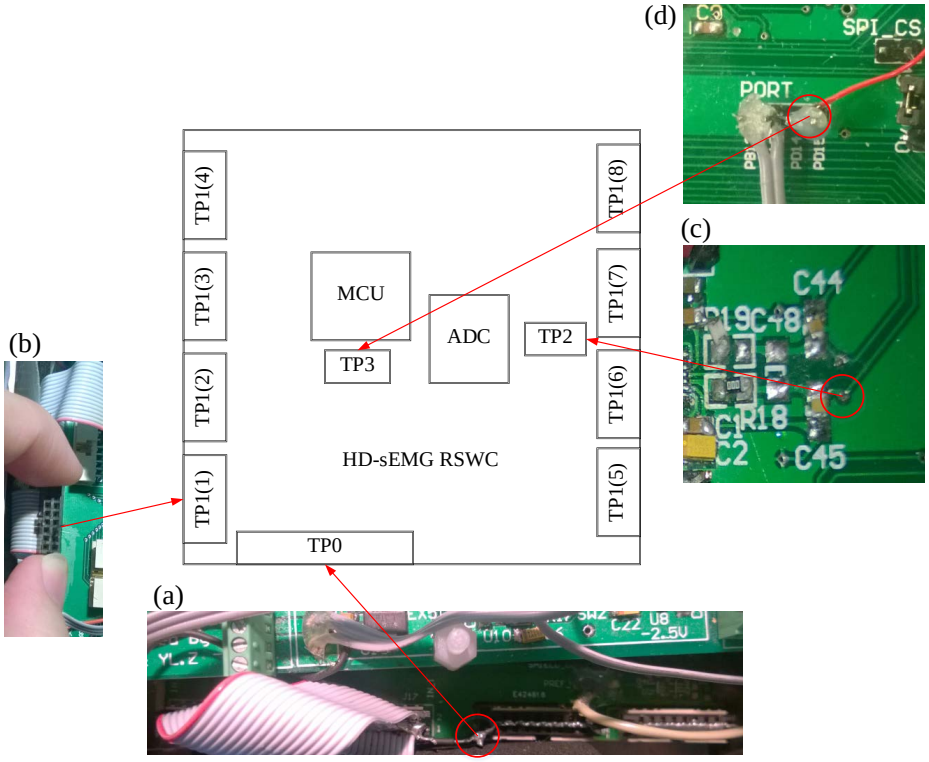


Figure3.22: Positions of test points of the HD-sEMG RSWC prototype. (a) Test point 0 (TP0) is 1 point, which is set at the common end of 1-to-64 channel connector as input to analog front end. (b) Test point 1 (TP1) consists of 64 points (64-channel output of AFE), and an example of channel 1 to channel 8 is provide at the left side of the figure. (c) Test point 2 (TP2) is 1 point, which is set to the common output point of multiplexers (placed near capacitor C45). (d) Test point 3 (TP3) is 1 point, which is set to the input conversion signal (CNV) of ADC.

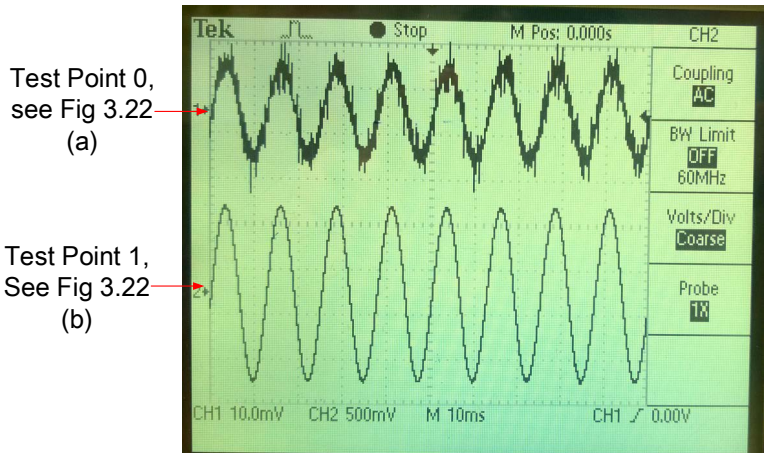


Figure3.23: An example of oscilloscope image taken during the calibration of analog front end (AFE) of HD-sEMG RSWC prototype. The calibration is done by comparing two signals from TP0 and TP1 that monitored by an oscilloscope (e.g. Tektronix TDS210). In this example, the input signals was a sinusoid wave (80Hz, 20mV peak-to-peak, no offset) generated by signal generator. The signals acquired from TP0 showed the origin signal was a sinusoid wave (80Hz,

20mV peak-to-peak, no offset) with noise. The signals acquired from TP1 showed the signal was a sinusoid wave with 96 V/V gain of the origin signal (80Hz, 20mV peak-to-peak, no offset) with noise removed. Because each channel of the AFE includes a band-pass filter. The steps appears in the displaying signal of test point1 is caused by the resolution of digital oscilloscope, which actually is not exist in real signal (checked recorded signals during this test from our data recording system visually).

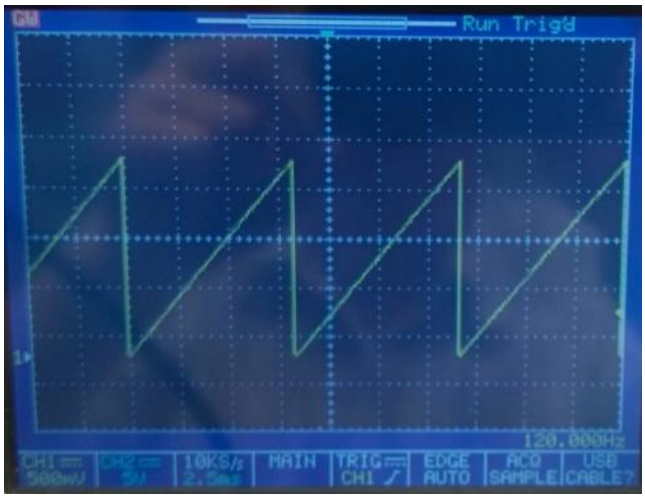


Figure3.24: An example of oscilloscope image taken during the calibration of multiplexers and ADC. The calibration is done by monitoring TP2 (Test Point 2) with an oscilloscope. In this example, the input signal to multiplexers directly (without AFE connected) was a ramp wave (120Hz, 2V peak-to-peak, 2V offset) generated by the signal generator. The signals acquired from TP2 showed exactly the same shape of the input signal of the ramp wave (120Hz, 2V peak-to-peak, 2V offset).

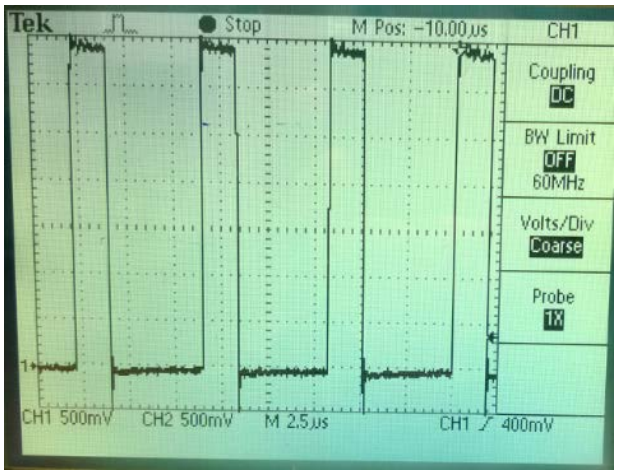


Figure3.25: An example of oscilloscope image taken during the calibration of the delay between two channels of the HD-sEMG RSWC. The calibration is done by monitoring TP3 (Test Point 3) with an oscilloscope. The signals acquired from TP3 showed conversion trigger signal (CNV) of ADC. The delay between two channels (measured by computing the time duration between the rising edges of the square waves) was 6µs.

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ui/static/active/en/resource/technical/document/datasheet/DM00037051.pdf. Accessed on: Sep.15, 2014.

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4

Off-line Signal Processing

4.1 Signal Display

Sixty-four channel surface monopolar EMG signals are recorded in a SD memory card as plain binary files as described in **SECTION3.3.3**. The 64-channel electrode array (see **Figure5.2**) that used in our physiological applications (described in **SECTION5**) is 8x8, with IED =1cm.

Figure4.1 describes how to display 64-channel EMG signals off-line. Recorded signals are loaded to Matlab (version 2010a) as 16-bit data with big endian encoding format (machine code). Pre-processing is performed to remove (or reduce) electrodes offset, artefact and noises. Root mean square (RMS) amplitude of the monopolar surface EMG

signals is used for muscle activity estimation.

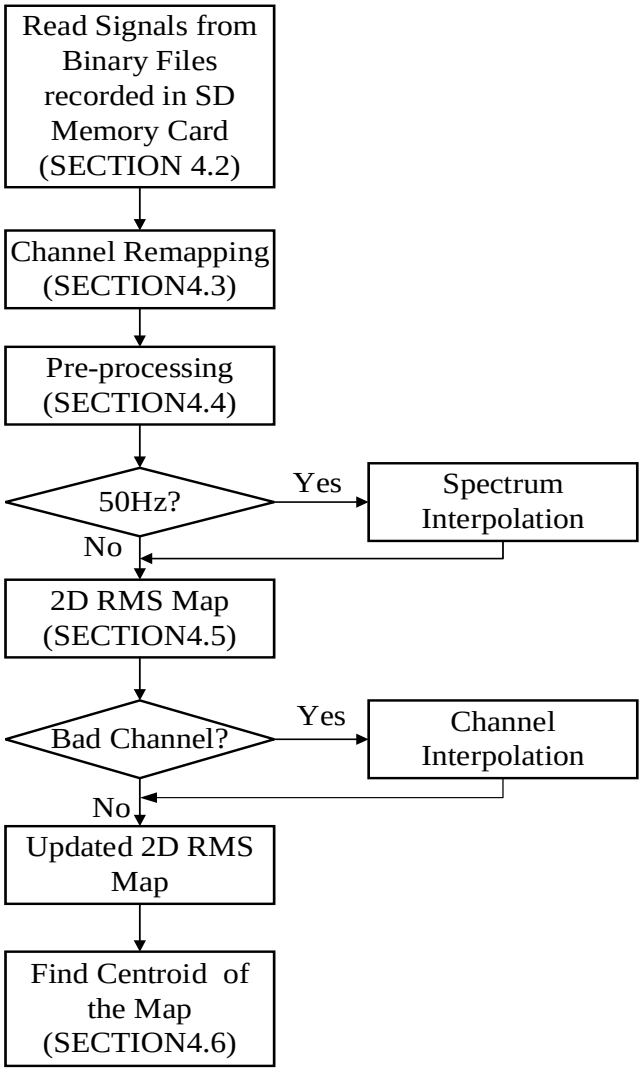


Figure4.1: Data processing flow chart. Raw sixty-four channels surface EMG signals are recorded in SD memory card as binary files and these binary files are read into MATLAB by the program described in "read signals from specific binary files" (see Figure4.2). In "channel remapping", data are going to be converted from 1D (one-dimension) to 2D (two-Dimension) described in Figure4.3**. In "pre-processing", the electrodes offset, artefacts and other noises outside the EMG bandwidth [20Hz, 500Hz] are removed (or reduced) from raw signals by the program described in Figure4.5,. After pre-processing, Power-Spectral-Density (PSD) analysis is used to check whether 50Hz power line interference exists or not. If exists, spectrum interpolation is performed to reduce 50Hz power line interference and its harmonics (up to 10th harmonics) by the program described in Figure4.8. In "bad channel detection", channel interpolation will be performed to update the RMS map if bad channels are detected. Finally, the centroid of the updated map (replacing the values below threshold with zero) is found and marked with white cross by the program described in section4.6.**

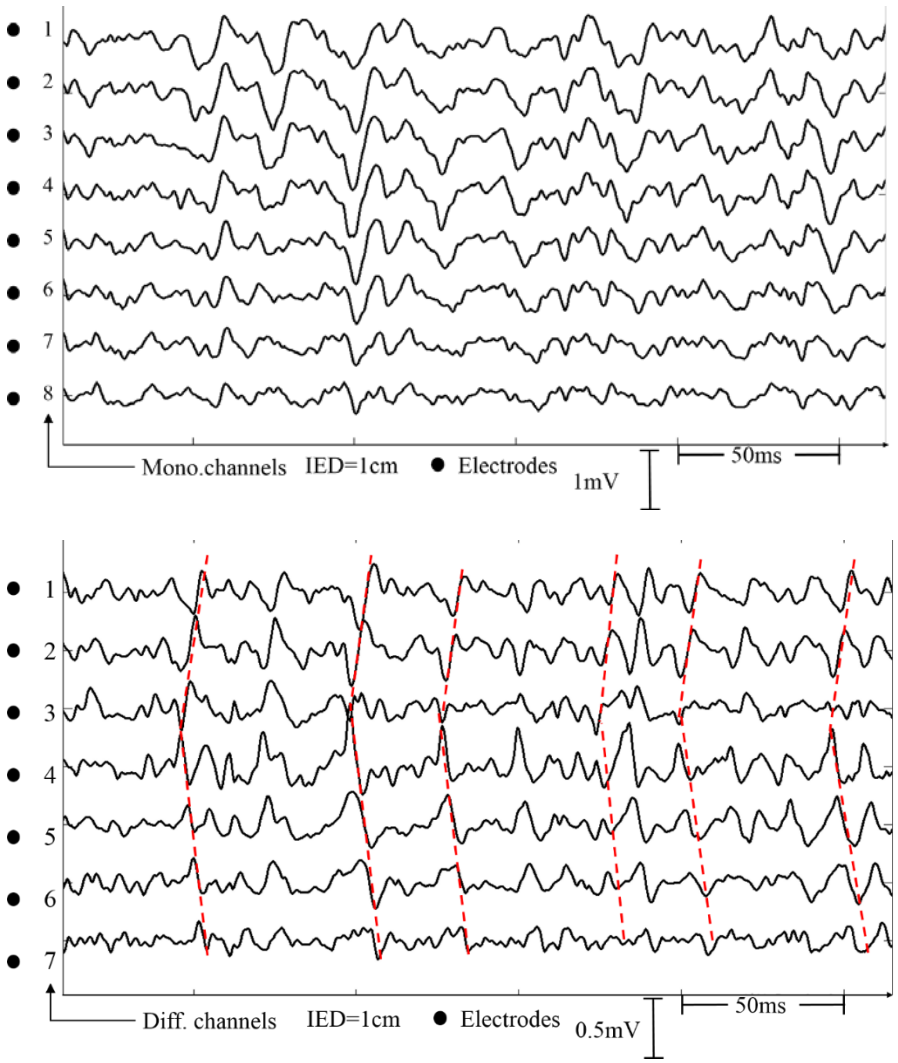


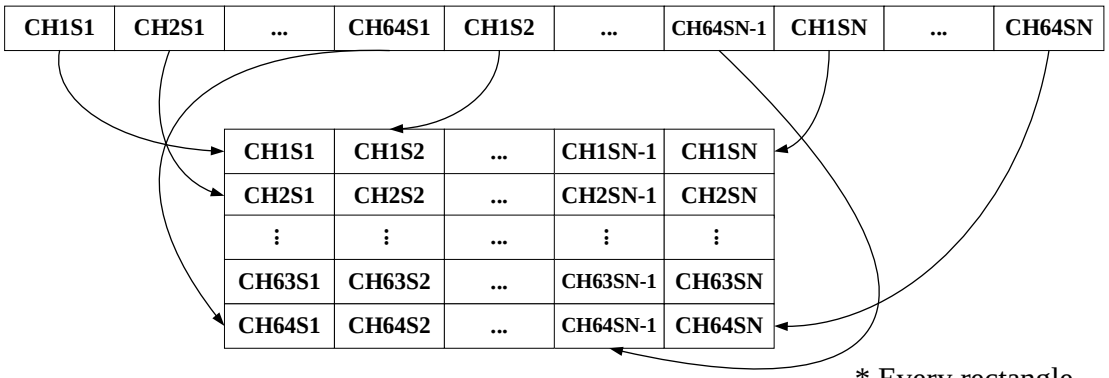
Figure4.2: Monopolar (upper) and single differential (lower) EMG signals acquired from column 3 of the 64-channel electrode grid (see Figure5.2) of subject 1 (S1) contracting with holding 3kg weight. EMG signals acquired originally were monopolar and were computed to single differential by software. In single different mode, motor unit action potential (MUAP) produced by motor units of biceps brachii is easy to be detected with an inter-electrode distance (IED) of 1cm. The red lines indicate the propagation of MUAPs along muscle fiber direction.

4.2 Read Signals from Binary Files

EMG signals (16-bit each sample) are recorded in SD memory card following a big-endian ordering, as described in **SECTION 3.3.3**. These data are loaded to MATLAB using the function “fread” with arguments ‘uint16’ and ‘b’ [1]. ‘uint16’ sets the precision of the reading data to unsigned 16-bit integer. ‘b’ set the machine format to

big-endian ordering. After implementing “fread” function, MATLAB will read these data and produce an array of data that needs to be reshaped so that data are represented as two dimension matrix (see **Figure4.3**).

a) An array of data read by ‘fread’ function under MATLAB*



b) A 64xNsamples matrix reshaped from a)

* Every rectangle contains a 16-bit value

Figure4.3: (a) Structure of the raw data loaded into MATLAB is an array that consists of recorded samples in a specific ordering. (b)The structure of reshaped data is a 64xNsamples (Number of samples) matrix. After reshaping, each row of the 64xNsample matrix contains all the samples acquired from the same channel. ‘CH1S1, CH1S2, …, CH1SN-1,CH1SN’ indicate the 1st, 2nd, …, (N-1)th, Nth sample of channel one. ‘CH2S1, CH2S2, …, CH2SN-1,CH2SN’ indicate the 1st, 2nd, …, (N-1)th, Nth sample of channel two. ‘CH63S1, CH63S2, …, CH63SN-1,CH63SN’ indicate the 1st, 2nd, …, (N-1)th, Nth sample of channel sixty-three. ‘CH64S1, CH64S2, …, CH64SN-1,CH64SN’ indicate the 1st, 2nd, …, (N-1)th, Nth sample of channel sixty-four.

4.3 Channel Remapping

The sEMG signals are recorded using two 4x8 electrodes grids, however, the order of the electrodes in a 2D grid is different from the order of input channels in data acquisition system of the multi-channel HD-sEMG recording system with wireless communication. To show the spatial localization of EMG amplitude distributions of these signals in a 2D map, a channel remapping procedure is required. According to the placement direction of the electrodes, two different remapping methods are depicted in **Figure4.4** and **Figure4.5**.

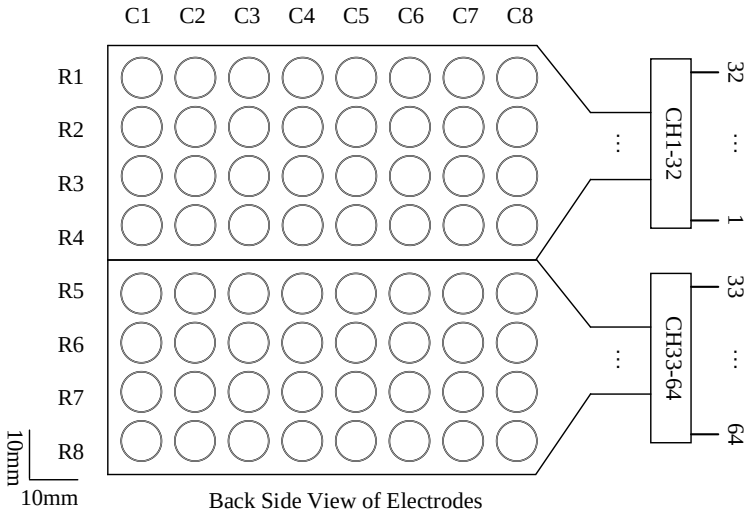


Figure4.4: Channel remapping method 1 according to the placement of 64-channel electrode grid and the connections with input channels of data acquisition system of the multi-channel HD-sEMG recording system with wireless communication as presented in this figure. CH33-64 connector (a 32-channel connector connected with channel 33-64 of the data acquisition system) is connected to the lower 32-channel electrodes grid and CH1-32 connector (another 32-channel connector is connected with channel 1-32 of the data acquisition system) connected to the upper 32-channel electrodes grid. C1 is column 1 and R1 is row 1. The Inter-Electrode Distance (IED) is 10mm.

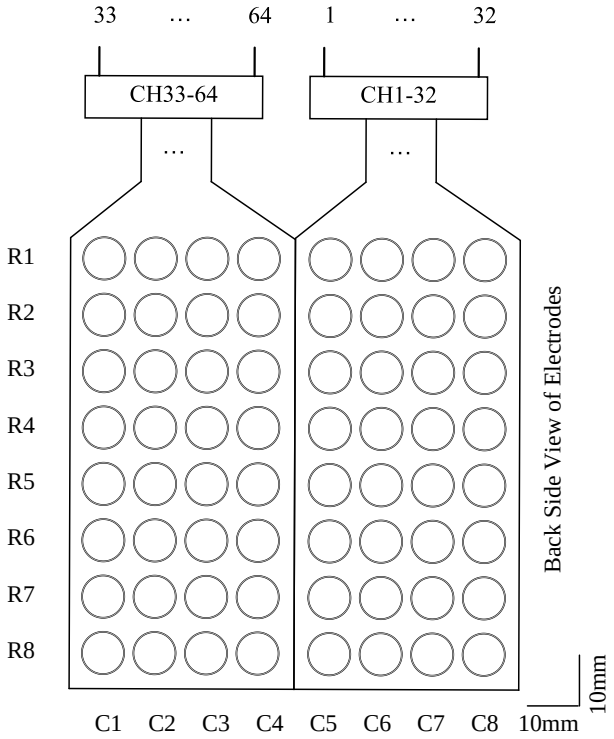


Figure4.5: Channel remapping method 2 according to the placement of 64-channel electrode grid and the connections with input channels of data acquisition system of the multi-channel HD-sEMG recording system with wireless communication as shown in this figure. CH33-64 connector (a 32-channel connector connected with channel 33-64 of the data acquisition system) is connected to the left 32-channel electrodes grid and CH1-32 connector (another 32-channel connector is connected with channel 1-32 of the data acquisition system) connected to the right 32-channel electrodes grid. C1 is column 1 and R1 is row 1. The Inter-Electrode Distance (IED) is 10 mm.

4.4 Pre-processing

Raw HD-sEMG signals are contaminated by various noises (electrode noise, electrode motion artefact, cable motion artefact and alternating current power line interference) [2]. Therefore, pre-processing will be performed to remove (or reduce) these noises.

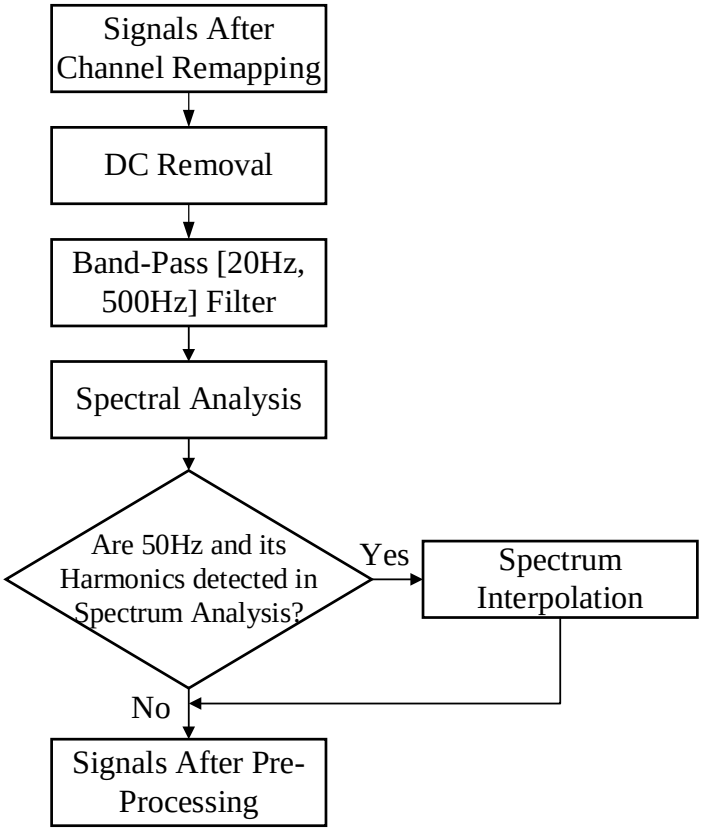


Figure4.6: Signals pre-processing flow chart. In "DC Removal", the DC offsets were removed from each signal after channel remapping. A 2nd order digital Butterworth zero-lag band-pass (around [20, 500] Hz) filter was performed to remove the noises outside surface EMG bandwidth. If 50Hz power line interference and its harmonics were detected using spectral analysis, an approach called spectrum interpolation will be performed to reduce the power line interference and its harmonics (up to 10th harmonics).

By means of a 2nd order digital Butterworth zero-lag filter with cut-off frequency at 20Hz (high-pass) and 500Hz (low-pass), noises outside of the bandwidth of surface EMG can be removed. Furthermore, spectral analysis and spectrum interpolation are performed to detect and reduce the 50Hz power line interference and its harmonics, which are inside the surface EMG bandwidth [20Hz, 500Hz].

Spectral analysis of EMG signals detected during voluntary constant force isometric contractions is usually performed using the short time Fourier transform (STFT) with nonoverlapping epochs of 0.25 to 1s [3]. **Figure4.7** depicts how to perform Power Spectral Density (PSD) estimation of three second EMG signals during voluntary

contractions

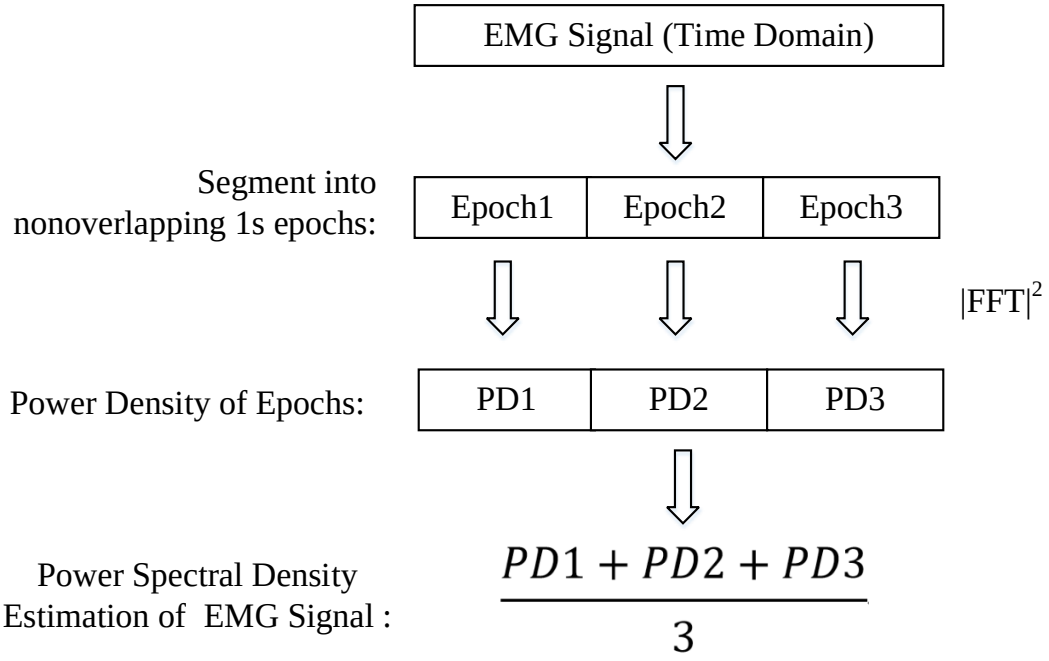


Figure4.7: Estimation of EMG signal (3s) spectrum. In the spectral estimation during voluntary contractions, EMG signal is divided into a sequence of 1s epochs during which the signal is assumed stationary. Power Spectral Density (PSD) estimation is the average of the power density of three epochs.

As shown in **Figure4.6**, Fast Fourier Transform (FFT) is adopted to generate the spectrum of a given EMG signal. The FFT is a faster version of the Discrete Fourier Transform (DFT). The FFT utilizes some clever algorithms to do the same thing as the DFT, but in much less time [4].

In mathematics, DFT converts a finite list of equally spaced samples of a function into a list of coefficients of a finite combination of complex sinusoids, ordered by their frequency [5]. It can be said to convert the sampled function from its original domain (often time or position along a line) to the frequency domain. The DFT of a signal may be defined by the following equation [6].

$$X(\omega_k) \triangleq \sum_{n=0}^{N-1} x(t_n) e^{-j\omega_k t_n}, \quad k = 0,1,2,\dots,N-1 \qquad (4\text{-}1)$$

Where '≜' means "is defined as" or "equals by definition", and

$x(t_n)$ ≜ input singal amplitude (real or complex) at time t_n(sec)

t_n ≜ $nT = nth$ sampling instant (sec), n is an integer ≥ 0

T ≜ $t_n - t_{n-1}$sampling interval (sec),

$X(\omega_k)$ ≜ spectrum of x (complex valued), at frequency ω_k (k^{th} harmonic)

N ≜ number of time samples = no. frequency samples (integer).

Matlab's FFT function is an effective tool for computing the DFT of a signal. The syntax of the function in Matlab is: Y = fft(X,N), which returns the n-point DFT. If the length of X is less than N, X is padded with trailing zeros to length n. If the length of X is greater than N, the sequence X is truncated. When X is a matrix, the length of the columns are adjusted in the same manner [7]. In our application, the 'N' in the syntax of Y = fft(X,N), is set to the length of 'X'. Furthermore, if 'N' is set to the length of 'X', it can be seen that there is even symmetry around the center point, 0.5 x length of 'X', the Nyquist frequency. This symmetry adds redundant information. In our application, N is set to 2000 (is not the power of 2), which is the sample rate of the system.

If 50 Hz and its harmonics are detected with PSD estimation, spectrum interpolation will be performance to remove or reduce 50 Hz and its harmonics. By spectrum interpolation [8][9], the magnitude and phase of the EMG spectrum at 50 Hz and its harmonics are interpolated (estimated) by the magnitude and phase of spectra lines around (±2Hz) the 50Hz and the harmonics respectively. **Figure4.7** depicts how to perform a linear interpolation of the magnitude of 50Hz.

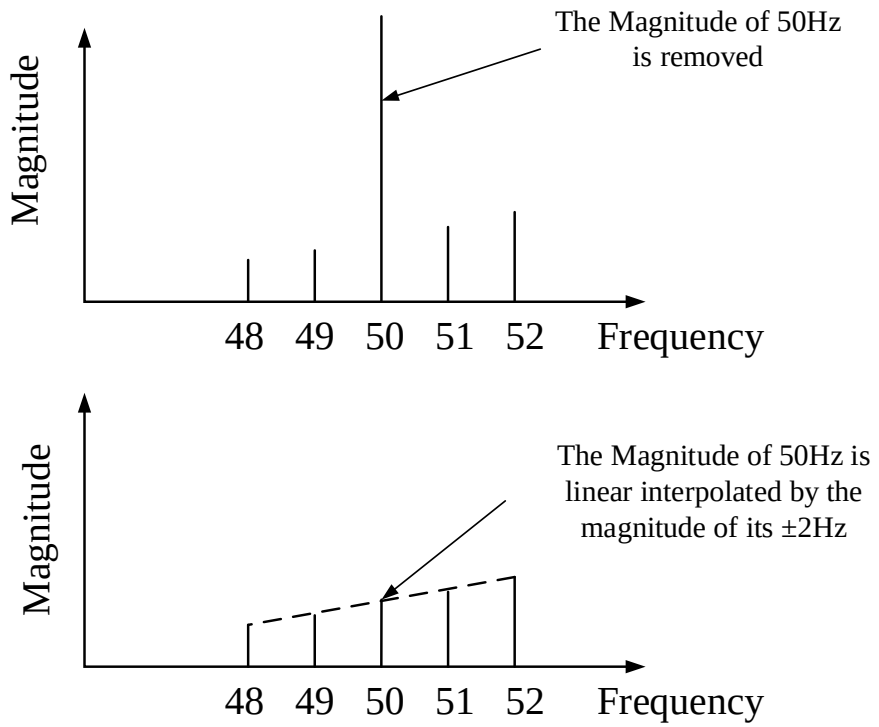


Figure4.8: An example shows how to perform linear interpolation to a signal (with epoch length considered as 1 s). The magnitude of origin 50Hz is removed and interpolated with the average magnitude of 48Hz to 52 Hz (±2Hz to 50Hz respectively).

Besides the magnitude of 50Hz, the phase of 50Hz, the magnitude and phase of the harmonics (10th) of 50Hz are also interpolated with the same method (linear interpolation) presented in **Figure4.7**. Based on this concept, the following procedures are performed for removing 50Hz power line interference and its harmonics in digitized EMG recordings. The diagram of the procedures is depicted in **Figure4.8** and an example of the EMG signal before and after pro-processing is presented in **Figure4.9**.

1) The total length of EMG signal were segmented into 1s epoch signals;
2) Spectral interpolation over magnitude and phase of each epoch;
3) Using inverse FFT, return the interpolated signals in frequency domain to time domain.

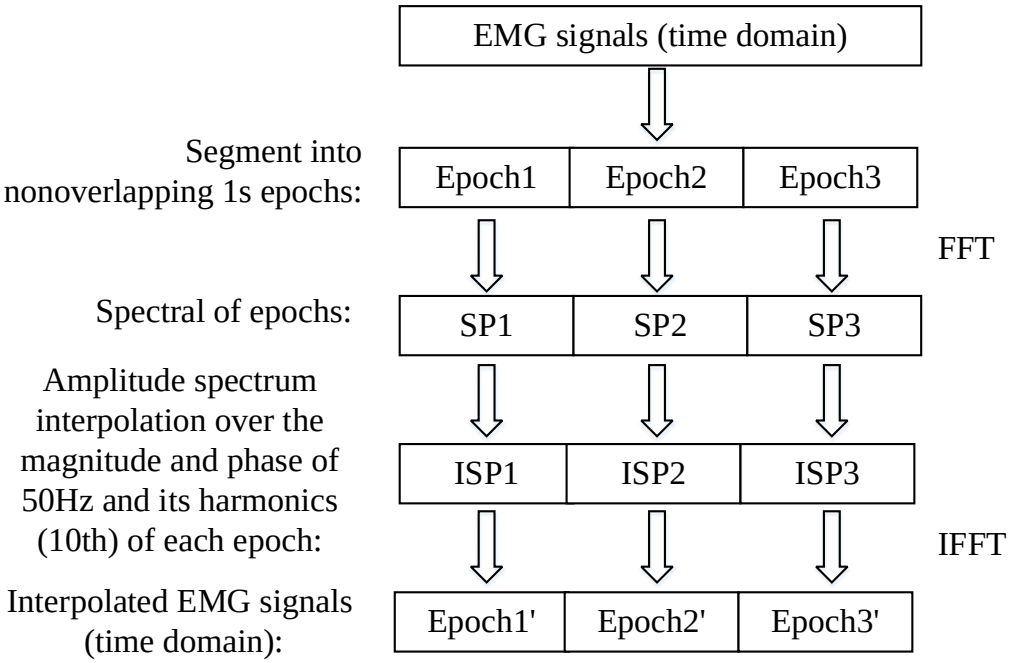


Figure4.9: Diagram of the procedure to perform the spectrum interpolation of EMG signal during voluntary contractions over the magnitude and phase of 50Hz and its harmonics. The total length of EMG signal (3s) were segmented into 1s epoch signals. Using FFT, each epoch was transmitted into frequency domain, indicated by SP1, SP2 and SP3. Each epoch was interpolated over the magnitude and phase of 50Hz and its harmonics (10th), indicated by ISP1, ISP2 and ISP3. Each 1s epoch was transmitted to time domain using inverse FFT (IFFT), and the sum of these nonoverlapping 1s epoch returned a 3s interpolated EMG signal in time domain.

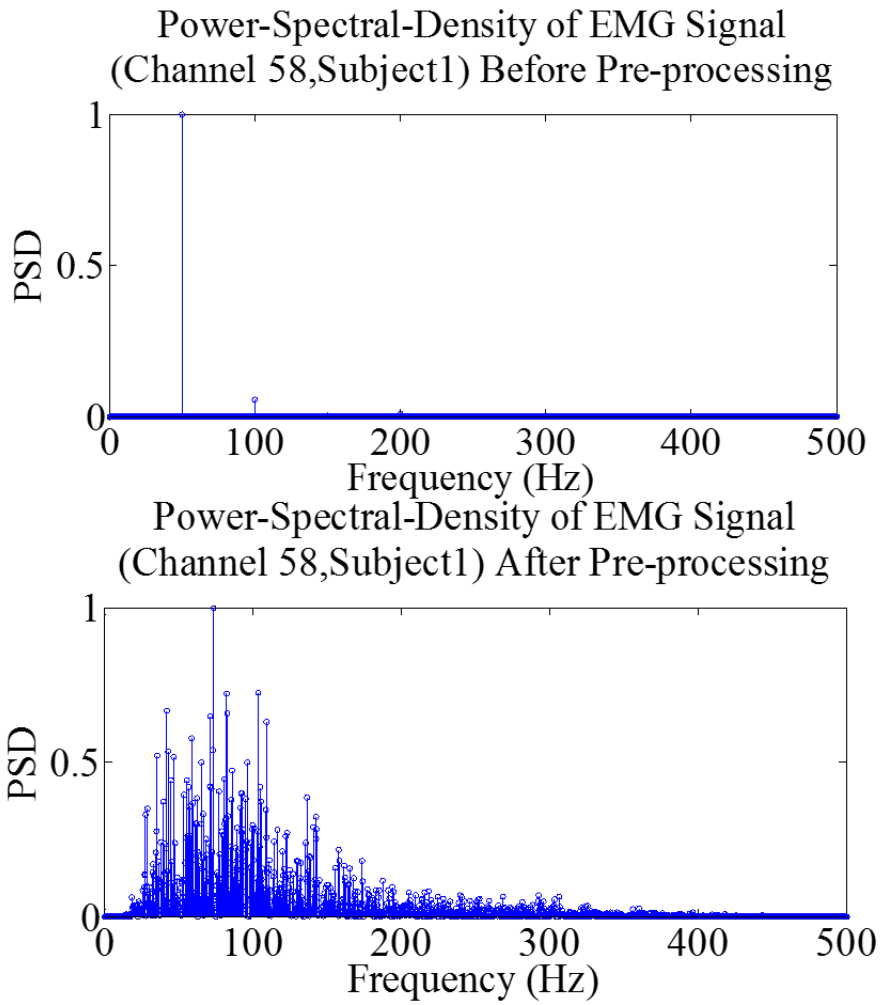


Figure4.10: Power-Spectral-Density (PSD) plot of experimental data (channel 58, subject1) before (upper) and after pre-processing (lower). After pre-preprocessing, the DC offset and other noise outside the surface EMG bandwidth was removed. The 50Hz power line interference and its harmonics (10th) are reduced significantly by spectrum interpolation.

4.5 2D RMS Map

The amplitude of the EMG signal in time is stochastic or random. The root mean-square (RMS) is considered to be the most meaningful parameter because it reflects the level of the physiological activities in the motor units during contraction [10]. RMS gives a measure of the power of the EMG signal. For small muscles, the relationship between force and the RMS of EMG signal tend to be linear [11]. Despite the fact that there is

not a simple equation to correlate the muscle force with the EMG signal amplitude, the qualitative relationship between them has proved useful in many scenarios [12].

The RMS value of a set of values is the square root of the arithmetic mean of the squares of the original values (or the square of the function that defines the continuous waveform). In the case of a set of *n* sampled values $\{x_1; x_2; \dots ; x_n\}$, the RMS is defined as following.

$$X_{RMS} \triangleq \sqrt{\frac{1}{n}\left(x_1^2 + x_2^2 + \cdots + x_n^2\right)}$$

Where '≜' means "is defined as" or "equals by definition".

The way to plot a 2D RMS map of the two dimensional high density surface EMG (HD-sEMG) in our application is described as following. The signals inside the epoch [1s, 4s] were extracted to calculate the RMS values of each channel and fill these values to a 2D map with a colored bar. If exists, the RMS value from bad channel (due to short-circuit in adjacent electrodes or bad contact of electrode-gel-skin interface and so on) should be interpolated to update a new 2D RMS map [13]. **Figure4.10** depicts how to interpolate the RMS of two bad channels with their close-proximity neighborhood.

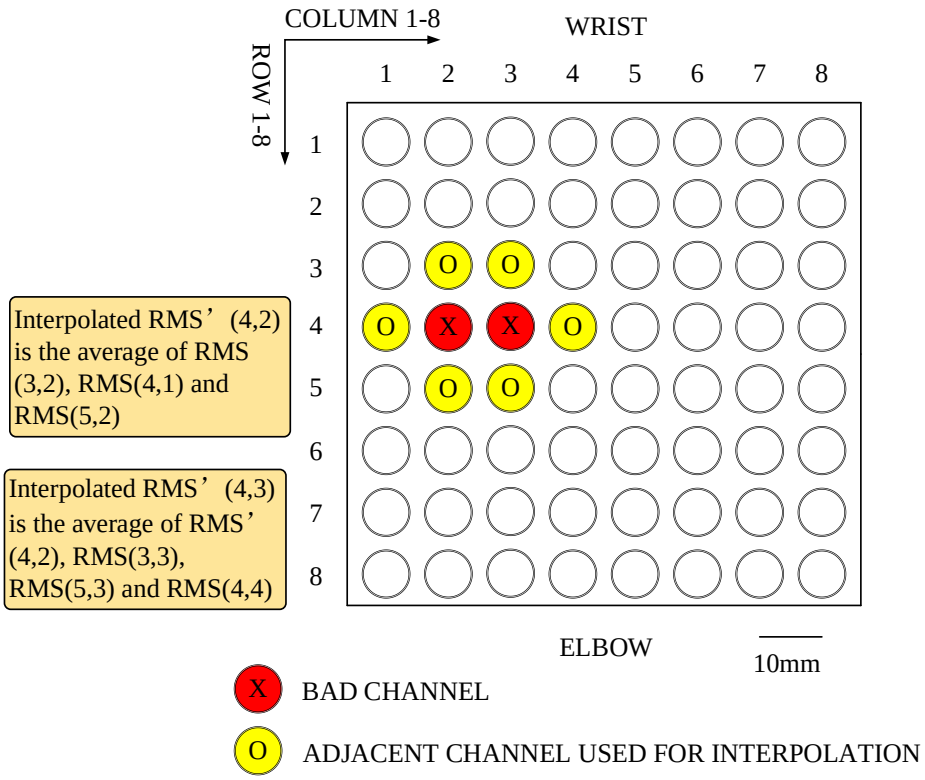


Figure4.11: Bad channel interpolation methodology in 2D RMS map. Two bad channels, with RMS value of RMS(4,2) and RMS(4,3), can be interpolated by their close-proximity neighborhood. RMS(4,2) and R' (4,2) are the origin RMS value and interpolated value row four column two in the 2D RMS map. RMS(4,3) and RMS'(4, 3) are the origin RMS value and interpolated value of row four column three in the 2D RMS map. The two circles colored with red are using to mark the bad channels, while the circles colored with yellow mark the channels used for interpolation.

4.6 Find the Centroid of the RMS Map

Centroid of 2D RMS map (or image) is commonly used to estimate the position of the EMG source during each contraction. These 2D RMS maps were updated by replacing the RMS values below a threshold (e.g. 70% of the maximal RMS value of the RMS map) with zero, in order to make a better estimation of most active region [14]. Furthermore, different thresholds (60%, 70% and 80% of the maximal RMS value of the RMS map) will be applied to our experimental data acquired during the physiological application (**SETCTION5.4**) to select a proper threshold.

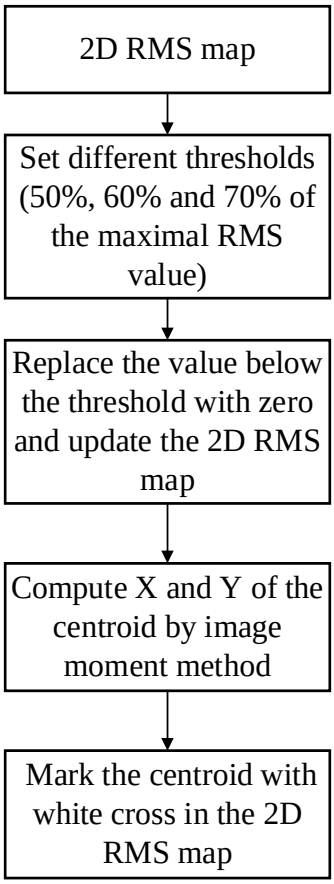


Figure4.12: Flow chart of the procedures to find and mark the centroid of the 2D RMS map. The 2D RMS maps are updated by replacing the RMS values below the threshold (50%, 60% and 70%) with zero. The coordinate (X, Y) of the centroid of the new RMS map is calculated by image moment method and is marked on the same RMS map with white cross.

In image processing, computer vision and related fields, an **image moment** is a certain particular weighted average (moment) of the image pixels' intensities, usually chosen to have some attractive property or interpretation. Image moments are useful to describe objects after segmentation. Some properties of the image which are found via image moments include area (or total intensity), its centroid, and information about its orientation [15]. Image moment is computed as following. If $f(x, y)$ defines the pixel intensities of a scalar (greyscale) digital image, then the moment (sometimes called "raw moment") of order (p + q) is defined as:

$$\mathrm{M}_{pq} = \sum_x \sum_y x^p y^q f(x, y) \qquad (4\text{-}2)$$

Where $\bar{x} = \frac{M_{10}}{M_{00}}$ and $\bar{y} = \frac{M_{01}}{M_{00}}$ are the components of the centroid.

Positions of centroids will be vary according to different thresholds and the proper threshold for detecting the most active area during the contractions in the physiological application (see **SETCTION5**) will be investigated in **SETCTON 5.3.3**.

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