The Doherty Power Amplifier: Review of Recent Solutions and Trends

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***Abstract*—In this work, an extensive review of the most up-to-date papers on microwave Doherty power amplifiers is presented. The main applications are discussed, together with the employed semiconductor technologies. The different research trends, all aimed to improve the advantages of the Doherty scheme and to solve its inherent drawbacks, are presented. The first considered topic is the maximization of efficiency and/or linearity, where analog and digital techniques are exploited. Another important trend is the bandwidth enlargement of the Doherty architecture, that involves a large number of papers. Multi-band, multi-mode solutions are also considered, using either fixed or reconfigurable solutions. The final section is dedicated to the most significant Doherty integrated implementation.**

***Index Terms*—Doherty power amplifier, gallium nitride, gallium arsenide, linearization, wireless communications.**

I. Introduction

WIRELESS communications have been literally exploding in the last few years, and their growth is not expected to stop in a near future. While the market is asking for higher throughput and lower power consumption, the designers of wireless transmitters have to cope with even more stringent demands on system bandwidth, linearity and versatility.

The power amplifier (PA) is a crucial element of the transmitter, since it strongly affects both power efficiency and linearity [1].

Thanks to its high efficiency in a wide range of output power, the Doherty Power Amplifier (DPA) [2]–[4] represents a convenient, widely adopted solution for PAs dealing with the amplitude modulated signals required to achieve the throughput needed in modern digital transmitters. In this paper, we present a review of the most recently published contributions on DPAs, giving continuation to the work of Grebennikov and Bulja [4]. In fact, we discuss some significant examples, representative of the main research trends on DPAs, considering published journal papers from January 2011 to present.

The back-off efficiency enhancement issue can be approached with alternative strategies, like outphasing, bias modulation and envelope tracking.

The outphasing PA adopts two saturated, high efficiency amplifiers, fed with constant envelope signals, conveniently obtained from the input signal. Adopting the Chireix power combiner [5], signal amplification can be performed with high total efficiency, but it degrades the PA linearity. Recently, the outphasing amplifier has been progressed significantly [6].

The bias modulation technique, or the Kahn transmitter in its analog form [1], also adopts a saturated high efficiency PA, usually a switching current amplifier, driven by a constant envelope signal carrying the phase information of the input signal. The amplitude information is recovered by modulating the drain voltage of the PA with a linear envelope amplifier.

A more viable solution is the envelope tracking [1], [7], where a linear PA, driven with the amplitude modulated input signal, is adopted and the drain bias voltage tracks the envelope of the signal to minimize the power dissipation. Also in this case, when a large modulation bandwidth is required, the envelope amplifier becomes critical, and solutions need to be found to trade-off bandwidth and efficiency. Although the envelope tracking has become very popular for handset PAs, its employment as a class AB replacement for base stations is not straightforward due to the high power involved.

Considering this aspect, DPAs are often preferred because they can be effectively considered as class AB PA replacements. In fact, the other described techniques should refer to the whole transmitters rather than to the PA. In this context, they require a deep revision of the complete system architecture, with a strong impact on back compatibility and cost. Table I, reporting a comparison between DPA and other PA solutions in terms of the characteristics of their standard implementations, shows that one of the major concerns about DPA is its limited RF bandwidth. However, as discussed later in this paper, different solutions have been proposed to solve this issue. Also the other techniques have been revised to overcome their intrinsic limitations: for example, outphasing PAs can now achieve good average efficiency [6]. Other issues remain open, such as modulation bandwidth in high power outphasing and envelope tracking, and DPAs are still a preferred choice.

The importance of DPA for the microwave research community can be highlighted by the fact that, browsing the IEEE electronic library in the considered time span, among 1100 results on "microwave power amplifiers" and "RF power amplifiers", more than 100 relate to DPAs. What it is interesting to notice is that, along the years, the number of published papers on PAs and, in particular, DPAs, has constantly grown, following the spreading of high data rate mobile communications, see Fig. 1(a). Furthermore, the impact ratio between papers on DPA and total papers on PAs is constantly

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Type	Output Power	Average Efficiency	RF Band	Mod. Band
Class AB	High	Low	High	High
DPA	High	High	Low	High
Outphasing	High	Medium	Low	Low
Envelope tracking	Medium	High	High	Low
Bias modulation	Low	High	High	Low

TABLE I
DPA VS. OTHER PA IMPLEMENTATIONS: COMPARISON OF MAIN CHARACTERISTICS.

increasing, see Fig. 1(b).

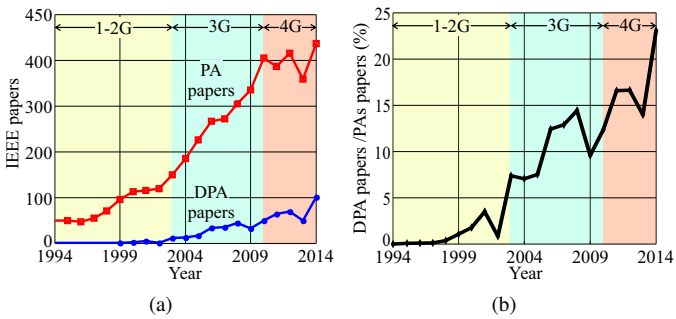

Fig. 1. Survey on IEEEXplore database: papers on PAs and DPAs vs. year (a), ratio between papers on DPAs and papers on PAs (b). Data on 2014 are extrapolated from the first 7 months.

A brief overview of the basics of DPA is given in Section II, describing its advantages and limitations. Section III explores the most important applications where DPAs play an important role, together with the device technologies exploited for their implementations. In the remaining Sections, the main research trends in DPA are accurately described and documented. In particular, Section IV shows the solutions adopted for DPA efficiency and linearity optimization for 6 dB and higher back-off. Section V introduces and analyses the bandwidth enlargement techniques, while Sections VI focuses on multi-band DPAs. The integrated solutions, i.e., Radio Frequency Integrated Circuit (RFIC) and Monolithic Microwave Integrated Circuit (MMIC) technologies, are described in Section VII. Finally, some conclusions are drawn in Sec. VIII.

II. Doherty concept

The DPA was firstly proposed by W. H. Doherty [2], for the amplification of amplitude modulated signals with vacuum tubes. For many years in the more recent solid state device era, high frequency power amplifiers dealt with constant envelope modulated signals, e.g., phase and frequency modulations, which represent the most suitable and simple choice for the maximization of PA power efficiency. In this framework, DPA architectures with their rather complex layouts did not attract particular attentions from the PA designers which preferred more conventional and simpler approaches. Things completely changed with the establishment of the new communication standards, whose high data rates require modulations with spectral efficiencies affordable only through mixed modulation techniques, i.e., acting on both amplitudes and phase/frequency. The new scenario forced a renewed interest on DPA idea starting in the '90s, where basestation market began to ask for linear microwave amplifiers adopting solid state technologies able to maintain high efficiency in presence of modulated signals with significant Peak-to-Average Power Ratio (PAPR) [1], [4], [8]. In fact, despite the efficiency of basestations based on class AB PAs is appropriate at maximum output power, it is significantly reduced when the output power level is decreased, i.e., the amplifier is working in back-off conditions. The DPA presents an inherent linearity that is suitable for handset applications, while first base-station DPAs needed feedforward linearization to overcome the intrinsic high distortion of solid state devices. Thanks to the introduction of digital predistortion techniques, feedforward has been gradually replaced, and DPA has become a suitable PA solution also for 3G and 4G systems. The combination of DPA and digital predistortion allows in fact to achieve, at the same time, high average efficiency and the required linearity. The DPA architecture, consisting of two PA stages, the main and the auxiliary, see Fig. 2, improves back-off efficiency thanks to load modulation.

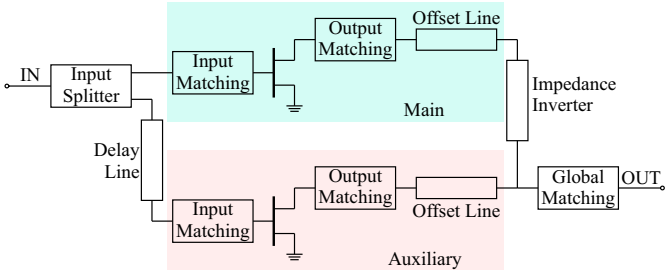

Fig. 2. Typical block scheme of a standard, 2-way DPA.

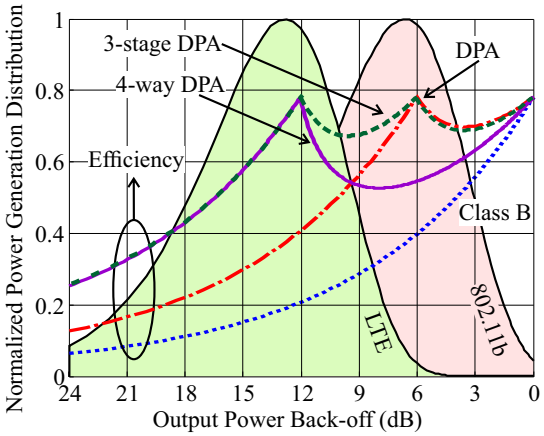

Fig. 3. Normalized efficiency of class B and Doherty PAs (standard, 4-way and 3-stage) vs. normalized output power, over-imposed to examples of normalized power distributions of modulated signals for wireless applications.

At low input power, the auxiliary is off, usually thanks to its class C bias point. In the case of Fig. 2, that refers to a two-way symmetrical DPA, the main amplifier, normally biased in class AB, works on a load that is $2R_{\mathrm{opt}}$ where R_{opt} is the optimum load for maximum output power. At 6 dB Output power Back-Off (OBO) from maximum power,

the main output voltage reaches its maximum swing, and it becomes maximally efficient. At the same time, the auxiliary starts injecting current into the DPA common node. Two effects can be observed when power increases: the output power increases of 3 dB because of the auxiliary current, while the load seen by the main amplifier decreases proportionally to the output power, reaching R_{opt} at saturation, and allowing a further 3 dB increase of the main output power while it remains at maximum efficiency.

The impedance inverter at the output of the main stage is necessary to guarantee the correct load modulation, and the phase difference that it introduces is recovered at the DPA input inserting a delay line. Main and auxiliary output matching networks present R_{opt} to the main and auxiliary devices at saturation, as in standard PAs.

The so-called offset lines [9], [10] can be inserted in the output section of the DPA, see Fig. 2. Their characteristic impedance is chosen equal to the load seen by the stage at saturation, in order not to affect the saturated DPA behaviour, but they are useful to optimize performance at lower power. In fact, for the main stage, the offset line length is tuned to provide a purely real $2R_{\mathrm{opt}}$ load at the device drain, a condition not generally satisfied with a simple matching network. The auxiliary stage offset line ensures instead that the turned-off auxiliary does not influence the load seen by the main stage. As a result, offset lines improve DPA performance, e.g., the gain flatness vs. output power, since they allow to optimize the load modulation.

The DPA ideal efficiency vs. is represented in Fig. 3. The ideal efficiencies of a 3-stage DPA, a 4-way DPA, and an ideal tuned load class B are also reported. The multi-way DPAs can be considered as DPAs where the auxiliary is a combined PA: on monolithic solutions, larger periphery is usually adopted for the auxiliary stage (asymmetrical devices) [4]. In Fig. 3, the power distributions (approximated with Rayleigh distributions [8]) of widely employed modulated signals for modern wireless communications are also represented. It can be clearly seen that the 2-way DPA advantages in terms of efficiency are maximized at 6 dB OBO, and are still significant for larger PAPR signals. Moreover, efficiency can be further increased introducing more sophisticated DPA solutions.

III. Applications and Technologies

The physical layer for the down- and up-link of mobile and wireless communications is spread on several frequency bands, at present almost all limited below 6 GHz. Fig. 4 reports the frequency occupation of the main mobile and wireless services. While the GSM bands stand below 2 GHz, from the third generation of mobile networks the trend has been to occupy also higher frequencies. UMTS widely uses the 2.14 GHz band, while the fourth mobile generation, i.e., LTE and WiMAX, also extends to higher frequencies. Wireless Local Area Networks (LANs), mainly represented by the WiFi protocol, are developed on the ISM 2.4 GHz band and on higher frequencies, including 5.5 GHz band. Regarding power levels, WiFi systems are strongly limited around few watts. Mobile base stations need power levels up to hundreds of watt, while the user terminals are limited to below one watt.

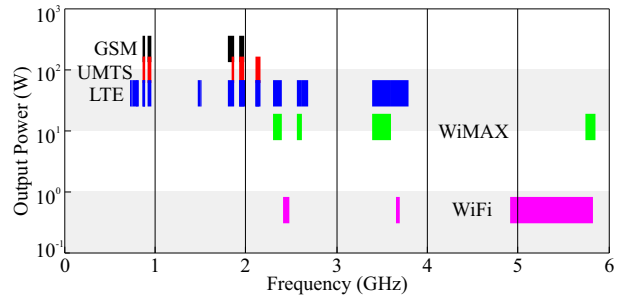

Fig. 4. Frequency bands up to 6 GHz and output power levels for the main mobile (downlink channel) and wireless services.

The usage of higher frequencies for the radio channel access is limited by several factors, among which the necessity of eyesight connection that would impede users' mobility, and by the increasing cost of high frequency electronics. However, 60 GHz wireless LAN are under development for small environments, for example inside building communications. Moreover, high frequency radio links are widely adopted for the implementation of the mobile infrastructure, where the communicating devices are fixed in space, and high gain antenna can be employed. An important example is the backhaul [11], i.e., the connection of the basestations to the core of the network, that is expected to be deeply revised in the next few years due to the increasing need of capacity. In fact, the implementation of backhaul through microwave point-to-point radio links working from few GHz to mm-wave frequencies, will cover an important market share for microwave electronic manufactures. The power levels are, in this case, in the range from few watts to some tens of watt. Regarding future development, the usage of mm-wave carrier for 5-th generation mobile networks is under consideration, due to GHz signal bandwidth required and the availability of spectrum resources.

The frequency of operation and the power level are the main factors influencing the choice of the semiconductor technology for the design of power devices and amplifiers. When more solutions are available, cost, power, efficiency and linearity become the deciding factors.

For base-stations, LDMOS and GaN HEMT devices are popularly used due to their characteristics of high breakdown voltage and power density. The LDMOS is a low cost, silicon based device that demonstrates very high reliability and very good linearity behaviour. The GaN HEMT provides higher efficiency, in particular on SiC substrate, but it is a more expensive solution. The bias voltage is similar between the two technologies (28, 40, 50 V drain bias options are commercially available), resulting in a comparable optimum real load. However, the intrinsic properties of GaN devices permit higher frequency operation and larger bandwidth [12] thanks to the reduced capacitive effects. Outstanding performance in terms of output power and back-off efficiency have been already demonstrated with GaN-based high power DPAs [13]–[15], and it has to be noticed that almost all the broadband DPA prototypes presented in this review are based on GaN transistors, see Sec. V.

HBT devices are preferred for handset application for about 1 W level PAs with drain voltage below 4.5 V, due to the reliable, low cost technology process.

CMOS-based DPAs have also been actively researched due to flexibility and co-integration capability with baseband block. However, with respect to HBT DPAs, they exhibit inferior performance, because of CMOS drawbacks such as low breakdown, no via holes and low power density.

Finally, GaAs pHEMTs are good candidates to develop medium/high power, millimeter wave PAs above 20 GHz, where also GaN transistors, at least at research level, are starting to be investigated. From the DPA design point of view, the characteristics that favorably place GaN with respect to GaAs are related to impedance levels, allowing for wideband matching and reduced losses. Moreover, thanks to the higher power density, the need of complex combiners is reduced, enabling the implementation of advanced topologies like the DPA [16].

Ref.	Freq. (GHz)	Tech.	P_{SAT} (dBm)	OBO (dB)	Eff. (%)
[20]	2.14	Si LDMOS	50.5	10.5	35
[21]	1.85	GaAs HBT	30	6,10	37,31
[22]	2.6	GaN HEMT	41.9	7, 12, 17	62
[23]	2.655	GaN HEMT	51.7	8.1	60.5
[17]	2.14	Si LDMOS	53	6	50
[24]	0.87	Mixed	51	6, 8, 10	61, 56, 51
[25]	10	GaN HEMT	49.8	7.8	49
[26]	10	GaAs pHEMT	29	6	43
[27]	2.01	Si LDMOS	42.5	6	33
[28]	2.14	GaAs pHEMT	31.6	6	53
[29]	3.5	GaN HEMT	49.5	6	46
[30]	1.8	GaN HEMT	31	7	31
[31]	2.1	GaN HEMT	42	6	48
[32]	1.88	GaAs HBT	33.5	6	44

TABLE II
PERFORMANCE COMPARISON BETWEEN DPAS FOR EFFICIENCY/LINEARITY ENHANCEMENT.

IV. EFFICIENCY AND LINEARITY MAXIMIZATION

DPA standard implementations have limitations on linearity and achievable average efficiency, that can be ascribed to the intrinsic DPA nature and to other problems related to the device non-idealities. Digital predistortion is practically always employed to comply with the communication system linearity specifications. To reduce the complexity of the predistorters and to enhance the overall system performance, techniques for the reduction of amplitude and phase distortion, as well as memory effects, are often matter of scientific contributions. The works of [3], [17] focus on distortion compensation at high power level, optimizing bias and devices' size. In [18], [19] the relationship between load modulation and phase distortion in DPAs is analyzed following different approaches.

Regarding the efficiency, the request of its further enhancement can be easily understood given the importance of power consumption reduction. Table II reports the list of the papers referenced in this section, with an indication of employed technology, frequency target, output power, target OBO and OBO efficiency. More details on the design strategies can be found in the following subsections. It is important to notice that all the proposed techniques never consider efficiency or linearity independently. In fact, every approach that allows for efficiency improvement usually implies an added complexity, and a very accurate input splitting design, bias selection and phase synchronization between the stages to avoid detrimental non-linear effects like strong saturation. A last remark on the fact that digital signal processing is often employed to adaptively adjust these parameters.

A. Back-off extension

An intrinsic limitation of the standard 2-way DPA is given by the fact that the first maximum efficiency peak is at 6 dB OBO. However, in most of modern communication systems the PAPR exceeds this value, hence asking for an extension of the high efficiency range. Multi-way and multi-stage DPAs are two viable solutions to increase the high efficiency back-off region. According to the classification used in [4], a N-way DPA is realized by parallelizing N-1 auxiliary stages that turn on simultaneously (see Fig. 5-left for a 4-way DPA), obtaining an equivalent asymmetrical DPA operation. By increasing N and properly optimizing power splitting and bias, the first efficiency peak can be extended beyond 6 dB. Fig. 3 shows the efficiency curve for a 4-way DPA, optimized for 12 dB OBO first efficiency peak: it can be noticed that the efficiency curve drops significantly in the Doherty region. The N-stage DPA can overcome this issue. It has N-1 auxiliary amplifiers, see the block scheme of Fig. 5-right for the 3-stage case, which are turned on at different power levels, coinciding with the efficiency peaks. The efficiency drop in the power region between peaks is significantly attenuated, (see Fig. 3 for an asymmetrical 3-stage DPA case), when devices' size and input splitting ratio are properly dimensioned.

On the other hand, the main amplifier of a 3-stage DPA can be pushed into a strong saturated region, thus requiring proper device size selection and ad-hoc design solutions. Very interesting 3-stage DPA approaches were proposed by works presented before the time-range considered in this review. A state of the art WCDMA DPA is shown in [33], where three separated input drives for the main and the two auxiliaries are used. In [14], gate bias adaptation technique is applied, improving the linearity of the stage.

The work of [20] implements a 2.14 GHz 3-stage inverted DPA in LDMOS technology, using different sizes for the main and the two auxiliary stages, in order to optimize the back-off efficiency. The designed DPA delivers 50.5 dBm of maximum output power while, at 10.5 dB OBO with a WCDMA signal, it maintains a drain efficiency of 35% with 9.5 dB gain.

A different case is analyzed in [21], where the focus is on a hardware that needs to operate in two modes, high power mode employing a Doherty, and low power mode, where a switched load is used to enhance the efficiency at 10 dB back-off. The DPA, which includes a driver stage, is developed at 1.85 GHz on InGaP/GaAs HBT technology for the power stage.

A multi-mode DPA is also exploited in [22]: in this pa-

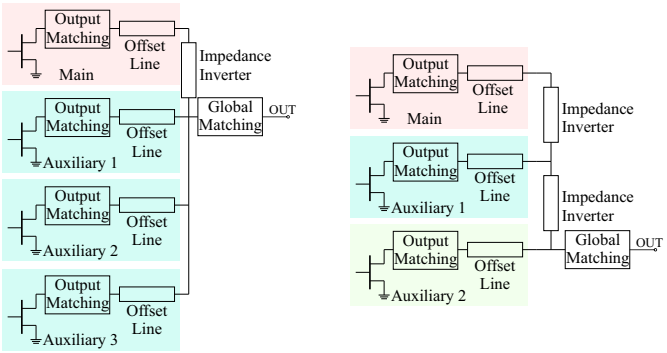

Fig. 5. Output combiner sections of a 4-way asymmetrical DPA (left), and of a 3-stage DPA (right).

per, the best efficiency OBO is set through Micro Electro-Mechanical Switch (MEMS)-based reconfigurable matching networks (located at the output combiner and at the main branch input), and auxiliary stage bias adjustment. The design is carried out at 2.6 GHz, employing GaN HEMT devices; the saturated output power is 41.9 dBm, while at average power levels of 35, 30 and 25 dBm, set according to the selected configuration, the PAE remains higher than 62%.

In [23], a new output combiner is developed, allowing for an easier matching of the auxiliary device. The hardware works at 2.665 GHz, is based on GaN HEMT devices from CREE, and is able to deliver at saturation an output power of 51.7 dBm. When measured with WiMAX signals with 8.3 dB PAPR, the DPA exhibits 43.6 dBm of output power, together with average efficiency higher than 60%.

B. Asymmetrical devices and splitting

Another important source of investigation in literature is the proper dimensioning and turning on of the auxiliary stage. In fact, for an ideal behaviour of the DPA, either the auxiliary device should be roughly double-sized with respect to the main (asymmetrical devices), or the input power splitting should be asymmetrical, giving more power to the auxiliary branch [34]. The adoption of asymmetrical input splitting is widely adopted in hybrid solutions using packaged or die transistors, and is well established in commercial products. In fact, at least in principle, this technique permits to build a DPA starting from two identical power amplifiers, focusing on the design of offset lines, impedance inverter and input splitter. The asymmetrical devices solution is favorable in monolithic implementations, thanks to the flexibility in device size selection. However, different devices' size can be used also with packaged transistors, with the limitation to choose among a small basket of peripheries.

In [17], the adoption of an auxiliary device larger than the corresponding main is carefully analyzed, in particular focusing on the derived advantages: improved load modulation, well-timed turn-on effect, effective nonlinear distortion cancellation, and simple topology. As case studies, two DPAs, optimized respectively for linearity and efficiency, were fabricated and measured for 2.14 GHz, 4-carrier WCDMA operation, employing LDMOS devices. The achieved output power is around 53 dBm. If compared to a standard DPA implementation, the modified structures have better linearity, roughly 1 dB higher output power and, in the case optimized for efficiency, around 5% higher efficiency.

In [24], a DPA realized with a LDMOS main and a GaN auxiliary is presented: thanks also to the asymmetrical voltage bias, the device power utilization factor [35] is maximized. The position of the first efficiency peak can be set at 6, 8 and 10 dB of OBO by proper bias tuning.

C. Output combiner optimization

A great effort has been given to the optimization, modification and revision of the output combiner of the 2-way DPA. In the works of [25], [26] the Doherty load modulation is revised to account for the variation of knee voltage for different currents, due to the on-resistance of the device. They exploit an OBO main load larger than $2R_{\mathrm{opt}}$, with a consequent efficiency improvement at back-off, see Fig. 6. The hardware

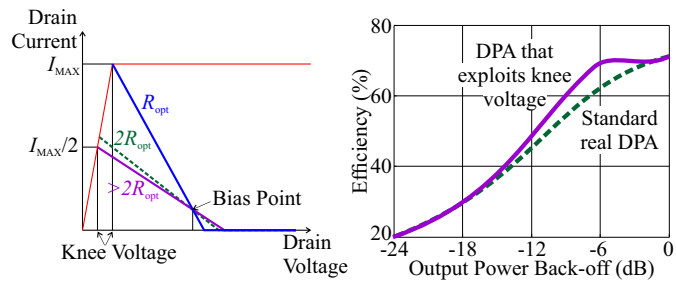

Fig. 6. Larger back-off impedance for efficiency maximization [25], [26]. Dynamic load lines of the main device at saturation and back-off (left). Typical efficiency improvement (right).

proposed in [25], based on GaN CREE devices, yields almost 50 dBm of output power. Instead, the DPA of [26] is developed at X-band on GaAs MMIC, and it achieves 29 dBm of output power.

The solution of [27] substitutes the standard DPA impedance inverter with a coupled-line loaded with a capacitor. This solution helps harmonic suppression, and the intermodulation distortion can be reduced by 23 dB, with respect to a standard DPA, by proper tuning of this new structure. The design example is developed with LDMOS devices at 2.01 GHz, with maximum output power of 42.5 dBm and 6 dB OBO efficiency around 33%.

In [28], the output matching network (impedance inverter and global matching to 50 Ω) is adjusted to correct the current unbalance between the main and the auxiliary branches. A theoretical analysis is provided and the results prove the effectiveness of the solution. In fact, 13% higher back-off efficiency with respect to standard DPA is demonstrated by a prototype developed on GaAs pHEMT at 2.14 GHz, with 31.6 dBm of output power.

The design of [29] combines several of the previously cited techniques in order to maximize the back-off efficiency. In particular, it modifies the output combiner for asymmetrical device sizes, using stepped impedance networks. The prototype is conceived for large instantaneous bandwidth signal (100 MHz LTE), for 3.5 GHz operation. The DPA is realized

with GaN HEMT devices, and it achieves 49.5 dBm of output power with 6 dB OBO efficiency larger than 46%.

D. Other techniques

Deeper variations to the DPA structure are proposed in [30] and [31]. In [30], the DPA load is connected in series [2], [4] allowing for more favorable impedance transformations. Input and output baluns are needed for the differential-to-common mode transition. A distortion reduction method, that can also be applied to shunt-type Doherty, is analytically derived and proved. It works by reducing the phase and gain deviations between the main and auxiliary branches through proper bias tuning. A prototype is developed at 1.8 GHz, employing GaN HEMTs. The maximum power is around 31 dBm, while at 24 dBm the Power Added Efficiency (PAE) is 31%.

In [31], a branch line coupler replaces the standard DPA output combiner. With this solution, similar results with respect to a standard DPA can be achieved, but the impedance level are far more favourable, especially for high power operation. The prototype is developed at 2.1 GHz employing GaN HEMTs. The maximum output power is 42 dBm, while at 6 dB OBO an efficiency of 48% is obtained.

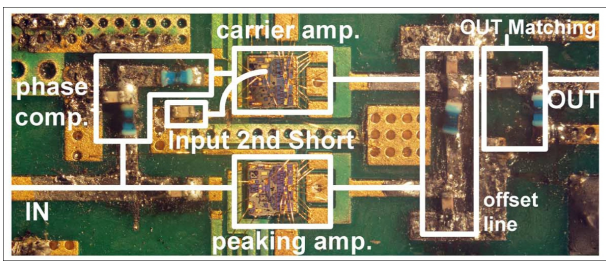

Fig. 7. Picture of the DPA presented in [32].

Finally, the work of [32] focuses on the compensation of non-idealities arising in HBT Doherty implementations, in particular due to the non-linear behaviour of the collector-base capacitance C_{bc}. Class F harmonic closure is used for back-off efficiency optimization. A prototype has been realized, see Fig. 7, and it delivers 33.5 dBm of output power at 1.88 GHz.

V. Bandwidth enhancement

Several factors limit the bandwidth of a DPA. In fact, while for a combined PA the broadband design can be actually seen as a broadband matching problem, in DPAs the situation is more complicated. The added complexity is related to the need of a correct load modulation, that requires different impedances at different power levels. In particular, the DPA impedance inverter, the offset lines, and the phase synchronization at the output common node can be seen as the typical DPA bandwidth limiting factors. The impedance inverter is usually realized by means of a quarter-wave length transmission line, that is intrinsically narrowband. Some of the referenced works in this section present new realizations of the impedance inverter, able to extend its bandwidth. The offset lines are well defined for single frequency operation: a solution often adopted in the cited papers is to embed the offset line within the output matching network, thus reducing the overall quality-factor of the filter. An optimal load modulation over a large frequency band, achievable with good phase synchronization between main and auxiliary, can be obtained through a revision of the DPA basic structure, as it happens in the so-called digital DPA, where the signal between the main and auxiliary stages is split at baseband.

A comprehensive analysis of the bandwidth limitations given by the output section of DPAs is discussed in [36]. Other factors limiting the bandwidth can be related to the adoption of harmonic terminations, that are usually realized by means of resonant elements, intrinsically narrowband.

Table III reports the list of the paper referenced in this section. It gives indication of the employed technology, center frequency, fractional bandwidth (BW), moreover reporting the minimum saturated output power, and OBO efficiency on the declared bandwidth. The considered OBO is also reported. More details on the design strategies can be found in the following subsections.

Ref.	Tech.	Freq. (GHz)	BW (%)	P_{SAT} (dBm)	OBO (dB)	Eff. (%)
[37]	InGaP/GaAs HBT	1.83	27	35	7.5	30
[38]	GaN HEMT	3.3	18	43	6	38
[39]	GaN HEMT	0.85	35	50	6	52
[36]	GaN HEMT	2.6	31	39.5	5, 6	40
[40]	GaN HEMT	0.85	30	43	9	49
[41]	GaN HEMT	0.776	21	49.3	6	43
[42]	GaN HEMT	0.98	41	40.2	6	30
[43]	GaN HEMT	2.2	22	42	6, 7	40
[44]	GaN HEMT	2	41	42	6	42
[45]	GaN HEMT	1.73	115	43.1	6	45

TABLE III
Performance comparison between DPAs for bandwidth extension.

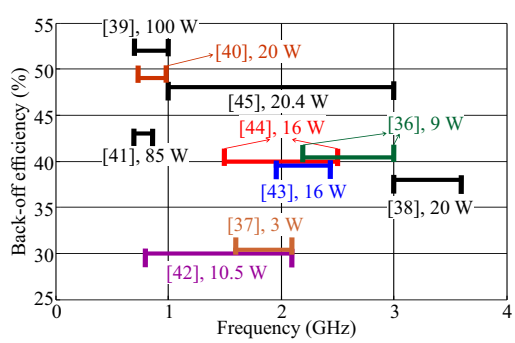

Fig. 8. Bandwidth enhancement DPAs. Minimum in-band back-off efficiency vs. frequency. Saturated output power indicated in legend.

A. Matching networks optimization

The correct load modulation is a defining characteristic of the DPAs, but at the same time is the feature that mostly affects their bandwidth. For this reason, many papers have been devoted to the optimization of the output section of the DPA, in order to guarantee high back-off efficiency on large

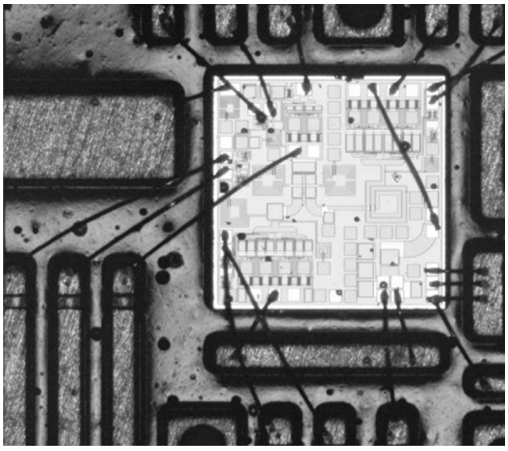

Fig. 9. Picture of the LTE DPA presented in [37].

bandwidth. The technique proposed in [37] improves DPA bandwidth by integrating the functions of matching, offset lines and impedance inverter blocks in a single, simpler matching network. A similar approach is adopted for all the other DPA structures. The design example is carried out for handset applications, using a HBT process on InGaP/GaAs, see Fig. 9. The DPA is tested with a LTE signal with 7.5 dB PAPR and 10 MHz bandwidth: in the 1.6-2.1 GHz band the PA exhibits, at the average power of 27.5 dBm average efficiency higher than 30%, however complying with the standard emission masks. The approach followed in [38] is based on wideband

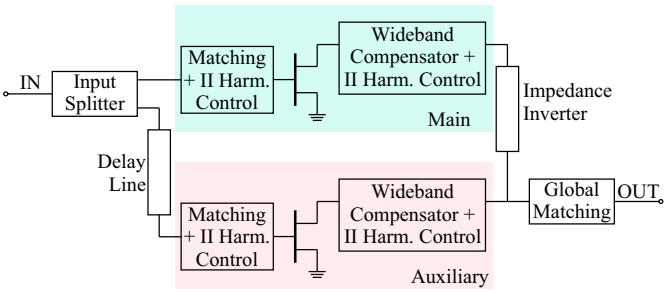

Fig. 10. Block scheme of the wideband DPA presented in [38].

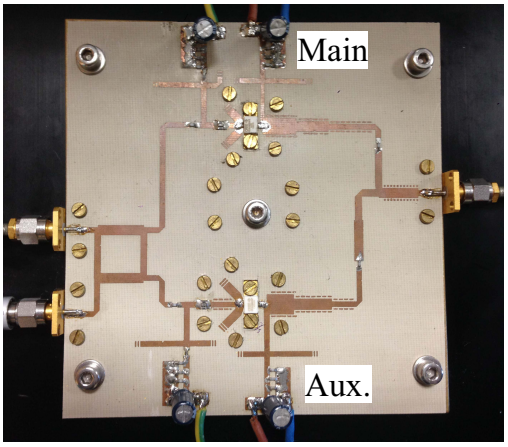

Fig. 11. Picture of a 20 W GaN-based 3-3.6 GHz DPA described in [38].

compensator networks, that cancel, on the band of interest, the reactive effects of the devices, see block scheme in Fig. 10. Moreover, second harmonic tuning is exploited at back-off for the higher frequencies of the band, in order to obtain flat power and efficiency. The DPA is fabricated using CREE 10 W GaN HEMTs, see Fig. 11, and it shows, in the 3-3.6 GHz band, an output power exceeding 43 dBm, and a 6 dB OBO efficiency larger than 38%.

In [39], the authors expand the bandwidth of the classical DPA by using a quasi-lumped quarter-wave transmission line and the Klopfenstein taper [46]. However, this DPA requires different drain supply voltages for the main and auxiliary transistors. The implemented Doherty PA delivers very good performance at high power (saturated output power of 50 dBm), with minimum 6 dB back-off efficiency of 52% over a fractional bandwidth of 35%.

In [36], the broadband matching is achieved following a simplified real frequency technique [47], to obtain the desired frequency-dependent optimum impedances. Two prototypes are realized with CREE GaN HEMTs. The sample achieving larger bandwidth shows an output power in excess of 39.5 dBm, with 6 dB OBO efficiency higher than 40%, on the 2.2-3 GHz band.

A combination of bandwidth and OBO enhancement is achieved in [40], thanks to proper cancellation/absorption of the device output capacitances in a three-way DPA. To fabricate the prototype, a 10 W CREE GaN device is used for the main stage, while two 25 W CREE GaN devices are used for the auxiliary branches.

The focus of the DPA presented in [41] is on the optimization of the instantaneous bandwidth, in order to adopt 100 MHz LTE signals. To this aim, the drain bias networks are designed to minimize electrical memory effects, employing ad-hoc LC resonators. An integrated Doherty combiner is used (RDO750A03 from RN2 Technologies co.), and its impact on the bandwidth is compensated by broadband output matching networks, designed applying a simplified real-frequency technique. The prototype, realized with CREE 60 W GaN transistors, shows a considerable improvement of ACLR (4 dB) and ACLR asymmetry (3 dB), with respect to the same DPA adopting conventional bias networks.

A completely different solution is used in [42]: in this design, the impedance inverter is removed, but still good results in terms of back-off PAE are achieved thanks to an appropriate matching. Despite it may be questionable if this PA can still be considered a Doherty, the measured results on the prototype are very good: on the 0.8-1.2 GHz band, the output power is higher than 40.2 dBm, with 6 dB OBO efficiency higher than 30%. The DPA is realized with 10 W CREE GaN devices.

B. Digital DPA

The introduction of digital DPAs opens new degrees of freedom in the Doherty design. According to this strategy, main and auxiliary stages are independently driven from baseband, see Fig. 12. Proper digital signal conditioning, applied to the two branches, accounts for the output section bandwidth

limitations. On the other hand, the utilization of separated baseband processing and up-conversion process asks for a re-definition of the transmitter: in this case, the pros and cons with respect to a standard solution must be carefully evaluated.

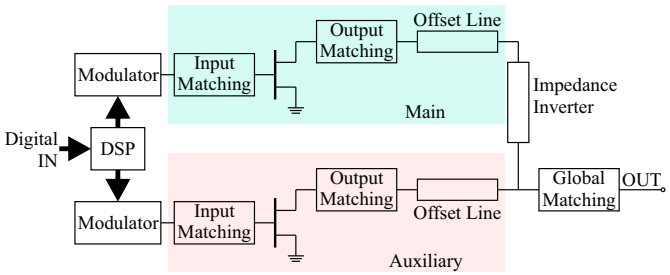

Fig. 12. Block scheme of the digital DPA.

The work of [43] is based on a careful analytical comparison between conventional and digital DPA. It is shown that the bandwidth can be increased of a 2.8 factor. The proposed prototype adopts 10 W GaN CREE devices, and shows an output power greater than 42 dBm with 6 dB OBO efficiency larger than 40% over the 1.96-2.44 GHz bandwidth.

The work of [44] introduces a modification in the digital Doherty approach through a novel output combiner with better bandwidth characteristics. Moreover, the proper drain bias setting of the main device allows to configure the desired OBO at 6, 8, and 10 dB. The prototype, based on 15 W GaN CREE devices, reaches 42 dBm of output power between 1.5 and 2.5 GHz, with 6 dB OBO efficiency larger than 40%.

A more extensive analysis on digital DPA operation is performed in [45]: a continuum between Doherty and Outphasing harmonic loading conditions of the devices is demonstrated under ideal conditions studying a dual-digitally driven DPA. For the actual implementation, a combiner assuming non-ideal harmonic closure is analyzed and designed, showing possible good efficiency level. Then, it is exploited for the realization of an over 100% fractional bandwidth DPA. The prototype adopts 15 W GaN CREE HEMTs, and on the 1-3 GHz band shows an output power higher than 43.1 dBm, with 6 dB OBO efficiency higher than 48%.

VI. Multi-band solutions

The increasing number of available frequencies for mobile communications requires to design multi-band RF front-ends. Multi-band designs can take advantage of discrete frequencies matching solutions, with potential better performances than wideband DPAs used to cover more frequencies. In some cases, multi-band hardware is used for concurrent operation: two or more modulated signals at different carrier frequencies can fed simultaneously the DPA, with consequent increased PAPR of the total signal and the need of ad-hoc predistortion techniques. In fact, with concurrent signals, both intermodulation and cross-modulation must be considered. In other cases, the multi-band DPA is useful for a reconfigurable transmitter that works on different frequencies at different time slots.

Different approaches are also followed in the practical realization of the multi-band filters. In some cases, a real multi-band approach is followed, by using multi-resonant structures that provide narrowband matching around a discrete number of frequencies. In other examples, a wideband approach is followed for filter design, but the hardware is used at discrete points. The wideband approach has advantages in terms of design robustness, because it is intrinsically less resonant, and provides more flexibility. On the other hand, if the separation between the bands is very large, the wideband approach becomes unfeasible, due to the bandwidth limitations of the DPA, while ad-hoc multi-band filters can be designed to cover the specific bands.

Table IV reports a list of the multi-band DPAs presented in this Section, summarizing their performance. It reports frequency bands, output power and OBO efficiency, together with the considered OBO. More details on the design strategies adopted in every paper are described in the following. It has to be noticed that most of the DPAs illustrated in this section are fabricated adopting GaN HEMT devices.

Ref.	Freq. (GHz)	P_{SAT} (dBm)	OBO (dB)	Eff. (%)
[48]	0.88/1.96	41/40	6	36/35
[49]	1.96/3.5	43/42	6.5	40/30
[50][1]	1.5/2.1/2.65	46/43/42	6	60/50/38
[50][2]	0.95/1.5/2.1/2.65	44/44.5/42/42	6	58/49/49/32
[51]	2.14/2.655	43.5/43.2	6.5	40/45
[52]	1.85/2.15/2.65	44/44/44	6	58/50/42
[53]	0.9/2.31	46/45.5	9	61/44
[54]	0.85/2.33	44/42.5	6	50/42
[55]	1.9/2.14/2.6	41.5/40.5/40	6	60

TABLE IV
Performance comparison between multi-band DPAs.

In the work of [48], two dual-band DPAs are developed. The design is carried out by using dual-band input splitter, offset lines, and impedance inverter, realized employing T-shaped networks and coupled lines. The two DPAs have frequency dependent OBO, equal in one case, and unbalanced in the other, in order to evaluate the differences between the two approaches. The DPA is fabricated adopting SiC MESFET devices by CREE for the WCDMA bands of 880 MHz and 1960 MHz. The comparison between balanced and unbalanced DPAs did not show significant differences. Concurrent, 2-dimensional predistortion [56] is successfully applied to linearize the DPA under two-tone excitation.

Always mainly focusing on the output section of the DPA, the GaN-based prototype of [49] presents the analysis and design of dual-band offset lines for dual-band DPA performance improvement.

Tri- and quad-band DPAs are developed in [50] where the theoretical study and practical implementation of multi-band impedance inverter are described. In this case the two DPAs, realized with GaN HEMT devices, show the typical Doherty behaviour for all the design frequencies, i.e., 1.5, 2.1 and 2.65 GHz in the tri-band case, and 0.95, 1.5, 2.1 and 2.65 GHz for the quad-band case.

The DPA of [51] is designed adopting a revised Doherty output section. In particular, the global output matching is removed, and the DPA is directly loaded with 50 Ω. Moreover, the auxiliary is not directly connected to the common load, but it employs two quarter-wave length sections for the power matching. The devices are matched with a broadband class-E reactance compensation [57]. The resulting structures can be actually considered as wideband, but the goal of the design is the operation at two discrete frequencies, 2.14 and 2.655 GHz. Two 10 W GaN CREE devices are used for the fabrication of the DPA. In [52], the same broadband class-E amplifier is used as a building block also for a tri-band DPA. A detailed description of the output combiner design is provided, with a discussion on the broadband strategy adopted.

While the previous works are mainly focused on the output section design, the DPAs of [53], [54] point out the importance of the frequency dependence of the input power splitting to compensate for the device gain decrease vs. frequency and to correct the auxiliary device turning on. In [53] a three-way dual-band DPA is shown, employing GaN HEMTs. Efficiencies at 9 dB OBO of 61% and 44% are achieved at 0.9 and 2.31 GHz, respectively, with saturated output power around 46 dBm. In [54], an asymmetrical two-way DPA is presented with 10 W GaN CREE devices, showing at 0.85 and 2.33 GHz an output power of 44 and 42.5 dBm and 6 dB OBO efficiency of 50% and 42%, respectively.

A reconfigurable approach is followed instead in [55], where multi-band operation relies on MEMS reconfigurable structures, located at the output combiner and at the main branch input. The tunable elements realize tunable loaded transmission lines through single-pole, double-throw switches. The prototype is a tri-band DPA, with bands at 1.9, 2.14, and 2.6 GHz, where the output power is of 41.5, 40.5, and 40 dBm, respectively. It has to be noticed that, at 6 dB OBO, the efficiency is above 60% for all the three configurations.

VII. Integrated implementation

Integrated implementations of DPAs include Silicon-based RFICs and compound semiconductor MMICs. Integrated solutions are feasible for low frequency, low power applications (handset) and for high frequency solutions (backhaul, 5G), with low, medium power levels. The selection between RFIC and MMIC is driven by many factors. CMOS is less linear, less efficient and requires more complicated structures than compound technology to achieve watt-level power levels. On the other hand, it has big cost advantages for high volume production, and is more keen to a mixed-signal integration. This also allows to embed on-chip the advanced controls required for bias and power splitting ratio. For both technology families, the DPA implementation poses specific challenges.

Among the papers presented in the previous sections, the DPAs of [21], [26], [32], [37] are integrated, but they have been inserted there since focused on particular techniques for performance enhancement. In this section, DPAs with special features specifically conceived for integration are instead referenced. Table V reports a resume of the referenced papers, with main technology and performance information.

Ref.	Freq. (GHz)	Tech./F.I.	P_{SAT} (dBm)	OBO (dB)	Eff. (%)	Size (mm^2)
[58]	2.4	Si CMOS/Y	26.3	6	25	1.88
[59]	1.75	Si CMOS/Y	28.6	6	25	2.42
[60]	1.9	Si CMOS/Y	28	12	19.7	2.94
[61]	2.4	Si CMOS/Y	31.9	12	25	2
[62]	45	SOI CMOS/Y	28.5	6	26	0.45
[63]	0.75	GaAs HBT/N	38.8	10	37	6.28
[64]	1.88	GaAs HBT/Y	28	9	25.1	1.2
[65]	7	GaN HEMT/Y	35.5	9	42	3.15
[66]	7	GaN HEMT/Y	37	7	47	21.6
[67]	7	GaN HEMT/Y	38	7	42	21.6
[68]	2.14	GaN HEMT/N	40.5	7.3	51	8.58
[69]	2.14	GaN HEMT/N	41.2	4.7	43	6.75

TABLE V
Performance comparison between integrated DPAs. Tech./F.I. column indicates the technology and if the DPA is fully integrated.

A. Silicon technology

The employment of RFIC on CMOS technology is quite common for the realization of chipsets for mobile equipment, see [70], where power levels are not too high. To overcome some issues related to the unavailability of via holes and high losses in Si CMOS substrates, the use of differential DPAs with transformer-based matching is a convenient choice, see the block scheme of Fig. 13. In this case, the DPA should be considered as a voltage- instead of current-combiner. For

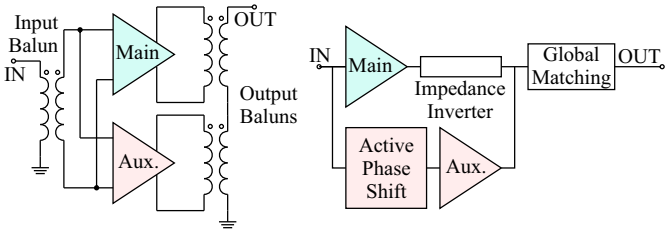

Fig. 13. Simplified scheme of a series, transformer based DPA, typically adopted in CMOS technology (left). Block scheme of the active phase shift DPA adopted in [62] (right).

example, the DPA of [58] is developed on a 90 nm CMOS process for 2.4 GHz applications. It adopts a series combining transformer allowing for chip implementation of an asymmetrical DPA. In fact, it uses different sizes for main and auxiliary stages, and optimizes the behavior thanks to a properly unbalanced output transformer. The total chip size is 1.88 mm×1 mm.

The DPA of [59] is based on 180 nm CMOS technology, for 1.75 GHz applications. It adopts an output voltage transformer instead of conventionally combining the output currents. The input balun is realized on an external board, while the core active part of the DPA and the output transformers are integrated on two different chips, with 0.79 mm×1.46 mm and 0.79 mm×1.6 mm size, respectively.

A further enhanced structure is proposed in [60] using 40 nm CMOS technology for 1.9 GHz LTE applications. A

hybrid series-combining transformer consisting of two Distributed Active Transformers (DATs) ensures high efficiency even when only one of the four amplifiers is active. Both main and auxiliary DAT are composed by two PAs. The system, which achieves a saturated output power of 28 dBm, operates in high-power (HP) and low-power (LP) modes. The measured PAE if of 25.5% and 19.7% at 6 dB and 12 dB back-off, respectively. The total chip size is 2.1 mm×1.4 mm.

A DPA using a variable balun transformer as impedance inverter is analyzed in [61]: it achieves load modulation without any phase delay circuit, thus reducing the total chip area. Additionally, adaptive bias control of the auxiliary stage assists the load modulation, resulting in an improved back-off efficiency. The DPA, based on 130 nm CMOS technology for 2.4 GHz, delivers an output power of 31.9 dBm, while it keeps the efficiency above 25% over a 12 dB OBO range.

At mm-waves frequencies, the use of Si integrated technology can lead to great advantages in terms of mass production cost. The work of [62] is developed on 45 nm SOI CMOS, for 45 GHz applications (both radar and communications). Several features are used in this design for performance maximization: the main and auxiliary are realized by stacked devices to improve the output power without compromising the impedance level. In one prototype, the main stage input phase delay, usually realized by means of a transmission line, is substituted by a driver-amplifier stage, that allows gain improvement. In another DPA realization the use of slow-wave coplanar waveguide [71] helps improving both PAE and gain. The achieved output power is 28.5 dBm with 6 dB OBO efficiency of 26% for the active phase shift DPA, that shows a size of 0.5 mm×0.9 mm.

B. Compound technology

For achieving high power or frequency, compound semiconductor technology can be used instead of silicon. The DPA of [63] shows a Doherty implemented in low-voltage GaAs HBT technology, for 750 MHz. The integrated part which includes pre-driver, driver, and main and auxiliary devices, has a size of 2.36 mm×2.66 mm. The DPA impedance inverter is realized as Π-type CLC network, with integrated MIM capacitors and external bond-wires working as inductors. However, external impedance matching is still needed since the common node impedance is rather low (0.7 Ω). The presented measurements, that also include the output matching losses, show a saturated output power higher than 39 dBm on the 728-756 MHz band. On the same band, the PAE at 10 dB OBO is higher than 25%.

A fully integrated series-type extended Doherty amplifier was proposed in [64]. To apply it to a W-CDMA handset transmitter, all circuits are compactly implemented on a single InGaP/GaAs HBT MMIC. The DPA achieves 26 dBm peak output power, while the PAE is kept above 25.1% over a 9 dB range of output power.

The DPAs presented in [65]–[67] adopt the same TriQuint 0.25 μm GaN on SiC MMIC process, and have been conceived for 7 GHz microwave backhauls. In the first two cases, an asymmetrical DPA architecture is adopted, with 4×100 μm and 10×100 μm device sizes for the main and the auxiliary, respectively. In [65], the focus of the design is on bandwidth enhancement and size reduction. The PAE at 9 dB OBO is higher than 30% from 6.7 to 7.8 GHz with a delivered output power higher than 34.5 dBm. The MMIC size is 2.1 mm×1.5 mm. The DPA of [66] is thought for back-off efficiency enhancement and maximum power utilization. The layout, whose microscope picture is shown in Fig. 14, has a size of 4.6 mm×4.7 mm. The delivered output power at 7 GHz is larger than 37 dBm, and the 7 dB OBO efficiency is of 47%. To achieve a good fractional bandwidth, the DPA of [67]

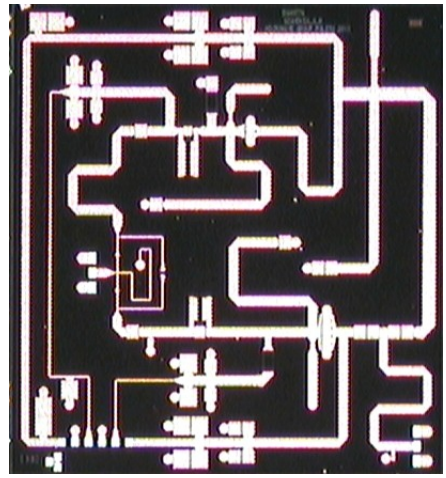

Fig. 14. Picture of the GaN MMIC DPA for 7 GHz backhaul presented in [66]. Size of 4.6 mm×4.7 mm.

adopts a driver on the auxiliary branch, and a coupled line as input power splitter. The achieved maximum power is 38 dBm, with a 7 dB back-off efficiency of 42%. The occupied area is 4.6 mm×4.7 mm.

The design of [68] is realized on TriQuint 0.25 μm GaN on SiC MMIC, for 2.14 GHz small cell base-stations. The DPA delivers 40.5 dBm of saturated output power, while at 7.3 dB of OBO the efficiency is still higher than 50%. For loss reduction, two strategies have been followed: on one side, the core components of the DPA are integrated with semi-lumped topology minimizing the parts count. On the other hand, the high value inductors needed for bias and at input splitter are realized through external, high-Q chip inductors. Similarly to the approach followed in [66], the auxiliary device has larger size (22×200 μm) with respect to the main (16×200 μm), while more power is delivered by the input splitter to the main stage, for gain and back-off efficiency improvement. Fig. 15 shows a microscope picture of the realized DPA (size 3.3 mm×2.6 mm), with the bond-wires for the RF/DC feed and connection to external inductors.

The DPA of [69] is fabricated on TriQuint 0.25 μm GaN MMIC, for 2.14 GHz femto-cell base stations. In this case the integration does not include the Doherty output combiner, the output matching and the drain bias network. A driver stage is present: the interstage is optimized by removing subcircuits matched on 50 Ω and inserting a coupler optimized for the devices' impedances. The DPA, that adopts a total gate periphery at the output section of 2.4 mm, reaches an output

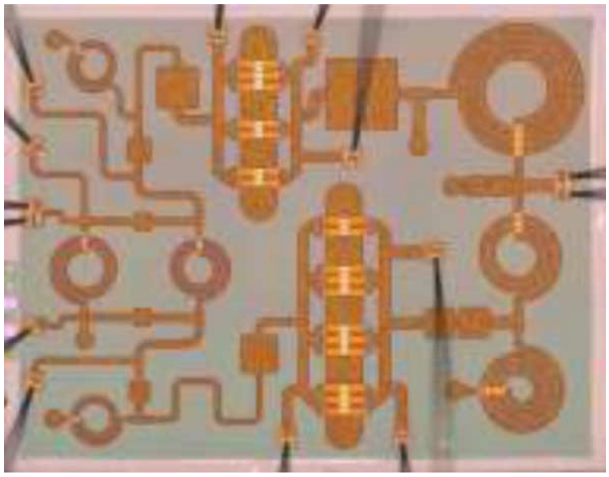

Fig. 15. Picture of the DPA presented in [68] for 2.14 GHz small cell base-stations. Size 3.3 mm×2.6 mm.

power of 41.2 dBm, with first efficiency peak of 43% at 4.7 dB OBO. Thanks to the driver stage, the gain is around 20 dB. The MMIC and the full module have area of 2.5 mm×2.7 mm and 7 mm×15 mm, respectively.

The design procedure of a K-band DPA with embedded drivers is shown in [72]: the measured results on the realized hardware, see a microscope picture in Fig. 16, show a saturated output power exceeding 1 W, together with gain higher than 9 dB over a 10% bandwidth.

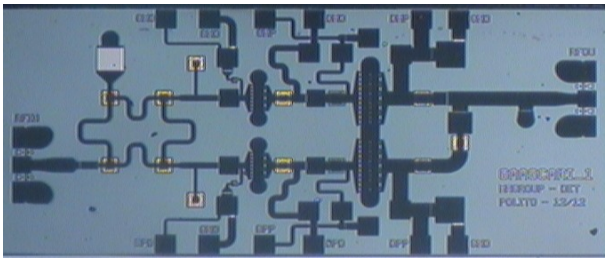

Fig. 16. Microscope picture of the GaAs MMIC DPA designed following the guidelines of [72] for K-band point-to-point radios. Size: 3 mm×1.43 mm.

VIII. Conclusion

In this paper, the most recent literature on Doherty power amplifiers has been reviewed, after the basic Doherty concepts have been briefly summarized.

The main research trends have been addressed, considering their links with the newly available technologies and the requirements of the present and future wireless communication systems.

Considering base-stations, where Si LDMOS and GaN HEMTs are the preferred choices, the main efforts are focused to enhance the back-off efficiency, and to design multi-standard hardware through multi-band or wideband solutions.

Similar tendencies are observed for portable systems, where the development of multi-standard feature has to be considered even more interesting. Implementations mainly rely on Si CMOS or GaAs HBT integrated circuits, adopting ad-hoc techniques to cope with the integration issues.

The market of backhaul point-to-point radios, at high frequency, e.g., at C- or K- band, is rapidly growing. In this framework, Doherty solutions based on GaN and GaAs HEMT monolithic circuits and adopting techniques for gain, efficiency and bandwidth enhancement are effectively exploited.

References

[1] F. Raab, P. Asbeck, S. Cripps, P. Kenington, Z. Popovic, N. Pothecary, J. Sevic, and N. Sokal, "Power amplifiers and transmitters for RF and microwave," *IEEE Trans. Microw. Theory Techn.*, vol. 50, no. 3, pp. 814–826, Mar. 2002.

[2] W. H. Doherty, "A new high efficiency power amplifier for modulated waves," *Proceedings of the Institute of Radio Engineers*, vol. 24, no. 9, pp. 1163–1182, Sep. 1936.

[3] B. Kim, J. Kim, I. Kim, and J. Cha, "The Doherty power amplifier," *IEEE Microw. Mag.*, vol. 7, no. 5, pp. 42–50, Oct. 2006.

[4] A. Grebennikov and S. Bulja, "High-Efficiency Doherty Power Amplifiers: Historical Aspect and Modern Trends," *Proc. IEEE*, vol. 100, no. 12, pp. 3190–3219, Dec. 2012.

[5] H. Chireix, "High Power Outphasing Modulation," *Proceedings of the Institute of Radio Engineers*, vol. 23, no. 11, pp. 1370–1392, Nov 1935.

[6] J. Qureshi, R. Liu, A. J. M. De Graauw, M. van der Heijden, J. Gajadharsing, and L. C. N. De Vreede, "A highly efficient Chireix amplifier using adaptive power combining," in *IEEE MTT-S International Microwave Symposium*, Jun. 2008, pp. 759–762.

[7] F. Wang, A. Yang, D. Kimball, L. Larson, and P. Asbeck, "Design of wide-bandwidth envelope-tracking power amplifiers for OFDM applications," *IEEE Trans. Microw. Theory Techn.*, vol. 53, no. 4, pp. 1244–1255, Apr. 2005.

[8] I. Kim, Y. Y. Woo, J. Kim, J. Moon, J. Kim, and B. Kim, "High-Efficiency Hybrid EER Transmitter Using Optimized Power Amplifier," *IEEE Trans. Microw. Theory Techn.*, vol. 56, no. 11, pp. 2582–2593, Nov. 2008.

[9] Y. Yang, J. Yi, Y. Y. Woo, and B. Kim, "Optimum design for linearity and efficiency of microwave Doherty amplifier using a new load matching technique," *Microwave Journal*, vol. 44, no. 12, pp. 20–36, Dec. 2001.

[10] R. Quaglia, M. Pirola, and C. Ramella, "Offset lines in Doherty power amplifiers: Analytical demonstration and design," *IEEE Microw. Wireless Compon. Lett.*, vol. 23, no. 2, pp. 93–95, Feb. 2013.

[11] S. Chia, M. Gasparroni, and P. Brick, "The next challenge for cellular networks: backhaul," *IEEE Microw. Mag.*, vol. 10, no. 5, pp. 54 –66, Aug. 2009.

[12] R. S. Pengelly, S. M. Wood, J. W. Milligan, S. T. Sheppard, and W. L. Pribble, "A review of GaN on SiC high electron-mobility power transistors and MMICs," *IEEE Trans. Microw. Theory Techn.*, vol. 60, no. 6, pp. 1764 –1783, Jun. 2012.

[13] H. Deguchi, N. Ui, K. Ebihara, K. Inoue, N. Yoshimura, and H. Takahashi, "A 33W GaN HEMT Doherty amplifier with 55% drain efficiency for 2.6 GHz base stations," in *IEEE MTT-S International Microwave Symposium*, Jun. 2009, pp. 1273–1276.

[14] I. Kim, J. Moon, S. Jee, and B. Kim, "Optimized Design of a Highly Efficient Three-Stage Doherty PA Using Gate Adaptation," *IEEE Trans. Microw. Theory Techn.*, vol. 58, no. 10, pp. 2562–2574, Oct. 2010.

[15] A. Grebennikov, "A high-efficiency 100-W four-stage Doherty GaN HEMT power amplifier module for WCDMA systems," in *IEEE MTT-S International Microwave Symposium*, Jun. 2011, pp. 1–4.

[16] V. Camarchia, J. Moreno Rubio, M. Pirola, R. Quaglia, P. Colantonio, F. Giannini, R. Giofrè, L. Piazzon, T. Emanuelsson, and T. Wegeland, "High-Efficiency 7 GHz Doherty GaN MMIC Power Amplifiers for Microwave Backhaul Radio Links," *IEEE Trans. Electron Devices*, vol. 60, no. 10, pp. 3592–3595, 2013.

[17] J. Kim, B. Fehri, S. Boumaiza, and J. Wood, "Power Efficiency and Linearity Enhancement Using Optimized Asymmetrical Doherty Power Amplifiers," *IEEE Trans. Microw. Theory Techn.*, vol. 59, no. 2, pp. 425–434, Feb. 2011.

[18] L. C. Nunes, P. M. Cabral, and J. C. Pedro, "AM/PM distortion in GaN Doherty power amplifiers," in *IEEE MTT-S International Microwave Symposium*, Jun. 2014, pp. 1–4.

[19] L. Piazzon, R. Giofrè, R. Quaglia, V. Camarchia, M. Pirola, P. Colantonio, F. Giannini, and G. Ghione, "Effect of load modulation on phase distortion in Doherty power amplifiers," *IEEE Microw. Wireless Compon. Lett.*, vol. 24, no. 7, pp. 505–507, Jul. 2014.

[20] M.-W. Lee, S.-H. Kam, Y.-S. Lee, and Y.-H. Jeong, "Design of Highly Efficient Three-Stage Inverted Doherty Power Amplifier," *IEEE Microw. Wireless Compon. Lett.*, vol. 21, no. 7, pp. 383–385, Jul. 2011.

[21] Y. Cho, D. Kang, J. Kim, K. Moon, B. Park, and B. Kim, "Linear Doherty power amplifier with an enhanced back-off efficiency mode for handset applications," *IEEE Trans. Microw. Theory Techn.*, vol. 62, no. 3, pp. 567–578, Mar. 2014.

[22] A. Mohamed, S. Boumaiza, and R. Mansour, "Doherty power amplifier with enhanced efficiency at extended operating average power levels," *IEEE Trans. Microw. Theory Techn.*, vol. 61, no. 12, pp. 4179–4187, Dec. 2013.

[23] J. Son, I. Kim, J. Moon, J. Lee, and B. Kim, "A highly efficient asymmetric Doherty Power Amplifier with a new output combining circuit," in *IEEE International Conference on Microwaves, Communications, Antennas and Electronics Systems (COMCAS)*, Nov. 2011, pp. 1–4.

[24] D. Wu and S. Boumaiza, "A mixed-technology asymmetrically biased extended and reconfigurable Doherty amplifier with improved power utilization factor," *IEEE Trans. Microw. Theory Techn.*, vol. 61, no. 5, pp. 1946–1956, May 2013.

[25] J. Moon, J. Kim, J. Kim, I. Kim, and B. Kim, "Efficiency enhancement of Doherty amplifier through mitigation of the knee voltage effect," *IEEE Trans. Microw. Theory Techn.*, vol. 59, no. 1, pp. 143–152, Jan 2011.

[26] P. Colantonio, F. Giannini, R. Giofrè, and L. Piazzon, "Increasing Doherty Amplifier Average Efficiency Exploiting Device Knee Voltage Behavior," *IEEE Trans. Microw. Theory Techn.*, vol. 59, no. 9, pp. 2295–2305, Sep. 2011.

[27] S. Zhao, Z. Tang, Y. Wu, and L. Bao, "Linearity Improved Doherty Power Amplifier Using Coupled-Lines and a Capacitive Load," *IEEE Microw. Wireless Compon. Lett.*, vol. 21, no. 4, pp. 221–223, Apr. 2011.

[28] S. Chen and Q. Xue, "Optimized Load Modulation Network for Doherty Power Amplifier Performance Enhancement," *IEEE Trans. Microw. Theory Techn.*, vol. 60, no. 11, pp. 3474–3481, Nov. 2012.

[29] J. Xia, X. Zhu, L. Zhang, J. Zhai, and Y. Sun, "High-Efficiency GaN Doherty Power Amplifier for 100-MHz LTE-Advanced Application Based on Modified Load Modulation Network," *IEEE Trans. Microw. Theory Techn.*, vol. 61, no. 8, pp. 2911–2921, Aug. 2013.

[30] S. Kawai, Y. Takayama, R. Ishikawa, and K. Honjo, "A High-Efficiency Low-Distortion GaN HEMT Doherty Power Amplifier With a Series-Connected Load," *IEEE Trans. Microw. Theory Techn.*, vol. 60, no. 2, pp. 352–360, Feb. 2012.

[31] R. Giofrè, L. Piazzon, P. Colantonio, and F. Giannini, "A Doherty architecture with high feasibility and defined bandwidth behavior," *IEEE Trans. Microw. Theory Techn.*, vol. 61, no. 9, pp. 3308–3317, Sep. 2013.

[32] D. Kang, Y. Cho, D. Kim, B. Park, J. Kim, and B. Kim, "Impact of Nonlinear C_{bc} on HBT Doherty Power Amplifiers," *IEEE Trans. Microw. Theory Techn.*, vol. 61, no. 9, pp. 3298–3307, Sep. 2013.

[33] M. Pelk, W. Neo, J. Gajadharsing, R. Pengelly, and L. C. N. De Vreede, "A High-Efficiency 100-W GaN Three-Way Doherty Amplifier for Base-Station Applications," *IEEE Trans. Microw. Theory Techn.*, vol. 56, no. 7, pp. 1582–1591, Jul. 2008.

[34] J. Kim, J. Cha, I. Kim, and B. Kim, "Optimum operation of asymmetrical-cells-based linear Doherty power Amplifiers-uneven power drive and power matching," *IEEE Trans. Microw. Theory Techn.*, vol. 53, no. 5, pp. 1802–1809, May 2005.

[35] S. Cripps, *RF power amplifiers for wireless communications*, ser. Artech House Microwave Library. Artech House, 2006.

[36] G. Sun and R. Jansen, "Broadband Doherty Power Amplifier via Real Frequency Technique," *IEEE Trans. Microw. Theory Techn.*, vol. 60, no. 1, pp. 99–111, Jan. 2012.

[37] D. Kang, D. Kim, Y. Cho, B. Park, J. Kim, and B. Kim, "Design of Bandwidth-Enhanced Doherty Power Amplifiers for Handset Applications," *IEEE Trans. Microw. Theory Techn.*, vol. 59, no. 12, pp. 3474–3483, Dec. 2011.

[38] J. Rubio, J. Fang, V. Camarchia, R. Quaglia, M. Pirola, and G. Ghione, "3–3.6-GHz Wideband GaN Doherty Power Amplifier Exploiting Output Compensation Stages," *IEEE Trans. Microw. Theory Techn.*, vol. 60, no. 8, pp. 2543–2548, Aug. 2012.

[39] D.-T. Wu and S. Boumaiza, "A Modified Doherty Configuration for Broadband Amplification Using Symmetrical Devices," *IEEE Trans. Microw. Theory Techn.*, vol. 60, no. 10, pp. 3201–3213, Oct. 2012.

[40] H. Golestaneh, F. Malekzadeh, and S. Boumaiza, "An Extended-Bandwidth Three-Way Doherty Power Amplifier," *IEEE Trans. Microw. Theory Techn.*, vol. 61, no. 9, pp. 3318–3328, Sep. 2013.

[41] C. Ma, W. Pan, S. Shao, C. Qing, and Y. Tang, "A Wideband Doherty Power Amplifier With 100 MHz Instantaneous Bandwidth for LTE-Advanced Applications," *IEEE Microw. Wireless Compon. Lett.*, vol. 23, no. 11, pp. 614–616, Nov. 2013.

[42] J. Shao, R. Zhou, H. Ren, B. Arigong, M. Zhou, H. S. Kim, and H. Zhang, "Design of GaN Doherty power amplifiers for broadband applications," *IEEE Microw. Wireless Compon. Lett.*, vol. 24, no. 4, pp. 248–250, Apr. 2014.

[43] R. Darraji, F. Ghannouchi, and M. Helaoui, "Mitigation of Bandwidth Limitation in Wireless Doherty Amplifiers With Substantial Bandwidth Enhancement Using Digital Techniques," *IEEE Trans. Microw. Theory Techn.*, vol. 60, no. 9, pp. 2875–2885, Sep. 2012.

[44] D. Gustafsson, C. Andersson, and C. Fager, "A Modified Doherty Power Amplifier With Extended Bandwidth and Reconfigurable Efficiency," *IEEE Trans. Microw. Theory Techn.*, vol. 61, no. 1, pp. 533–542, Jan. 2013.

[45] C. Andersson, D. Gustafsson, J. Chani Cahuana, R. Hellberg, and C. Fager, "A 1–3-GHz Digitally Controlled Dual-RF Input Power-Amplifier Design Based on a Doherty-Outphasing Continuum Analysis," *IEEE Trans. Microw. Theory Techn.*, vol. 61, no. 10, pp. 3743–3752, Oct. 2013.

[46] R. Klopfenstein, "A transmission line taper of improved design," *Proceedings of the IRE*, vol. 44, no. 1, pp. 31–35, Jan. 1956.

[47] H. Carlin and J. Komiak, "A new method of broad-band equalization applied to microwave amplifiers," *IEEE Trans. Microw. Theory Techn.*, vol. 27, no. 2, pp. 93–99, Feb. 1979.

[48] W. Chen, S. Bassam, X. Li, Y. Liu, K. Rawat, M. Helaoui, F. Ghannouchi, and Z. Feng, "Design and Linearization of Concurrent Dual-Band Doherty Power Amplifier With Frequency-Dependent Power Ranges," *IEEE Trans. Microw. Theory Techn.*, vol. 59, no. 10, pp. 2537–2546, Oct. 2011.

[49] K. Rawat and F. Ghannouchi, "Design Methodology for Dual-Band Doherty Power Amplifier With Performance Enhancement Using Dual-Band Offset Lines," *IEEE Trans. Ind. Electron.*, vol. 59, no. 12, pp. 4831–4842, Dec. 2012.

[50] X. A. Nghiem, J. Guan, T. Hone, and R. Negra, "Design of Concurrent Multiband Doherty Power Amplifiers for Wireless Applications," *IEEE Trans. Microw. Theory Techn.*, vol. 61, no. 12, pp. 4559–4568, Dec. 2013.

[51] A. Grebennikov and J. Wong, "A Dual-Band Parallel Doherty Power Amplifier for Wireless Applications," *IEEE Trans. Microw. Theory Techn.*, vol. 60, no. 10, pp. 3214–3222, Oct. 2012.

[52] A. Grebennikov, "Multiband Doherty Amplifiers for Wireless Applications," *High Frequency Electronics*, vol. 13, pp. 30–46, May 2014.

[53] X. Li, W.-H. Chen, Z.-H. Feng, and F. Ghannouchi, "Design of dual-band tri-way GaN Doherty power amplifier with frequency dependent power division," *Electronics Letters*, vol. 48, no. 13, pp. 797–798, Jun. 2012.

[54] W. Chen, S. Zhang, Y. Liu, Y. Liu, and F. Ghannouchi, "A concurrent dual-band uneven Doherty power amplifier with frequency-dependent input power division," *IEEE Trans. Circuits Syst. I*, vol. 61, no. 2, pp. 552–561, Feb. 2014.

[55] A. Mahmoud Mohamed, S. Boumaiza, and R. Mansour, "Reconfigurable Doherty power amplifier for multifrequency wireless radio systems," *IEEE Trans. Microw. Theory Techn.*, vol. 61, no. 4, pp. 1588–1598, Apr. 2013.

[56] S. Bassam, M. Helaoui, and F. Ghannouchi, "2-D Digital Predistortion (2-D-DPD) Architecture for Concurrent Dual-Band Transmitters," *IEEE Trans. Microw. Theory Techn.*, vol. 59, no. 10, pp. 2547–2553, Oct. 2011.

[57] J. K. A. Everard and A. King, "Broadband power efficient Class E amplifiers with a non-linear CAD model of the active MOS device," *Journal of the Institution of Electronic and Radio Engineers*, vol. 57, no. 2, pp. 52–58, Mar. 1987.

[58] E. Kaymaksut and P. Reynaert, "Transformer-Based Uneven Doherty Power Amplifier in 90 nm CMOS for WLAN Applications," *IEEE J. Solid-State Circuits*, vol. 47, no. 7, pp. 1659–1671, Jul. 2012.

[59] C. Zhao, B. Park, and B. Kim, "Complementary metal-oxide semiconductor Doherty power amplifier based on voltage combining method," *IET Microwaves, Antennas Propagation,* , vol. 8, no. 3, pp. 131–136, Feb. 2014.

[60] E. Kaymaksut and P. Reynaert, "A dual-mode transformer-based Doherty LTE power amplifier in 40nm CMOS," in *IEEE International Solid-State Circuits Conference Digest of Technical Papers (ISSCC)*, Feb. 2014, pp. 64–65.

[61] N. Ryu, S. Jang, K. Lee, and Y. Jeong, "CMOS Doherty Amplifier With Variable Balun Transformer and Adaptive Bias Control for Wireless LAN Application," *IEEE J. Solid-State Circuits*, vol. 49, no. 6, pp. 1356–1365, Jun. 2014.

[62] A. Agah, H.-T. Dabag, B. Hanafi, P. Asbeck, J. Buckwalter, and L. Larson, "Active Millimeter-Wave Phase-Shift Doherty Power Amplifier in

45-nm SOI CMOS," *IEEE J. Solid-State Circuits*, vol. 48, no. 10, pp. 2338–2350, Oct. 2013.

[63] U. Karthaus, D. Sukumaran, S. Tontisirin, S. Ahles, A. Elmaghraby, L. Schmidt, and H. Wagner, "Fully Integrated 39 dBm, 3-Stage Doherty PA MMIC in a Low-Voltage GaAs HBT Technology," *IEEE Microw. Wireless Compon. Lett.*, vol. 22, no. 2, pp. 94–96, Feb. 2012.

[64] C.-H. Koo, J.-H. Kim, and Y.-W. Kwon, "Fully Integrated HBT MMIC Series-Type Extended Doherty Amplifier for W-CDMA Handset Applications," *ETRI Journal*, vol. 32, no. 1, pp. 151–153, Jan. 2010.

[65] D. Gustafsson, J. Cahuana, D. Kuylenstierna, I. Angelov, N. Rorsman, and C. Fager, "A Wideband and Compact GaN MMIC Doherty Amplifier for Microwave Link Applications," *IEEE Trans. Microw. Theory Techn.*, vol. 61, no. 2, pp. 922–930, Feb. 2013.

[66] V. Camarchia, J. Fang, J. Moreno Rubio, M. Pirola, and R. Quaglia, "7 GHz MMIC GaN Doherty Power Amplifier With 47% Efficiency at 7 dB Output Back-Off," *IEEE Microw. Wireless Compon. Lett.*, vol. 23, no. 1, pp. 34–36, Jan. 2013.

[67] L. Piazzon, P. Colantonio, F. Giannini, and R. Giofrè, "15% bandwidth 7 GHz GaN-MMIC Doherty amplifier with enhanced auxiliary chain," *Microwave and Optical Technology Letters*, vol. 56, no. 2, pp. 502–504, Feb. 2014.

[68] C. H. Kim, S. Jee, G.-D. Jo, K. Lee, and B. Kim, "A 2.14-GHz GaN MMIC Doherty Power Amplifier for Small-Cell Base Stations," *IEEE Microw. Wireless Compon. Lett.*, vol. 24, no. 4, pp. 263–265, Apr. 2014.

[69] J. Lee, D.-H. Lee, and S. Hong, "A Doherty Power Amplifier With a GaN MMIC for Femtocell Base Stations," *IEEE Microw. Wireless Compon. Lett.*, vol. 24, no. 3, pp. 194–196, Mar. 2014.

[70] K. Yamamoto, T. Heima, A. Furukawa, M. Ono, Y. Hashizume, H. Komurasaki, S. Maeda, H. Sato, and N. Kato, "A 2.4-GHz-band 1.8-V operation single-chip Si-CMOS T/R-MMIC front-end with a low insertion loss switch," *IEEE J. Solid-State Circuits*, vol. 36, no. 8, pp. 1186–1197, Aug. 2001.

[71] S. Seki and H. Hasewaga, "Cross-tie slow-wave coplanar waveguide on semi-insulating GaAs substrates," *Electronics Letters*, vol. 17, no. 25-26, pp. 940–941, Dec. 1981.

[72] R. Quaglia, V. Camarchia, T. Jiang, M. Pirola, S. Donati Guerrieri, and B. Loran, "K-Band GaAs MMIC Doherty Power Amplifier for Microwave Radio With Optimized Driver," *IEEE Trans. Microw. Theory Techn.*, vol. 62, no. 11, pp. 2518–2525, Nov 2014.

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