Parameterized and DC-Compliant Small-Signal Macromodels of RF Circuit Blocks

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***Abstract*—This paper presents a new approach for the generation of reduced-order compact macromodels of analog circuit blocks in highly integrated Radio Frequency (RF) and Analog-Mixed-Signal (AMS) design. The circuits under investigation are designed and assumed to operate at certain bias points, where they should perform as linear as possible. So, they can be well approximated to first order by linearized transfer function models, assuming small-signal excitation around these operating points. This work concentrates on a number of key aspects. First, a fully-parameterized macromodeling flow is described, for the closed-form inclusion of external geometrical or design parameters in the macromodel responses. This aspect is important for fast optimization, design centering, and what-if analyses. Second, a parameterized DC correction strategy is presented, in order to guarantee that the DC response of the linearized macromodel matches to machine precision the true DC responses of the original circuit block. This aspect is fundamental when the macromodel is used in a system-level simulation deck that combines linearized and fully nonlinear models of other components. The main result of proposed approach is a SPICE-compatible reduced-order macromodel that can replace complex transistor-level circuit blocks plus passive interconnect networks, thus enabling dramatic speedup in transient system-level analyses and Signal Integrity verifications.**

***Index Terms*—Macromodeling, active and passive device modeling, analog/mixed-signal, behavioral modeling, CAD modeling, compact circuit modeling, linearization techniques, rational approximation, reduced order modeling, RF and mixed signal IC design, RF device modeling and characterization, signal integrity.**

I. Introduction and Motivation

Compact portable devices, such as smartphones and tablets, represent one of the dominant segments in the market of consumer electronics. Customer expectations as well as competition are the major drivers for the suppliers of such devices, who are forced to lower the costs and to continuously improve the performance of systems that are extremely compact in physical size, yet almost as powerful as modern laptop computers. This push for performance imposes stringent high level constraints during the entire design flow, and requires fast and reliable system-level verification in the early design stages to meet the required time to market.

Analog/RF System On Chip (SoC) has emerged as a successful integration approach for meeting the above performance and miniaturization goals. Different Digital, Analog Mixed/Signal (AMS) and (especially in mobile communication ICs) many Radio Frequency (RF) Circuit Blocks (CB) coexist on a single chip substrate, providing all necessary functionalities within a very compact volume [1], [2]. This proximity is often the root cause for Signal and Power Integrity problems, due to a great variety of possible coupling mechanisms (e.g., inductive, capacitive, substrate) that may occur between subsystems that are intended to be functionally isolated. Huge efforts are therefore spent during the entire design phase, in order to minimize inter-block couplings and interference [3].

Once a prototype design is available, extensive numerical simulations are required using suitable models for all CB's to verify the proper functioning of the entire system, under the great variety of operating conditions which must be supported. When full transistor level descriptions or even layout-extracted netlists are used for such simulations, the overall circuit complexity requires tremendous computational resources in terms of memory and runtime. In several situations, however, the dynamic response of individual CB's can be approximated by suitable reduced-order behavioral macromodels, which once validated against the full transistor level netlist, may offer an excellent solution for drastically reducing the overall runtime of system-level simulations.

Several approaches have been proposed for the identification of nonlinear behavioral models of CB's. These techniques range from Volterra series approximation [4], [5] and classical Wiener or Hammerstein model identification [6], to more recent approaches based on X-parameters [7]. As for applications, behavioral models have been applied both to single devices [8] and to complete CB's [9]. The above techniques aim at a full representation of nonlinear and dynamic effects of the CB under modeling. In this work, we have a simpler objective. Our targets are those building blocks, such as Low Noise Amplifiers (LNA), Operational Amplifiers (OA), Low Dropout regulators (LDO), or programmable filters, that are designed to operate almost linearly around their operation point. The nonlinear effects of such structures are deliberately weak by design [10]. Therefore, after a suitable verification of this local linearity (which is in fact part of the design flow), we derive reduced-order linear transfer function macromodels that provide a linear approximation to the broadband dynamic response of the transistor level CB, provided that small-signal operation holds. The Reader is referred to [11], [12] and references therein for a general discussion on the best linear approximation of weakly nonlinear systems.

Since the proposed macromodeling approach is based on a linearized representation of the CB responses, we can apply any of the existing state of the art techniques that have been

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proposed for model identification of linear (passive) structures, such as filters and electrical interconnects. These methods are based on rational frequency-domain curve fitting [13]–[15] applied to measured or simulated time or frequency responses, and lead to state-space reduced-order equivalents. Whenever necessary, macromodel passivity can be checked and enforced using one of the several available algorithms [16]–[19].

Successful application of this rational fitting to small-signal models of nonlinear CB's has been demonstrated in [20]. However, particular care must be taken for such structures in the accurate representation of the DC steady state response, which must match very accurately the DC response of the original (transistor-level) CB. A minimal deviation could in fact lead to wrong biasing conditions when multiple macromodels of different CB's are interconnected in a complete transceiver chain, resulting in incorrect results. This problem has been discussed in [21], where a small-signal DC compliant macromodeling technique was presented. This approach is based on the assumption that the bias conditions, hence the operating point, are fixed. Several applications, however, require the biasing conditions to change as a result of device programmability, e.g., for fine control on power consumption. This would require, in a verification stage, to recompute the behavioral macromodel for any different biasing condition, resulting in an inefficient modeling and simulation flow.

In this paper, we present a new parameterized behavioral modeling approach that is able to: i) reliably compute a reduced order small-signal macromodel of linearized CB; ii) enforce the DC response of the reduced equivalent to match exactly the DC response of the original CB; iii) include in the macromodel coefficients a closed-form parameterization in terms of both biasing conditions, e.g., the nominal V_{dd} applied to the CB, and even additional design or operation parameters, e.g., temperature or process variables.

The approach presented here builds on existing parameterized curve fitting approaches that are available in the literature [22]–[30]. Our focus is to show what modifications are needed in these (general-purpose) algorithms in order to guarantee at the same time a good parameterization and full DC compliance. The novel contributions of this work are

- a parameterized DC enforcement scheme, realized through suitable equality constraints embedded in the macromodel identification;
- the extension of the DC correction [21] to the parameterized case;
- the combination of above DC enforcement and correction schemes with existing parameterized macromodeling engines in order to derive DC-compliant parameterized small-signal reduced-order macromodels;
- a feasibility analysis of proposed small-signal linear transfer function modeling for several CB of interest in Analog/RF SoC.

This paper is organized as follows. Section II states the main problem, revises some background information, and sets notation. Section III presents our proposed parameterized and DC-compliant macromodel extraction technique. Section IV illustrates the method through various examples. Section V discusses applicability and limitations of proposed approach. Finally, Section VI draws conclusions and suggests future research directions.

II. Background and problem statement

We consider a generic nonlinear and dynamic Circuit Block (CB) represented by the following state-space equations [31]

$$\dot{x}(t;\lambda) = f(x(t;\lambda), u(t);\lambda) \tag{1}$$

$$y(t;\lambda) = g(x(t;\lambda), u(t);\lambda) \tag{2}$$

where $u, y \in \mathbb{R}^P$ denote system inputs and outputs, $x \in \mathbb{R}^Q$ is an internal state vector, and $\dot{x}$ indicates the time derivative of the state vector. In (1), the vector $\lambda \in \mathbb{R}^\rho$ collects the ρ physical or design parameters, which the circuit block response depends on and are the main subject of this investigation. Note that both state and output equations may depend on λ, inducing a parameter dependence on their solution. Therefore, state $x(t;\lambda)$ and output $y(t;\lambda)$ vectors are multivariate functions of time t and parameters λ. We assume that inputs are invariant for each geometrical or physical configuration of the system, so that $u(t)$ does not depend on λ.

A. Linear Transfer Function Models

For AMS and RF applications, several circuit blocks, such as Low Noise Amplifiers (LNA's) or programmable active filters, are designed to operate almost linearly when suitably biased and excited by small-signal inputs within the maximum allowed range of input power. Under these conditions, input, output and state vectors can be represented as a superposition of constant DC terms $U_{DC}, X_{DC}(\lambda), Y_{DC}(\lambda)$ and small-signal time dependent terms $\tilde{u}(t), \tilde{x}(t;\lambda), \tilde{y}(t;\lambda)$.

If the small-signal input $\tilde{u}(t)$ is switched off and only the constant DC bias is applied, we have $\dot{x}(t;\lambda) = 0$ uniformly for each instance of the parameter vector λ. The corresponding solution of (1)-(2) leads to the definition of the parameter-dependent DC operating point as a triplet $U_{DC}, X_{DC}(\lambda), Y_{DC}(\lambda)$, which can be easily computed through a direct DC sweep of the transistor-level circuit block, covering the desired range of the parameter vector.

Conversely, when the small-signal input is switched on, a first-order Taylor expansion of both state (1) and output (2) equations leads to

$$\dot{\tilde{x}}(t;\lambda) \approx \mathbf{A}(\lambda)\tilde{x}(t;\lambda) + \mathbf{B}(\lambda)\tilde{u}(t), \tag{3}$$

$$\tilde{y}(t;\lambda) \approx \mathbf{C}(\lambda)\tilde{x}(t;\lambda) + \mathbf{D}(\lambda)\tilde{u}(t), \tag{4}$$

where $\mathbf{A}(\lambda) \in \mathbb{R}^{Q\times Q}$, $\mathbf{B}(\lambda) \in \mathbb{R}^{Q\times P}$, $\mathbf{C}(\lambda) \in \mathbb{R}^{P\times Q}$ and $\mathbf{D}(\lambda) \in \mathbb{R}^{P\times P}$ denote parameter-dependent state-space matrices defining the small-signal Linear Transfer Function Model (LTFM) of the CB around the specified bias conditions, with frequency- and parameter-dependent input-output response

$$\mathbf{H}(s;\lambda) = \mathbf{C}(\lambda)(s\mathbf{I} - \mathbf{A}(\lambda))^{-1}\mathbf{B}(\lambda) + \mathbf{D}(\lambda). \tag{5}$$

The elements of these state matrices are formally defined as partial derivatives of the various components of (1)-(2) evaluated at the current DC point.

B. Frequency and Time-domain macromodeling

The standard approach for the characterization of the small-signal input-output behavior of the CB is to extract a set of frequency- and parameter- dependent small-signal Scattering $\mathsf{S}(\jmath\omega;\lambda)$, Admittance $\mathsf{Y}(\jmath\omega;\lambda)$ or Impedance $\mathsf{Z}(\jmath\omega;\lambda)$ parameters, in the following collectively denoted as $\mathsf{H}(\jmath\omega;\lambda)$ through a set of small-signal AC analyses. Standard circuit solvers of the SPICE class are able to perform this operation only for discrete values of frequency

$$\omega \in \{\widehat{\omega}_\nu,\ \nu = 1,\dots,N\} \tag{6}$$

and parameters

$$\lambda \in \{\widehat{\lambda}_k,\ k = 1,\dots,K\}, \tag{7}$$

resulting in a set of $P \times P$ complex matrices

$$\widehat{\mathsf{H}}_{\nu,k} = \mathsf{H}(\jmath\widehat{\omega}_\nu;\widehat{\lambda}_k)\,. \tag{8}$$

Throughout this paper, we denote with a hat $\widehat{Z}$ any quantity Z that is available from a direct solution of the original transistor-level CB via, e.g., a SPICE run. This includes also the computed DC operating points for the state and the output vectors over the parameter grid

$$\widehat{X}_{DC,k} = X_{DC}(\widehat{\lambda}_k) \tag{9}$$

$$\widehat{Y}_{DC,k} = Y_{DC}(\widehat{\lambda}_k)\,. \tag{10}$$

The discrete samples (8) of the linearized system response provide an excellent approximation of the system behavior for design and verification purposes, as long as this verification is conducted in the frequency domain and for the available parameter values $\widehat{\lambda}_k$. However, if the CB response is required for an arbitrary parameter configuration λ_* that is not part of the discrete set $\{\widehat{\lambda}_k\}$, a new extraction is required by solving the original CB system (1)-(2). For complex CB's and for repeated parameter instances this approach may be overly time-consuming.

If the verification has to be performed in the time-domain, a frequency-to-time conversion is further required. Several macromodeling approaches are available [13], [15] for performing this conversion and obtaining an approximate state-space representation in form of (3)-(4) or (5). This process usually leads to a reduced-order compact system with a number of states $q \ll Q$. Macromodeling approaches are standard for non-parameterized systems. In our setting, for any fixed parameter instance $\lambda = \widehat{\lambda}_k$, the frequency dependence of the data samples $\widehat{\mathsf{H}}_{\nu,k}$ is approximated by a rational model, or equivalently a state-space system in form

$$\mathbf{H}_k(s) = \mathbf{C}_k(s\mathbf{I} - \mathbf{A}_k)^{-1}\mathbf{B}_k + \mathbf{D}_k \tag{11}$$

by minimizing the macromodel error $\|\mathbf{H}_k(\jmath\widehat{\omega}_\nu) - \widehat{\mathsf{H}}_{\nu,k}\|$ in the desired norm. The Vector Fitting (VF) scheme [13] with all its possible variants provides an excellent numerical tool.

The standard VF approach however does not solve the problem of making a compact model available for any desired values of the parameters λ. Fortunately, an explicit treatment of the parameter dependence for the derivation of a parameterized macromodel is also possible, using one of the available parameterized rational curve fitting strategies [22]–[30]. These methods are able to process collectively the samples (8) to obtain a multivariate representation of the system as a parameterized reduced-order macromodel in a form identical to (5), by minimizing the error $\|\mathbf{H}(\jmath\widehat{\omega}_\nu;\widehat{\lambda}_k) - \widehat{\mathsf{H}}_{\nu,k}\|$ over the entire set of frequency and parameter samples. A more detailed description of this approach is postponed to Section III.

C. The need for DC correction

Another issue may affect the above described macromodeling flow, possibly making the resulting small-signal parametric macromodels completely useless when employed in time-domain transient simulations. In fact, a direct replacement of the nonlinear CB with the Linear Transfer Function Model (LTFM) in a transient simulation setup leads to possibly incorrect biasing, since the small-signal macromodel does not include any information of the underlying DC operating point. When excited by constant inputs $u(t) = U_{DC}$, the LTFM (5) provides its closed form DC output solution

$$\begin{aligned} Y^0_{DC}(\lambda) &= \mathbf{H}(0;\lambda)U_{DC} \\ &= (\mathbf{D}(\lambda) - \mathbf{C}(\lambda)\mathbf{A}^{-1}(\lambda)\mathbf{B}(\lambda))U_{DC}, \end{aligned} \tag{12}$$

which has no relationship with the true DC operating point of the original nonlinear CB. This information is not embedded in the LTFM, which only represents the dynamics of small signal variations around the bias point. This problem becomes severe when several CB's are connected together to form a complete RF transceiver path. If one of the CB models provides the incorrect DC bias as its output, which is in turn fed to the input of another block, the latter will not function properly due to inconsistent biasing, and the entire verification results will be wrong.

For the non-parametric case, or equivalently for any fixed instance $\lambda = \widehat{\lambda}_k$, it was shown in [21] how the correct DC bias can be recovered by adding suitable constant DC correction sources at the macromodel ports. Assume that for any discrete parameter value $\widehat{\lambda}_k$, the correct bias conditions provided by the input U_{DC} and output $\widehat{Y}_{DC,k} = Y_{DC}(\widehat{\lambda}_k)$ are known from a numerical solution of the original non-linear system. We compute the DC solution $Y^0_{DC}(\widehat{\lambda}_k)$ of the LTFM driven by the same nominal biasing inputs U_{DC} as in (12), and we form the difference

$$\Delta_{DC}(\widehat{\lambda}_k) = \widehat{Y}_{DC,k} - Y^0_{DC}(\widehat{\lambda}_k), \tag{13}$$

which represents the correction that must be applied to the DC solution of the LTFM in order to obtain the nominal CB bias level. The correction terms $\Delta_{DC}(\widehat{\lambda}_k)$ are applied by defining an enlarged DC-corrected small-signal macromodel which embeds the original LTFM and adds at its interface ports suitable constant sources (see Fig. 1), whose values are the components of $\Delta_{DC}(\widehat{\lambda}_k)$. It should be noted that using constant correction sources will affect and fix the DC point only, without any effect on the accuracy of the LTFM dynamics around the operating point under small-signal excitation.

The above approach is valid only for a fixed parameter value $\lambda = \widehat{\lambda}_k$. Therefore, a new LTF macromodel extraction and a new computation of the DC correction sources for any new

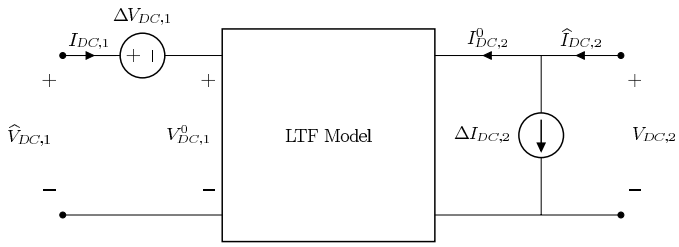

Fig. 1. DC point correction for a two port LTFM, assuming a hybrid configuration with one current-controlled (left) and one voltage-controlled (right) port. The correct DC bias is set via constant current sources $\Delta V_{DC,1}$ and $\Delta I_{DC,2}$ applied at the input ports of the LTFM. The source values are provided by the elements of the correction vector (13).

instance of the parameters is required. The main purpose of this work is to present a general strategy that is able to process the full set of samples (8), providing a DC-compliant reduced-order parameterized LTF macromodel that can be directly used to replace a transistor-level CB for any system-level time-domain verification and for any arbitrary parameter value λ within an admissible range.

III. DC-COMPLIANT PARAMETERIZED MACROMODELING

A. Outlook

The proposed strategy for the extraction of a DC-compliant and parameterized small-signal macromodel can be summarized in the following steps:

1) create a suitable CB characterization test bench in the adopted circuit simulation environment and apply the desired biasing circuitry to each CB pin;
2) extract DC bias information $\widehat{Y}_{DC,k}$ and small-signal frequency response $\widehat{\mathsf{H}}_{\nu,k}$ of the CB from a set of circuit simulations of the non-linear system, here represented by (1)-(2), for a set of discrete parameter values $\lambda \in \{\widehat{\lambda}_k,\ k = 1, \ldots, K\}$ and at a discrete set of frequencies $\omega \in \{\widehat{\omega}_\nu,\ \nu = 1, \ldots, N\}$;
3) perform a parameterized rational curve fitting of the data $\widehat{\mathsf{H}}_{\nu,k}$ using a multivariate parametric macromodeling scheme, and obtain a state-space realization (5) of the LTFM;
4) compute $Y^0_{DC}(\widehat{\lambda}_k)$ from (12) and $\Delta_{DC}(\widehat{\lambda}_k)$ from (13) over the discrete parameter grid $\widehat{\lambda}_k$;
5) interpolate the data $\Delta_{DC}(\widehat{\lambda}_k)$ with a closed-form parametric expression $\bar{\Delta}_{DC}(\lambda)$ so that
$$\bar{\Delta}_{DC}(\widehat{\lambda}_k) = \Delta_{DC}(\widehat{\lambda}_k) \tag{14}$$
6) synthesize a circuit netlist with a standard parameterized macromodel realization, complemented by DC correction sources $\bar{\Delta}_{DC}(\lambda)$ connected at its external ports.

Figure 1 depicts the result of this process in terms of high-level schematic blocks. Next sections provide more details on our proposed modeling strategy for steps 3), 5), and 6).

The strategy for the determination of the parameter and frequency grids in step 2) will vary on a case by case basis. For all CB that we analyzed, the parameter grid points are collocated on a cartesian grid in the parameter space, with uniform spacing along any direction, see Sec. IV. About frequency sampling, the main guideline is to guarantee an accurate representation of all dynamics over a broad frequency band ranging from DC up to the highest frequency of interest for the specific application. Frequency sample distribution and density will have to track the frequency variations of the small-signal transfer functions under modeling. For all test cases reported in this work, we used a uniform logarithmic spacing with $N_d = 20$ samples per decade, plus of course the DC point.

B. Parameterized rational curve fitting

This section presents some further background information on parameterized rational curve fitting, in order to set additional notation for later developments. We consider the following representation for the parameterized small-signal macromodel
$$\mathbf{H}(s,\lambda) = \frac{\mathbf{N}(s,\lambda)}{d(s,\lambda)} = \frac{\sum_{m=0}^{M} \mathbf{R}_m(\lambda)\phi_m(s)}{\sum_{m=0}^{M} r_m(\lambda)\phi_m(s)} \tag{15}$$
where the frequency-dependent basis functions are partial fractions [13] associated to a set of distinct prescribed poles q_m, defined as $\phi_0(s) = 1$ and $\phi_m(s) = (s - q_m)^{-1}$, and where the parameter-dependent coefficients are expressed as a superposition of multivariate basis functions $\xi_\ell(\lambda)$ as
$$\mathbf{R}_m(\lambda) = \sum_{\ell=1}^{L} \mathbf{R}_{m,\ell}\xi_\ell(\lambda), \quad r_m(\lambda) = \sum_{\ell=1}^{L} r_{m,\ell}\xi_\ell(\lambda) \tag{16}$$
with constant and unknown coefficients $\mathbf{R}_{m,\ell}$ and $r_{m,\ell}$. The representation (15) is quite general, since it provides an implicit parameterization of M-th order rational matrices with both parameter-dependent poles and residues [22], [24], [32].

Several choices are possible for the basis functions $\xi_\ell(\lambda)$, such as monomials, orthogonal polynomials, or finite elements defined over structured or unstructured grids in the parameter space [22]–[30]. In this work we use standard monomials, as in Response Surface Modeling [33], by setting
$$\xi_\ell(\lambda) = \prod_i \lambda_i^{\kappa_{\ell,i}} \tag{17}$$
with i spanning the number ρ of free parameters (components of λ), with ℓ interpreted as a global index spanning the set of all multivariate monomials including powers up to $L_i - 1$ of the i-th parameter λ_i. The determination of L_i is discussed in Sec. III-D. The total number of basis functions is therefore
$$L = \prod_{i=1}^{\rho} L_i\,. \tag{18}$$
The choice of polynomials is justified here by the expected smooth parameter dependence for the structures of our interest. This will be confirmed by all examples of Sec. IV. This choice is however not restrictive, since the same procedure can be applied without any modification to different parameterization schemes based on general basis functions $\xi_\ell(\lambda)$.

Given the set $\widehat{\mathsf{H}}_{\nu,k}$ of small-signal transfer matrices available at the frequency points $\widehat{\omega}_\nu$ and parameter grid values $\widehat{\lambda}_k$, the

coefficients $\mathbf{R}_{m,\ell}$ and $r_{m,\ell}$ are computed through a generalized parametric Sanathanan-Koerner (SK) iteration [24], [34], which minimizes the following cost function

$$\mathcal{E}_\mu^2 = \sum_{\nu=1}^{N}\sum_{k=1}^{K} \left\| w_{\nu,k}^{(\mu)} \left[\mathbf{N}^{(\mu)}(\jmath\widehat{\omega}_\nu;\widehat{\lambda}_k) - d^{(\mu)}(\jmath\widehat{\omega}_\nu;\widehat{\lambda}_k)\widehat{\mathsf{H}}_{\nu,k} \right] \right\|^2 \tag{19}$$

at each iteration $\mu = 1, 2, \ldots$, where the iteration-dependent weight $w_{\nu,k}^{(\mu)}$ is defined as the inverse of the denominator estimate available at the previous iteration

$$w_{\nu,k}^{(\mu)} = \left[d^{(\mu-1)}(\jmath\widehat{\omega}_\nu;\widehat{\lambda}_k) \right]^{-1} \tag{20}$$

with the initialization $w_{\nu,k}^{(0)} = 1$. The above SK formulation is a standard approach in linear and parameterized macromodeling. It allows to cast a global nonconvex optimization problem as a sequence of linearized problems (19), since the residual whose norm is being minimized at each iteration is an affine combination of the free variables $\mathbf{R}_{m,\ell}$ and $r_{m,\ell}$. Therefore, the numerical solution of (19) does not involve particular difficulties, requiring a simple linear least squares solver. There is however an additional difficulty, due to the fact that (19) will minimize the least squares error, without any control over the accuracy of the fitted model at prescribed frequency points, including DC. For our application, which requires an exact representation of the DC response of the small-signal macromodel, we need a better control.

C. DC enforcement and correction

The DC response of the parameterized macromodel is readily computed from (15) as

$$\mathbf{H}(0,\lambda) = \frac{\mathbf{N}(0,\lambda)}{d(0,\lambda)} = \frac{\sum_{m=0}^{M}\mathbf{R}_m(\lambda)\phi_m(0)}{\sum_{m=0}^{M} r_m(\lambda)\phi_m(0)}\,. \tag{21}$$

Denoting with

$$\widehat{\mathsf{H}}_{0,k} = \mathsf{H}(0;\widehat{\lambda}_k) \tag{22}$$

the DC value of the linearized response of the original system, which is easily extracted or extrapolated from a circuit solution of the original schematic, we can enforce the parameterized macromodel to match exactly this DC response by adding the following set of equality constraints

$$\sum_{m=0}^{M}\mathbf{R}_m(\widehat{\lambda}_k)\phi_m(0) - \widehat{\mathsf{H}}_{0,k}\sum_{m=0}^{M} r_m(\widehat{\lambda}_k)\phi_m(0) = 0 \tag{23}$$

for $k = 1, \ldots, K$ to the linear least squares problem (19). The constraints (23) are also expressed as affine combinations of the decision variables. Therefore, the minimization of (19) subject to (23) is easily achieved through any standard solver for linearly-constrained linear least squares problems.

Once the macromodel coefficients are available, we proceed with the computation of the DC bias correction sources using (13), for each of the available parameter grid values $\widehat{\lambda}_k$. Then, a parameterized set of DC correction sources is defined as a superposition of the basis functions $\xi_\ell(\lambda)$ as

$$\bar{\Delta}_{DC}(\lambda) = \sum_{\ell=1}^{L}\bar{\Delta}_\ell\xi_\ell(\lambda). \tag{24}$$

The coefficients $\bar{\Delta}_\ell$ are computed by enforcing the fitting/interpolation condition (14) for each k, which requires the solution of a further linear least squares system.

D. Order selection

The determination of a correct dynamical order M (number of poles) and number L of parameter-dependent basis functions is very important to obtain accurate macromodels with minimal complexity. In general, model accuracy increases when increasing M and L. However, it is important to limit the number of basis functions in order to avoid overfitting conditions. Since an a priori determination of the orders required for tracking both frequency and parameter variations is generally not available, we determine these orders adaptively during the construction of the macromodels, through the following steps

1) We first consider an independent rational function fit for few small-signal scattering responses corresponding to selected parameter grid points (e.g., the nominal configuration and all corners of the parameter range). A standard VF run is used in its implementation [14] for iteratively increasing the rational function order until all such responses are independently fitted with a satisfactory accuracy. The selected model order M is thus defined as the order that guarantees that nominal and corner individual fits fall uniformly below a prescribed accuracy threshold.
2) We extract the pole set q_m from the order-M rational macromodel corresponding to the nominal parameter configuration (typically the center of the parameter range of interest), and we use it in the construction of the parameterized SK iteration (15).
3) The polynomial order L_i required for tracking the variations induced by each component λ_i of the parameter vector λ is determined by fitting, via independent parameterized SK iterations, one-dimensional subsets of small-signal responses, by freezing the remaining parameter components $\lambda_{j\neq i}$ to their nominal value. Also in this case we iteratively increase L_i until the accuracy is satisfactory.
4) The multivariate polynomial order L is then determined from the individual orders L_i based on representation (17), and the multivariate SK iteration (19) is run to compute the final parameterized macromodel.
5) The same procedure of step 3) is used to approximate the DC correction sources via (14).

E. Computational complexity

We discuss here the complexity of the model extraction procedure. The relevant parameters are: number of ports P, number of frequency samples N, total number of samples in the parameter space K, model dynamical order M, and total number of polynomial basis functions L, defined in (18). The step that dominates the identification process is the minimization of the SK cost function (19), which requires a least squares solution. The associated matrix has size $\mathcal{N}_r \times \mathcal{N}_c$, with $\mathcal{N}_r = 2P^2KN + 1$ and $\mathcal{N}_c = L(M+1)(P^2+1)$. Since typically $\mathcal{N}_r \gg \mathcal{N}_c$, the CPU cost for the LS solution

scales as $O(\alpha \mathcal{N}_r^2 \mathcal{N}_c)$, with a constant α that depends on the particular implementation. In case the number of ports P exceeds few units, this complexity can be decreased by independently fitting each individual transfer function element, leading to a CPU cost scaling as $O(P^2)$ instead of $O(P^6)$.

From the above scalability estimates, it becomes evident that the proposed approach can only be applied with a limited number of concurrent parameters ρ, say few units, otherwise the model identification will suffer from a curse of dimensionality. The same consideration applies to the polynomial order L_i for each considered parameter. The approach is effective if also L_i is limited to few units, say up to ten, in order to limit both computational complexity and numerical ill-conditioning during model identification. Should a higher order be required (a situation that never occurred in the analyzed testcases), then the overall modeling approach would become ineffective.

F. Macromodel representation and synthesis

The above described procedure results in a DC compliant parameterized small-signal macromodel $\mathbf{H}(s, \lambda)$ defined in (15), plus a set of parameter-dependent DC correction sources $\bar{\Delta}_{DC}(\lambda)$ defined in (24). These two block elements are connected as in Fig. 1. The final step consists of casting these expressions in a form that can be used in a circuit solver of the SPICE class.

For the small-signal macromodel part, the detailed derivation in [24], see also [35]–[37] shows that $\mathbf{H}(s, \lambda)$ can be easily converted into a parameterized descriptor form

$$\begin{aligned} \mathbf{E}\dot{\tilde{x}}(t;\lambda) &= \mathbf{A}(\lambda)\tilde{x}(t;\lambda) + \mathbf{B}(\lambda)\tilde{u}(t), \\ \tilde{y}(t;\lambda) &= \mathbf{C}(\lambda)\tilde{x}(t;\lambda) \end{aligned} \tag{25}$$

where the parameter-dependent matrix elements correspond one-to-one with the coefficients $\mathbf{R}_m(\lambda)$ and $r_m(\lambda)$. Since polynomial basis functions $\xi_\ell(\lambda)$ are used in our expansion, a SPICE synthesis of these equations is straightforward using elementary dependent sources with polynomial gain. The same consideration and synthesis applies for the DC correction sources $\bar{\Delta}_{DC}(\lambda)$. The components of the resulting macromodel netlists are thus defined as closed-form functions of the external parameters. At runtime, these parameters are known and fixed (e.g., ambient temperature or nominal V_{dd}), so that each macromodel instance becomes fully specified, with all components characterized by a fixed numerical value.

G. Stability and passivity

The proposed macromodeling flow is applied here to describe the linearized behavior of active nonlinear CB's. Therefore, passivity verification and enforcement –a standard requirement in linear macromodeling applications (see e.g. [16]–[19])– is not required at all since the original CB is not a passive device when characterized through small-signal transfer functions. Should the application at hand require a guaranteed passive parameterized macromodel, a passive parameterization should be used instead of (15). See [27]–[30] for more details.

Conversely, uniform stability is important for any subsequent transient analysis. All macromodel poles (which depend on the parameters λ) should be confined into the left half complex plane for any value of the parameters within the admissible range. A simplistic approach to enforce uniform stability is to not parameterize the poles at all, at the price of a reduced accuracy and generality of the small-signal macromodel. This is easily achieved by removing in (15) the dependence on the parameters λ of the denominator coefficients $r_m(\lambda)$, see [20]. In general, necessary and sufficient criteria that are able to guarantee uniform stability without compromising the macromodel accuracy, e.g. by imposing additional structure in the model equations, are still not available.

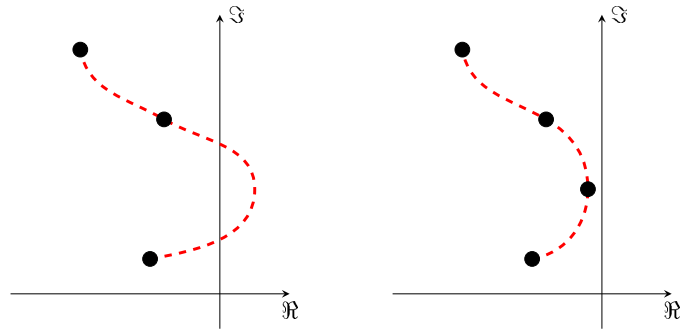

Fig. 2. Left panel: using a coarse grid (dots) for model identification may lead to parameterized pole trajectories (dashed line) leaking into the right hand complex plane. Right panel: grid refinement constrains the parameterized poles into the stable region.

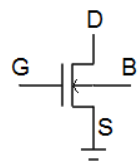

Fig. 3. Schematic of the single NMOS transistor testcase.

Guaranteed stable non-parameterized macromodels (11) for any fixed parameter value are easy to obtain, see [13]. When introducing the external parameters λ, the essential condition for preserving uniform stability is to start with a sufficiently dense parameter grid $\widehat{\lambda}_k$, so that all system poles are tracked with sufficient resolution between grid values. Figure 2 provides an intuitive illustration that instability may occur for coarse grids due to insufficient knowledge of the original system dynamics between grid values. A proper dense grid facilitates the enforcement of uniform stability.

In our implementation, after computing an initial parameterized macromodel (15), we compute the macromodel poles, i.e., the generalized eigenvalues of pencil $(\mathbf{E}, \mathbf{A}(\lambda))$, over a dense grid in the parameter space. Note that this verification involves a minimal cost due to the compact size of the macromodel. Should unstable poles be detected for some parameter value λ_*, the identification grid $\widehat{\lambda}_k$ is enlarged by adding λ_* and the macromodel is recomputed. This last repeated fitting stage was never required for all application examples that were tested.

IV. Examples

The effectiveness of the proposed methodology is demonstrated on several examples from a state-of-the-art low-power

and high-performance CMOS technology. The first two cases are very simple: a single NMOS transistor and a two-stage buffer. These examples are mainly used as a proof of concept. The third example is instead a fully implemented circuit block, namely a Low Dropout Voltage regulator used in a commercial 3G transceiver design. One last example presents a simple system-level scenario, showing significant speedup in transient simulation when multiple reduced-order macromodels are used to replace the corresponding transistor-level CB's. In all cases, the accuracy of the macromodels is demonstrated through reference frequency-domain or time-domain responses, obtained either by numerical SPICE simulations of full transistor-level netlists, or by alternative modeling approaches. The construction of the macromodels for all examples was performed in the MATLAB software environment, running on a notebook (2.7 GHz clock, 16GB RAM, Windows 7, 64bit). All circuit simulations were instead performed on a Linux server (2.6 GHz clock, 160 GB RAM), where the required circuit simulation software and related component libraries were available.

We remark that, although the test cases that we discuss in this paper are intended for RF applications operating in the microwave range, the bandwidth over which the macromodels are validated is much broader. In fact, since the models are here intended for Signal and Power Integrity analysis and verification, we should consider that the spectrum of noise that might be injected into the system from various sources (EMI, resonances of the global power distribution network, etc...) can be significant in very different frequency bands. In fact, most often chip-package-board resonances induce noise that may have significant spectral components even at lower frequencies. If the transistors that form the circuit blocks are biased with a voltage that oscillates due to a broadband noise disturbance, the functional RF performance of the entire system will be affected. Therefore, the type of analysis that we target require an accurate characterization in a very broad frequency band, and not only in the microwave range or in a small bandwidth around the carrier frequency. For these reason, all macromodels will be validated from DC up to a very large upper frequency, so that also the high-frequency asymptotic behavior can be verified.

A. A NMOS transistor

The first example illustrates the proposed methodology on a single NMOS transistor, for which a small-signal linearized model is derived using the source-drain bias voltage $V_{\rm ds}$ as a free parameter. A three-port configuration is considered, where port one is the drain, port two the gate, and port three the bulk, all referenced to the source, as depicted in Figure 3. This is the typical test pattern used to characterize field effect transistors. Because of the technology used $V_{\rm th} \approx 0.6$ V, the NMOS is biased with $V_{\rm gs} = 1.2$ V and $V_{\rm bs} = 0$ V. As a consequence, a sweep of $V_{\rm ds}$ from 0.8 V to 1.2 V explores the linear region of the NMOS characteristic.

A comparison of the small-signal S_{12} response of the original device with the corresponding parameterized model is reported in Fig. 4 for a $V_{\rm ds}$ sweep ranging from 0.8 V to 1.2 V.

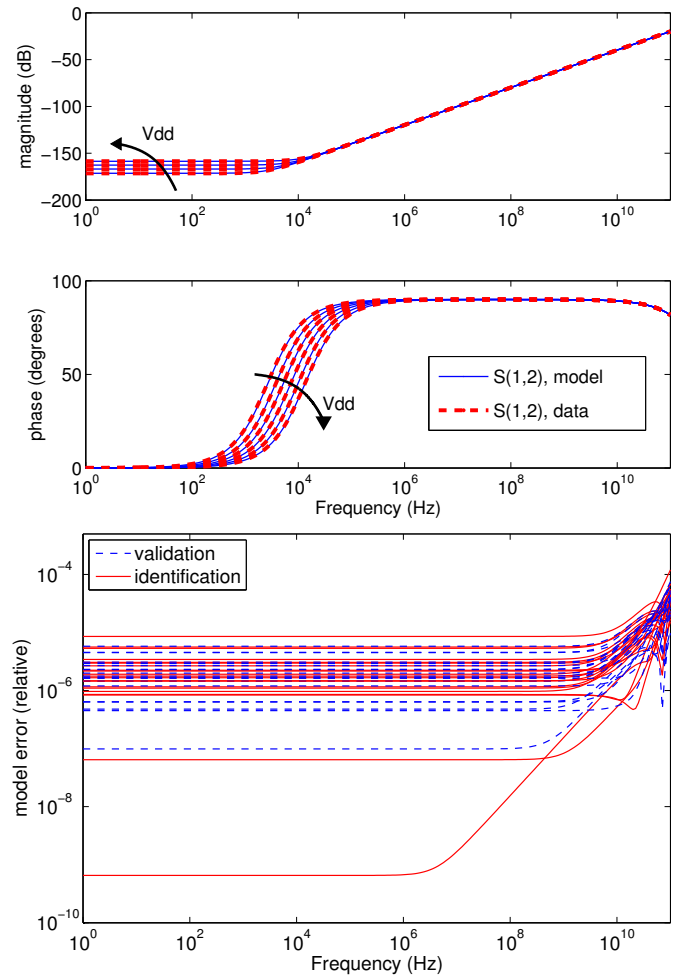

Fig. 4. Magnitude (top) and phase (middle) of S_{12} for the parameterized small-signal NMOS model (blue solid lines) compared to the corresponding original responses (dashed red lines), plotted for different values of the parameter $V_{\rm ds}$ ranging from 0.8 V to 1.2 V. The S_{12} is the response with the smallest values at DC for a sweep of the $V_{\rm ds}$. This result demonstrates the effectiveness of the proposed DC enforcement strategy. Bottom panel reports the frequency-dependent relative approximation error between macromodel and original responses, for all parameter configurations (both identification and validation points).

This figure demonstrates that, even if the dynamic variation of the responses is very large, the proposed DC enforcement strategy is able to guarantee a very accurate macromodel, even at low frequencies where the magnitude response is very small (lower than -150 dB).

Figure 5 shows the computed parametric correction source to be applied to the input port (Gate) for DC compliance. Only the points marked with red squares ($K = 21$ points, with linear spacing within the investigated V_{ds} range) were used for the macromodel identification, whereas the blue crosses indicate additional validation points (20 in total) used to verify the interpolation. As expected, the dependence of this correction source on $V_{\rm ds}$ is very smooth and therefore well captured by a low-order interpolation. The parameterized model has dynamical order two, while both numerator and denominator polynomial bases (15) have degree two. Finally, Fig. 6 reports the parameterized macromodel (real) poles, that for this simple

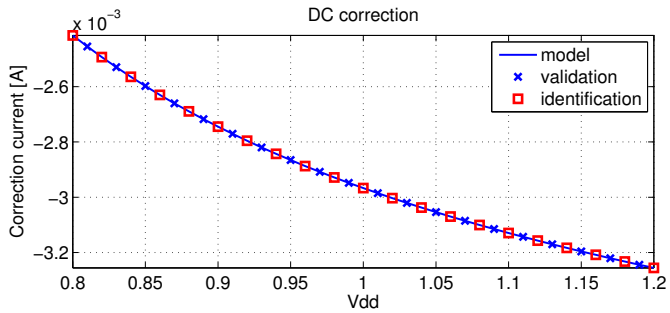

Fig. 5. Parametric DC current correction source (Gate) for the small-signal NMOS model, plotted as a function of $V_{\rm ds}$.

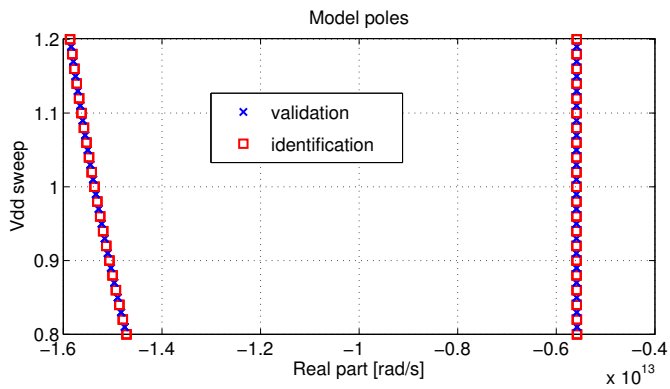

Fig. 6. Parameter-dependent poles of the small-signal NMOS model.

device show a weak and smooth dependence on the free parameter $V_{\rm ds}$ as a consequence of the small variation of charges in the MOS channel while working in the linear region. The construction of the parameterized macromodel required only two seconds, while the extraction of the small-signal scattering parameters required a fraction of a second.

B. A two-stage buffer

The second example is the two-stage buffer depicted in Fig. 7. For this test case, two parameters are used: the supply voltage $V_{\rm dd} \in [0.7, 1.2]$ V and the ambient temperature, in the range $T \in [-25°, 125°]$ C. The grid of parameter values used for model identification was defined with six points along $V_{\rm dd}$ and 26 points along T with linear spacing, thus defining a

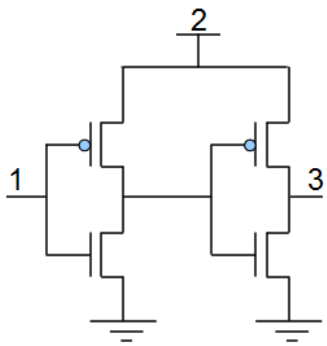

Fig. 7. A two-stage buffer with specification of the adopted port numbering.

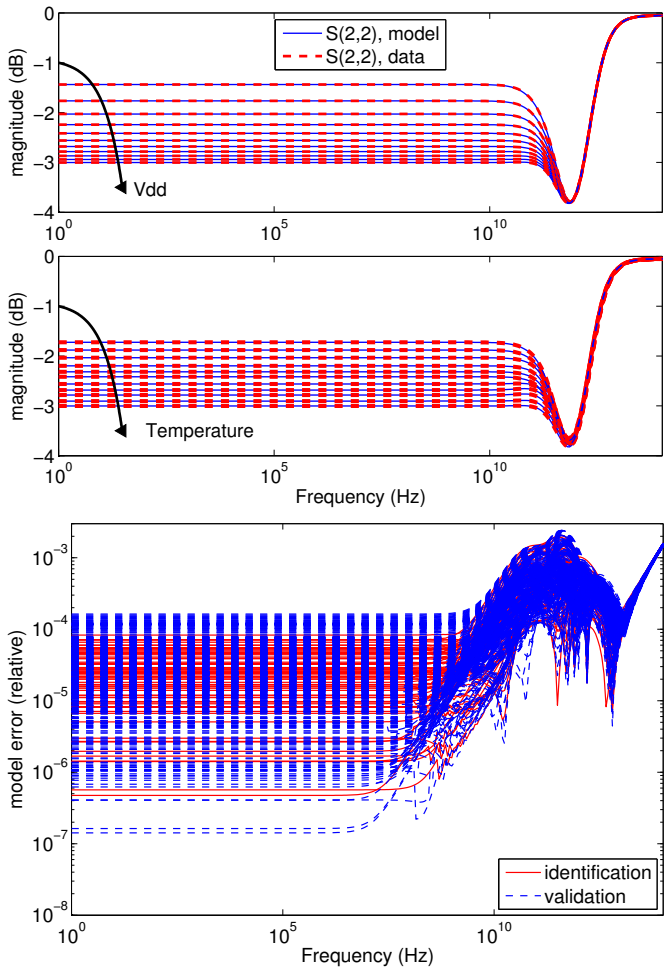

Fig. 8. S_{22} for the parameterized small-signal buffer model (blue solid lines) compared to the corresponding original response (dashed red lines). In the top panel, the temperature T is fixed to 20°C and $V_{\rm dd}$ sweeps from 0.7 V to 1.2 V, while in the middle panel, $V_{\rm dd}$ is fixed to 0.75 V and T sweeps in the range $-25 \div 120$°C. S_{22} is presented being the S-parameter with the largest variation induced by both parameters $V_{\rm dd}$ and T. Bottom panel reports the corresponding relative approximation errors for all parameter grid values (both identification and validation).

5×25 regular mesh. The centers of the resulting rectangular patches in the parameter domain were used as additional points to validate the interpolation. Due to the very simple circuit topology, the extraction time of S-parameters required less than a second.

The accuracy of the parameterized macromodel is demonstrated by comparing the small-signal S-parameter S_{22} (corresponding to the $V_{\rm dd}$ pin) of the original buffer to the macromodel response for two sweeps of $V_{\rm dd}$ and T in the two panels of Fig. 8. For this example, we used a dynamical order four, with both numerator and denominator polynomial bases (15) having degree two.

Figure 9 depicts the parameterized DC correction sources at the supply and output ports of the buffer, comparing the raw data with the interpolated model. Considering that temperature effects in transistors models are described by low degree polynomials (two or three at most), these two dimensional correction functions can be expected to be smooth

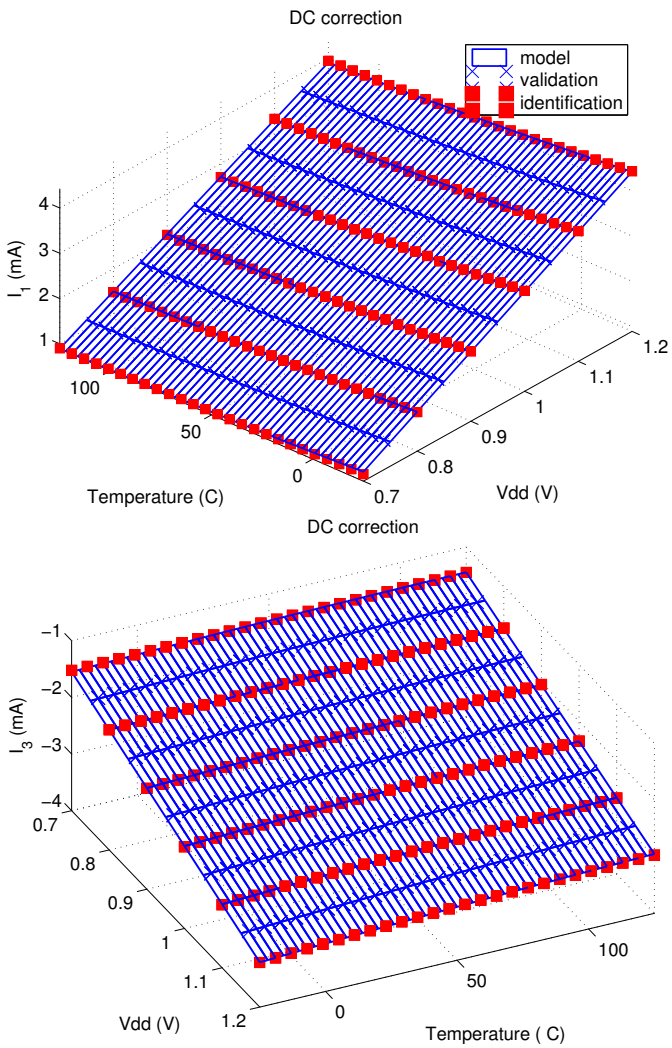

Fig. 9. Parameterized DC correction sources for the supply (top) and output port (bottom) of the two-stage buffer.

as well thanks to the proposed explicit DC constraint in the macromodel fitting. Therefore, a low-order interpolation scheme is appropriate. We used for this example a multivariate polynomial of order two, leading to a root mean square error of the polynomial interpolation less than 10^{-5}. Overall macromodel identification required 55 seconds.

C. A Low Dropout (LDO) voltage regulator

The next example is a Low Dropout (LDO) voltage regulator, whose transistor level schematic is taken from a commercial 3G transceiver design. A high-level block diagram is depicted in Fig. 10. This device is intended to provide a stabilized output voltage, under control of external settings provided by a logic unit. The parameter that is considered is again the supply voltage $V_{\rm d} \in [1.2, 1.7]$ V. For such a sweep of $V_{\rm d}$ and using a reference voltage of 0.6 V, the LDO works in the linear region of the characteristic. The original schematic includes hundreds of transistors, therefore a reduced-order macromodel is desirable to reduce complexity and runtime in system-level simulations. We remark that the

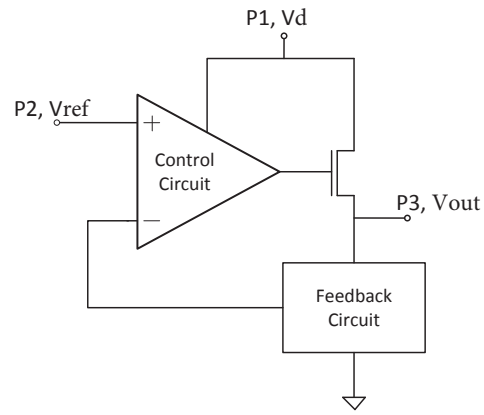

Fig. 10. High-level block diagram of a Low Dropout Voltage regulator, with associated port numbering.

TABLE I
TRANSIENT SIMULATION RUNTIME FOR DIFFERENT LDO MODELS AND CORRESPONDING SPEEDUP FACTORS.

LDO model	Elapsed time	SpeedUp
Transistor-Level	1h 5m 33s	
S-parameters	7m 35s	vs TL: 8.64×
LTFM	48.67s	vs TL: 80.8×; vs S-pars: 9.35×

only information used for macromodel computation consists of a set of small-signal S-parameters and additional DC sweeps, both defined at the external ports, computed through SPICE runs. No information on the internal transistor-level description is used for macromodel identification, which is thus purely black-box. The evaluation small-signal S-parameters for a single value of $V_{\rm d}$ required a SPICE runtime of 2.9 seconds, leading to an overall extraction time for a full parametric sweep of about 75 seconds.

A representative scattering response of the computed parameterized macromodel is compared to the corresponding small-signal scattering response of the transistor-level netlist in Fig. 11. Also for this case, we see that an excellent accuracy is achieved for all values of the parameter $V_{\rm d}$ within the range of interest. The parameterized model has dynamic order 16, while numerator and denominator polynomial bases (15) have respectively degree three and two. Figure 12 shows the computed parametric correction source to be applied to the power supply port ($V_{\rm d}$) for DC compliance. Only the points marked with red squares (26 in total, linearly spaced in the parameter range of interest) were used for the macromodel identification, whereas the blue dots indicate additional 25 validation points used to verify the interpolation.

We now turn to the transient analysis of the synthesized parameterized macromodel. We excited port one of the LDO with a noisy signal obtained as a superposition of

- a Pseudo-Random Binary Sequence (PRBS) with period 10 μs, rise and fall time $\tau = 4$ μs, $V_{\rm min} = 1.23$ V and $V_{\rm max} = 1.25$ V;
- another 25 MHz PRBS of 3 mV amplitude;
- a 200 kHz tone of 4 mV amplitude;
- a 16 MHz tone of 2 mV amplitude;

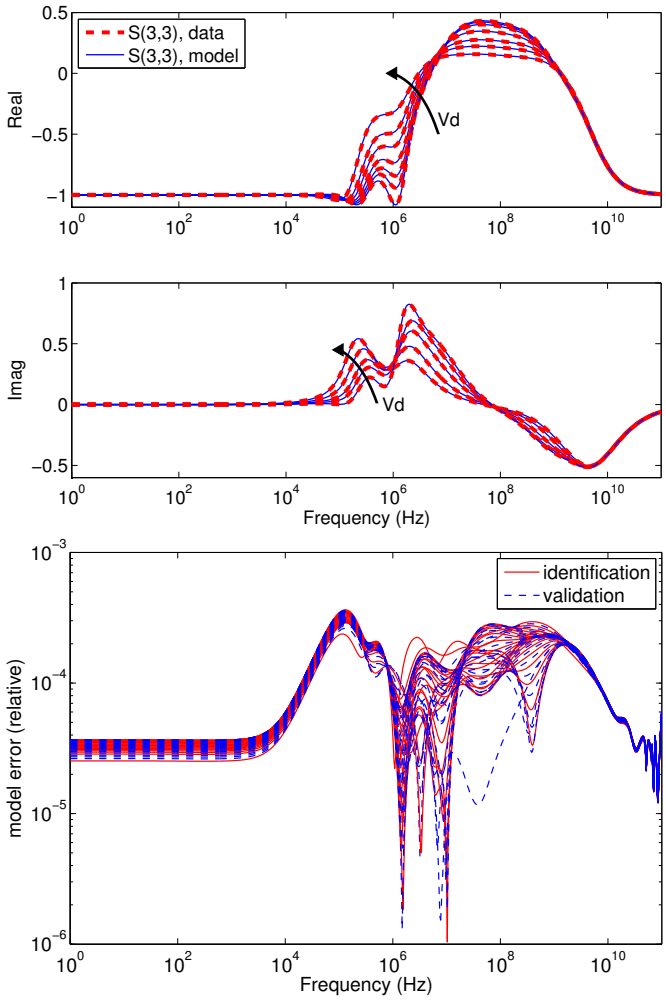

Fig. 11. Real (top panel) and imaginary (middle panel) part of S_{33} for the parameterized small-signal LDO model (blue solid lines) compared to the corresponding original responses (dashed red lines), plotted for different values of the parameter V_{d} ranging from 1.2 V to 1.7 V. The depicted S_{33} element is characterized by the largest variation induced by V_{d}. Bottom panel reports the corresponding relative approximation errors for all parameter grid values (both identification and validation).

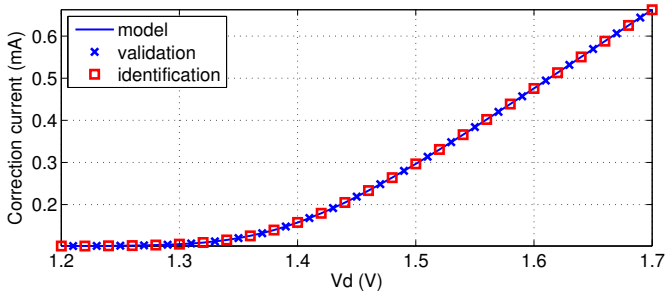

Fig. 12. Parametric DC current correction source at the power supply port V_{d} for the small-signal LDO model, plotted as a function of V_{d}. Similar results are obtained for the current correction sources on the other ports.

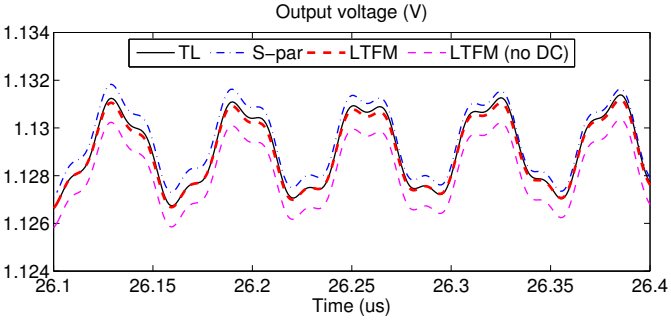

Fig. 13. Transient analysis results for the LDO circuit block excited by a noise signal at its input port, using different LDO models (see text).

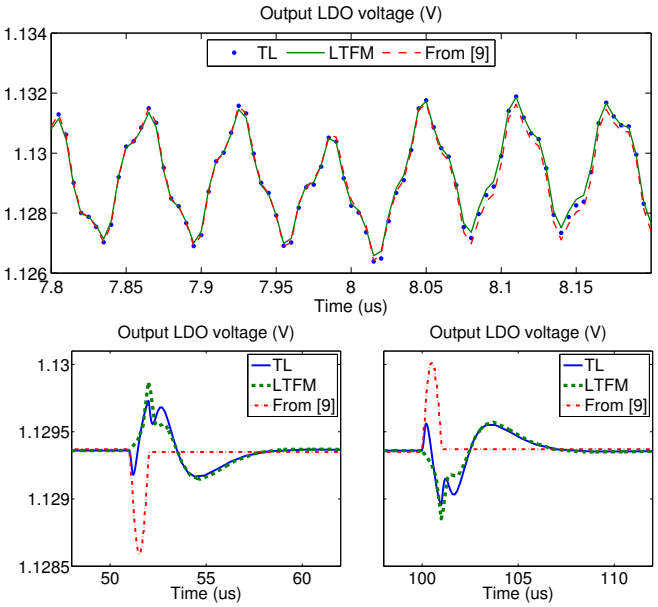

Fig. 14. Comparison between proposed macromodel and [9] for two different validation inputs. Top panel: noisy signal (see text); bottom panels: falling and rising transitions of a 10 kHz square wave.

- a 50 MHz tone of 1 mV amplitude;

with a random relative phase shift between the three tones. This signal is representative of the actual fluctuations that affect the input to the LDO during normal operation. Four different transient simulations were performed over a 500 μs time span, using the following different LDO models:

- the full transistor-level CB;
- the small-signal S-parameter model, run by feeding the circuit solver directly with the frequency samples; the adopted solver performs the transient analysis by direct convolution with the sampled impulse response obtained by inverse FFT;
- the proposed DC-corrected small-signal LTFM macromodel;
- the small-signal LTFM macromodel without DC correction.

A snapshot of the corresponding transient results is provided in Fig. 13, whereas the runtime required for each simulation and the corresponding speedup factors are reported in Table I. From these results, we note that the proposed macromodel

(whose construction required only 12 seconds) outperforms in terms of runtime the transistor level model, with a speedup of $80.8\times$. A significant speedup of $9.35\times$ is obtained also with respect to the direct use of S-parameter samples in the solver. Of course, since S-parameter samples are not parameterized, any new simulation with different parameter settings would require a new small-signal extraction. This step is not necessary with proposed parameterized macromodel, which just needs to be instantiated for the desired parameter configuration. Figure 13 also demonstrates that without DC correction the proposed model is incorrect (the corresponding root mean square error with respect to the TL results is $\epsilon_{\mathrm{RMS}} = 0.84$ mV, mainly due to the incorrect DC bias). The DC-corrected model is also more accurate ($\epsilon_{\mathrm{RMS}} = 0.10$ mV) than the direct S-parameter simulation ($\epsilon_{\mathrm{RMS}} = 0.21$ mV), mainly due to the discretization and preprocessing errors performed by the circuit solver in the computation of the impulse responses.

The proposed approach is now compared to the state of the art behavioral modeling technique [9]. The latter approach, as implemented in the software suite [38], constructs nonlinear macromodels starting from transient input and output sampled signals, with a prescribed degree of nonlinearity and dynamic order. Therefore, the objective is much more general and ambitious than ours. Nonetheless, we used the implementation [38] to derive a linear macromodel (dynamic order five) for the LDO, using a subset of samples from the transistor-level CB response to the above noisy input as identification signal. The top panel of Fig. 14 compares the two macromodel responses to a validation signal (a different subset of samples from the same noisy input). We see that the accuracy is good for both approaches.

A reduced dynamic order 5 was sufficient for the model from [9] since the input signal excites the system on a restricted frequency band. Therefore, we do not expect this model to be accurate for more general validation signals. This is in fact confirmed in the bottom panel of Fig. 14, where the macromodel responses are compared for a different input signal (a single 10 kHz square wave, exciting slower dynamics). The differences are now clearly visible. We could not succeed in enhancing the accuracy of the model [9] by increasing model order, essentially due to memory limitations in the identification process. This limitation may become severe when trying to model broadband dynamics from time sampled data, due to the very large number of required input/output samples. A frequency-domain identification as we suggest in this work is more robust and flexible in this case. We therefore conclude that our approach is more accurate and effective than [9] for the specific class of (linearized, broadband, and parameterized) models of our interest.

The real benefit of the proposed methodology should be addressed on complex system level simulation scenarios: replacing several CB with parameterized-LTFM can lead to a tremendous complexity reduction while preserving the accuracy of the simulation. This is illustrated by next example.

D. A system-level simulation testcase

This last example illustrates a common signal-integrity verification scenario, depicted in Fig. 15. The output from a

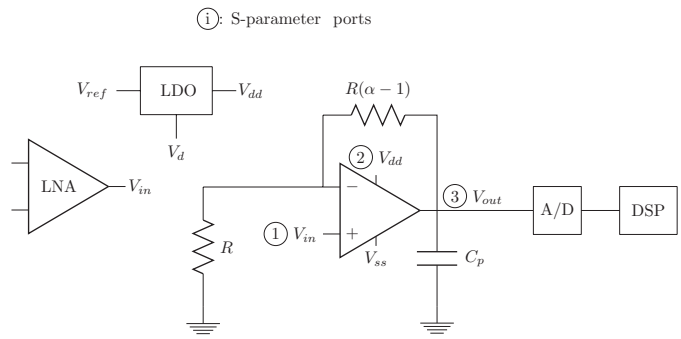

Fig. 15. A system-level simulation testcase.

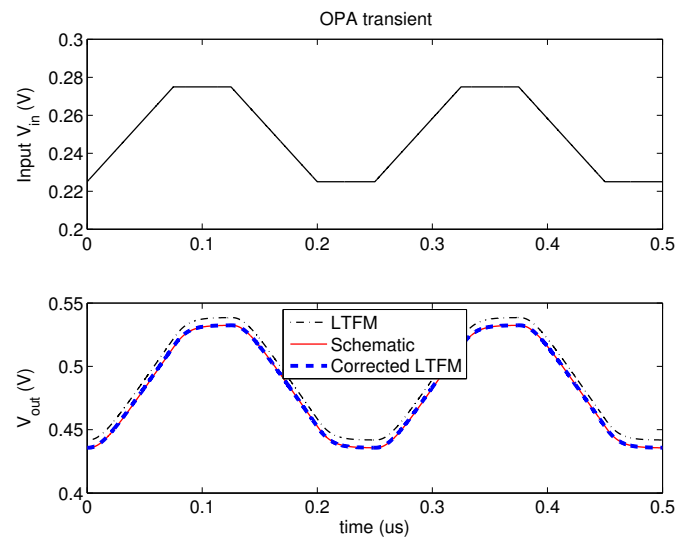

Fig. 16. Input (top) and output (bottom) signals for the OA in the configuration of Fig. 15.

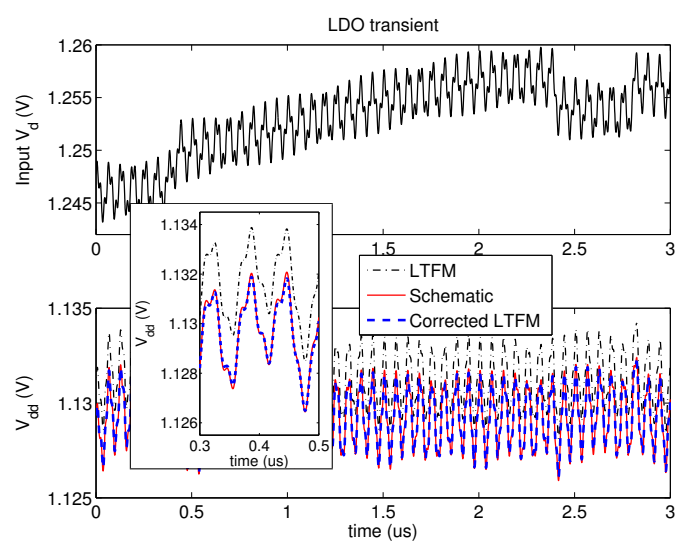

Fig. 17. Input (top) and output (bottom) signals for the LDO in the configuration of Fig. 15. Inner box provides a zoom on the fine features of the output responses.

differential LNA in a base-band receiver chain is amplified and filtered using an OA. Signal quality and noise rejection are of paramount importance since the analog output from the OA is fed to an A/D converter, whose output is passed to a Digital Signal Processing block. The main purpose of the LDO is to reject any broadband disturbances on its voltage input V_{d}, due to cross-talk or external noise sources. The output of the LDO must be a stable supply voltage V_{dd} for the OA. In order to verify the noise rejection properties of the full system, a multi-tone multi-amplitude aggressor signal is added to a 50 kHz, 20 mV PRBS and used as disturbance on the V_{d} input of the LDO. At the same time, we feed the input of the OA with a 4 MHz trapezoidal wave. We want to observe the induced variations on the supply voltage of the OA, as well as its output signal.

We processed both LDO and OA by the proposed parameterized small-signal macromodeling algorithm, producing two LTF models. The LDO model was as described in Sec. IV-C, whereas for the OA we used a dynamic order 11 with numerator and denominator polynomial bases with order one and two, respectively. These models were connected as in Fig. 15. We then performed a transient simulation up to 0.25 ms with a circuit solver using both the full transistor-level circuit blocks for all system parts, as well as replacing LDO and OA with their corresponding LTF macromodels. The full transistor-level simulation required 43 minutes, whereas the macromodel-based netlist required only 29 seconds. The corresponding $88\times$ speedup factor was achieved at no loss of accuracy, as demonstrated in Fig. 16 and Fig. 17. These figures show for the OA and the LDO the corresponding input signals at the OA noninverting input and at the LDO V_{d} input (top panels). Bottom panels show, respectively, the OA and the LDO output, by comparing the full transistor-level results with the LTFM results obtain by enabling and disabling the DC correction. The simulation with the DC-corrected LTFM models is able to reproduce with excellent accuracy the full transistor-level results.

V. Discussion, applicability, and limitations

A. Application scope and limitations

The modeling methodology presented in this paper is focused on those analog and RF circuit blocks which are designed to operate as linearly as possible in a specified operating region. Lots of design efforts are normally spent (especially in advanced CMOS technologies) to achieve a certain specified level of linearity and to suppress as much as possible frequency mixing or conversion effects in the prescribed operating range. To validate the limits of linear behavior, many simulation and measurement methods have been established and are adopted in industrial design flows; examples are third-order intercept point (IP_3), 1 dB compression point [10], or X-parameters [7]. Any circuit that complies with the local linearity assumption is a good candidate for the proposed modeling approach.

The design of a semiconductor system typically starts with the identification of smaller fundamental sub-blocks. For each sub-block, specifications and environmental/boundary conditions are given, fixed, and used as a reference for its design. Ad-hoc testbenches are setup and used to verify stability, linearity, gain and several other key figures of merit that are usually target of specification. Inevitably, in case a sub-block is used in different bias and/or load conditions, compliance to specifications and system functionality are not anymore guaranteed: changing the environment conditions would normally require a complete re-design of the sub-block and of any corresponding simulation models.

The above statements provide a clear scope for applicability of proposed approach: the linearized macromodels are not intended to represent the general behavior of a complex CB under arbitrary termination and simulation conditions; they are rather intended to speedup transient analysis within the well specified loading and biasing conditions that are required for the application at hand. We remark that the particular CB's that are considered in this work are usually analyzed by small-signal S-parameters. Our approach enables an efficient transient simulation of such devices, without having to extract their small-signal S-parameters and convert them to a transient simulation model for any new parameter instance. An example was discussed in Sec. IV-C, showing that our proposed approach leads to faster and more accurate transient simulations with respect to a direct use of S-parameter files in the circuit solver.

We finally remark that the proposed technique is applicable only when the small-signal dynamic behavior of the CB is characterized by a smooth dependence on the parameters, so that different biasing and operation modes admit a common model structure, as the adopted parameterized SK form. In particular, the assumption of a common dynamic order (number of poles) must be verified throughout the parameter space. If this assumption is violated, then alternative model structures should be used.

B. Port variables and parameters

Some remarks are in order about the parameters λ that the proposed models depend on. It should be emphasized that these parameters are intended and must be considered as static variables that, once instantiated, will never change during any transient simulation of the model. Let us consider for instance the *nominal* supply voltage V_{dd}, which is used as a parameter in several test cases. We consider V_{dd} as a parameter, since the devices of our interest are typically programmable by external digital control circuitry, that may decrease or increase the power supply, e.g., to reduce power consumption. The small-signal responses of the CB depend of course on the bias point induced by the particular value that is selected for V_{dd} within its admissible range $[V_{\mathrm{dd,min}}, V_{\mathrm{dd,max}}]$, defined in the simulation testbench. Our proposed model enables fast (small-signal) transient analysis of the CB at that prescribed bias point, which in turn is not intended to vary during the transient analysis. This is not to say that the voltage signal at the supply port $v_{\mathrm{d}}(t)$ is fixed and constant. We do model the small-signal variations of the $v_{\mathrm{d}}(t)$ signal around its nominal (fixed) value V_{dd} by means of a linearized transfer function model. Therefore, e.g. power integrity analyses are allowed, provided that the variation of the power supply voltage remains small

such that a linearized description is adequate. The last example of Sec. IV-D shows indeed a typical application scenario, where the nominal supply has a prescribed fixed value within the admissible range. A small-signal noise is injected and superimposed to the nominal supply voltage. Our linearized model is able to predict with good accuracy how such noise perturbations are mapped to the other circuit ports.

C. Global stability and passivity

A completely different scenario and a completely different modeling approach would be required if the parameters λ were time-varying as $\lambda(t)$, as a result of some feedback mechanism from the circuit block itself or from its terminations. Continuing on the example of the supply voltage, this situation would arise under large-signal operation, such that the splitting of the supply voltage $v_{\rm d}(t)$ into a fixed constant term $V_{\rm dd}$ plus small variations $\tilde{v}_{\rm d}(t)$ would not apply. In such case, a fully nonlinear modeling approach would be required, such as [4], [5], [7]–[9]. In particular, suitable care should be placed on the certification of global stability [9] and even global passivity, provided that the entire semiconductor system is characterized by the complete set of input and output signals at all ports at which it interacts with the environment.

A general solution to the problem of black-box nonlinear dynamic behavioral modeling (with stability and passivity constraints) is an extremely challenging goal, for which no satisfactory answer is yet available. However, special features of specific classes of structures may allow for problem simplification and approximate formulations, in terms of model representation and/or parameterization schemes, required number of degrees of freedom for tracking a particular variation (frequency of parameter domain), as well as identification algorithms, thus enabling ad hoc solutions for complexity reduction by behavioral modeling. This paper suggests indeed such an ad hoc solution.

The focus of this paper is on structures found in RF circuit blocks in wireless transceiver chains. Part of the feasibility analysis that is documented in the paper is indeed the verification that for typical structures in this class, the number of required basis functions (equivalently, the polynomial order for parameter-induced variation within the proposed macromodeling framework) is not excessive, due to the smoothness of the nonlinear maps being approximated. The same applies for the dynamical order (the number of poles). Should the class of structures under modeling change, so that abrupt nonlinearities arise, then different choices of basis functions or even different overall model structures will be in order.

The proposed macromodeling approach has another potential limitation. As discussed in Sec. III-G, it is relatively easy to enforce uniform stability of the macromodels throughout the parameter range of interest and within the boundary conditions enforced by their simulation testbenches. However, it may be conceivable that the stability of each specific macromodel is not sufficient to guarantee global stability in system-level simulations. In fact, even if the underlying transistor level netlist is verified to be stable within its simulation testbench, the small approximation errors that inevitably arise in the curve fitting process might lead to destabilization. Our only present possibility to prevent such situation is to keep these approximation errors small over a broad frequency band. Macromodel stability during transient analysis was verified a posteriori on a set of relevant examples, but no explicit conditions were enforced in the construction of the macromodel in order to prevent destabilization.

The occurrence of instability in a transient analysis is strongly dependent on all terminations providing feedback into the macromodel ports. For the simpler case of linear interconnect modeling, passivity conditions on each individual model are sufficient to guarantee global stability, hence the interest in linear passivity enforcement schemes in the last few years [16]–[19]. In the present context, where multiple macromodels of nonlinear possibly active blocks can be interconnected, more sophisticated and specialized conditions must be enforced during the construction of macromodel, see e.g. the initial investigations in [9]. Moreover, existing results that are commonly used in robust control design, such as the Small Gain Theorem [36], are too conservative to be applied in this context. As a conclusion, the problem of global stability enforcement in nonlinear macromodeling is definitely open and requires major future research efforts.

VI. Conclusion

This paper presented a systematic methodology for the extraction of compact parameterized small-signal macromodels of complex circuit blocks typically found in Mixed-Signal and RF applications, and designed to operate as linearly as possible around prescribed operating points. Such local linearity assumptions are verified during the circuit design process by means of dedicated testbenches, in which bias and load boundary conditions are opportunely set. Thanks to an explicit constraint on the DC response and to the inclusion of parameterized DC correction sources, the proposed macromodels can seamlessly replace the corresponding transistor level schematics in system-level Signal and Power Integrity verifications, leading to a significant speedup in the computing time required by transient simulations.

The feasibility of the proposed approach was demonstrated on two simple academic examples (a single transistor and a two-stage buffer from a state-of-the-art CMOS technology) as well as on a complex circuit model of a Low Dropout voltage regulator, taken from a real 3G transceiver design. The availability of accurate and efficient macromodels is a key enabling factor for comprehensive system verification, allowing a fast systematic analysis of the large number of configurations and operation modes required by modern digitally-programmable systems.

References

[1] R. J. Baker, "CMOS Mixed-Signal Circuit Design", *IEEE Press Series on Microelectronic Systems*, $2^{\rm nd}$ ed., Hoboken, NJ:Wiley, 2008.

[2] B. Razavi, *RF microelectronics*, $2^{\rm nd}$ ed., Upper Saddle River, NJ:Prentice Hall, 2011.

[3] M. H. Zaki, S. Tahar, and G. Bois, "Formal Verification of Analog and Mixed Signal designs: a survey", *Microelectronics Journal*, vol. 39, no. 12, pp. 1395–1404, Dec. 2008.

[4] S. Boyd and L. O. Chua, "Fading memory and the problem of approximating nonlinear operators with Volterra series," *IEEE Transactions on Circuits and Systems*, Vol. 32, No. 11, pp. 1150–1161, Nov. 1985.

[5] J. C. Pedro and S. A. Maas, "A comparative overview of microwave and wireless power-amplifier behavioral modeling approaches," *IEEE Transactions on Microwave Theory and Techniques*, Vol. 53, No. 4, pp. 1150–1163, Apr. 2005.

[6] L. Ljung, *System Identification, Theory for the User, 2nd ed.*, Englewood Cliffs, NJ: Prentice Hall, 1999.

[7] J. Verspecht and D. E. Root, "Polyharmonic distortion modeling," *IEEE Microw. Mag.*, Vol. 7, No. 3, pp. 44–57, June 2006.

[8] F. Filicori, G. Vannini, and V. A. Monaco, "A nonlinear integral model of electron devices for HB circuit analysis," *IEEE Transactions on Microwave Theory and Techniques*, Vol. 40, No. 7, pp.1456–1465, Jul. 1992.

[9] B. N. Bond, Z. Mahmood, Li Yan, R. Sredojevic, A. Megretski, V. Stojanovic, Y. Avniel, and L. Daniel, "Compact Modeling of Nonlinear Analog Circuits Using System Identification via Semidefinite Programming and Incremental Stability Certification," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, Vol. 29, No. 8, pp. 1149–1162, Aug. 2010.

[10] S. C. Cripps, *RF Power Amplifiers for Wireless Communications*, Norwood, MA:Artech House, 1999.

[11] T. Dobrowiecki and J. Schoukens, "Linear Approximation of Weakly Nonlinear MIMO Systems," *IEEE Transactions on Instrumentation and Measurement*, Vol. 56, No. 3, pp. 887–894, June 2007.

[12] Y. Rolain, W. Van Moer, R. Pintelon, and J. Schoukens, "Experimental Characterization of the Nonlinear Behavior of RF Amplifiers," *IEEE Transactions on Microwave Theory and Techniques*, Vol. 54, No. 8, pp. 3209-3218, Aug. 2006.

[13] B. Gustavsen and A. Semlyen, "Rational approximation of frequency domain responses by vector fitting", *IEEE Transactions on Power Delivery*, vol. 14, no. 3, pp. 1052-1061, Jul. 1999.

[14] S. Grivet-Talocia and M. Bandinu, "Improving the convergence of vector fitting for equivalent circuit extraction from noisy frequency responses," *IEEE Trans. on Electromagnetic Compatibility*, vol. 48, no. 1, pp. 104–120, Feb. 2006.

[15] D. Deschrijver, B. Haegeman, and T. Dhaene, "Orthonormal Vector Fitting: A Robust Macromodeling Tool for Rational Approximation of Frequency Domain Responses," *IEEE Transactions on Advanced Packaging*, vol. 30, no. 2, pp. 216–225, May 2007.

[16] S. Grivet-Talocia, "Passivity Enforcement via Perturbation of Hamiltonian Matrices" , *IEEE Trans. Circuits and Systems I: Fundamental Theory and Applications*, vol. 51, no. 9, pp. 1755-1769, Sep. 2004.

[17] D. Saraswat, R. Achar, and M. Nakhla, "Global Passivity Enforcement Algorithm for Macromodels of Interconnect Subnetworks Characterized by Tabulated Data," *IEEE Transactions on VLSI Systems*, vol. 13, no. 7, pp. 819–832, July 2005.

[18] C. P. Coelho, J. Phillips, and L. M. Silveira, "A Convex Programming Approach for Generating Guaranteed Passive Approximations to Tabulated Frequency-Data," *IEEE Trans. Computed-Aided Design of Integrated Circuits and Systems*, vol. 23, no. 2, pp. 293–301, Feb. 2004.

[19] B. Gustavsen and A. Semlyen, "Enforcing passivity for admittance matrices approximated by rational functions," *IEEE Trans. Power Systems*, vol. 16, no. 1, pp. 97–104, Feb. 2001.

[20] S. Grivet-Talocia, P. Brenner, and F. G. Canavero, "Fast Macromodel-based Signal Integrity Assessment for RF and Mixed-Signal Modules," *IEEE International Symposium on Electromagnetic Compatibility, Honolulu, Hawaii (USA)*, 8–13 July 2007, pp. 1-6.

[21] S. B. Olivadese, P. Brenner, and S. Grivet-Talocia, "DC-Compliant Small-Signal Macromodels of Non-Linear Circuit Blocks", Proc. of 17th *IEEE Workshop on Signal and Power Integrity (SPI)*, Paris (France), May 12–15, 2013, pp. 1–4.

[22] P. Triverio, "Self Consistent, Efficient and Parametric Macromodels for High-speed Interconnects Design", Ph.D. Thesis, Politecnico di Torino, Italy, April 2009.

[23] S. Grivet-Talocia, S. Acquadro, M. Bandinu, F. G. Canavero, I. Kelander, and M. Rouvala, "A parameterization scheme for lossy transmission line macromodels with application to high speed interconnects in mobile devices," *IEEE Trans. Electromagnetic Compatibility*, vol. 49, no. 1, pp. 18–24, Feb. 2007.

[24] P. Triverio, S. Grivet-Talocia, and M.S. Nakhla, "A Parameterized Macromodeling Strategy with Uniform Stability Test," *IEEE Transactions on Advanced Packaging*, vol. 32, no. 1, pp. 205-215, Feb. 2009.

[25] P. Triverio, M. Nakhla, and S. Grivet-Talocia, "Parametric Macromodeling of Multiport Networks from Tabulated Data," *IEEE 16th Topical Meeting on Electrical Performance of Electronic Packaging (EPEP 2007)*, Atlanta (GA), USA, Oct. 29–31, 2007, pp. 51–54.

[26] P. Triverio, S. Grivet-Talocia, M.S. Nakhla, F. Canavero, and R. Achar, "Stability, causality, and passivity in electrical interconnect models", *IEEE Transactions on Advanced Packaging*, vol. 30, no. 4, pp. 795–808, Nov. 2007.

[27] E. R. Samuel, L. Knockaert, F. Ferranti, and T. Dhaene, "Guaranteed Passive Parameterized Macromodeling by Using Sylvester State-Space Realizations", *IEEE Transactions on Microwave Theory and Techniques*, vol. 61, no. 4, pp. 1444-1454, Mar. 2013.

[28] F. Ferranti, T. Dhaene, and L. Knockaert, "Compact and Passive Parametric Macromodeling Using Reference Macromodels and Positive Interpolation Operators," *IEEE Transactions on Components, Packaging and Manufacturing Technology*, vol. 2, no. 12, pp. 2080–2088, Dec. 2012.

[29] F. Ferranti, L. Knockaert, and T. Dhaene, "Passivity-Preserving Parametric Macromodeling by Means of Scaled and Shifted State-Space Systems," *IEEE Transactions on Microwave Theory and Techniques*, vol. 59, no. 10, pp. 2394–2403, Oct. 2011.

[30] F. Ferranti, L. Knockaert, T. Dhaene, and G. Antonini, "Passivity-Preserving Parametric Macromodeling for Highly Dynamic Tabulated Data Based on Lur'e Equations," *IEEE Transactions on Microwave Theory and Techniques*, vol. 58, no. 12, pp. 3688–3696, Dec. 2010.

[31] L. O. Chua, C. A. Desoer, and E. S. Kuh, "Linear And Non Linear Circuits," New York:McGraw-Hill, 1987.

[32] K. Singhal and J. Vlach, "Symbolic Analysis of Analog and Digital Circuits," *IEEE Trans. Circuits Syst.*, vol. CAS-24, no. 11, pp. 598–609, Nov. 1977.

[33] A. I. Khuri and S. Mukhopadhyay, "Response surface methodology," *WIREs Comp. Stat.*, vol. 2, pp. 128–149, Mar/Apr 2010.

[34] C. K. Sanathanan and J. Koerner, "Transfer function synthesis as a ratio of two complex polynomials," *IEEE Trans. Automatic Control*, vol. 8, no. 1, pp. 56–58, Jan. 1963.

[35] T. Kailath, *Linear Systems*, Englewood Cliffs, NJ, USA: Prentice-Hall, 1980.

[36] K. Zhou, J. C. Doyle, and K. Glover, *Robust and optimal control*. Upper Saddle River, NJ, USA: Prentice-Hall, 1996.

[37] S. Xu and J. Lam, *Robust Control and Filtering of Singular Systems*, Lecture Notes in Control and Information Sciences, vol. 332, Berlin, Germany:Springer, 2006.

[38] *STINS: A MATLAB tool for stable identification of nonlinear systems via semidefinite programming* [Online]. Available: http://www.rle.mit.edu/cpg/codes/stins

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