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Doctoral Program in Electronic and Communication Engineering

Final Dissertation

Analog-Digital System Modeling for Electromagnetic Susceptibility Prediction

A case study : Integrated Circuits and Communication Networks in Aerospace Environment

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Abstract

The thesis is focused on the noise susceptibility of communication networks. These analog-mixed signal systems operate in an electrically noisy environment, in presence of multiple equipments connected by means of long wiring. Every module communicates using a transceiver as an interface between the local digital signaling and the data transmission through the network. Hence, the performance of the IC transceiver when affected by disturbances is one of the main factors that guarantees the EM immunity of the whole equipment. The susceptibility to RF and transient disturbances is addressed at component level on a CAN transceiver as a test case, highlighting the IC features critical for noise immunity.

A novel procedure is proposed for the IC modeling for mixed-signal immunity simulations of communication networks. The procedure is based on a gray-box approach, modeling IC ports with a physical circuit and the internal links with a behavioural block. The parameters are estimated from time and frequency domain measurements, allowing accurate and efficient reproduction of non-linear device switching behaviours. The effectiveness of the modeling process is verified by applying the proposed technique to a CAN transceiver, involved in a real immunity test on a data communication link. The obtained model is successfully implemented in a commercial solver to predict both the functional signals and the RF noise immunity at component level.

The noise immunity at system level is then evaluated on a complete communication network, analyzing the results of several tests on a realistic CAN bus. After developing models for wires and injection probes, a noise immunity test in avionic environment is carried out in a simulation environment, observing good overall accuracy and efficiency.

Acknowledgements

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I would also like to thank Prof. Canavero, the advisor of this thesis, for allowing me to carry out my PhD research activity at Politecnico di Torino. His encouragement and support throughout the development of the activity were a relevant factor during my Ph.D. I also wish to thanks the whole EMC Group for making my time an interesting and enjoyable working experience. In particular, I am very grateful to Luca Rigazio and Prof. Ivano Maio for their help in the test measurements carried out in the research lab.

Finally, i would like to thank Dr. Todd Hubing for giving me the possibility of spending four months at the Clemson University International Center for Automotive Research (CUICAR), Greenville, SC, USA. His guidance and his profound experience on PCBs and integrated circuits were invaluable for my work and allowed me to significantly progress in the research development with the analysis of the transient noise effects on a IC in the Clemson Vehicular Electronics Laboratory.

Contents

Chapter 1

Introduction

Electromagnetic Compatibility (EMC) is defined as the ability of an equipment or a system to perform satisfactorily in its electromagnetic environment without introducing intolerable interference into any other electrical apparatus in that environment. The electromagnetic compatibility concerns two main phenomena, that are the emission of spurious noise and the susceptibility, either conducted or radiated.

The electromagnetic compatibility is a key factor in the design of electronic systems and equipments. In the past few years the ability of Integrated Circuits (IC) to safely operate in an environment of increasing interferences from radio frequencies has been reduced. Concerns related to EMC increased when low emission and high immunity to radio-frequency interference (RFI) signals appeared as performance factors in integrated circuits. The evolution of electronic components parameters required deep understanding of sources affecting EMC of electronic systems. The increasing complexity of ICs associated with growing problems related to immunity and emission led to the development of susceptibility and emission models. The models are used not only by IC manufacturers to check if components pass EMC specifications, but also by users to test the EMC at system level. The development of a model reproducing the EMC behavior of a component is a real challenge, since it must be sufficiently specific and compatible with simulations proposed by the most common tools. In most cases, the validity of EMC models is based on the quality of the characterization of certain parameters. EMC characterization requires knowledge in terms of methodology and EMC standards.

The measurement standards provide methods to extract the emission spectrum and susceptibility level, either conducted or radiated in integrated circuits. Integrated circuits, with system internal oscillations, are important sources of electromagnetic pollution, attacking certain frequency bands by means of conducted or radiated coupling and considerably degrading wireless communications and even endangering the security of some systems.

This thesis focuses on the IC modeling of electromagnetic immunity, analyzing the effects of interferences on analog and digital circuits. In particular, the main topic is the analysis of ICs used in communication networks and buses, as their use is often required in noisy environments where high levels of electromagnetic interference (EMI) affects the usual functionality. The IC performance is assessed firstly at component level and afterwards at equipment level according to official standards depending on the context in which they are used. The development of a

novel procedure to model the behaviour of complex mixed-signal ICs will be proposed to take into account the susceptibility features in a simulation environment. The goal of the activity is to be able to simulate the robustness to noise of a complete communication system. The obtained voltage and current signals are computed under the noise stress and used by the designer to evaluate the system performance, checking the compliace to official standards in an early design phase.

The activity was carried out in the EMC Group of the Department of Electronics and Telecommunication of Politecnico di Torino, Italy. EADS Innovation Works (IW) financed the research and several tests in avionic environment were done in the EADS IW labs in Toulouse, France. Furthermore, the activity related to the immunity analysis towards transient noise has been done in Clemson Vehicular Electronics Laboratory (CVEL) of Clemson University International Center for Automotive Research (CUICAR) located in Greenville, SC, USA.

1.1 Outline of the Thesis

The outline of this thesis is as follows.

In Chapter 2, EMC-related features of ICs are considered. The technological trend, the strong scaling of IC parameters and the reduced noise margins are highlighted as a main reason for the growing EM emission and susceptibility problems. The main effects of EMI on digital designs are highlighted and the test setups for measuring IC susceptibility to RF and transient noise are detailed. Afterwards, a summary of the available IC models for immunity characterization is presented.

Chapter 3 outlines a thorough analysis of the IC immunity in communication networks at component level. The IEC characterization of a Controller Area Network (CAN) transceiver performance when affected by noise is detailed and carried out on several ICs as a test case. The impact of RF and transient noise on CAN bus is evaluated analyzing non-linearities and the non-idealities limiting common-mode noise rejection.

In Chapter 4, a novel modeling procedure based on an Analog Mixed-Signal (AMS) block structure is described, for the generation of IC immunity models from real measured data. Its accuracy is validated on a CAN transceiver model, comparing the immunity threshold obtained from measurements with simulation data.

In Chapter 5, the CAN network susceptibility to RF noise is addressed at system level. Shielded twisted wires are characterized as transmission lines and their impact on the global system immunity is analyzed in different test setups. Modeling the noise injection capability of an injection probe, the immunity of a CAN bus is evaluated by simulation and validated with measurements.

Chapter 6 provides the main conclusions that can be drawn from the results of this Thesis.

Chapter 2

EMC of Integrated Circuits

The design of electronic systems becomes more and more complex. The push for functionality is ever increasing, while cost and time-to-market should be kept as low as possible. At the same time, as technology advances, new challenges show up, also because the environment in which the equipment is supposed to operate becomes harsher. In modern equipments the functionality is embedded in one or more integrated circuits through the use of analog and digital electronic circuits. Substrate noise modeling and EMI have become dominant noise sources in mixed-signal designs.The root cause of any failure due to susceptibility can be always brought back to an electronic component being unable to withstand the interference. In the following sections, a research upon state-of-the-art EMC topics related to integrated circuits is presented.

2.1 Integrated circuit parameters

In the past few years, an evolution of physical and electrical parameters of electronic components has occurred. A research [1] collected informations and trends about integrated circuit technology. The results are summarized in the International Technology Roadmap for Semiconductor (ITRS,[2]), which provides very detailed insight into the evolution of the microelectronics industry, highlighting trends, technology targets, and milestones for the next 15 years. It also describes the evolution of EMC problems in the years to come with the technological evolution of semiconductors and electric parameters. Another road-map focuses on design automation tools with a chapter related to EMC [3]. From these road-maps, a subset of parameters and associated trends has been extracted, focusing on the processor frequency, gate currents, I/O trends, and noise margin evolution.

2.1.1 Technology and Frequency

Studies on semiconductor technology have shown significant advancement on the next technological steps of ICs. Fig. 2.1 shows IC technology scale-down over the next years for high-performance microprocessors and cost-performance microcontrollers. It can be seen that the embedded microcontrollers use technologies nearly five years after their introduction in high-end microprocessors. This technological reduction related to MOS channel length follows a linear

trend. High performance microprocessor technology in a decade passed from 0.13 μm in 2000 to 32 nm in 2010. In the same time microcontrollers passed from 0.35 μm to 90 nm. With each lithography scaling step, the linear dimensions are reduced approximately by a factor of 0.7 such that the silicon area is reduced by a factor of 2. By 2022, the ITRS road map projects the minimum physical gate length of transistors to be close to 7 nm, which is considered by most researchers to be the physical limit of silicon.

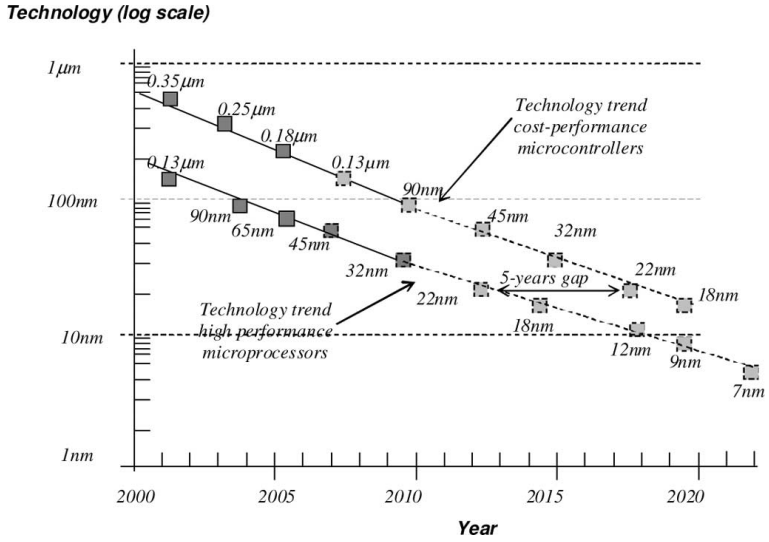

Figure 2.1. Technology scale-down toward nano-scale devices associated with microprocessor and microcontroller manufacture [2]

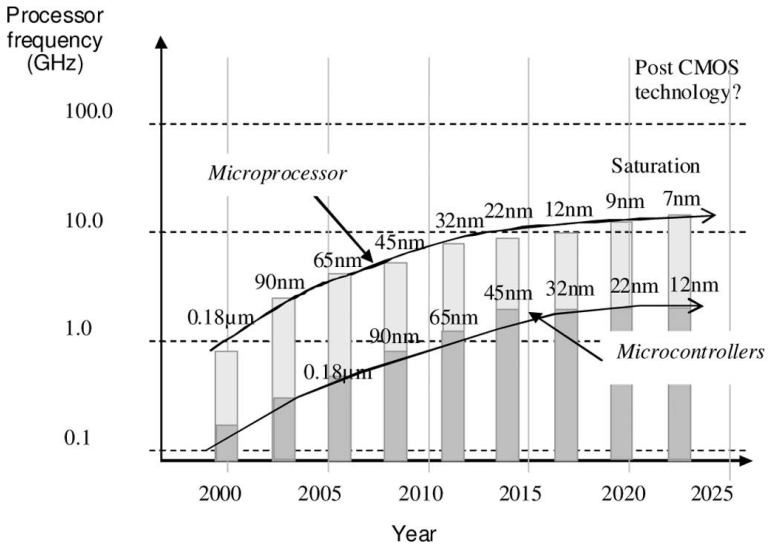

Figure 2.2. Microprocessor and microcontroller frequency increase until 2020 [2].

The microprocessor frequency depends on the channel length of IC transistors, therefore their

speed increases with technology scale-down. Fig. 2.2 shows the frequency evolution of microcircuits according to the technological dimensions.

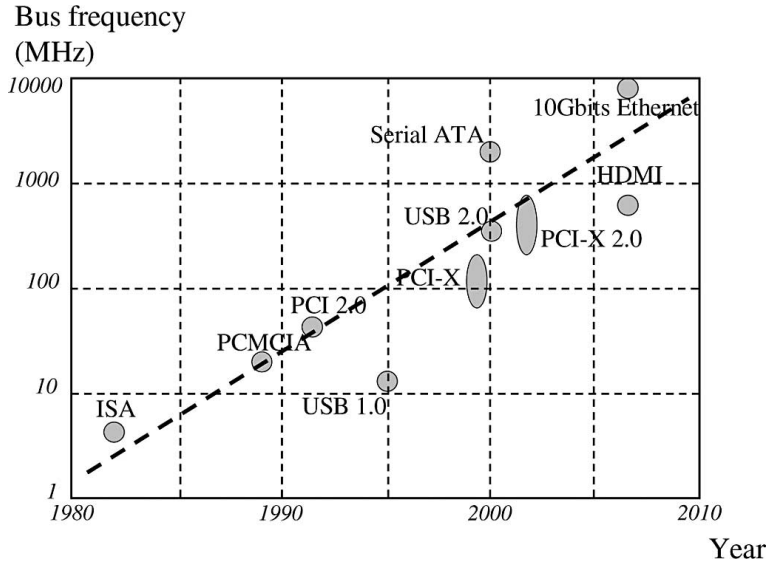

Figure 2.3. Frequency increase of data bus transfer [2].

According to ITRS 2007, the on-chip clock frequency is increasing (14 GHz predicted for 2012) as well as the communication speed between chips. To reach these higher speeds and reduce power requirements, ICs are designed with transistors that require less supply voltage (0.5 V in 2022) to lower the power consumption. As logic thresholds reduce accordingly, the noise margin is going down, resulting in more vulnerability to EMI. By 2022, processors are expected to run at 20 GHz; the saturation scenario considers several limiting factors such as MOS mobility degradation, interconnect delay, and power dissipation. Parallel architectures may compensate for these limitations while maintaining the pace in performance improvements.

The frequency increase also concerns the data transfer between ICs, as shown in Fig. 2.3. Universal Serial Bus (USB), Peripheral Component Interconnect (PCI), and serial Advanced Technology Attachment (ATA) protocols have been developed to operate around 1 GHz while new protocols approaching 10 GHz have been specified with an increased bandwidth to support ultrahigh-speed data transfer.

2.1.2 IC current and I/O ports

The technology evolution of semiconductors leads to a reduction of gate currents; as shown in Table 2.1, switching currents decrease with the smaller size of channel transistor. Intrinsically, this should have a positive impact on the transient switching noise. However, the steady increase in IC complexity, power consumption, and faster switching speeds jeopardizes these benefits in terms of *di/dt* noise. Even if peak current amplitude consumed by a gate is constantly decreasing, the number of simultaneously switching gates increases especially when many functions are working in parallel on the same circuit. In high density circuits such as microprocessors, hundreds of

thousands gates switch at the same time, causing high amplitude current peaks. Moreover, starting with 90-nm technology, chips with more than 1000 I/Os may be designed. The simultaneous switching of active buffers may thus be the dominant contributor to parasitic emissions. Fig. 2.4 shows the evolution of the maximum number of I/Os per chip, which follows a quasi-exponential law. An accurate evaluation of I/O behavior and its transient current consumption are of utmost importance for emission and immunity prediction.

Technology	External supply (V)	Average Current (A)	Gate density (/mm^2)	Gate current peak (mA/gate)	Capacity (fF/gate)
1.2 µm (1985)	5 V	<1	8 K	1.1	60
0.8 µm (1990)	5 V	<1	15 K	0.9	40
0.5 µm (1993)	5 V	3	28 K	0.75	30
0.35 µm (1995)	5-3.3 V	12	50 K	0.6	25
0.25 µm (1997)	5-2.5 V	30	90 K	0.4	20
0.18 µm (1999)	3.3-2.0 V	50	160 K	0.3	15
0.12 µm (2001)	2.5-1.2 V	150	240 K	0.2	10
90 nm (2004)	2.5-1.0 V	186	480 K	0.1	7
65 nm (2006)	2.5-0.7 V	236	900 K	0.07	5
45 nm (2008)	1.8-0.8 V	283	2000 K	0.05	3

Table 2.1. Evolution of key parameters versus technology node [2].

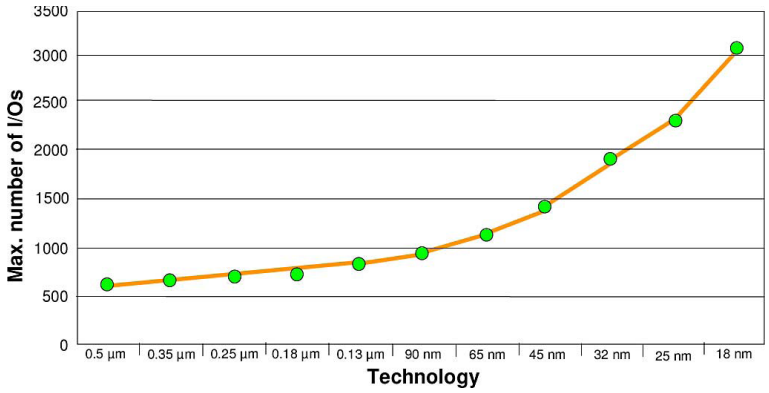

Figure 2.4. Maximum number of I/Os in ICs [2].

2.1.3 Power supply voltage

The trend in terms of IC technology is the steady decline of supply voltages. In Fig. 2.5, variation of supply voltages in future technologies is shown. The external I/O supply, which represents the nominal voltage of the technology,varies step by step (5 V, 3.3 V, 2.5 V, 1, 8 V). The supply voltage decreases with technology scale-down from 5 V to 1 V in 90 nm; the reduction of noise margin associated with lower supply voltages is noticed. The noise margin has been reduced by a factor of 10 in 20 years and goes below 100 mV in 2015. The power supply voltages of integrated circuits are steadily reduced in order to reduce the consumption of the circuits and to allow the reduction of oxide thickness and hence increased switching speeds. The supply voltages of integrated circuits do not decrease at the same rate as the reduction in the size of transistors for two reasons: the threshold voltage of transistors decreases with increasing leakage current and voltage levels are standardized to ensure the compatibility between interconnected systems or circuits. A reduced noise margin means an increased sensitivity to external interference.

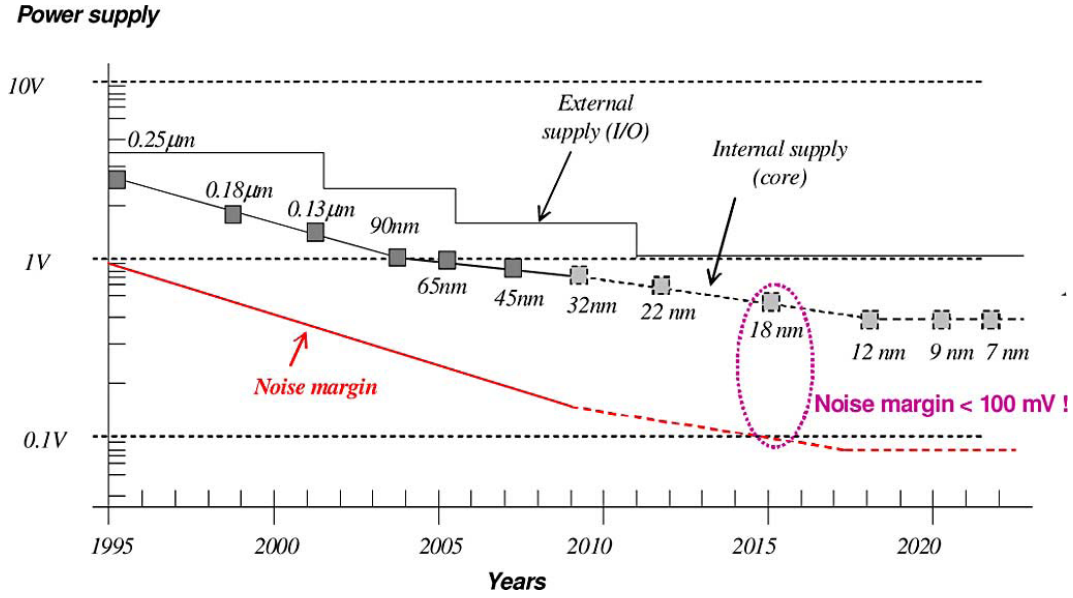

Figure 2.5. Continuous decrease of power supply voltages [2].

2.2 EM emissions

The EM spurious emissions arise in electronic components from the current used during switching of elementary circuits such as inverters. The evolution of transistor technologies and the abundance of elementary circuit logic within the electronic components involve greater power consumption and increased noise. The performances of microprocessors, using multiple clocks with different frequencies, and of ICs at higher operating frequencies create spurious emission spectra towards the high frequencies which could disrupt sensitive applications. Assessments were done on integrated circuit improvements expected for the next years and spurious emission levels until 2020

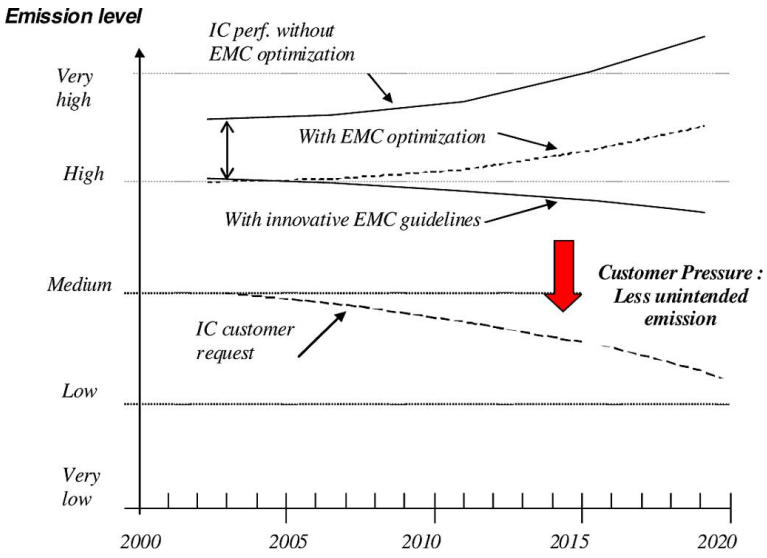

Figure 2.6. Evolution of the peak emission level over the last few years and projection until 2020 [1].

are shown in Fig. 2.6, given the requirements of both IC manufacturers and customers. Without any EMC optimization strategy, the parasitic emission will increase in the next years. IC users show a strong demand for fabrication of electronic devices with low emissions. Integrated circuits built without EMC optimization suffer from high noise emissions and require decoupling capacitors, protection and filtering at the circuit board. In early 2000, the gap was reduced by almost 20 dB between noise emissions levels of EMC non-optimized ICs and those that incorporate new EMC design rules. Without EMC optimization, the technology trend toward more complex and faster designs is expected to lead to increased emission levels (Fig. 2.6, upper curve). Although EMC optimization techniques have partially filled the gap between IC customer requests and IC performance (Fig. 2.6, middle curve), new innovative techniques need to be investigated to compensate for the induced parasitic effects of technology scale-down. In 2020, the required efficiency of these techniques should allow a reduction in unintended emissions of 40 dB. Despite these continuous efforts, there is a gap between IC customer requests and intrinsic IC performance. Not only do generic low-emission design guidelines need to be generalized and integrated in design flows, but advanced design techniques should also be applied to respond to IC customer pressure for less conducted and radiated noise.

2.3 EM susceptibility in integrated circuits

The origin of IC susceptibility lies in many physical phenomena. The use of radio link and integrated circuits more or less noisy generates an electromagnetic field in a non-negligible space where many critical electronic components can be found; conducted and radiated disturbances are transformed into currents and voltages in integrated circuits, which can cause malfunction or even destruction. The main sources of electromagnetic fields are natural, such as lightnings, or produced by other electronic components such as equipment, mobile phones, radar sources and

wireless base stations that can generate RF interference in integrated circuits. EM disturbances can be classified according to their energy levels and their frequency bands. As it is explained later in the document, disturbances act in different ways according to if their fundamental frequency is included or not in the operating bandwidth of the integrated circuit.

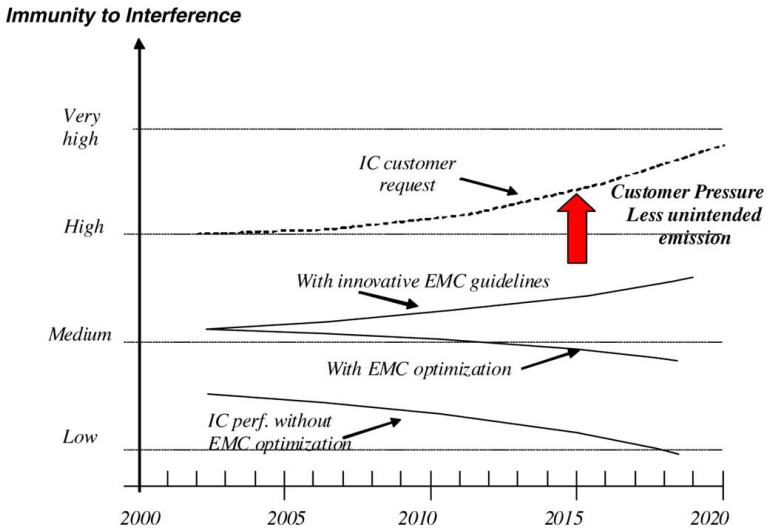

Figure 2.7. Diverging trends between IC immunity requirements and increased susceptibility with technology improvements [1].

The technological trend toward lower noise margins, the growing integration of I/O structures and higher bus speeds should lead to increased susceptibility of integrated circuits for radio frequency interference. Fig. 2.7 shows the different trends in the evolution of IC susceptibility: customer requirements and IC performance with and without EMC optimization. The actual level of IC immunity, without EMC performance, is low and tends to decline in the years to come. With the application of EMC design rules an increase in component immunity is expected in the future. Generic high-immunity design guidelines should be introduced in design flows, as a response to IC customer pressure for higher immunity.

2.3.1 Noise margins

The reduction of supply voltages in MOS technology has a direct impact on the inner workings of digital ICs, particularly regarding thresholds of logic gates. Each MOS circuit technology operates according to a standard voltage levels for I/O, which represent the two logic states. The voltage levels associated with each state accept a tolerance zone limited by specified voltages: V_{IH} and V_{OH} for high logic state and V_{IL} and V_{OL} for low logic state. In order to guarantee nominal operation of the circuit, the definition of switching zones must comply with rules assuring a certain immunity to noise. The noise margins are directly related to circuits supply voltages, meaning that they depend on the evolution of MOS technologies. Fig. 2.5 compares threshold levels of different CMOS technologies. Table 2.2 shows the evolution of high level noise margins (NM_H) and low level noise margins (NM_L) for digital design technologies. It is clear that the constant decline in

noise margins makes integrated circuits more sensitive, significantly increasing the susceptibility of electronic components.

Technology	V_{OH}	V_{IH}	NM_H	V_{IL}	V_{OL}	NM_L
CMOS 5V	4.44V	3.5V	0.94V	1.5V	0.5V	1V
CMOS 2.5V	2.3V	1.7V	0.6V	0.7V	0.2V	0.5V
CMOS 1.8V	1.2V	1.17V	0.03V	0.7V	0.45V	0.25V

Table 2.2. Noise margin evolution in CMOS technology

2.3.2 Perturbation effects on digital circuits

Digital integrated circuits are inherently less susceptible to EM interference than their analog counterparts: a natural resistance against EM disturbances is given by voltage thresholds between logic levels, leading to a higher immunity to interferences; however this does not mean that they are completely immune to it. EMI has been observed to have two distinct effects on digital devices [4, 5, 6]. The first one is false switching or static failure, which occurs when interference is of sufficient amplitude to cause an otherwise static logic signal to appear to change state. The second effect is that of EMI-induced delays. It has been observed that significant changes in the propagation delay of a device occur at much lower amplitudes of EMI than those that cause false switching. These changes lead to violations of critical timing constraints, such as the minimum set-up and hold times of flip-flops, which are referred as dynamic failure. Unlike static failures, dynamic failures are dependent on the phase of the EMI relative to a logic transition. In a worst case situation, depending on the total EMI level, digital integrated circuits can fail a complete data transmission because some significant bits were permanently flipped into another state owing to a particularly strong EMI injection. Nevertheless, as long as realistic EMI levels are considered and if some basic precautions are taken in order to reduce and prevent the injection of EMI into the circuit, digital ICs exhibit a higher immunity to EMI than analog ones, because of their threshold levels.

The coupling of an interference with a circuit may lead to different results and their effects are classified according to electrical and physical damages they provoke:

- Single error: the disturbance signal is interpreted as a valid logic input and a wrong output signal is generated [7].
- Repeated error: the disturbance signal is continuously applied on the circuit leading to a long-term degradation.
- Irreversible error: the circuit is driven by an interference signal into an instable state where chaos phenomena are observed [8].
- Physical damage: high-power transient signals can provoke physical damages in the circuit such as cracks or melted components; Elecro-static discharges cause such type of harm due to localized heating which melts certain circuit elements [9].

In the following sections, examples of digital errors due to harmonic signal interferences are shown, obtained from HSpice simulation of a TI SN74AHC04 buffered inverter model; errors are characterized visualizing the output signal with and without superimposing disturbance in the input port.

Static errors

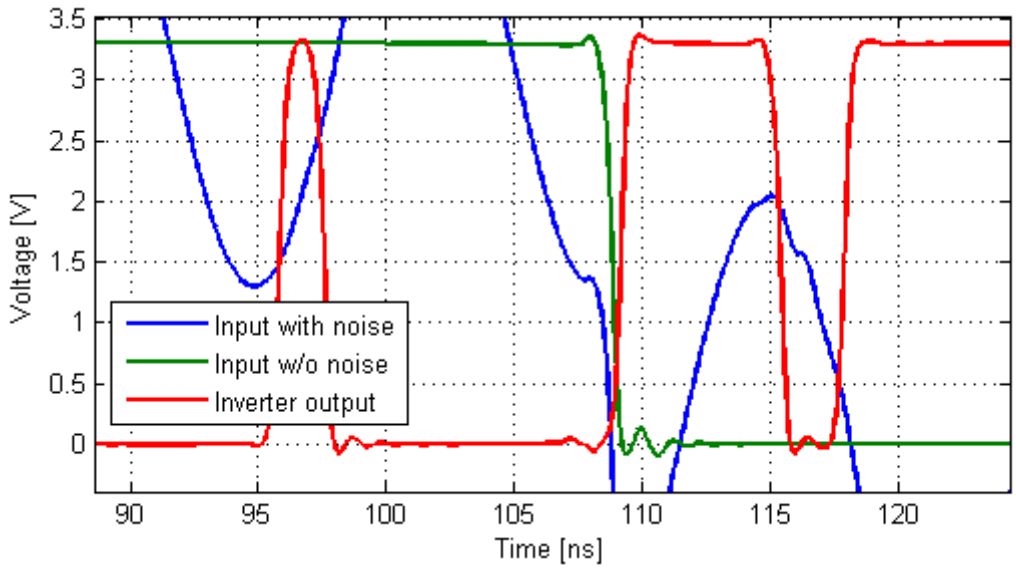

Figure 2.8. Static error due to harmonic interference

The disturbance signal superimposed to input signal produces incorrect changes of the logic level of the output. Such errors are defined as "glitches" and their presence is strongly linked to the EM interference amplitude. From a functional point of view, a glitch appears when the sum of logic input signal and interference overcomes the noise margin and the commutation threshold.

In Fig. 2.8 glitches are caused by a harmonic signal with a 2 V amplitude superimposed on the inverter input signal, whose power supply voltage is $V_{dd} = 3.3$ V. A similar scenario is found if the circuit is disturbed by a transient signal, such as a pulse, or if an interference couples with power supply voltage or with clock signal [10], affecting the whole circuit behavior instead of only a single component.

Dynamic errors

This error type appears during logic signal commutations; the disturbance effects upon logic commutations cause two effects depending on interference amplitude: jitter and pseudo-commutations. The output is affected by jitter when an input signal influenced by interference during the logic commutation phase crosses voltage threshold V_{IH} or V_{IL} earlier or later than expected, therefore modifying propagation time t_p through the logic gate that could lead to violations of critical timing

constraints. In Fig. 2.9 jitter is caused by a harmonic signal with a 0.4 V amplitude superimposed on the inverter input signal, provoking an output logic commutation after $t_p = 1.2$ ns instead of standard $t_p = 1.5$ ns propagation time obtained from the inverter data-sheet.

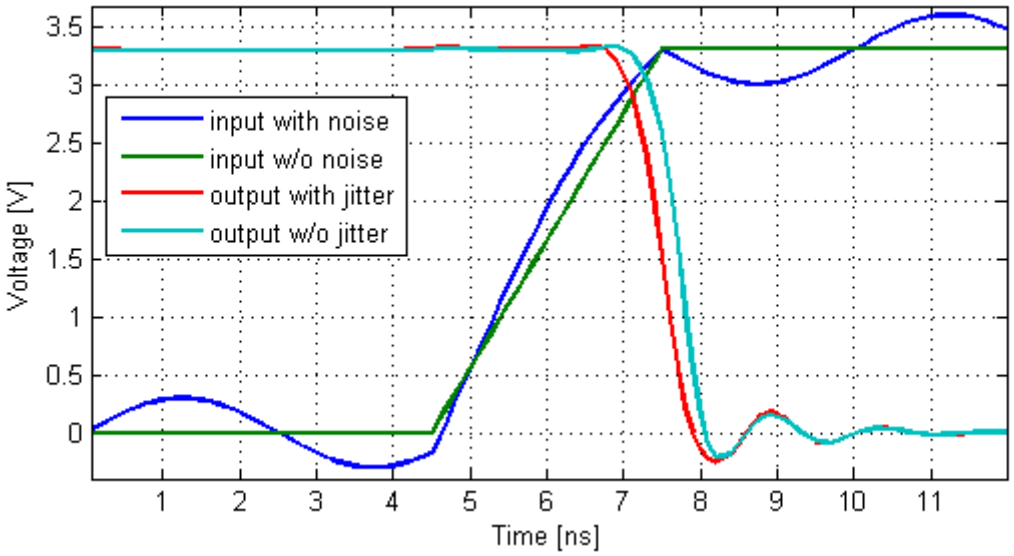

Figure 2.9. Jitter caused by harmonic interference

Pseudo-commutations appear when input signal rise or fall time is slow compared to harmonic interference period; the input signal crosses the voltage logic thresholds V_{IH} and V_{IL} multiple times leading to additional spurious commutations on the output port.

Rectification

EM interference effects on IC are divided in literature into In-Band or Out-Band perturbation depending on whether the disturbance signal bandwidth is included or not into the IC operating frequency range; the distinction is done due to the different EMC problems they provide. As shown in Fig. 2.10, an out-band high frequency disturbance, reaching a sensitive and non-linear circuit node in an integrated circuit, mixes with the wanted signal and induces a non linear distortion [11] known as *rectification*. It has been first observed in PN junctions of bipolar transistor [12, 13] and it refers to the distortion of the signal amplitude as well as to the position of spectral components. When nonlinear circuits are excited with a sinusoidal signal, the frequency spectrum of the output contains a spectral component at the original fundamental frequency, as well as spectral components at multiples of the fundamental frequency (harmonic frequencies) [14]. Harmonic distortion is particularly harmful because the harmonic components associated with the nonlinear distortion of a sinusoidal out-of-band EMI signal, may appear in the signal band, even if the EMI frequency band is not interfering with the wanted signal band. From then on, filtering or removing interfering EMI harmonic component(s) becomes very difficult.

Moreover, a component at DC appears as well, depending on the even-order nonlinear behavior

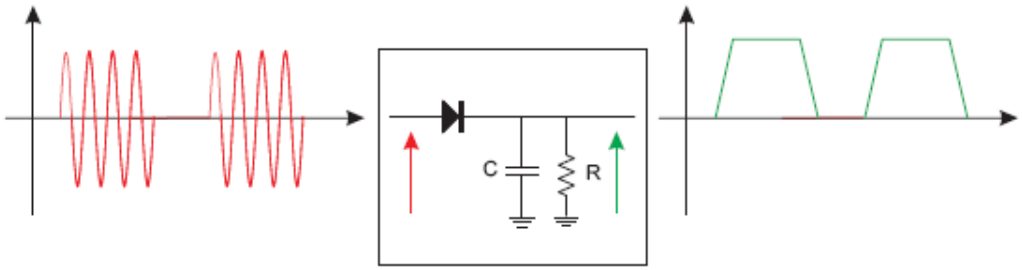

Figure 2.10. Rectification effect caused by harmonic interference

[15]; the DC shift phenomenon, which arises when this DC component is accumulated (e.g. in a capacitor), is extremely harmful because the correct DC operating region of a given circuit may radically change under influence of an interfering EMI signal.

2.4 EM Susceptibility Measurement Techniques

Several different experimental techniques described in this section have been developed to describe the impact of disturbances on the functional behavior of integrated circuits. The main objective of these measures is to determine frequency and disturbance power levels which the circuit under test is susceptible to; EM susceptibility criteria are defined upon observable physical quantities such as IC output voltages. The disturbance origins can be very different and interference signals present various time domain waveforms. The disturbance waveform is clearly important as it affects the interfering signal coupling with the device under test and therefore the susceptibility measurements; the relevance of measures outcomes will be acceptable only if the injected signal is as close as possible to the disturbance type under review. Waveforms of EM disturbances can be divided into two categories:

- Harmonic signals: a sinusoidal signal is injected in the DUT either at a fixed frequency and power level (continuous wave) or amplitude modulated in order to observe how the circuit behaves when attacked by a constant disturbance. EM susceptibility measurement techniques for harmonic signals are grouped under the standard IEC 62132 [16].
- Transient signals: these disturbances present various waveforms and their effects mainly depend on the energy contained in pulse and transition times. The spectral content of this type of aggression could reach very high frequencies due to fast rise and fall times. Susceptibility measurement methods for impulses, Electrostatic Discharge (ESD), Electrical Fast Transients (EFTs), Surges and Electrical Over-Stress (EOS) are described in the standard IEC 62215 [17].

2.4.1 Test Methods for Harmonic Signal Susceptibility Measurements

Tests are performed by injecting a continuous disturbance signal or an amplitude modulated one with a power-amplified signal generator. Differences between test methods depend on the config-

uration set up to inject the signal into the circuit. The standard IEC 62132 [16] is dedicated to IC susceptibility to RF over a frequency range originally up to 1 GHz. The most mature susceptibility measurements are the WBFC, BCI and DPI approaches which guarantee a high degree of repeatability and correlation, but recently some additional methods have been proposed, as detailed in Table 2.3.

Standard	Description	Stage in 2011
IEC 62132-1	General Conditions and Definitions	International standard
IEC 62132-2	TEM-Cell and Wide-band TEM-Cell Method (GTEM)	International standard
IEC 62132-3	Bulk Current Injection (BCI)	International standard
IEC 62132-4	Direct RF Power Injection (DPI)	International standard
IEC 62132-5	Work Bench Faraday Cage (WBFC)	International standard
IEC 62132-6	Local Horn Injection Antenna (LIHA)	New proposal
IEC 62132-7	Mode Stirred Chamber	New proposal
IEC 62132-8	IC Strip-line	New proposal
IEC 62132-9	Near Field Scan Immunity (NFSI)	New proposal

Table 2.3. Standard IEC 62132 - Measurement of IC susceptibility

Direct Power Injection - DPI

This measurement technique is described in the standard IEC 62132-4 [18] and in a frequency range between 150 kHz and 1 GHz. The measurement setup is shown in Fig. 2.11.

The frequency variable RF generator provides the disturbance that is amplified by the connected RF amplifier. The directional coupler and the RF power meters are used to measure the actual forward power injected into the DUT. At the RF injection port the RF power is delivered to the test PCB. To avoid supplying DC into the amplifier output, the RF amplifier is decoupled by a DC block, which is by default a capacitor of 6.8 nF. The DC supply is prevented from getting RF power by a decoupling network that has a high RF impedance on the side that is connected to the RF injection path.

To monitor the behavior of the DUT, an oscilloscope can be used; to decouple the RF signal crosstalk of the DUT from the low frequency measurement performed by the oscilloscope, a second decoupling network is used. In order to understand the influence of each individual pin, each pin that is expected to be exposed to RF disturbance should be tested individually. Multiple pin testing is permissible into pins of differential mode systems.

The nature of this measurement makes it very suitable to be incorporated directly in circuit simulators.

Bulk Current Injection - BCI

This method is used to inject a disturbance current in a DUT. This technique is derived from a standard measurement technique for characterizing automotive equipment and is currently defined in a frequency range between 150 kHz and 1 GHz in the standard IEC 62132-3 [19]. The measure-

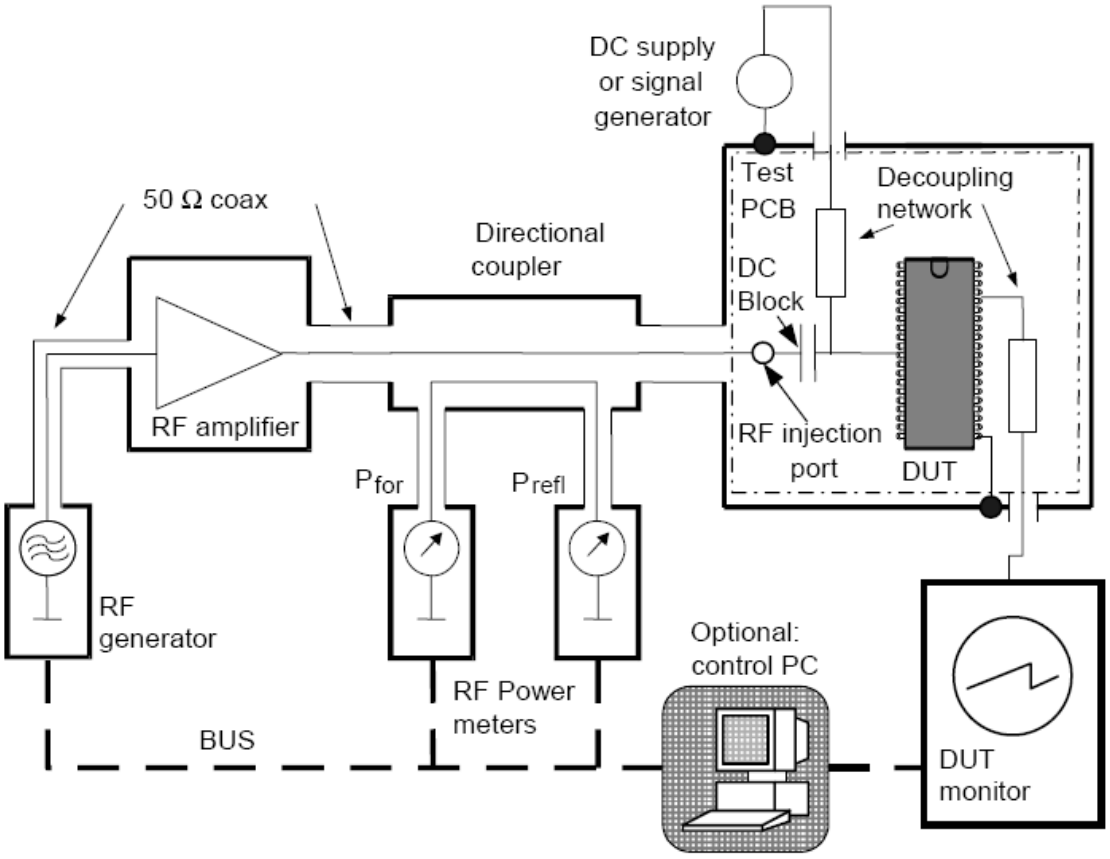

Figure 2.11. Direct Power Injection measurement setup

ment reproduces the induced current that is generated in the real world by electromagnetic field coupling into the wires of a system.

Two electrically shielded magnetic probes are clamped on one or a combination of wires that are connected to the DUT, as depicted in Fig. 2.12. The first probe is for the injection of RF power that induces the disturbance current onto the wires. The second probe is used for monitoring the induced current on the same wires. The disturbance current flows in a loop comprising: wires, the selected IC's pins to the power supply voltage, ground path and supportive circuitry. This supportive circuit provides the IC functional elements as source and load. The supportive circuitry is directly connected to the IC. When the equivalent RF impedance of the supportive circuitry is larger than 50 Ω, then a bypass capacitor is recommended. The by-pass capacitance, to be used at the supportive circuitry side, may also be needed to confine the loop area in which the induced current will be flowing. The main problem which prevents this measurement method to be used in circuit simulations is the fact that the magnetic coupling between the current probe and the wire is not exactly known; moreover, it is difficult to inject the current in a specific pin due to probe volume.

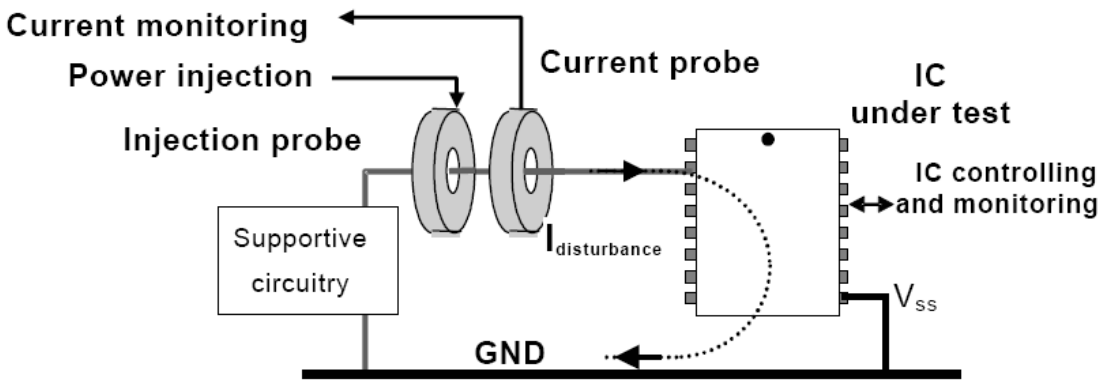

Figure 2.12. Bulk Current Injection measurement setup

Work Bench Faraday Cage - WBFC

The workbench Faraday cage is a standard method [20] for carrying out conducted immunity measurements to EM common mode disturbances in a 150 kHz - 1 GHz bandwidth.

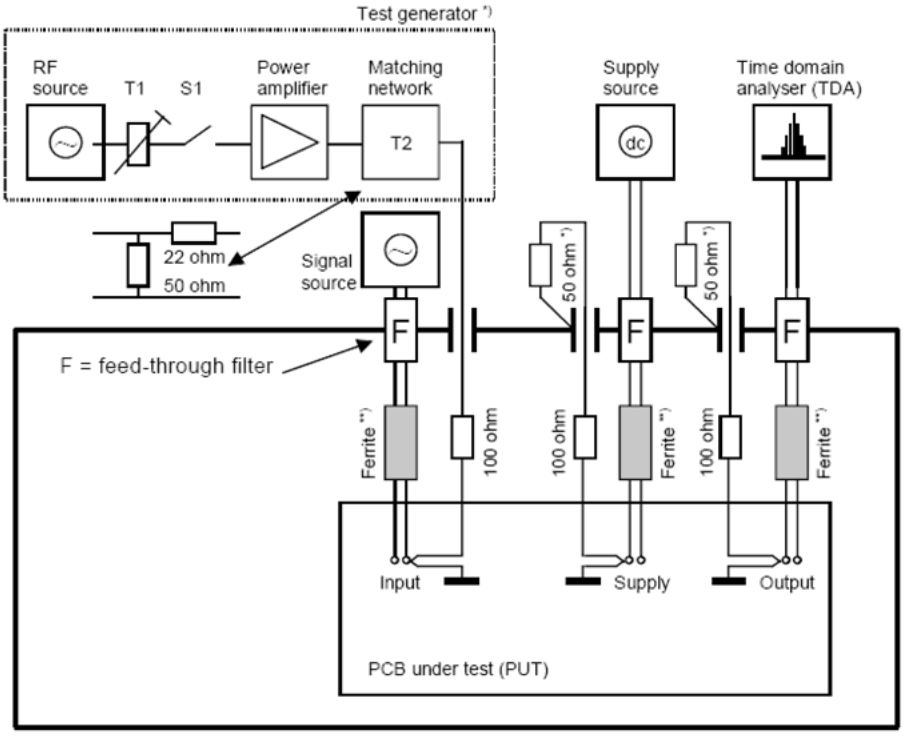

Figure 2.13. Work Bench Faraday Cage measurement setup

The IC is inserted into a Faraday cage in order to isolate the circuit from the external EM

environment, as depicted in Fig. 2.13. The disturbance signal is injected through a conducted resistance on the circuit. Filters are inserted at each interface of the cage to limit the spreading of RF in measuring devices. However, the scope of this measurement setup is very restricted, since it is only applicable to electronic products that are connected to external wiring: it is therefore not a suitable measuring method to measure e.g. small wireless appliances. Finally, this method is not practical to simulate.

2.4.2 Test Methods for Transient Susceptibility Measurements

The need to characterize the susceptibility of circuits is not limited to study the effects of harmonic disturbances. Indeed, these past few years many publications have shown that circuits were more sensitive to transient disturbances. M. Camp and H. Garbe research [21] evaluates the effects of fast transients on several PC hardware architectures, and it appears that the transient susceptibility of circuits increases with the arrival of new generations of processors as summarized in Fig. 2.14. The joint contribution of lower supply voltages, the increased integration of transistors and higher frequencies of operation are the main reasons for this decrease of immunity of integrated circuits.

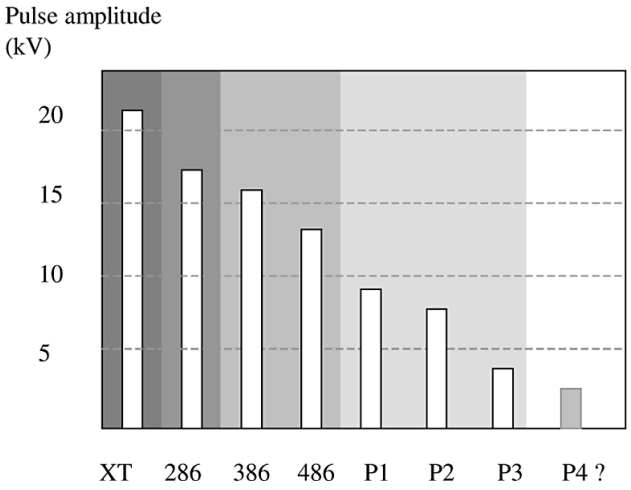

Figure 2.14. Immunity to transients tends to decrease with computer generation [21].

In recent years, the majority of analyses and studies on the characterization of the immunity of circuits to transient disturbances are about the effects of electrostatic discharge (ESD). However, transient disturbances are not limited to ESD; the disruptive effect of different types of transition depends on the energy they carry and therefore on their electrical characteristics such as their waveform, amplitude, rise time, duration, and repetition rate. The different transients are defined in the following way:

1. ESD [22]: transfer of electric charge between bodies at different electrostatic potentials in proximity or through direct contact.

2. EFT [23]: test with bursts consisting of a number of fast transients, coupled into power supply, control, signal or earth port of electronic equipment. Significant parameters for the

test are the high amplitude, the short rise time, the high repetition rate and the low energy of the transients. They are generated from the interruption of inductive loads, relay contact bounce, etc.

3. Surge [24]: transient wave of electrical current, voltage, or power propagating along a line or a circuit and characterized by a rapid increase followed by a slower decrease. It is generated by a power system switching or by a lightning stroke.

Transient signal energy is certainly low, but the probability that a disturbance of this type affects an electronic circuit is relatively high. Indeed, in the semiconductor industry, these natural disturbances are one of the main causes of component failure [9], along with Electrical Overstress (EOS). EOS disturbances include many different types of pulses and they include high-energy disturbances such as lightning and electromagnetic pulse. Damages caused by this type of disturbance are generally large and can cause interconnection destruction and oxide breakdown. There are many mechanisms of generation of transients, which give rise to short pulses with relatively large voltages and currents. Transients is a source of disturbance whose threat to electronic systems is increasing, and more particularly to ICss; therefore manufacturers must address these problems during the qualification phase of their products. Testing methods were developed and standardized in order to study circuit robustness.

Very Fast Transmission Line Pulsing - VF TLP

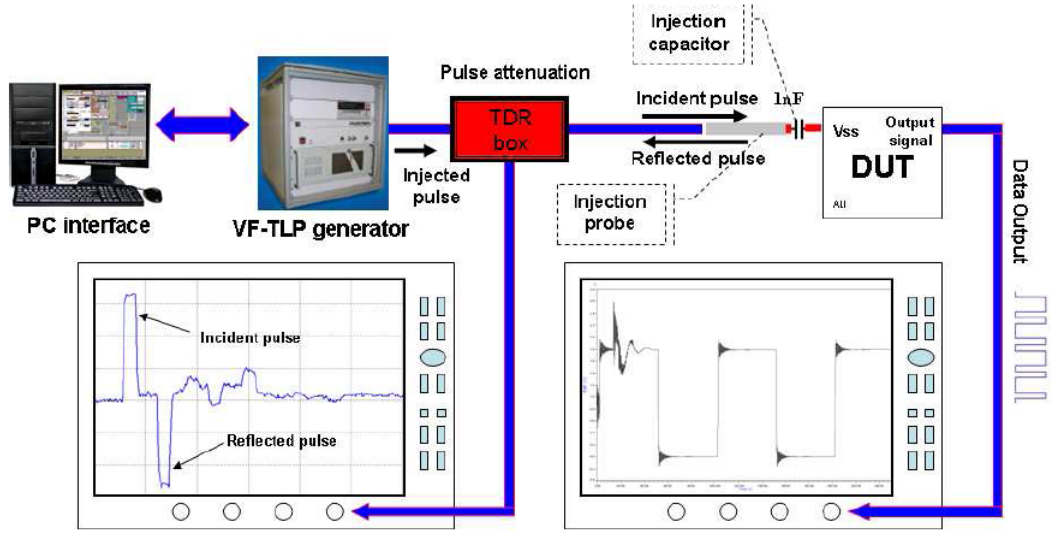

Figure 2.15. VF-TLP test bench

Over the years new ways of testing have emerged to characterize the behavior of electrical circuits in high current environment when stressed by ESD or other transients. So far Transmission Line Pulsing (TLP) [25] and Very Fast Transmission Line Pulsing (VF-TLP) tests [26] have

been introduced to describe respectively the sensitivity of the circuits of a Human Body Model (HBM) and Charged Device Model (CDM) ESD stress. These techniques are used to obtain a I-V static characteristic of ESD protection structures to extract the essential parameters for optimization. However, these testers are not limited only to this type of experiments since they allow to characterize the susceptibility level of integrated circuits to ESD. In fact, ESD is now regarded as an electromagnetic interference which can cause errors in integrated circuits. This type of study is done to determine the ESD levels of disturbance for which there appears a failure: it is an ESD characterization at the functional level. Studies based on the measurement principle VF-TLP were used to analyze the effects of disturbances on simple circuits and complex operating conditions [27] . This test bench is composed of a pulse generator controlled by a computer used to control the electrical parameters of the pulse (width and amplitude). An oscilloscope is added to the system in order to visualize the pulses injected into the circuit and it is connected to a Time Domain Reflectometry (TDR) box which allows to view independently incident and reflected pulses. This measurement method is similar to the DPI method because the ESD pulses are directly injected into a line connected either to supply or to ground via a capacitance selected to not filter the interfering signal. The different results obtained with this method confirm that the VF-TLP pulse generator itself is an excellent solution to evaluate the susceptibility of an integrated circuit operating during transient interference signals. This technique is particularly useful in the evaluation of the behavior of integrated circuits during a fast transient because it allows to choose the configuration of input pulses. However, this technique requires the establishment of a test bench incorporating relatively expensive equipment, which may limit its use.

2.4.3 Susceptibility Measurements at System Level

The main test for conducted susceptibility testing of electronic systems is the widely used Bulk Current Injection (BCI). A number of reasons make this technique extremely attractive. On one hand, BCI permits a susceptibility screening at the early design stages of units and subsystems at moderate costs and with limited investment of time. On the other hand, it is a fast and noninvasive procedure, and allows for onboard testing in case of large and complex systems. Consequently, BCI-based techniques have progressively gained the attention of several international standards, spanning from the aerospace [28] to the automotive [29] sectors. For the avionic environment, the BCI test determines whether equipment will operate within performance specifications when the equipment and its interconnecting wiring are exposed to a level of RF modulated power from 10 kHz to 400 MHz, by injection probe induction onto the power lines or on the interface circuit wiring. The test is made to qualify an equipment into a category defining the conducted RF test levels it can withstand, according to the thresholds depicted in Fig. 2.16. The category to be applied to a system or equipment frequently must be chosen before the internal RF environment of the aircraft is known. Further, many systems or equipments are designed with the intent that they will be installed in several different types of aircraft. Therefore the equipment manufacturer should design, test and qualify the equipment to the category consistent with expected location, exposure and use.

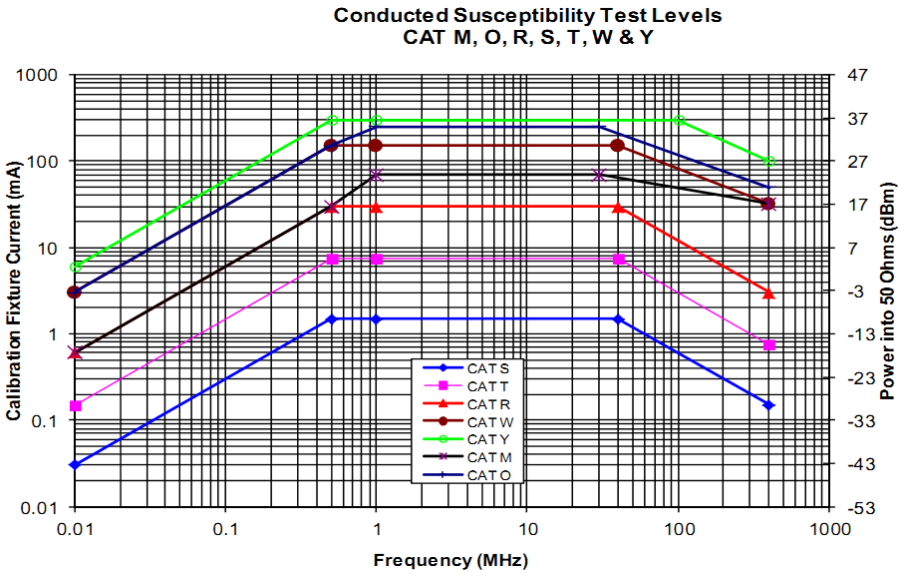

Figure 2.16. Minimum RF immunity level for aerospace systems depending on equipment category.

2.5 EM Immunity Models

The analysis of susceptibility is not limited to the characterization on a real experimental basis; there is a need to develop models for predicting susceptibility of the IC because, in the design phase of integrated circuits, experimental methodologies for immunity characterization are not available. The model must be able to predict with good precision the circuit behavior differences after being attacked by interference signals with varying amplitudes and waveforms, while remaining simple enough to keep simulation time to a minimum and to facilitate integration of the model into the stream of design tools. Moreover it is important to implement an immunity model taking into account the circuit non-linear behaviour. However all these features which an immunity model should have are in conflict with each other and this makes the operation of building an immunity model a complex research task and not fully mature yet. In this section the main strategies of immunity modeling at different levels of abstraction are shown and several immunity models are overviewed.

2.5.1 Failure criteria definition

In order to be able to predict the susceptibility of an integrated circuit during the design phase, the definition of a failure criterion is required; after simulation, data is processed to check if signals are in agreement with the chosen failure criterion. The interference signal amplitude is increased until failure criterion on observed signal output is violated. In this paragraph a list of failure criteria at integrated circuit level is presented, which can be easily checked in a simulation environment.

Template waveforms

When checking immunity on ICs, several digital signals critical for the correct circuit behavior are monitored and their waveforms are compared to a default template signal, where maximum allowed deviations from standard high and low voltage levels are defined; rise and fall time variations are also checked in order to evaluate if jitter violates a threshold and consequently provoke a digital failure.

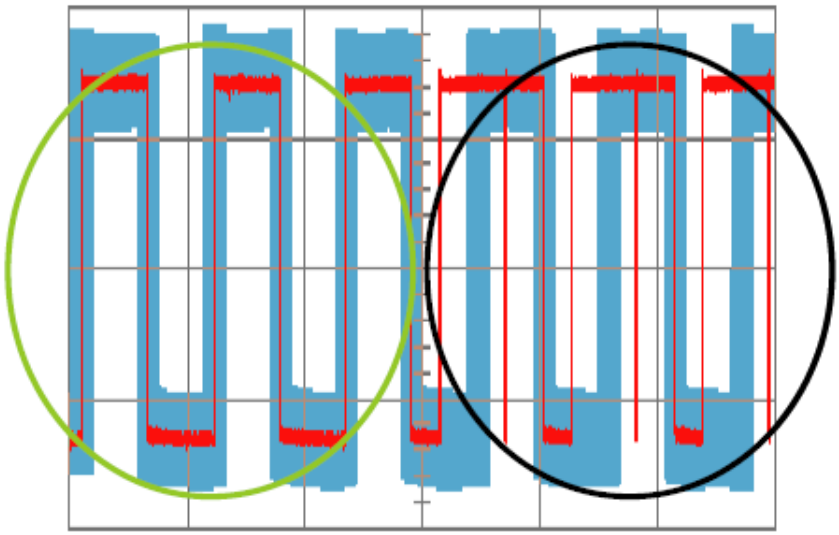

Figure 2.17. Template waveform failure criteria [30]

In Fig. 2.17 an EM immunity test applying template waveform criteria is shown. A microcontroller output signal is periodically toggled; when interference couples with the IC, the output signal waveform depicted in red is modified and it is compared with a default template (shown in blue). On the area marked with a green circle, the signal doesn't violate template thresholds and therefore immunity test is passed, while on the area marked with a black circle the interference corrupts the waveform and the immunity test is failed.

Stress of the power supply

In the presence of a RF disturbance, the voltage of the power supply can fluctuate. This fluctuation is called ground bounce when it is observed on the V_{ss} die, and supply bounce when it results from the V_{dd} die. Below a certain limit, these effects are tolerated by the active blocks of the circuit and no error is observed. Beyond this limit, the potential difference between the external and internal V_{ss} references is such that a part of the information from the outside can be badly interpreted by the active parts of the circuit and generate logical faults.

The idea is to perform iterative simulations by varying the frequency characteristics of the aggression voltage. For each frequency, the amplitude of the disturbance is increased until the fluctuation of the internal V_{ss} reference is higher than or equal to 20% of the nominal power

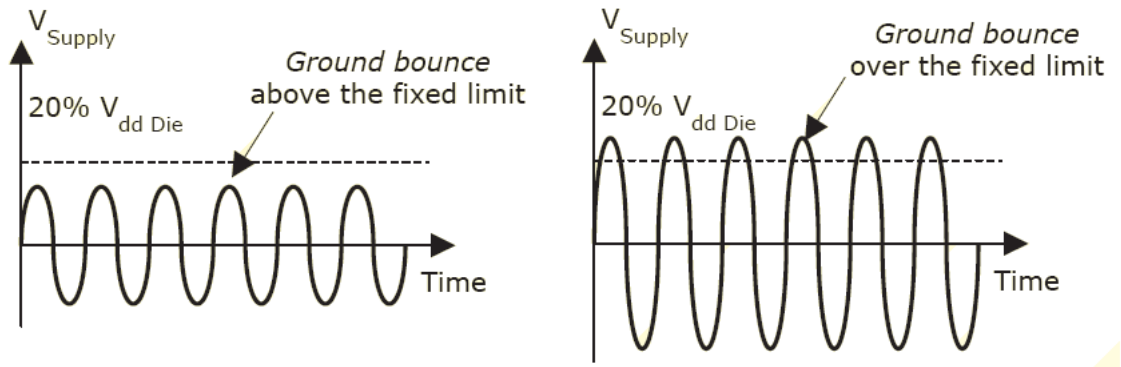

Figure 2.18. Power supply stress failure criteria

supply voltage. Once the level is reached, the criterion for susceptibility is supposed to be met, as shown in fig. 2.18.

Decrease of the power supply voltage

An important failure criterion lies in the decrease of the internal power supply voltage, defined as the difference between the reference voltages V_{dd} and V_{ss}. Below a certain margin, which can be defined at 30% of V_{dd}, the switching of the logical circuits is significantly slowed. This phenomenon originates delays of signal distribution and can lead to the loss of features of logical or analog circuits. [31] presents the switching delays according to the fall of the power supply voltage, in a simulation made for an CMOS inverter designed in 0.25 μm technology with typical load conditions. It shows that a decrease of 30% of the power supply voltage (from 2.5 V to 1.75 V) corresponds to an increase of the switching delay of about 60%. A decrease of 50% of the voltage V_{dd} generates a switching delay 150% higher. Such increase may cause some functional blocks to be no longer correctly operational at component level.

Over-consumption of current

A disturbance injection on the power supply network of a printed circuit board can generate parasitic effects on the on-chip power supply network, such as current flow of very strong intensity. These currents possess certain limitations due to the physical elements they cross. The current that can nominally flow through a gold bonding wire can be estimated as:

$$I_{max} = J_{cur}\pi r^2 \tag{2.1}$$

where J_{cur} is the maximal current density defined in $[A/m^2]$, r the conductor radius and I_{max} the maximal current which can flow before destruction of the conductor. It is important to note that the dependence on temperature is not taken into account, therefore in nominal functioning this maximum current is certainly lower than the proposed value. Consequently, these limits can be exploited to define a new failure criterion within the framework of analog simulations. For instance, an integrated circuit which consumes a nominal current I_{nom} of about 100 mA is supposed

to be able to stand 500 mA (5 x I_{nom}) current peaks. Furthermore, currents whose intensity is higher than 1 A have a very strong probability of destroying the most fragile elements of the chip.

2.5.2 Circuits Models

A realistic and faithful approach consists in building transistor-level models; a physics-based or "white-box" model can be used to simulate circuits susceptibility starting from an accurate description of the DUT. Historically, such model approach has been used first in a study [12] proposing to simulate RF disturbance effects on bipolar transistors using their Ebers-Moll model; it correctly defines parasitic elements and controlled sources in order to describe the non-linear effects due to signal rectification for PN junction. This kind of approach has been successfully applied to studies on circuits such as operational amplifiers and logic gates [4] and more recent research [32, 11] has studied circuit susceptibility modifying model characteristics, such as the operational amplifier model [33] shown in fig 2.19. For CMOS-based technology it is also possible to use the BSIM model for transistors that is easily exploitable by simulators of SPICE type. This model, not originally developed for immunity prediction, is a compact model of third generation and commonly used in microelectronics design; it models with great precision different operating regions due to the presence of many user-defined parameters.

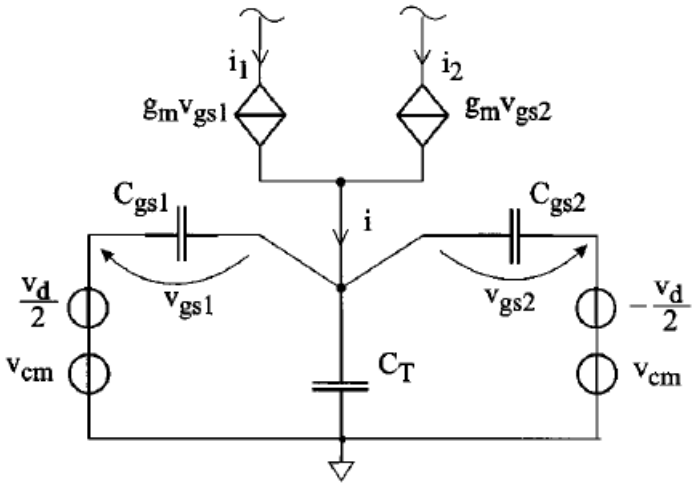

Figure 2.19. Operational amplifier immunity model

More recently the susceptibility simulation of complex circuits has been done using a full transistor-level circuit [27]. These studies are related to circuits built for susceptibility characterization, meaning that there is a direct collaboration with the circuit manufacturer. However this type of modeling is seldom used nowadays because it is not suitable for large circuits due to their huge complexity and long simulation time; a complete simulation of a logic core requires large computational time and therefore it is necessary to develop simplified models to shorten simulation time.

Moreover, for industrial circuits, such modeling approach requires access to confidential information and chip manufacturers often do not provide a complete netlist of their circuit. Therefore new model types have been developed in order to comply with those requirements.

2.5.3 Behavioural Models

The principle of behavioural modeling is to replace all or part of a component by a mathematical model reproducing the circuit behavior when affected by interference. A behavioral model expresses the outputs of a system as a function of its inputs and of several internal "state variables", i.e. by means of mathematical expression, therefore it does not require physical and technological details of the circuit. A behavioral model can then take into account only the most important phenomena required by the application; consequently, there is always a trade-off between simulation speed and accuracy. Those models provide a description of the functional blocks at a level of abstraction higher than the transistor-level model; it proposes to develop a "black box" in which input and output variables are linked by a set of differential equations, non-linear functions or data tables. Development of behavioural models is expanding with the widespread use of standard languages such as MAST, HDL-A, VHDL-AMS and Verilog-AMS, that position themselves as direct competitors of SPICE type circuit simulations. VHDL-AMS (Analog and Mixed-Signal) has many advantages over other languages: it is standardized [34], upward-compatible with VHDL, and modeling and simulation tools are now mature. Several studies have been done about behavioural models; Stievano work [35] consists in behavioural model identification by means of nonlinear dynamic parametric models. In this approach, the parameters of a suitable model are estimated from the voltage and current waveforms measured at the device ports. The modeled device is considered as a black-box, i.e., in principle, no knowledge of the internal structure is required and the modeling information is completely contained in the device external responses. Owing to this feature, parametric models can be effectively estimated from measured transient responses or from simulated responses computed for detailed reference transistor-level models. Besides, since the structure of the parametric models is partially selected by the identification process itself, they automatically include all significant physical effects relating input and output waveforms. It has been demonstrated [36] that this modeling solution is able to address EMC problems and signal integrity.

Another model has been successfully built by Chahine [37] who has proposed to use Artificial Neural Networks (ANN). The modeling procedure consists in building a susceptibility mathematical model based on an inverter susceptibility measurement from a DPI test; indeed, the conducted susceptibility problem can be considered as a non-linear mathematical function such as an ANN that connects inputs and output variables. Depending on the complexity of the function to approximate, training and building a Neural Network could be computationally heavy.

In [38], a new technique to create an accurate immunity model of an analog IC is proposed. The model is based on surrogates, constructed using ANNs, replacing the real netlist and concealing the IP of the manufacturer. Data are collected by means of harmonic balance (HB) simulations, allowing to model both the functional and the noisy behavior of the nonlinear circuit in the frequency domain, making it ideally suited for efficient DPI or BCI immunity simulations. The novel method is validated by means of an industrial case study, being an automotive voltage regulator, clearly showing the capabilities and practical advantages of the technique.

Generally speaking, behavioral models present interesting features for manufacturers since they do not release any confidential information about the internal structure of ICs; however their validity domain is strictly related to the adopted mathematical formulation, which may reduce their effectiveness. In addition, they could display a non physical behaviour since generally no physical constraints are included in the model, apart from input/output data.

2.5.4 Macromodels

By definition, macromodeling aims at replacing a system or part of it with a model in order to reduce computational time during simulation. Therefore macro-modeling consists in constructing an electrical model as simple as possible and able to reproduce with precision the behavior of the system. A macro-model is built with a "gray-box" approach, as it can be composed of a mix of ideal linear elements (passive components and controlled sources), non-linear active components (diode, transistors) and mathematical formulations from measured or simulated data. This class of models has been widely used both in academic and industrial world to build susceptibility model. In an industrial context, a macro-model is preferred if it has compatibility with main circuit simulators (SPICE, VHDL-AMS) and it does not disclose confidential information. For these reasons, the macro-model is viewed as the most appropriate model type; however, unlike EM circuit emission, currently there is no standard for immunity modeling. Research elaborating a susceptibility model is underway in academic contexts. In the following sections several macromodels for IC are described.

IBIS

The first important contribution to standard EMC modeling originates from the I/O buffer information specification (IBIS) [39] working group, originally developed by INTEL engineers, that proposed a standard aimed at describing the electrical performance of I/O structures of ICs. IBIS is a standard for describing the analog behavior of a buffer; the specification provides a standard parsed file format consisting of current-voltage (I-V) characteristics, voltage-time (V-t) characteristics, device package parasitics, input capacitance, and timing measurement information for several types of I/O structures. IBIS models provide information that accurately models a buffer's behavior without revealing proprietary information about the circuit's structure or fabrication process. IBIS models are component-centric; the IBIS model describes all pins of the physical component. So, IBIS models are particularly well-suited for interfacing with the component footprints of large PCB databases describing hundreds or thousands of nets. Systems designers use IBIS models to perform board level signal integrity simulations and timing analyses.

Fig. 2.20 presents the structure of input and output described according to the IBIS specification. The most important keywords relating to EMC are listed in Table 2.4.

From a EMC point of view, IBIS does not provide specific information about ICs core noise and considers the power supply as an ideal voltage source, therefore a more advanced model is needed for immunity simulation.

IBIS feature	EMC Application
R,L,C Package	Used for defining Passive Distribution Network (PDN)
Input protection diodes	Susceptibility Analysis
Output driver characteristics	I/O driver emission
Supply structure for each pin	PDN definition
Pin input capacitance	Immunity analysis

Table 2.4. Role of IBIS in EMC of ICs

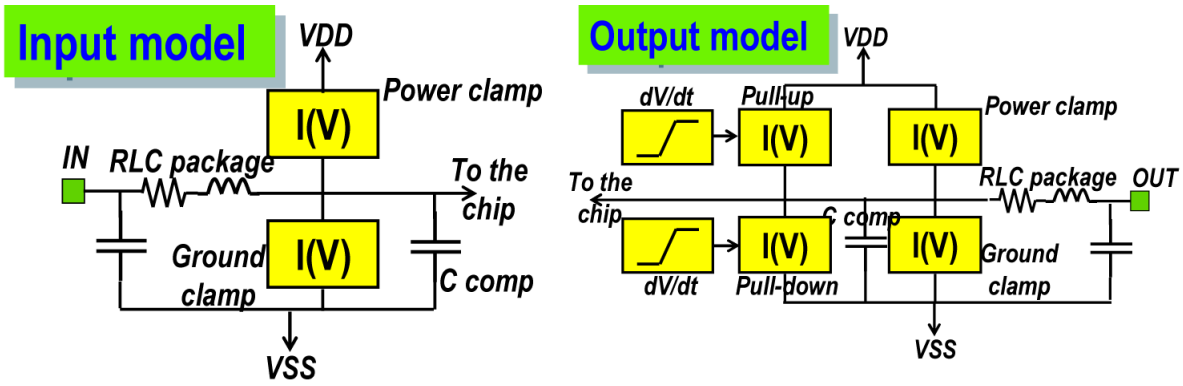

Figure 2.20. IBIS model structure

LECCS

To achieve fast EMI/EMS simulations of digital devices and printed circuit boards, an EMC macro-model for digital ICs/LSIs has been developed that was named Linear Equivalent Circuit and Current Source (LECCS) model. The model was originally proposed to evaluate the RF noise current on a power pin of a core logic circuit. LECCS models consist of linear equivalent circuits (LEC) combined with equivalent current sources (CS) that express the internal noise source caused by the switching operations of the transistors; the switching duration of each transistor is as short as sub-nano seconds, which is short enough when compared to the time constants of the noise current. Therefore, most of the noise characteristics of the device under test can be expressed by linear macro-impedance models such as the one shown in Fig. 2.21, and the macro impedances, including a chip and package, can be evaluated from the outside. So, the equivalent circuit of linear impedance is practically applicable and accurate enough for EMC simulations. Two types of LECCS models have been proposed, the LECCS-core for the internal core logic circuit and the LECCS-I/0 for the output buffer circuit. They have been applied to practical ICs to simulate and control RF power current of devices.

The LECCS-core model is composed of a linear equivalent impedance, Z_i, and an internal equivalent current source, I_s, The device model provides the RF current in the power pin of an IC as the noise excitation source. The LECCS model for core circuits has the following features:

- All the model parameters can be determined by measurements, so there is no need to consider the internal design parameters. Of course, the parameters can also be derived from a

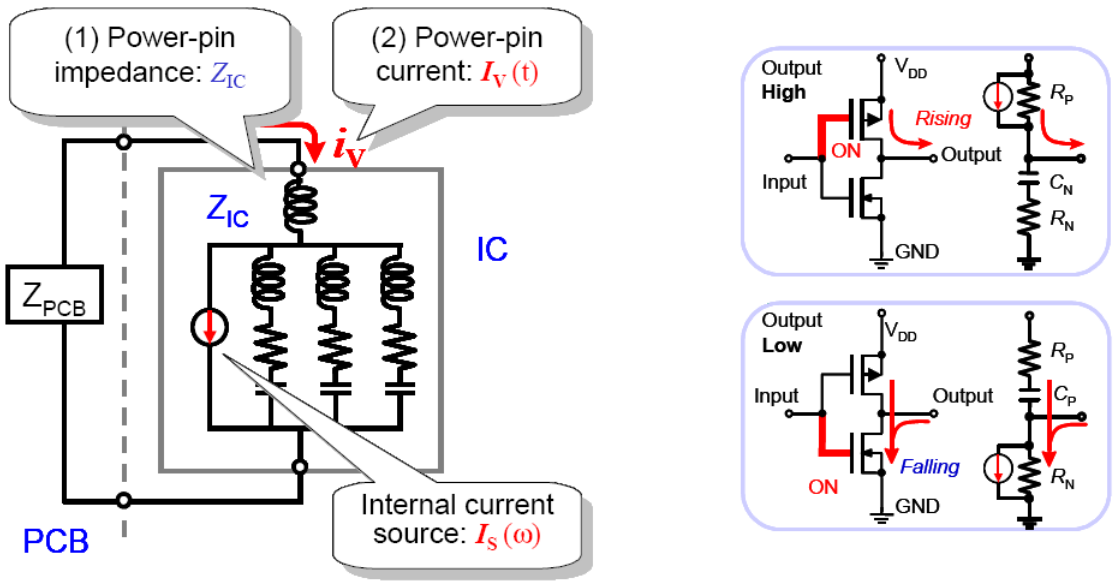

Figure 2.21. LECCS Core (left) and LECCS I/O (right)

SPICE model of the device.

- The internal current source is determined from the measured current spectrum.
- The model can express RF noise characteristics of the power current of an IC. The effects of decoupling capacitors on a PCB or of on-package and on-chip decoupling capacitors can be evaluated.

The LECCS-core model was applied to simulate EMI from practical PCBs and good agreement between simulations and measurements was achieved [40]. The results include decoupling simulation with on-package and on-board capacitors, and EMI simulation with a powerbus resonance model of a multi-layer PCB.

The LECCS-I/0 model was proposed to express the variation of the RF power current dependent on the external output load of the drivers. Two quasi-static (H or L) states were separately modeled with a set of linear equivalent circuits. When the LECCS-I/0 model is compared with the LECCS-core model, they can be defined as follows: the LECCS-core model describes the electrical characteristics of the internal blocks of an LSI or IC with no global I/0 interconnection, and the LECCS-I/0 model describes the characteristics of blocks having external I/0 interconnections.

The LECCS-core model is also applicable for immunity evaluations; Ichikawa et al. [41] have shown that LECCS model could be used to describe component susceptibility. Indeed the impedance characterization of coupling path and circuit is critical because it allows to simulate interference propagation inside the circuit. The frequency-dependent internal impedance is directly related to its susceptibility as it impacts the power levels of interfering signal.

ICEM

The Integrated Circuit Emission Model (ICEM) [42] has been developed to simulate conducted and radiated emission due to internal circuit activity and input/output commutations, therefore not for simulating susceptibility test. Based on this IC architecture,which describes all the functional blocks and all the internal and external connections, an ICEM model is defined to describe the electrical and electromagnetic behavior of all the internal blocks. An ICEM model is built around a set of ICEM blocks, which are composed of different components, as shown in Fig. 2.22:

- Passive Distribution Network (PDN): The PDN for this analysis describes impedances seen between terminals such as power-supply and I/0.
- Internal Activity (IA): The IA describes the current driven by the internal blocks. It can be expressed in time or frequency domains. Spice source components such as IPWL and IPULSE can be used to describe low complexity signals.
- Inter-Block Coupling (IBC): the IBC component describes the connection between two internal terminals such as two different grounds.

With these three ICEM components and a set of block ICEM models, a structural ICEM model can describe a full IC architecture. For example, I/Os can be described using the PDN for the internal and external impedance and the IA for the specific activity of this port.

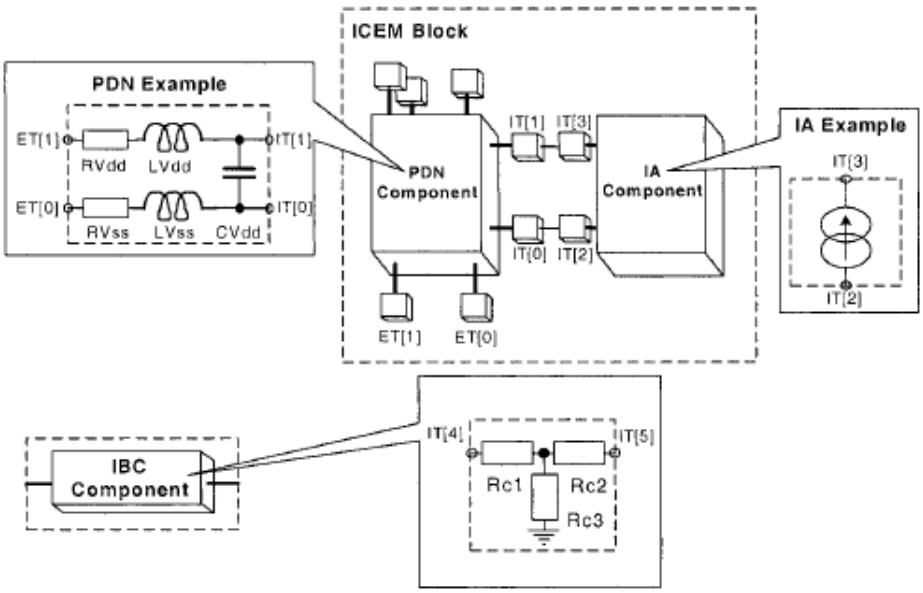

Figure 2.22. ICEM structure

Since the integrated circuit emission mode used for the simulation of parasitic emissions gave interesting results, a similar development path to set up the immunity model for components is used. The integrated circuit immunity model reused the passive elements of the ICEM model; the

electrical elements of the model are directly linked to the physical dimensions of the component, to the on-chip capacitances and to the power supply network. As immunity simulation is relatively different to parasitic emission simulation, a current generator is no longer necessary. but, from the point of view of the RF generator, the IC core is perceived as a load. Consequently, the current generator is replaced, in a first approximation, by a resistance load. . Research done by Baffreau [43, 30] successfully reproduced susceptibility tests when RF interference coupled with power supply; however this model is far less useful when interferences are injected on I/O ports, because non-linear elements protecting IC ports are not modeled in ICEM; adding those circuits as necessary, such as clamp diodes during injection of RF disturbances on a I/O, improved susceptibility prediction significantly.

ICIM

The development of a model able to predict ICs response to interferences is mandatory in order to improve EM immunity and in a industrial context, a general immunity model of IC functional blocks is needed to deal with this issue in a way as realistic as possible.

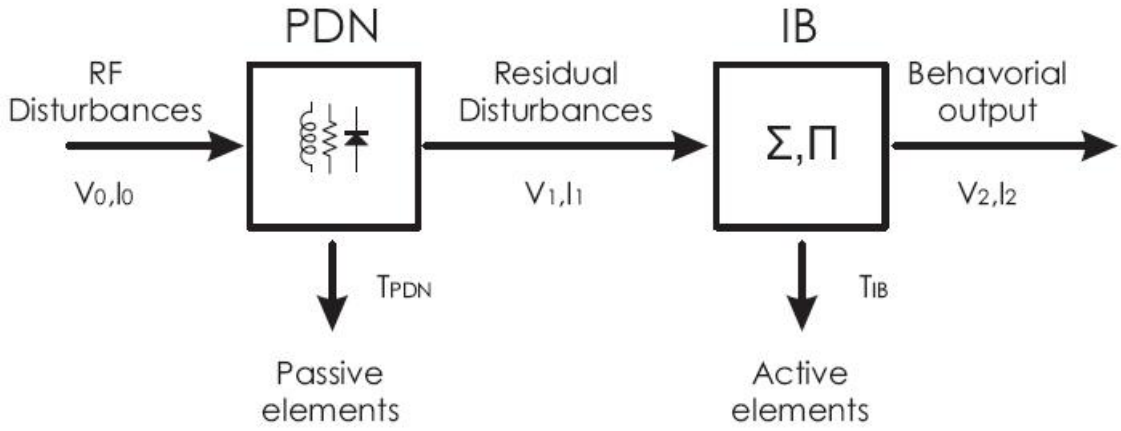

Figure 2.23. ICIM structure

Starting from ICEM model, the first attempts to standardize these approaches were performed through the proposed standard ICIM [44]; the internal structure, shown in Fig. 2.23, is defined by two blocks:

- Passive distribution network: The PDN consists of passive elements for the package, bonding and on-chip interconnections. It represents the input network of the power and signal pins of the chip. It characterizes the coupling path for the RF disturbances, which can undergo filtering and distortion.
- Immunity Behaviour (IB): the IB corresponds to a behavioral block which reproduces functional behavior when disturbances couple with the component. The information output, where immunity criterias are applied, from the IB via one or more observable outputs describes circuit response to a disturbing signal applied to one or more input ports.

A first model has been made by Lafon et al. [45] dedicated to the prediction of immunity behavior for continuous wave (CW) disturbances, in the 1 MHz - 3 GHz frequency range, on a LIN transceiver analyzed with a DPI test; the agreement between measurement and simulation were good when RF interference coupled with power supply.

Other models

An interesting model of microcontroller immunity has been described by Steinecke et al. [46]; it presents an approach to simulate the immunity of the microcontroller based on dynamic, nonlinear and passive model. By introducing the dynamic elements, this modelling technique reflects both those dynamic and nonlinear behaviour of ports and cores of the microcontroller. The dynamic model is suitable for time domain simulation, capable of simulating both RF and pulse immunity of the microcontroller.

In order to apply immunity criteria the model should correctly predict the interference arriving at the functional blocks. Impedance is one of the most important properties of the microcontroller that determine the transmission coefficient. The impedance of the I/O, the impedance of the load of the power network and the impedance of the interconnection lines work together to determine how much disturbance will be coupled into the microcontroller and how much of them will reach specific functional blocks. To be able to simulate the immunity properly, the model of the microcontroller should includes all significant impedance components. Those components can be divided into two groups:

- Passive components: package, on-chip PDN and substrate are modeled in a standard manner with basic structures of RLC networks, extracted from the technology profile and layout design of the microcontroller with EDA tools.

- Active components: Cores and I/O.

Cores of microcontrollers have three important electrical properties: they create dynamic current, their impedances are strongly nonlinear with respect to core supply, and finally once core supply is out of operation range, it stops working and the core current becomes very small. Fig. 2.24 shows the immunity model that can correctly simulate the behaviour of the core, composed of C_m, sum of parasitic and decoupling capacitors of the core, and dynamic voltage dependent resistors, simulating the active part of the core. The upper resistor and lower resistor are switching resistors that charge and discharge the load capacitor C_o; when they are in on-state, their resistances depend on both the voltage across them and local V_{dd}.

The model of the digital I/O contains a dynamic element simulating the driver/buffer, a pair of voltage controller resistors simulating the power and ground clamp, a pair of capacitors simulating the pad capacitances to power and ground. It is worth to point out the difference between this model and the model generated from IBIS, due to the presence of non-ideal power and ground.

Time domain simulation in HSPICE are run with this model and EM immunity test of microcontrollers can be done, obtaining realistic functional failures when disturbance is injected either on digital I/O or power supply [46].

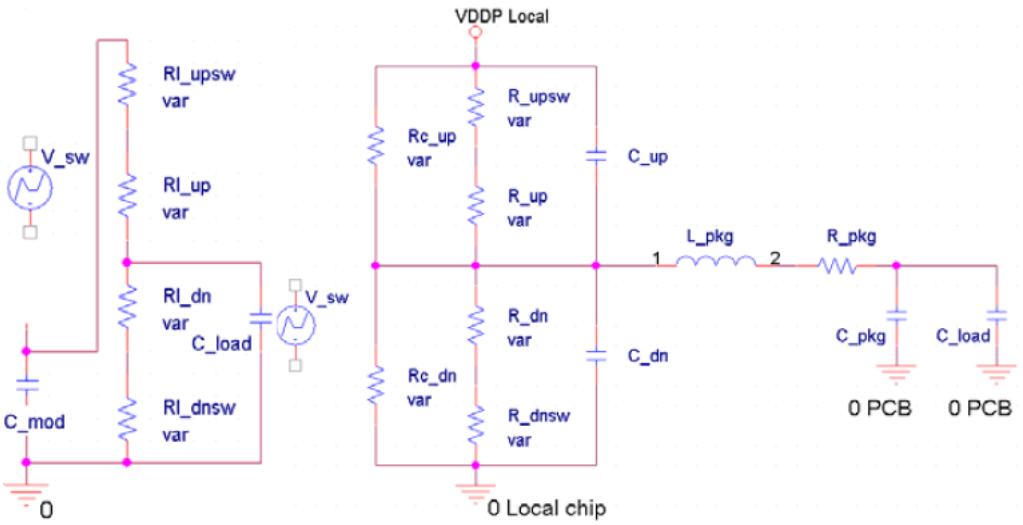

Figure 2.24. Dynamic core model (left) and model of digital I/O (right)

2.6 Chapter Summary

In this chapter, the EMC of integrated circuits was introduced analyzing the technological trend of the last years. The EM emission and susceptibility problems are steadily growing due to the IC physical scaling and the increasing frequencies. The basic EMI effects on ICs and the most common failures are highlighted. Several different experimental techniques are described to measure the impact of RF and transient disturbances on the functional behavior of integrated circuits at component and system level. The designers' need to have immunity models of ICs is highlighted and a review of the different modeling approaches is carried out. In the following chapters a susceptibility characterization and a novel modeling approach are presented for ICs used in communication networks.

Chapter 3

Communication Network Immunity Analysis

The first step required to understand the EM susceptibility of a complex electronic equipment is to analyze the behaviour of its integrated circuits when affected by disturbances. In particular, the IC electromagnetic immunity is of paramount importance in communication system networks in noisy environments. Today, in automotive, avionic or industrial environments, well-designed network standards are able to provide data integrity and performance requirements of safety critical systems at a reasonable effort. These network-based systems offer a significant weight reduction, lower development cost and substantial procurement and maintenance savings compared to dedicated communication systems. This is mainly achieved using a network backbone which serves as a shared resource for the communication between multiple modules. Every module communicates using a transceiver as an interface between the local digital signaling and the signaling through the network. Hence, the performance of the IC transceiver when affected by disturbances is one of the main factors that guarantees the EM immunity of the whole equipment. The IC susceptibility needs to be addressed before being able to generate an accurate immunity model for design purposes. In this chapter, as a test case, an immunity analysis is carried out on CAN transceivers, representing the main components of each CAN bus node.

3.1 Test Case : Controller Area Network

CAN is a network protocol that allows multiple processors in a system to communicate efficiently with each other. Developed by Bosch [47] in 1986, today CAN represents a standard for high-speed, mission-critical, real-time control networks in multiple environments. CAN uses high-speed analog circuit techniques to provide data transfers up to 1 Mbps and has proven advantages of cost, low power consumption, and noise control. CAN is a multi master network where any network node can act as transmitter or receiver, sending messages through a serial bus with the individual nodes (processors) in the network linked together in a daisy chain, as shown in Fig. 3.1.

Any processor can send a message to any other processor, and if a particular processor fails, the other devices in the system will continue to work properly and communicate with each other. Any node on the network needing to transmit a message waits until the bus is free. Every message

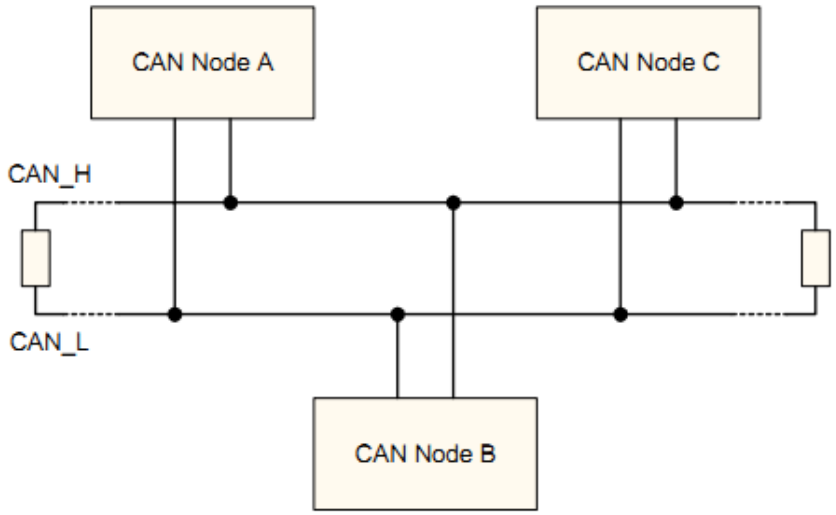

Figure 3.1. CAN topology diagram

has an identifier, and every message is available to every other node in the network. The nodes select those messages that are relevant for them and ignore the rest. Controller Area Network systems only involve the transmission of brief, simple messages to trigger events or to provide monitoring values from sensors, such as temperature or pressure. Also, a CAN system is usually closed, and does not need to account for system security, presenting data in a user interface, or monitoring network logins or sessions. Hence, only layers 1 and 2 of the ISO/OSI model, Physical and Data Link, are included in the ISO 11898 specification.

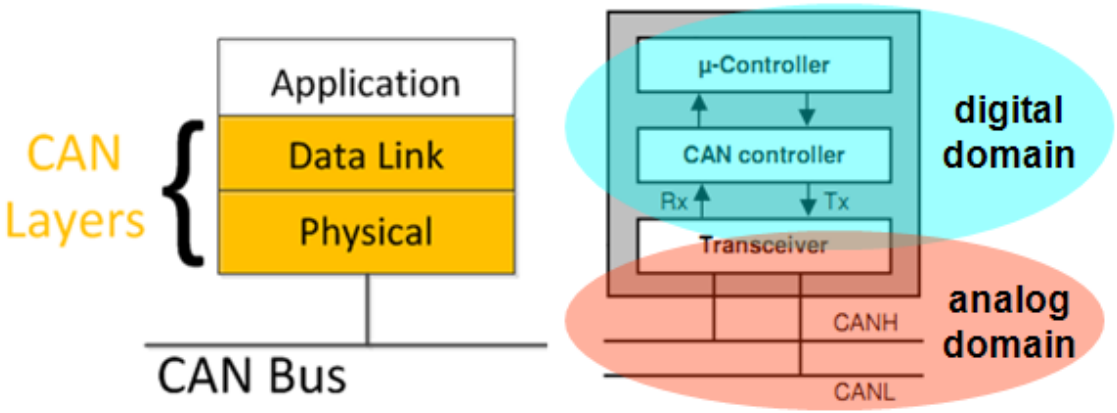

Figure 3.2. CAN Node and equivalent ISO/OSI Model

As shown in Fig. 3.2, the two layers are implemented in every CAN node, which includes three main components: the CAN transceiver, the CAN controller and the micro-controller. The

CAN transceiver is the interface between the transmission line and the CAN controller. Its task is to transform the logical signals, coming from the CAN controller, into the physical bus levels specified in ISO 11898. It also converts the analog signals received from the bus into logical signals that can be understood by the CAN controller. The CAN controller, also named protocol engine, coordinates the communication between the micro-controller and the bus via the transceiver. It generates the CAN message frame containing the information that should be submitted to the bus. When the CAN node acts as receiver during a message frame, it reads the message frame and prepares this information for the micro-controller, which runs the higher level applications.

3.1.1 Physical Layer

The physical layer governs the connection between the nodes in a network, and the actual transmission of electrical impulses across a copper wire, coax or fiber optic cable, or wireless signal. The transmitter's physical layer translates data drawn from the data link layer into an electronic signal. On the receiving end, the physical layer translates those electronic signals back into a data format that is then passed up to the data link layer. Thus the physical layer provides standards for bit representation, bit timing and synchronization, and the type of pin connectors and cables to use.

Bit Encoding

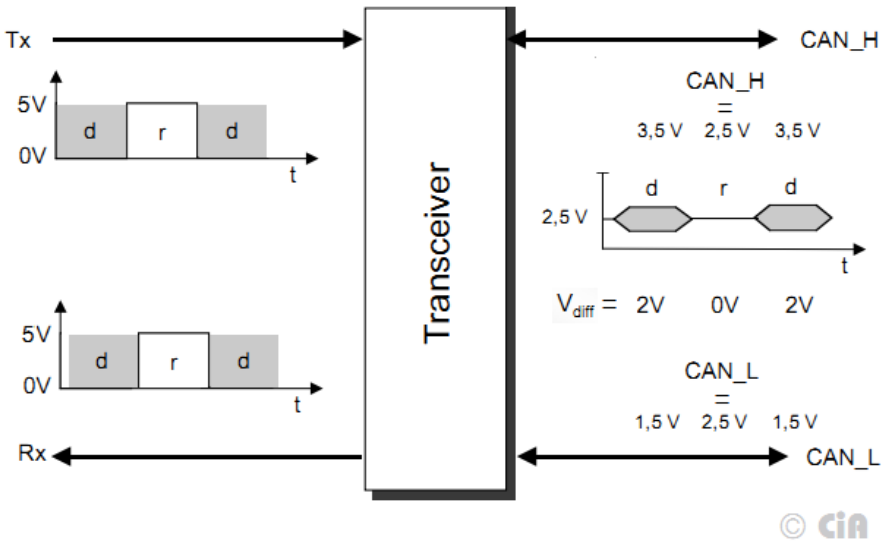

Figure 3.3. CAN Bit Encoding and Bus States

A CAN controller is connected to the transceiver via the Tx serial data output line and the Rx serial input line. The transceiver is attached to the bus line via its two bus terminals CANH and CANL, which provide differential receive and transmit capability. Tx and Rx are direction-related signals, while the differential signal between CANH and CANL is undirected. Each transmitting

CAN node reads the output back; but there is a delay between the bits transmitted and the related received bits to be considered. Tx and Rx logical signals are coded according to the Non-Return-to-Zero (NRZ) method. This means that during the total bit time the generated bit level is either 'high' or 'low'. One characteristic of Non-Return-to-Zero code is that the signal provides no edges that can be used for resynchronization if transmitting a large number of consecutive bits with the same polarity. Therefore bit-stuffing is used to ensure synchronization of all bus nodes. This means that during the transmission of a message, a maximum of five consecutive bits may have the same polarity.

When describing CAN signals, it is common to use the terms 'recessive' and 'dominant' to describe the state of the bus. For a two-wire bus the recessive bus state occurs when the CANL and CANH lines are at the same voltage level (CANL = CANH = 2.5V), and the dominant bus state occurs when there is a difference in voltages (CANL = 1.5V and CANH = 3.5V). The CAN bus remains in the recessive state when it is idle. The transmitter translates a logical '0' as a dominant bus state and a logical '1' as a recessive bus state. The bus node receiver detects a recessive bus condition if the voltage of CANH is not higher than the voltage of CANL plus 0.5 V. If the voltage of CANH is at least 0.9 V higher than CANL, then a dominant bus condition is detected.

Bit Timing and Sampling

The Controller Area Network protocol uses the synchronous data transmission method. For CAN systems, every node sends and receives using the same clock rate, and all clock rates in the network are based on a single reference point. This makes data transmissions more efficient, but it is difficult to keep any two clocks synchronized over time without some sort of reference signal. Clocks commonly lose their synchronization due to oscillator drift, propagation delays, and phase errors. CAN nodes use two different methods to synchronize their clocks, Hard Synchronization and Resynchronization. Hard Synchronization occurs only once during a message transmission, at the beginning of a new message frame. Before a frame begins, the CAN bus is in a recessive (idle) state. The first bit of a frame is a Start of Frame bit which is always transmitted dominantly. Every node synchronizes its clock using the transition created by this Start of Frame bit. The clocks are not able to remain synchronized throughout the entire frame so they must continually resynchronize. Resynchronization occurs every time the bus transitions from recessive to dominant. If there is a string of '0's or '1's then the CAN nodes depend on the transition created by the stuff bit to resynchronize their clocks.

Bus Topology

There are several official and industry standards dealing with CAN medium attachment, the most important of which is the CAN high-speed standard ISO 11898-2 [48] for general purpose applications. It assumes the network wiring technology to be close to a single line structure in order to minimize reflection effects on the bus line. Cables chosen for CAN bus lines should have a nominal impedance of 120 Ohm, and a specific line delay of nominal 5 ns/m. Line termination has to be provided through termination resistors of 120 Ohm located at both ends of the line, as shown in Fig. 3.4.

CAN bus is highly immune to electromagnetic interference due to the differential nature of the

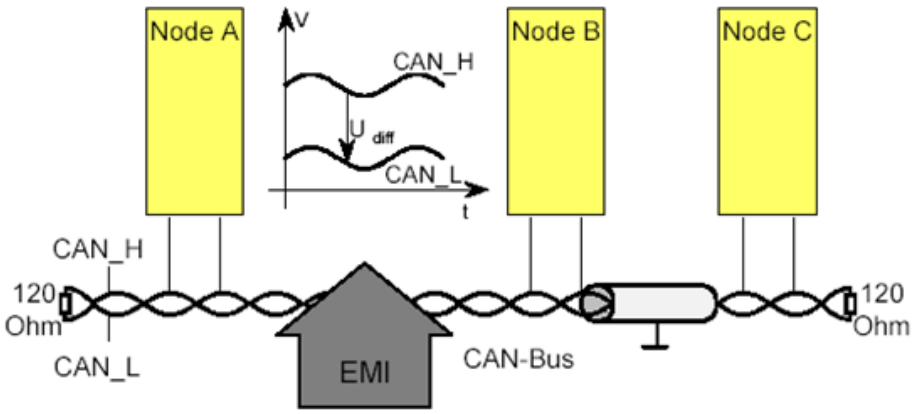

Figure 3.4. CAN Bus Topology

transmission signal: both bus lines are affected in the same way which leaves the differential signal unaffected. Additionally twisted pair wires are a common choice as physical medium, therefore their behavior, jointly with wire shielding, reduces EM interference effects on bus line.

3.1.2 CAN Transceiver Port Analysis

In a CAN network, every transceiver is responsible for translating digital I/O data into CAN signaling on the bus and all transceivers share some common features and ports. An example of a transceiver with its standard pins is illustrated in Fig. 3.5. TXD and RXD ports carry the digital I/O data, while CANH and CANL have adjusted analog voltage levels to ensure communication based on differential signaling. The VCC port is connected to a 5 V power supply, while GND connects to the ground reference for both analog and digital ports. Additional ports found on different types of transceivers are used to control the transceiver activity or to provide an additional power supply for digital signals.

A driver and a receiver inside the transceiver translate the digital signals on the TXD and RXD ports into signals interfacing with components related to CAN ports shown in the schematic. The receiver is composed of a Schmitt trigger that compares the differential signal to specified voltage levels, using hysteresis to reduce the receiver's susceptibility to noise. Nominally the RXD output is set to '1' if the differential signal CAN_{diff} is lower than 0.5 V and to '0' if it is higher than 0.9 V. Usually, CAN signals show a voltage difference on a 60 Ω load equal to 2 V in a dominant state and 0 V in a recessive state.

For an EMC analysis a critical part of the transceiver is the output stage, because, along with the recessive state voltage regulator, it defines the CAN ports impedance and describes also the non-linear behavior due to the MOS transistors switching between different operating regions. The circuit schematic shown in Fig. 3.6 is composed of two branches between the VCC-CANH and CANL-GND ports, respectively. Those branches are composed of a diode in series with a MOSFET transistor, representing the n-channel and p-channel connections respectively to the VCC and GND ports. Controlled by a signal coming from TXD port through the driver, the

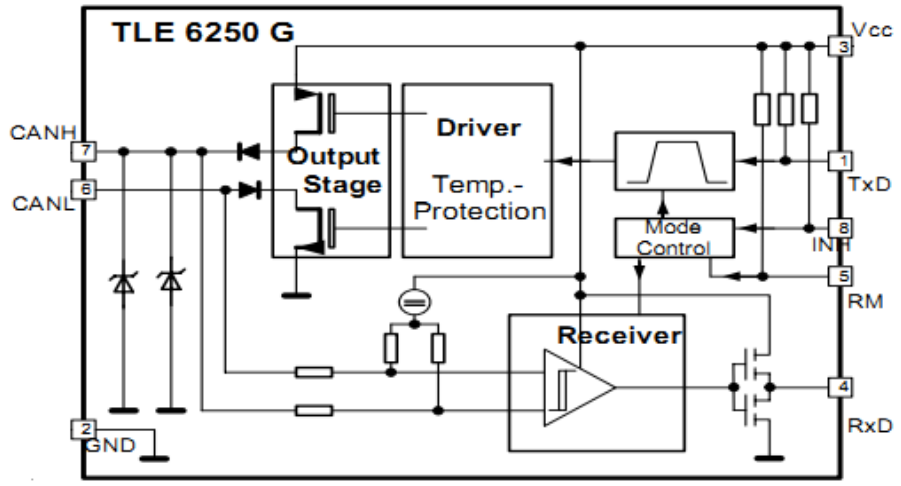

Figure 3.5. Transceiver TLE6250G structure [49]

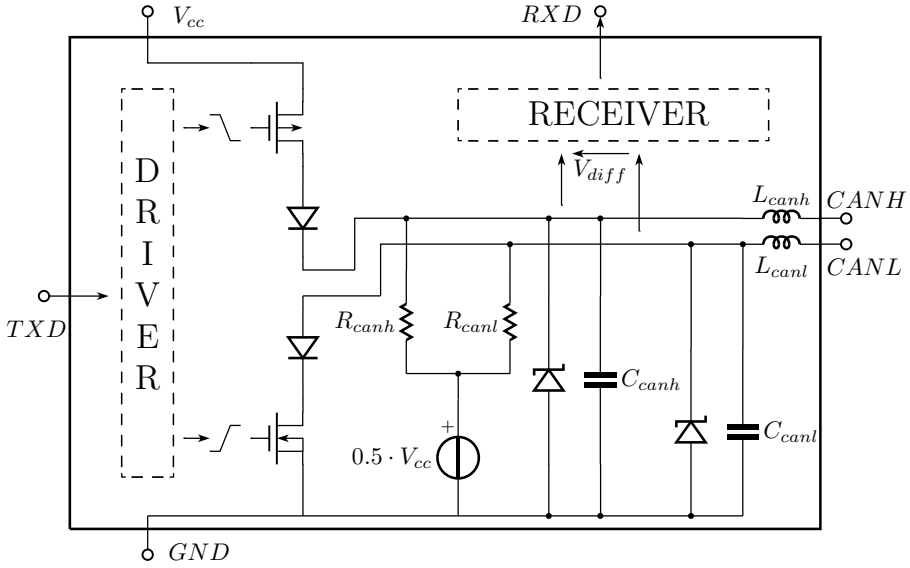

Figure 3.6. General CAN output stage schematic

transistors work as switches set by the transceiver state. They are both turned on in the dominant state and the CANH-CANL voltage levels are primarily determined by the MOSFETs, diodes and any external load placed between the CAN ports. In the recessive state both transistors are turned off and voltage levels on the CAN ports are set by an ohmic voltage divider with series resistances having a nominal value of $R_{can} = 10 - 30$ kΩ. These resistors determine the bias voltage level as a fraction of the power supply voltage, nominally 0.5 VCC. When all CAN transceivers in the

network are in the recessive state, no current flows through the transistors and the CANH and CANL port voltages are weakly driven by this block.

CAN ports are often affected by high voltage transient waveforms such as those produced by ESD, therefore protection diodes are placed between CANH/CANL and GND to ensure that transient current do not damage internal circuitry. In the schematic, parasitic elements such as package inductances (L_{canh}, L_{canl}) and port capacitances (C_{canh}, C_{canl}) are included to assess the port impedances correctly at high frequencies.

To better understand the failure mechanisms of a CAN transceiver, two ICs made by different suppliers were selected to be tested for immunity. The transceivers, specifically TLE6250G made by Infineon [49] and TJA1050 made by NXP [50], have been characterized through external measurements on the CAN ports; further details are available in section 4.1.3.

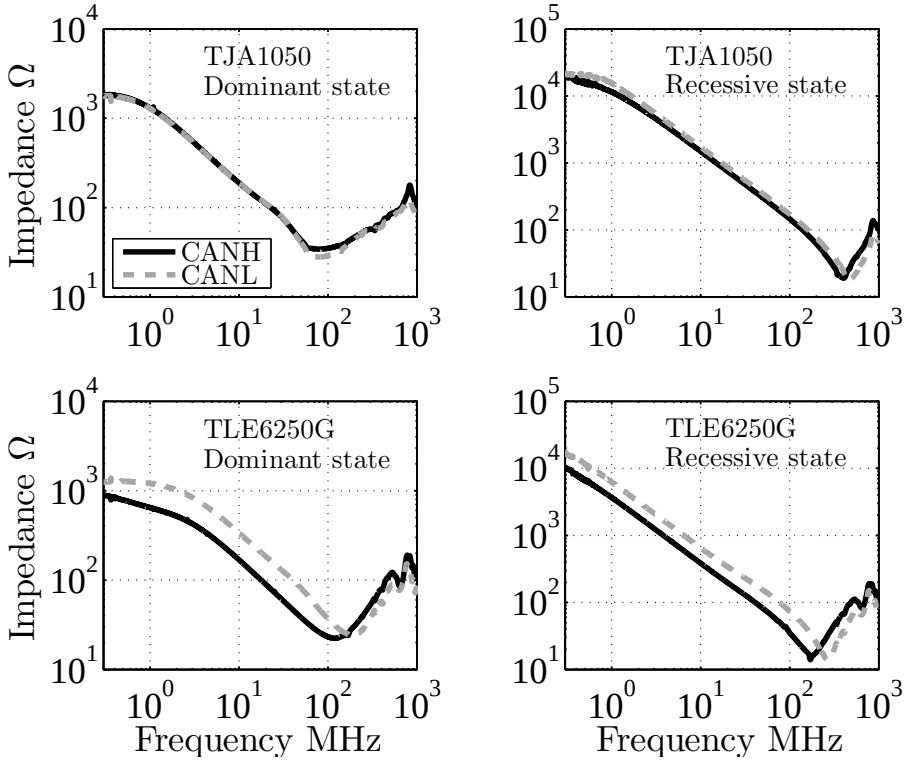

Figure 3.7. CANH and CANL port impedances in dominant and recessive state

In the recessive state, all impedances depicted in Fig. 3.7 start from a value equal to $10-30\,\mathrm{k}\Omega$ defined by R_{can}, decreasing by -20 dB/decade due to the C_{can} capacitance up to 200-300 MHz, where the inductance L_{can} begins to dominate. In the dominant state the impedance is about one order of magnitude lower due to the MOSFETs being turned on by the driver. Thus, during an immunity test the transfer function between the noise source and the transceiver depends on the IC state. The noise voltage peak amplitude seen on a CAN port will be higher when the device is in the recessive state and lower in the dominant state.

3.2 EMC Evaluation of CAN transceiver

The immunity of CAN transceivers to conducted disturbances is evaluated according to IEC/TS 62228 test method [51]. This test standard is a standardized common scale for EMC evaluation of CAN transceivers, where disturbances are capacitively coupled to the ports with a DPI circuit [18] and the susceptibility is characterized in terms of the incident noise voltage or power causing a failure. The transceiver's susceptibility is analyzed injecting different noise waveforms such as RF or pulse disturbances, whose parameters are varied accordingly to provoke failures in the network.

A simple CAN network consisting of 2 powered nodes was used to test the EMC behavior of a transceiver, where a communication test function was run and analog and digital port signals were observed to verify send-and-receive functionality and to detect any errors. The bus central termination consists of a resistor R = 60 Ω to comply with the CAN physical layer specification [48], while cable lengths were kept as short as possible to minimize propagation delay between transceivers.

Each CAN node consisted of a transceiver and decoupling network for the monitored pins. Node 1 operated as a transmitter for a bit pattern, which simulated a CAN message to be received and monitored at the RxD output ports of all nodes in the configured network. As a test communication, a signal with a 0-1-0-1 pattern was sent from the Node 1 TxD port, with a bit rate equal to 1 Mbps (T_{Bit} = 1 μs), the maximum possible bit rate on a standard high-speed CAN network. This signal is equivalent to a square wave with a frequency of 500 kHz. It should be noted that the digital signals flowing in and out from a transceiver are used to transmit both data and clock to CAN controllers. The rise and fall timing of a signal are used to align the digital clock and thus to determine the correct sampling times on the bit stream.

To determine the immunity of the transceiver against noise, disturbances were injected into the network increasing the amplitude until a fault was detected. As a fault criterion for immunity evaluation the maximum voltage variation on the RxD signal of every transceiver was checked. If a voltage variation equal or higher than 0.9 V was detected, a glitch occurred and an error event for this test was recorded. The bit period T_{Bit} was also monitored. A time variation equal or higher than 10% T_{Bit} (0.1 μs) was considered to be a fault.

3.2.1 Susceptibility to RF noise

To test the transceivers against RF narrow-band disturbances, the sinusoidal continuous wave source is a signal generator with an output impedance of $50\ \Omega$ and interferences are injected in the network with a pair of RC-serial circuits (R = $120\ \Omega$, C = 4.7 nF), which symmetrically couples the RF signal on CAN ports as common-mode noise, as depicted in Fig. 3.8. The RC circuit behaves as a high-pass filter with a cut-off frequency equal to $f_c = 1/(2\pi RC) = 282$ kHz of RC-serial circuit, thus the capacitance can already be considered as a short circuit in the frequency range of interest for noise injection. Voltages on the CAN lines were measured through a high-impedance RC probe built directly on the PCB in series with the $50\ \Omega$ input of the oscilloscope. The RC values were chosen equal to $R = 1$ kΩ and $C = 1$ μF in order to not load CAN lines and to not filter the CAN signals at frequencies above 160 Hz.

For each frequency starting from 1 MHz onwards, disturbances are injected in the network increasing noise power level up to 36 dBm until a fault is detected according to the susceptibility

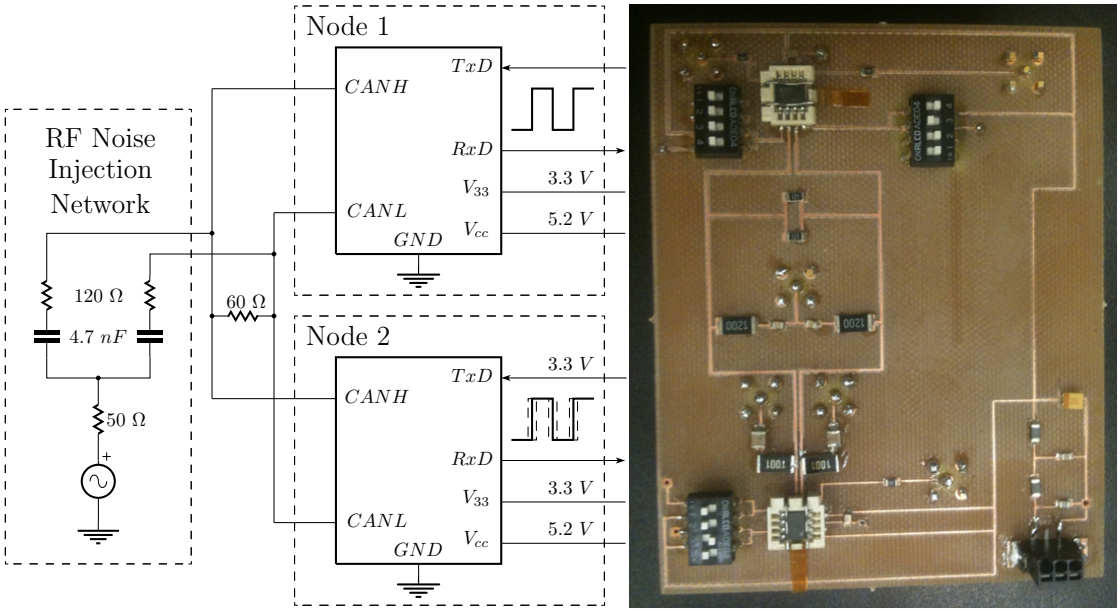

Figure 3.8. Schematic view of Direct Power Injection test circuit (left) and corresponding PCB (right) for evaluation of CAN transceiver susceptibility to RF disturbances

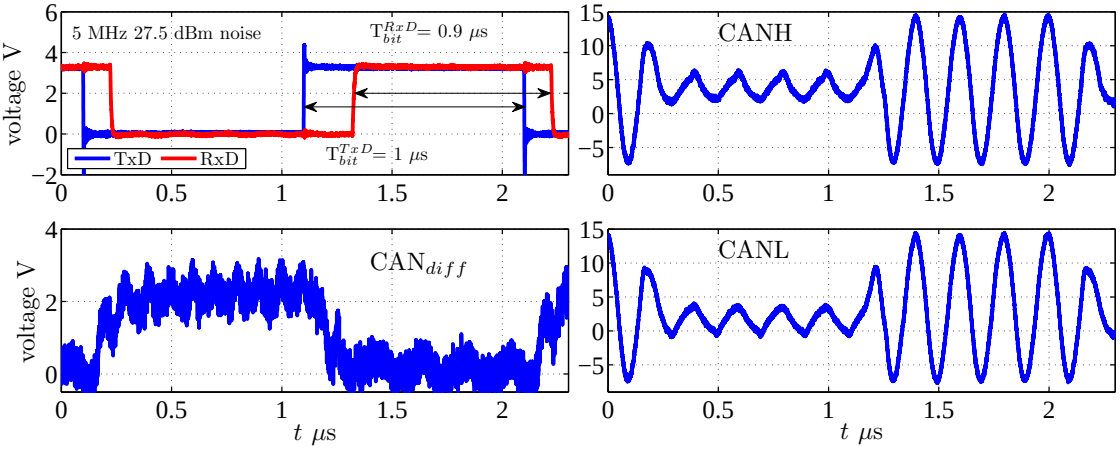

Figure 3.9. Node 1 TxD, Node 2 RxD digital signals (top left), analog common mode (top and bottom right) and differential (bottom left) CAN signals with 5 MHz RF noise injection on TLE6250G

criteria described in the previous section. The noise power level is defined from the forward power generated by the disturbance source [51], as the power that would be transferred if the load would be matched. Such condition is never met in a DPI test due to the combined impedance of the RC circuit and the IC, therefore only a fraction is transferred to the transceiver, depending on the IC port impedances at the corresponding noise frequency.

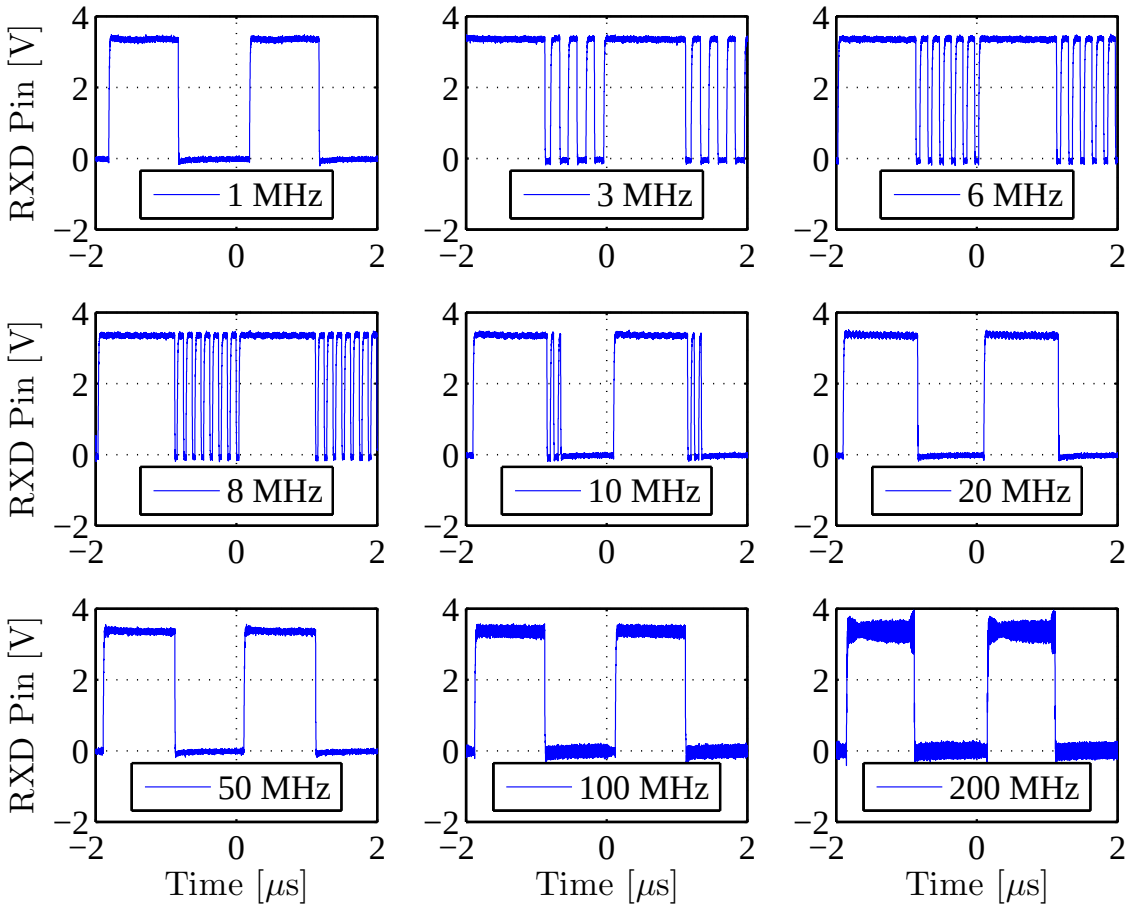

Figure 3.10. Node 2 RXD signal with +30 dBm noise injected at various frequencies on TJA1050

Waveforms related to a single DPI test on TLE6250G transceiver are shown in Fig. 3.9, where communication between nodes is stressed injecting RF noise at 5 MHz. Different RF noise effects in the network can be observed and their dependence on the bus state is evident. As described in subsection 3.1.2, in dominant state the impedance is about 1 order of magnitude lower than in recessive state, therefore the sinusoidal noise amplitude is reduced. Furthermore, the RF common mode noise is not symmetrically coupled due to the asymmetries between CANH and CANL ports. Such asymmetries slightly influence the differential signal as well and modify transitions between bus states. Thus a square wave signal transmitted over the network is seen by the receiver with a modified duty cycle, as the dominant state period last longer than the recessive one; this behaviour is identified as a main source of errors and it leads to a digital output signal affected by jitter, whose amplitude fulfills the specified susceptibility criteria. The RF noise power level required to record a failure on RxD signal is 27.5 dBm at 5 MHz.

To better understand the failure mechanism of CAN transceivers, a set of DPI measurements on TJA1050 is done by fixing the RF signal power at a constant level of 30 dBm; the waveforms

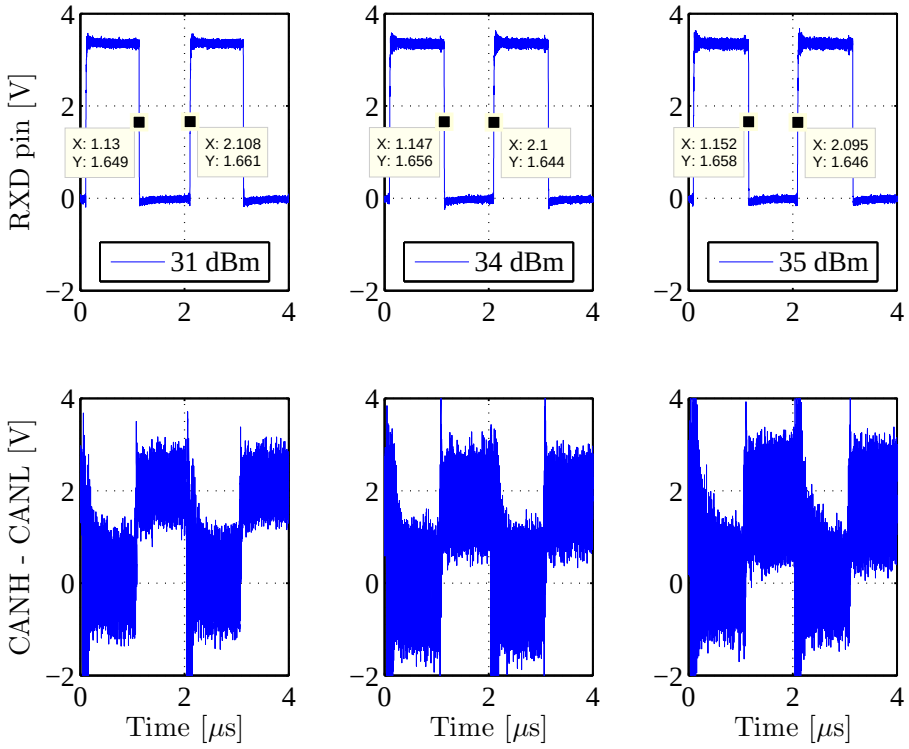

Figure 3.11. Node 2 RXD and analog differential CAN signals with a 50 MHz RF noise injected at various power level on TJA1050

shown in Fig. 3.10 were recorded at the RXD pin of Node 2 CAN transceiver varying the noise signal frequency. Two different behaviors can be observed depending on RF frequency:

- Between 1 and 15 MHz, the RF disturbances superimposed to CAN signaling are detected by the transceiver; a small part of noise signal, which is not symmetrically coupled to CAN bus lines and therefore not rejected by differential receiver, leads to errors on the digital output signal. The error type depends on the amount of injected RF power. Conducted RF disturbances in this frequency bandwidth are interpreted as meaningful signal and translated to digital errors as they are not filtered by timing characteristics of the receiver, such as setup time of input signal and delay between ports (Fig. 7 of [50]).

- When the injected signal frequency is higher than 15 MHz, the spikes' time widths on CAN analog signal are so short that they are not detected by the receiver and therefore not translated as spurious commutations on digital RXD output signal. As an example in Fig. 3.11 digital RXD output and analog differential CAN signals are shown when the network is affected by a 50 MHz sinusoidal noise. In order to recognize a CAN dominant state (RXD = '0'), the CAN signal has to be higher than the 0.9 V threshold for a time interval known as 'setup time'. While this intrinsic feature helps the receiver to filter noise spikes and remove error on digital output, it also increases the duty cycle of output RXD

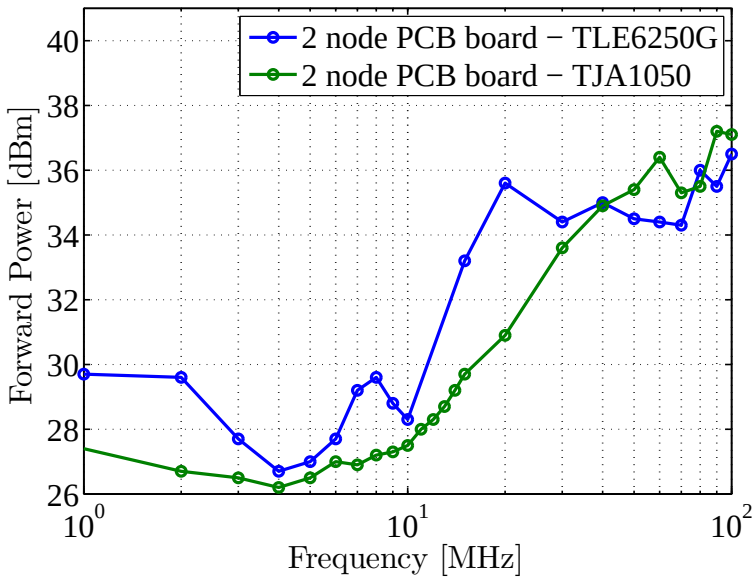

Figure 3.12. CAN transceiver immunity graphs for RF noise

signal: the '1' bit period becomes longer than '0' bit period, as it can be noticed in the data tips of Fig. 3.11.

In order to be able to quantify the CAN transceivers immunity, DPI test are run increasing interference signal amplitude until the IEC/TS 62228 failure criterion on RXD signal output [51] is violated and the measurements are summarized in the immunity graph shown in Fig.3.12. In both transceivers, the immunity threshold is lower between 1 and 10 MHz and then increases with frequency. This behavior can be qualitatively explained by looking at the previous examples depicted in Fig. 3.10-3.11, which show the CAN signaling in the presence of a 5 and 50 MHz RF noise. A CAN signal is less affected by high frequency noise due to intrinsic delay between IC ports: time widths of noise spikes decrease with frequency so that the disturbed CAN signal does not stay over the logic commutation threshold long enough to let the receiver recognize the disturbances as a CAN state change. Even if the disturbance is filtered by differential transmission, the transceiver is more susceptible to RF noise whose frequency is close to CAN signal bandwidth: noise waveforms are interpreted as meaningful signal and translated to digital errors.

3.2.2 Susceptibility to EFT noise

EFT noise was injected into the network through a pair of capacitors (C = 1 nF) which symmetrically coupled the EFT signal to the CAN ports as common-mode noise. To determine the immunity of the transceiver against EFT noise, the EFT amplitude was set to 10 V and increased until a fault was detected.

The EFT susceptibility test was carried out on the TLE6250G and TJA1050 transceivers, soldering the ICs to the PCB shown in Fig. 3.13. The power supply was decoupled from the IC using

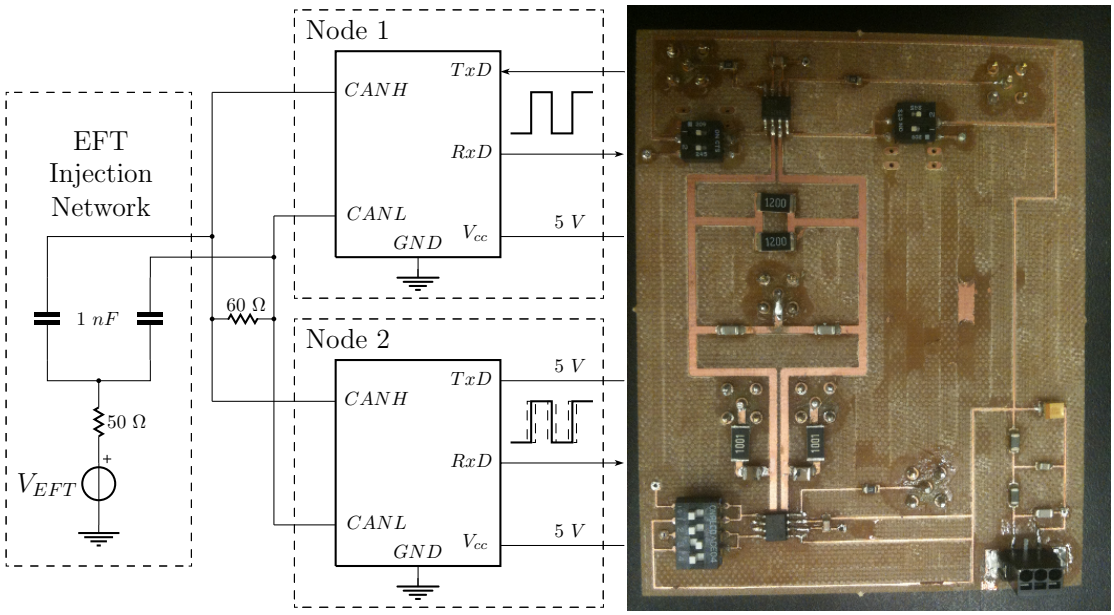

Figure 3.13. Schematic view of Direct Power Injection test circuit (left) and corresponding PCB (right) for evaluation of CAN transceiver susceptibility to EFT disturbances

a filter composed of ferrite beads and capacitors to observe only CAN port failures.

The amplitude of the EFT injection was adjusted by changing the voltage on the EFT generator. For each amplitude the test was run for 1 minute, with a random delay between each EFT spike. The random timing was used to apply a voltage spike during all possible operating conditions. In this way, each transceiver was tested in both recessive and dominant states, and during transitions between different logic states.

The test results for both positive and negative EFT are collected in the graph depicted in Fig. 3.14. For each operating condition, the minimum EFT peak voltage required to provoke an error according to the susceptibility criterion of [51] is marked for each transceiver.

The operating condition least immune to EFT is during a state transition. As shown in the left graph of Fig. 3.15, even a low-amplitude EFT may trigger an error near a bit transition due to switching MOSFETs inside the IC; if the transistors don't switch on/off at the same time, CANH and CANL port impedances are very different and transient noise doesn't symmetrically couple to them, provoking multiple glitches on the output. Even if the RXD digital signal is not sampled near the transition, this error type may corrupt the clock signal embedded in CAN data [47] used to determine the optimal sampling time.

In the other graphs of Fig. 3.15, EFT waveforms are shown turning on ESD diodes on CANH and CANL, whose I-V characteristics are often not symmetric and present a snapback behavior (see section 4.1.5). In the third graph an error is present, because, after a negative EFT event, the positive voltage bounce on the CAN lines is high enough to bring the diode into the snapback region. In the transceiver TJA1050 CANH and CANL port do not display the same I-V characteristics for positive voltages; therefore the receiver sees a voltage difference and sends out a

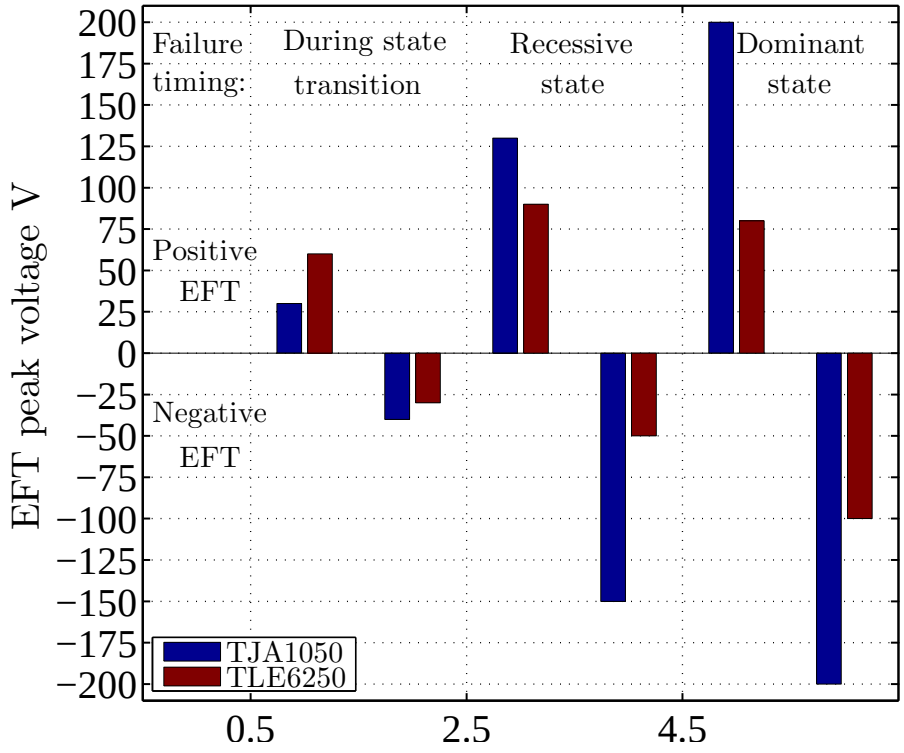

Figure 3.14. EFT Immunity graph on 3 operating regions for different transceivers

dominant bit instead of a recessive one. On the other hand, in the second graph no glitches are detected, because the amplitude of EFT event is not high enough to drive the ESD diodes into the asymmetric positive snapback region, thus ideal differential signaling and common-mode noise rejection are guaranteed.

Another cause of noise-induced failures on the receiver is shown in Fig. 3.16. Several EFT events on TLE6250G provoke glitches on the RXD signal. In the first two graphs, the transceiver is in the recessive and dominant states respectively. As the EFT common-mode noise couples to the CAN ports, it is partially transformed into the differential signal shown in the middle graphs and therefore a glitch appears on the RXD output, even without the diodes turning on. The receiver failure is due to the asymmetrical impedance of the CANH and CANL ports of TLE6250G, as depicted in Fig. 3.7. If the EFT peak voltage is higher as in the third graph, then the ESD diode is turned on and the glitch duration is longer due to the diode snapback effect.

It can be seen in Fig. 3.14 that TJA1050 is the most immune to EFT noise among the tested ICs in both the recessive and dominant states, because the port impedance symmetry is an important factor that affects the CAN transceiver's ability to reject common-mode EFT noise.

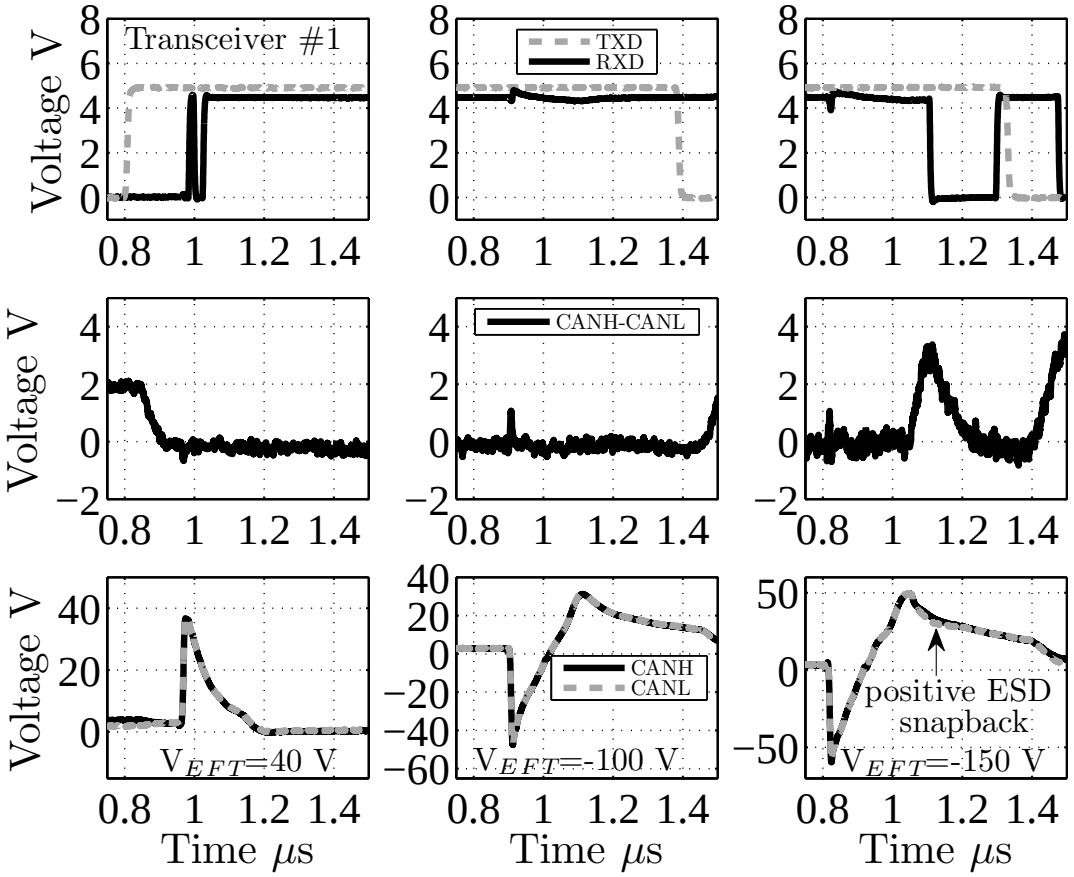

Figure 3.15. EFT waveforms from TJA1050, digital (top) differential (center) and CAN (bottom) signals; left: positive 40 V EFT on state transition, glitch on RXD; center: negative 100 V EFT on recessive state, no errors; right: negative 150 V EFT on recessive state, glitch on RXD due to diode snapback asymmetry

3.2.3 Chapter Summary

In this chapter, an analysis of IC EM Immunity has been reported, carried out on a CAN transceiver by means of DPI on signal ports. Analyzing the effects of RF and EFT interferences, the noise power injected to provoke errors has to be significant, due to intrinsic noise resistant features, such as differential signaling and twisted pair transmission medium. The EM interference impact was analyzed both on digital I/O and CAN signal port and the CAN bus immunity to interferences injected in signal ports was characterized as a function of noise power and frequency. The main sources of communication failures are CAN port impedance asymmetry and ESD diode effects; these characteristics hamper ideal common mode noise rejection, because part of the interference is converted into differential noise. These features, along with IC commutation according to its logic state, need to be correctly addressed in the IC model generation in order to simulate immunity

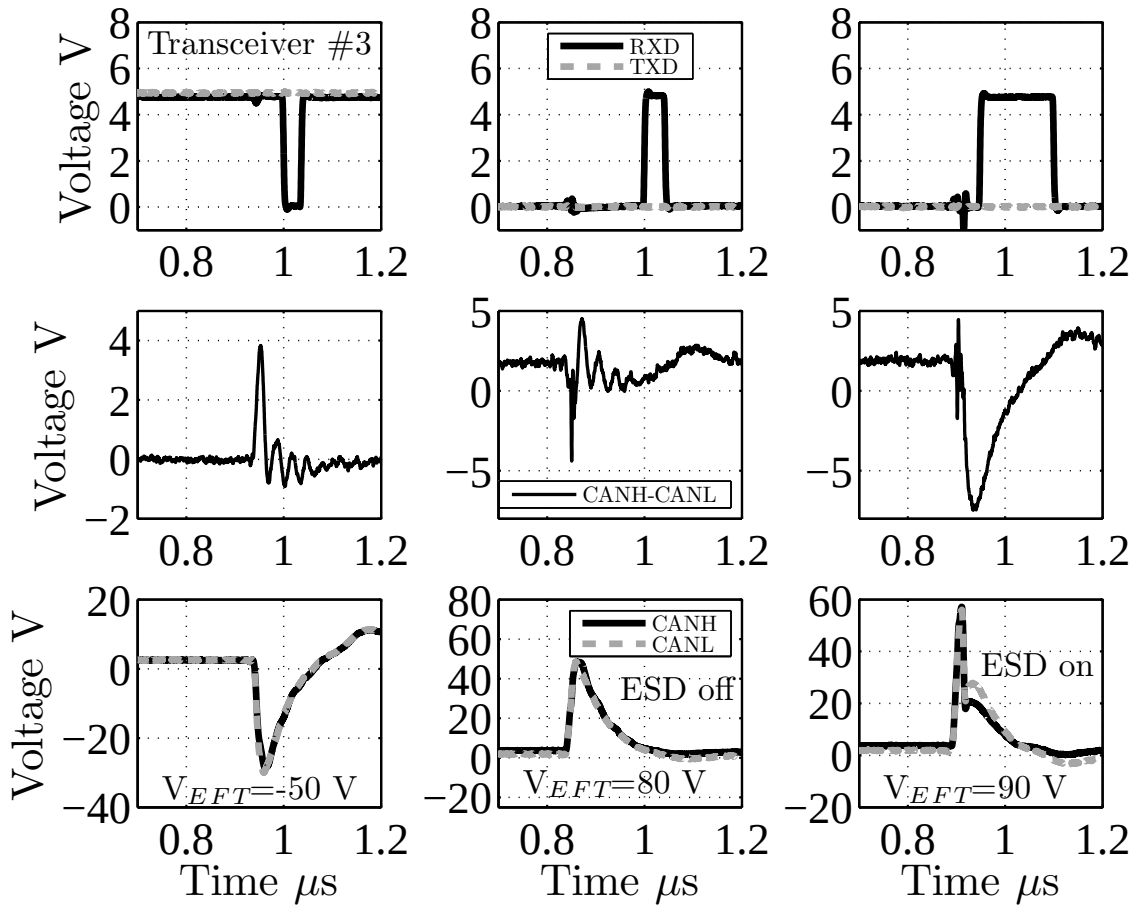

Figure 3.16. EFT waveforms from TLE6250G, digital (top) differential (center) and CAN (bottom) signals; left: negative 50 V EFT on recessive state, glitch on RXD due to CANH-CANL impedance difference; center: positive 80 V EFT on dominant state, glitch on RXD, diode turned off; right: negative 150 V EFT on dominant state, glitch on RXD, diode turned on

tests at component and system level; this is envisaged in the next chapter.

Chapter 4

IC Modeling Procedure for EM Immunity Evaluation

In order to simulate the operation of communication networks for the assessment of signal integrity (SI) and EMC problems, suitable IC models are needed. The models must be efficient and accurate enough to handle the complexity of actual simulation problems and to yield reliable predictions of reflections and signaling. In this chapter, a novel modeling procedure, based on an AMS block structure for the generation of IC immunity models from real measured data is presented. The new models aim at reproducing the electrical behavior of device ports and prove to be adequate to simulate the effects of noise injection in electrical equipments.

4.1 IC Modeling Procedure

The proposed approach to the modeling of active devices is via simplified equivalent circuit representations, in which the information on the internal structure of the device is used to derive a simplified equivalent circuit for each analog I/O port. The equivalent circuit is composed of various blocks, accounting for specific static or dynamic effects and delays between digital ports. The model is developed to be used in time-domain simulation, as the I/O ports of ICs are highly non-linear and the electrical properties are linked to their switching behaviour. Furthermore, the immunity criteria for communication networks are defined on time-domain signals, looking at failures related to glitches and jitter [51],that make a purely frequency-domain approach clearly unsuitable.

The models are implemented in VHDL-AMS language [34] - [52], a modeling environment created with the intent of enabling designers of analog/digital mixed systems to create and use modules that encapsulate high-level behavioral descriptions as well as structural descriptions of systems and components. The selected language provides both continuous-time and event-driven modeling semantics, particularly well suited for verification of mixed-signal integrated circuits. The model implementation and validation is done using Synopsys SABER and its VHDL-AMS simulator.

The IC modeling procedure can be divided into five step described in the following sections:

1. Block structure identification: identify components of critical circuit blocks for each port and internal connections from datasheet to model logic state switching structure.

2. Logic state static characterization: evaluate DC port I-V values in every logic state to fit component parameters

3. Port parasitic element evaluation: estimate LC parasitic elements in port circuit blocks from frequency-domain impedance measurements.

4. Internal block behavioural modeling: estimate a behavioural model to take into account internal links from IC switching and DPI measurements in time domain.

5. ESD protection structure analysis: estimate I-V curve of ESD protection diodes through TLP measurements to analyze port transient behaviour.

The procedure is validated on the TLE6250G CAN transceiver, whose noise immunity was analyzed in the previous chapter. The developed model must be able to estimate analog noise effect on CAN transceiver ports according to its logic state and evaluate noise impact on digital output in time domain according to IEC immunity criteria [51]. The CAN transceiver model can be used for immunity evaluation of RF noise up to 100 MHz, which has been chosen as an upper frequency limit, as the transceiver were proven immune to higher frequency noise in section 3.2.1.

A CAN transceiver was chosen as a test case because no transistor-level model is publicly supplied by the IC manufacturer, therefore the model parameters has to be extracted from measurements or taken from the datasheet. Furthermore, to the author's best knowledge the behavioural models available in literature have not taken into account the IC susceptibility to RF noise. Several mixed-mode models of a CAN transceiver were developed to evaluate complex network topologies, signal integrity [53], transceiver finite state behavior, CAN network fault analyses [54] and verification of internal vehicle networks [55]. An analysis of ESD diodes impact on differential signaling was carried out in [56], when sinusoidal noise is injected in an automotive network. However the growing complexity of CAN networks operating in a noisy environment demands for a refinement of transceiver models, including noise immunity features; non-idealities on transmitter/receiver differential signaling have to be implemented in the model to correctly evaluate noise effects on CAN communication system. Combined with wire models and other bus components, EMC assessment of a complete CAN network can be carried out.

It is relevant to remark that the outlined procedure is not restricted to CAN transceiver, but may be applied to any IC used in a communication network. For example a transmitter or receiver of automotive or avionic bus (MOST, LIN, Flexray, ARINC, etc...) can be modeled taking into account their susceptibility to RF or transient noise.

4.1.1 Block Structure Identification

The first step of the modeling procedure is to identify the critical ports for the immunity behaviour of the IC. In a CAN communication system, disturbances are typically injected in the bus network or through power supply, therefore in VHDL-AMS modeling environment the transceiver ports that could be affected by noise are modeled as analog ports, while other pins carrying control

signals for the IC can be defined as digital ports. Afterwards, a block circuit library is created to describe the IC behaviour; the blocks can be divided in two types:

- Port circuit block: it physically describes the electrical connection between the corresponding analog I/O port and the local ground and power supply pins. It is composed only of analog linear (resistors, capacitors, inductors) and non-linear circuit elements (transistors, diodes, TVS) whose behaviour is described by their relevant physical equations and their relevant parameters [52]. The port schematic is usually taken from the IC datasheet or from literature; it has to be able to describe the port impedance in every IC logic state and any non-linear effect in order to correctly assess the noise coupling in a system-level EM analysis. Common circuit structures are for example a CMOS stage or a LVDS (Low Voltage Differential Signaling) logic.
- Internal connection block: it describes the IC inner structure and the link between different I/O ports. The characterization of the internal switching structure is done using a behavioural model, as the physical structure of the IC logic core is protected by Intellectual Property of the producer and not disclosed. The block is composed of AMS elements, such as comparators, filters and digital delays, and it has to model the internal propagation delay between different I/O ports. Features like the input signal setup time and the voltage threshold have to taken into account to correctly assess the switching behaviour when driven by a noisy signal.

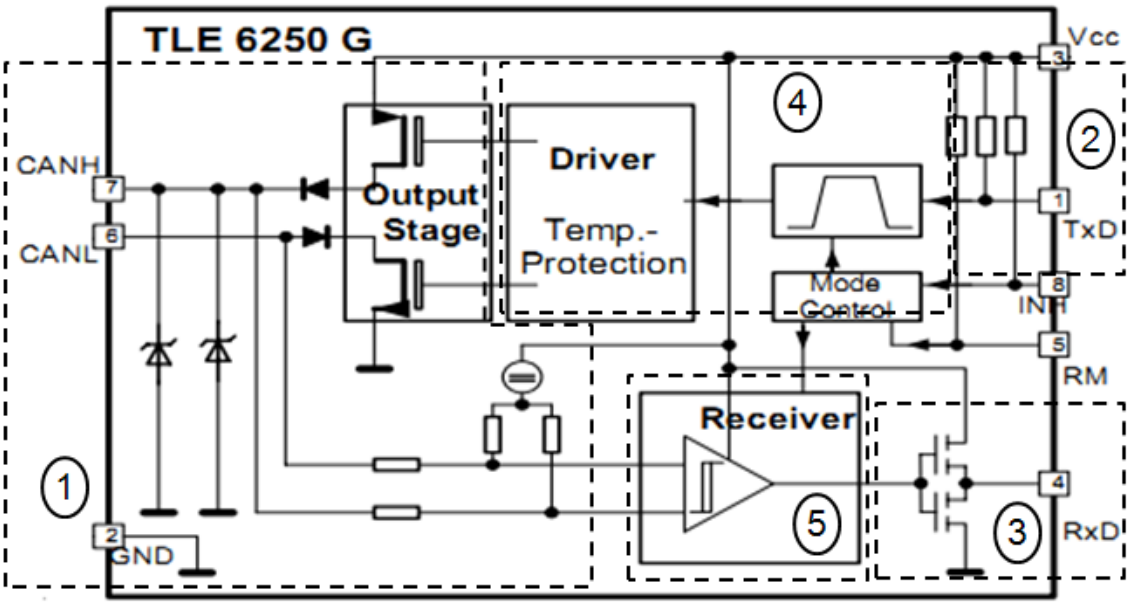

Figure 4.1. Transceiver TLE6250G block structure [49]

For the TLE6250G CAN transceiver device chosen as a reference, the block diagram of the AMS model is depicted in Fig. 4.1. Ground (GND), power supply (VCC), digital I/O (TXD, RXD)

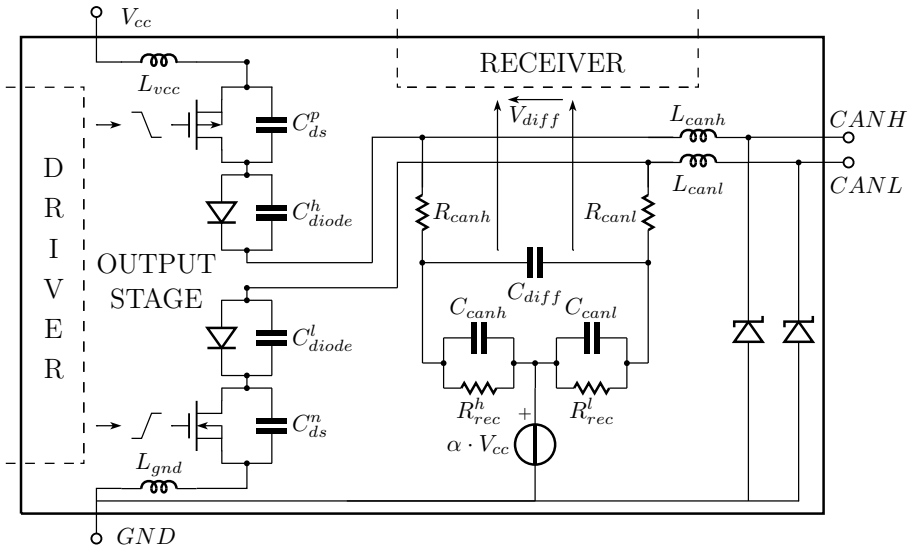

Figure 4.2. TLE6250G output stage block schematic

and CAN signaling (CANH, CANL) are modeled as analog ports, while control ports connected to external system (INH,RM) are defined as digital ports. With reference to Fig. 4.1 obtained from the datasheet [49], the block library includes:

1. CAN output stage (port circuit block): it defines the output impedance and takes into account the non-linear behaviour of CAN ports due to the MOS transistors switching between different operating regions. The circuit model shown in Fig. 4.2 is made of two branches between VCC-CANH and CANL-GND ports respectively. Each branch is composed of a diode in series with a MOSFET transistor, of type n-channel and p-channel if connected to VCC and GND ports respectively. The diodes limit the current flowing through the transistor when they are reversely polarized by external signals. Controlled by a signal from the driver, the transistors work as switches set by the transceiver state; for dominant state they are both turned on and CANH-CANL voltage levels are primarily determined by MOSFET non-linear equations and corresponding parameters, such as voltage threshold V_{th} and transconductance k [52]. On the other hand, in recessive state both transistors are turned off and voltage level on CAN ports is set by the voltage regulator. This voltage divider is connected to CAN ports through series resistances with a nominal value of $R_{rec} = 20$ kΩ, defining a bias voltage level as a fraction α of power supply, nominally 0.5 VCC. When all CAN transceivers in the network are in recessive state, no current flows through the transistors and therefore CANH and CANL port voltages are weakly driven by this block. Furthermore, parasitic elements such as package port inductances (L_{vcc}, L_{gnd}, L_{canh}, L_{canl}), diode, MOS drain-source and package capacitances (C_{diode}, C_{ds}, C_{can} and C_{diff}) and recessive state series resistances R_{can} have to be included in the model to define correctly port impedances and switching behaviour between states. Two ESD protection diodes are used to protect CANH and CANL from high-voltage transient and discharge to ground any

current that could damage the logic core. It is relevant to remark that the output stage block is directly connected to VCC port and therefore the transceiver voltage dependency from power supply is integrated in the model's electrical equations; the influence of non-ideal effects of power supply lines and of possible variations of supply voltage can be included in AMS simulations to predict proper output current and voltage values.

2. TXD (port circuit block): it is composed of a pull-up resistor R_{pull} connecting TXD port to VCC, in order to put the transceiver in a recessive state unless a dominant bit is received by the port. Series resistance R_{TXD}, package capacitance C_{TXD} and inductance L_{TXD} is added to assess port impedance.

3. RXD (port circuit block): a CMOS output stage, driven by the receiver internal block, connects the RXD output port to GND and VCC. MOSFET drain-source capacitances (C^n_{RXD},C^p_{RXD}), series resistance R_{RXD} and package inductance L_{RXD} is added to model port impedance.

4. Driver (internal circuit block) : after processing the TXD input waveform through a high-impedance comparator, the block transforms the digital signal to analog waveforms driving gate-source voltage of MOSFET transistors. Several parameters, like the comparator's voltage threshold, the rise and fall time of transistor driving signal and asymmetric digital delays between ports and driver, can be set to accurately model transitions between states.

5. Receiver (internal circuit block) : the differential analog signal from CANH and CANL ports is processed by the receiver and sent to RxD output port. The receiver is composed of a Schmitt trigger (a comparator with hysteresis), which compares the differential signal with specified voltage levels and sends a digital bit through the transceiver logic core to RxD selecting between recessive and dominant state. In the model shown in Fig. 4.3, the logic core behavior is modeled as an LC circuit filtering the signal before it is processed by the Schmitt trigger; the transceiver internal delay is taken into account by an asymmetrical delay in the A/D block to correctly address signal timing between CAN and RxD ports. The net effect is that the RxD output moves to a new logic state only after a received signal crosses the voltage thresholds for a certain setup time; even if the Schmitt trigger output is prone to spurious switching due to noise from the environment, the filter should suppress high frequency interferences and fast transient pulses, ensuring that the output swaps only when a state switching actually occurred in the network.

4.1.2 Logic state static characterization

A first estimation of the port circuit's parameters is done by measuring the DC voltage on the relevant pins in every logic state of the IC. During the measurements, a logic signal on the input port drives the IC in high and low logic state while the other ports are loaded in their usual operating conditions; for example, digital output ports are connected to high impedance loads. Furthermore, DC resistance port values are measured with a multimeter or taken from the IC datasheet. It has to be noted that all measurements are done between the relevant port and the local ground pin, which has to be connected to the global ground of the test setup.

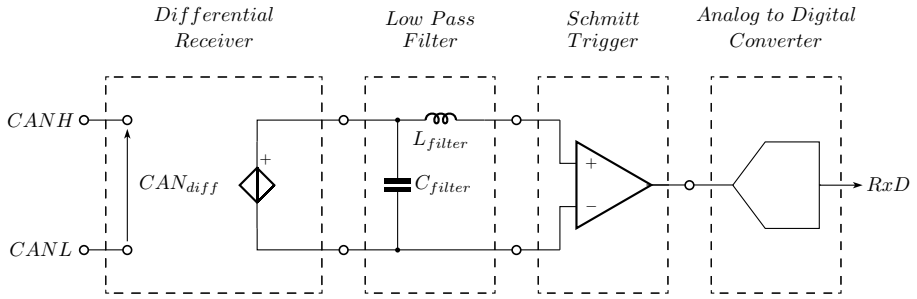

Figure 4.3. Receiver block layout

In a real CAN network, a transceiver is connected through a wire stub to the main CAN bus which is terminated by two 120 Ω resistors at both ends to ensure impedance matching in the transmission line and to minimize reflection effects. Hence, a differential impedance of 60 Ω is found between CAN ports on every node and therefore the electrical behavior of a transceiver is evaluated in the measurement setup shown in Fig. 4.4. Dominant state voltage levels on CAN ports are used to estimate the parameters ($Vth_n = Vth_p = 0.1$ V, $k_n = 7.8$ mA/V^2,$k_p = 9.5$ mA/V^2) of output stage MOSFET transistors, being in the triode region of operation. When the transceiver is in recessive mode, MOSFETs are in cutoff region, CANH and CANL port are at the same voltage levels and no current flows through the output stage and the 60 Ω resistor; therefore the voltage regulator parameter α can be estimated from recessive voltage levels and found equal to $\alpha = 0.487$, lower than 0.5 nominal value. Voltage divider resistances values are set to $R^h_{rec} = R^l_{rec} = 20$ kΩ, while TXD pull-up resistance is equal to $R_{TXD} = 25$ kΩ.

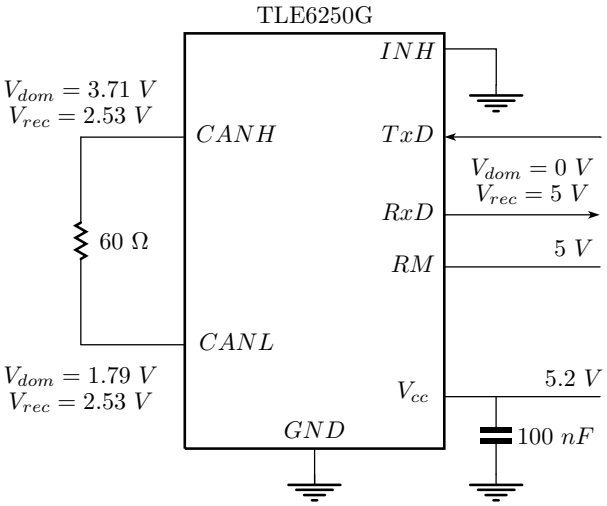

Figure 4.4. Transceiver test circuit for static characterization with relevant voltage levels in dominant and recessive state.

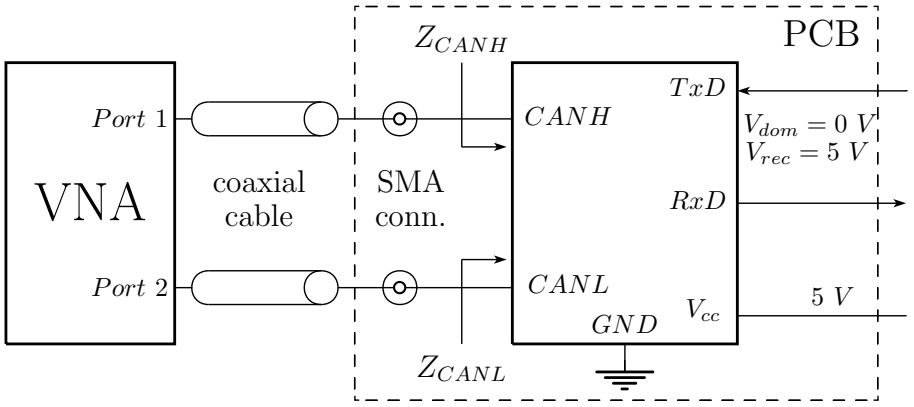

Figure 4.5. Measurement setup for estimating CANH and CANL port impedances.

4.1.3 Port parasitic element evaluation

In order to assess in a DPI test the amount of noise power actually transferred to the transceiver, port impedances need to be correctly modeled in both logic states. To extract the port impedance, the component is mounted on a PCB with the IC ground pin linked to its solid copper ground plane; SMA connectors are soldered to the PCB and linked to the IC ports through a short copper line. Connecting the Vector Network Analyzer to the PCB through a coaxial cable and calibrating the VNA to the end of SMA connectors, a S-parameter measurement is performed on the pins to measure the impedance, as shown in Fig. 4.5. If needed, the PCB impedance without the IC can be measured and deembedded; as the maximum noise frequency used in the DPI test is 100 MHz, no PCB characterization was done and its electrical behaviour was considered ideal. The IC ports are loaded with the VNA input impedance, which is composed by a $50\ \Omega$ resistor in series with a high-value capacitor acting as a DC block. Furthermore, the VNA performs a low signal measurement testing the behaviour of the port circuit around its operating point; therefore the parameters of any non-linear components have to be characterized in other modeling steps.

Fig. 4.6 shows the impedances seen at CANH and CANL ports, recorded with the transceiver set in dominant and recessive state. Across the bandwidth of the DPI test, the device structure shows a smooth capacitive behaviour, up to 80-100 MHz where a parasitic inductive load due to bonding wires and IC frame package is detected. The Figure compares the measurements with the responses of the lumped equivalent circuits of Fig. 4.2, whose parasitic element values have been estimated via simple fitting. Impedance curves measured in recessive state are preliminary employed to estimate capacitances and inductances belonging to the voltage regulator block, while parasitic elements of the output stage are determined afterwards from dominant state impedance.

4.1.4 Internal block behavioural modeling

In a mixed-signal model construction, the interaction between ports has to be correctly assessed. A square wave signal is sent on the input port to estimate the internal delays and the switching voltage thresholds of I/O signals. Then, DPI susceptibility measurements are carried out on the IC

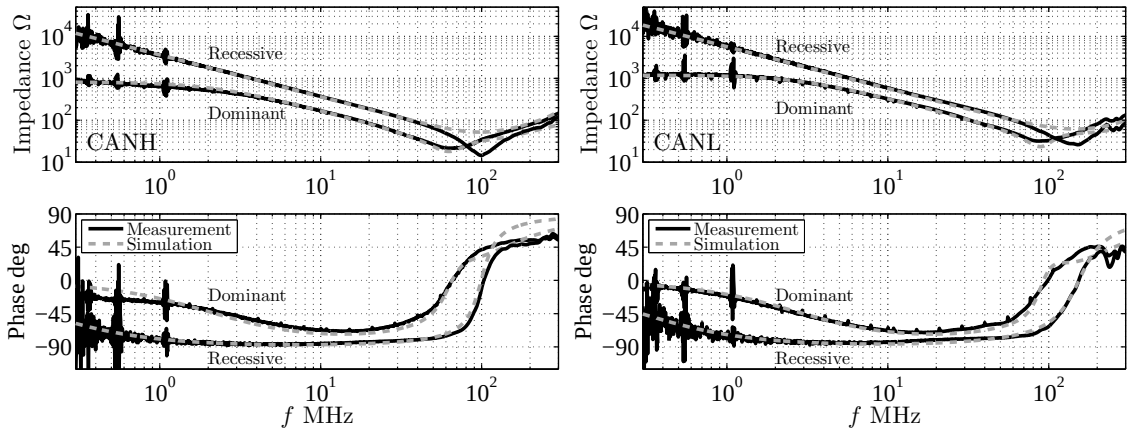

Figure 4.6. CANH (left panel) and CANL (right panel) port impedances in dominant and recessive state. Solid lines: real measurement carried out on the TLE6250G transceiver; dashed lines: prediction obtained via the equivalent circuit of Fig. 4.2.

Circuit Block	Element	Value	Element	Value	Element	Value	Element	Value
Output stage	R^h_{rec}	20 kΩ	R^l_{rec}	20 kΩ	R_{canh}	50 Ω	R_{canl}	50 Ω
Output stage	C_{canh}	50 pF	C_{canl}	25 pF	L_{canh}	40 nH	L_{canl}	40 nH
Output stage	L_{vcc}	80 nH	L_{gnd}	100 nH	C_{diff}	5 pF	C^p_{ds}	20 pF
Output stage	C^n_{ds}	10 pF	C^h_{diode}	50 pF	C^l_{diode}	20 pF		
TXD	C_{TXD}	10 pF	L_{TXD}	20 nH	R_{TXD}	20 Ω		
RXD	C^n_{RXD}	5 pF	C^p_{RXD}	10 pF	L_{RXD}	20 nH	R_{RXD}	20 Ω

Table 4.1. Element values of port circuit blocks

signal ports usually affected by noise. The recorded waveforms are used as input for the complete IC model to fit the parameters of the behavioural internal connections.

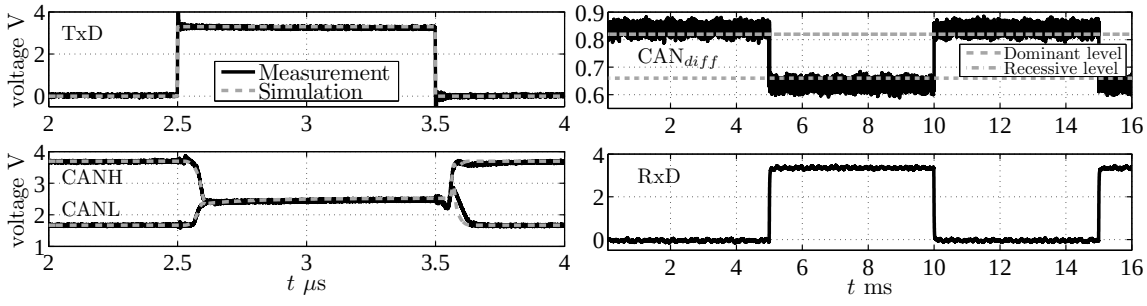

Figure 4.7. Left: port voltage responses (solid black curves) and model predictions (dashed gray curves) of the transceiver state transition driven by a 1 Mb/s input signal. Right: square wave differential input signal for voltage level estimation of receiver hysteresis

The measurement setup shown in Fig. 4.4 is used to verify the proper functionality of the transceiver when state transitions occur, driven by a 1 Mb/s switching digital signal on TxD port. The transceiver internal delay from a TxD digital event to the corresponding CANH and CANL signal change is evaluated from the measured waveforms shown in Fig. 4.7; the delay (30-40 ns), the rise and fall time of transistor driving signals (80-90 ns) and the voltage threshold (2 V) are taken into account in the model, fitting the driver block parameters and thus estimating the transient waveform of MOSFETs gate-source voltages. The good agreement between measurements and simulations confirm that the model properly represents I/O timing and may correctly validate signal integrity for CAN systems operating at the highest bit rate possible.

As the susceptibility criterion used in the immunity test relies on RxD signal analysis, the characterization of the receiver functionality is of paramount importance to correctly predict noise influence on bus lines, thus the parameters of the receiver block depicted in Fig. 4.3 have to be carefully characterized. First of all, the differential analog signal from CANH and CANL ports is the input for the Schmitt trigger; recessive-to-dominant and dominant-to-recessive transitions on the bus line are detected on different voltage levels due to the comparator inherent hysteresis. A differential square wave signal is applied to CAN ports and its high and low voltage levels are reduced until glitches and spurious commutations are found on RxD signal in both logic states; a low frequency (100 Hz) signal is preferred, as shown in Fig. 4.7, to avoid measurement errors from parasitic capacitance discharge during transitions.The receiver characterization is done on a transceiver in recessive state fixed to a '1' logic level on TxD port, as the IC is set in this condition while not transmitting any data in the bus.

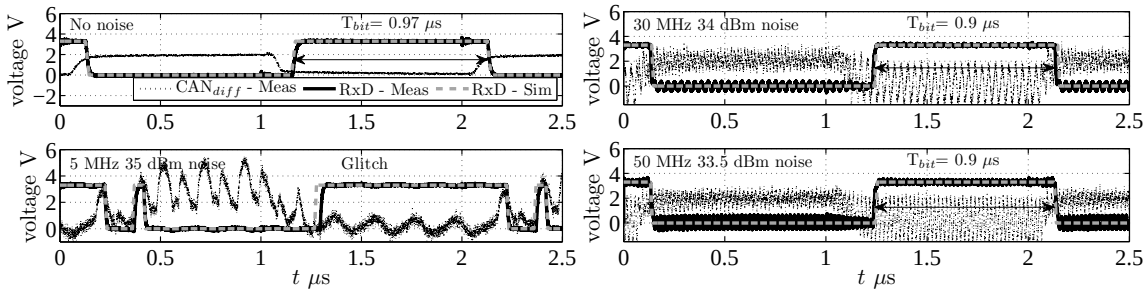

Figure 4.8. Noisy CAN port voltages and corresponding digital output signals for receiver characterization; noise frequency and power level reported along susceptibility criterion infringement; dotted black lines : measured noisy differential CAN signal ; solid black lines : measured RxD signal; dashed grey lines: predicted RxD signal

Additionally, the low-pass response of the logic core has to be assessed. The receiver behaviour affected by sinusoidal noise is evaluated in the DPI test setup shown in Fig. 3.8. Several faulty transmissions in the CAN network, along with a set of noiseless waveforms, are reported in Fig. 4.8 with various noise frequency and injected power level; it is worth noting that high power level noise (35 dBm) induces spurious commutations on RxD output in the 1-10 MHz bandwidth, while at higher frequencies only errors due to jitter are detected. Recorded waveforms of CAN differential signal are used as an input for the receiver block model; a good accuracy level is obtained in simulation environment by modeling the transceiver low-pass behaviour as a Bessel 2nd

order LC filter ($C = 950$ pF, $L = 6276$ nH) with a cutoff frequency of $f_c = 2.5$ MHz.

4.1.5 ESD protection structure analysis

The ESD protection diode behaviour used to protect the ports from transient interferences has to be assessed to analyze IC susceptibility to EFT. In order to extract the I-V characteristic, a quasi-static Transmission Line Pulse measurement [57] was performed on CANH and CANL ports, collecting a number of voltage-current pairs from a 100 ns pulse waveform generated using the test setup depicted in Fig. 4.9. A 1-100 ns high-voltage Picosecond PulseLabs 2600C pulse generator was connected to the PCB-mounted transceiver and a 1 Ω resistor was placed in series with each CAN port in order to determine the current flowing through it. In the recessive state, a 1 Ω resistor does not significantly modify the port impedance. Voltages are measured using high-impedance probes built into the PCB and connected to the 50 Ω input of an oscilloscope.

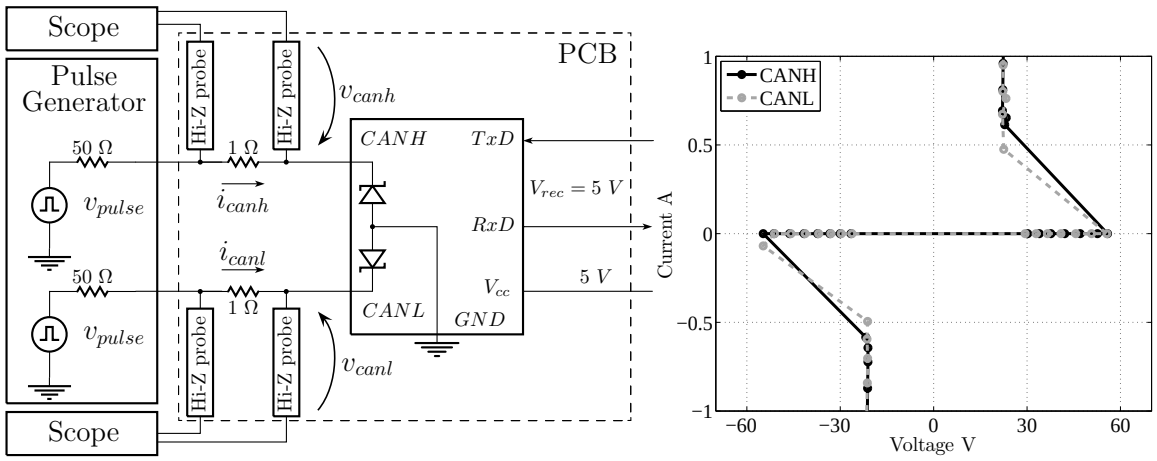

Figure 4.9. Left: TLP measurement setup on CANH and CANL ESD protection diodes. Right: measured I-V characteristics for the diodes between CANH-CANL and GND pins

The I-V diode characteristics are depicted in Fig. 4.9; the diodes exhibit a snap-back effect when they turn on both on positive and negative voltages, contributing to asymmetries in the CANH and CANL curves. Thus the ESD protection circuits may activate at different times and in a different way when affected by common-mode transient noise, transforming it into a differential disturbance. The ESD protection diode is implemented in VHDL-AMS using a behavioural formulation based on a state machine model [58]. In the analog domain, the ESD diode model is split into several modes (no conduction, reverse or forward conduction, snapback) and each operating region is associated to an equation mirroring the measured I-V curve. A state machine change conditions is defined to select the analog equation according to the behavioral ESD structure.

The implementation of the complete AMS model in the simulator is shown in Fig. 4.10. The IC ports are linked to the port circuit blocks (TXD, RXD, CAN output stage), while the internal circuit blocks (Driver, Receiver) model the connection between ports components, driving the gate signal of the MOSFET transistors. The schematic is used as as subcircuit in the following immunity simulations.

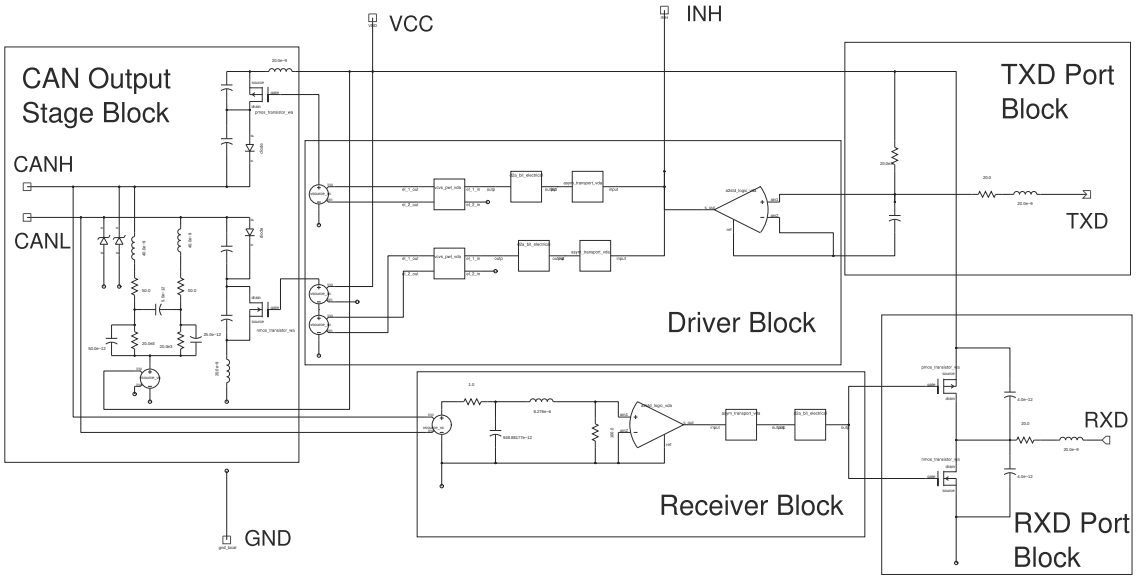

Figure 4.10. TLE6250G Transceiver AMS model

4.2 IC Model Validation

The proposed modeling approach is validated on several examples, predicting transient analog waveforms and digital I/O signals of the transceiver affected by common mode RF noise. The DPI test described in section 3.2.1 is carried out in simulation and the measured signals are used as reference waveforms; time domain responses are computed by means of Synopsys Saber.

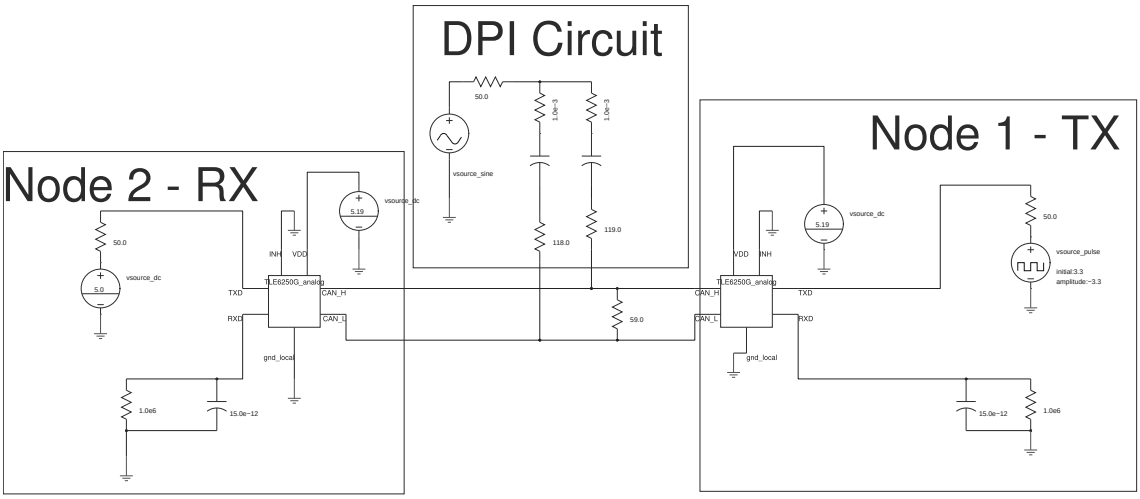

Figure 4.11. AMS model of the Direct Power Injection PCB for evaluation of CAN transceiver susceptibility to RF disturbances

The first test case is the injection of a RF signal with constant power level (30 dBm) at several frequencies up to 100 MHz, to correctly assess the transfer function between the noise generator and CAN ports, when Node 1 transceiver is on recessive or dominant state. Several waveforms reported in Fig. 4.12 confirm the capacitive behavior of the port impedances in recessive state, because the sinusoidal amplitude is reduced as the noise frequency increases. On the other hand, in dominant state the noise triggers a non-linear behavior: varying the voltage amplitude on CAN ports lead to a shift of the transistor operating region, from triode to saturation region and vice versa, thus producing a distortion of the sinusoidal waveforms. The proposed model is able to reproduce those features, validating noise injection simulations in the whole frequency bandwidth.

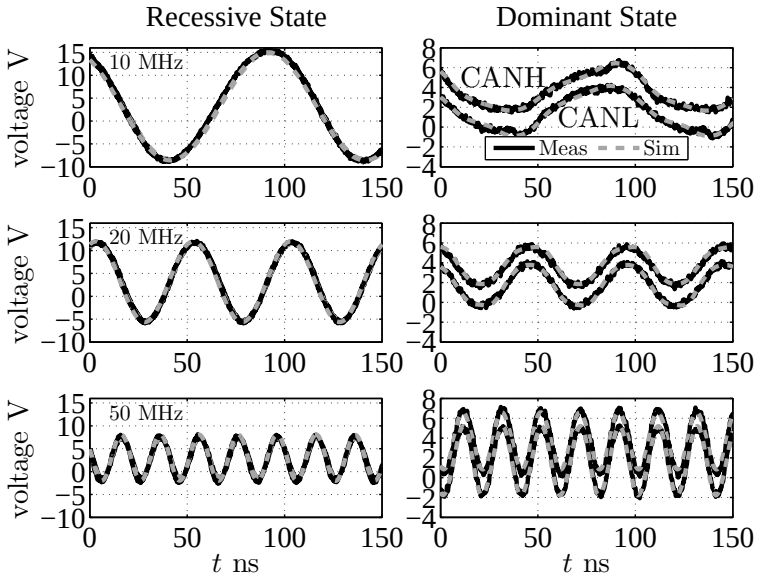

Figure 4.12. Noise injection with constant 30 dBm power level on CAN transceiver ports in recessive and dominant state. Solid black lines : reference. Dashed grey lines : prediction

The second test case is the simulation of a complete DPI test on the transceiver at a single frequency. 1 Mbps CAN communication between nodes is stressed injecting RF noise at 15 MHz, whose waveforms are shown in Fig. 4.13; noise power level required to record a failure on RxD signal is 33 dBm. The non-ideal asymmetries between CANH and CANL ports are correctly assessed in simulation, since the common mode noise is not symmetrically coupled to both bus lines, therefore slightly influencing the differential signal as well, and modifying transitions between bus states. Hence, a square wave signal transmitted over the network is seen by the receiver with a modified duty cycle, as the dominant state period lasts longer than the recessive one; this behavior leads to a digital output signal affected by jitter, whose amplitude fulfills the IEC susceptibility criteria [51]. The good agreement of the reported curves confirms the model capability to describe RF noise effects on the CAN transceiver and highlights the importance of taking into account the complex relation between the noisy analog differential signal and the digital output. The simulation time required to obtain these waveforms is 6.2 s, proving a good computational efficiency.

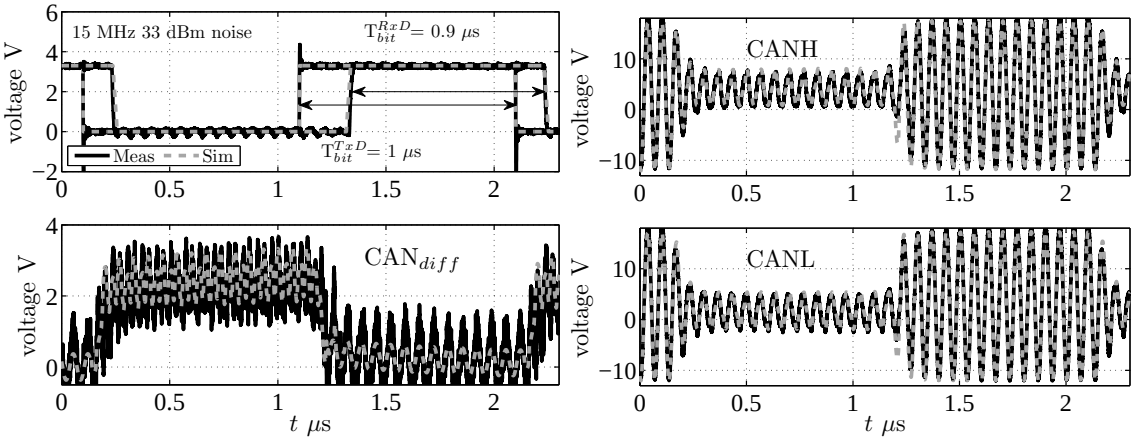

Figure 4.13. Node 1 TxD and Node 2 RxD digital signals and analog CAN waveforms in network depicted in Fig. 4.11 with 15 MHz noise injection; solid black lines : reference; dashed grey lines : prediction.

4.3 Immunity Simulation at component level

As an application example, the TLE6250G transceiver immunity model is used to reproduce a real DPI test at component level. Time-domain simulations are carried out on the schematic shown in Fig. 4.11 to generate an immunity graph according to the test procedure defined in [51]. As a test of the communication channel, a signal with a 0-1-0-1 pattern was sent from the Node 1 TxD port, with a bit rate equal to 1 Mbps. For each frequency point starting from 1 MHz onwards, disturbances are injected in the network increasing the noise power level up to 36 dBm; the RXD signal of Node 2 is monitored until a fault is detected according to the susceptibility criteria (glitches or 10% jitter). In order to obtain a complete immunity graph, the parameters of the RF noise source have to be varied in the DPI circuit, therefore time-domain simulations are run in three nested loops:

1. Noise frequency: the RF frequency of the noise source is the parameter varied in the outer loop, in order to scan the whole frequency bandwidth required by the immunity test.

2. Noise amplitude: in the middle loop the forward noise power is set at a value (20 dBm) low enough to not cause any immunity criteria violation in the whole bandwidth. The noise power level is then increased with a 0.5 dB step until a fault is found on the monitored signal. In simulation the noise amplitude is defined using the sinusoidal peak value of the RF source on an open circuit, therefore the forward power has to be converted to a voltage value according to the following equation:

$$V_{RF} = 2\sqrt{2 * 10^{\left(\frac{P_{dBm}-30}{10}\right)} * 50}$$

3. Noise phase: the last parameter to be set in the inner loop is the phase of the RF noise. While the transceiver transmits data at 1 Mbps during the DPI test, the CAN ports vary

their impedance depending on the logic state; thus in time domain the peak of the sinusoidal noise waveform can be coupled with the transceivers during a transition or in dominant or recessive state. In a real measurement, the noise phase is randomly generated by the voltage source and every possible combination of RF phase and transceiver state is evaluated by running the test for the 1-s dwell time specified in [51]. However, in simulation this condition is not true, therefore several simulations has to be run varying the phase angle between 0 and 360 °.

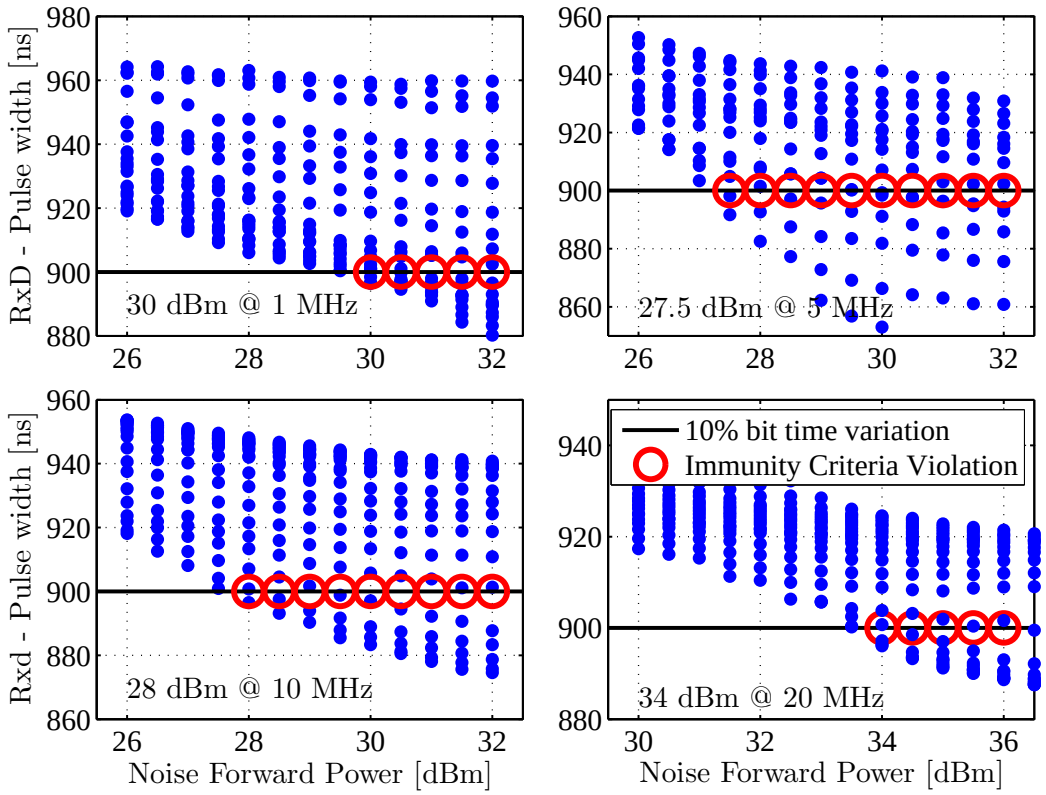

Figure 4.14. Node 2 Rxd signal pulse width jitter obtained in DPI simulation on TLE6250G transceiver for different noise frequencies, power level and phase

The simulation results of the DPI test on the TLE6250G transceiver are shown in Fig. 4.14. On each graph the pulse width of the positive bit of the node 2 RXD signal is plotted with the corresponding RF noise power: an immunity criteria violation is found when the pulse width is lower than 900 ns, as the node 1 TXD input signal has a T_{Bit} = 1 μs and therefore a 10% variation is detected. The effect of the noise phase on the test results can be clearly seen as different pulse width values are recorded for the same noise frequency and power. The lowest noise power value provoking a failure is then recorded for each frequency as the minimum level required to fail the immunity test. To obtain a jitter simulation graph, a number of 340 time-domain simulations are run for a single frequency, varying noise power and phase at each step by 0.5 dBm and 18 °

respectively; the simulation time is about 25 minutes.

The results are then collected into the immunity graph shown in Fig. 4.15 showing an excellent agreement between the data obtained by measurements and the simulated immunity model. At 1 MHz, the IC withstands 30.5 dBm and still operates correctly, while the model returns 30 dBm as a maximal acceptable value of the RF noise power. For the frequency range from 2 MHz until 10 MHz this value decreases according to both setups, with a maximum error of 2.5 dB at 7 MHz between the two curves. For frequencies higher than 10 MHz, the IC is clearly more immune to interferences, as it withstands more than 33 dBm of RF noise, and it fully passes the DPI test on several frequencies being able to tolerate a noise power level of 36 dBm. To obtain the results of this test, the simulation time is about 10 hours on a common laptop; this is deemed to be an acceptable time for industrial needs.

It is ought to be noted that the immunity graph of the measured DPI test is not employed in the modeling procedure and only used as a reference to validate the simulated immunity curve. If the IC immunity criteria is modified for industrial needs, the model is still valid and can be used to estimate an immunity curve according to the new susceptibility functions.

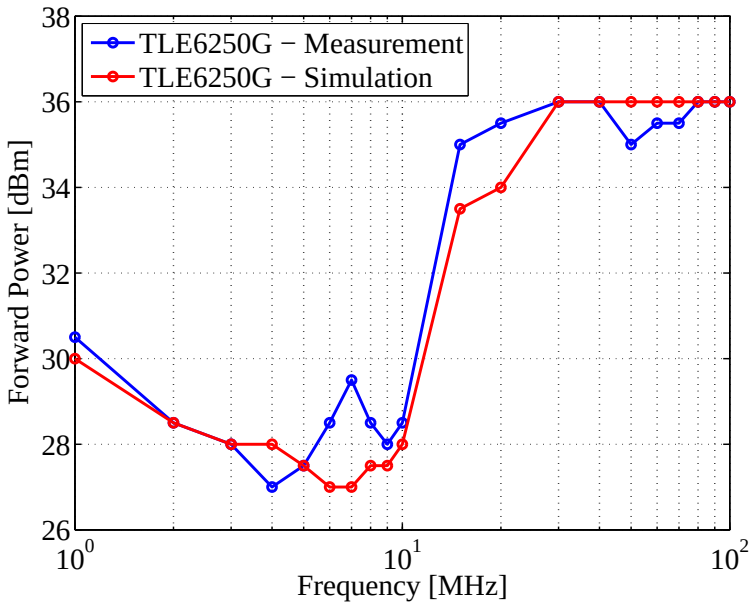

Figure 4.15. DPI immunity graph measurement and prediction on TLE6250G transceiver

4.4 Chapter Summary

A novel procedure is proposed for the IC modeling for mixed-signal immunity simulations of communication networks. The procedure is based on the use of schematic blocks, whose parameters are estimated from time and frequency domain measurements, allowing accurate and efficient reproduction of device terminal behaviors. The obtained models may handle RF noise up to 200

MHz injected and can adequately reproduce its effects on both analog and digital signals for SI and EMC investigations. A representative test case of a CAN transceiver was selected, for which the model construction parameters have been calculated and optimal settings have been selected ensuring high precision and efficiency. The model was integrated into a circuit simulator and validated at component level with the measurements detailed in the previous chapter. Its usefulness for a system level immunity simulation is analyzed in the following chapter.

Chapter 5

System-Level Noise Susceptibility Assessment

An analysis at system level regards the combination of equipment, integrated circuits, wiring and its load, in a standardized test equipment configuration.

In this chapter, the focus is on the modeling of the disturbance coupling and in their propagation inside the system down to the component. As a test case, the susceptibility of a CAN network is addressed in DPI and BCI tests highlighting the differences. The impact of wiring in the network robustness is considered, developing a wire model for time-domain simulations. To simulate a BCI test the complex relationship between the injection probe and the wiring needs to be understood and implemented in an accurate model.

5.1 CAN Bus DPI Test

To evaluate the noise susceptibility of a CAN network, a DPI test setup was assembled using a pair of commercially available boards. The first one is a Xilinx Spartan-3A Starter Kit board, based on a small size XC3S700A FPGA device, which is programmed to send and receive digital I/O and provide the power supply to the ICs. The second board is a Digilent FX2WW board where the TLE6250G CAN transceivers and the DPI subcircuit are mounted.

Two different CAN networks were assembled, with 2 and 3 transceivers respectively, whose topologies are shown in Fig. 5.1. Both topologies are based on a main bus, whose lengths are 4.3 and 9.3 meters respectively, and the TLE6250G transceivers are connected through wire stubs 0.3 meter long, linked with 3-way T connectors. The wires are shielded twisted pairs designed for CAN bus [59]; on both ends of the main bus, two $120\ \Omega$ resistors are placed between CANH and CANL wires, to match the characteristic impedance of CAN twisted wires [48]. RF noise is generated by the voltage source and injected through the DPI RC subcircuit (R = $120\ \Omega$, C = $4.7\ nF$) with a maximum noise power level equal to 40 dBm. CANH and CANL wires are connected to RC branches while wire shields are connected to ground; noise is injected directly into the wires without having to pass through the shield.

A 1-0-1 digital signal with 1 Mbps bit rate is used as a test communication waveform on TXD Node 1 input and the IEC immunity criterion [51] is checked on each RXD signal, that is the

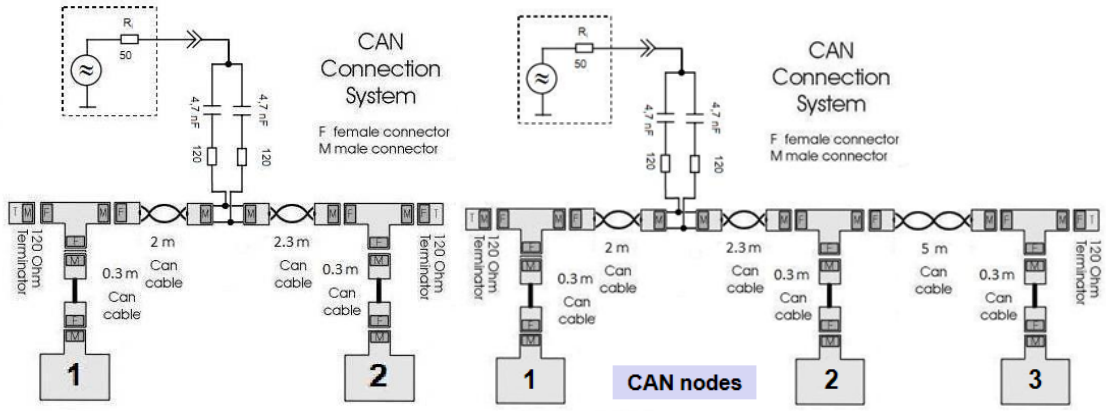

Figure 5.1. Left: 2 nodes network topology. Right: 3 nodes network topology

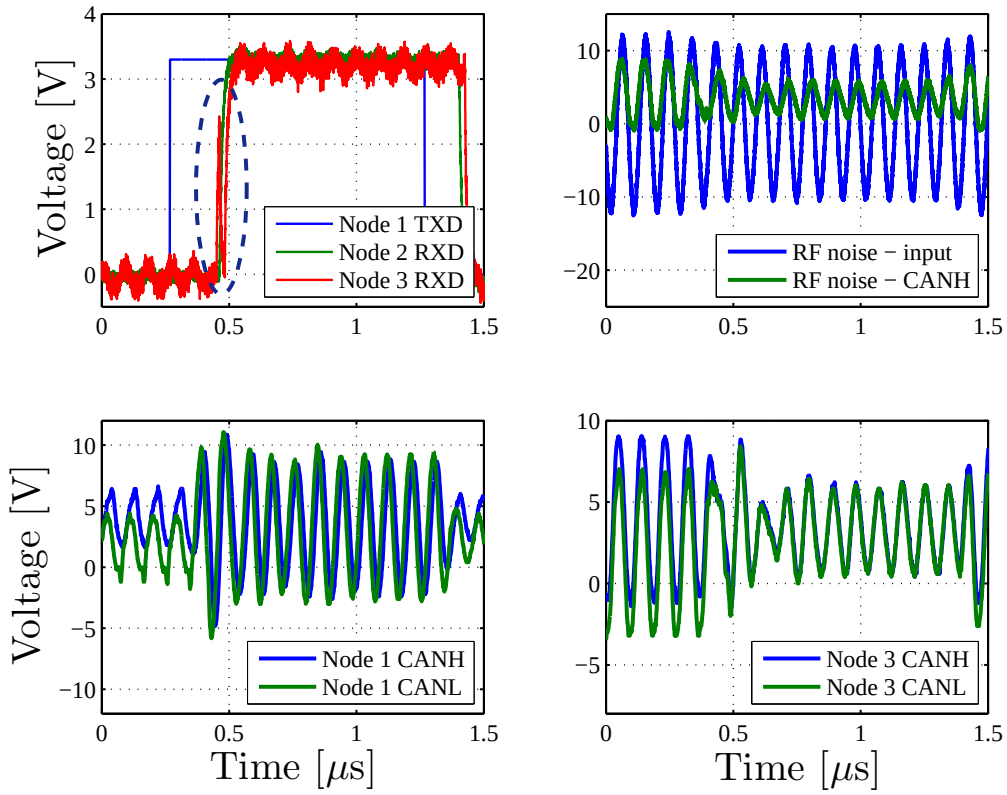

Figure 5.2. 3 nodes CAN network: Glitch on RXD Node 3 on 11 MHz 29.8 dBm RF noise

digital output of each CAN node; for each frequency, noise power level is increased until a glitch or jitter equal to 10% of T_{bit} are detected.

A set of waveforms is shown in Fig. 5.2 to depict a glitch error (29.8 dBm noise at 11 MHz) on the 3-node CAN network. On top left graph, digital input (TXD node 1) and output (RXD node 2 and 3) are depicted, while on the other 3 graphs analog CAN waveforms (Node 1 on bottom left, Node 3 on bottom right) and RF noise injection point (top right) are shown.

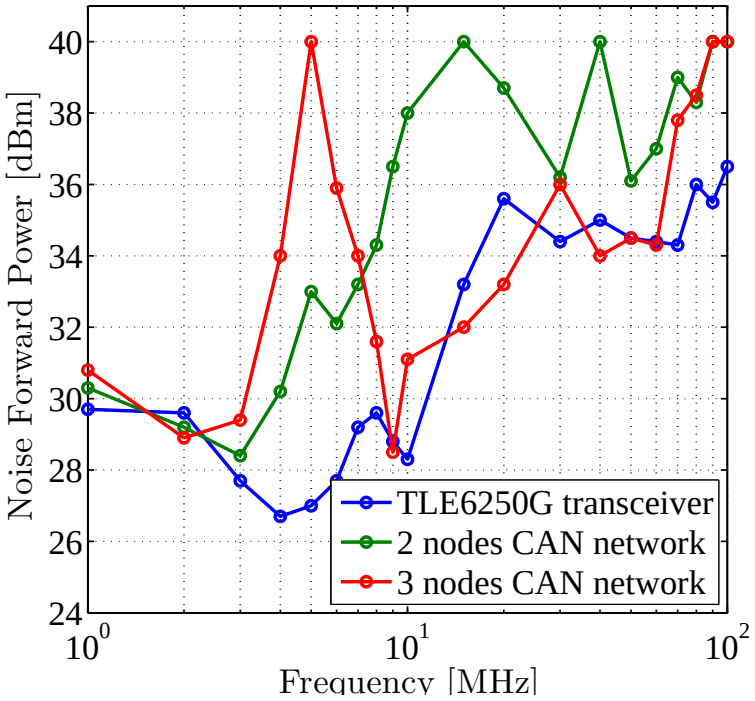

Figure 5.3. Immunity diagram of 2 and 3 nodes CAN networks compared to component level susceptibility curve

The DPI immunity diagram shown in Fig. 5.3 depicts the RF susceptibility curves of the two CAN networks, compared to the IC susceptibility on the PCB for component level testing; all circuits are based on the same CAN transceivers (TLE6250G). On each CAN circuit, RF noise immunity increases with frequency; this behavior can be explained by observing CANH and CANL port impedances on Fig. 4.6: lower impedance means that the noise coupling decreases at higher frequencies and port voltages values are lower (see Fig. 4.12). Moreover, the receiver comparator (Fig. 4.3) is a high impedance component and its output depends only on input voltages, disregarding small currents flowing through ports; it filters the input signal showing a low pass behavior as shown in section 4.1.4; this feature combination can explain the RF immunity curve trends. CAN networks are less susceptible to RF noise due to CAN wires; in this test case RF noise is injected far from the transceiver and voltage peak values are lessened (see Fig. 5.2 top right graph compared to bottom graphs) due to their propagation through the cables. The susceptibility curve of a communication network is clearly dependent on where the noise is injected; an open issue is

to estimate a worst case noise injection position.

5.1.1 Cable Characterization

In order to simulate a data transmission or a noise immunity test on a CAN network, a cable model in VHDL-AMS language is required to be connected with the CAN transceiver model developed in chapter 3.

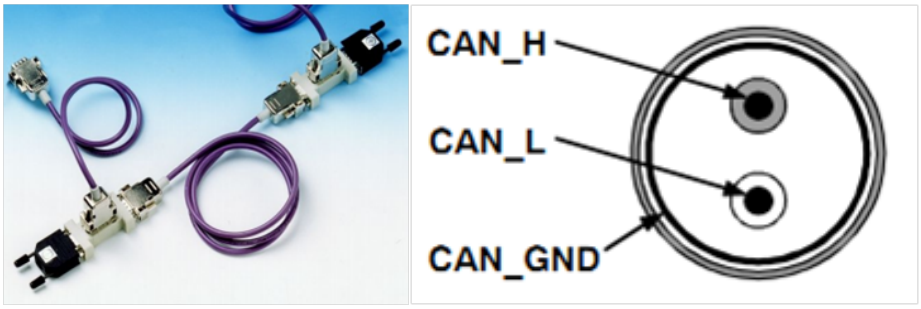

Figure 5.4. Left: CAN shielded twisted cable [59]. Right: wire inner structure

CAN cables [59] are shielded twisted wires, whose connector is a DSUB 9-pin termination, compliant to CAN standard [48]. CAN analog signals are transmitted along CANH and CANL twisted wires, while CAN_GND shield is used as ground reference; therefore a 3 conductor structure has to be characterized.

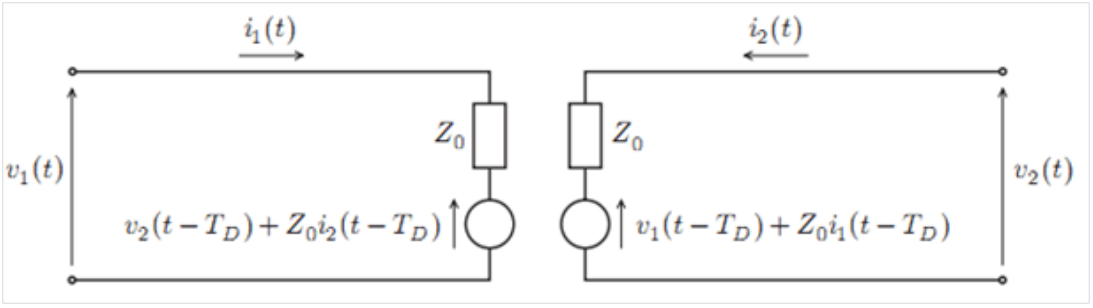

Figure 5.5. Lossless single transmission line Branin model [61]

The model is a realized by means of an equivalent circuit composed of three transmission lines [60]; each line is modeled as lossless Branin model [61], where voltages v and currents i are calculated using the following equations, with T_d defined as transmission delay and Z_0 characteristic impedance:

$$v_1(t) = Z_0 i_1(t) + v_2(t - T_d) + Z_0 i_2(t - T_d)$$
$$v_2(t) = Z_0 i_2(t) + v_1(t - T_d) + Z_0 i_1(t - T_d)$$

The three transmission lines have the same propagation speed v, physical length l and relative dielectric constant $\epsilon_r = 2.5$, but their characteristic impedance is different: the two transmission lines between CANH and CAN_GND and between CANL and CAN_GND show a common mode impedance $Z_0 = Z_c = 60\ \Omega$, while the line between CANH and CANL has a differential mode impedance $Z_0 = Z_d = 120\ \Omega$ [48].

The multi-transmission line model [61] does not include losses or any frequency-dependent phenomena, but it is accurate enough to simulate these small CAN networks, as it is shown in the next section. If any higher-order effects has to be included to simulate longer network, a more accurate cable model has to used.

5.1.2 Noise Immunity Simulation

The 2-node CAN network is simulated in Synopsys Saber environment connecting CAN transceiver and cable models developed in this thesis, together with lumped elements and digital I/O signal from Saber libraries, as shown in Fig. 5.6.

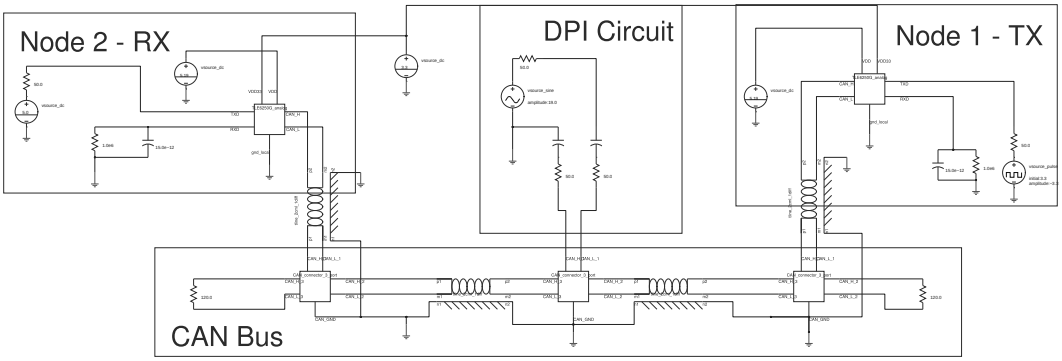

Figure 5.6. AMS model of DPI test for evaluation of CAN bus susceptibility to RF disturbances

Before simulating DPI test, a comparison between different measurements and simulation results is done to validate the proposed model. A transmission test is done on the 2-node network, removing the DPI circuit and the 120 Ω resistor on CAN bus end near Node 2 transceiver. In this way, the transmission line load between CANH and CANL is not matched to characteristic impedance Z_d and wave reflections are provoked on analog signals through the bus. As shown on Fig. 5.6, wave reflections affect CAN signal waveforms, so that digital output duty cycles are modified; it is relevant to remark that '1' bit periods are reduced from 1 μs (TXD node 1) to 0.938 μs (RXD node 2). These 'jitter' effects could affect synchronization between nodes and cause communication errors [48]. A good agreement is found between measurements and simulations on digital signals and analog waveforms, proving that transceiver and wire models are able to correctly estimate, in time domain, both IC internal delays and cable transmission line behaviors, such as reflection due to mismatched loads and propagation delays.

After validating the cable models, a DPI test on 2-node CAN network is simulated in Synopsys Saber schematic shown in Fig. 5.6. A 31.5 dBm 5 MHz noise is injected in the network from the

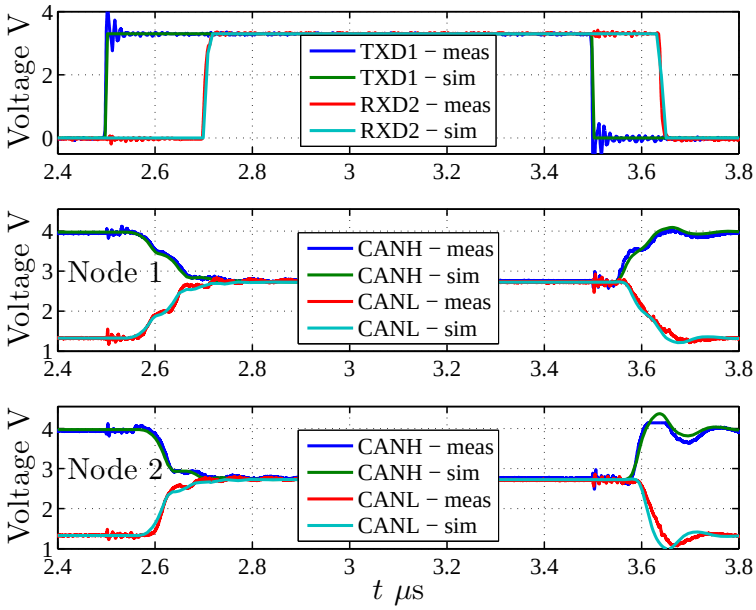

Figure 5.7. Transmission test waveforms on 2-node CAN network without noise injection and with unmatched cables

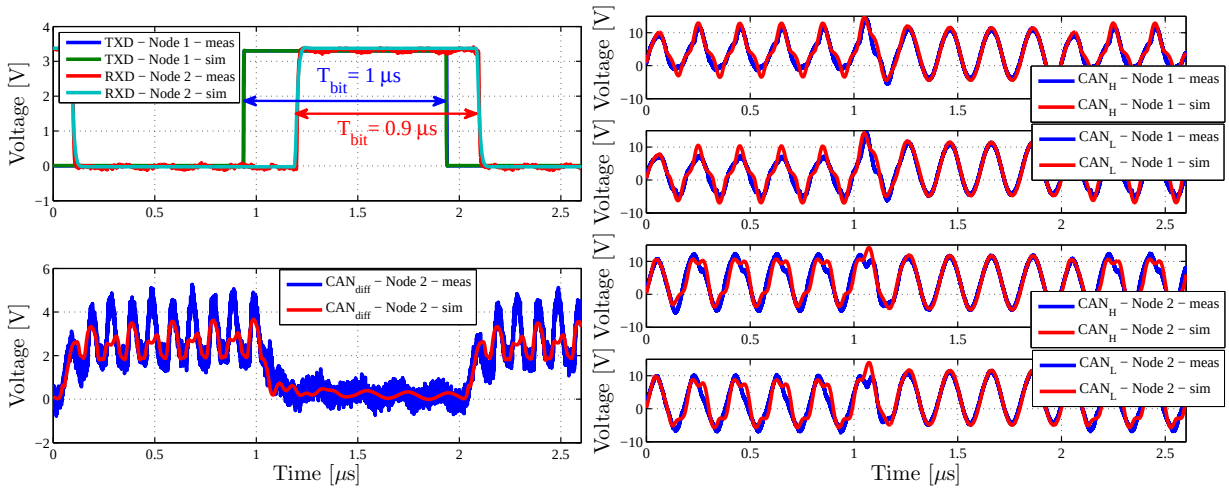

Figure 5.8. 31.5 dBm 5 MHz RF noise DPI test simulation on 2-node CAN network

RF signal generator through the DPI circuit; IEC susceptibility criterion [51] is fulfilled because a 10% jitter is detected on Node 2 RXD digital output signal. As shown in Fig. 5.8, CAN analog waveforms (bottom graphs) obtained from measurements and simulation are in good agreement and the susceptibility criterion is verified on digital signals (top left graphs), proving that the proposed models are able to perform a DPI test procedure in a simulation environment, as long

as the injected noise frequency is included in a bandwidth where models were validated. The simulation time required to obtain these waveforms is 9.8 s on a commercial laptop, proving a good computational efficiency.

At last, the complete model of the 2-node CAN network is used to carry out a DPI immunity test at equipment level. Time domain simulations are run according to the same procedure defined for testing noise susceptibility at component level (see Section 4.3); RF noise parameters (frequency, power and phase) are varied in three nested loops to cover all the possible combinations of network communication and noise injection. The lowest noise power value provoking a transmission failure on the Node 2 RXD signal is then recorded for each frequency as the minimum level required to fail the immunity test.

The results are then collected into the immunity graph shown in Fig. 5.9 and it shows good agreement between the data obtained by measurements and the simulation of the immunity test on the equipment. At 1 MHz both the real CAN network and the model returns 30 dBm as a maximal acceptable value of the RF noise power. For the frequency range from 2 MHz up to 15 MHz, this value increases for both setups, with the exception of 2 and 3 MHz frequencies where the maximum errors is 2 dB. For frequencies higher than 15 MHz, the network is able to withstand RF noise whose power is between 36 dBm (4 watts) and 40 dBm (10 Watts), a very high power level. To obtain the results of this test, the simulation time is about 14 hours on a common laptop.

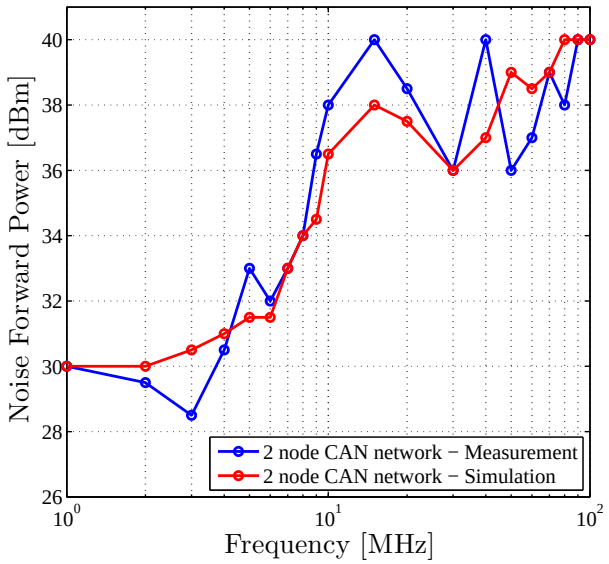

Figure 5.9. DPI immunity graph measurement and prediction on 2 nodes CAN network

5.2 CAN Bus BCI Test

A BCI test [19] is carried out on the 2-node CAN network to evaluate its immunity to injected RF currents, according to avionic standards [28]. As shown in Fig. 5.10, the two boards (Digilent and

Xilinx) and CAN cables used for the previous DPI test are placed on a copper plane, connected to CAN network ground. A F140 probe [62] is used to inject RF noise from the signal generator in CAN cables, due to its usable frequencies (1 MHz - 1 GHz) covering the test bandwidth.

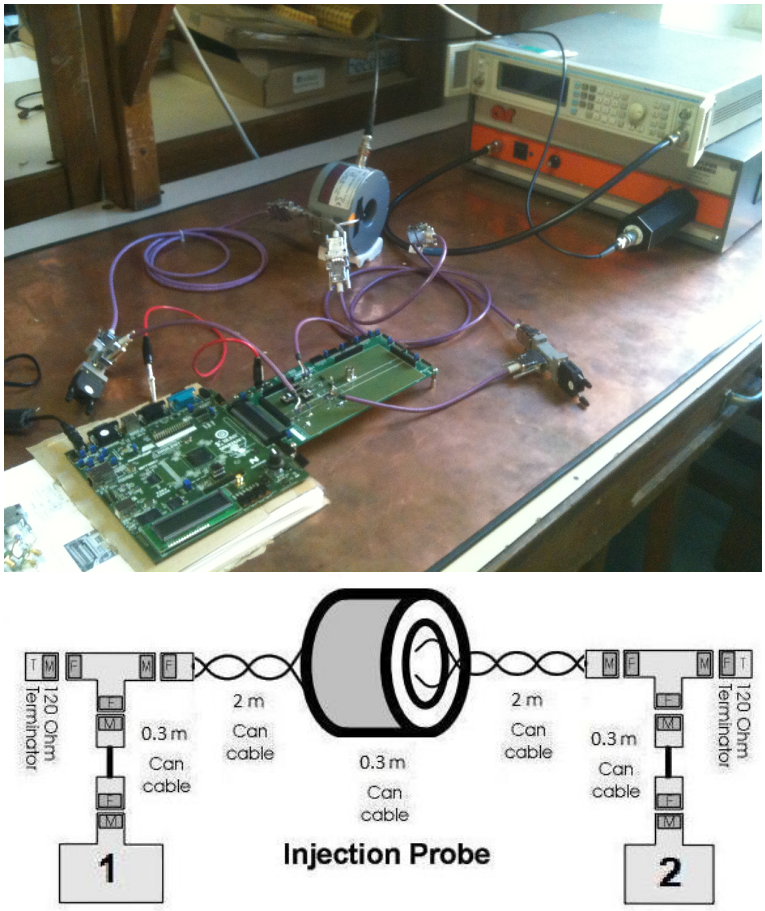

Figure 5.10. BCI measurement setup on 2-node CAN network and schematic

CAN network topology, depicted in Fig. 5.10, shows that the total cable length from node 1 to node 2 is 4.9 meters and the noise injection point is in the middle of CAN cable bus, as it has been done in the 2-node network shown in Fig. 5.1 used for DPI testing. Furthermore, the cable shield CAN_GND is divided near the probe from CANH and CANL wire; while CAN data wires go through the probe hole, CAN_GND passes outside the probe. Hence, RF noise is not injected into the shield, which is connected to ground and is used as reference conductor for the entire cable length.

This test setup choice is made because RF noise could not be injected in CAN_GND; the wire shield, acting as ground for the CAN wires, is connected to the ground of the whole system. If noise is injected also into CAN_GND, it would also affect the digital I/O signals, whose ground is in commond with CAN signals. Therefore any noise injection would affect directly the digital

signaling and the transceiver immunity could not be correctly evaluated.

It is relevant to remark that the described setup is different from the one depicted in [28]. The standard requires to put all the wires through the probe, including the shield, and to not connect the cable shield CAN_GND to the copper plane, in order to not connect it directly to the global ground reference. Thus the floating cable shield is connected to the global ground plane only through a capacitive coupling. However, the coupling value depends on the geometry of the measurement setup and it is very sensitive to small changes, therefore a more stable setup was preferred.

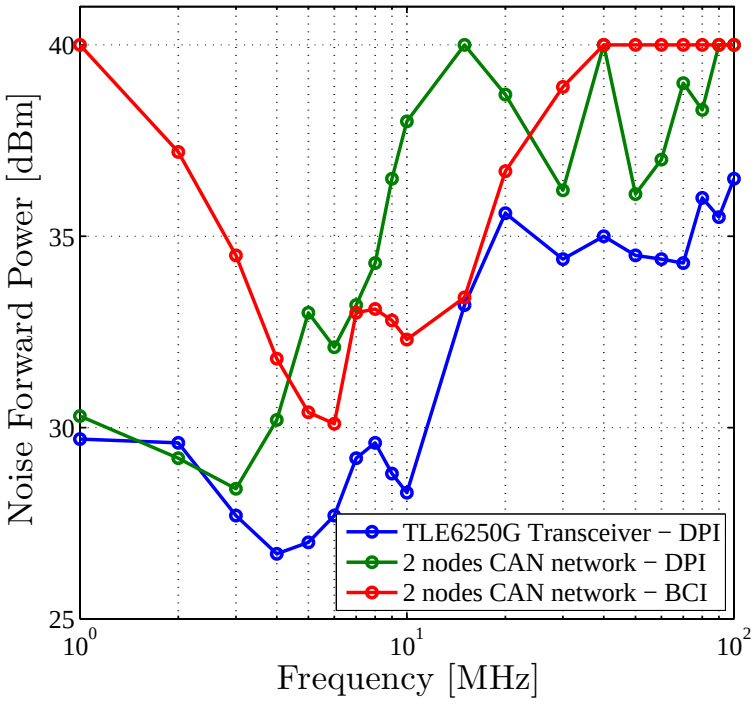

Figure 5.11. RF immunity graph comparing DPI and BCI test result on 2-node CAN circuits at component and system level

A BCI RF immunity test is carried out using the glitch-jitter susceptibility criterion [51]; the immunity curve depicted in Fig. 5.11 shows band-pass susceptibility, due to CAN transceivers being susceptible to BCI RF currents in a bandwidth between 3 and 20 MHz. This curve confirms the transceiver's susceptibility to noise frequencies up to 15-20 MHz. In this bandwidth the internal receiver can interpret noisy waveforms as meaningful CAN signals and it translate them to digital errors. This behaviour is explained noting that the CAN maximum bitrate is 1 Mbps, which is equivalent to a square wave signal with a 500 kHz frequency. The frequency spectrum of the signal is mainly located in the 1-10 MHz bandwidth and therefore the receiver is designed to filter frequencies higher than the expected ones, confirming the immunity at higher frequencies.

It is important to notice that, while the error provoked by DPI injected noise is almost always 'jitter', BCI RF currents cause mainly glitches on digital output, as shown in Fig. 5.12, where waveforms recorded during the BCI test are displayed when when injecting 10 MHz noise.

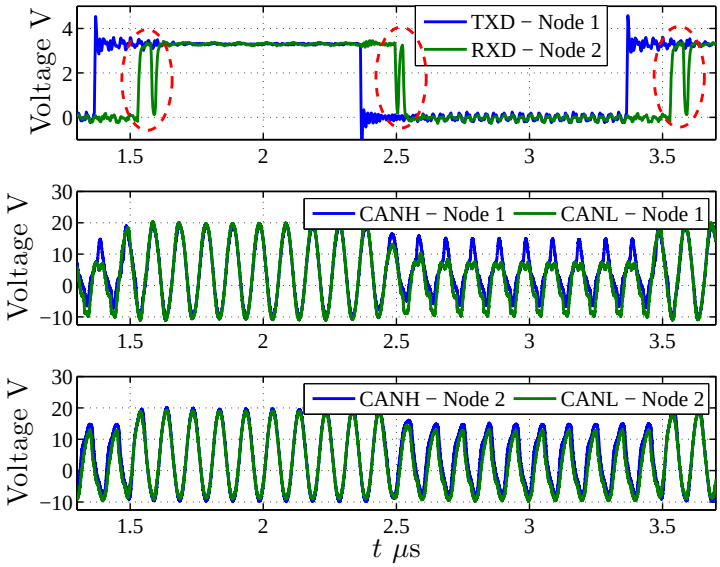

Figure 5.12. 32.4 dBm 10 MHz noise causing multiple glitches on Node 2 RXD

A possible explanation is given by different impedance values displayed by CANH and CANL transceivers ports and for non-simultaneus transition from recessive state and viceversa. For example, in Fig. 5.12 it can be noted that the glitches are located in time after a state transition; during this phase, the CAN port impedance is clearly not symmetric and common-mode noise rejection is limited, converting it into differential noise. The current injected during a BCI test amplifies the phenomena causing a glitch on RXD signals before internal IC filter-like behavior fix the digital output.

5.2.1 Injection Probe Modeling

A characterization of the probe through a VNA frequency-domain measurement is done to evaluate the RF noise injection in a 3-conductor CAN cable. The probe input is Port #1 (P1), on wire head CANH and CANL are Port #2 (P2) and #3 (P3) respectively, while on wire tail they are labeled #4 (P4) and #5 (P5). S-parameters are measured using as reference the cable shield CAN_GND, connected to the copper ground plane.

As depicted in Fig. 5.14, transmission parameters from BCI port to CANH or CANL are constant in a bandwidth between 1.5 and 30 MHz, equal to -7.4 dB. It is relevant to remark that RF noise attenuation through a DPI subcircuit is -8.6 dB in the same bandwidth. The phase contribution can be ignored, since the noise source works in an open loop configuration, and any delay from the generator to the injection node is irrelevant. In Fig. 5.14 the transmission parameters from CANH and CANL head to the corresponding tail wire are depicted, showing that cable extraction from shielding and probe clamping introduce 2-3 dB attenuation on signal.

In order to simulate a BCI susceptibility test, a time-domain behavioural model of the injec-

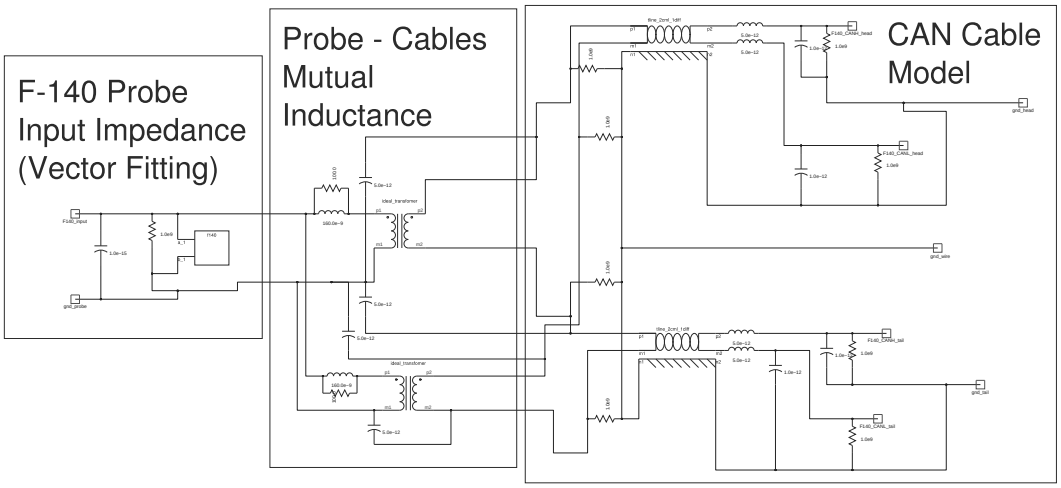

Figure 5.13. AMS model of F-140 BCI injection probe on CAN cables

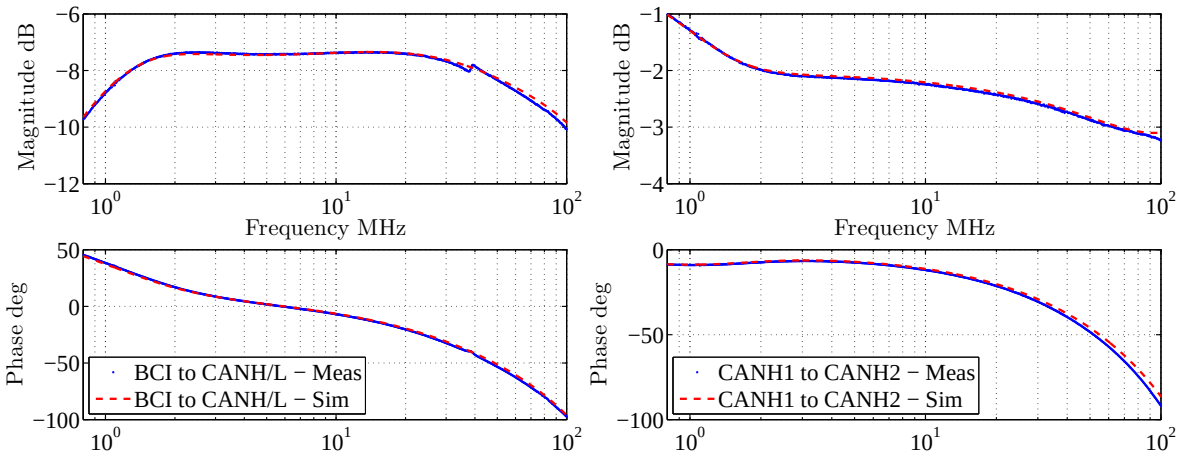

Figure 5.14. Measured and simulated S-parameters for the F-140 injection probe on CAN wires (left) and propagation through cables (right)

tion clamp is developed. Essentially, a ferrite-core injection probe behaves as an RF transformer, the secondary winding being the wire bundle onto which the probe is clamped. The frequency-dependent and lossy characteristics of the ferrite core of the probe, as well as additional capacitive/inductive effects related to the primary winding, to the clamped conductors, and to the input connector of the probe contribute significantly to the frequency response of the injection device.

The selected approach is similar to [63] and [64], measuring with a VNA the input impedance of the injection clamp in absence of the secondary winding. To overcome the modeling problem of the frequency-dependent features, the impedance of the probe ferrite core is modeled by processing the measured impedance through Idem [65]; the tool produces an equivalent netlist from a

frequency domain response by applying the vector fitting algorithm [66], which fits the curve with rational function approximations with the required poles and zeros. The generated netlist can be used in a time-domain simulation while duplicating the behavior of the measured S-parameters.

The mutual inductive coupling between probes and cables is represented as an ideal transformer with a lossy inductor on a winding. The transformer ratio is equal to the number of windings in the ferrite core, while the inductance value is estimated with the 5 port VNA measurement previously detailed. Two capacitances were added into the circuit to represent the additional capacitance of the 30 cm wire to the injection clamp package. The final circuit representation of the BCI clamp with coupling to the CAN cables is shown in Fig. 5.13 and the simulated S-parameters show good agreement up to 100 MHz with 5 port characterization depicted in Fig. 5.14.

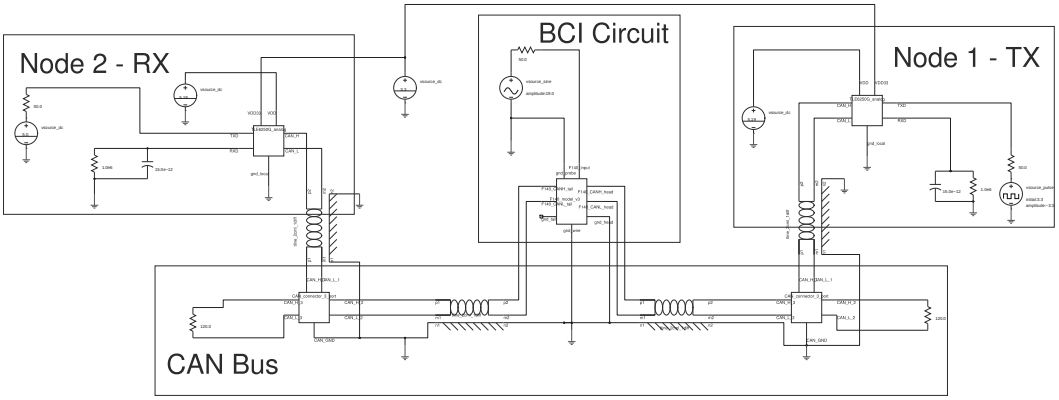

Figure 5.15. AMS model of BCI test on CAN network

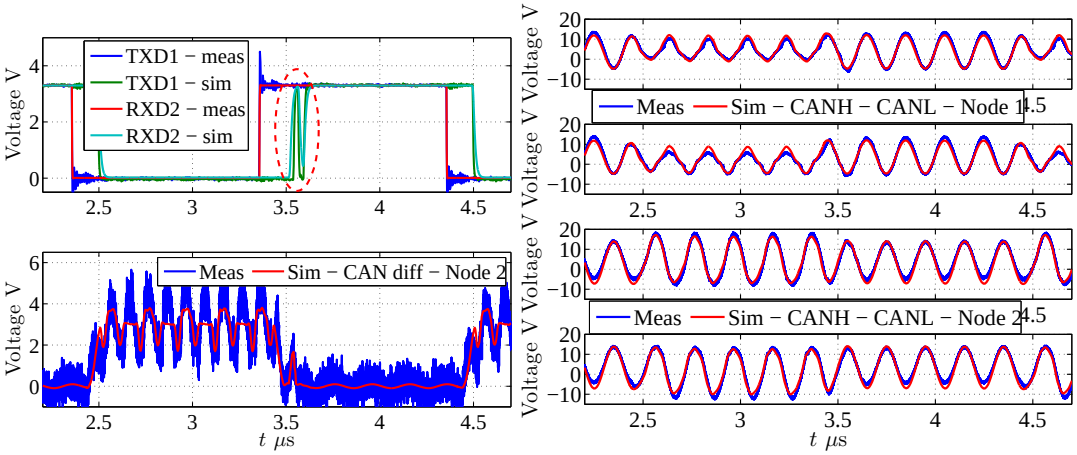

Figure 5.16. 30.3 dBm 5 MHz RF noise BCI test simulation on 2-node CAN network

The validity of the probe model is evaluated by simulating the complete BCI test on the 2

nodes CAN network. The models developed in the thesis are assembled to create the simulation test bench shown in Fig. 5.15. A 30.3 dBm 5 MHz noise is injected in the network with the F140 probe, causing a glitch on the received RXD signal. The simulated waveforms are depicted in Fig. 5.16, proving that the common-to-differential noise conversion is modeled with good accuracy in this setup. The simulation requires 29.7 s on a commercial laptop.

5.3 Chapter Summary

This chapter tackled the open problem of the noise immunity testing at system level, highlighting the relationship between the susceptibility of integrated circuits and electronic equipments in communication networks. A characterization of different test setups has been carried out to understand the feasibility of testing noise immunity in a simulation environment, in order to evaluate the available noise margins and to determine criticality levels. The modeling strategy is based on the combination of ICs and wire models, whose susceptibility is investigated in time-domain according to standardized test methods.

Chapter 6

Conclusions

The activity done for this thesis concerns the IC immunity to electromagnetic interference. The ICs are of paramount importance for the assessment at system level of EMC effects in high-performance electronic equipment.

More concretely, the noise effects on mixed-signal ICs in communication networks has been evaluated. An immunity analysis was carried out at component level superimposing RF or transient disturbances on a functional signal; the main effects induced by noise are timing jitter and glitches on digital I/O signals. As a test case, a CAN transceiver immunity was characterized according to IEC standards, analyzing the internal link between noisy signals on CAN ports and digital outputs. The main sources of errors are the non-idealities of differential communication, as they hamper ideal common mode noise rejection converting part of the interference into differential noise. These features were identified in port impedance asymmetry, ESD protection diodes and non-synchronous switching, and they have to be included in the immunity model. The strongly non-linear IC behaviour, along with the definition of immunity criteria on digital signals, has led to verify the immunity behaviour in time-domain simulations.

A novel procedure is proposed for the IC modeling for mixed-signal immunity simulations of communication networks. The procedure is based on the use of schematic blocks, whose parameters are estimated from time and frequency domain measurements, allowing accurate and efficient reproduction of port circuits and IC internal links. The obtained models may handle RF noise up to 200 MHz injected and can adequately reproduce its effects on both analog and digital signals for SI and EMC investigations. A representative test case of a CAN transceiver was selected, for which the model construction parameters have been calculated and optimal settings have been selected ensuring high precision and efficiency. The model was integrated into an AMS circuit simulator and its immunity behavior was correctly predicted at component level, confirming the effectiveness of the modeling process.

Furthermore, the noise immunity simulations were done at system level. In order to accurately predict the results of susceptibility test, all the components need to be modeled and taken into account. A characterization of multiple test setup has been done, highlighting the differences between DPI and BCI tests on communication networks. The susceptibility of a CAN network is investigated in time-domain according to standardized test methods. A modeling strategy, based on the combination of ICs, wire and injection probe models, was developed to assess the noise

immunity at equipment level. The results of the proposed framework are promising, as it has been possibile to predict boh the functional signals and the noise effects on analog and digital signals.

Although this research has answered to a certain number of needs for the development of IC models and modeling techniques, several issues still require further work. Firstly, the simulation framework currently uses models validated for frequencies up to 200 MHz. The industrial need of scalable and efficient high-frequency IC models requires further studies. Additional analyses have to be carried out regarding the impact of transient noise on ICs; this work has been focused on EFTs effects on CAN communication and it has to be extended to all different types of transient interferences. Also, the modeling procedure has been applied mainly to small CAN networks; it should be validated on bigger networks or more complex communication systems. Furthermore, the methodology is based on measurements: an automated procedure to generate models from reference transistor-level circuits is required to simplify immunity analysis in a simulation environment.

List of Acronyms

A/D	Analog/Digital
AMS	Analog Mixed-Signal
ANN	Artificial Neural Networks
BCI	Bulk Current Injection
CAN	Controller Area Network
CDM	Charged Device Model
CW	Continuous Wave
DPI	Direct Power Injection
DUT	Device Under Test
EDA	Electronic Design Automation
EFT	Electrical Fast Transient
EM	Electromagnetic
EMC	Electromagnetic Compatibility
EMI	Electromagnetic Interference
EOS	Electrical Overstress
ESD	Electrostatic Discharge
FPGA	Field Programmable Gate Array
HB	Harmonic Balance
HBM	Human Body Model
IBIS	Input/output Buffer Information Specification
IA	Internal Activity
IB	Immunity Behaviour
IC	Integrated Circuit
ICEM	Integrated Circuit Emission Model
ICIM	Integrated Circuit Immunity Model
IEC	International Electrotechnical Commission
I/O	Input/Output
IP	Intellectual Property

ISO	International Organization for Standardization
ITRS	International Technology for Semiconductor
LECCS	Linear Equivalent Circuit and Current Source
LVDS	Low Voltage Differential Signaling
MTL	Multiconductor Transmission line
PCB	Printed Circuit Board
PDN	Passive Distribution Network
RFI	Radio-Frequency Interference
RTCA	Radio Technical Commission for Aeronautics
SI	Signal Integrity
SMA	SubMiniature version A
TDR	Time Domain Reflectometry
TLP	Transmission Line Pulsing
VHDL	VHSIC Hardware Description Language
VNA	Vector Network Analyzer
WBFC	Work Bench Faraday Cage

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