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K-band GaAs MMIC Doherty power amplifier for microwave radio with optimized driver

Roberto Quaglia, *Member, IEEE*, Vittorio Camarchia, *Senior Member, IEEE,* Tao Jiang, Marco Pirola, *Member, IEEE,* Simona Donati Guerrieri, *Member, IEEE,* and Brian Loran

***Abstract*—In this paper, a Doherty power amplifier for K-band point-to-point microwave radio, developed in TriQuint GaAs 0.15 μm PWR pHEMT monolithic technology, is presented. Highly efficient driver stages on both the main and auxiliary branches have been designed and optimized to boost gain with minimal impact on power added efficiency. The selected architecture enables a modular combination to reach higher power levels. Matching network structures have been designed, according to simple equivalent circuit approaches, to obtain the desired 10% fractional bandwidth. The fabricated power amplifier exhibits, at 24 GHz in continuous wave conditions, an output power of 30.9 dBm, with a power added efficiency of 38% at saturation and 20% at 6 dB of output power back-off, together with a gain of 12.5 dB. System level characterization at 24 GHz, in very demanding conditions, with 28 MHz channel, 7.5 dB peak-to-average ratio modulated signal, showed full compliance with the standard emission mask, adopting a simple predistorter, with average output power of 23.5 dBm, and average efficiency above 14%. The measured performance favorably compare with other academic and commercial K-band power amplifiers for similar applications.**

***Index Terms*—Gallium arsenide, MMICs, Doherty power amplifiers, point-to-point radio.**

I. Introduction

MICROWAVE point-to-point radio represents a convenient solution for the deployment of mobile network backhauls when compared to wired solutions in terms of installation and maintenance costs. The adopted frequency bands span nowadays the entire microwave frequency spectrum, from 7 to 42 GHz [1]. Focusing on the power amplifier (PA), the growing request for high peak-to-average modulated signals asks for advanced solutions to enhance the average Power Added Efficiency (PAE). In fact, increasing PAE gives great advantages not only in terms of power consumption, but also concerning the simplification of the cooling setup, implying cost and weight reduction.

High efficiency PA schemes like the Doherty Power Amplifier (DPA) have been demonstrated at lower frequencies, also exploiting the promising GaN technology e.g., [2]–[4], but the trend is towards increasing the working frequency, for capacity improvement and apparatus size reduction. In this framework, particular interest is given to K-band, also adopted for satellite communications and radars. At these frequencies, the demonstrated power amplifiers are mainly limited to class AB parallel stages, developed in GaAs MMIC technology.

The aim of this work is to explore the Doherty scheme as an alternative to conventional class AB PAs for K-band (20.8 to 24 GHz) microwave backhaul. In fact, a GaAs MMIC DPA has been designed in TriQuint Semiconductor's 0.15 μm PWR pHEMT MMIC process. The guidelines for the device selection and the design strategies have been presented in [5], together with preliminary simulation results. This paper, in addition to the content of [5], contains several new results: a detailed description of the design procedure, the Continuous Wave (CW) experimental characterization of the realized MMIC, and a system level characterization in K-band, that represent a significant added value and relevant scientific content.

The MMIC of this work represents one of the first examples of GaAs K-band DPAs. In fact, the work of [6] presented a DPA developed in Ku-band on GaAs MMICBlue. However, it was designed for an output power of 25 dBm, i.e., 6 dB less than in this work, and showed a limited gain of 8 dB. This paper presents a novel contribution: thanks to the careful design of the architecture, driver stages and matching networks, the fabricated GaAs DPA can be considered a promising solution for point-to-point applications in terms of gain, power and PAE levels.

The paper is organized as follows: Section II presents the design strategy, Section III shows the most important simulation results, while in Section IV the CW and system level experimental characterization results are shown. Finally, in Section V some conclusions are drawn.

II. Design

Considering the high directivity of the adopted antennas, microwave backhaul radio links require power levels on the order of a few watts to guarantee the needed coverage distance range. In the present work we present a DPA with a single power device for main and auxiliary stages, targeting an output power of 31 dBm in the 21.2-23.6 GHz band. The design has been developed utilizing for the power stage 12×85 μm power devices. This device, for which an accurate foundry nonlinear model is available, delivers an output power of around 29 dBm. With respect to more complex DPAs adopting combined (larger periphery) main and auxiliary units, this choice

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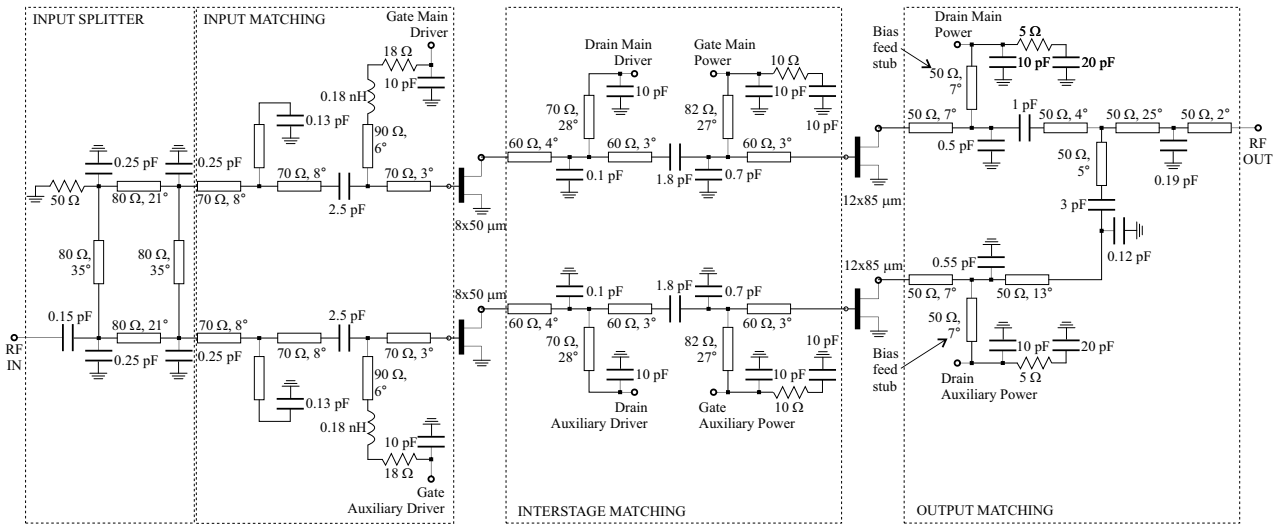

Fig. 1. Complete scheme of the DPA. Equivalent ideal lines are represented: electrical length refers to 22.4 GHz.

allows the designing, testing, and optimization of a single-cell building-block DPA with more favorable impedance levels. Once the single-cell DPA performance is assessed, higher power levels can be reached combining these single-cells using 50 Ω combiners/splitters. The complete scheme of the amplifier is reported in Fig. 1, where all the component values are indicated: the reported dimensions refer to the final layout, refined with electro-magnetic simulations. In the following, the most critical aspects of the design will be addressed highlighting the strategy adopted in the present work.

A. Doherty gain enhancement

The achievement of higher gain is a crucial aspect in PAs, also considering its impact on the resulting PAE. Since, with respect to analogous combined PAs [2], DPAs suffer of gain degradation, we investigated two driving architectures, see Fig. 2, in terms of performance and complexity.

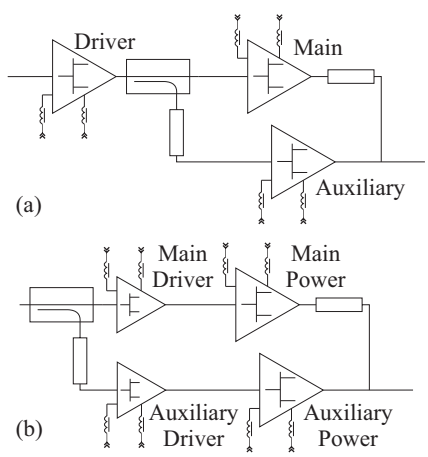

Fig. 2. Comparison between driver strategies for DPA.

Strategy (a) employs a single driver before the DPA, instead (b) adopts a driver for both main and auxiliary branches. While both schemes exhibit similar behavior in terms of gain improvement, the situation is rather different concerning the overall PAE. To compare the two schemes, we started considering an ideal DPA without driver, adopting $12{\times}85\,\mu$m devices for main and auxiliary. According to single tone simulations, this DPA exhibits a gain G_{DPA} of 6 dB, with an efficiency η_{DPA} of 41% and a PAE of 31% at 6 dB back-off. The PAE in the two cases is evaluated as $\mathrm{PAE}_{\mathrm{a,b}} = \eta_{\mathrm{a,b}}\left(1 - \frac{1}{G_{\mathrm{a,b}}}\right)$, where $\eta_{\mathrm{a,b}}$ and $G_{\mathrm{a,b}}$ are the overall efficiency and gain, respectively. These results allow us to evaluate the overall PAE of the scheme of solution (a): in fact, the overall gain G_{a} is the product between driver's gain and G_{DPA}, while the total efficiency can be approximated as:

$$\eta_{\mathrm{a}} = \left(\frac{1}{\eta_{\mathrm{DPA}}} + \frac{1}{G_{\mathrm{DPA}}\eta_{\mathrm{D}}}\right)^{-1}, \qquad (1)$$

where η_{D} is the driver's efficiency: the driver is assumed as an ideal amplifier, since we are interested in a comparative analysis. The resulting overall PAE is plotted vs. drivers' efficiency in Fig. 3 (dashed lines), for different drivers' gain values.

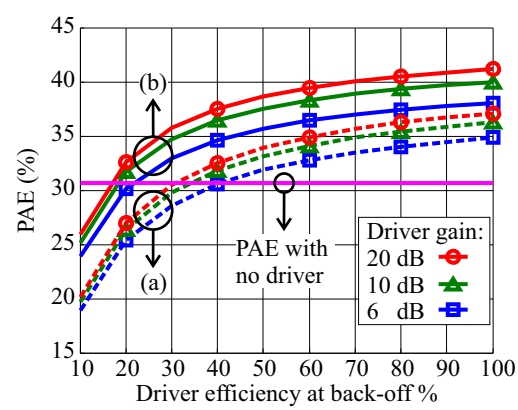

Fig. 3. Total PAE of DPA with driver vs. driver efficiency, for different driver gains. Strategy (a): dashed lines. Strategy (b): solid lines. Ideal DPA PAE without driver: solid horizontal line.

The assessment of the 6 dB OBO PAE for the scheme of

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Fig. 2(b) requires some assumptions and additional data. In particular, the overall PAE is the PAE of the main branch only, i.e., the cascade of the driver + the $12\times85\,\mu$m device on load condition before DPA break point, multiplied by a factor $\beta < 1$ that accounts for power lost due to auxiliary stage non-ideal behaviour. Single tone simulations have been performed on the $12\times85\,\mu$m device loaded with double real impedance load with respect to the optimum one, i.e., the load ideally seen by the main device before auxiliary turning-on. At an output power 6 dB lower than the DPA maximum output power, the HEMT shows a gain $G_{\rm H}$ of 8.7 dB and an efficiency $\eta_{\rm H}$ of 52%. Then, the overall gain $G_{\rm b}$ has been evaluated as the product of the driver's gain and G_H, and accounting for the splitting factor of the input divider, set at 2.7 dB for coherence with the other scheme. The overall efficiency can be approximated as:

$$\eta_{\rm b} = \beta\left(\frac{1}{\eta_{\rm H}} + \frac{1}{G_{\rm H}\eta_{\rm D}}\right)^{-1}. \qquad (2)$$

With $\beta = 0.85$, a value obtained from preliminary simulations on this structure, the overall PAE is plotted in Fig. 3 (solid lines).

Observing Fig. 3, it can be noticed that solution (b), always offers higher PAE than (a). Moreover, a higher PAE than DPA without driver (horizontal line in the figure) is obtained for lower driver efficiencies. For example, to provide PAE enhancements using a 6 dB gain driver, scheme (b) just needs a 20% efficiency (see blue solid line in Fig. 3), while, in scheme (a), a 40% efficiency is required.

Solution (b) has hence been adopted, also considering its advantages in terms of output power and linearity. In fact, the auxiliary power device is biased in class B/AB since the auxiliary driver, biased in class C, is responsible for correctly turning-on the auxiliary branch [4]. On the other hand, solution (b) requires a more complex layout, and an increased number of different bias voltages. Concerning the driver amplifiers, a $8\times50\,\mu$m device has been chosen since it is able to deliver, before its compression, the input power needed to fully drive the main and auxiliary $12\times85\,\mu$m power devices.

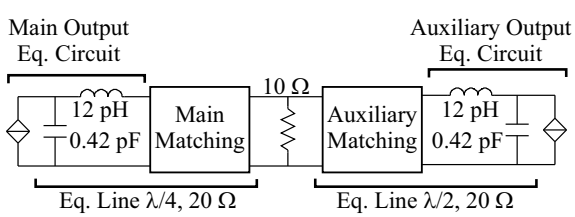

Fig. 4. Output equivalent reactive network of the $12\times85\,\mu$m device and DPA output matching strategy.

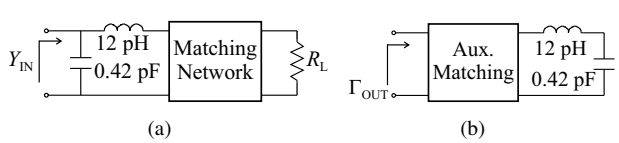

Fig. 5. Simulation setup for the design of output matching networks.

B. Matching strategy

The intrinsic drain optimum load of the power device, extracted from simulated load-pull on the non-linear model, resulted in $R_{\rm opt} = 20\,\Omega$, the value hence adopted for the characteristic impedance of the Doherty impedance inverter Z_0. The common load $Z_{\rm L} = 10\,\Omega$ requires a final output matching to reach the external $50\,\Omega$. To design the main and auxiliary output matching networks, the device has been approximated in the operative frequency band adopting the equivalent circuit shown in Fig. 4, that is a representation of the optimum load reactance obtained from load pull analysis. The approach has been to absorb the device output elements

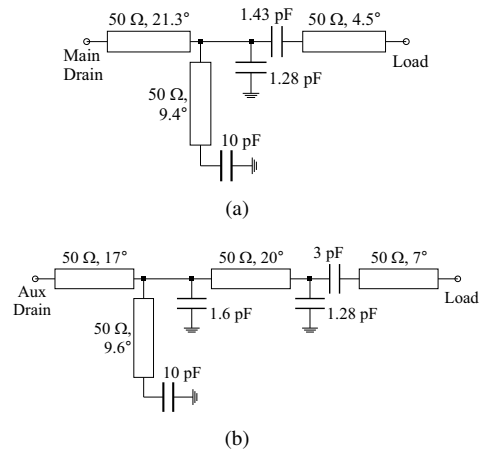

Fig. 6. Circuit diagram of output matching networks: main (a), auxiliary (b).

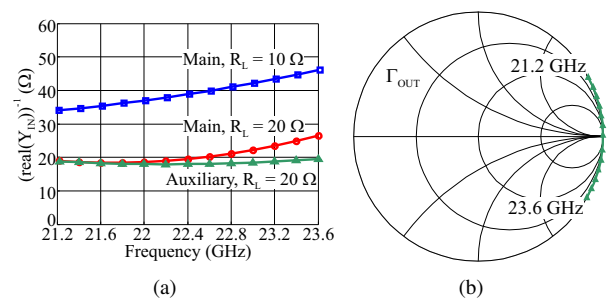

Fig. 7. Simulated $Y_{\rm IN}$ vs. frequency for the main and auxiliary cases (a). Simulated $\Gamma_{\rm OUT}$ for the auxiliary in "off" condition.

into an equivalent impedance inverter for the main (i.e., a $\lambda/4$, $20\,\Omega$ equivalent line), and into a $\lambda/2$, $20\,\Omega$ equivalent line for the auxiliary, see Fig. 4. The simulation setup of Fig. 5(a) has been used for the design of the main output matching, setting $R_{\rm L}$ at 10 and $20\,\Omega$ and evaluating $Y_{\rm IN}$, to account for the Doherty load modulation. For the auxiliary case, the setup of Fig. 5(a) has been adopted for simulating the saturated power condition, with $R_{\rm L}$ at $20\,\Omega$, while the scheme of Fig. 5(b) has been employed to set $\Gamma_{\rm OUT}$ close to open circuit when the auxiliary is off. The resulting main and auxiliary matching network are shown in Fig. 6(a) and Fig. 6(b) respectively.

The simulated $Y_{\rm IN}$ is reported in Fig.7(a). It can be noticed that, for the main, the load variation vs. frequency ranges between 18 and $26\,\Omega$ at saturation and between 34 and $46\,\Omega$ at back-off, while for the auxiliary it remains almost constant

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around 20 Ω in the whole frequency range (Fig.7(a)). The ratio between saturated and back-off main load is almost constant, guaranteeing good load modulation. Finally, in Fig. 7(b) the Γ_{OUT} of the auxiliary in "off" state is shown. The obtained impedance transformations have been considered reasonable in the design frequency range.

In both solutions, no harmonic control has been explicitly enforced, to avoid resonant effects, even if the second harmonic termination has been monitored to avoid detrimental effects on the efficiency.

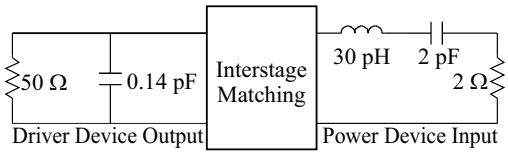

Fig. 8. Equivalent circuits adopted for interstage matching design.

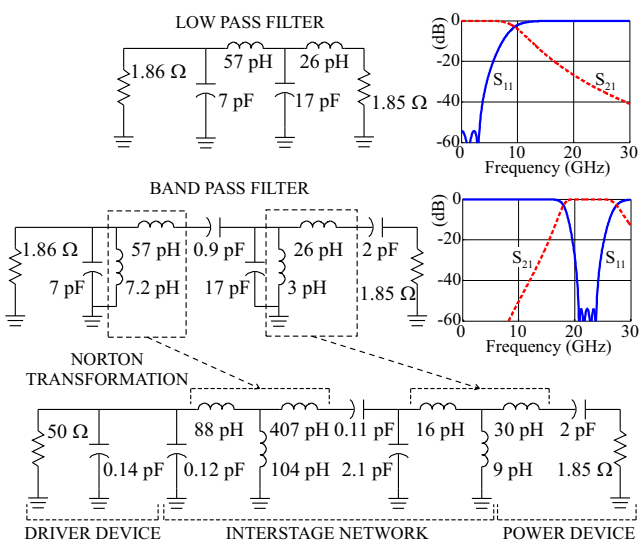

Fig. 9. Interstage matching design procedure.

The interstage matching networks have been designed adopting a simplified procedure. The input of the power device and the output of the driver device have been approximated, in the band of interest, by linear equivalent circuits extracted from simulated load-pull, as reported in Fig. 8.

Main and auxiliary devices operate in different conditions, and therefore optimum narrowband performance could be achieved using different equivalent device representation. However, given the large bandwidth considered, and the significant process variation impact at the design frequency, the same equivalent circuit has been adopted for the two branches. This allowed to preserve symmetry, and to improve the robustness to phase deviations between the two stages. As a consequence, the sources of phase misalignment should be limited to the output combiner and the branch-line splitter. The matching strategy has been based on the procedure described in [7], in particular for a 4th order filter, (see Fig. 9). At first, a low-pass to band-pass transformation has been adopted yielding a Chebychev filter. Finally, through two Norton impedance transformations, the desired impedance matching, maintaining the same filter response and bandwidth, has been derived. In our case, the low-pass equivalent structure topology has been preferred in order to absorb the devices' equivalent elements within the filter. The lumped elements present in the interstage matching network have been substituted by integrated capacitors and transmission lines.

The input section of the amplifier includes a pre-matching network of the driver devices' input to 50 Ω, and a semi-lumped branch-line divider realized through capacitive-loaded transmission lines.

III. Simulations

Broadband loop stability has been analyzed adopting linear models at suitable bias points, accounting for the device self-biasing in nonlinear operation. Crucial device parameters have been swept to evaluate the effect of process deviations and model inaccuracies. Pad/bond-wires/external bias-tee models have been added to simulate low-frequency behaviour. The power stages evidenced two critical frequency bands around 7-8 GHz and 0.8-1 GHz. This issue has been solved, on one side, by the insertion of shunt resistors (with a series DC-block) in parallel to the DC-bypass capacitors at drain and gate, and on the other hand by a proper dimensioning of the drain feed stub lengths (highlighted in Fig. 1) of the power stage. The modification of the stub lengths had a small influence on the matching conditions, however the necessary correction could be achieved by tuning the other output combiner elements. For the driver stages, reasonable stability margins have been obtained by introducing a series resistor in the gate path before the by-pass capacitor. Regarding robustness to process variations, Monte Carlo simulations of the building blocks and of the DPA have been carried out. Some structures revealed the need of a trade-off between sensitivity and loop stability margins. Since the main goal of the design is to prove the potentialities of GaAs DPAs in K-band and of the employed solution for gain enhancement, we decided to accept a higher sensitivity to process variations, hence assuring good stability margins. In particular, the drain feed stubs have a big influence on the loop gain trajectory, and the proper selection of their lengths permitted to guarantee large phase margins. On the other hand, this choice brings along a detrimental effect on the design sensitivity. A more accurate analysis regarding robustness and bandwidth improvements could be carried out in the engineering phase of the product. However, to minimize other causes of dispersion, symmetries have been ensured wherever possible, for example adopting identical input and interstage matching structures for the main and auxiliary stages. Electro-Magnetic (EM) simulations have been extensively employed, in particular for the design of the output combiner, where the coupling at the junction of the main and auxiliary branches has to be carefully assessed. In fact, as it can be noticed comparing the circuit diagrams of Fig. 1 and of Fig. 6, the final dimensions of lines and capacitors have been significantly re-tuned in the full schematic. Notice also that all the results presented in this section have been obtained with EM-simulated passive blocks.

The scattering parameters have been evaluated for different bias points, see Table I for a bias reference map. The drain

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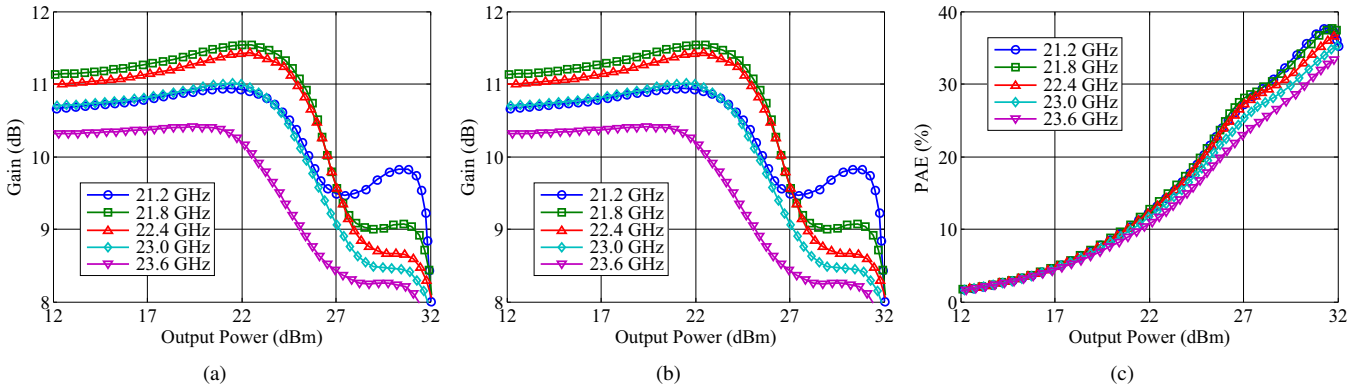

Fig. 10. DPA simulation results. (a): scattering parameters in the 18-26 GHz range, at different bias points (see Table I). (b) and (c): gain and PAE vs. output power at BIAS#1 in the 21.2-23.6 GHz band.

Stage	BIAS #1	BIAS #2	BIAS #3
Main Power	AB, I_D=102 mA	AB, I_D=102 mA	AB, I_D=40 mA
Main Driver	AB, I_D=40 mA	AB, I_D=40 mA	AB, I_D=10 mA
Aux. Power	AB, I_D=20 mA	B, V_G=-1 V	B, V_G=-1 V
Aux. Driver	C, V_G=-1.5 V	C, V_G=-1.5 V	C, V_G=-1.5 V

TABLE I
BIAS REFERENCE FOR MULTI-BIAS RESULTS: CONDUCTION CLASS AND BIAS POINTS.

voltage of all stages is set to 6 V. The gate voltage of the main power and driver device is identical, while the auxiliary power and driver devices are biased independently.

The scattering parameters results are shown in Fig. 10. Gain shows a reasonably flat behaviour in the 20-24 GHz range for the BIAS#1 case, thanks to the introduced mismatch at low frequencies to compensate for intrinsic device gain vs. frequency decrease. Single tone simulations, carried out at BIAS#1, indicated an expected saturated output power higher than 31 dBm in the design band. Gain and PAE, see Fig. 10(b) and Fig. 10(c) respectively, had a uniform behaviour in the band, with the latter exceeding 33% at saturation and 20% at 6 dB back-off.

IV. CHARACTERIZATION

A. CW results

The mask area occupied by the DPA is $3 \times 1.43\,\mathrm{mm}^2$. The fabricated MMIC is shown in Fig. 13. The amplifier has been characterized in small and large signal CW conditions by using the real-time large signal power measurement bench of the Politecnico di Torino [8].

Fig. 11(a) shows the scattering parameters of the DPA for different bias conditions. The measured small signal scattering parameters highlighted a gain S_{21} higher than 9 dB in the 22–26 GHz band (gain peak at 24 GHz). The DPA exhibited a center-frequency shift with respect to the designed band that can be ascribed to the high sensitivity to process variations of some elements of the matching networks. This has also been verified by characterizing some passive test structures included in the tape-out, that evidenced a frequency shift compatible with the one experienced by the DPA. Moreover, on wafer scattering measurements on bare devices confirmed the validity of the model, at least in small signal condition.

The measured gain and PAE as a function of the output power are shown in Fig. 11(b) and Fig. 11(c), respectively, at BIAS#1. The operating band resulted in the 22.8-25.2 GHz range (10% of fractional bandwidth), see Fig. 12(a). The PAE results higher than 25% (saturated) and 15 % (at 6 dB OBO from saturation), and the gain higher than 11 dB with ripple lower than 1.5 dB in the entire band. At the measurement center frequency of 24 GHz, the measured gain and PAE for different bias points are shown in Fig. 12(b) and Fig. 12(c), respectively. It can be seen that a reasonable compromise between gain flatness and PAE performance can be achieved by proper bias adjustment.

Tab. II reports a comparison between the DPA of this work and other PA examples in K-bands, both from commercial and academic contributors. CHA5350 is a 17-24 GHz Medium Power Amplifier from United Monolithic Semiconductors, HMC756 is a 16-24 GHz 1 Watt PA from Hittite Microwave Corporation, and TGA4535 is a K-Band Power Amplifier from TriQuint Semiconductor. The designed DPA favorably compares in terms of back-off efficiency (6 dB output back-off from saturated power) with the other combined PAs.

Ref.	Freq. (GHz)	P_{SAT} (dBm)	PAE (%)	PAE_6 (%)	G (dB)	St.
[6], DPA	17	25	37	25	8	1
[9], DPA	21-24	37	48	27	16	2
[10], AB	17.5-20	32	22	8	16	4
CHA5350, AB	17-24	27	27	n.a.	26	4
[11], AB	27-32	33.5	26	9	21	3
HMC756, AB	16-24	33	28	10	22	n.a.
TGA4535, AB	21-24	34	21	7	22	3
[12], AB	19-22	36.5	25	8	22	3
This, DPA	**22.8–25.2**	**30.9**	**38**	**20**	**12.5**	**2**

TABLE II
PERFORMANCE COMPARISON OF MMIC POWER AMPLIFIERS FOR K-BAND POINT-TO-POINT RADIO. PAE_6 IS CALCULATED AT 6 dB OBO. G IS THE GAIN. St. IS THE NUMBER OF CASCADED STAGES.

For an exhaustive survey, we included in Tab. II the DPA of [9], that shows very good performance in K-band, demonstrating the feasibility of the DPA solution for point-to-point radios. However, it has been developed on a 0.15 μm GaN on SiC process. It relies on the intrinsic features of GaN transistors that enable lower DPA complexity to achieve higher output power and PAE with respect to GaAs PAs.

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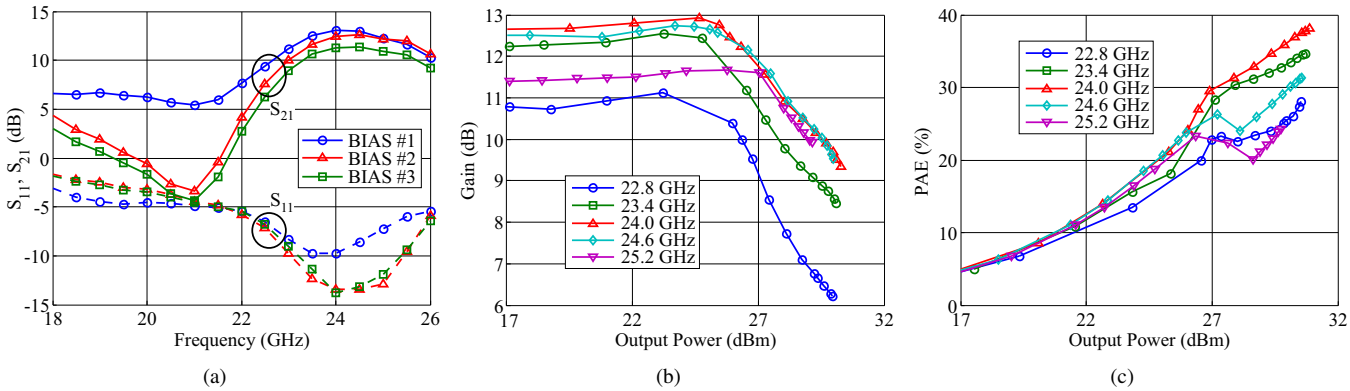

Fig. 11. DPA measured results. (a): scattering parameters in the 18-26 GHz range, at different bias points (see Table I). (b) and (c): gain and PAE vs. output power at BIAS#1 in the 22.8-25.2 GHz band.

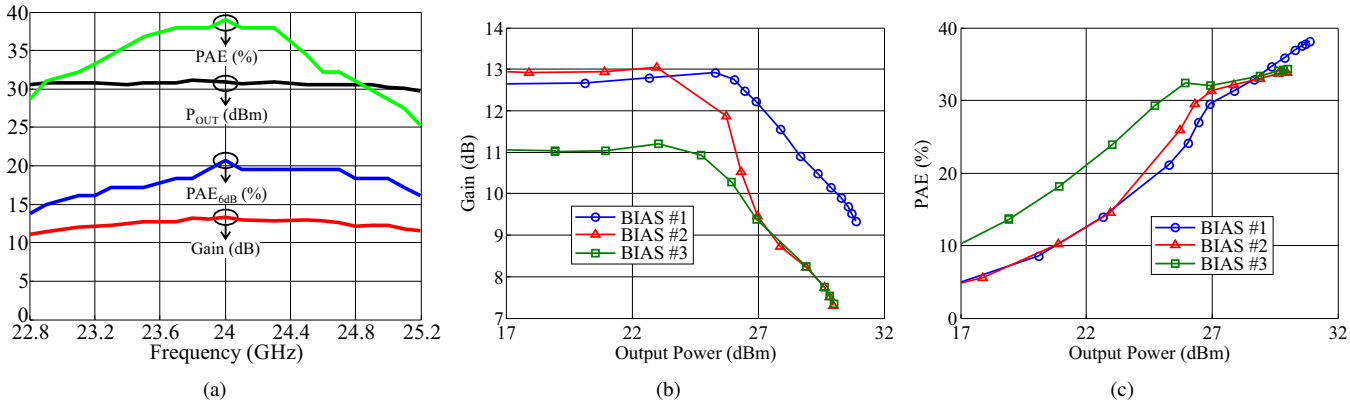

Fig. 12. DPA measured results. (a): CW saturated output power, saturated PAE, 6 dB back-off PAE and gain vs. frequency at BIAS#1. (b) and (c): gain and PAE vs. output power at 24 GHz at different bias points (see Table I).

Since this GaN process is not commercially available, it cannot be considered as an immediate feasible solution for the backhaul radios market. In fact, GaAs technology still ensures advantages in terms of reliability, robustness, cost and back-compatibility when compared to the relatively new GaN process. The commercial 0.25 μm GaN processes available from different providers (TriQuint Semiconductor, United Monolithic Semiconductor, WIN Semiconductors) are targeted to operate at X-band, Ku-band at best. The full release of 0.15 μm GaN processes is, to our best knowledge, still under development.

B. Modulated signal results

The DPA has been characterized also at system level adopting the setup of Fig. 14.

The modulated signal is provided by a vector signal generator (E8267D from Agilent), and the output of the DUT is collected by a vector signal analyzer (N9030A from Agilent). For accurately evaluating the average output power and efficiency of the DPA, a CW on-wafer calibration has been performed, relating the measured power at the DPA plane to the measured power at the vector signal analyzer input.

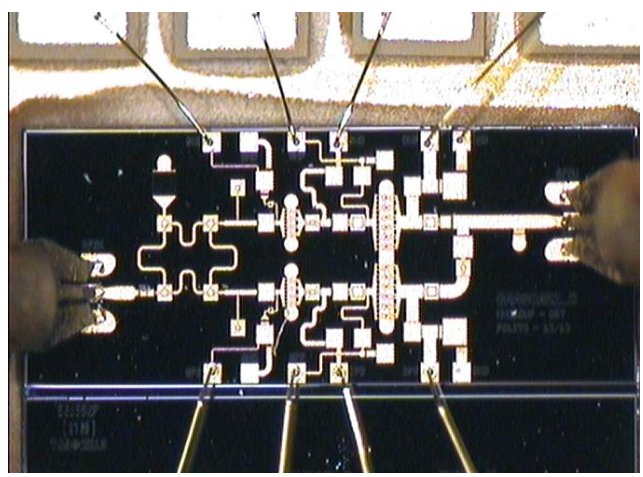

Fig. 13. Microscope picture of the manufactured DPA, with DC bonding wires and microwave probes.

The adopted test signal has been a 256- Quadrature Amplitude Modulation, with 7.5 dB PAPR, and channel of 7 MHz and 28 MHz. The emission mask, chosen according to the European Telecommunications Standards Institute (ETSI), refers

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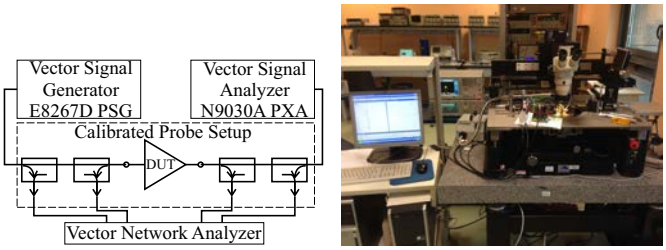

(a) (b)

Fig. 14. Measurement setup for system level characterization and predistortion. (a): schematic; (b): picture.

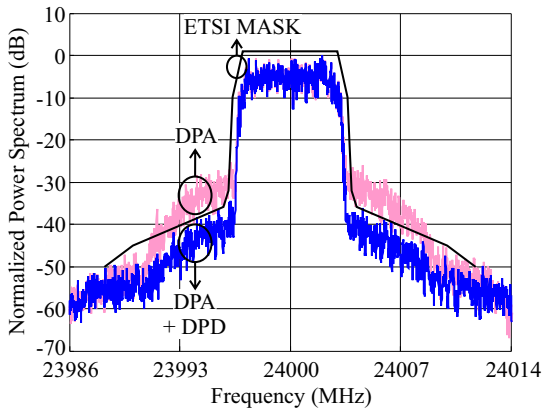

Fig. 15. 7 MHz channel test signal. Measured output spectrum of the DPA, without and with predistortion. ETSI emission mask is reported. Average output power is 23.5 dBm, average efficiency is higher than 14%.

to spectral efficiency classes 6L and 6LA for the 7 MHz and the 28 MHz cases, respectively [13].

ETSI directives refer to a band between 22 and 23.6 GHz. Due to the frequency shift experienced, the characterization has been carried out at 24 GHz.

In both cases, measuring the DPA in BIAS#1 condition of Table I, and setting the average output power at its theoretical limit of 23.5 dBm, i.e., at around the saturated power minus the signal PAPR of 7.5 dB, the mask compliance could not be achieved.

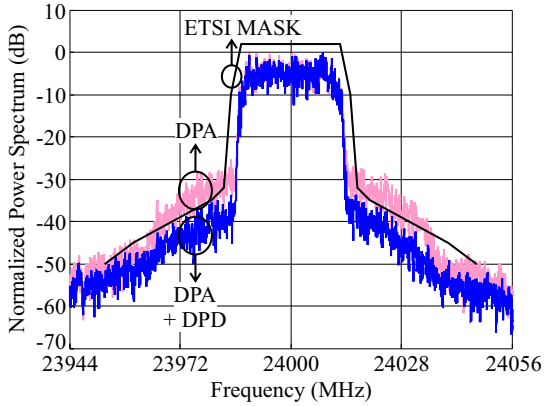

Fig. 16. 28 MHz channel test signal. Measured output spectrum of the DPA, without and with predistortion. ETSI emission mask is reported. Average output power is 23.5 dBm, average efficiency is higher than 14%.

A digital predistorter (DPD) based on a memory odd-polynomial model [14] has been introduced. In both the 7 MHz and 28 MHz channel cases, mask compliance could be achieved, with average output power level of 23.5 dBm, by a DPD odd-polynomial order of $2p + 1$ with $p = 4$, and memory depth of 2. Fig. 15 and Fig. 16 compare the output spectrum with and without predistortion, with resulting average efficiency higher than 14%.

V. Conclusion

Design, simulations, and RF and system level characterizations of a 31 dBm GaAs MMIC Doherty power amplifier for K-band microwave point-to-point radios has been presented. The key design steps, from the topology selection for optimum gain vs. power added efficiency trade-off, to the detailed matching networks synthesis, have been addressed. CW characterization results showed promising results, confirming the feasibility of the adopted strategy, while system level measurement adopting digital predistortion proved good performance in presence of higher-order modulated signals. The partially envisaged frequency shift, related to the high sensitivity to process variation of some parts, will be corrected in the new foundry run with the desensitization of the overall design.

Acknowledgment

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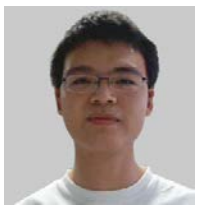

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