Methodology modeling of MaE-fabricated Porous Silicon Nanowires

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A. Antidormi, D. Chiabrando, M.G. Graziano, L. Boarino, G. Piccinini

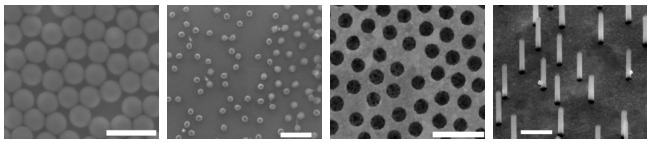
***Abstract*—Porous Silicon Nanowires (PS-NWs) represent very promising electronic devices with a wide range of applications, all taking advantage of the irregular microscopic structure of PS. The strong variability of the electrical properties of the material with technological process makes computer simulation of PS-nanowires a cumbersome task. Here we present a simple model of PS-NWs which can be implemented for simulations in physics-based software TCAD Atlas thus giving a contribution to the investigation of the effects of the peculiar structure on the material resistivity. Extensive simulations have been performed on PS-Nws with microscopic characteristics deduced from our experimental fabricated devices. We investigated the dependence of current from applied voltage and channel doping also in relation with the electrical field inside the device and with the carriers' mobility.**

Finally we suggest an electrical model for PS-NWs easily implemented in commercial circuit simulators (Eldo in this case). It will allow to exploit the actual simulation tools also for the analysis and design of circuits where PS-based devices are present.

I. Introduction

Silicon Nanowires (Si-NWs) are largely being studied in the emerging scenario of (nano)electronics for their versatile properties, their obvious integrability with standard Silicon based technologies, and for the fabrication techniques in several cases exploiting techniques based on self-assembly not requiring lithographic processes. A major distinction should be done between pure-cristalline Si-NWs, mainly used for computation applications [1]–[3] and NWs presenting an irregular, non cristalline, i.e. porous, structure. Porous Silicon (PS) is an interesting material with several possibilities of application, in particular in gas sensing [4]- [5]. It is composed of a network of small Si crystals with a typical size of a few nanometers. This structure makes transport properties of PS rather unique. On one hand, PS cannot be considered a bulk wide-bandgap semiconductor because of its granular structure in the nanometer scale. On the other hand, it is not a insulator, since its crystallites retain the lattice structure of the bulk material. Moreover, the electrical properties of this material largely depend from the geometrical dimensions of the pores as well as their concentration. The consequence is a complete absence of numerical models in commercial device simulators apt to describe the behaviour of PS, as well as of any other kind of models. This is a critical missing point, especially from the electronic applications point of view, since the design of PS sensors systems cannot be verified and engineered as it would be necessary especially in critical applications, as gas sensing might be.

In this paper we aim at filling the gap in two steps. First we introduce a simplified method to model a PS nanowire in a physical level simulator (Silvaco Atlas) using as a reference real geometrical data on PS nanowires (PS-NWs) we fabricated. The goal of this step is to get an solid insight on the behaviour of this simplified structure for varying silicon doping and considering realistic distribution of pores in the NW volume. Second we suggest an equivalent electrical model of PS-NWs that, starting from the physical level results, could be simulated using spice-like simulators (Eldo from Mentor Graphics in our case).



(a) PS nanospheres deposited

(b) After O_2 plasma etch

(c) After Au deposition and spheres removal

(d) After 1' MaE

Fig. 1. SEM images: Si NWs fabrication steps (marker: 500 nm)

The structure of the paper is as follows: in the first section we present a short description of the technological process to fabricate our PS-NW and images showing the resulting devices. The description of the model for PS-NW is treated in section II with the results of some parametric analysis we performed. Finally, an electrical model of PS-NWs is introduced.

II. Technological Process

A. Fabrication of Si NWs

Metal-assisted etching (MaE) is the technique used to fabricate our PS-NWs ([7]). This technique consists in an electroless etching of silicon in $HF/H2O2$ solution. A thin film noble metal catalyzer ($Ag, Au, Pt, AuPd$) is deposited on the surface of the silicon sample. Depending on the geometrical properties of the deposited metal film, different structures can be obtained (nanowires, pores or even more complicated objects). However, It is actually possible to pattern the deposition, thereby obtaining regular layers where areas covered by metal have approximately the same planar dimensions of all the others areas.

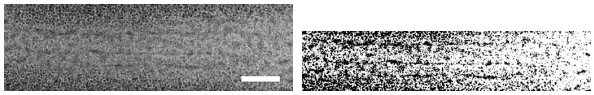
In our case, we chose highly p-type doped silicon (10-20m$\Omega\cdot$ cm $<100>$). Polystyrene (PS) nanospheres (diameter: 210nm $\pm$ 5%) were spread on the silicon sample by spin coating in order to obtain a self-assembled hexegonal-packed monolayer (fig. 1-a). Their diameter has been later reduced of a factor 2 via oxigen plasma etching (fig. 1-b). At this point, a 20 nm thick Au film was deposited on the surface using e-gun evaporator. This machine allows to achieve a continuous film also in case of very reduced thickness. Finally, PS nanospheres

have been removed in ultrasonic bath obtaining an "antidot" metal pattern (fig. 1-c).

We performed MaE dipping the sample in a solution of ($(H_2O$:H_2O_2:HF 1:1:3)) at a temperature of $60°C$ for 1 minute. Fig. 1-d clearly shows NW which diameter is the same of the reduced nanospheres.

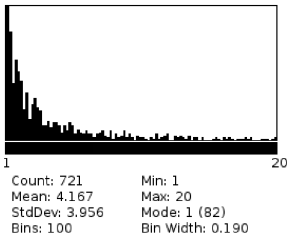
B. TEM analisys

Transmission Electron Microscopy (TEM) was performed after having scratched the fabricated NWs on a TEM grid. Hence, their structural properties could be investigated and extrapolated data have been used as a starting point for subsequent simulations. Fig. 2-a shows the internal structure of a NW: darker dots are nanocrystals of silicon immersed in a porous structure. Using ImageJ software it can be possible to locate the nanocrystals exactly and, consequently to statistically evaluate mean and distributions of their geometrical properties. Starting from these images, a binary (b/w) copy is generated (fig. 2-b) and a graph of the area distribution can be plotted, like in fig. 2-c. According to the results in the picture nanocrystals have an average area of 4.1 nm.



(a) TEM image of a single Si NW (marker: 50 nm)

(b) ImageJ b/w conversion



(c) Area distribution of Si nanocrystals

Fig. 2. TEM image analisys

III. PS-NW MODELING AND SIMULATIONS

In this section we describe the procedure we followed to construct a simple model for a porous silicon nanowire; this model is suitable for numerical analysis in the physics-based software TCAD Atlas [9]. Electrical characterization of a PS-NW can then be performed and data on the main electrical quantities of the material can be obtained together with their dependence on physical and geometrical parameters.
As it is evident from Fig. 2-b, representing the results of elaboration of an image of the fabricated nanowires, silicon nanocrystals are immersed among non-crystalline regions forming an irregularly networked pore structure. At the best of authors' knowledge, no models are present in physical simulators for porous materials, nor physical data are present to describe their electrical properties (mobility, energy gap, dielectric constant,...); the reason for this being the unavoidable dependence of the electrical parameters of the materials from the dimensions of the pores and from their effective shape.
Our research for a simulative model of PS-NWs is also driven by a second idea. The uniform distribution of the pores along the channel and the statistics of their geometrical properties make an analytical treatment of the electrical problem rather impractical. Consequently, the simulative approach seems to be the most promising way to tackle the problem and, in order for it to be effective, a physical model of these devices is strongly required.

A. PS-NW model

We modelled a PS-NW as a 3D-wire with square section composed of p-doped crystalline silicon ($N_A = 10^{15}$ atoms/cm^3). Its lateral surfaces are drilled through slit pore segments randomly arranged and filled with air. These pores have a squared section; their number, depth and position are randomly chosen according to the geometrical properties of our fabricated devices in a way which will be explained in the following. An image of a silicon nanowire with this structure is shown in Fig. 3-a.
This is the simplest model of a pore in a S-NW: air has been inserted in the volume created from the slits. However, in general, non-crystalline silicon and/or gas fill that space, thus changing the electrical conductivity of the whole device. To keep things treatable by Silvaco Atlas software, air is actually the proper choice. Secondarily, this allowed us to focus attention on the dependence of the nanowire resistivity from the physical parameters of the device. It is worthy to be mentioned that the peculiar geometry chosen for the pores does not restrict the range of devices to be simulated and subsequently does not limit the validity of the obtained results. In fact, we left the pores the possibility to spatially overlap and intersect each other so that ramified porous entities can arise thus making the pores' geometry rather arbitrary.
The contacts have been chosen to be non-rectifying metal contacts in order not to include the effects of the Schottky contacts in the transport process.
We have described the structure of the PS-NW in Atlas software by means of a rectangular mesh, denser in correspondence of the interfaces between different materials (silicon-air/metal) and sparser elsewhere. This guarantees a faster convergence of the numerical method implemented in the nodes of the grid. The image of a mesh as described in Atlas is depicted in fig.3-b.

To compute the relevant electrical quantities in the PS-NW we adopted a Boltzmann distribution of the carriers in the channel. Moreover, their mobility has been chosen to depend on the local electrical field according to the model FLDMOB implemented in Silvaco Atlas. It takes into account the effect of velocity saturation of the carriers through a reduction in the effective mobility according to the Caughey and Thomas expression which provides a smooth transition between the low-field and high-field regimes ([9]). As it will become clear, non-uniformities of the electrical field in the channel are responsible for a gradual reduction of the current with the applied voltage. This mobility model coherently describes the current saturation effect in non-homogeneous electrical fields.

The nanowire we analysed through simulations has a channel length of $100nm$ and a squared section of $900nm^2$. In order to obtain valuable information about the fabricated

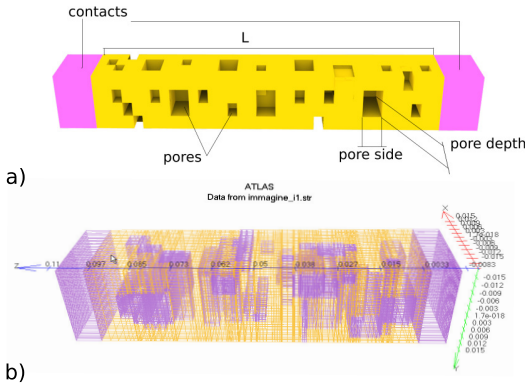


Fig. 3. a) Scheme of the model for Porous Silicon Nanowire; b) Atlas mesh of a PS NW (pores are coloured in purple).

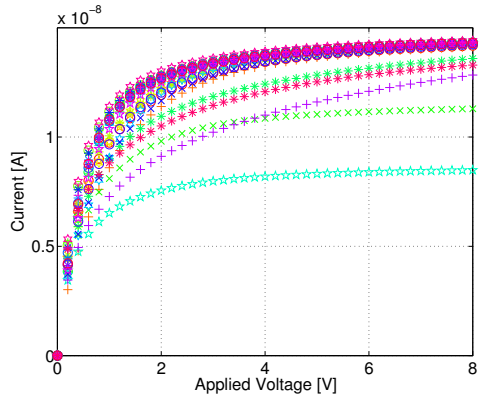


Fig. 4. Voltage-Current characteristics of some PS-NWs with 30 pores having different geometrical parameters (position, depth, side). Their position along the wire is uniformly distributed, their depth and side are normally distributed.

nanowires, we simulated many devices whose pores present geometrical characteristics similar to those shown in fig. II-B. According to the results of a statistical analysis on the actual pores, their distribution along the simulated wire is uniform while the pore depths and sides are normally distributed with average values respectively $\mu_{depth} = 19.2nm$, $\mu_{side} = 6.3nm$. The corresponding standard deviations are $\sigma_{depth} = 11.4nm$, $\sigma_{side} = 3.2nm$.

B. Simulation Results

Fig.4 shows the current-voltage characteristics for some actual realizations of silicon nanowires: each curve corresponds to a particular device with specific distribution and properties of pores. As it is clear, the current behaviour is strongly non-linear, each curve reaching a saturation value for sufficiently high voltage applied. Specifically, in the regime of low voltage, the current in each nanowire increases linearly with a slope which is influenced by the concentration and dimensions of the pores. A larger amount of silicon removed by the pores produces a greater differential resistivity of the device since less conductive paths are available for the current. As the voltage is increased, the current rate gradually decreases. This behaviour can be justified by considering the distribution of the electrical field in the channel (Fig. 5): for sufficiently high voltage the electric field ceases to be uniform, becoming more intense in certain particular regions (lighter regions in

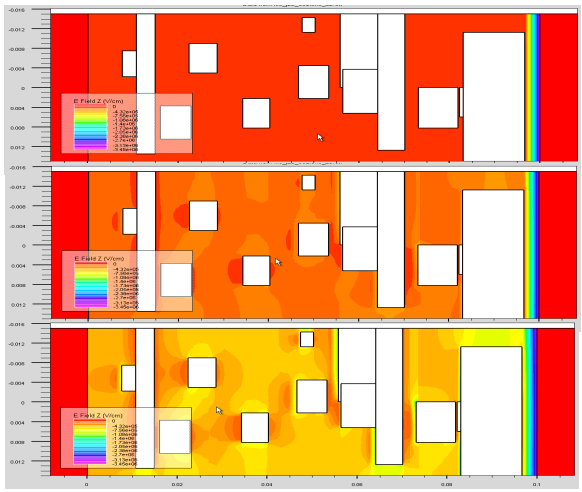


Fig. 5. Electric field distribution in a section of a PS-NW with L=100nm and section $900nm^2$ for V=0.2V, V=2.5V and V=8V from top to bottom respectively. The uniform electric field for low voltages becomes soon non-uniform for higher voltages provoking the velocity saturation of carriers in some channel regions. Higher voltages increases the extensions of saturated regions and total current consequently plateaus.

the figures). There, the electric field will soon reach a value such that the mobility saturation will occur according to the transport mobility chosen. The current flow in that region will consequently be limited by the mobility of the carriers thus reducing the overall charge flow along the device. Current will continue to increase with voltage until more regions will be interested by a strong electrical field. Then the current will plateau. The voltage at which the current deviates from linearity and the saturation current are actually dependent on the specific configuration of pores along the channel.
Fig. 6 shows the differential resistivity of a PS-NW averaged over the ensemble of devices which have been analysed. The vertical bars in the figure represent the standard deviation. The resistivity naturally grows with voltage, while the increment of the corresponding standard deviation can be explained with the fact that for high voltages a small difference in the differential variation of current for two devices can result in a large difference in the differential resistivities: these consequently present a larger deviation from the average value.

We finally discuss the results of the simulation of the ensemble of different nanowires for different doping channels. Higher doping levels produce lower resistivity as shown in Fig. 7 where the average resistivity and its standard deviation computed at $V = 1.0V$ are depicted. Moreover, larger deviations from the average values are found for increasing doping level, due to the fact that, for fixed applied voltage, electrical field in more doped channels is higher with respect to the electrical fields in channels with lower doping. In more doped devices this reduces the carriers' mobility (increasing resistivity) counteracting the effects of the augmented concentration of carriers through doping. Doping can then be used to trim the sensitivity of the sensor, as well as applied voltage has to be carefully defined at the PS-NW sensor engineering phase. In other words, detailed data on what can be obtained are essential during a sensor design and simulation phase, thus confirming the importance of the modelling attempt presented in this work.

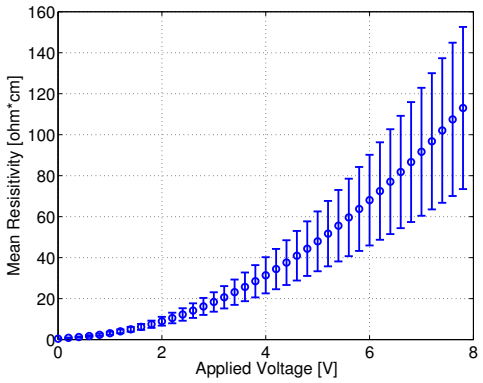


Fig. 6. Differential resistivity of a PS-NW with L=100nm and section $900nm^2$ as a function of the applied voltage. The vertical bars represent the standard deviation.

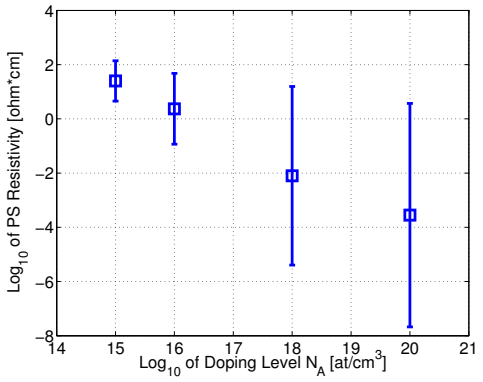


Fig. 7. Differential Resistivity computed at $V = 1.0V$ averaged over a large number of nanowires with different channel doping.

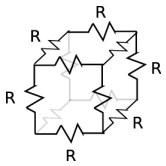


Fig. 8. Elementary block of the circuit model of a PS-NW.

IV. A POSSIBLE ELECTRICAL MODEL FOR PS-NW

We conclude the paper with the suggestion of a possible electrical model which could be implemented in commercial circuit simulators, like Eldo. This would allow to exploit the existing simulation tools for the analysis and design of circuits where PS-NWs are present. Once the physical parameters of the device have been explored through a physics-based simulation (Sect.III) and the electrical model has been defined, the analysis and design of complex circuits by means of a commercial simulator is dramatically simplified and time-efficient.

The whole geometrical structure of our nanowire is subdivided in many elementary blocks of cubic shape. Each cube is substituted by the block depicted in fig.8, a 3D 4-terminal component made of simple resistors representing the main possible conductive paths for carriers in a piece of material ([5]). The values of the resistances included in each block is actually variable, depending on the applied voltage, the physical dimension chosen for the elementary cube and from the doping level of silicon. In general they can be obtained from the electrical field distribution computed via a physical simulation. By connecting more of these blocks together, the equivalent circuit model for a PS-nanowire is obtained. The validity of the model can be easily extended to the deep nanometer regime, when quantum confinement effects start to affect the transport properties. In our simple model these effects can be included by adding some more conductive paths (resistances) in the elementary blocks. For example, resistances of proper value could be inserted across the pores to describe the tunnelling current contribution while quantum resistances can be added if ballistic regime is to be included in the computations.
We actually developed the elementary block in Eldo and built a whole model for a PS-NW. However, a complete analysis of the values of the resistances and a validation of the model is yet to come.

V. CONCLUSION

In this paper we described the state of our research in fabrication and modelling of Porous Silicon NWs. Starting from a statistical analysis of the fabricated NWs, we devised a simple model for a PS NW which can be implemented in the physics-based simulator TCAD Atlas. We used it to investigate the current-voltage characteristics of an ensemble of PS-NWs with different pores' distribution and doping: we revealed the relation between the current non-linear behaviour in terms of the electrical field in the channels. Finally, a simple modular electrical circuit for a PS NW has been, capable of being implemented in commercial circuit simulators.
In the future, electrical characterization of the fabricated nanowires could give more information on the electrical properties of Porous Silicon and good agreement between numerical and experimental data will be sought.

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