13-bit GaAs serial-to-parallel converter with compact layout for core-chip applications

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Abstract

Design and characterization of a 13 bit serial-to-parallel converter in GaAs technology for smart antennas are presented. The circuit has been realized with NOR-based super-buffered enhancement/depletion logic, and optimized for a compact layout. The serial-to-parallel converter operates properly well above the 20 kHz design clock frequency.

Keywords: serial-to-parallel converter, gallium arsenide, core-chip, smart antenna, X-band

1. Introduction

The adoption of smart antennas, synthetic aperture radars and phased array radars on satellites and other aero-spatial carriers is experiencing a huge development. The radiating elements of those systems, that can be in the order of some hundreds/thousands, are fed by RF amplitude and phase controlled signals to achieve the required beam-forming. Core-chip MMICs integrate all the electronic subsystems needed to set the proper signal amplitude and phase for each radiating element, and greatly simplify the overall system architecture. Every Core-chip needs to be digitally driven by a central unit, controlling the RF programmable elements, e.g. switches, phase shifters and attenuators, through a dedicated number of connections.

In case of parallel-controlled Core-chips [1, 2, 3], the interface between the MMIC and its control unit is rather complex, since many pins are needed; such solution is therefore hardly acceptable for control words exceeding 10 bit. When more bits are required, as in the present case, a possible solution is the integration of a serial interface between the Core-chip and its control unit [4, 5, 6], whose main advantage consists in a reduced number of control signals required for data and synchronization, that becomes independent from the number of bits. Such implementation requires the Core-chip to embody a digital section able to handle the serial data stream deriving the control word with proper parallelism to drive the RF elements. In this paper,

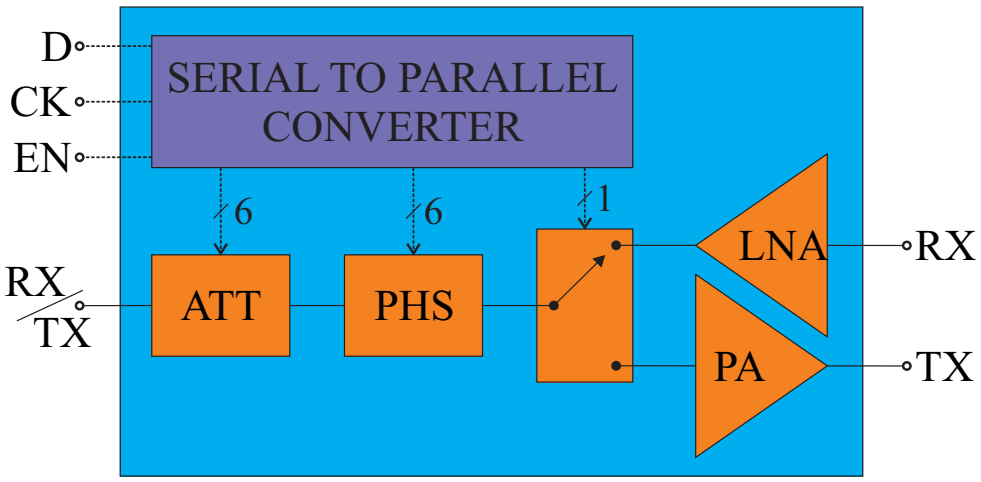

Figure 1: Core-chip structure with integrated serial to parallel converter.

a compact 13 bit serial-to-parallel converter (S2P) is presented: it is realized in GaAs technology, suitable for the integration in a X-Band phased-array antenna core-chip. The latter requires 6 bit for the phase shifters, 6 bit for the programmable attenuators and 1 bit for RF transmit/receive selection, see Fig. 1. Although the GaAs MMIC technology is now standard for microwave analog applications, the realization of GaAs digital ICs still faces several issues. Firstly, the lack of complementary GaAs logic forces towards the selection of an enhancement/depletion (E/D) technology, and for this reason the ED02AH 0.18 μm pHEMT GaAs process by OMMIC has been chosen. The integration of GaAs-based logic increases the chip size and total power consumption: these figures of merit have been optimized in the present work.

Furthermore, the robustness of the resulting design *vs.* process variations, a crucial issue in GaAs-based digital circuits, has been carefully considered.

The idea allowing a major reduction in the resulting area occupation consists in an innovative NOR solution, realized introducing layout modifications at the single active device (HEMT) level. The area reduction, as compared to standard realizations, is about 20 % and 28 % for the NOR structure and D-type flip-flop, respectively. This solution has been combined with an accurate optimization campaign involving all the basic structures, to reduce the power consumption and to improve noise margins. The final design has been realized and tested. The S2P detailed design and performance that comply with the system requirements are here presented. The specific measurements of the D-type flip-flop performance have been carried out and presented in [7], while full RF Core-chip behavior and performance have been tested exhibiting very good agreement with the expected ones [8]. Table 1 reports a comparison of the full Core-chip characteristics with other published examples: the proposed solution has comparable complexity with respect to the other examples, but offers, in comparison with other serial control solutions, a reduced area occupation.

Ref.	**Band (GHz)**	**Interface**	**Att. Bits**	**Phs. Bits**	**TX/RX Bits**	**Area (mm^2)**
[1]	3-3.5	Paral.	7	6	1	4.3×3.9
[1]	5-6	Paral.	6	7	0	3.3×3.8
[1]	8-11	Paral.	8	7	1	4.3×3.3
[2]	8-12	Paral.	6	6	1	4.5×5.5
[3]	9-10.2	Paral.	3	0	1	3.0×2.0
[5, 6]	8–12	Serial	7	7	1	4.4×4.2
This Work	**8.6-10**	**Serial**	**6**	**6**	**1**	**4×3.7**

Table 1: Comparison of the Core-chip embedding the serial-to-parallel converter here presented with other published Core-chips. Att. Bits, Phs. Bits and TX/RX Bits are the number of bits assigned to attenuator, phase shifter and mode selection, respectively.

The paper is structured as follows: in Section II the design procedure of the basic logic blocks of the structure is presented; the full S2P design is described in Section III, and the measurements on the final structures are shown in Section IV together with a description of the experimental setup; finally, conclusions are reported.

2. System Architecture

The implemented S2P block diagram is reported in Fig. 2, where the constitutive parts of a serial-in/parallel-out shift register are evidenced. The input serial data stream (D) shifts from one memorization unit to the adjacent at each clock event. Signal control data (EN), common to all units, activates the cell inputs transfer, i.e. the bits of the data stream under shifting, to internal latches that hold the S2P outputs controlling the programmable RF analog blocks (attenuators, switches and phase shifters). The system architecture has been obtained by reiterating a basic cell. This primary unit, shown in Fig. 2, is realized stacking a pair of D flip-flops (DFF, which are the logical level building blocks), driven by clock (CK) and enable (E) control data. This modular strategy, where identical cells perform latching and shifting of each bit, allows to modify the system parallelism by simply changing the number of cascaded basic modules, hence preserving system architecture and design strategy at logic and electrical layers. The D flip-flop is im-

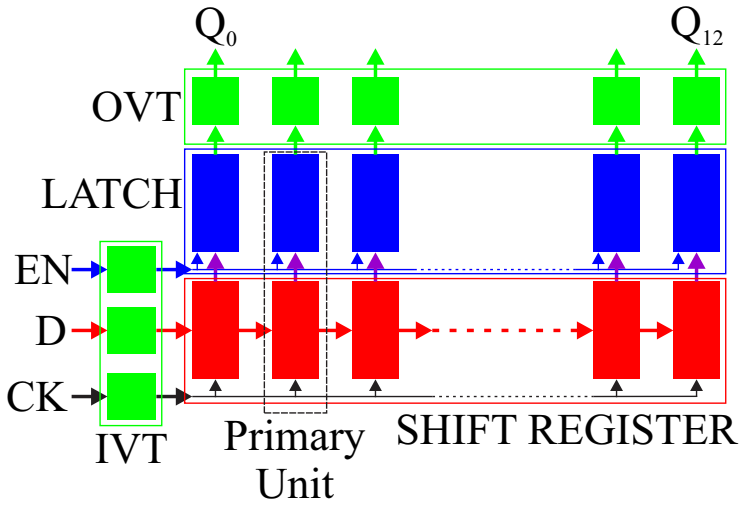

Figure 2: Block diagram of the designed S2P converter.

plemented as a negative edge-triggered D Flip-Flop (DFF), according to the NOR gate expansion reported in Fig. 3a. The input and output voltage translators (IVT and OVT, respectively) provide the compatibility with external logic and with analog microwave circuits respectively, in terms of voltage levels and waveforms specifications. In particular, IVTs have been designed

to ensure TTL/CMOS compatibility at input, while OVT output voltage levels have to be consistent with the -3.9 V pinch-off voltage of OMMIC HEMTs. Area occupation design limits ($3\times1\,mm^2$), and power consumption design constraints (less than 250 mW) required accurate analysis and design optimization of all S2P subsystems. In fact, the design started from an accu-

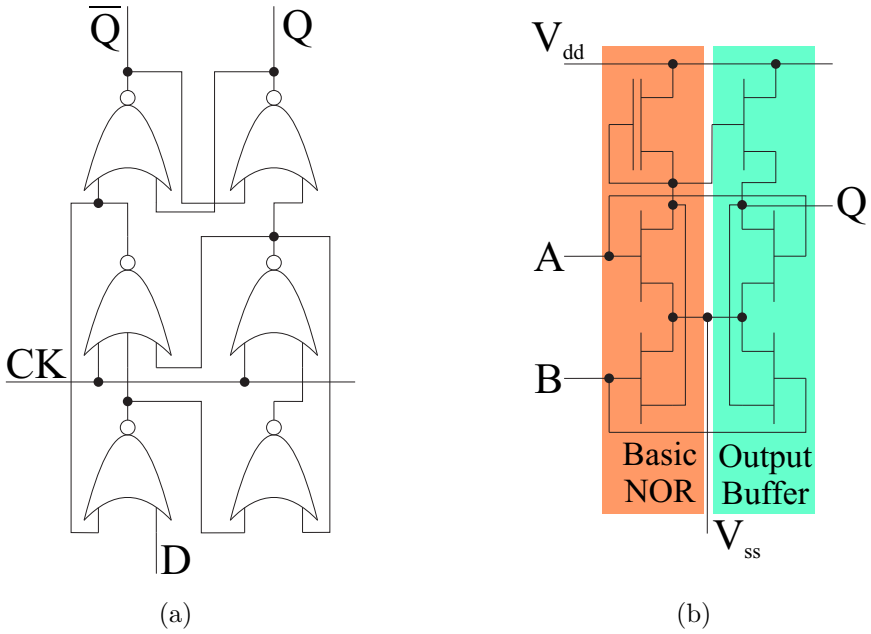

Figure 3: Schematics of the DFF (a) and of the EDSB NOR (b).

rate comparison of the simulated performance achievable with the available GaAs logic families. All simulations have been carried out both within Agilent ADS CAD suite (used also for layouting) [9], and Spice-like environment, where foundry design kits are available. Considering the adopted technology features (OMMIC E/D 0.18 μm pHEMT GaAs process), NOR-based Super Buffered Logic (EDSB) [10] has been identified as the most suitable. It allows in fact a reasonable compromise between occupied area and power consumption, ensuring at the same time acceptable noise margins and tolerance to process dispersions. A statistical analysis has been carried out through ADS Montecarlo simulations using the information and modeling of the OMMIC process dispersion available in the design kit. A preliminary appraisal has been carried out also to optimize the gate peripheries of the HEMT devices

within the flip-flop, to define the aspect ratio between gate widths of the active pull-up and pull-down HEMT pairs. NOR gate, chosen as the base logic port, is realized as a multiple-input extension of an inverter, according to the scheme shown in Fig. 3b [11], where the logic function is implemented through a pair of complementary E/D PHEMTs, with an additional buffer stage to increase noise margins. Optimum voltage supplies have been selected through extensive simulations including effects induced by input and output translators, that impact on power consumption and internal data synchronization. Supply voltage of 1.4 V provides a good trade-off between noise margins and power consumption. The latter are indicated by simulations around 0.8 V and 7 mW, respectively. Further increasing the DC supply voltage negatively impacts on DC power consumption, without significantly improving the noise margins. Clock, Enable and data IVTs are implemented

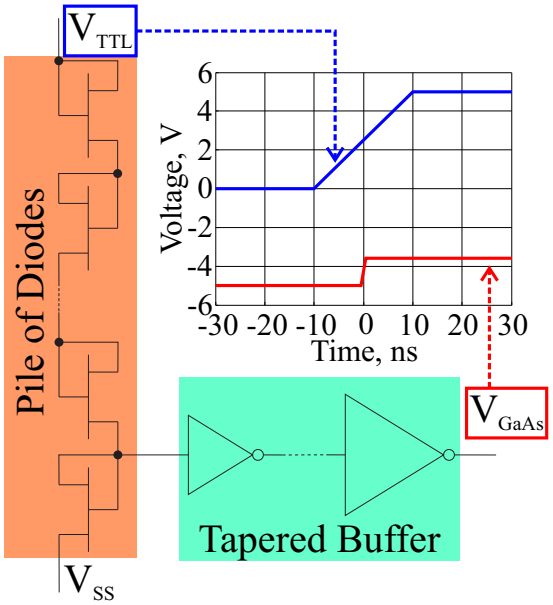

Figure 4: Circuit schematic and behavior of IVT.

as two-stage modules (Fig. 4): the first stage, common to all three signals, is realized through a series of diodes providing the voltage drop between external 5 V TTL/CMOS level and internal 1.4 V supply. IVT second stage behaviors are crucial for the S2P proper operation, and their realization is different for the three cases. In fact, simulations stressed that, due to the high

speed of GaAs-based logic, Same Edge Skew [12] phenomena, producing multiple bit shifting on the same clock edge, can occur. This issue is particularly critical for the CK signal, since specifications for the S2P proper operation, evaluated through simulations, indicate a 0.45 ns maximum falling time. The external TTL/CMOS clock signal with minimum 20 ns falling time must be therefore properly reshaped forwarding it through a cascade of properly designed tapered buffer, before it could simultaneously drive all flip-flop clock inputs. Simulations, accounting also for process variations through statistical and yield analysis, allowed to identify an optimized linear taper profile realized by progressively enlarging the pHEMTs periphery within the several buffers of the chain. Since EN and D signal constraints are less demanding (maximum 10 ns falling time), simplified buffering strategies can be adopted in these cases: two inverter stages are cascaded for EN, while a single inverter is adopted for D signal. The introduced negation of D is compensated by the output translators that introduce a logic inversion too. Finally, all IVTs have been optimized by considering a minimum 2.4 V V_{IH}, and a maximum 0.4 V V_{IL}. A E/D totem-pole structure (logically behaving as a NOT, see

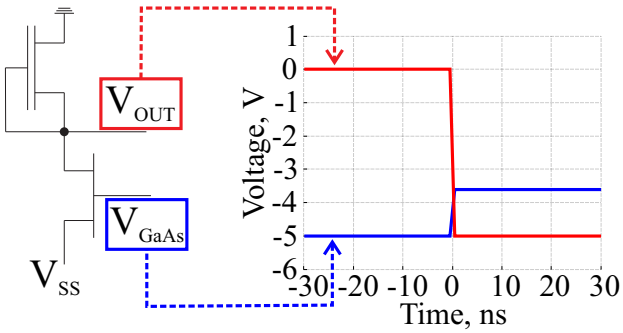

Figure 5: Circuit schematic and behavior of OVT.

Fig. 5) is chosen for the OVTs, with optimized aspect ratio of 2 between E/D PHEMTs, that are biased between VSS= -5 V and 0 V (GND). The S2P will be therefore supplied with two negative voltages (namely $V_{DD} = -3.6$ V and $V_{SS} = -5$ V), providing the aforementioned 1.4 V difference. The voltages are negative with respect to the ground reference, in common with the RF section. The total number of output connections is 18, since for the outputs of the S2P labeled from 9 to 13, that operate in differential mode, both direct and inverted outputs have to be provided. Accounting for the 3 digital

inputs (D, CLK, EN), and the 2 DC biases, one for the digital part and the other required by OVTs for RF level compatibility, the total number of I/O pins of the S2P hence amounts to 23: the 18 output internal connections to the RF section, and the 5 external inputs.

3. Layout design

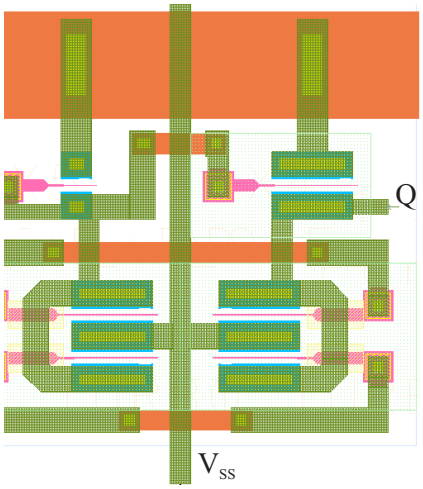

Figure 6: Layout of the 2-port TURBO NOR.

Thanks to the S2P modular structure, minimization of the occupied area can be carried out at flip-flop level, and several solutions have been investigated to optimize the NOR ports embodied in the flip-flop structure. To meet the severe area constraints, the layout compactness has to be maximized, and to this purpose the layout at active device level has been modified to exploit multi-finger HEMTS with interrupted metal interconnections among gate fingers. This essential process variation allows to realize all multiple pull-down transistors required in a NOR using the HEMT internal connections among drains and sources, without any additional cost, in term of used area and routing (see Fig. 6). This innovative process modification allowed the realization of extremely compact two- and three-input NOR gates (TURBO NORs). At DFF level, such modification yields to a 28 % estimated area reduction as compared to standard DFF layouts, see Fig. 7, where pull-down HEMTs drain and source terminals are connected through external routing.

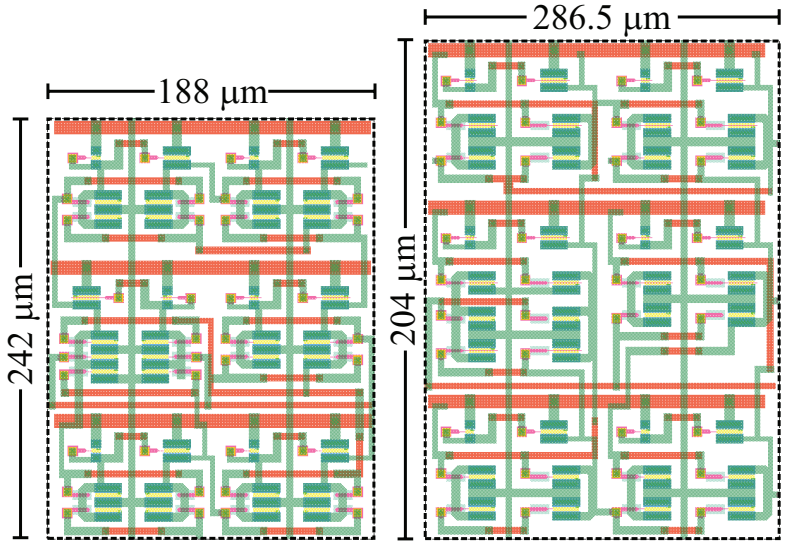

Figure 7: Comparison of TURBO (left, 0.045 mm^2) and standard (right, 0.058 mm^2) DFF layouts. Area saving with TURBO solution is around 28%.

To ensure great flexibility in terms of connections with the RF sections, flip-flop and latch pillar layouts are designed to be indifferently vertically flippable without affecting connections with the adjacent bit cells. In this way direct and negate outputs can be located, to fit RF design requirements, at the S2P top or bottom sides, hence optimizing connectivity and routing between digital and analog Core-chip sections. S2P layout geometry is composed by 13 cascaded cells whose two DC supply voltages are distributed through a pair of metallization rails that, from the external pads, reach the 13 cells to which they dispense the required currents. Since the voltage drops along the rails, induced by the supplied current, actually reduce the cell effective DC bias voltages, rail widths have to be accurately sized to minimize noise margin degradation. In the above context, two important comments have to be outlined: firstly, the cells located far away from DC pads suffer the biggest penalty from such issue. The second consideration is on the current level, that is unevenly distributed along the rails: it is maximum at the DC pad section, and progressively decreases moving inside the S2P. Optimal rails width design would require a tapered profiles compromising the S2P structure modularity; since the latter is a guideline of the present design strategy, this option will not be considered. In fact, the bias rail design has been car-

ried out accounting for the metal paths resistivity, trading off between rail widths and S2P size. When allowed by routing issues, both metallization layers provided by the technological process have been used, to reduce as much as possible the ohmic voltage drops along the DC supply lines. The resulting S2P overall size is $0.8 \times 2.7\,\mathrm{mm}^2$.

4. Prototype Characterization

For a complete characterization campaign, the S2P and the most important subsystems have been fabricated and realized as stand-alone test cells. In detail, together with a stand-alone fully probable S2P, the TURBO NOR, the CK IVT, the OVT and the DFF have been realized.

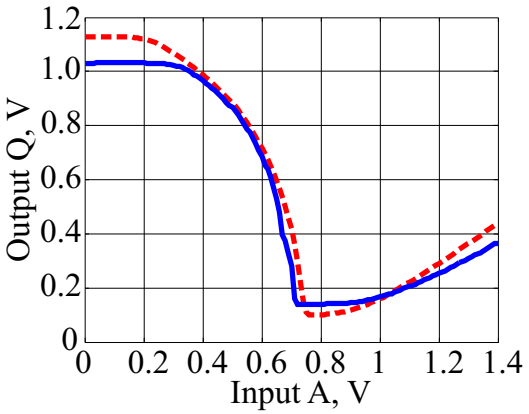

Figure 8: Trans-characteristic (Q vs. A) of the TURBO NOR, with input B set at '0'. Red dashed curve: simulation. Blue curve: measurements.

The two-input NOR trans-characteristic has been measured with respect to both input signals, showing a good agreement with the behavior expected from simulations. Fig. 8 compares simulated and measured NOR response when one of the inputs (B) is set at zero logic level. The layout of the fabricated DFF version suitable for probing is reported in Fig. 9 (dimensions of the flip-flop are $60 \times 50\,\mu\mathrm{m}^2$). Static characterization confirmed its expected behavior. Additional measurements have been carried out to assess DFF behavior vs. frequency, to evaluate its speed performance up to 40 MHz, a limit fixed by the capabilities of the experimental setup. The DFF exhibited the correct behavior, together with a constant 6.5 mW power consumption over

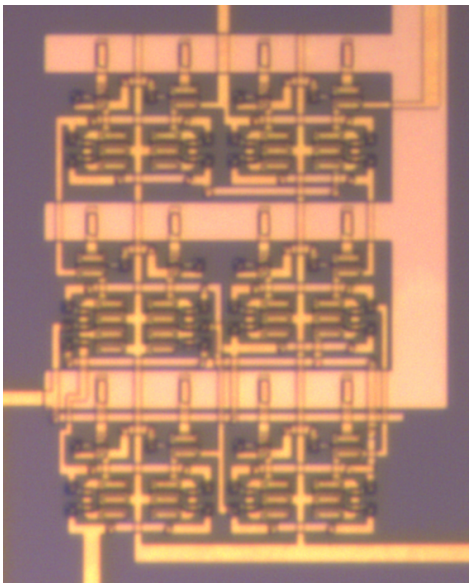

Figure 9: Microscope picture of the realized DFF.

the measured frequency range. Characterization results at the maximum frequency (40 MHz) are reported in Fig. 10.

Concerning the complete S2P test, an ad-hoc probable layout has been designed, with pad array geometry compatible with available commercial probe pitches. Apart from the test-pads, the layout is identical to the one embedded in the complete core-chip. Fig. 11 shows a microscope picture of the circuit, with highlighted building blocks on the lower-side figure.

The devised test procedure has been carried out over 21 chip samples using a dedicated and fully automated measurement set-up, able to scan and verify all the 2^{13} possible configurations (Fig. 12). Measurements are carried out through a Digital Oscilloscope (Agilent DSO6034) that samples, using an analog multiplexer board, the 13+5 output signals, together with the three digital input signals (CK, D, EN) generated by three synchronized Agilent 33220A Arbitrary Waveform Generators. Supply voltages are provided by an Agilent 6624A programmable 4-channel DC source, allowing also for DC current monitoring, and hence power consumption evaluation, that resulted around 220 mW. The full characterization has been carried out at the operating frequency of 20 kHz. Finally, Fig. 13 reports very significant measurements: the input signal (a single pulse) is sampled at each clock

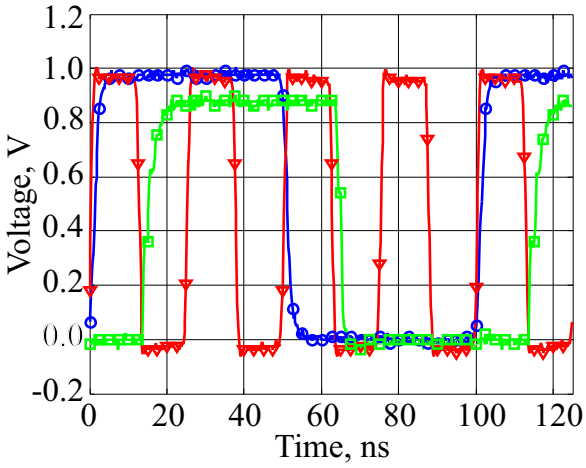

Figure 10: DFF response with 40 MHz clock. Red line with triangles: clock. Blue line with circles: input data. Green line with squares: output data.

falling edge (20 ns falling time), and the enable signal is triggered at every period (falling edge with 20 ns falling time). Proper outputs shifting of the pulse can be observed, thus confirming the S2P correct behavior. The effect of the DC level on noise margins, and logic behavior has been tested through characterization at several voltage supply levels. The S2P demonstrated to properly operate for voltages above 1.2 V, hence showing a good safe margin with respect to the nominal 1.4 V bias. It is also to be remarked that the designed S2P (as integrated into the overall Core-chip) has been tested [8], successfully demonstrating its correct behavior, at Core-chip level. In fact, RF characterizations in terms of phase shifting, and attenuation as a function of the input controlling data configuration, exhibited the expected proper behavior for all logical input configurations.

5. Conclusions

The design and characterization of a GaAs-based 13 bit S2P for Core-chip applications have been presented. The full design procedure has been described, starting from the basic logic blocks and focusing on the interfaces with the external control and RF circuitry. The resulting layouts are shown, and the measured performance of the converter demonstrates its correct operation, well above the design frequency. The S2P can be easily re-sized to a

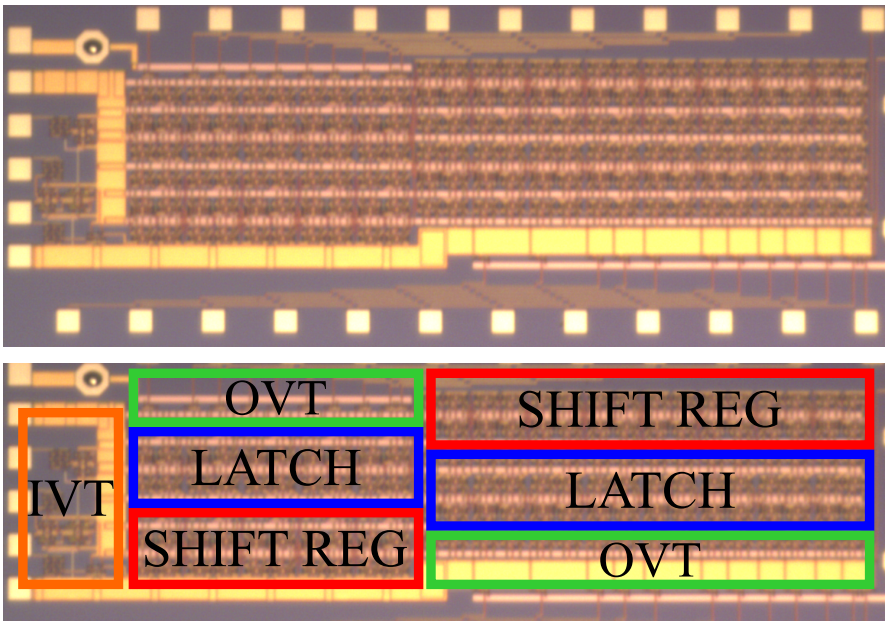

Figure 11: Microscope picture of the probed-for-test S2P (top); highlight of the building blocks (bottom).

different parallelism. The complete Core-chip has been realized, successfully tested, and the results have been here reported and commented.

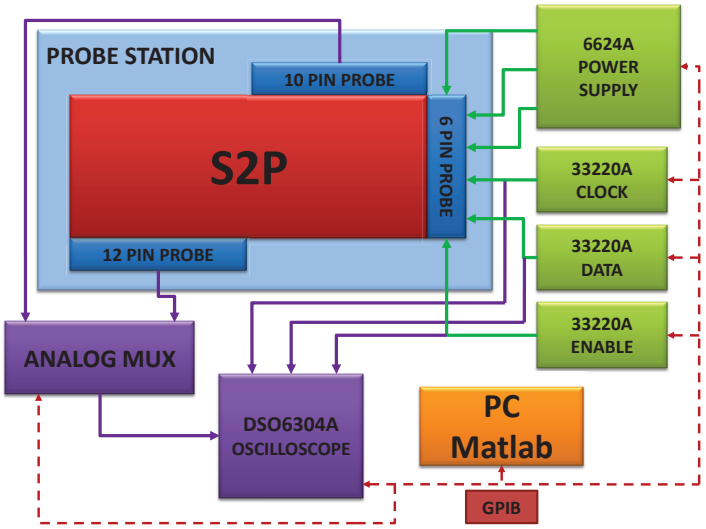

Figure 12: Block diagram of the experimental setup.

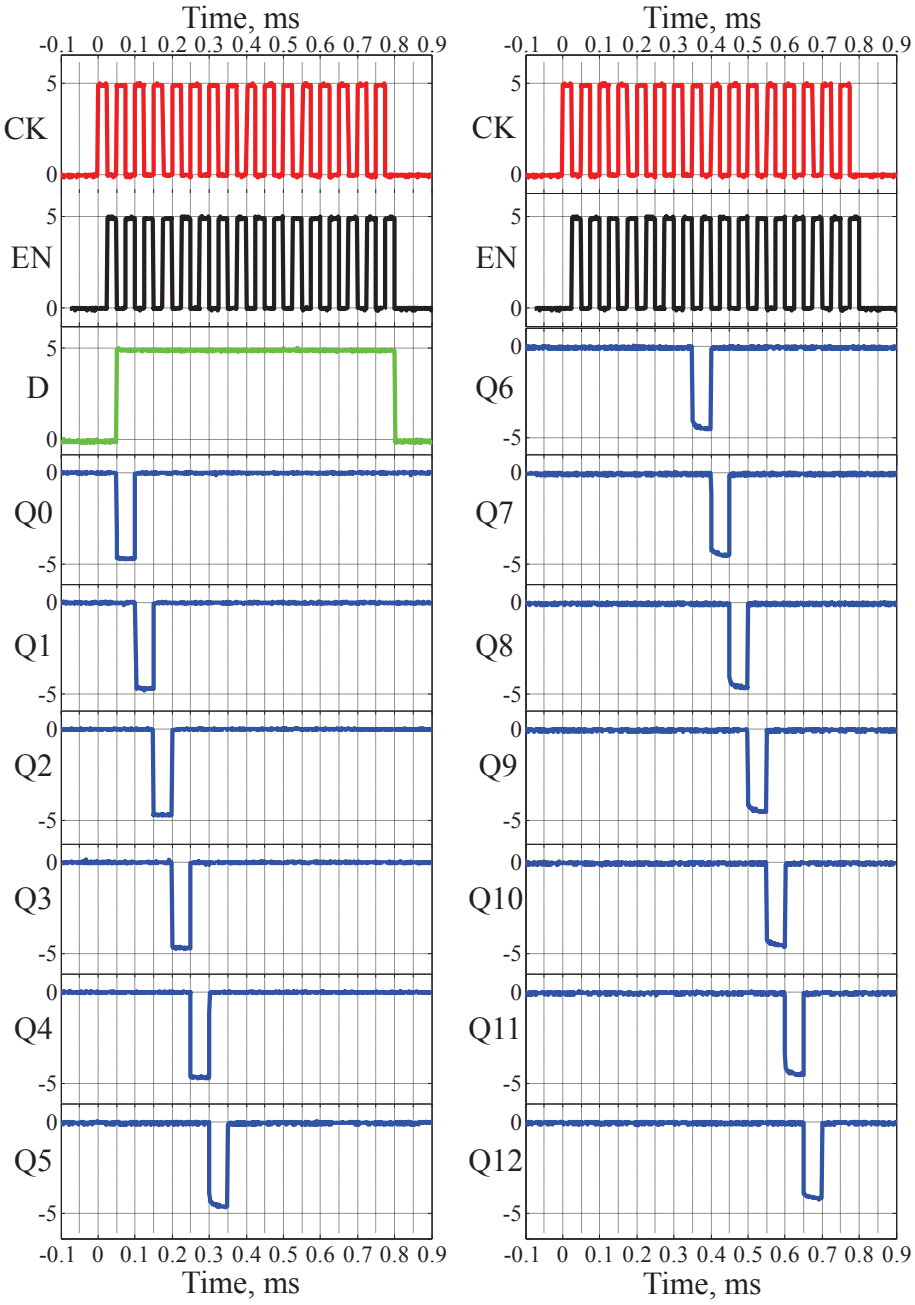

Figure 13: S2P measured performances at 20 KHz clock, with a single '0' pulse input.

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