Time domain dynamic electrothermal macromodeling for thermally aware integrated system design

Time Domain Dynamic Electrothermal Macromodeling for Thermally Aware Integrated System Design

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***Abstract*—Time domain identification of reduced thermal dynamic models is pursued with well established macromodeling techniques, providing electrical equivalents to be integrated in standard circuit simulators. Self and mutual thermal impedances of electronic structures, preliminarily evaluated through accurate 3-D FEM thermal simulation, are directly identified with Time Domain Vector Fitting and synthesised in a lumped PSPICE circuit. Two relevant examples of dynamic electrothermal co-simulation are given, which exhibit significant differences with respect to their isothermal counterparts.**

I. Introduction

Thermal issues are entailing an increasing reduction of performance and reliability in highly-integrated electronic systems [1], [2]. In particular, it is well recognized that overheating adversely impacts also power and signal integrity [3], [4]. As a consequence, the thermal management is becoming crucial, and integrated electrothermal (ET) analyses relying on accurate thermal models are greatly envisaged at any design level and stage.

Generally speaking, the thermal modeling of electronic systems involves different granularity levels, namely, component, chip, package and PCB. Hence, various methods have been proposed to derive efficient multi-scale and multi-source thermal dynamic models of devices and systems. For a system-level ET simulation it is advisable that the considered models are reduced to minimum complexity for a prescribed accuracy, and easily integrated into standard circuit simulation tools. This goal can be pursued by (i) classical order-reduction techniques [5] from the discretized thermal equations [6] or by (ii) applying standard electrical macromodeling techniques, e.g. Vector Fitting (VF) [7], to the identification of the thermal impedance matrix, measured or computed by means of accurate 3-D thermal simulations. In [8], [9], such identification has been succesfully tackled in the frequency domain with the convex formulation introduced in [10], followed by a concretely passive synthesis [11], adapted to the specific purposes of thermal modeling.

The thermal impedances are, however, mainly defined, measured and simulated in the time domain. In this paper we show the application of the Time Domain Vector Fitting (TDVF) [12], [13] to perform a direct identification of thermal impedances, avoiding not strictly necessary and often numerically challenging domain transformation.

As a feasibility demonstration and case study, the proposed strategy is successfully exploited to analyze the impact of ET effects on an interconnect line embedded in a module fabricated in ultra-thin chip stacking technology (UTCS) as well as on the dynamic behavior of a silicon-on-glass (SOG) bipolar current mirror.

II. Time-Domain Vector Fitting for thermal impedance reduced modeling

The concept of *thermal impedance* was introduced to model the dynamic thermal behavior (e.g., under pulse applications) of semiconductor elements (i.e., elementary cells in a complex transistor or chips embedded in a power module) [14]. In particular, the self-heating thermal impedance of a device/chip at a given time instant t is defined as

$$Z_{TH}(t) = \frac{T(t) - T_{AMB}}{P_D} = \frac{\Delta T(t)}{P_D} \tag{1}$$

where T and T_{AMB} are the device/chip and ambient temperatures, respectively, and P_D is the amplitude of the applied power step. The mutual thermal impedance between two devices/chips designated as i-th and j-th is given by

$$Z_{THij}(t) = \frac{T_i(t) - T_{AMB}}{P_{D_j}} = \frac{\Delta T_i(t)}{P_{D_j}} \tag{2}$$

i.e., it represents the temperature rise over ambient of a heat source due to the activation of the other one, normalized to the power dissipated by the latter. It must be remarked that, in spite of the (unfortunate) nomenclature, the mutual impedance must be considered as an indicator of the thermal coupling degree between the devices/chips. The thermal impedance matrix represents a black-box block for a description at the terminals of interest of the thermal problem and can be obtained through a transient 3-D thermal simulation – performed for the case studies with COMSOL Multiphysics [15] with logaritmical time sampling, i.e., $t_k = \theta t_{k-1}$ for some $\theta > 1$.

Let us consider a single temperature rise $\Delta T(t) = Z(t)$ excited by a unit power step $P(t)$, computed at the time instants t_k (we omit for the reminder of this section the subscripts $_{TH}$ and $_{i,j}$ for simplicity). Under linearity and time-invariance assumptions, we can consider the dynamic power-temperature system as described by the frequency (Laplace) domain transfer function $Z(s)$. Our objective is to derive a lumped black-box model $\widetilde{Z}(s)$, here assumed in rational form

$$Z(s) \approx \widetilde{Z}(s) = \sum_{n=1}^{N} \frac{R_n}{s - p_n}, \tag{3}$$

by optimizing poles p_n and residues R_n so that the transient model response matches the original data, $\widetilde{\Delta T}(t_k) \approx \Delta T(t_k)$ when excited by the same unit power step $P(t)$.

The identification of model poles and residues is here performed using a generalized iterative TDVF scheme [12], [13]. We define a set of initial poles q_n^0 at iteration $i = 0$ to be logarithmically distributed along the real negative axis. Then, we write the model (3) in the equivalent form

$$\widetilde{Z}(s) = \frac{\sum_{n=1}^{N} \frac{b_n}{s-q_n^0}}{1+\sum_{n=1}^{N} \frac{c_n}{s-q_n^0}} \tag{4}$$

where the coefficients b_n and c_n are unknown. Considering a Laplace-domain power input $P(s)$, we want to enforce the following condition

$$\Delta T(s) \approx \widetilde{Z}(s) P(s). \tag{5}$$

Multiplying by the model denominator leads to

$$\left\{1+\sum_{n=1}^{N} \frac{c_n}{s-q_n^0}\right\} \Delta T(s) \approx \left\{\sum_{n=1}^{N} \frac{b_n}{s-q_n^0}\right\} P(s) \tag{6}$$

which translates, after converting to time domain and evaluating both sides at the time points t_k, into

$$\Delta T(t_k) + \sum_{n=1}^{N} c_n \Delta T_n(t_k) \approx \sum_{n=1}^{N} b_n P_n(t_k), \tag{7}$$

where

$$\Delta T_n(t) = \int_0^t \Delta T(\tau) e^{q_n^0 (t-\tau)} d\tau, \tag{8}$$

$$P_n(t) = \int_0^t P(\tau) e^{q_n^0 (t-\tau)} d\tau = \frac{e^{q_n^0 t} - 1}{q_n^0}. \tag{9}$$

The numerical evaluation of $\Delta T_n(t_k)$ using the available temperature data is straightforward. Collecting now (7) for all time samples t_k leads to a linear system with unknowns b_n and c_n, which can be easily solved in Least Squares (LS) sense.

As standard in VF and TDVF applications [7], [12], [13], the coefficients c_n are used to find the roots of the model denominator in (4), which are denoted as q_n^1 and used as starting poles for the second iteration $i = 1$. Then, this pole relocation process is iterated until the set q_n^i stabilizes to the dominant poles of the model p_n. Once these poles are known, the residues R_n are computed by solving the LS system having its k-th row

$$\sum_{n=1}^{N} R_n P_n(t_k) \approx \Delta T(t_k), \tag{10}$$

which is obtained by multiplying both sides of (3) by $P(s)$ and converting back to time domain.

The above procedure can be applied to self and mutual thermal impedances, leading to different pole/residue pairs for each element of the thermal impedance matrix. Alternatively, a common pole set can be used for all matrix elements, by forming a pole relocation system (7), which collects all temperature responses at the same time. This approach is standard [12].

III. Case Studies

The approach outlined in Section II was successfully exploited to analyze the impact of dynamic ET effects on a interconnect line in UTCS module as well as of a SOG bipolar current mirror.

A. UTCS module

ET effects play a major role in state-of-the-art ultra-compact systems relying on the vertical integration of thin silicon chips, which are conceived to reduce size and costs for a given performance. This issue is ascribed to the layers needed to electrically insulate the chips (e.g., benzocyclobutene), which – being also good thermal insulators – effectively counteract the heat removal from the power dissipating regions [16], [17]. A well-known consequence of the module heating is the increase of the propagation delay of a digital signal through interconnect lines between chips, due to the thermally-enabled growth in distributed resistance [4].

The identification/synthesis procedure presented in Section II was applied to an UTCS structure containing two chips, the active circuitries of which are connected through tungsten vias and a copper line [9]. An illustrative 3-D view of the active regions and the interconnect scheme is shown in Fig. 1, which details the discretization chosen to describe the copper line from the electrical and thermal viewpoints; in particular, the line was partitioned into 7 elements denoted with letters "a", "b",..., "g".

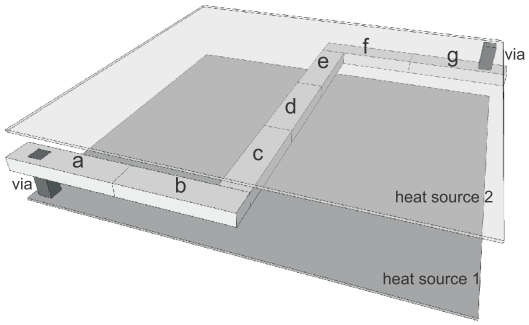

Fig. 1. Representation of the circuitries lying on the chips and of the interconnect scheme.

An extensive ET dynamic analysis of this module was carried out in [9], where the matrix of self-heating and mutual impedances associated to the heat sources embedded in the structure was represented by a generalized multiport Foster topology, whose elements were identified with a technique relying on Vector Fitting and positive fraction convex identification. Here it is demonstrated that the application of the TDVF and the resulting synthesized network allow obtaining results nearby coinciding with those presented in [9]. An ET simulation was performed by assuming that the buried (1^{st}-level) and top (2^{nd}-level) chips dissipate powers P_{D1}=45 W and P_{D2}=15 W over chosen time intervals, as shown in Fig. 2, which also reports the corresponding temperature rises above ambient ΔT_1 and ΔT_2, as well as the time instants t_1, t_2, t_3, t_4 selected as starting points for the ET analysis. Fig. 3 details the temperature increments for the elements of the copper line due to P_{D1} and P_{D2} at the aforementioned instants. The ET impact on the interconnect features was investigated by applying to the line input a digital signal V_{IN} with 1 V amplitude and 1 GHz frequency with 50% duty cycle, and performing ns-long simulations: it has been found that the propagation delay increases of slightly less than 20% due to the line heating [9].

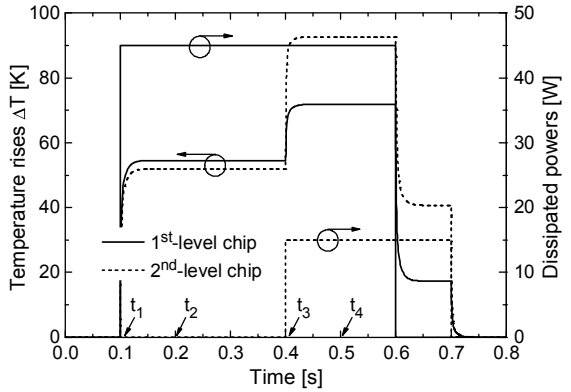

Fig. 2. Dissipated powers and temperature rises over ambient against time for the two stacked active silicon chips.

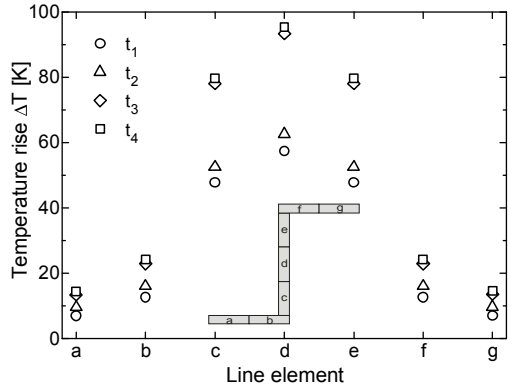

Fig. 3. Temperature rises over ambient at the elements of the interconnect line due to the heat emerging from the dissipating chip circuitries.

B. Current mirror

Current mirrors are commonly recognized as the dominant building blocks in analog ICs. Although these circuits were traditionally used as dc biasing elements, in last decades the analysis of their transient behavior has become crucial in current-mode and mixed-signal applications, where they are subject to large current variations and – if improperly designed – may adversely impact the performance of the entire circuit [18]. In addition, current mirrors are steadily affected by heating issues due to the adoption of low thermal conductivity materials and/or advanced isolation schemes. A comprehensive study of the influence of ET effects on the behavior of bipolar current mirrors fabricated in SOG [19] and GaAs technologies has been presented in [20], although the analysis was limited to the steady-state case. It was demonstrated that severe self-heating of the individual devices may not only lead to a poor mirroring of the reference current I_{REF}, but also to a reduction of the safe operating area of the output transistor induced by the occurrence of a *flyback* phenomenon, i.e., the onset of a negative differential resistance (NDR) branch in the $I_{OUT}-V_{OUT}$ characteristics.

In this work, the analysis is extended to include dynamic conditions by making use of the approach discussed in Section II. A bipolar SOG mirror is considered, a sketch of which is shown in Fig. 4. The input (Q_1) and output (Q_2) transistors are assumed identical; the supply voltage V_{CC} is connected to the Q_2 collector through a load resistance R_L. The current I_{REF} is varied from 0 to an I_{REF1}=0.3 mA value at t=0 s and from I_{REF1} to I_{REF2}=1 mA at t=150 ms.

In this analysis, three combinations of values for the supply voltage and the load resistance will be investigated, namely, V_{CC}=5 V, R_L=500 Ω (case 1), V_{CC}=5 V, R_L=5000 Ω (case 2), and V_{CC}=1 V, R_L=100 Ω (case 3), which will lead to a different thermally-induced behavior. The study was performed by describing Q_1 and Q_2 by PSPICE-compatible macromodels [21], that (i) besides the standard electrodes, are provided by additional "temperature" (input) and "power" (output) terminals, (ii) allow modifying the temperature-sensitive parameters during the simulation run, (iii) account for all relevant physical mechanisms impacting the forward active mode, like impact ionization [22], [23]. The current mirror variant suited for dynamic ET simulations was constructed by connecting the thermal feedback (TF) block including the synthesized network that describes the matrix of thermal impedances to the macromodel-based mirror.

Fig. 5 illustrates the ET steady-state $I_{OUT}-V_{OUT}$ curves corresponding to I_{REF1} and I_{REF2}, which exhibit an S-like shape ascribed to the Q_2 heating. It is fairly clear that an increase in the reference current shrinks the safe operating area of device Q_2 [20]. For a better understanding of the circuit behavior, also the corresponding isothermal (at T=300 K) curves, as well as the load lines (defined by $V_{OUT}=V_{CC}-R_L\cdot I_{OUT}$) associated to cases 1, 2, 3, are represented. The intersections between the load lines and the ET $I_{OUT}-V_{OUT}$ characteristics identify the quiescent operating points of transistor Q_2, which are designated as $A_{1,2,3}$ (I_{REF1}, case 1,2,3), $B_{1,2,3}$ (I_{REF2}, case 1,2,3). An inspection of the figure reveals that in various conditions (A_1, B_1, B_3) the mirroring action is severely degraded by ET effects, since the steady-state current I_{OUT} is much higher than the applied I_{REF}. Conversely, the normal operation of the circuit would be fully restored under isothermal conditions; in this case, the slight discrepancies between I_{OUT} and I_{REF} would be induced by the Early effect only.

Fig. 6 reports the transient I_{OUT} behavior for all the considered cases, which is found to be consistent with the steady-state analysis illustrated in Fig. 5; it is shown that (i) in case 1, I_{OUT} is much larger than the applied I_{REF}, since the load line defines high-current quiescent points well inside the NDR region; (ii) in case 2, the huge R_L counteracts the transistor self-heating, thus restoring low I_{OUT} values (in particular, I_{OUT} at B_2 almost coincides with the current that would be obtained under isothermal conditions); (iii) in case 3, the mirror forces a large I_{OUT} transition due to the sharp slope of the load line, leading to a 25 ms-long response – while the expected rise time should be in the order of ns.

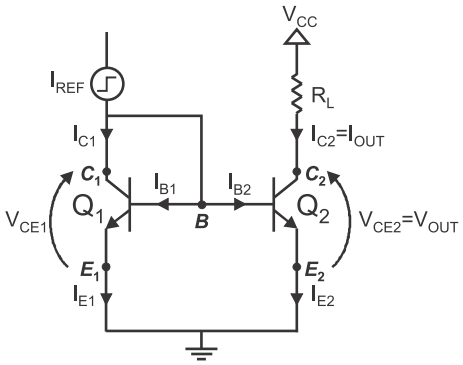

Fig. 4. Sketch of the analyzed bipolar current mirror.

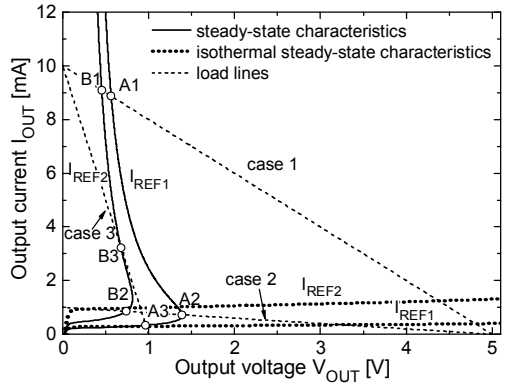

Fig. 5. Steady-state ET (solid lines) and isothermal (dotted) $I_{OUT}-V_{OUT}$ characteristics of transistor Q_2 corresponding to I_{REF1} and I_{REF2}, along with the load lines associated to cases 1, 2, 3 (dashed).

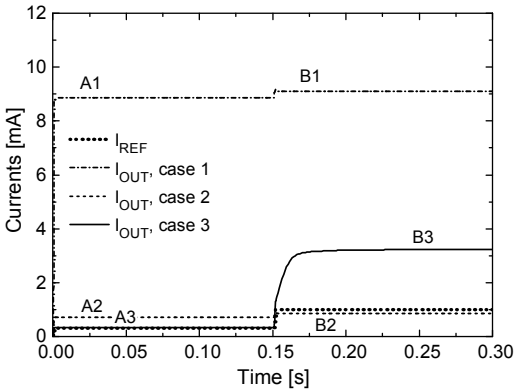

Fig. 6. I_{OUT} against time for all the cases analyzed in this work, along with the applied I_{REF} step; the steady-state conditions corresponding to I_{REF1} and I_{REF2} are labeled as in Fig. 5.

Fig. 7 shows the S-shaped steady-state ΔT_2-V_{OUT} curves corresponding to the $I_{OUT}-V_{OUT}$ characteristics depicted in Fig. 5, as well as the dynamic ΔT_2 trajectories eventually ending in the quiescent points. The highest temperatures – which are expected to lower the device reliability – are reached for case 1 due to the high V_{CC} and the relatively low R_L. It is surprisingly found that the transition $I_{REF1}-I_{REF2}$, despite the increase in I_{OUT}, entails a ΔT_2 *reduction* for cases 1 and 2. This can be explained by considering that points A_1 and A_2 are associated to a higher V_{OUT} in comparison to B_1 and B_2, respectively, which – prevailing over the lower I_{OUT} – give rise to a higher dissipated power. The opposite behavior is detected for case 3 since the load line identifies a much larger current on the I_{REF2} characteristic (B_3) compared to the I_{REF1} one (A_3), while V_{OUT} remains almost unchanged.

IV. Conclusions

In this work we have shown that a direct time domain identification of reduced electrical equivalents for thermal impedances can be successfully pursued, obtaining a compact thermal feedback dynamic network well suited to perform electrothermal co-simulation in a SPICE-like environment. The proposed technique relies on the Time Domain Vector Fitting, which reveals effective in identifying a logarithmically time sampled thermal impedance matrix. Electrothermal dynamic analyses have been performed for an interconnect line embedded in a ultra-thin-chip-stacked module and a silicon-on-glass current mirror, showing respectively a thermally-induced (i) delay degradation, and (ii) current mirroring mismatch and much slower response.

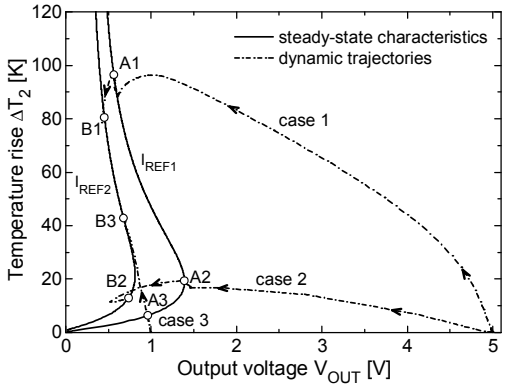

Fig. 7. Steady-state ET ΔT_2-V_{OUT} characteristics associated to I_{REF1} and I_{REF2} (solid lines), along with the dynamic temperature trajectories for cases 1, 2, 3 (dashed).

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