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Tesi di Dottorato

Realization of superconducting quantum devices based on tunnel Josephson junctions by micro and nanofabrication techniques

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A Edoardo e Enrico
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Summary

The aim of this thesis is the realization of superconducting quantum devices based on overdamped Nb/Al-AlO_x/Nb SNIS (Superconductor - Normal metal - Insulator - Superconductor) tunneling Josephson junctions, interesting for several application fields (voltage metrology, digital electronics, radiation sensors, nanoSQUID, etc.). The challenges faced by quantum electronics and metrology are directing the new generations of devices towards smaller dimensions and higher levels of integration. Taking into account this requirement, SNIS-based prototypes have been realized exploiting the thin film technology, to guarantee a good control of electrical parameters of junctions, a higher reproducibility of their current-voltage response, and increasingly their dimension control.

The main objective of this experimental activity was addressed on downscaling the junction dimensions from the micro to the nanoscale exploiting three different lithographic techniques: the optical lithography to realize SNISs with a micrometer resolution, the Electron Beam Lithography (EBL) at the subμm and, finally, exploiting a recently purposed mesoscopic tunnel junction nanofabrication technique concerning the Focused gallium Ion Beam (FIB) present at Nanofacility Piemonte Laboratory, at National Institute for Metrological Research (INRIM) in Torino (Italy).

The first introductory Chapter starts with a brief essay of superconductivity and the Josephson effect, with the main relations describing this quantum effect, followed by some notions in Chapter 2, concerning the Josephson junction as quantum physical system, and its main typologies.

The Chapter 3 is focused on the SNIS Josephson junction, an innovative junction recently implemented and studied at INRIM representing a valid alternative to the other technologies for different applications.

The Chapter 4 describes the main thin film techniques employed to perform the Nb/Al-AlO_x/Nb-based devices under investigation in this thesis, and focusing on deposition, patterning and etching processes.

The Chapter 5 reports the multi-step fabrication process studied and implemented at INRIM to realize superconducting quantum devices based on SNIS junctions, wherein the area is patterned by optical lithography, at the micrometer scale.

The Chapter 6 details the experimental results relating to the realization and

the electrical characterization of a binary-divided array based on 8192 overdamped SNIS junctions for a 1 V programmable Josephson Voltage Standard. A metrological introduction concerning the state of the art of the Josephson Voltage Standard is also reported.

The Chapter 7 reports experimental results concerning SNIS junctions fabricated in the sub micrometer scale exploiting the Electron Beam Lithography (EBL), as nanolithographic technique to define the effective area of junctions, focusing on the optimization of the EBL and reactive ion etching processes for the process validation.

Finally, the Chapter 8 details the recent work concerning the employment of an innovative three-dimensional Focused Ion Beam (3D FIB)-based nano machining to fabricate SNIS junctions on a deep sub micrometer scale, with a higher resolution compared to resist-based processes previously used. The fabrication process and the electrical characterization of a nano SNIS junction prototype is reported.

The further appendix (Appendix A) reports a review of the measurement facilities used either for DC or RF characterization, in cryogenic ambient at liquid helium temperature of 4.2 K, of the SNIS- based devices. A collection of process recipes (Appendix B) and technical instrumentations (Appendix C) is also presented.

Contents

Part I

Theory

Chapter 1

Superconductivity and Josephson effect

1.1 Normal metal conduction

The motion of electrons in solids is at the base of a lot of phenomena such as thermal and electrical conductivity. The electrical conduction in metals was first described from a macroscopic point of view by the Ohm's law $V = R \cdot I$ (where V is the potential difference measured across the conductor in units of volts, R the resistance of the conductor in units of ohms, and I the current through the conductor in units of amperes).

An electron moving in a metal with a perfect lattice can be represented by a plane wave that moves in the same direction. This wave can pass through this perfect periodic structure without any diffusion because it is a stationary solution of Schrödinger equation describing the undisturbed propagation of electrons through crystal lattice.

A consequence of this mechanism is that in a perfect metal electron current will not encounter any resistance at $T = 0$ K. Anyway two effects can break the perfect periodicity of the lattice:

1) For $T > 0$ K atoms move themselves from their equilibrium position;

2) atoms of other elements (impurities) or other defects (dislocations) can be present inside the metal.

Consequently the resistance in a metal can be written as the contribution of two terms:

$$R(T) = R_0 + R_{ph}(T) \tag{1.1}$$

where R_0 is the contribution of the imperfections of the lattice and $R_{ph}(T)$ represents the contribution of thermal agitation.

1.2 The theory of the superconductivity

The discovery of superconductivity starts at the beginning of 20th century from studies of the resistance of metals as function of temperature and material purity.

In 1911 Kamerlingh Onnes, studying the changing of the resistance of Hg with the temperature, found that the value of R below 4 K fall down very quickly till a non-measurable value [1]. This drop happened in a very narrow temperature range and it appeared to be independent from materials purity. It was obvious that the sample was in a new state not yet known, characterized by zero electrical resistance. This phenomenon took the name of superconductivity (Figure 1.1).

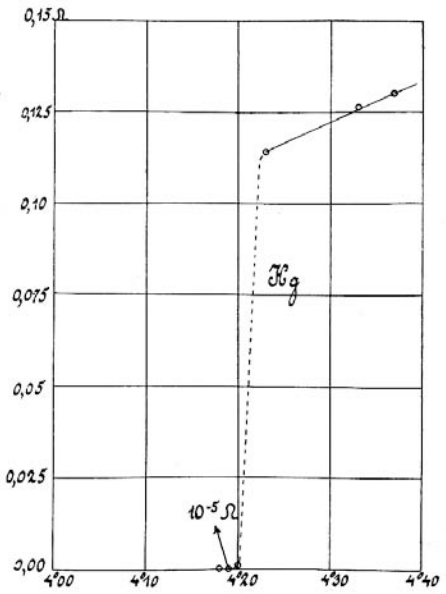

Figure 1.1. The historic plot of resistance (Ω) versus temperature (K) for mercury from the 26 October 1911 experiment shows the superconducting transition at 4.20 K.

In the following years the same behaviour was observed in many other materials at different temperatures. The transition temperature from a normal state to a superconductive one is called critical temperature T_c. Later was discovered that the superconductivity could have been destroyed not only by a temperature increase above T_c but also by a magnetic field. The value of the magnetic field needed to destroy the superconductivity for a specific material is called critical field H_c. More rapid development of superconductivity started in 1933 when Meissner and Ochsenfeld [2] discovered that a superconductor cooled below its critical temperature would expel the magnetic field. This discovery was quickly followed by the two fluids model of Gorter and Casimir [3] and electromagnetic theories of the London brothers [4]. Subsequent improvements in describing the phenomenology of the

superconducting state were achieved by Ginzburg and Landau [5] and by Pippard [6]. In contrast to the quick advancing in a macroscopic model, the setting up of a microscopic theory was slow. The first indications that the electron-phonon interaction was responsible for superconductivity came as late as 1950 with Frohlich's [7] model and with the discovery of the isotope effect [8,9]. It took a few years to find a satisfactory mathematical solution and in 1957 Bardeen, Cooper and Schrieffer succeded in formulating a theory (known as BCS Theory) which was capable of explaining a surprising number of experimental results [10].

BCS theory states that the interaction between electrons and phonons produces a weak attraction between electrons which is sufficient to bound them in pairs in some materials and, if the temperature is low enough, despite the electrostatic repulsion due to their charge. All electron pairs, called Cooper pairs, are condensed into the same state, the superconducting ground state, and their collective degrees of freedom are described by a single quantum mechanical wave function. So a collective motion can be described. The energy needed to break a pair into two single quasi-particles (single excitation above the ground state) is the minimum threshold energy Δ, called "energy gap".

An important contribution to the development of a microscopic theory for superconductors came in 1956 from Cooper [11] who recognized that the ground state ($T = 0$ K) of an electron gas is unstable if one adds a weak attractive interaction between each pair of electrons. The qualitative idea is that an electron, moving into a positively charged ion lattice, owing to its negative charge, distorts the latter and leaves a deformation trail behind, affecting the position of positive ion cores in the crystalline lattice. This trail is associated to an increased density of positive charges and thus an attractive effect on another electron. The lattice deformation causes, therefore, a weak attraction between pair of electrons called Cooper Pair, but this attractive electron-electron interaction is slower than the instantaneous Coulomb repulsion between the electrons, because of the slow motion of the massive ions. The lattice deformation reaches its maximum elongation at a distance from the first electron, which can be estimated from the electron velocity (Fermi velocity $\nu_F \approx 10^8$ cm/s) and the phonon vibration period ($\approx 10^{-13}$ s).

As a consequence, the characteristic length scale of this interaction within a Cooper pair is given by the coherence length $\xi_0 = \frac{\hbar \nu_F}{\pi \triangle}$, being $\triangle$ the superconducting energy gap. This length is about 100 nm and it is the size of the Cooper pair (Figure 1.2); typically it is much larger than interatomic distance of the lattice, showing the strong overlap of the Cooper pairs in the superconductor. It is evident that the long interaction range of the two correlated electrons is the reason why the Coulomb repulsion is insignificant, being screened out over distances of just few Angstroms.

The lattice deformation can be understood thinking of electrons, which continuously emit and absorb phonons interacting with the lattice: the phonons constituting

such a lattice deformation are "virtual" phonons, only existing for an interval of time defined by the uncertainty relation and after they must be absorbed. Obviously, the attractive interaction due to the lattice deformation is appreciable only at temperatures near 0 K, since its effect can be negligible compared to the thermal vibrations.

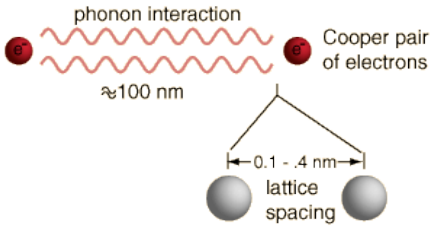

Figure 1.2. Two electrons, forming a Cooper pair, are locked together by phonon exchange.

1.2.1 Superconductors properties

The temperature at which the resistance of a superconductor goes to zero is called also transition temperature and it is typical for each metal or alloy. In general, this temperature is not sensitive to small amounts of impurity, though magnetic impurities can lower the T_c. Since the transition is influenced by the specimen composition, it is very sharp for very pure and physically perfects crystals. Even when the transition is spread over a large temperatures range (a lot of impurities in the material) the resistance still seems to disappear completely below a certain temperature.

Since the measurement of zero resistance values could be rather difficult if not impossible due to the sensitivity and detectability of experimental set-up, a sensitive test was proposed by Gallop, to verify this special electrical regime, measuring the current decay in a superconducting ring after a long time. Supposing the self inductance of the ring is L, and current $I(0)$ at time $t = 0$; at a later time t the current results:

$$I(t) = I(0)e^{-(R/L)t} \tag{1.2}$$

where R is the resistance of the ring. Measuring the magnetic field generated by the current flowing in the ring it is possible to observe how the current decays over time in an insulated system. Gallop measurements showed that the resistivity of the superconducting metal was less than 10^{-26} Ω·cm. This allows to consider the resistance of a superconductor as a zero resistance.

A further distinctive feature for superconductors is the magnetic behaviour: a

magnetic field applied to a superconductor cannot penetrate into it during its transition to the superconducting state. This phenomenon was discovered in 1933 by two German physicists, and indeed, it is well-known as Meissner-Ochsenfeld effect [2]. It implied that inside a superconductor an external magnetic field had to be completely compensated by the field generated by (super) currents in a layer at the surface. The experiment demonstrated for the first time that superconductor is not only a perfect conductor; it is above all a perfect diamagnetic (Figure 1.3).

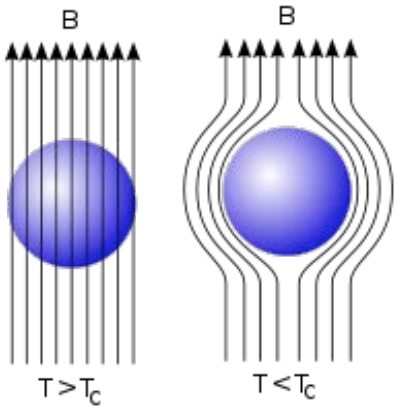

Figure 1.3. The Meissner effect: a superconducting material brought into magnetic field $H \ll H_c(0)$ while in the normal state, then cooled through T_c (H). At the transition to the superconducting state the magnetic field is spontaneously expelled.

This unexpected effect provided the first evidence that classical electromagnetism was insufficient for explaining the superconductivity, and is consistent with the fact that superconductivity is a real thermodynamic state of matter. The effect of the magnetic field can be described in a relatively simple way for a class of superconductors called Type I. Its value in function of the temperature is given by the empiric formula:

$$H_c = H_c(0)[1 - (T/T_c)^2] \tag{1.3}$$

and can be plotted as in Figure 1.4. This curve can be looked upon as representing a boundary between a superconducting and a normal phase of the material.

1.3 The Josephson effect

In 1962 Brian Josephson published a theoretical paper [12] predicting the existence of another effect, the so called Josephson effect, involving superconductors. He

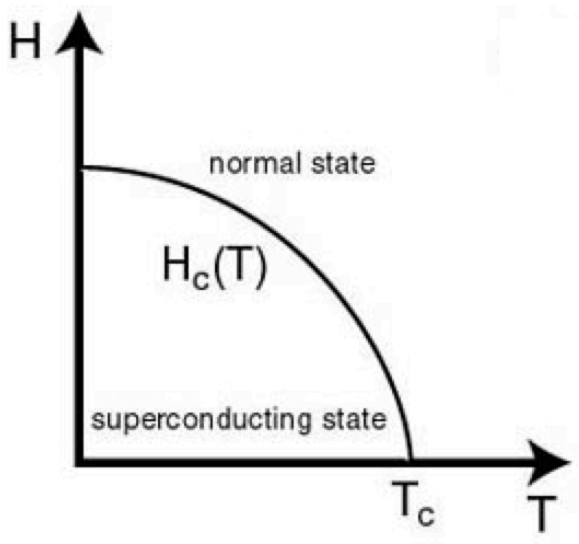

Figure 1.4. H versus T for superconductors of Type I.

asserted that Cooper pairs could tunnel lossless through the barrier in a superconducting tunnel junction (namely the Josephson junction). Their tunneling current or supercurrent I_s depends upon the phase difference between the two quantum mechanical wave functions describing the collective motion in the two superconductors:

$$I_s = I_c sin\varphi \tag{1.4}$$

where I_c is the maximum zero-voltage current which can flow through the junction (the so called "critical current") and φ is the phase difference. The maximum value of the I_s occurs when there is a phase difference of $\pi/2$ and then is equal the critical current I_c of the gap. In its simplest form, the Josephson effect claims that if the tunneling barrier is sufficiently thin, up to a certain current ($I < I_c$), the voltage across the junction is zero. The Equation 1.4 represents the DC Josephson effect.

If the current I in a superconductor exceeds the critical value I_c a finite potential drop V occurs across the barrier, the phase difference varies in time as follows:

$$\frac{d\varphi}{dt} = \frac{2eV}{\hbar} \tag{1.5}$$

where e is the elementary charge, $\hbar = h/2\pi$ the Dirac constant, and h the Planck constant.

Equation 1.5, representing the AC Josephson effect, is a first order differential equation with separable variables and, if the voltage is constant at the value V_0, it can be integrated and substituted in Equation 1.4. The result is that the Josephson current oscillates at the Josephson frequency:

$$f_J = \frac{2eV_0}{h} \tag{1.6}$$

First observations of the Josephson effect were verified by Anderson and Rowell [13], Shapiro [14], Tien and Gordon [15] in 1963, and Anderson and Dayem [16] in 1964, and soon became clear that the Josephson effect exists not only in tunnel junctions, but also in other systems so-called weak links, small sections of superconducting circuits wherein the critical current is suppressed.

Chapter 2

The Josephson junction

2.1 Introduction

The Josephson effect (Section 1.3) mainly occurs in a Josephson junction, namely a physical device wherein two superconducting electrodes are "weakly" connected through a tunneling barrier. Furthermore, this phenomenon could arise in a variety of other structures, like a superconducting film with a constriction or a point contact can behave as a tunnel junction, as well.

In the last decades, many typologies of Josephson junction have been developed, and, in the simplest cases, it is realized by sandwiching the two superconducting electrodes with an insulating barrier, forming a stacked structure like Superconductor - Insulator - Superconductor, called SIS junction, or with a normal metal (N) barrier in a Superconductor - Normal metal - Superconductor, called SNS junction. A general representation of a Josephson junction is reported in Figure 2.1.

2.2 Current - Voltage *I-V* characteristic

Analysing the current - voltage I-V characteristic of different Josephson devices, a great variety of behaviours are observed. Tunneling Josephson junction can, for example, exhibit current-voltage responses markedly hysteretic: there are two voltage states ($V = 0$ and $V \neq 0$) for current values lower than the maximum critical current I_c. In point contact or bridges structures, I-V curves are usually single-valued, at least for temperatures not too far from the critical one.

Many of the features of the I-V curves of the weak links can be described in terms of a simple circuit model, wherein the distributed capacitance and the quasi-particle conductance of the device are considered as lumped elements in parallel with a non linear Josephson element.

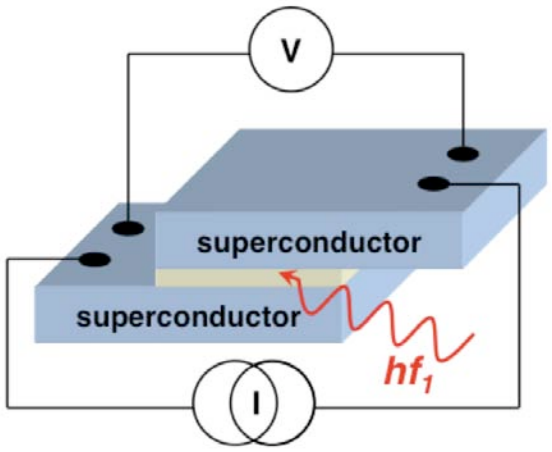

Figure 2.1. A schematic representation of a Josephson junction.

Following the Resistively Shunted Junction Model, RSJ of McCumber [17], Stewart [18] and Johson [19], it is possible to represent a weak link by a simple equival circuit, where the Josephson junction is considered as a circuit composed by a Josephson bipole (a junction in which only the supercurrent I_s can flow) and a resistor connected in parallel. The resistor constitutes a simplified model of the electrical conduction processes into a junction with dissipation (electron tunneling, etc.). A schematization of the RSJ bipole is shown in Figure 2.2.

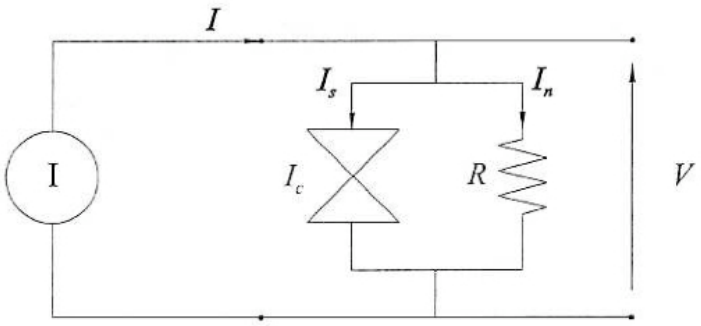

Figure 2.2. RSJ generalized bipole with current biasing, representing a model for a Josephson junction.

The total current I in the bipole, it whose leads a voltage V is present, is given by:

$$I = I_s + I_n = I_c sin\theta(t) + \frac{V(t)}{R} \tag{2.1}$$

and being the voltage across the junction

$$V = \frac{\hbar}{2e}\frac{d\theta(t)}{dt} \tag{2.2}$$

The first equation can be written in the form:

$$I = I_c sin\theta(t) + \frac{\hbar}{2eR}\frac{d\theta(t)}{dt} \tag{2.3}$$

Dividing by I_c, and being this model characterized by a parameter representing the characteristic frequency f_c

$$f_c = \frac{2e}{h}RI_c \tag{2.4}$$

the Equation 2.3 becomes

$$\frac{I}{I_c} = sin\theta(t) + \frac{1}{2\pi f_c}\frac{d\theta}{dt} \tag{2.5}$$

Analysing this Equation, if $|I| \leq I_c$ the possible solution is $\mathrm{d}\theta/\mathrm{d}t = 0$ that means θ constant and $V = 0$.

For $|I| \geq I_c$ the Equation admits a solution $\theta = \theta(\mathrm{t})$ and also the V across the junction varies in time. The I-V characteristic is well described by this model, since for bias current below I_c and zero voltage drop, while for higher values, an oscillating voltage $V(\mathrm{t})$ appears. The mean value of the voltage can be calculated:

$$< V(t) >= RI_c\sqrt{(I/I_c)^2 - 1} \tag{2.6}$$

This is the I-V characteristic of the simplified RSJ model and is represented in Figure 2.3, where for $|I| \gg I_c$, $\langle V(t)\rangle \approx RI$ so, while the current in the resistor I_n increases, the supercurrent remains limited $|I_s| \leq I_c$.

2.3 Shapiro's steps in the RSJ model

When a high frequency bias is also fed, the current is $I = I_{dc} + I_{rf}\ \sin(\omega_{rf}\ t)$ and Equations 2.2 and 2.3 do not admit analytical solutions. Numerical methods can, anyway, be used. Quantized voltage steps appear in the DC I-V characteristic (Figure 2.4), called Shapiro's steps [14]. The amplitude ΔI of the steps for the RSJ model is a function of the signal amplitude V_{rf} and of its frequency ω_{rf}. This dependance is more complex than that seen in Section 2.2:

$$\Delta I_n = 2I_c|J_n\left(\frac{2eV_{rf}}{\hbar\omega_{rf}}\right)| \tag{2.7}$$

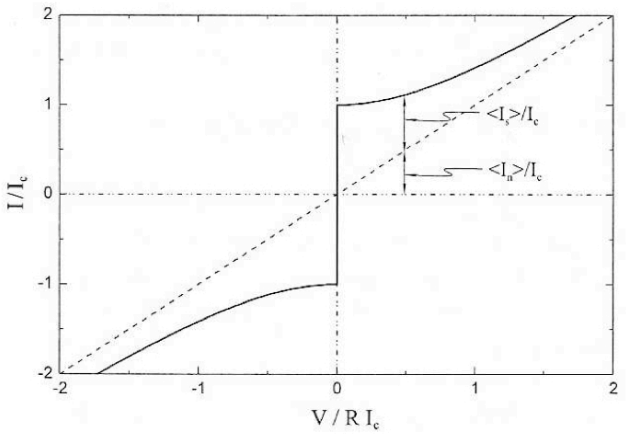

Figure 2.3. RSJ I-V characteristic. On the axis normalized quantities are reported. ⟨Is⟩ and ⟨In⟩ are the currents in the Josephson dipole and in the resistor, respectively.

where J_n is the first kind n-th order Bessel function. The corresponding voltage steps are:

$$V = k\frac{h}{2e}f_{rf} \tag{2.8}$$

with k {±1,2,3,...}.

In particular, the step amplitude reaches its optimum value when $f_{rf} \simeq f_c$. Figure 2.4 shows the I-V characteristic for a junction with $I_c = 0.1$ mA and $R = 0.414\ \Omega$ having, following the Equation 1.6, a characteristic frequency $f_c = 20$ GHz. Curves (2) and (3) represent the steps for $n = \pm 1$ with a step amplitude ΔI maximized in function of the amplitude I_{rf} of the bias power at 20 and 5 GHz, respectively.

2.4 Generalized RSJ model

The generalized RSJ model introduces also a capacitance in parallel to the previous model (Figure 2.5).

The equations of the RSJ generalized bipole are:

$$I = I_c sin\theta(t) + \frac{V(t)}{R} + C\frac{dV(t)}{dt} \tag{2.9}$$

$$V = \frac{\hbar}{2e}\frac{d\theta(t)}{dt} \tag{2.10}$$

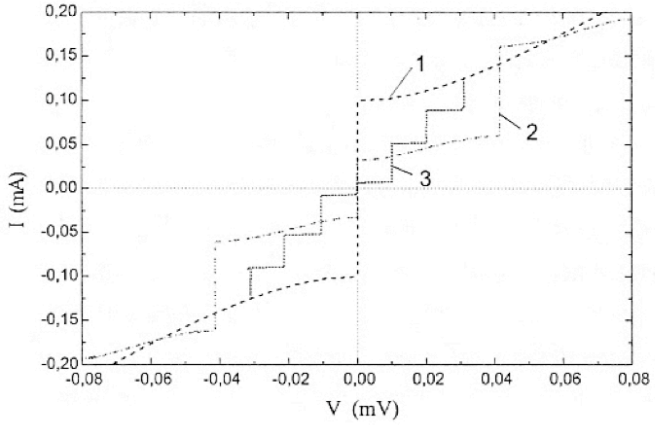

Figure 2.4. Shapiro's steps in the I-V RSJ characteristics. Dashed curve (1) represents the I-V characteristic in absence of RF power. Curve (2), the I-V characteristic for a junction fed with a sinusoidal current with $f_{rf} = 20$GHz, with $f_{rf} = f_c$, while curve (3), $f_{rf} = 5$GHz, when $f_{rf} = f_c/4$.

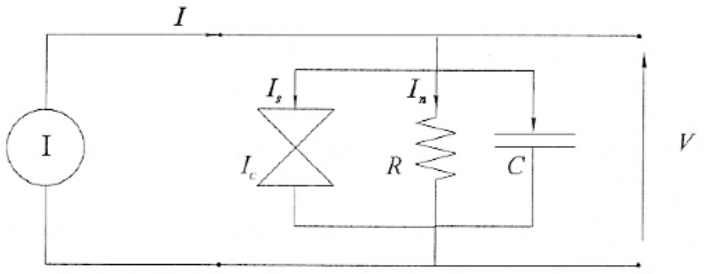

Figure 2.5. RSJ generalized bipole with current biasing.

The first equation can be rewritten as follows:

$$\frac{\hbar C}{2eI_c}\frac{d^2\theta(t)}{dt^2} + \frac{\hbar}{2eRI_c}\frac{d\theta(t)}{dt}sin\theta(t) = \frac{I}{I_c} \tag{2.11}$$

which is the complete equation of the pendulum. Now, making the variable change:

$$t \rightarrow \frac{\hbar}{2eRI_c}\tau = \tau_c\tau \tag{2.12}$$

where $\omega_c = 1/\tau_c$ is the critical pulsation of the system, the following equation is obtained:

$$\beta_c \frac{d^2\theta(t)}{d\tau^2} + \frac{d\theta(t)}{dt} + sin\theta(t) = \frac{I}{I_c} \tag{2.13}$$

This model is characterized by the parameter $f_c = \omega/2\pi$, characteristic frequency of the generalized RSJ model for a Josephson junction, and by the new parameter:

$$\beta_c = \frac{2eI_cR^2C}{\hbar} = \omega_c RC \tag{2.14}$$

that describes the hysteresis present in the real I-V characteristic of the junction.

From Equation 2.14 different conditions arise with respect to β_c:

- $\beta_c \ll 1$: *high damping junction*. In this case the intrinsic capacitance C of the junction is low, so there is a low capacitive coupling between the junction electrodes (high ω_c). Then Equation 2.13 reduces to Equation 2.5 and the I-V characteristic is the one in Figure 2.3 described by Equation 2.6. This behaviour is typical for SNS junctions, defined as *overdamped* junctions.

- $\beta_c \geq 1$: *low damping junction*. The I-V characteristic can only be calculated numerically. In Figure 2.6 the characteristic of a junction with $I_c = 0.1$ mA, $R = 0.414\ \Omega$ and $\beta_c = 10$ is reported. On the other hand, this behaviour is typical for SIS junctions, called *underdamped* junctions.

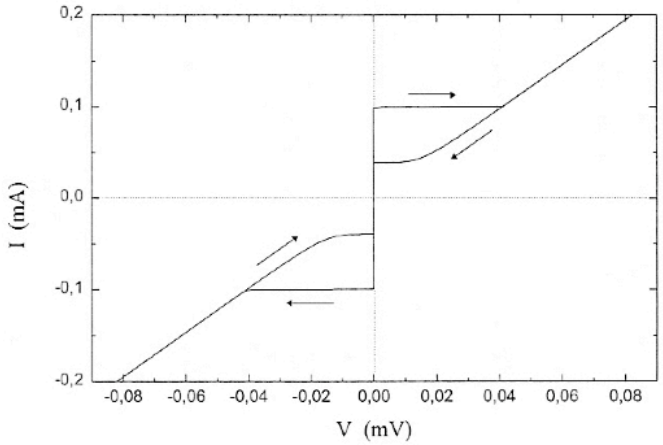

Figure 2.6. I-V characteistic for the generalized RSJ model with βc = 10.

The presence of hysteresis in the case $\beta_c \geq 1$ is noticeable. Therefore, some voltage values are obtained in correspondence of two distinct values of the bias current. This feature is observed in practice, so RSJ generalized model better describes the junction behavior.

2.5 Critical current and magnetic field

It can be seen that the maximum critical current ${I_c}^{max}$ flowing into the junction depends on the external applied magnetic field. In fact, supposed that the insulating layer laying on the (x,y) plane, if a constant magnetic induction field $B(0,B_y,0)$ is applied on the y direction, the relation between the phase difference θ of the two wave functions and the magnetic field is:

$$\frac{\partial\theta}{\partial x} = \frac{2e}{\hbar} B_y d \tag{2.15}$$

with $d = \lambda_1 + \lambda_2 + s$, where λ_1 and λ_2 are the two London penetrations, s is the barrier width and d is the magnetic penetration of the junction. The presence of the magnetic field causes a point to point variation of the phase difference inside the barrier with the relation:

$$\theta(x) = \int_0^x \frac{\partial\theta(p)}{\partial p} dp = \frac{2e}{\hbar} B_y dx + \theta_0 \tag{2.16}$$

As a consequence, the phase difference θ is not uniform on the junction area, so the supercurrent density is also not uniform; it is represented by the equation:

$$J(x) = J_c sin\left(\frac{2e}{\hbar} B_y dx + \theta_0\right) \tag{2.17}$$

and it is modulated by the field B. Because of the periodic nature of this relation, the supercurrent density can be null in some point of the junction and can change sign in others.

The total current I_s which crosses the junction is obtained integrating this current density on the junction area:

$$I_s = I_c^{max}(\Phi)\, sin\theta_0 \tag{2.18}$$

in which:

$$I_c^{max}(\Phi) = I_c(0)\left|\frac{sin(\pi\Phi_e/\Phi_0)}{\pi\Phi_e/\Phi_0}\right| \tag{2.19}$$

$\Phi_0 = h/2e \sim 2.068 \cdot 10^{-15}$ Wb is the flux quantum, $\Phi_e = LdB_y$ is the flux of the magnetic field in the junction barrier and $I_c(0) = wLJ_c$ (L and w are the junction dimensions). So the maximum supercurrent ${I_c}^{max}$ flowing into the junction, as function of the magnetic flux into the barrier, is zero when $\Phi_e/\ \Phi_0 = k$ with $k =$ 0,1,2,..., that is when the magnetic flux into the junction is an integer multiple of the flux quantum as shown in the experimental curve in Figure 2.7.

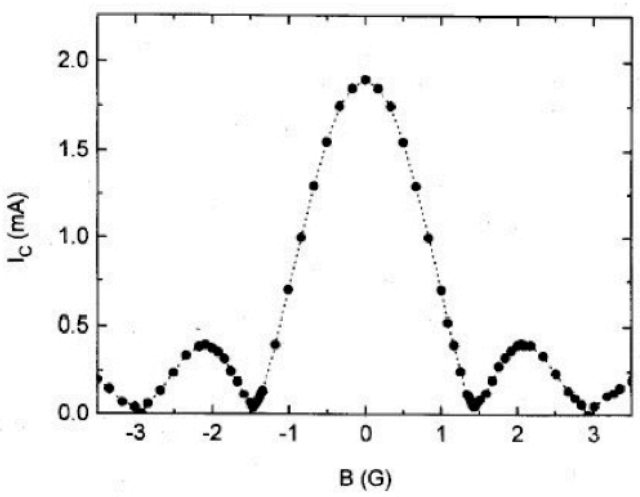

Figure 2.7. Magnetic field pattern of a Josephson junction at 4.2 K.

2.6 Main Josephson junctions and their applications

There are different typologies of junctions wherein the Josephson effect occurs, thanks to the weak interaction between superconducting electrodes: tunneling barrier junction, Notarys bridge, Dayem constriction, point contact junction, ion implantation bridge, proximity effect bridge, and so on. Tunneling barrier junctions are considered to realize complex devices, and the nature of the barrier (oxide, metal or semiconductor) determines the I-V response, and as a consequence, their application field.

As already mentioned (Section 2.4), there are two main families of tunneling Josephson junctions:

- Superconductor - Normal metal - Superconductor, SNS, or *overdamped* junction, linked to a non- hysteretic I-V behaviour (Figure 2.8 left)

- Superconductor - Insulator - Superconductor, SIS, or *underdamped* junction, linked to a typical hysteretic I-V behaviour (Figure 2.8 right)

and the main electrical parameters of a Josephson junction are the critical current I_c (and the related current density, J_c) and the characteristic voltage V_c ($V_c = I_c \cdot R_n$, being R_n the normal resistance of the junction).

Nowadays, these systems find their main application in voltage metrological

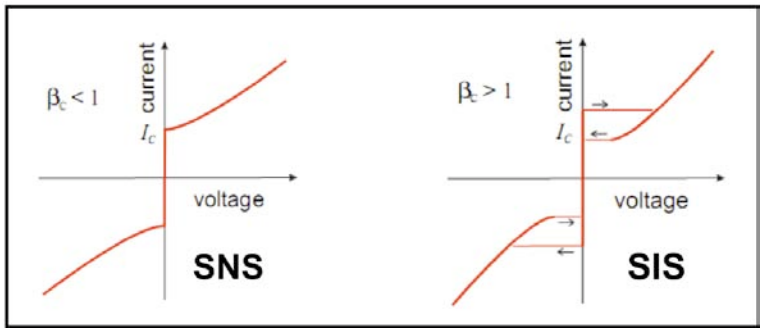

Figure 2.8. DC I-V characteristics for SNS (left) and SIS (right) junctions.

and digital electronics fields. In particular, SIS junction is employed in conventional DC Josephson Voltage Standards (JVS) systems and fabricated with planar $Nb/Al_2O_3/Nb$ thin-film structures, while overdamped Nb/Al/Nb SNS junction is widely studied and a great variety of junctions have been realized for AC JVSs.

Fortunately, significant improvements have been made in both the materials and fabrication techniques of Josephson junctions so that uniform arrays of damped, non-hysteric junctions ($\beta_c < 1$) can now be produced. Single-valued and intrinsically stable electrical characteristics were originally achieved with SIS junctions by externally shunting them with thin-film resistors. The most common method today for producing stable junctions for voltage standards is to fabricate intrinsically shunted junctions by use of a normal metal in the junction barrier, as in SNS or in another typology developed at the Physikalisch-Technische Bundesanstalt (PTB), namely Superconductor - Insulator - Normal metal - Insulator - Superconductor (SINIS) junctions [20]- [23], which consist of a multilayer of $Nb/Al/AlO_x/Al/AlO_x/Al/Nb$ [22], [24]. The insulating barriers for these junctions have significantly larger capacitance as compared to the negligible capacitance of SNS junctions, so that the SINIS junctions are critically damped with a unity McCumber parameter ($\beta_c \simeq 1$) and have non-hysteretic intrinsically stable I-V curves.

In the last years, at INRIM, another type of overdamped junction has been developed. This junction is structurally considered as an intermediate state between SIS and SNS, with a Superconductor - Normal metal - Insulator - Superconductor (SNIS) multilayer of $Nb/Al\text{-}AlO_x/Nb$.

This Josephson junction will be extensively explained in the following, since SNIS represents the elemenary cell of all the superconducting quantum devices studied and realized in this dissertation.

Part II

The SNIS Josephson junction

Chapter 3

The Nb/Al-AlO$_x$/Nb SNIS junction

3.1 The structure of the Nb/Al-AlO$_x$/Nb SNIS junction

The SNIS junction is a four-layered structure, wherein both underdamped and overdamped states can be achieved. Its multilayer structure derives from the trilayer process described by Gurvitch et al. in 1983 [25]. Developed during the 1980's, the Nb/Al technology has several advantages:

- Sputtering of the thin-film sandwich that forms all the junctions can be performed without breaking the vacuum.
- This ensures very clean interfaces and allows oxidation of an extremely thin and homogeneous insulating junction barrier.
- Using Nb, the junctions are mechanically and chemically stable. This was not the case with the lead-alloy junctions used earlier. As a result, no aging of the Josephson arrays is observed.
- Since the critical temperature of Nb is 9 K, the circuit can be operated in liquid helium at a temperature of 4.2 K. At a temperature of half the critical temperature, all the superconducting parameters have approached their $T = 0$ value [26].

In the SNIS junction, the tunneling barrier is represented by a thick aluminum layer opportunely oxidised, postponed between two niobium superconducting electrodes, called "base" electrode and, at the top, the "counter" one, according to the layered sequence Nb/Al-AlO$_x$/Nb (Figure 3.1). In this specific case the aluminum thickness

is usually ranging since 30 to 100 nm, one order of magnitude larger than the value used for the standard hysteretic SIS junctions, as well as the transparency of the AlO$_x$ [27,28]. Because of this thick Al film, which is a normal metal (N) at the liquid helium temperature, these devices could be better described as Superconductor - Normal metal - Insulator - Superconductor (SNIS) junctions.

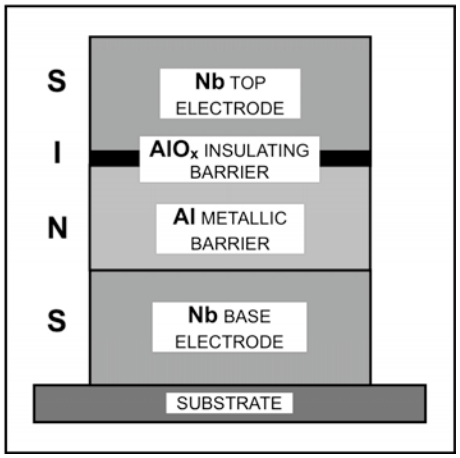

Figure 3.1. The structure of the Nb/Al-AlO$_x$/Nb SNIS Josephson junction.

3.2 The properties of the Nb/Al-AlO$_x$/Nb SNIS junction

The SNIS junctions, arising from Nb/Al SNS (Superconductor - Normal metal - Superconductor) junctions [20], achieve the overdamped state at 4.2 K [29], because of the presence of a very thin oxide layer and a thick normal metal. This response can be also obtained by changing the operating temperature of the junction. Moreover, SNIS junctions exhibit a wide range of electrical parameters at liquid helium temperature, such as current densities, J_c ranging from 10^3 to 10^5 A/cm^2 and characteristic voltage, V_c ($I_c \cdot R_n$, being R_n the normal resistance of the junction) up to 0.7 mV [30]. The combination of these properties makes the SNIS junctions extremely appealing for digital applications [31] and for programmable voltage standard [32].

3.2.1 Hysteretic to non-hysteretic behaviour

Differently from other SIS or SNS devices, SNIS junctions can switch between a hysteretic and a non-hysteretic regime in the I-V response. This behaviour can

be induced either by varying a fabrication parameter or by changing the junction operating temperature [30]. However, these junctions become overdamped and show nonhysteretic I-V characteristics when the Al oxide is sufficiently thin. This is obtained by keeping the oxidation exposure E, defined as the oxygen gas pressure times the oxidation time, below 500 Pa · s. In particular, reproducible overdamped junctions with hysteresis at 4.2 K ranging from 0 to a few % were fabricated for Al = 30 – 100 nm and E ranging between 100 and 500 Pa · s, with the best results being obtained at 150 – 300 Pa · s (Figure 3.2).

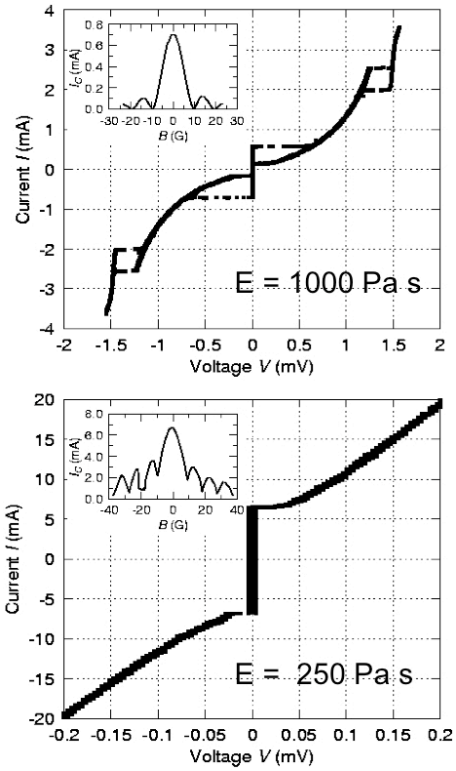

Figure 3.2. The transition from hysteretic to a non-hysteretic behaviour by changing the fabrication parameters, i.e. the oxidation exposure, E.

Fixing the aluminum thickness and the exposure dose for the tunneling barrier, the same transition could be also observed simply by varying the junction operating temperature T, below 4.2 K during the electrical measurement (Figure 3.3), [30].

3.2.2 Temperature dependence

These junctions have been characterised by measuring the I-V characteristics in a wide temperature range both in DC and supplying a RF signal, and also by

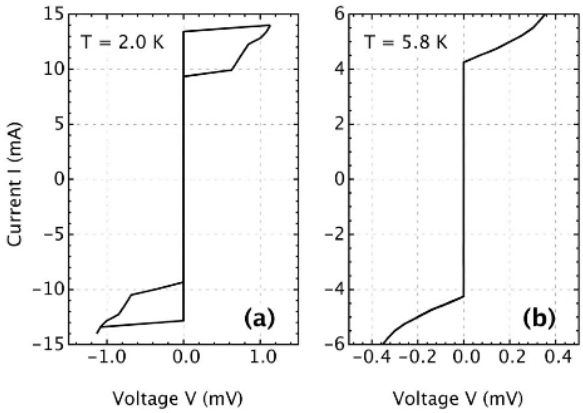

Figure 3.3. I-V characteristics of the same Nb/Al–AlO$_x$/Nb junction at two different operating temperatures: (a) hysteretic I-V characteristic at $T = 2.0$ K, (b) completely non-hysteretic I-V characteristic at $T = 5.8$ K.

measuring their magnetic field pattern at 4.2 K. High values of J_c up to 75 kA/cm^2 and V_c up to 0.7 mV at 4.2 K have been routinely measured.

In order to test a possible employment of these junctions at $T > 4.2$ K, their temperature behavior was studied by measuring the $I_c(T)$ dependence from 2 K to the transition temperature T_c. This transition temperature ranged typically from 7.5 to 8.8 K, depending on the relative thickness of the niobium base electrode and the aluminum overlayer.

Independently from the actual value of T_c, three temperature ranges corresponding to different junction behaviors were observed. For $T/T_c < 0.4$, the junction is a superconductor - insulator - superconductor junction; for $T\ /\ T_c > 0.6$, a SNS-like junction; and for $0.4 < T/T_c < 0.6$, a transition region is identified.

This behavior underlines a peculiar feature: the possibility for a junction with a given Al and AlO$_x$ thickness to induce a transition between the hysteretic and the non-hysteretic regime by varying the temperature below or above 4.2 K, as shown in Figure 3.3.

An advantageous characteristic of these junctions for a voltage standard operating above liquid helium temperature is the smoothness of $\mathrm{d}I_c(T)/\mathrm{d}T$ for $T/T_c > 0.6$. At $T = 0.7 - 0.8\,T/T_c$, I_c decreases to only 0.25 – 0.40 of the value of I_c at 4.2 K. A similar scaling has been observed for V_c, since R_n does not change in this temperature range. Consequently, values of J_c of tens of kA/cm^2 and V_c of more than 100 μV were measured near T_c.

To test the metrological performance, measurements of the RF- induced voltage steps at 75 GHz were carried out by varying the operating temperature of the junctions from 4.2 K up to the Nb transition temperature. This frequency of 75 GHz is the best choice to avoid an exceedingly high integration level of the voltage standard

circuit, while optimizing the homogeneity of the junction parameters and the distribution of the microwave radiation. For instance, programmable voltage standards at 1 and 10 V fabricated with junctions with a characteristic voltage optimized for operating at this frequency require a reduced number of series-connected junctions with respect to other circuits working at lower frequencies [33].

The size of the measured junctions was 5 x 5 μm^2 and they had $J_c = (2 - 5) \cdot 10^4$ A/cm^2 and $V_c = 200 - 500$ μV at 4.2 K. The amplitude and stability of the quantized voltage steps were monitored via a nanovoltmeter to ensure their flatness at the due metrological level. At each temperature, the RF power was varied to maximize the amplitude of the RF- induced steps.

The temperature behavior of the first steps at 75 GHz of a single overdamped junction is shown in Figure 3.4. For clarity, each curve is shifted by $2V_1$ on the horizontal axis, where V_1 is the voltage corresponding to the $n = 1$ RF- induced step. The height of the $n = 1$ and $n = 2$ voltage steps is well above 1 mA even at the highest measurement temperature shown in this figure. The inset shows the RF-induced steps at $T = 8.3$ K, a temperature close to the transition temperature of Nb in this device. It must be noted that the voltage steps are flat at the nanovolt level also at the highest temperatures, clearly demonstrating the possible use of these junctions in precision measurements above liquid helium temperature.

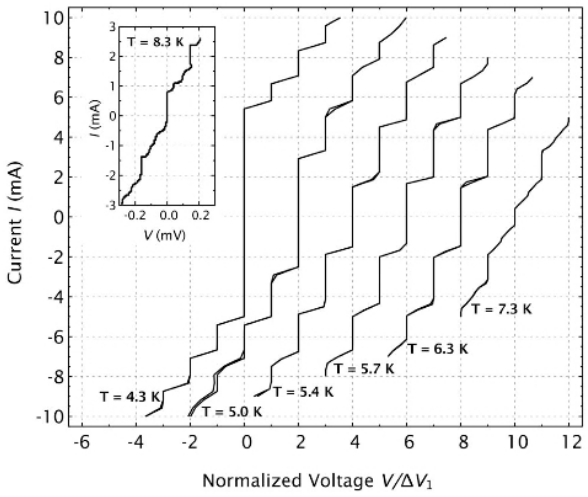

Figure 3.4. I-V characteristics showing the RF- induced steps at 75 GHz of a single overdamped junction at several temperatures. Each curve is shifted on the horizontal axis by $2V_1$. The inset shows the I-V characteristic at 75 GHz at a temperature close to the transition temperature of Nb.

Rounding of the step was observed when approaching the transition temperature, for $T/T_c > 0.85$, depending also on the value of the characteristic voltage of the junction at the measurement temperature.

Calculations derived from the basic theory of Josephson junctions state that the maximum amplitude of the first step and the minimal power dissipation are achieved when the junction characteristic frequency $f_c = V_c\ (2e/h)$ and the microwave drive frequency f_d, satisfy the relation $f_d/\ f_c = 1$, while the step amplitude is considerably reduced for $f_d/\ f_c < 1$, and the dissipation of RF power in the junction is greatly increased for $f_d/\ f_c > 1$ [34]. This explains the decrease of I_c and, consequently, of the height of the first step, which is steeper than expected in junctions at temperatures where $f_d/\ f_c > 1$, as the increased power dissipation in the junction induces instantaneous transitions and, hence, a reduction of the critical current and of the $n = 1$ step.

This is outlined in Figure 3.5, where the measured height I_1 of the $n = 1$ step is plotted as a function of the reduced temperature. For each temperature, the height of first quantized step is normalized to the critical current of the junction at that temperature.

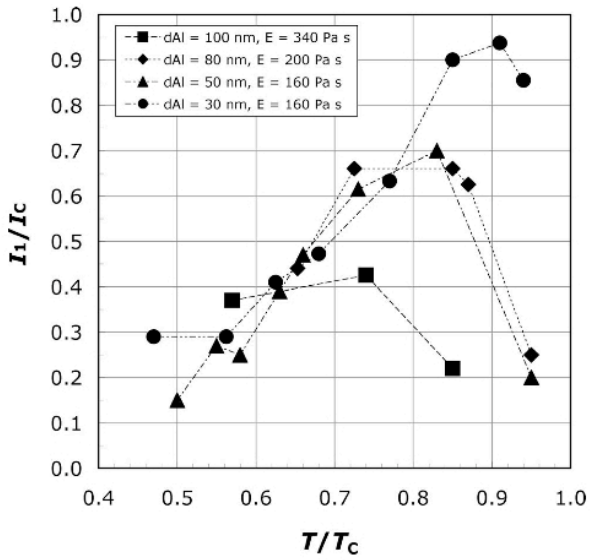

Figure 3.5. Temperature dependence of the height of the first RF- induced step for single junctions at 75 GHz. The height of the step I_1 is normalized to the value of I_c at each temperature.

Figure 3.6 shows the corresponding values of V_c as a function of the normalized temperature, for the same junctions of Figure 3.5, together with data for a ten-junction array. The junctions shown in Figures 3.5 and 3.6 have decreasing values of the Al thickness from 100 to 30 nm and of the oxygen exposure from 340 to 160 Pa $\cdot$ s. $I_1(T)/I_c(T)$ increases with temperature and reaches its maximum at $T/T_c = 0.75 - 0.9$, where $f/f_1 \sim 1$. The reduced temperature corresponding to the maximum of I_1 is, therefore, inversely proportional to the junction characteristic

frequency. This allows us to define the optimal design and operating conditions for these junctions, choosing Nb/Al bilayers with the highest possible transition temperature and using them at temperatures of 7 – 8 K.

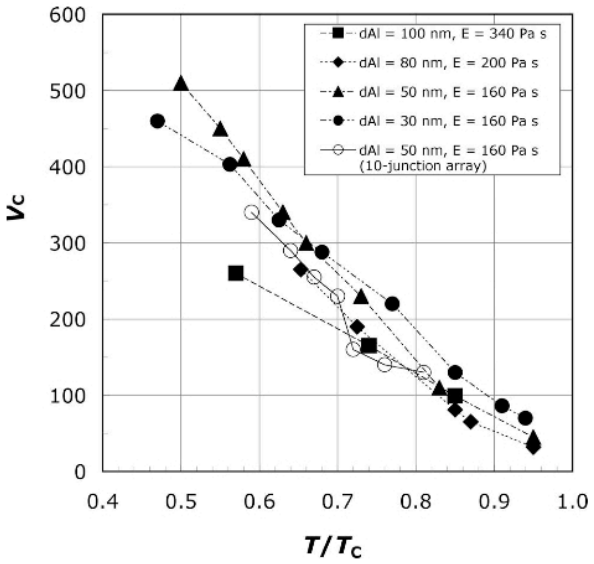

Figure 3.6. Temperature dependence of V_c for the same junctions in Figure 3.5. The open circles correspond to data for a ten-junction array.

These results pave the way to using such junctions for voltage standard circuits in a more convenient setup, e.g., with a cooling system based on the 10 K cryocoolers family developed for cryopumps minimum operating temperature at 6.5 K, with significant advantages in terms of costs and refrigerating power [35]. Furthermore, this is achieved without the need of complex fabrication processes required by other junctions' technologies.

Part III

The Nb/Al-AlO$_x$/Nb SNIS fabrication process

Chapter 4

Thin film technology: main techniques

4.1 Introduction

Modern thin film technology has evolved into a sophisticated set of techniques used to fabricate many products. Applications include very large scale integration (VLSI) circuits, electronic packaging, sensors, and devices, optical films and devices, as well as protective and decorative coatings.

The realization of a thin film device requires typically three operating steps, namely the film deposition, the patterning (to define one or more geometries), and the etching.

At INRIM, in the "Nanotechnology and Quantum Devices" group, it is currently active a Thin Film Laboratory associated with the NanoFacility Piemonte Lab for material micro and nanomachining, where superconducting devices based on a thin film structure are fabricated and characterized. Different facilities are present in these laboratories, among which a DC and a RF sputtering (Appendix C.1) systems for the thin films deposition, a Reactive Ion Etching (RIE) (Appendix C.2) for their removal by plasma etching and a clean room for their geometrization by photolithographic processes (Appendix C.3).

This Chapter details the techniques adopted to perform the Nb/Al-AlO_x/Nb-based devices under investigation in this thesis. Two other additional lithographic techniques used in this dissertation, as the Electron Beam Lithography (EBL) and the Focused Ion Beam (FIB) (Appendix C.4), will be rather described in the Chapters 7 and 8, respectively.

4.2 Deposition of thin films

In recent years considerable advances have been achieved in the science and technology of the thin film deposition processes. Up to the present, thin films have been studied from a viewpoint of the relationship between structure and properties; on the other hand, the commercial use of thin films has been growing at a rapid rate in almost all industrial fields, above all electronics and optics. The films are formed by depositing material onto a supporting substrate through a complicated building up process, rather than by thinning them down by mechanical polishing and/or ion milling techniques. Low temperature physics applied to the realization and the study of thin film devices needs a complex structure of high-tech laboratories for deposition and patterning of thin film devices.

The realization of thin film devices requires either to deposit the films controlling their physical and structural properties or to define suitable patterns, able to reproduce the circuitry geometries.

4.2.1 Basic vacuum concepts

Many prevalent deposition techniques used in the modern thin film technology require the creation of a vacuum for the deposition to occur. As a result, an entire industry and a new branch of science have developed to meet this requirement. For many of this techniques, the quality and consistency of the final product depends on the vacuum conditions during deposition. The vacuum degree is also one of the most critical factors able to influence the superconducting performances of thin films at cryogenic temperatures. In particular, a high and ultra high vacuum ambient reduce the gaseous inclusions into the deposited layer, avoiding, for example, a reduction of the niobium transition temperature.

A number of reasons exist for the deposition of materials in a vacuum environment. Vacuum conditions increase the mean free path for atoms, eliminate the presence of gases that could react with the deposited material, reduce the vapor pressure (thus lowering the evaporation temperature of materials), and provide the ultimate clean environment.

A vacuum is absence of material, including the gases, moisture and particles which normally fill our environment. In a deposition system, a container is provided and the majority of these elements are removed to create a vacuum. The complete and total removal of gases from any vessel is impossible. As a result, the degree of quality of vacuum required depends on the application.

Several systems of units have been developed to measure and quantify the quality of a vacuum, including the torr, also referred to as mm of mercury (mm Hg), Pascal (Pa), millibars (mbars), etc. The standard international (SI) unit of pressure, Pa, will be the primary units of measure in this dissertation. However, a conversion to

millibar (1 mbar = 100 Pa) will usually be provided because it is a very common unit of measure.

4.2.2 The sputtering technique

There are three categories of thin film deposition processes: physical vapor deposition (PVD), chemical vapor deposition (CVD) and chemical methods. The sputtering is a PVD process involving the removal of material from a clean solid cathode (target) (Figure 4.1). This is accomplished by bombarding the cathode with positive ions emitted from a noble gas discharge [36]. When ions with high kinetic energy are incident on the cathode and accelerated by an electrical field, the subsequent collisions knock loose, or sputter, atoms from the material. The process of transferring momentum from impacting ions to surface atoms forms the basis of the sputter coating. The emitted atoms condense onto a substrate forming a film of the same material of the target. Electrons on a clean metal surface would need very high kinetic energies, several hundreds of keV, to accomplish physical sputtering because the energy transfer between the light electrons and the heavy atoms is very inefficient. For this reason ions are commonly used for this purpose, they can be accelerated better than neutral atoms using electric fields. At very high energies the process involves more radiation damage than sputtering. The range useful for sputter deposition is considered from the threshold to about 5 keV. Measurements on sputtering yield and average velocities of sputtered atoms (higher than evaporated ones) show that sputtering is a rather inefficient process where 95% of energy is dissipated as target heat. Sputtering was originally developed to deposit refractory metals, which could not be deposited using the thermal evaporation techniques of that time. Today, sputtering has developed into a versatile deposition technique that is able to deposit most materials.

A typical sputter deposition system consists of a vacuum chamber, a sputter source, vacuum sensors, a substrate holder, and a pumping system (Figure 4.2) [37]. Deposition pressure is controlled by the rate of gas passing into the chamber and by a throttle valve placed between the vacuum pump and deposition chamber. By adjusting the gas flow into the system and the throttle valve opening that controls the pumping speed, a constant pressure is maintained. This supply of rare gas is the ionized using large potentials at the source, resulting in the generation of a plasma and a sputtering from a target material onto the substrate and chamber walls.

The two most common typologies of sputter sources are diodes and magnetrons. Both of these configurations can be operated with direct current (DC) or radio frequency (RF) potentials to generate a plasma through the ionization of a rare gas.

A basic diode sputter source consists of a target in the shape of a flat disk bounded to a water-cooled plate. An external potential is applied from an outside power source, charging the target to a high negative voltage (3 to 5 kV). A rare

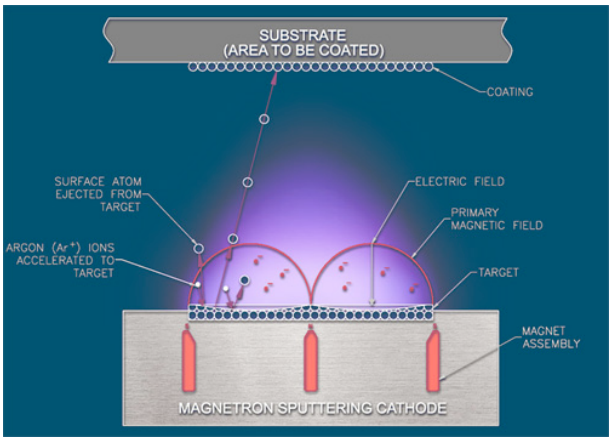

Figure 4.1. Scheme of the sputtering phenomenon.

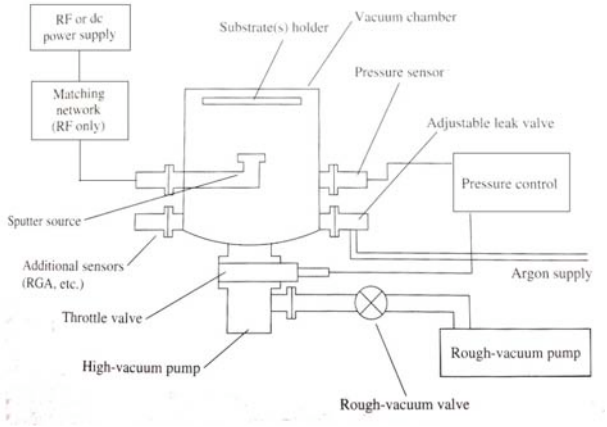

Figure 4.2. Schematic representation of a typical sputtering system.

gas, usually Argon is introduced into the vacuum chamber between the target and the grounded substrate and chamber walls. The large difference in potential forma a plasma, caused by ionization of the Ar atoms in the intense electric field. This ionization results in a negatively charged electron and positively charged ion pair, whereas the plasma itself retains a net neutral charge. Positively charged ions are attracted to the negatively charged target and accelerated by the electric field, resulting in a collision with the target material. Bombardment of the target with these high-energy ions leads to sputtering of the target atoms, forming a coating on the substrate and the chamber walls. In this type of configuration, the target and the substrate holder can be considered a parallel plate capacitor. This creates a number of advantages:

- The plasma or ionized gas is created uniformly between the cathode and anode,

causing a uniform consumption or sputtering of the target.

- Diodes sources are the cheapest and least-complex sputter source to use.
- Target for this type of source consist of a flat disk. They can be easily fabricated without the need for complex shapes often required for magnetrons. As a result, the targets are lower in cost, which can be a critical issue for deposition of precious metals.

Based on these advantages, diodes sources are widely used in manufacturing for the metals and metal alloy of films. However, there are several limitations:

- Diodes sources are inefficient and do not make use of the generated electrons to maintain the plasma.
- Electrons generated in the plasma irradiate the substrate, which can result in damage to the substrate surface, or lattice, for highly crystalline substrates.
- Deposition rates from diode sources are much lower than those from magnetron sources.

Magnetron sources overcome the limitations of the diode sources by using a magnetron field to control the motion of electrons. This approach centers around a magnetic field's ability to exert a force on a charged particle in motion. Because electrons and ions in a plasma have identical charges but radically different masses, the radius of their helical paths is quite different. Low-mass electrons are highly affected by the magnetic field and move with a radius that is usually much less than the dimensions of the plasma and deposition system. By comparison, the much heavier ions travel with a radius much greater than the dimensions of the plasma and deposition system; as a result, the magnetic effect on the ions is not significant. Magnetron sources use the properties defined in this physical law to control the electrons generated in the plasma and apply them toward plasma regeneration.

The key difference between a planar magnetron source and a diode one is that a permanent magnet is placed behind the target. The resulting magnetic field confines the electrons to a circular path on the surface of the target disk. These energized electrons further ionize the gas molecules through collision, resulting in a large increase in plasma density at the target surface and increase in sputtering rate from the target, with reduced irradiation of the substrate and chamber walls. Because the sputtered target atoms are relatively massive and neutrally charged, they are not affected by the magnetic field, and they migrate to coat the substrate and exposed chamber surfaces. The key advantages of this type of source include a vast improvement in efficiency compared the diode sources, sputter deposition rate are improved because of the increased plasma density and a reduction in substrate

bombardment by energetic electrons occurs. The primary problems of magnetron sources are that they are more complex and therefore more expensive.

Both type of sources can be operated with DC and RF potentials. The first technique it is very effective for the deposition of conductive materials. However, targets composed of insulators will build up a significant positive charge, resulting in collection of positive ions that cannot be drained away. As a result, methods using RF sputtering were developed. RF sputtering uses a 13.56 megahertz (MHz) sinusoidal voltage to drive the source. The substrate and the chamber walls are held at ground potential. Using this approach, the charge that builds up on a dielectric target is dissipated though the second half of the cycle.

RF sputtering is perhaps the most versatile technique and can be used to deposit virtually any materials. Because the deposition mechanism of sputtering is mechanical and highly energetic in nature, refractory materials such tungsten, nioubium, tantalum and molybdenum can be easily deposited at temperatures below their melting points.

4.2.2.1 Sputter etching

Sputtering can be also use to removed portions of films, previously deposited. This process is called sputter-etching and it is realized reversing the polarization applied between target and substrate: in this configuration the Ar ions are accelerated towards the substrate instead of the target. The sputter etching performs an anisotropic remotion of the film, essentially along the direction perpendicular to the substrate. The bombardment in this case is useful to eliminate the impurities on the substarte surface.

The use of this surface cleaning technique improves both the electrical properties of ultra-thin films by decreasing the impurity content of the substrate, and the adhesion of the deposited film on the substrate.

4.2.2.2 Presputtering

Sputtered thin films are deposited with a gaseous impurity background, which is primarily borned to desorption and breakup by argon ion bombardment of surface adsorbed species. The background, generated by the plasma, decreases with the duration of the discharge owing to the getter property of nioubium.

The presputtering consists of a cleaning up process of the target surface and differs from the real sputtering only for the absence of the substrate on the anode: the tension between the target (cathode) and the anode is equally applied, and the target is sputtered, being its surface cleaned up. Presputtering is therefore performed before each deposition.

The presputtering of a Niobium target, anyway, carries on another fundamental task: owing to the Nb getter properties, an extensive presputtering is usuful to clean the chamber from impurities, decreasing the base pressure before starting the deposition.

4.3 Pattern generation techniques

4.3.1 Introduction

Fabrication of thin film integrated circuits, semi or superconductor devices requires to deposit the thin films by accurately controlling both physical and structural properties and pattern definition through microlithographic processes, which play a critical role in the overall success of integrated circuit manufacturing. Lithographic processes define substrate regions for subsequent etching removal or materials additions. The size and precision of these regions depends on the capabilities of the particular process. Lithographic processes essentially drive integrated circuit design and fabrication and are responsible for advances in integrated circuit feature size, speed, and packaging density. The International Technology Roadmap of Semiconductors [38] states pushes the integration levels in the direction of decreasing feature size and increasing the number of devices. This trend is responsible for the dramatic decrease in cost per function, the increase of the elaboration speed although the cost per integrated circuit essentially remains the same.

Many different techniques are available to pattern thin films, and the most common ones will be described in details here: wet etching, dry etching and lift-off. All these process are based on the photolithographic technique, employed to transfer a defined geometry from a metallic mask to a photosensitive material, namely photoresist, previously dispensed on the films.

Since the minimum dimension of the geometry, transferred to the resist layer, is determined by lithography, it is fundamental maintaining an accurate control of the environmental parameters of the laboratory where the process is carried out: it is necessary to avoid the deposition of dust or different particles onto the mask or onto the photoresist surface compromising the correct replication of the established geometry. So, to reduce defects the photolithographic process is completely performed in a clean and controlled environment (clean room), where the number and the dimensions of the particles inside are strictly controlled by suitable filters. The clean room laboratories are classified according to the number and the dimension of the particles. The clean room at INRIM is a ISO 5 clean room (Appendix C.3), and means that inside there are less than 832 particles with dimensions larger than 1 μm in a m^3.

4.3.2 Photolithography

Photolithography is the production of a three-dimensional relief image based on the exposure to light and subsequent development of light-sensitive photoresist [39]. Microlithography is used to print ultrasmall patterns, primarily in the semiconductor industry. The types of radiation, materials, and tools are important characteristics of a process, but the basic steps are generally the same as those conventional otical lithography. Radiation-sensistive photoresist is applied to a substrate as a thin film. Image exposure is then transmitted to the photoresist, usualy through a mask of clear and opaque (cromium layer previously deposited) areas on a quartz substrate. Clear areas within the mask allow exposure of the photoresist material, which photochemically alters the material. Depending on the type of photoresist used, exposure will either increase or decrease the solubility of the exposed areas in a suitable solvent called developer: positive photoresist will become less soluble in exposured regions. The solubility differential of exposed to unexposed areas is responsible for the reproduction of the mask image into the photoresist.

After development, regions of the substrate are no longer covered by the photoresist film. Further subtractive or additive processing can now be performed, either by etching unprotected areas or by depositing layers over exposed layers of the substrate (plating or lift-off). The photoresist, therefore, must be capable of reproducing desired pattern imagesand providin protection, or resistance, for the substrate in subsequent processes. A schematic of positive and negative photolithographic processes is shown in Figure 4.3.

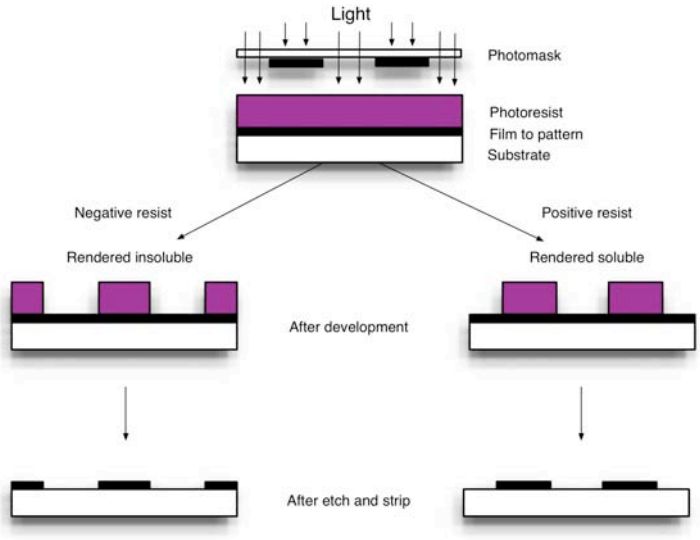

Figure 4.3. The basic steps of a photolithographic process: negative (left) and positive tones (right).

All the optical masks used in this thesis were fabricated at the Physikalisch-Technische-Bundesanstalt (PTB), in Braunschweig, Germany.

4.3.2.1 Photoresist

Photoresist is generally an organic polymer material, which allows to transfer the geometry of an hard metallic mask (usually Cromium-Quartz) to the surface of the device. Resists must be classified either as positive or negative depending on their response to exposure. Generally they are two-component systems, where the resist is formulated from a base matrix resin, which serves as a binder for the material, and a sensitizer, which provides appropiate exposure sensitivity. In addition to these components is a casting solvent that keeps the resist in a liquid state until application.

Optical resists can be sensible to different wavelenghts in the electromagnetic spectrum (from X-ray, UV, IR or optical-lenght). Shorter wavelengh of the incoming radiation results in a better resolution of the lithographic process, allowing the reduction of the minimum size of the obtainable geometry. At INRIM the photolithographic system is based on a UV radiation generated by a Hg vapor lamp, working at a wavelenght of 350 - 410 nm, allowing a spatial resolution of 1 μm (Appendix C.5).

After cleaning and priming the substrate with an adhesion promoter, its surface can be coated with photoresist. This is generally achieved by spin coating resist over the wafer. The spin coating procedure is composed of three stages: (1) dispensing some resist drops onto the wafer surface; (2) acceleraing the wafer to the final rotational speed, and (3) spinning the wafer at constant speed to spread and dry the resist film. After the spinning step, the coating acquires a relatively uniform, symmetrical flow profile. Most spin coating is perfomed at the speeds from 300 to 7000 rpm for 20 to 60 seconds, producing coatings with variable uniformities. In this thesis two angular speeds were generally used, 3500 and 4000 rpm, and thicknesses of 1.5 μm and 1.2 μm were obtained (for Recipes, refer to Appendix B.1 and B.2). The photoresist is then baked (soft-bake) and partially dried, removing solvents and improving adhesion to the surface of the substrate.

The device is then aligned to the desired mask and the resist layer is exposed to the UV radiation for a fixed time, by using an optical system, called mask aligner. This system is equipped by micromovements and an optical microscope for the alignment, and the UV lamp for the exposure. The exposure process modifies the chemical structure of the photoresist: the strong energy of the UV radiation breaks the chemical bonds of the long polymeric chains. The area of the photoresist exposed to the UV light through the quarz becomes more soluble and easily removed in a basic liquid solution (developer) compared to the resist area shielded by the chromium.

The optical lithography described above is defined as a "positive" lithographic process, because the metallic pattern present in the mask is exactly transferred to the resist layer, as a positive image of the geometry. Rather, if the complementary image of the metallic mask has to be replicate, a different resist (negative resist) has to be employed, where shorter polymeric chains polymerise by using UV radiation. In this case, the exposed resist area becomes less soluble than the part not exposed, and this opposite process is called "negative". For a negative process it is also possible to use a reversal resist (Appendix B.2).

At the end, a post-development baking step (hard-bake) can be performed to remove residual solvents, improve adhesion, and increase the etch resisteìance of the resist. Additionally, this baking step causes some resist flow, which can fill pinholes in the film and reduce stress between film layers. The basic lithographic processes in cross sectional views are shown in Figure 4.3.

4.3.3 Thin film etching

The etching process results in the removal of material (insulating or metallic layers) in the regions not protected by photoresist, and can be done with suitable chemical solutions in the liquid state or plasma etching in the ionized gas state. The main etching techniques are classified in wet etching, dry etching and lift-off.

This Section will detail the main etching methods used to fabricate the devices under investigation in this thesis and described in Chapters 6 and 7, and in this dissertetion, the etching was mainly concerning metallic niobium films as a fundamental step to realize Nb/Al-based devices.

4.3.3.1 Wet etching

Wet etching is a chemical process where the substrate is immersed in a liquid each bath, usually a strong acid or base solution, to remove the uncovered layer. A simple wet etching process may dissolve material without changing its chemical nature, and in general, can involves one or more chemical reactions that consume the original reactants and produce new species.

The advantages of wet etching are low cost, high reliability, excellent selectivity in most cases with respect to both resist mask and substrate materials. The major disadvantages of the wet etching are that, for certain films, the selectivity to the photoresist is poor, a higher safety risks due to the direct chemical exposure of the personnel and the resist's loss of adhesion to the substrate. Another disadvantage is that, for most substrates, wet etching is isotropic, meaning that the etch rate is the same in all directions. This results in the lateral etch and vertical etch being almost equal, with a consequent limitation in resolution.

Wet etching was not directly exploited in this research, but the fundamental aspects were considered in comparison with the other following techniques.

4.3.3.2 Dry etching

The dry etching is the most used technique in thin films patterning. It is a process in which the substrate is exposed to gases in an excited state (plasma) able to etch and remove the films. The ions are accelerated to the circuit and the uncovered and unprotected material is ejected from the substrate. The main advantage of dry etching is that the substrate can be etched anisotropically (with vertical etch walls). There are several dry etching techniques and the differences are the operating conditions of the plasma and the type of gas in the plasma.

The main dry etching technique employed in this dissertation was the Reactive Ion Etching (RIE). This technique is a combination of physical and chemical etching. The plasma used for the physical etching (generated between two parallel electrodes) is not generated by a noble gas ions, but it is chosen according to the material to etch. For Nb, gases like CF_4 or SF_6 are employed. The etching mechanism involves chemical reactions between the accelerated ions and the thin film atoms. The resulting etching rate is higher than physical ones with the same applied powers. Generally, the RIE shows a good selectivity and the consequent etching results directional and highly anisotropic. Certain gases (carbon based) could lead a polimerization onto the device surface, slowing and eventually stopping the etching process. Adding oxygen into the plasma can prevent this problem.

The Figure 4.4 shows a diagram of a common RIE setup. A RIE consists of two electrodes (labelled 1 and 4) that create an electric field (3) meant to accelerate ions (2) toward the surface of the samples (5). The area labeled (2) represents plasma that contains both positively and negatively charged ions in equal quantities. These ions are generated from the gas that is pumped into the chamber. In the diagram CF_4 is pumped into the chamber, making a plasma with many Fluorine (F^-) Ions. The fluorine ions are accelerated in the electric field, cause them to collide into the surface of the sample. The purple layer represents the photoresist mask used to protect certain areas from etching, and exposing only the areas desired to be etched.

4.3.3.3 Lift-Off

Lift-off is a simple and easy technique in which the deposited thin film being applied to the substrate is addes only where the material is desired, as opposed to being removed from regions where the thin film is not desired. The substrate is coated with photoresist first and imaged, so that there is no photoresist where the thin film is desired. Then the thin film is deposited on the substrate. Finally, the photoresist is stripped off in a solvent, generally aceton, lifting off the undesired thin film on

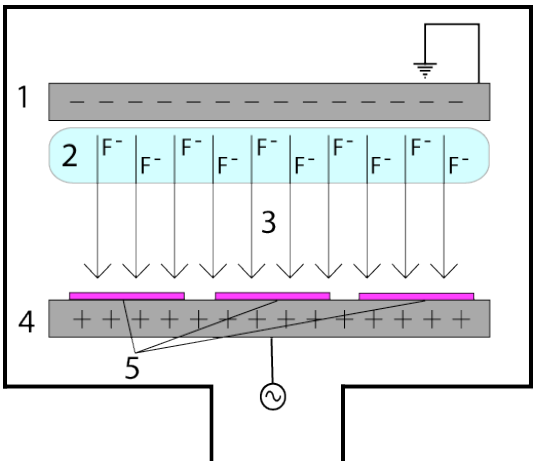

Figure 4.4. Diagram of a common RIE setup

the resist and leaving the thin film material on the substrate only where desired. A lift-off process is illustrated in Figure 4.5, [37].

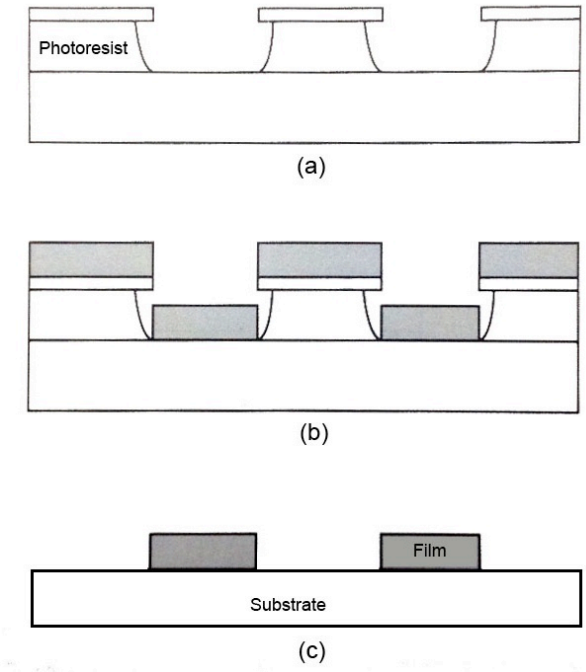

Figure 4.5. Lift-off process. (a) Create a reverse slope or undercut resist edge profile, (b) deposit film by sputtering, (c) chemically strip photoresist and lift-off film, leaving film in desired pattern.

This is the most simple technique to pattern the device, but the edges of the films

result not so sharp. For this reason it is not employed to define small areas or critical geometries. Finally, dry etching techniques are anisotropic, while wet etching is not directionally selective. This could be critical for the definition of small areas because the isotropic etching can remove material even under the protective resist mask (Figure 4.6) and the resulting geometry is not the desired one. Furthermore, the dry etching of a very thick film could be difficult because of a high energetic process occuring for a long time could melt or consume the resist, leading to undesired effects of over and under etching.

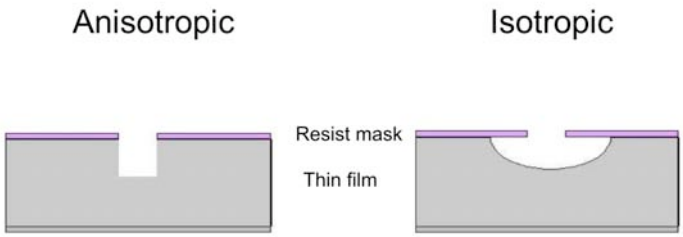

Figure 4.6. Resulting etching profiles: anisotropic shape typical for dry etching (RIE) and lift-off, compared to isotropic one typical of wet etching processes.

Chapter 5

Fabrication process of Nb/Al-AlO$_x$/Nb SNIS junctions

In this Chapter is described the multi-step fabrication process studied and implemented at INRIM to realize superconducting quantum devices based on Nb/Al-AlO$_x$/Nb SNIS Josephson junctions, wherein the area is patterned by optical lithography, at the micrometer scale. In particular, the sequence of the operating steps represents the basic process by which further SNIS-based prototypes have been realized, as described in the later chapters (Chapters 6 and 7), as subjects of this thesis. The basic device process can be summarized in the following steps:

- Substrate preparation and cleaning
- Deposition of superconducting electrodes and growth of the tunneling barrier
- Patterning of superconducting electrodes
- Patterning of the junction area
- Insulation of the junction sidewalls
- Deposition and patterning of metallic electrical contacts

The process flow is demonstrated in Figure 5.1.

Moreover, the fabricated SNIS prototypes reported in Chapters 7 and 8 required the use of additional techniques for the definition of junctions' area instead of photolithography, the Electron Beam Lithography (EBL) and the Focused Ion Beam (FIB) respectively, and will be described in details in their proper sessions (Sections 7.2.1 and 8.2).

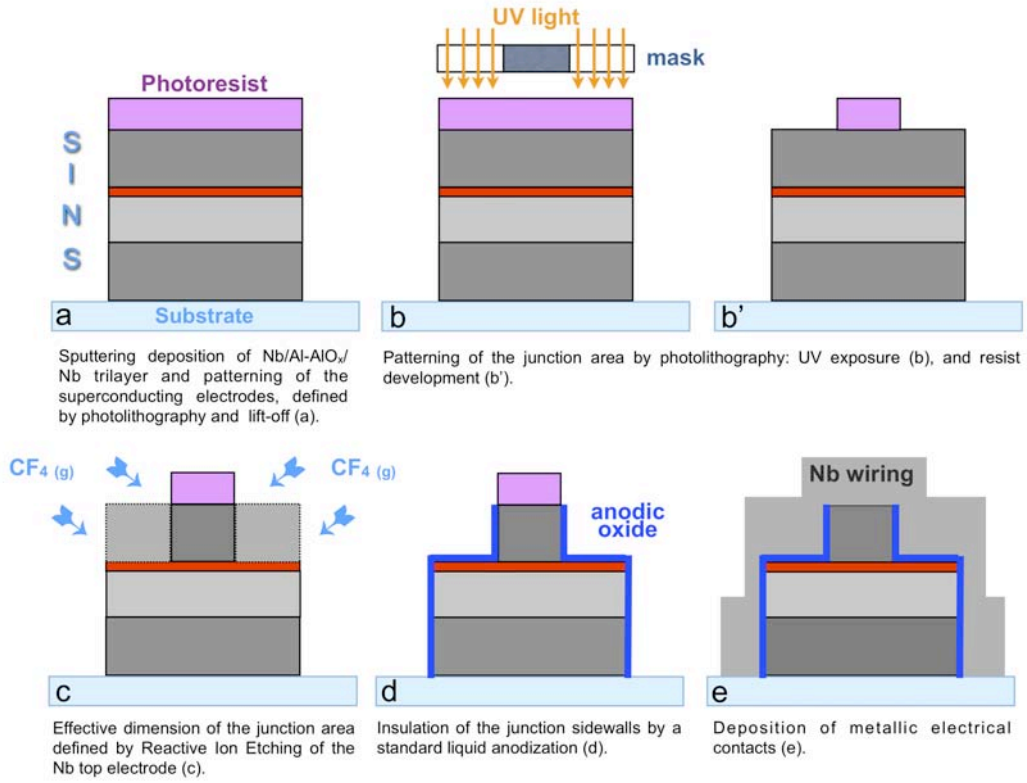

Figure 5.1. The main fabrication steps of the SNIS-based circuits process implemented at INRIM.

5.1 Introduction

As mentioned before into the Chapter 3, the Nb/Al-AlO$_x$/Nb SNIS Josephson junction is fabricated by sandwiching a thin insulating layer (I) and a thicker Aluminum normal layer (N) between two superconducting Niobium electrodes (S), as shown in Figure 5.2. The first Nb film previously deposited on the substrate is the so-called "base electrode", while the last one is the the "top-counter electrode".

5.2 Substrate preparation and cleaning

All Nb/Al-AlO$_x$/Nb multistructured films (or so-called "trilayer") were deposited on silicon substrates with a 250 - 500 nm oxidized surface layer with high resistivity (about 4500 ohm cm), unless otherwise stated. The choice of the substrate was studied to guarantee a good planarity and a lower risk of losses of the external microwave signals, at the desired frequency during measurements. A four inch wafer was diced with diamond tip into 2.5 × 2.5 cm^2 chips.

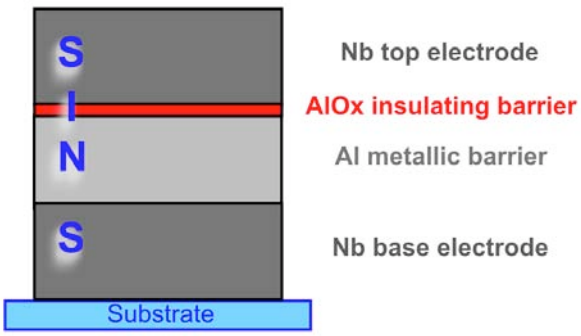

Figure 5.2. The multilayer structure of a Nb/Al-AlO$_x$/Nb SNIS Josephson junction.

Many fabrication problems encountered in micro and nanolithographic processing results from contaminations in substrate surface and in coating phases. Contaminants can lead to adhesion problems both for thin films and any type of resists. So, prior to loading into the sputter deposition system, or before the resist coating, the wafers were cleaned using an ultrasound bath of acetone, followed by further soaking and ultrasound in isopropanol, and drying it with a nitrogen gun.

5.3 Deposition of superconducting electrodes and growth of the tunneling barrier

Niobium is a superconducting and refractory material characterized by a high melting point (2750 K or 2477 °C), and a critical temperature of 9.2 K. Nb thin films are commonly deposited by a sputtering technique being an energetic process, in a high vacuum ambient to guarantee high-purity layers. Indeed, an oxygen content can reduce the critical temperature, compromising the electrical behaviour and the performances of the entire device.

The Nb/Al-AlO$_x$/Nb trilayers were deposited by a RF sputtering system (Appendix C.1), in high vacuum conditions (down to 10^{-7} mbar). A photoresist stencil was spread on each substrate before deposition to define the base electrode geometry for the subsequent lift-off process.

The trilayer deposition is preceded by 5 min of sputter etching with Ar^+ ions at a DC voltage bias of 500 V, in order to clean the substrate surface and improving the uniformity and the planarity of the subsequent Nb film. Moreover, such a slight sputter etching before deposition of the film improves the electrical and structural properties of the Nb layer. Afterwards, the cleaning of the target is also carried out by a pre-sputtering of 10 minutes at 1000 V at RF voltage.

Before starting the trilayer deposition, the base pressure into the deposition

chamber has to be of about some units in 10^{-7} mbar. This pressure guarantees defect-free films and with a such value Nb films show good superconducting properties and their critical temperature, T_c is close to the bulk (9.2 K). The Nb base electrode is than sputtered with a deposition rate of 0.65 nm/s and a pressure of $5 \cdot 10^{-3}$ mbar of Ar^+ (99,99% pure). The electrode is typically 120 nm thick, but could change depending on the particular device, as specified from time to time in this work. All these operating parameters strongly influence the properties of the Josephson junction, and these values represent a good compromise among a nearly stress-free film, better electrical features, and a smooth surface affecting the subsequent oxide barrier growth.

After the first deposition, the Nb base layer is allowed to cool and relax its internal stress for about 15 min (cooling time). Absence of stress and smooth layer surface is important to avoid any crack formation in the subsequent aluminum metallic layer.

Thereafter, the aluminum layer is deposited at the same Ar^+ pressure with a rate of 1.5 nm/s, later a presputtering of 10 min to clean the Al target. As mentioned before (Chapter 3), the SNIS junctions could vary both the Al thickness and the oxidation exposure, resulting different electrical behaviours. In particular, overdamped SNIS junctions were obtained by varying the Al thickness from about 50 to 100 nm, according to the desired critical current, I_c and the characteristic voltage, V_c.

Following, a thermal oxidation of the Al film is carried out *in situ*, introducing pure oxygen (99.99% pure) in the chamber without breaking the vacuum. In this way high reproducibility and quality are reached because of the highly pure Nb electrodes and the very low defects in the barrier. The oxygen pressure (P in Pascal, Pa) is monitored over the exposure time (t in seconds, s), resulting an exposure dose, E calculated by their product P $\cdot$ t (Pa $\cdot$ s). Oxidation time and oxygen pressure are variable parameters for controlling the aluminum oxide thickness and the transparency of the tunneling barrier, and, as a consequence, the critical current density, J_c, of the junction. SNIS junctions are characterized by an E value ranging from 120 to 1000 Pa $\cdot$ s, resulting in high critical current densities and negligible capacitance values.

Finally, the Nb top counter electrode is sputtered in the same operating conditions compared to the Nb base electrode, and, in principle, with the same thickness of 120 nm.

5.4 Patterning of superconducting electrodes

The geometry of the sputtered Nb/Al-AlO$_x$/Nb trilayer was previously defined by optical lithography through a photoresist mask. Subsequently the trilayer deposition, a following lift-off process was done by soaking the sample in acetone, and

easily removing the material in excess previously sputtered all over the wafer surface, above the resist stencil.

In this particular case, wherein the base electrode geometry is not so critical thanks to its large dimensions, the lift-off represents an ideal patterning method, providing a well-defined and stress-free trilayer structure. This fabrication step is represented in Figure 5.1a.

5.5 Patterning of the junction area

The following process step is the definition of the effective area of the junction through the patterning of the Nb top counter electrode. This area is defined by Reactive Ion Etching (RIE), and a further photoresist mask is previously patterned on the circuit (Figure 5.1b and b'), defining the top electrode dimensions. In particular, this lithographic step allows to cover with photoresist the section of the trilayer defining the effective tunnel area, and at the same time, leaving uncovered the Nb top layer which have to be removed by the reactive etching all around the stencil.

The advantage of RIE is due to its high anisotropic etching and high etch rate, with consequently vertical profiles along the sidewalls of the junction, even if a long exposure to tetrafluoromethane, CF_4 plasma can damage the resist stencil inducing a large stress on the Nb sputtered films. The RIE of the Nb top layer is performed in CF_4 gas with a pressure of about $5 \cdot 10^{-1}$ mbar, at RF power of 100 W (Figure 5.1c). Rather, in these operating conditions, the selectivity of the CF_4 is very high; in fact the AlO_x barrier represents a good etch stopper, due to its lower etch rate in F^- atmosphere compared to niobium. The wet etching (acid etching) was not considered for this step, because of its lower directionality and the high risk of under etching of the Nb top with a consequent uncontrolled reduction of the junction area.

5.6 Insulation of the junction sidewalls

As previously explained, the reactive etching performed by CF_4 leaves unprotected both a portion of the top electrode uncovered by the resist stencil and the sidewalls of the Josephson junction. However, all these exposed surfaces need being isolated by a later anodization process in order to avoid short circuits between the Nb top-counter and the base electrodes (Figure 5.1d), during the deposition of the metallic contacts, as described in the next paragraph.

The anodisation is performed by using a mixture of ammonium pentaborate, ethylene glycol and deionized water [40]. In this process, the Nb top layer and all the metallic parts exposed to the liquid represent the anode of the anodization circuit, while the cathode is a platinum wire, both merged in the conductive anodization

solution. This electrolytic process is able to convert all the resist-uncovered metals (Nb and or Al) into the stoichiometric anodic oxides (Nb into Nb_2O_5 and Al into Al_2O_3), insulating the Nb top layer from the base one. A constant current is fed into the circuit by a Keithley 220 current source. During the process, when Al in converted into Al_2O_3, the voltage across the anodization cell linearly increases with time, being measured by a HP 33120A multimeter and controlled by a software able to plot voltage vs time. When the aluminum is completely converted the slope of the curve changes because of the anodization process reaches the Al/Nb interface and the Nb is, therefore, converted into Nb_2O_5. About 1 nm of Al is converted in 2 nm of Al_2O_3 for each volt across the anodization cell, while the Nb conversion is 0.9 nm of Nb into 2.3 nm of Nb_2O_5.

Figure 5.3 and Appendix C.6 demonstrate a scheme and the experimental setup adopted at INRIM for the anodisation process.

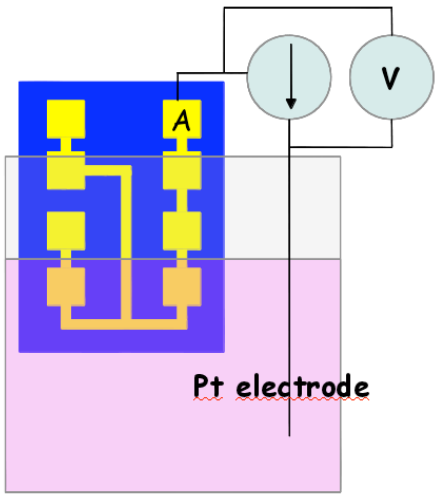

Figure 5.3. The anodization scheme. The sample is partially immersed in the anodic solution and connected via the *A* pad. A current is superimposed between the Pt electrode and the device, meanwhile the voltage is monitored in real-time.

The anodization process clearly entails an increment in the film volume, causing changes in the film [41] and inducing possible residual stress and cracks making shorts possible. Another drawback of this fabrication step is a possible under anodisation due to some current flows at the resist/Nb top interface, and unavoidably involving an uncontrolled reduction of the Josephson junction area [42]. For this reason, it is necessary to control the anodization current density and final voltage reached during the process. In this work, imposing anodisation current densities, J_c around 10 A/cm^2 and final voltages ranging from 30 to 50 V, no reductions on micrometer junction areas (5 x 5 μm^2 or more) and shorts were observed.

5.7 Deposition and patterning of metallic electrical contacts

The last step in the fabrication process necessary to complete the SNIS Josephson circuit essential to measure its I-V response in DC is the sputtering of a further niobium layer (Figure 5.1e). This metallic layer, called wiring, consists in a strip line connecting the top electrode of the junction to the measuring pads for electrical contacts. In case of arrays of Josephson junctions, the wiring connect them each other, in series.

After the umpteenth photolithographic step to define the wiring pattern, the device is inserted again into the sputtering chamber and its top surface is sputter-etched at 500 V for 5 min to remove the native oxide layer and possible contaminants incorporated during the entire fabrication process. The final Nb film is deposited with usual deposition parameters. If the sputter-etching process on top of the junction is not adequate, a series resistance appears on the I-V characteristic, degrading the supercurrent of the device. The wiring thickness has to be thick enough to exceed the difference between all the previous deposited films and the substrate level. The thickness is chosen evaluating the maximum relative step among layers avoiding breaking points along the strip line with a consequent electrical breakdown during measurements. Considering the sputtered trilayer previously deposited, the wiring ranges typically from 350 to 400 nm.

In the case of a single SNIS junction and/or small arrays (with 10 or 100 junctions series connected) the wiring strip line is also used to distribute the microwave signal through the whole device for its RF characterisation since the lower number of junctions allow to irradiate them without any further design structure for the signal distribution. On the other hand, considering devices with a higher number of Josephson junctions it is essential to distribute the external signal uniformly through the entire array by means of appropriate waveguide systems, as discussed in the next Chapter.

Part IV

EXPERIMENTAL RESULTS - SUPERCONDUCTING QUANTUM DEVICES BASED ON SNIS JUNCTIONS

Chapter 6

The Programmable SNIS Josephson Voltage Standard device

This Chapter reports the results relating to the realization of a 1 Volt binary-divided array based on 8192 overdamped SNIS Josephson junctions for programmable Josephson Voltage Standard (PJVS) application. A metrological hint concerning the Josephson Voltage Standard (JVS) is firstly reported.

6.1 Introduction

During the last century, the International System of Units (SI) changed its perspectives evolving from an artefact-based system to a system mainly based on fundamental constants and atomic processes. The modern units show major advantages compered to their artefact counterparts: they do not depend on any external parameters such as ambient conditions and, mainly, they do not drift their value with time. In addition, they can be simultaneously realized in laboratories all over the world, which strongly simplifies and improves the traceability of any measurements to primary standards. With the discovery of the Josephson effect (Section 1.3, [12]) and quantum Hall effect, two electrical quantum standards became available. As an important consequence, the worldwide consistency in the representation and maintenance of the electrical units and the electrical measurements based on them has improved a hundredfold in the last decade. The two quantum effects will also certainly play a major role in the next modernization of the SI when the last base unit still based on an artefact, the kilogram, is linked to fundamental constants.

6.2 The Josephson Voltage Standard

A voltage standard employing Josephson junction arrays has been adopted as an effective and suitable international standard for many years. Using properly designed cryogenic chips, laboratories around the world can reproduce voltage consistently with an accuracy of about few parts in a hundred million. The physics behind this standard is based on a very simple relation,

$$V = \frac{h}{2e} f \tag{6.1}$$

between two macroscopic quantities: the average voltage V (electrochemical potential difference) across the junction and the frequency f of the Josephson oscillation. $h/2e$ is a quantum mechanical fundamental constant, where h is the Planck constant and e is the electron charge in vacuum. In other words, it equates the quantum energy $h \cdot f$ and the classical electrostatic energy 2eV, both associated with the Cooper-pair dynamics.

In the voltage standard, the Josephson oscillation of relation 6.1 is phase-locked to an external microwave signal with a precisely determined frequency f, creating a Shapiro step with voltage V (at the first harmonic) [14]. The approximate 10^{-8} accuracy of the voltage standard is limited by the uncertainty in the experimental determination of the quantum mechanical constant.

The Equation 6.1 is also written as

$$V_n = n \frac{f}{K_J} \tag{6.2}$$

with n the step number and K_J is the so-called Josephson constant, given by

$$K_J = \frac{2e}{h} = \frac{1}{\Phi_0} \tag{6.3}$$

where e is the elementary charge, h the Planck constant, and Φ_0 the flux quantum. As this voltage is very small (about 145 μV for $f = 70$ GHz and $n = 1$), a voltage divider was required in the early days to enhance the reference voltages to the 1V level for practical use. But the voltage divider limited the precision, and its handling was rather complicated. For these reasons, the advantage of the quantum origin of the voltage could not be fully exploited. Therefore, an innovative idea was developed to increase the output voltage by connecting a certain number of Josephson junctions in series, and at the beginning of the 1980s important progress was achieved in reliable Josephson circuit technology.

Moreover, to be used as practical standards, the value of the Josephson constant K_J has to be known in SI units. In the SI, the electrical units are defined in terms of the mechanical base units metre, kilogram, and second through the definition

of the ampere and the assumption that electrical power and mechanical power are equivalent. To put the concept of the electrical units into practice, it is sufficient to realize two electrical units in terms of the metre, kilogram, and second. At present, the Farad and the Watt are the two chosen units, since they are the most accurately determined.

The best realizations of the Volt in the SI are about two orders of magnitude less accurate than the reproducibility of quantum standards based on the Josephson effects. Two electrical units realized in terms of the non-electrical SI units metre, kilogram, and second are needed to make the other electrical units measurable in the SI. With the Josephson effect, a fundamentally stable standard is available and thus it was realized that the world-wide consistency of electrical measurements could be improved by defining a conventional value for K_J.

The Comíte Consultatif d'Électricíte (CCE) was asked to recommend such values based on the data available. The value for K_J available by June 1988 in SI units was analysed and the following conventional values were proposed [43]: $K_{J-90} = 483597.9$ GHz/V. Relative uncertainty with respect to the SI of 4 $\times 10^{-7}$, was assigned to the value. The conventional value was accepted by all member states of the Metre Convention and became effective as of January 1, 1990.

Nowadays, robust, complex, three-dimensional integrated circuits having more than 300000 junctions and producing precision DC and AC voltages up to 10 V are available and reproducible. According to the nature of the Josephson junction barrier (oxide, metal or semiconductor) different I-V responses, either in DC or RF regime, are obtained, and as a consequence, a different behaviour determines their different application field, as reported in the two subsequent Sections.

6.2.1 The conventional DC Josephson Voltage Standard

In the 1970's, the voltage standard consisted of single junctions, which provided only small voltages, typically from 5 mV to 10 mV. Although the stability of the single-junction standard already exceeded the stability of the primary Weston cell standard, comparing the Weston cell to the Josephson standard required a precise voltage divider that was difficult to calibrate with the required accuracy. Therefore, attempts were made to increase the Josephson voltage output by connecting several junctions in series. The most ambitious project [44] used 20 junctions in series to produce a voltage of 100 mV with an uncertainty of a few parts in 10^9. Twenty individually adjustable current sources were needed to ensure that each junction remained on the appropriate voltage step. The difficulty of the tuning procedure prevented this approach from being widely implemented. The multiple bias problem was solved using a suggestion made by Levinsen [45] in 1977. Levinsen showed that a highly capacitive junction with a large McCumber parameter (SIS-like underdamped junction, with $\beta_c > 100$, being $\beta_c = (2eI_cR^2C)/\hbar$, Eq. 2.14) can generate an

hysteretic I-V curve (Figure 2.8), and when irradiated shows voltage steps that cross the zero-current axis, hence their name of zero-crossing steps (Figure 6.1).

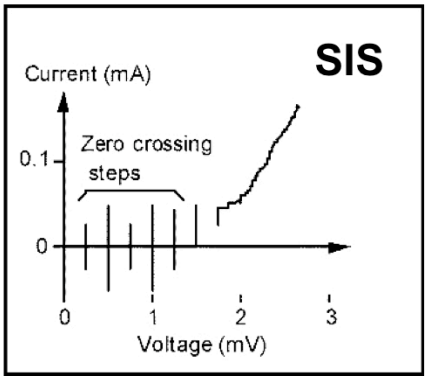

Figure 6.1. Current-voltage characteristic of an underdamped Josephson junction under microwave irradiation, with quantized zero-crossing voltage steps.

The lack of stable regions between the first few steps shows that the voltage of the junction must be quantized, at least for small current bias. After the problems of junction stability and microwave power distribution were solved, the first large array based on the Levinsen idea was fabricated [46], leading to the first practical 1V Josephson voltage standard (JVS) in 1985 [47, 48]. Improvements in the superconductive integrated-circuit technology allowed the fabrication of the first 10 V array in 1987 [49]. This array consisted of 14484 junctions that generated about 150000 quantized voltage steps when irradiated at 70 GHz, spanning the range between −10 V and 10 V. The 10 V JVS was then implemented in many National Metrology Institutes (NMI). The accuracy of these standards is determined by international comparisons between the transportable Josephson system of the Bureau International des Poids et Mesures (BIPM) and those of the NMI. Typically, the difference between two quantum standards is less than 1 part in 10^9 at a voltage of 10 V. The best comparisons, however, have uncertainties on the order of a few parts in 10^{11} [50].

Nowadays, all the SIS junctions for conventional JVS systems for application in voltage metrology are fabricated with planar $Nb/Al_2O_3/Nb$ thin-film structures. The most important condition for accurate measurements using a conventional JVS is the stability of the phase lock between the microwave current and the Josephson oscillator. This phase lock must be strong enough to prevent the array from frequently jumping from one voltage step to another during the course of a calibration. On the basis of the McCumber model, Kautz analyzed how the various junction parameters influence the stability of the phase lock with regard to chaos, thermal noise and uniformity of the current distribution (see [51, 52] for a review).

Therefore, the stability of the array is caught in a region of the parameter space

between instabilities due to thermal noise or chaos. However, an optimized design can lead to excellent stability that is sufficient for most DC calibrations.

For this 10 V array design, 20208 junctions form a series array, as shown in the schematic of Figure 6.2. The microwave power is collected by a finline antenna, split 16 ways, and injected into 16 segments, each containing 1263 junctions distributed along the micro-stripline. The most important consideration in the design of the array is that each junction must receive the same microwave power in order to develop the largest possible zero-crossing steps. The maximum number of junctions per segment is limited by the attenuation of the stripline. Microwave reflection at the end of each stripline is suppressed by a distributed lossy load. To meet the appropriate packaging density, the striplines are folded, taking into account that the microwave bend radius has a minimum value of three times the stripline width. All the segments are connected in series to produce the maximum DC voltage. The DC voltage is measured across superconducting pads placed at the edge of the chip via low pass filters.

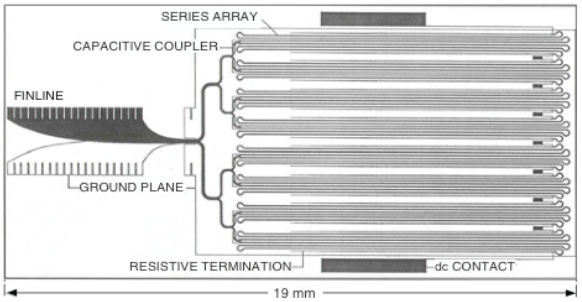

Figure 6.2. Scheme of a typical 10 V NIST (National Institute of Standards and Technology) array.

The most important application of the conventional Josephson voltage standard is the calibration of Zener-diode-based DC reference standards. Zener standards are convenient transportable voltage standards that are used to maintain the traceability chain to the primary Josephson standard [53] at 1.018 V and 10 V. The stability of the 10 V output of a Zener is around 10^{-6} per year. By carefully controlling the environmental conditions and by modelling temporal drift, output voltages can be predictable over periods of several weeks to within a few parts in 10^8. Ultimately, the uncertainty of the output voltage of a Zener standard is limited by a $1/f$ noise floor having a value between two and ten parts in 10^9 [54, 55]. Nevertheless, by using great care, standard uncertainties on the order of a few parts in 10^8 have been achieved by using Zeners as travelling standards in international comparisons (see [56, 57] and references therein).

Another important application of the conventional Josephson voltage standard

is the calibration and linearity measurement of high precision digital voltmeters.

6.2.2 The Programmable Josephson Voltage Standards

Conventional Josephson voltage standards have been operated very successfully for DC applications since the mid 1980s. However, these Josephson array voltage standards do not enable switching rapidly and reliably among different interest voltage levels, due to their overlapping, metastable constant-voltage steps. The increasing interest in rapidly switching arrays and in highly precise AC voltages has stimulated several research activities to develop measurement tools based on Josephson arrays to meet these requirements. One approach is the Programmable Josephson Voltage Standard (PJVS) first suggested by Hamilton et al. at National Institute of Standards and Technology (NIST) in 1995 [58]. In principle, it is a Josephson multi-bit digital-to-analog converter based on a series array of overdamped Josephson junctions divided into a binary sequence of independently biased smaller arrays. Modern versions contain more than 100000 junctions for output voltages up to 10 V.

PJVS are based on series arrays of overdamped junctions showing a non-hysteretic I-V characteristic (Figure 2.8). The current-voltage characteristic remains single-valued under microwave operation (Figure 6.3a). The series array of M total junctions is divided into smaller independently biased programmable segments (Figure 6.3b). The number of junctions per segment often follows a binary sequence, the so-called binary-divided arrays. The output voltage $V = nM\Phi_0 f$ is given by digitally programming the junction step number n for the junctions in each segment (typically is n = -1, 0, +1). Each constant-voltage step between -M and +M can be selected by suitable programming of the different segments. A fast bias electronics enables switching times of a few tens of nanoseconds [59]. The number of junctions necessary to attain a given voltage is increased by a factor of five compared with conventional SIS arrays, as PJVS are typically operated on the first-order constant-voltage step instead of the fifth on for SIS arrays.

Overdamped Josephson junctions are needed for PJVS. Hamilton et al. demonstrated a PJVS for the first time using externally shunted SIS junctions [58]. In an array consisting of 8192, 2048 junctions were operated at 75 GHz and delivered an output voltage of about 300 mV. As a design for externally shunted SIS junctions is rather complex and challenging, and the critical current and consequently the step width of these arrays are limited to a few hundred microamperes because of design restrictions, other junction types have subsequently been investigated. Calculations by Kautz gave important hints for the realization of optimized metallic-barrier Josephson junctions [34].

Most currently fabricated series arrays are based on one of three different junction types: SNS junctions, SINIS junctions, and SI'S junctions, the barrier of which

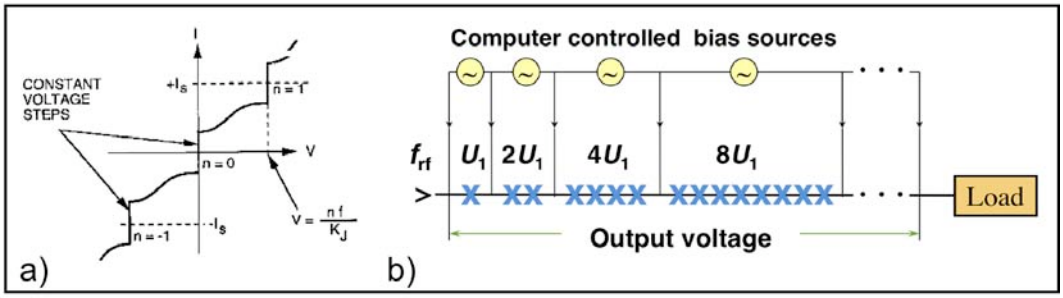

Figure 6.3. (a) Current-voltage characteristic of an overdamped Josephson junction under microwave irradiation. The microwave power is set to equalize the widths of zeroth and first constant-voltage steps. Quantized voltage steps of a SNS junction under irradiation; (b) Schematic design of a programmable JVS based on binary-divided series array of Josephson junctions shown as 'X'.

consists of a semiconductor such a Si doped with a metal and being near a metal-insulator transition. The low characteristic voltage V_c ($V_c = I_c \cdot R_n$, being I_c the critical current and R_n the normal state resistance of the junction) of SNS junctions leads to operating frequencies around 15 GHz. The V_c of SINIS and SI'S junctions can be tuned on the other hand over a wide range, enabling operation at frequencies either around 15 GHz or around 70 GHz.

In 1997 PTB started to investigate SINIS multilayer junctions fabricating small arrays [22], and shortly after, 1 V arrays [60] and providing a 10 V device in 2000 [61]. This success was partially caused by the use of 70 GHz junctions and by an active contribution of the junctions embedded into a low-impedance microstriplines. The arrays consisted of 8192 junctions (1 V) and 69120 junctions (10 V), respectively. However, the SINIS technology showed a seriuos drawback. Measurements of many arrays showed that a few junctions of SINIS series arrays are often missing (i.e. they exhibit a superconducting short). SINIS junctions seem to be very sensitive to some particular steps during fabrication, probably due to their very thin insulating oxide layers. This problems drove the research towards more robust barrier materials. A very promising material was investigated at NIST consisting of an amorphous silicon layer doped with a metal such a niobium [62] and in collaboration with the PTB a 1 V and a programmable 10 V arrays were realized.

Finally, the present state of the art of programmable and AC Josephson voltage standards include PJVS based on SINIS technology operating at 70 GHz [63], SNS Nb/Nb_x Si_{1-x}/Nb arrays operating at 20 or 70 GHz with 1 and 10 V output amplitudes [64, 65], and series arrays with up to 500 000 NbN junctions irradiated at 10–20 GHz, capable of generating voltages up to 17 V [66]. NbN based junctions, with TiN barriers have been used to realize DACs with 10 bits and amplitudes above 10 V operated in a cryocooler at 10 K [67].

In the last years, INRIM gave an important contribution to the development of a programmable Josephson Voltage Standards based on overdamped SNIS junctions, as a valide alternative to the others technologies. This research has been performed in part during this PhD activity, as reported in the following sections.

6.3 The SNIS Programmable Josephson Voltage Standard: the project

6.3.1 The "JoSy" IMERA Project

In metrology, quantum standards are most valuable as they are always reliable and do not depend on ambient conditions like temperature, air pressure or humidity. This feature allows calibrating with very high precision and ensures comparability and traceability. Based on a macroscopic quantum effect, the Josephson Effect, voltages can be traced to a frequency, one of the best known standards as being linked to atomic clocks. Thus Josephson voltage standards can reproduce voltages with very good uncertainties. Furthermore, voltage is one of the units which is used in experiments to really measure differences making voltage appealing for many other standards. Recent developments and progress in programmable Josephson array fabrication have reached and opened up fields of wide range of new applications.

The Josephson effect is well established at most National Metrological Institutes (NMIs) worldwide for the measurement of DC voltage. Quantum standards for AC metrology are still a research topic with measurement not yet demonstrated over an adequate range of voltage and frequency. For this purpose, from 2008 to 2011 the main European National Metrological Institutes (NMI) partecipated at the IMERA Plus Programme to introduce quantum-based measurement systems into AC metrology. This represents the first step towards establishing intrinsically referenced AC standards on the workshop floor providing much faster calibrations while at the same time ensuring much better uncertainties to support the electronic measurement and test equipment used in research and development. It addresses the frequency band from sub 1 Hz to 1 MHz where the majority of high performance measurement and control applications are to be found (Figure 6.4). The project aimed to develop a new generation of quantum voltage standards providing much faster calibrations while at the same time ensuring much better uncertainties.

The research within this EURAMET joint research project, called "JoSy" (Next generation of quantum voltage systems for wide range applications), has received funding from the European Union Seventh Framework Programme [68].

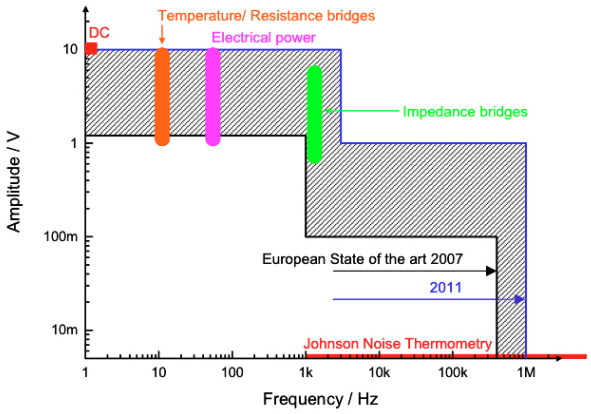

Figure 6.4. Voltage and frequency ranges addressed in this project compared to the current state of the art in Europe. The coloured areas illustrate the most important frequency and voltage ranges of various AC measurements.

6.3.2 The INRIM contribution

In the framework of the "JoSy" European project, INRIM joined the WP2 where the activities were focused on the fabrication of binary-divided arrays consisting of 8192 Josephson junctions as a fundamental component of quantum voltage standards.

The INRIM task encompassed investigations of new junction types with two aims: a) reducing the complexity of the fabrication process for voltage standard series arrays and b) testing new junction types suitable for operation above 4.2 K. INRIM investigated a new junction types based on Nb/Al-AlO_x/Nb trilayers, and the target was the fabrication and testing of series arrays for generating voltages up to the 1 V level.

6.3.3 Preliminary devices: fabrication and characterisation

The earlier research in the IMERA "JoSy" project was leaded before this PhD reasearch and focused on the study and the realization of preliminary devices with a lower number of SNIS junctions. Several samples were realized by varying both the aluminum thickness and the oxidation exposure of the tunneling barrier, following the standard INRIM process. SNIS junctions in single and in small arrays (including 10 and 100 junctions) configuration were realized, with dimensions reanging from 5 x 5 μm^2 and 5 x 10 μm^2 up to 10 x 10 μm^2.

As a further step, INRIM has adapted its fabrication process to the complete circuits of a 1600 SNIS junction array with coupled fin-line antenna according to the standard PTB fabrication process. Two fundamental features had to be fulfilled considering the design of a Josephson Voltage Standard: each junction must be DC

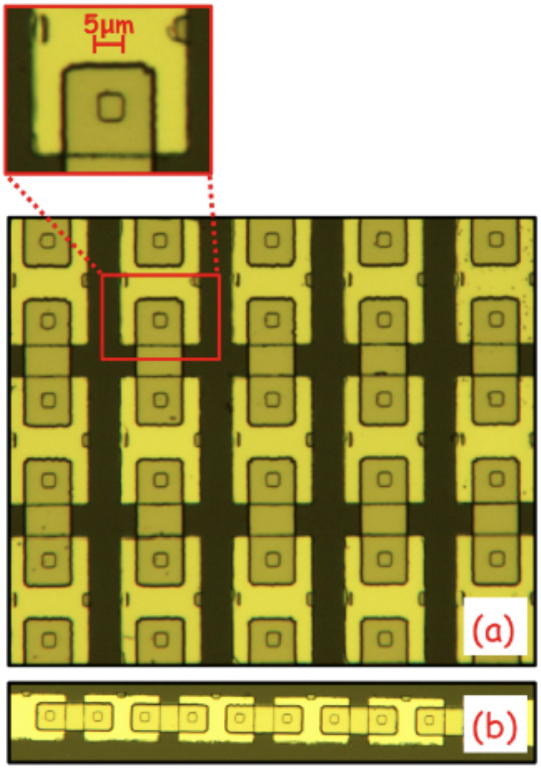

Figure 6.5. Optical microscope images of arrays of 100 (a) and 10 (b) SNIS junctions, series-connected through the wiring layer.

series connected, and the entire array must be uniformly irradiated by the external microwave signal. Figure 6.6 shows the CAD design of the 1600 JJs array.

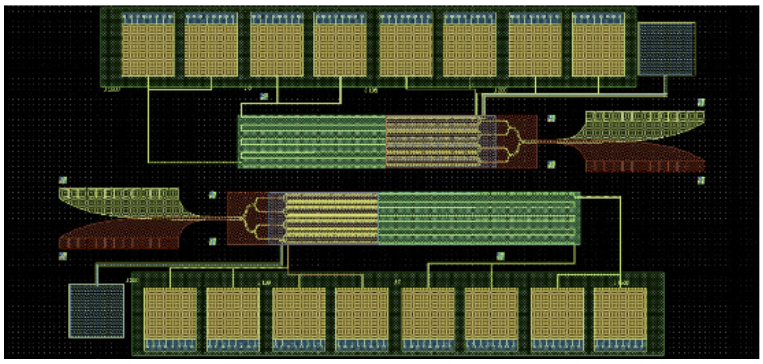

Figure 6.6. CAD design of 1600 SNIS junctions array.

The microwave signal is splitted in eight parallel stripline paths, with 200 junctions each. Each stripline path ends by a conducting load to avoid standing waves into the circuit. Low pass filters prevent the microwaves from reach the DC pads and four DC blocks working as capacitors avoid electrical shorting of the DC series connection of the tunnel junctions via the microwave power dividing stripline circuit (Figure 6.7).

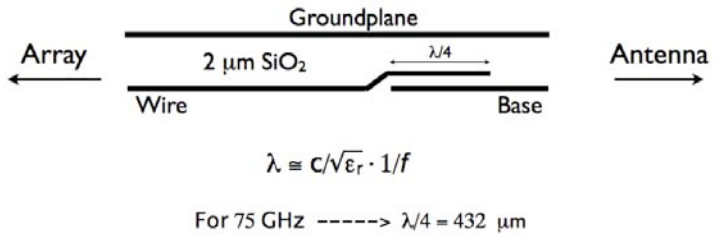

Figure 6.7. Scheme of DC blocks.

Some sub-array prototypes containing 200 and 400 junctions were fabricated. The deposition of an SiO_2 dielectric layer by Plasma Enhanced Chemical Vapour Depostion (PECVD) on top of the patterned trilayers were made at PTB for some samples, and the DC test of arrays accomplished in INRIM showed reproducible run-to-run and homogeneous parameter distribution.

The PTB circuit layout were redesigned in order to improve some critical fabrication steps of the INRIM process, such as the replacement of an aluminum anodization grid, which was initially etched by ion milling, by a niobium grid, which was then patterned more conveniently by reactive ion etching. Then INRIM realized in cooperation with PTB circuits containing 1600 SNIS junctions of 5×5 μm^2 size embedded in PTB's 70 GHz microwave design. Current densities span from 1 kA/cm^2 to 50 kA/cm^2 and characteristic voltages from 100 μV to 700 μV at 4.2 K depending on the thickness and the oxidation parameters of the aluminium film, respectively. DC tests showed a low spreads of the electrical parameters between 5% and 10%, mainly related to limitations of the fabrication process, and a good reproducibility of the parameters was additionally measured, but the homogeneous microwave distribution within the array was not satisfying. As additional work would have been needed for optimizing the matching of the microwave to the junctions, to modify the original project plan and to go directly to the development of programmable 1 V arrays.

6.4 The binary divided SNIS array for 1 Volt Josephson Voltage Standard

Therefore, a 1 V design based on experience of PTB was developed within close cooperation between INRIM and PTB and a 1 V binary-divided arrays consisting of 8192 SNIS Josephson junctions were successfully fabricated, and the main concerning results optained in the context of this PhD thesis are reported in the following.

6.4.1 Fabrication process

The preliminary tests (Section 6.3.3) were focused on to establish the fabrication parameters and, consequently, the main electrical parameters for the development of the 1 Volt SNIS device.

The starting design was the 1 V SINIS JVS commercially used all over the world and made by PTB [64]. The CAD drawing (Figure 6.8) has been modified respect to the SNIS technology by changing the RF microstripline width, and adapting the junction size to the current density of SNIS junctions. A good compromise between large SINIS areas and small SNIS ones was reached by drawing junctions of 5 x 12 μm^2 (Figure 6.9), more than two times compared to the classical SNISs (5 x 5 μm^2) employed in the preliminary tests. Each wafer included 21 1V SNIS JVS devices.

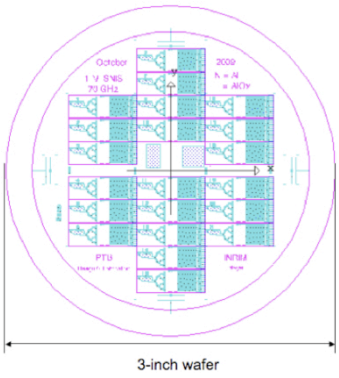

Figure 6.8. CAD design of the 1 V SNIS PJVS, with 21 devices.

For this purpose several SNIS trilayers were deposited at INRIM on eight 3-inch Si/SiO_2 wafers with high resistivity, used as substrates. The trilayer were sputtered with 150 nm Nb base electrode, using thicknesses of the Al layer in the range between 70 nm and 100 nm, and oxidation dose ranging from 160 Pa · s up to 450 Pa · s in

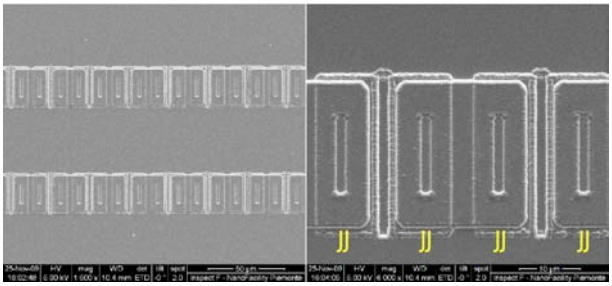

Figure 6.9. Scanning Electron Microscope (SEM) images of SNIS junctions included into the 1 V JVS device.

order to center the best electrical parameters matching better the RF coupling for the JVS device.

The further fabrication process was performed at PTB adapting the technology previously used for series arrays of Nb_xSi_{1-x} junctions [64], as shown in Figure 6.10.

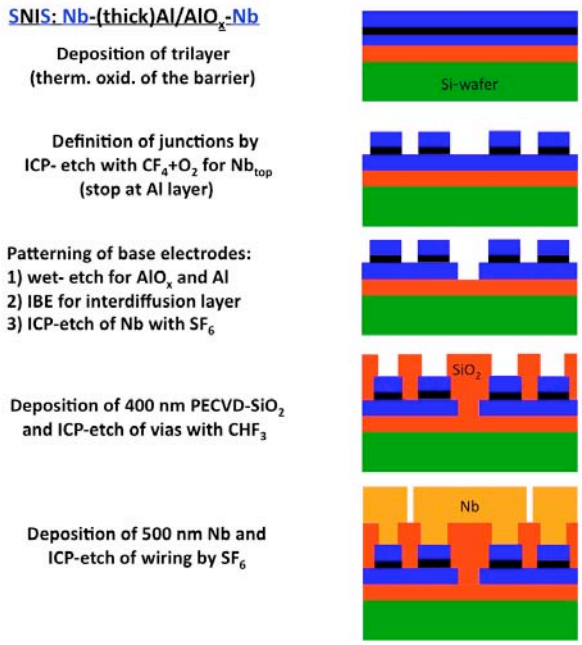

Figure 6.10. PTB process adapted to the INRIM trilayer.

The patterning of the device was carried out by optical lithography, while some other process steps were performed adapting the PTB facilities to the SNIS technology. In fact, processing different multilayer structures (SNIS vs SINIS) implies, of course, a variation in the sequence and typology of the fabrication steps.

The first step was the definition of the areas by removing the Nb top electrode by Inductively Coupled Plasma (ICP) etching with SF_6 gas at high RF power (300 W). Following, the definition of the base electrode with a larger area including two SNIS junctions. The unprotected aluminum layer was removed by wet etching with a solution of nitric, ortophosphoric and acetic acids, and a subsequent ICP with SF_6 is carried out to etch base niobium. The insulating layer, 400 nm of SiO_2, was then deposited by PECVD in two steps, to avoid pinholes (and consequently short-circuits between electrodes) all over the device, and some vias for the wiring contacts were patterned and generated by an ICP step in CHF_3.

A further Nb wiring was sputtered with a thickness of about 350 nm, and patterned by ICP, completing the DC part of the circuit.

Since the higher number of Josephson junctions, it is essential to distribute the external signal uniformly through the entire array. Different methods are implemented and applied to the microwave irradiation, like Fabry-Perot resonators or coplanar and strip line waveguides. In this case, a strip line waveguide was designed and employed because easily adaptable to the SNIS technology.

The strip line is a structure made by two superconducting layers separated by a dielectric and completed by a normal metal layer series connected, as demonstrated in Figure 6.11.

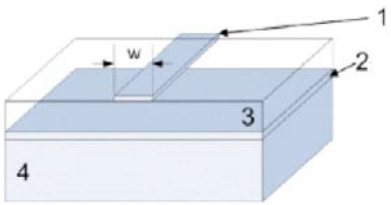

Figure 6.11. Schematic of a standard microstrip line structure. 1: superconducting niobium strip, 2: superconducting ground plane, 3: dielectric layer SiO_2, 4: silicon substrate.

As the dielectric layer in the micro strip line circuits, a silicon dioxide was deposited after the wiring. For this purpose, the suitable dielectric needs purity, defects free and a thickness around 1.5 - 2 μm, in order to avoid dissipations of the radiation signal and a better propagation of the microwave. For this purpose, the insulating SiO_2 layer was deposited by Plasma Enhanced Chemical Vapour Deposition (PECVD).

A further superconducting Nb layer called “ground plane” is deposited on top of the dielectric film, with a thickness of about 300 nm. A further resistive layer of gold/palladium (Au/Pd) normal metal film is sputtered and connected with the microstrip line, to dissipate the entire microwave to avoid reflections at the end of

the line. Possible reflections could cause a standing of the wave along the junction with different amplitude of the signal.

The last steps included the wet etching of the SiO_2 to clean the measurements pads, the cut of the wafer separating the 21 single devices, and finally the glowing of each unit on the carrier used for the electrical characterisation (Figure 6.12), and in Figure 6.13 [69] the detail of the 1 V SNIS Programmable Josephson Voltage Standard chip.

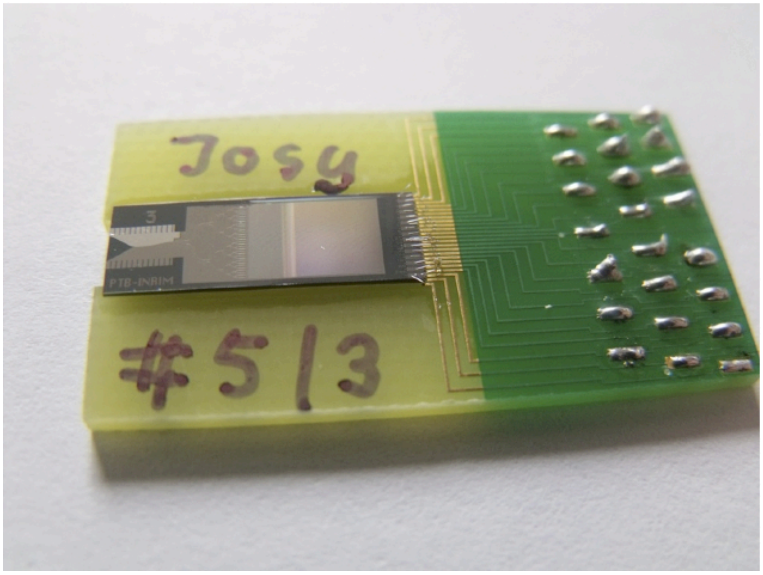

Figure 6.12. 1 V SNIS Programmable Josephson Voltage Standard on the carrier.

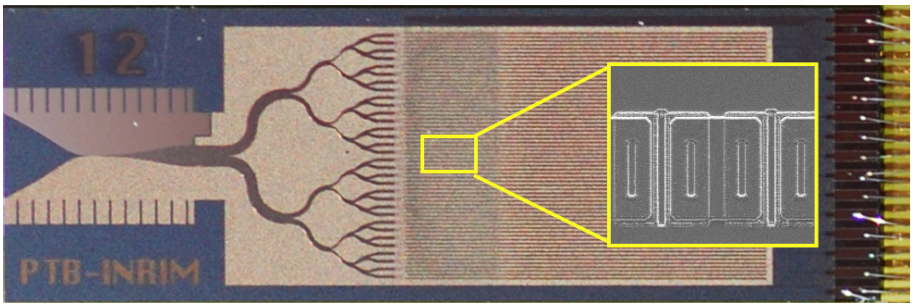

Figure 6.13. Image of the 1 V SNIS Programmable Josephson Voltage Standard chip (0.5 cm x 1.5 cm). In the inset, the detail of junctions, as reported in Figure 6.9.

6.4.2 Electrical characterisation

As already mentioned in Chapter 3, SNIS junctions can be fabricated over a wide range of electrical parameters, showing critical current density values J_c from less than 1 kA/cm^2 up to several tens of kA/cm^2, and characteristic voltage $V_c = I_c \cdot R_n$ easily tuned from 0.1 to 0.7 mV at 4.2 K (I_c being the critical current and R_n the normal state resistance, respectively). J_c is mainly controlled by the insulating layer thickness, while the characteristic voltage V_c can be controlled by the Nb/Al bilayer superconductive properties: it has been shown that the change of Nb energy gap and of proximity induced minigap in aluminum, obtained by varying the thickness of both layers, affect V_c of the junctions [70].

The binary-divided arrays have been therefore electrically characterised by means of the experimental set-up described in Appendix A.1. The DC measurements of the 8192 JJs arrays showed J_c values ranging from 3 to 20 kA/cm^2, and V_c from 0.27 up to 0.6 mV, depending on the set of the fabrication parameters used during the trilayer deposition. A small spread of I_c, of about 5 – 10% for the majority of samples across the array area of 1.5 mm × 4.5 mm, points to homogeneous SNIS junctions and a reliable fabrication technology. The DC I-V characteristic related to a 8192 JJs series array is shown in Figure 6.14, and the overdamped behaviour was maintained by trimming the fabrication parameters.

Figure 6.14. DC I-V characteristic of a 8192 junction series-connected PJVS array.

In order to observe a regular RF behavior of the junctions irradiated in the frequency range around 70 GHz, their hysteresis defined as $1 - I_r/I_c$, where I_r is the return current, had to be lower than 30%. Junctions with higher values of this parameter showed reduced Shapiro steps with chaotic features. One explanation for this trend is to be found in the change of the junction behavior as a function of the hysteresis from SNS-like to SIS-like, along with, in the latter case, a junction plasma frequency higher than necessary to prevent transition to chaos [71].

Concerning the step amplitude, the optimal value for the $n = 1$ step in overdamped junctions is obtained [34] when $f_{drive} \approx f_c = 2e/hV_c$, which gives values about 0.15 mV for $f_{drive} = 70$ GHz. However [72], a step of nth order is enhanced for $nf_{drive} = f_c$, i.e. higher order harmonic steps are enhanced in junctions with large V_c.

Binary-divided arrays are typically operated with the $n = 0$ and 1 steps equalized under microwave irradiation. A step width of about 1 mA is a good benchmark for current margins in metrological AC applications. This behavior was observed for SNIS arrays showing the lowest values of V_c with an $n = 1$ step of usable amplitude (1 mA or more) (Figure 6.15).

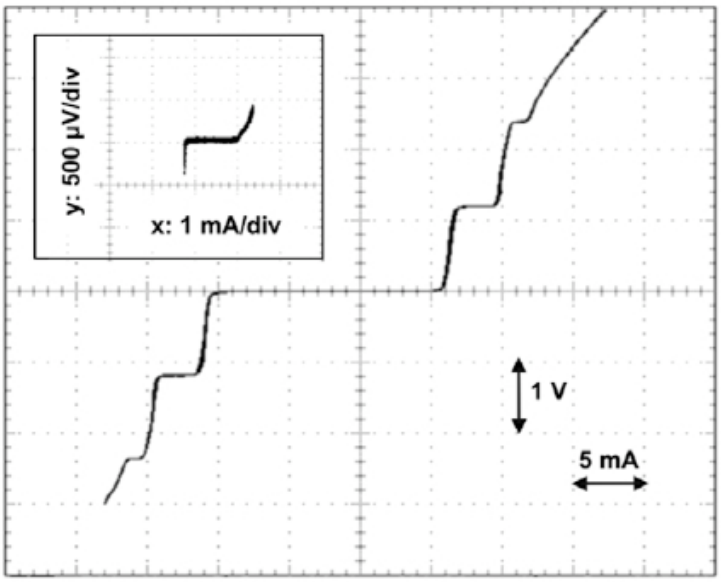

Figure 6.15. I-V characteristic of a 1 V PJVS with 8192 SNIS junctions under microwave irradiation at 70.29 GHz. The inset shows the 1 V step with high resolution. Junction parameters: $I_c = 11$ mA, $V_c = 0.270$ mV, $T = 4.2$ K.

The first-order steps are reduced in junctions with $V_c \geq 0.3$ mV, i.e. $f_c \gg f_{drive}$. However in the latter case, steps corresponding to second, third and even fourth harmonics of the fundamental drive frequency were observed at 2.473, 3.709 and 4.947 V (Figure 6.16). The choice of $f_{drive} = f_c$ is regarded as the best operating condition for Josephson binary arrays, since it ensures the minimal demand of microwave power for equal and maximized 0 and ± 1 step amplitude. For many applications the step $n = 0$ is needed to establish zero output voltage.

Depending on the value of V_c it was also possible for SNIS arrays to attain a condition where two adjacent steps, first and second or second and third, were wide and nearly equal. Of course, higher order steps require an increased microwave

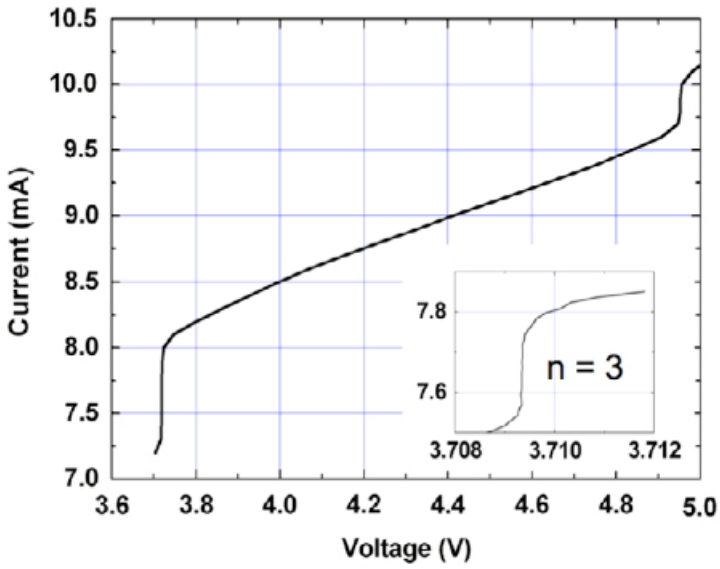

Figure 6.16. Binary-divided array of 8192 SNIS junctions irradiated by 73.00 GHz microwaves at a power level of about 100 mW, showing $n = 3$ and $n = 4$ steps at $V = 3.709$ V and 4.947 V, respectively. The step at 3.709 V may be suitable for precision measurements. The step at 4.947 V is not maximized due to microwave power limitations. The inset shows the $n = 3$ step with high resolution.

power to the junctions, which can be easily estimated assuming a Bessel function behavior (Figure 6.17). In particular, the condition where the steps $n = 0$, 1 and 2 are all optimized requires a small increase of the power, with respect to that for optimized steps $n = 0$ and 1.

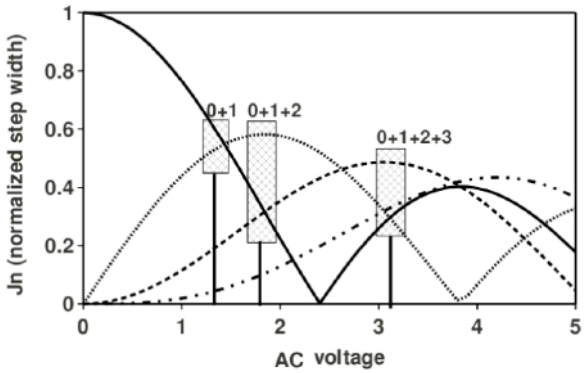

Figure 6.17. Bessel function behavior for $n = 0 - 3$. Conditions for optimal 0 and 1, 0, 1 and 2 and also 0, 1, 2 and 3 are indicated.

Experimentally, for a radiation frequency of 70 GHz, an RF power of about 40

mW was delivered at the input flange of the waveguide cryoprobe for equal first and second steps (Figure 6.18), to be compared with values of 20 – 25 mW for the case of $n = 0$ and 1. To observe steps $n = 3$ and 4 the output power of the Gunn diode was not sufficient and a 100 mW power microwave amplifier was used. The V_c of this array was 0.3 mV.

Because $V = \mathrm{N}n(h/2e)\, f_{drive}$, where N is the number of series connected junctions and n is the step order, this results in the possibility of using an array where half the number of junctions provides the same voltage output, with the same resolution, by realizing a suitable biasing electronics for the first and second and zeroth steps.

The step amplitudes were measured with oscilloscope techniques and with submicrovolt techniques to confirm $n = 1$ step flatness at metrological level (Figure 6.18).

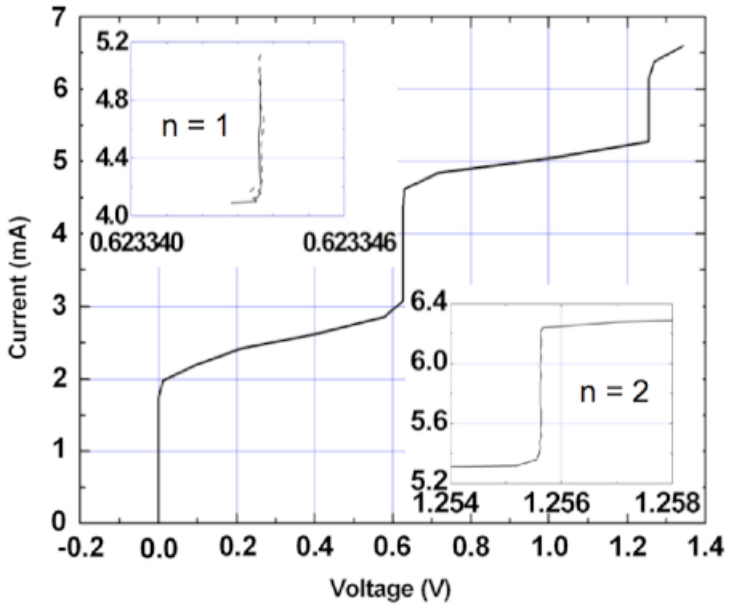

Figure 6.18. Part of a binary-divided array consisting of 4096 SNIS junctions irradiated by a 73 GHz microwave. The microwave power, 40 mW at the input flange, has been optimized to have equal and wide (1 mA) first and second steps. The insets show two different measurements of the step profiles with higher resolution. The $n = 1$ step was traced with a precision DVM (dashed) and by a direct comparison to a conventional Josephson voltage standard (continuous).

The high values of V_c measured at 4.2 K on some devices, alternatively, allow their operation at higher order steps or at increased temperature above the liquid helium level in the gas. Previous experiments on single junctions and small arrays of 10 junctions demonstrated the operation up to temperatures near the critical

temperature of the junctions [30].

Figure 6.19 shows a step at 1.25 V, 0.25 mA wide, measured for the first time on a Nb-based junction series array at $T = 6.3$ K. The characteristic parameters of the measured array were $I_c = 4.77$ mA and $V_c = 0.48$ mV at 4.2 K. The evaluated I_c and V_c at the operating temperatures were 2.2 mA and 0.2 mV. Wider steps, 0.5 to 1 mA, have been measured up to 7.2 K on subsections of the array.

These measurements have been carried out in gas, without any stabilization of the temperature, and therefore it is possible that the results will be improved by using a cryocooler setup.

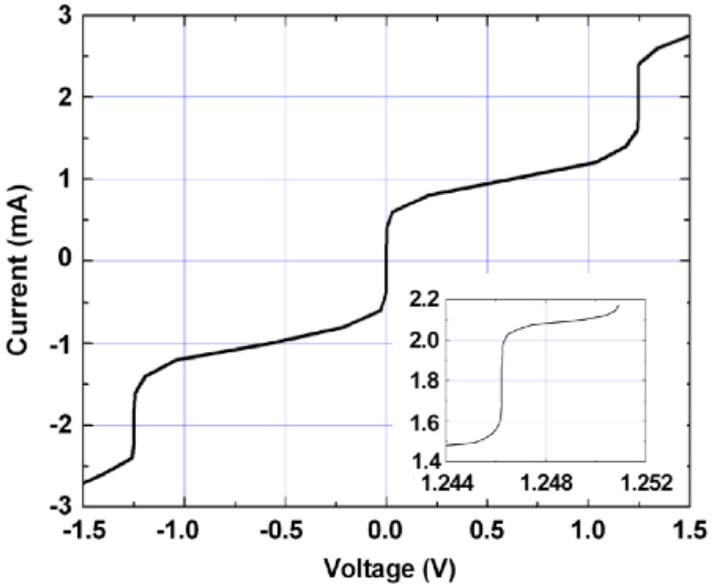

Figure 6.19. Voltage step at 1.25 V measured at $T = 6.3$ K on a binary array of 8192 Josephson junctions. The inset shows the detail of the $n = 1$ step, which is 0.3 mA wide.

6.5 Conclusions

In conclusion, a binary-divided Programmable Josephson Voltage Standard (PJVS) based on 8192 SNIS Josephson junctions (5 x 12 μm^2) connected in series has been successfully realized to reproduce 1 Volt, as output voltage at 4.2 K.

By the RF electrical characterization, stable quantised voltage steps of different order have been measured due to the SNIS high characteristic voltage values, and emphasizing the possibility to operate at higher quantized order steps than usual ones ($n = 0$ and $n = \pm 1$). Their large amplitude in current makes this technology

appealing for the development of a new generation of JVS. Therefore, the same output voltage provided through the conventional PJVS technologies (i.e. SINIS) has been achieved by a lower number of SNIS junctions (half array).

Finally, due to their large characteristic voltage the arrays could be also operated at higher order steps as well as at temperatures in the range 6.5 – 7 K suitable for cryocoolers in the 10 K class.

Chapter 7

The Subμ SNIS Josephson junction

This Chapter reports experimental results concerning Nb/Al-AlO$_x$/Nb SNIS junctions fabricated in the submicrometer scale exploiting the Electron Beam Lithography (EBL), as nanolithographic technique to define the effective area of junctions.

7.1 Introduction

The demand of reducing Josephson junction dimensions down to sub-micrometer scale occurs in several application fields. In superconducting digital electronics the rising of clock frequency, a reduction of capacitance values and a higher integration density for electronic circuits are some of the main requirements strictly linked to lower dimensions. In voltage standard metrology, the characteristic voltage V_c ($V_c = I_c \cdot R_n$, being I_c the critical current and R_n the normal resistance of the junction) determines the microwave optimal drive frequency thus the step voltage and the number of junctions needed to define the maximum output voltage. In this context an increase of critical current density could entail a gain in terms of size reduction. Sub-micron Josephson junctions are especially required in pulse driven arrays employed in the Josephson arbitrary waveform synthesizer, where a train of pulses is used to generate AC voltages with fundamental accuracy. The most reliable solution to guarantee pulse operation is to reduce array dimensions below a length shorter than λ/8, where λ is the wavelength of the microwave signal [73, 74].

As already reported, the overdamped Nb/Al-AlO$_x$/Nb SNIS Josephson junctions exhibit high values of critical current density and characteristic voltage, and the realization of sub-micron junctions according to the conventional INRIM fabrication process (Chapter 5), added to their peculiar features, could represent an interesting challenge making these devices appealing both for metrological applications and

digital electronics.

7.2 The subμ SNIS fabrication process

The fabrication process implemented and optimized during this thesis for the realization of subμm SNIS junctions retraces the same fabrication steps implemented for the SNIS junctions at the micrometer scale (Chapter 5), unlike from the patterning step to define the junction area, wherein the optical lithography was substituted by the Electron Beam Lithography (EBL) technique to further reduce the junction size. For this reason, this Chapter will be focused on the EBL technique (Section 7.2.1) and its employment in the patterning of submicrometer SNIS junctions (for all the other steps refer to the Chapter 5).

The main subμ process steps can be schematized as in Figure 7.1.

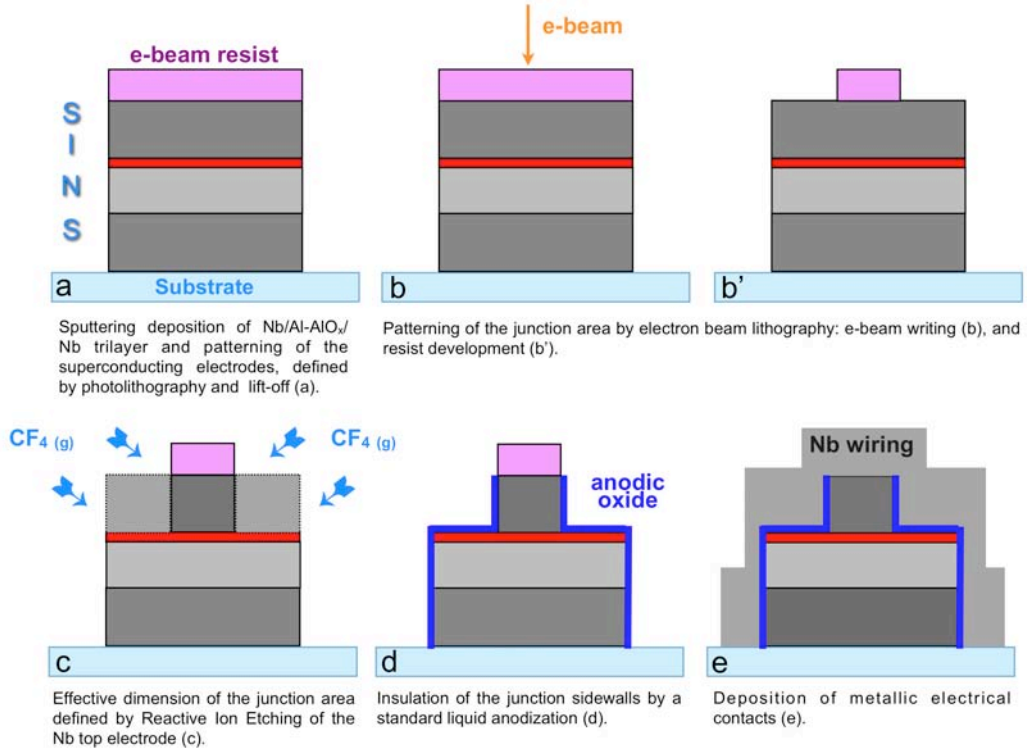

Figure 7.1. Main fabrication steps of subμm SNIS junctions.

7.2.1 The Electron Beam Lithography technique

7.2.1.1 Introduction

Electron beam lithography (often abbreviated as e-beam lithography or with the acronym EBL) is the practice of emitting a beam of electrons ("exposing") in a patterned fashion across a surface covered with a film (called the resist), and of selectively removing either exposed or non-exposed regions of the resist ("developing"). The purpose, as with photolithography, is to create very small structures in the resist that can subsequently be transferred to the substrate material, often by etching or by thin film deposition. Originally developed for manufacturing integrated circuits, nowadays it is also used for creating nanotechnology architectures.

The primary advantage of electron beam lithography is the overcoming of the diffraction limit of light, allowing the realization of features in the nanometer regime. This form of mask-less lithography has found wide usage in photomask-making used in photolithography (see Appendix B.7 as an example process used in SNIS device fabrication), low-volume production of semiconductor components, and research and development.

One of the key limitation of electron beam lithography is throughput, i.e., the very long time it takes to expose an entire silicon wafer or glass substrate. A long exposure time leaves the user vulnerable to beam drift or instability which may occur during the exposure. Also, the turn-around time for reworking or re-design is lengthened unnecessarily if the pattern is not being changed the second time.

Electron beam lithography systems used in commercial applications are dedicated e-beam writing systems that are very expensive. Anyway, for research applications, it is very common to convert an electron microscope into an electron beam lithography system using a relatively low cost accessory. Such converted systems have produced linewidths of $\sim$ 20 nm since at least 1990, while current dedicated systems have produced linewidths on the order of 10 nm or smaller.

Electron beam lithography systems can be classified according to both beam shape and beam deflection strategy. Older systems used Gaussian-shaped beams and scanned these beams in a raster fashion. Newer systems use shaped beams, which may be deflected to various positions in the writing field (this is also known as vector scan).

7.2.1.2 FEI Quanta™ 3D system at NanoFacility Piemonte

The Quanta™3D FEG installed at NanoFacility Piemonte (Figure 7.2) at INRIM is a versatile high-resolution, low-vacuum commercial SEM/FIB for 2D and 3D material characterization and analysis. This microscope is, at this moment, equipped with the Nanometer Pattern Generator System (NPGS) from J.C. Nabity, able to convert the SEM/FIB in a fully operative dual-beam lithography system. By means

of field-emission electron source technology the system delivers clear and sharp electron imaging combined with a reliable setup for high resolution lithography. Featuring three chamber vacuum modes, high-vacuum, low-vacuum and ESEM^{TM}, it accommodates a wide range of samples for both imaging and nanofabrication.

Figure 7.2. Picture of NanoFacility Piemonte Laboratory at INRIM. Left side: Quanta^{TM}3D FEG. Right side: Inspect F^{TM}FEG equipped with Energy Dispersive X-ray Spectroscopy (EDS) from EDAX.

7.2.1.3 Standard EBL process overview

The minimum time to expose a certain area for a given dose is expressed by the following formula:

$$D \cdot A = T \cdot I \tag{7.1}$$

where T is the time to expose the object (can be divided into exposure time/step size), I is the electron beam current, D is the dose and A is the area exposed.

For example, assuming an exposure area of 1 cm^2, a dose of 10^{-3} C/cm^2, and a beam current of 10^{-9} A, the resulting minimum writing time would be 10^6 seconds (about 12 days). This minimum write time does not include time for the stage to move back and forth, as well as time for the beam to be blanked (blocked from the wafer during deflection), as well as time for other possible beam corrections and adjustments in the middle of writing. Just to stress one of the crucial peculiarity of the EBL systems one can imagine to cover the 700 cm^2 surface area of a 300 mm silicon wafer, the minimum write time would extend to $7 \cdot 10^8$ seconds, about 22 years. This is a factor of about 10 million times slower than current optical lithography tools. It is clear that throughput is a serious limitation for electron beam lithography, especially when writing dense patterns over a large area.

E-beam lithography is then not suitable for high-volume manufacturing because of its limited throughput. The smaller field of electron beam writing makes for very slow pattern generation compared with photolithography (the current commercial

standard) because more exposure fields must be scanned to form the final pattern area ($\leq$ 1 mm^2 for electron beam vs. $\geq$ 40 mm^2 for an optical mask projection scanner).

Despite the high resolution of electron-beam lithography, the generation of defects during electron-beam lithography is often not considered by users. Defects may be classified into two categories: data-related defects, and physical defects.

Data-related defects may be classified further into two sub-categories. Blanking or deflection errors occur when the electron beam is not deflected properly when it is supposed to, while shaping errors occur in variable-shaped beam systems when the wrong shape is projected onto the sample. These errors can originate either from the electron optical control hardware or the input data that was taped out. As might be expected, larger data files are more susceptible to data-related defects.

Physical defects are more varied, and can include sample charging (either negative or positive), backscattering calculation errors, dose errors, fogging (long-range reflection of backscattered electrons), out-gassing, contamination, beam drift and particles. Since the write time for electron beam lithography can easily exceed a day, "randomly occurring" defects are more likely to occur. Here again, larger data files can present more opportunities for defects.

The primary electrons in the incident beam lose energy upon entering a material through inelastic scattering or collisions with other electrons. In such a collision the momentum transfer from the incident electron to an atomic electron can be expressed as [75]

$$dp = 2e^2/bv \tag{7.2}$$

where b is the distance of closest approach between the electrons, and ν is the incident electron velocity. The energy transferred by the collision is given by

$$T = (dp)^2/2m = e^4/Eb^2 \tag{7.3}$$

where m is the electron mass and E is the incident electron energy, given by $E = (1/2)mv^2$. By integrating over all values of T between the lowest binding energy, E_0 and the incident energy, one obtains the result that the total cross section for collision is inversely proportional to the incident energy E, and proportional to $1/E_0$–$1/E$. Generally, $E \gg E_0$, so the result is essentially inversely proportional to the binding energy.

By using the same integration approach, but over the range $2E_0$ to E, one obtains by comparing cross-sections that half of the inelastic collisions of the incident electrons produce electrons with kinetic energy greater than E_0. These secondary electrons are capable of breaking bonds (with binding energy E_0) at some distance away from the original collision. Additionally, they can generate additional, lower

energy electrons, resulting in an electron cascade. Hence, it is important to recognize the significant contribution of secondary electrons to the spread of the energy deposition.

In general, for a molecule AB [76]

$$e^- + AB \rightarrow AB^- \rightarrow A + B^-$$

This reaction, also known as "electron attachment" or "dissociative electron attachment" is most likely to occur after the electron has essentially slowed to a halt, since it is easiest to capture at that point. The cross-section for electron attachment is inversely proportional to electron energy at high energies, but approaches a maximum limiting value at zero energy [77]. On the other hand, it is already known that the mean free path at the lowest energies (few to several eV or less, where dissociative attachment is significant) is well over 10 nm [78, 79], thus limiting the ability to consistently achieve resolution at this scale.

With today's electron optics, electron beam widths can routinely go down to a few nm. This is limited mainly by aberrations and space charge. However, the feature resolution limit is determined not by the beam size but by forward scattering (or effective beam broadening) in the resist while the pitch resolution limit is determined by secondary electron travel in the resist [80, 81]. The use of double patterning allowed the spacing between features to be wide enough for the secondary electron scattering to be significantly reduced. The forward scattering can be decreased by using higher energy electrons or thinner resist, but the generation of secondary electrons is inevitable. It is now recognized that for insulating materials like PMMA, low energy electrons can travel quite a far distance (several nm is possible). This is due to the fact that below the ionization potential the only energy loss mechanism is mainly through phonons and polarons, although the latter is basically an ionic lattice effect. The travel distance of secondary electrons is not a fundamentally derived physical value, but a statistical parameter often determined from many experiments or Monte Carlo simulations down to < 1 eV. This is necessary since the energy distribution of secondary electrons peaks well below 10 eV. Hence, the resolution limit is not usually cited as a well-fixed number as with an optical diffraction-limited system. Repeatability and control at the practical resolution limit often require considerations not related to image formation, e.g., resist development and intermolecular forces.

In addition to producing secondary electrons, primary electrons from the incident beam with sufficient energy to penetrate the resist can be multiply scattered over large distances from underlying films and/or the substrate. This leads to exposure of areas at a significant distance from the desired exposure location. For thicker electrons, as the primary electrons move forward, they have an increasing opportunity to scatter laterally from the beam-defined location. This scattering is

called forward scattering. Sometimes the primary electrons are scattered at angles exceeding 90 degrees, i.e., they no longer advance further into the resist. These electrons are called backscattered electrons and have the same effect as long-range flare in optical projection systems. A large enough dose of backscattered electrons can lead to complete exposure of resist over an area much larger than defined by the beam spot.

Combining previous analysis one can stress that the smallest features produced by electron beam lithography have generally been isolated features, as nested features exacerbate the proximity effect, whereby electrons from exposure of an adjacent region spill over into the exposure of the currently written feature, effectively enlarging its image, and reducing its contrast, i.e., difference between maximum and minimum intensity. Hence, nested feature resolution is harder to control. The proximity effect is also manifest by secondary electrons leaving the top surface of the resist and then returning some tens of nanometers distance away. Proximity effects (due to electron scattering) can be addressed by solving the rather complex inverse problem and calculating the exposure function *E(x,y)* that leads to a dose distribution as close as possible to the desired dose *D(x,y)* when convolved by the scattering distribution point spread function *PSF(x,y)*. However, it must be remembered that an error in the applied dose (e.g., from shot noise) would cause the proximity effect correction to fail.

Since electrons are charged particles, they tend to charge the substrate negatively unless they can quickly gain access to a path to ground. For a high-energy beam incident on a silicon wafer, virtually all the electrons stop in the wafer where they can follow a path to ground.

7.2.2 The operating fabrication parameters of the subμ SNIS process

Approaching to the downscaling of SNIS junctions, the first aim was to validate the standard process implemented at the micrometer scale (Chapter 5), verifying, step-by-step, the compatibility of all the employed techniques (i.e. sputtering deposition, reactive ion etching, anodisation, etc.) respect to the lower and desired dimensions. For this purpose, maintaining the same sequence of the fabrication steps, a few operating parameters had to be modified adapting them to the new goal. In particular, both deposition and etching parameters have been redefined in order to match with the e-beam lithography used to pattern the effective area of the junctions.

In this work the Nb/Al-AlO_x/Nb trilayer was deposited by sputtering (Figure 7.1a, Appendix B.4) with an aluminum thickness of about 50 nm, being subject to an oxidation exposure dose ranging from 160 to 200 Pa · s, while the Nb top counter electrode was reduced from the usual 120 nm value to 50 nm, in order to drastically

lower the etching time during the later reactive ion etching step.

Whereas, the EBL process (Figure 7.1b, b') has been performed by a FEI Quanta 3D ESEM FEG equipped with a J. C. Nabity NPGS pattern generator (Appendix C.4), by using a negative e-beam resist (ma-N2400 series by *Microresist Technology*) to protect the Nb top electrode as usual, spinned down to a thickness of about 0.5 μm (Appendix B.6). Starting from a 5 x 5 μm^2 area down to 0.7 x 0.7 μm^2 (Figure 7.3), since the e-beam resist is considerably thinner than the optical one (0.5 μm vs 1.5 μm) and less stable during etching processes, both the RIE (Section 5.5), used to remove the Nb top electrode in excess, and the anodization (Section 5.6) steps have been adapted and properly optimized as a function of patterned dimensions by EBL, in order to preserve the resist employed to protect the Nb top electrode.

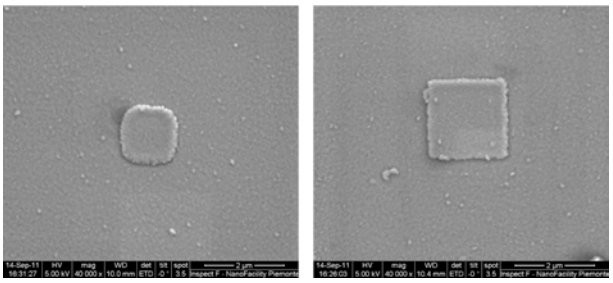

Figure 7.3. Scanning electron microscope (SEM) photographs of (a) 1 μm^2 and (b) 3 μm^2 SNIS junctions fabricated by electron-beam lithography, with Nb wiring on top.

It is well-known that the resolution of the e-beam lithography is mainly limited by both an incorrect exposure dose, D ($\mu C/cm^2$) and by the proximity effect, the deleterious consequence due to the scattering of electrons in the irradiated resist. As a consequence, the size of the exposed resist area could result larger or smaller than the diameter of the incident electron beam. For these reasons, a sistematic study of the correct D has been necessary, optimizing D with a proper scaling of the junction dimensions. A CAD layout was realized to perform the test, including a matrix of squares with different areas: from 0.5 x 0.5 μm^2 to 10 x 10 μm^2. The Figure 7.4 shows the dose matrix.

The exposure dose was linearly changing from 50 $\mu C/cm^2$ for large areas (10 x 10 to 1 x 1 μm^2), and 70 $\mu C/cm^2$ for small areas ($<$ 1 x 1 to 0.7 x 0.7 μm^2). These values were established by previous experiences in patterning of different geometries, shapes and respective dimensions. Greater is the area to draw, and consequently those exposed to the e-beam, smaller should be the dose D, since stronger is the proximity effect. The proximity effect in electron beam lithography is the phenomenon that the exposure dose distribution, and hence the developed pattern, is wider than the scanned pattern, due to the interactions of the primary beam electrons with the resist and substrate.

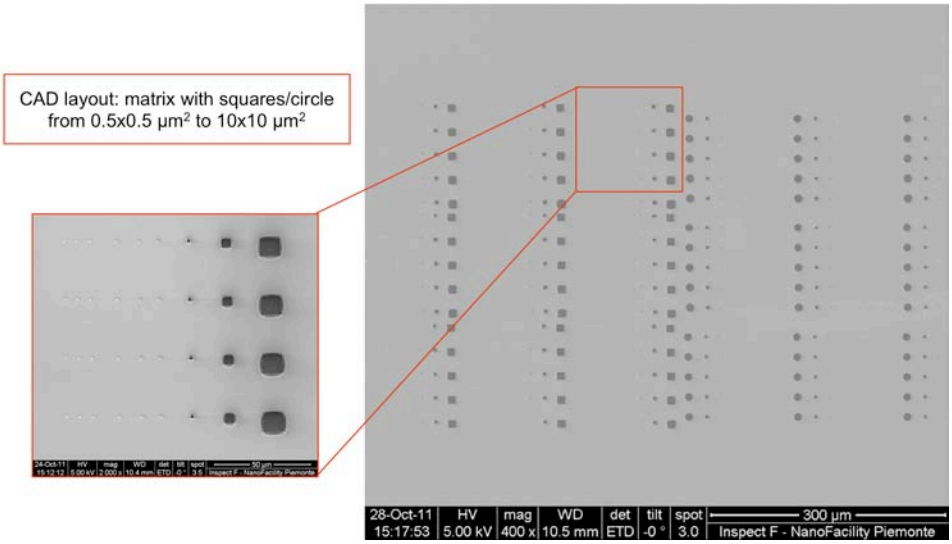

Figure 7.4. A SEM image of the matrix used for the optimisation of the e-beam exposure dose.

The first evaluation was carried out after the development of the e-beam resist, maintaing the development time constant and independent from the D value. The thickness, the quality of the resist walls and possible residuals of undeveloped resist around the drawn areas were evaluated by a visual inspection through the scanning electron microscope. Figure 7.5 shows a good resist appearance after development.

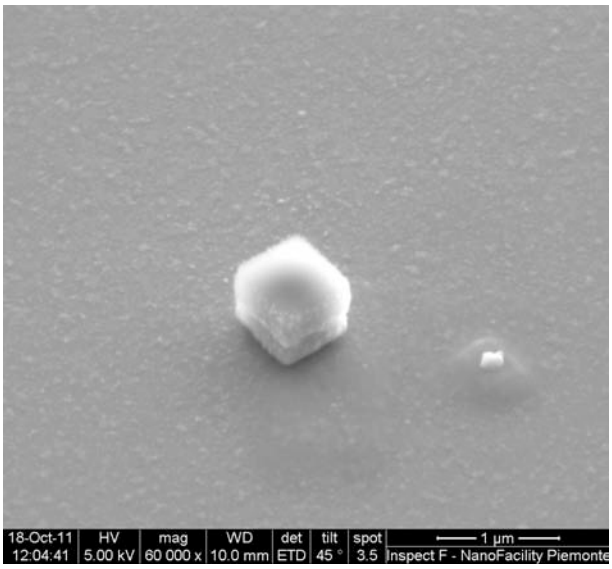

Figure 7.5. A good resist appearance after development.

Afterwards, a further evaluation arisen from the analysis of the Nb top layer residuals, the quality of the resist walls and its dimensions after the RIE step (Figure 7.1c). Figure 7.6 represents a schematic and detailed process flow including both e-beam lithography and RIE steps.

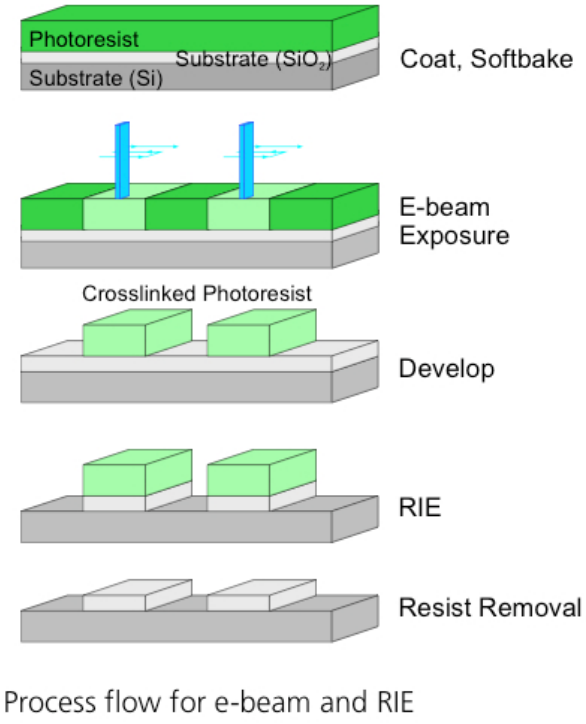

Figure 7.6. A process flow for e-beam and RIE processes.

In Figure 7.7 is reported a back-scattered SEM image concerning a junction after the RIE process. This typology of image is due to collecting back-scattered electrons (BSE), namely beam electrons that are reflected from the sample by elastic scattering. BSE are often used in analytical SEM along with the spectra made from the characteristic X-rays, because the intensity of the BSE signal is strongly related to the atomic number of the specimen. BSE images can provide information about the distribution of different elements in the sample. Thanks to this, it is possible to distinguish the e-beam resist (black), covering the Nb top electrode (white), and the Al layer consequently exposed and unprotected after the reactive ion etching.

Figure 7.8 is representative of an incorrect e-beam exposure dose, because of this residuals of Nb top layer are still present around the resist mask on top, after the RIE process. In this particular case, the final area results greater than those established by the CAD layout, due to the proximity effect above mentioned. In the

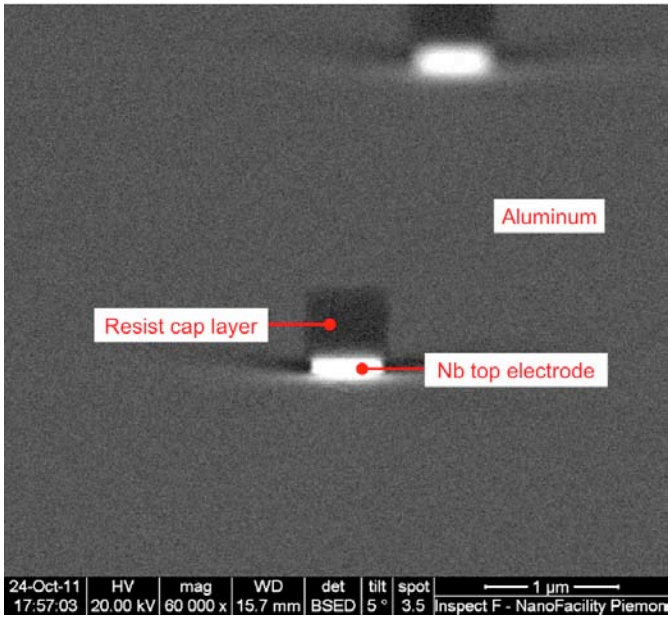

Figure 7.7. Back-scattered SEM image of a junction, after RIE. Different materials are noticeable (tilted images).

right side, the back-scattered SEM image, wherein the white layer represents the Nb layer in excess after the RIE.

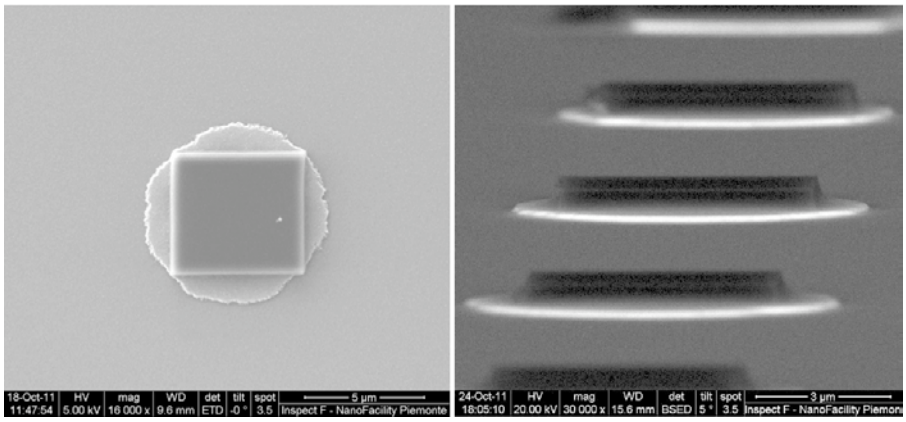

Figure 7.8. SEM images representative of an incorrect e-beam exposure dose. Left side: residuals of Nb top layer around the resist mask. Right side: the back-scattered image (tilted image).

Simultaneously, the RIE process has been optimized, as well: starting form the same operating conditions used at the micrometer scale (specifically, RF power of 100 W, etching time of 10 min and CF_4 pressure of $3 \cdot 10^{-1}$ mbar) an under etching occurred with a consequent uncontrolled reduction of the junction area. By the way,

in Figure 7.9 it is shown a boundary example, where the junction lateral dimension is clearly reduced down to about 340 nm compared to the original 500 nm previously defined by the resist mask.

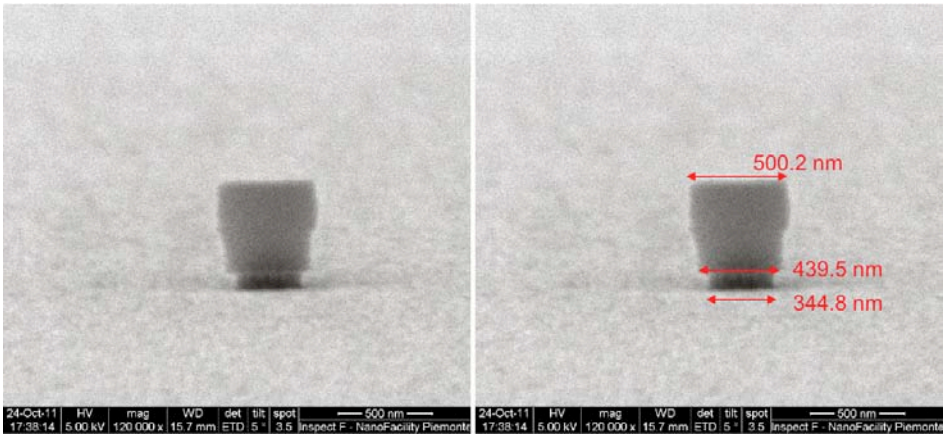

Figure 7.9. SEM images representative of the under etching occuring with improper RIE operating conditions (tilted images).

Therefore, considering the lower thickness of the e-beam resist, the etching time was reduced down to 3 minutes avoiding the undesired consumption of it, and the RF power was increased up to 200 W while the CF_4 gas pressure reduced to around 10^{-2} mbar, making the etching process more directional, and, consequently, reducing the under etching phenomenon, as reported in Figure 7.10 for a drawn junction of 500 nm as lateral dimension.

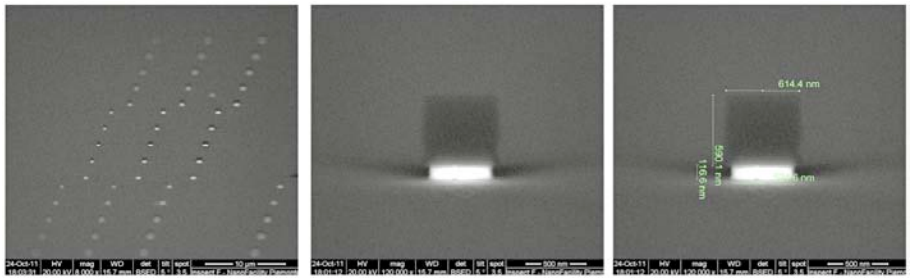

Figure 7.10. Back-scattered SEM images of junctions proving the enhancement in under etching.

Regarding the standard anodization, performed to avoid short circuits between the two superconducting junction electrodes (Figure 7.1d), it has been carried out paying attention to the current density ($8 \cdot 10^4$ μA/cm^2), so limiting under etching and/or under anodization effects due to the emploiment of a thinner resist. In the worst case, under anodisation could cause uncontrolled area reductions up to the total oxidation of the underlying Niobium top electrode (Figure 7.15h).

Balancing all these results, the EBL patterning to define subμ SNIS junctions was performed with an e-beam exposure dose of 60 μC/cm^2, escluding the biggest and the smallest areas, and concentrating the study to areas ranging from 0.7 x 0.7 μm^2 and 2 x 2 μm^2. Since smaller is the lateral dimension much critical are under etching and under anodisation phenomena, the limit for the junctions' dimensions has been defined at 0.8 x 0.8 μm^2 (Figure 7.13).

A traditional optical lithography was lastly exploited to define the trilayer layout, the wiring and the electrical contact pads (Figure 7.1e).

7.3 The electrical characterisation of subμm SNIS junctions

Electrical parameters of the subμm SNIS Josephson junctions have been therefore measured (measurement set up, Appendix A.1), and analyzing the DC *I-V* characteristics a proper scaling of current densities has been observed. In Figure 7.11(a) and (b) the *I-V* curve of a 1 μm^2 and a 3 μm^2 SNIS are shown, with critical current values of about 2.1 mA and 5.25 mA, respectively. Moreover, magnetic field patterns were carried out for several junctions to validate techniques employed in the framework of the usual process. They were performed on 0.7 x 0.7 μm^2 and on 1 μm^2 junctions. As shown in the inset in the Figure 7.11(a), the experimental data show a zero value of critical current at 185 Gauss. This confirms the absence of short circuits into the barrier and in the anodic oxide, assessing the high quality of the junctions, and it is well related to junction dimensions and current density.

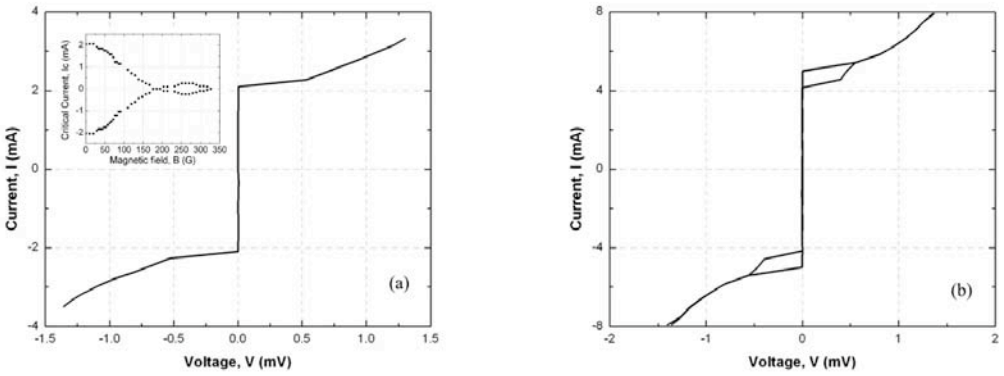

Figure 7.11. Current – voltage characteristics referred to (a) 1 μm^2 and (b) 3 μm^2 SNIS junctions defined by EBL. The inset in the figure (a) represents the magnetic pattern of the junction.

The RF and temperature behaviours have been also analyzed. Due to the peculiar high characteristic voltages, high order steps are enhanced. Irradiating a 1 μm^2 SNIS with a $V_c = 670$ μV, Shapiro steps have been measured up to $n = 7$ at 4.2 K (Figure 7.12(a)). This feature allows operating near the niobium critical temperature. The $n = \pm 1$ Shapiro steps have been optimized at about 7 K (Figure 7.12(b)).

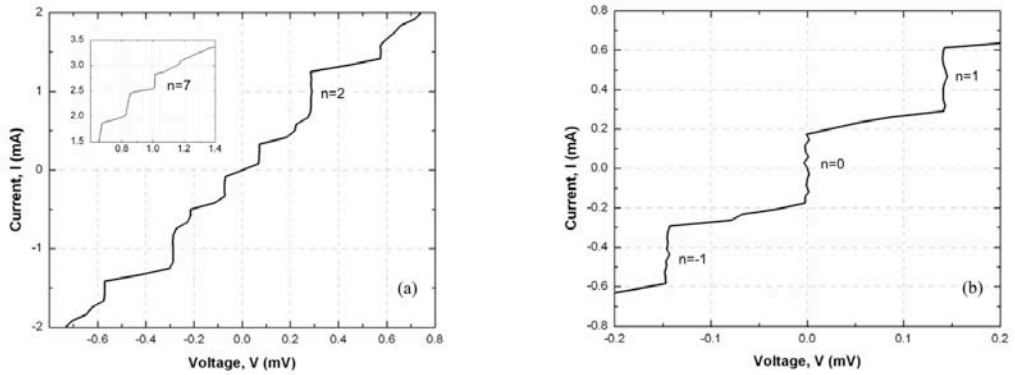

Figure 7.12. Quantized voltage steps for a 1 μm^2 single junction with a $V_c = 670$ μV, measured with a frequency of around 70 GHz at (a) 4.2 K and (b) at 6.7 K. The inset in the figure (a) shows the n = 7 step at 4.2 K, due to the high V_c value.

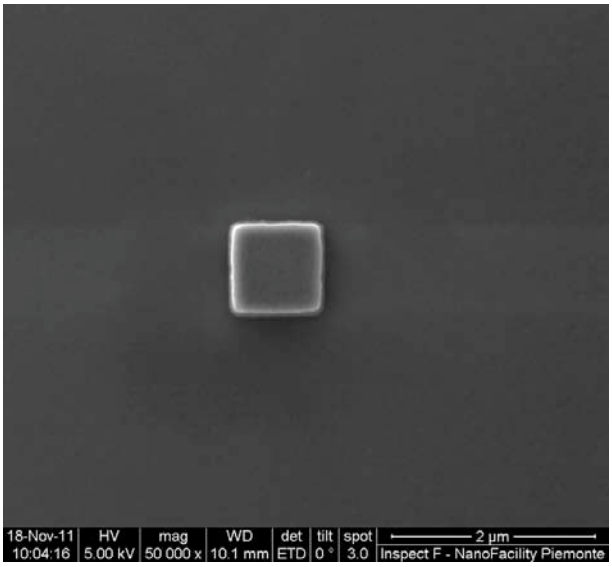

Figure 7.13. The SEM image related to a 0.8 x 0.8 μm^2 SNIS junction defined by EBL.

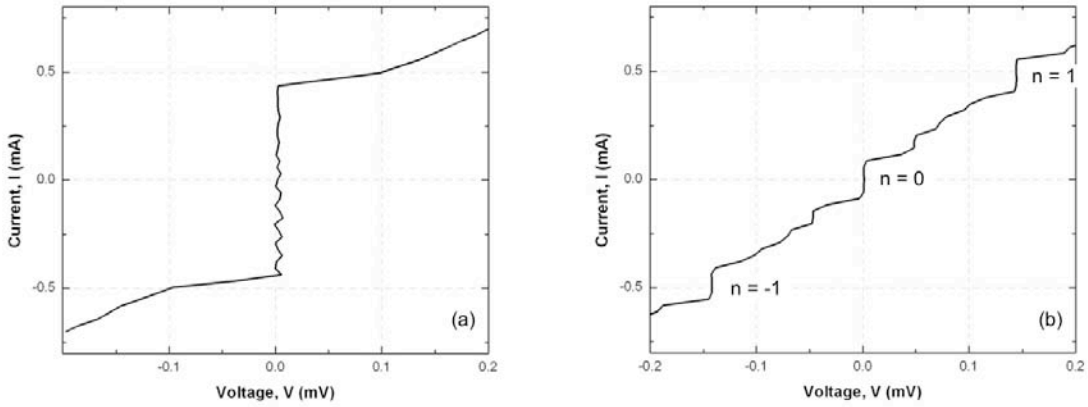

Figure 7.14. Current – voltage characteristics referred to a 0.8 x 0.8 μm^2 SNIS junction defined by EBL, at 4.2 K: the DC I-V (a), and the RF I-V (b), respectively.

Therefore, the junction dimensions were further reduced down to 0.8 x 0.8 μm^2 (Figure 7.13), and the corresponding DC and RF behaviours are reported in Figure 7.14. The DC I-V characteristic (Figure 7.14(a)) shows a I_c value of about 450 μA, and the first order steps (Figure 7.14(b)) with an amplitude around 100 μA were measured, irradiating the junction at aroud 70 GHz.

7.4 The resist-based process failures

Each resist-related process requires various steps to produce a pattern on a wafer. These steps are very crucial and are always changing. The each processes are in a particularly high state of flux. The ever-increasing demands for faster and more complex-circuits reach their culmination in these steps, and it is the responsibility of the lithography groups to manufacture the designs that are created. The entire lithographic process (both optical or e-beam) is critical, from the deposition of the resist to the alignment and exposure of the wafer to the each processes that actually define the patterns. The exact dimensions of all the structures must be maintained, and there must be no damage to other portions of the circuits while all of this activity is underway. This requires the utmost in care and precision. Therefore, working with resist-based lithographic techniques some disadvantages have to be considered, thereby lowering the yield of the entire fabrication process.

In some way, the resist could be considered as a metastable material. For this reasons many problems can occur during the device fabrication process, as the resist could be strictly affected by a non regular thickness and roughness, a lower adhesion on the substrate or metal layers with a consequent exfoliation, cross-linking, thermal

decomposition during the process, and so on. Specifically, during this thesis some failures arisen during the lithographic, etching and anodization processes. Some of them are summarized in Figure 7.15.

Since all these drawbacks, and in order to release the fabrication process from the resist, another approach has been considered to develop SNIS junctions exploiting a mask and a resist-less process, as reported in the later Chapter.

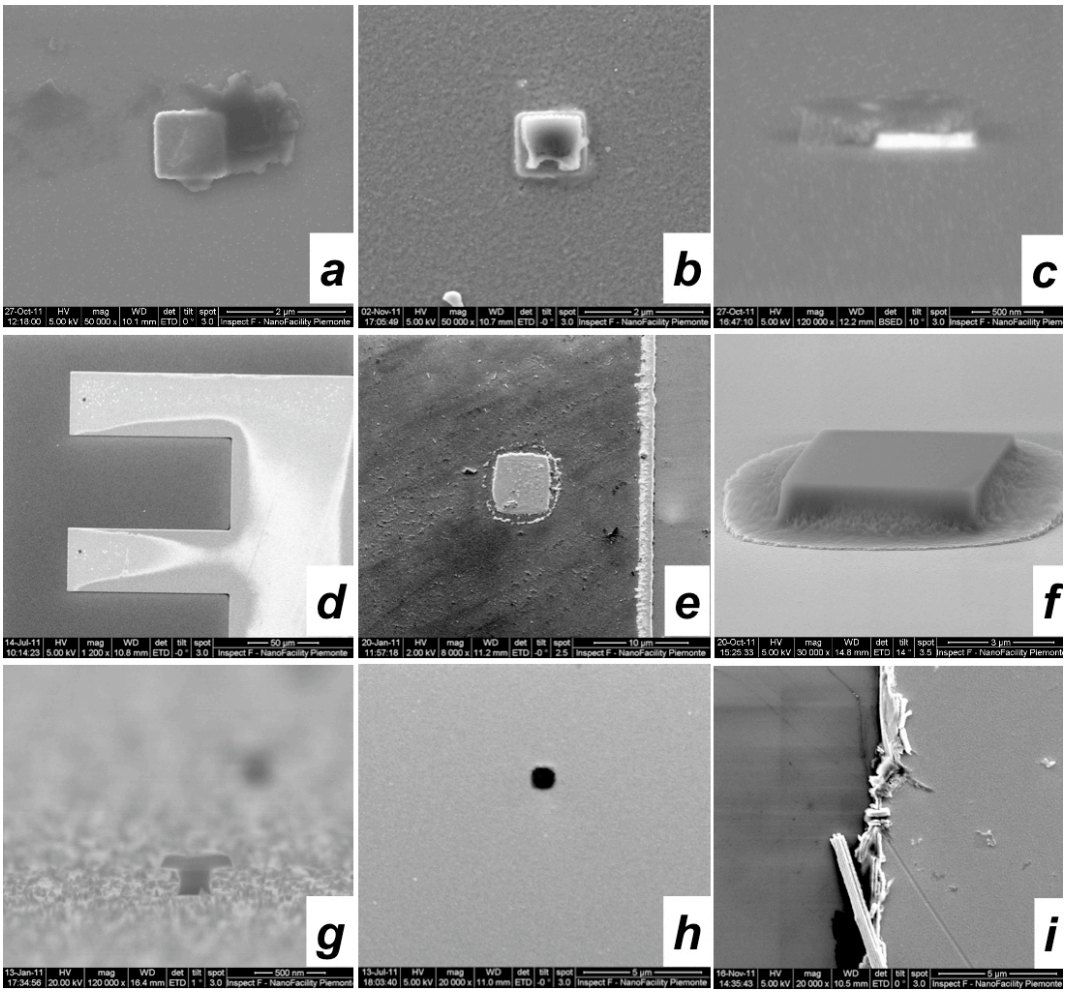

Figure 7.15. SEM images representative of typical failures occuring with a resist-based fabrication process: (a) resist residuals randomly localized on the sample surface; (b) resist residual on top of the Nb counter electrode; (b) damage of the resist, i.e. during etching processes; (d) and (e) incompleted RIE etching of the Nb top layer; (f) Nb top layer residuals due to an incorrect e-beam exposure dose; (g) under etching due to unsuitable RIE operating parameters; (h) under anodisation due to an inefficient adhesion of the resist on the Nb top electrode; (i) trilayer damage during the lift-off process.

7.5 Conclusions

An EBL process has been optimized to reduce the typical SNIS junction size (5 x 5 μm^2) at the submicrometer scale, down to 0.8 x 0.8 μm^2. Thereby, the optical lithography has been replaced and the "micro" fabrication process has been adapted by properly evaluating fabrication and electrical parameters considering the down-scaling of the areas. Meanwhile, since the e-beam resist is considerably thinner than the optical one and less stable during etching processes, the Reactive Ion Etching (RIE) and the anodization steps have been adapted and calibrated as a function of patterned dimensions by EBL, in order to preserve the resist and avoid uncontrolled reductions of sizes. Moreover, the magnetic pattern confirmed the absence of short circuits into the tunneling barrier and in the anodic oxide, so validating the fabrication process. A proper scaling of junction current densities has been observed and quantized Shapiro steps have been measured also at the temperatures of about 7 K, confirming the interest to use SNIS junctions at higher operating temperatures in a cryocooler set up for AC voltage standards.

Chapter 8

The NanoSNIS sculpted junction

This chapter details the recent work concerning the employment of an innovative three-dimensional Focused Ion Beam (3D FIB)-based nanomachining to fabricate Nb/Al-AlO_x/Nb SNIS junctions on a deep submicrometer scale, with a higher resolution compared to the ones obtained by the standard "window" resist-based process previously described in Chapters 5, 6 and 7.

The innovative nanoSNIS junction prototype has been realized in collaboration with NanoFacility Piemonte (INRIM), exploiting the know-how earlier acquired in the development of Hybrid Single Electron Transistors (HSET) as innovative current standard for metrological applications.

8.1 Introduction

The challenges faced by quantum electronics and metrology are directing the new generations of devices towards smaller dimensions and higher levels of integration. Quantum information processes, single photon detection, nanoelectro-mechanical resonator systems, nanomagnetism and spintronics will benefit of improved performances achievable by nanofabrication processes. It is well-known for instance, that limitations on Superconducting Quantum Interference Devices (SQUIDs) sensitivity set by thermal noise can be reduced by lowering the inductance and capacitance of the device. Also in the circuits for Rapid Single Flux Quantum (RSFQ) a basic property such as the maximum clock frequency scales with dimensions. Furthermore, in the AC waveform generators, when a pulse driven source is employed, the maximum device size must be shorter than the minimal wavelength of the incident radiation. Device downscaling must be pursued without affecting fundamental properties such as, for instance, the current-voltage I-V response of Josephson junctions (hysteretic or non-hysteretic behaviour). Rather, electrical parameters of the junctions, such as critical current, I_c and normal tunneling resistance, R_n must properly scale with

dimensions.

The junction downscaling is a technological challenge, since the merging of classical optical lithography with Reactive Ion Etching (RIE) and/or lift-off techniques to define the area entails an intrinsic and uncontrollable reduction of final dimensions. Due to the all drawbacks occurred during the previous fabrication process, another approach has been considered to realize SNIS junctions releasing the process from the resist. For this purpose, a mask/resist-less process based on the Focused Ion Beam technique has been adopted to fabricate Nb/Al-AlO$_x$/Nb SNIS junctions on a deep submicrometer scale, as reported in the following.

8.2 Focused Ion Beam lithography technique

The FIB technique was mainly developed during the late 1970s and the early 1980s [82, 83]. This technology enables precise cutting material, selective material deposition, enhanced etching and end-point detection. FIB etching is performed either by physical or by ion beam induced etching, with many potential applications such as micro and nano-machining, failure analysis by cross sectioning [84], and Transmission Electron Microscopy (TEM) lamellae preparation [85]. Moreover, FIB has several advantages such as high sensitivity and resolution, high material removal rate, low forward scattering, and direct fabrication in selective area without using any etching mask. In particular, the 3D FIB etching is an emerging technology for precision lithography, featuring fast fabrication of nanoscale structures as stacked-junction devices [86], nano-ribbons, 3D Single Electron Transistor (SET) devices [87], nano-scale SFS (Superconductor - Ferromagnet - Superconductor) Josephson junctions [88], used to prepare a range of devices including lenses on the ends of fibers [89], pseudo spin valves [90], and pillar micro-cavities [91].

Focused ion beam and dual-platform systems (i.e., systems with both ion and electron beam columns as the Quanta^{TM} 3D FEG installed at NanoFacility Piemonte, Appendix C.4) have been used extensively for micro- and nanofabrication during the past 10 – 15 years, for example, for circuit modifications and read-write head trimming. The tools can sputter and implant lines as narrow as 10 nm and deposit metals and insulators in lines as narrow as 30 nm in user-defined patterns. In addition, as the FIB is scanned, signals such as the generated secondary electrons (SE) can be collected for imaging. It is the combination of these capabilities that is at the heart of the instrument's power and versatility for micro and nanofabrication; a device or sample may be imaged and the FIB sputtering or metal/insulator deposition can then be made to within 50 nm of a feature or area of interest.

Over the last five years, there has been a marked increase in the diversity and complexity of the applications for these systems. This has been driven partly by the nanotechnology explosion but is mainly because the increased number of systems

installed in academia and industry has provided greater access. FIB technique complements conventional fabrication equipments, and typically its employment falls into one of two categories. The first category is the fabrication or modification of structures and devices that are difficult to prepare by using conventional processes, because of material or geometry constraints. The second one is the rapid prototyping or modification of structures and devices, which can be done in fewer, quicker, and simpler processing steps, impossible by using conventional processing.

8.2.1 The FEI Quanta^{TM} 3D Gallium column

The basic functions of the FIB, namely, imaging and sputtering with an ion beam, require a highly focused beam. A consistent principle of any focused beam is that the smaller the effective source size, the more current that can be focused to a point. Unlike the broad ion beams generated from plasma sources, high-resolution ion beams are defined by the use of a field ionization source with a small effective source size on the order of 5 nm, therefore enabling the beam to be tightly focused. The ion source type used in all commercial systems and in the majority of research systems designed with micromachining applications in mind is the liquid-metal ion source (LMIS). Of the existing ion source types, the LMIS provides the brightest and most highly focused beam (when connected to the appropriate optics). There are a number of different types of LMIS sources, the most widely used and the one mounted on the Quanta^{TM} 3D column being a Ga-based blunt needle source (Figure 8.1).

Figure 8.1. FEI Quanta^{TM} 3D LMIS Ga^{+} ions source

Gallium has undoubted advantages over other LMIS metals such as In, Bi, Sn, and Au because of its combination of low melting temperature (30°C), low volatility, and low vapor pressure. The low melting temperature makes the source easy to

design and operate, and because Ga does not react with the material defining the needle (typically W) and evaporation is negligible, Ga-based LMISs are typically more stable than other LMIS metals. During operation, Ga flows from a reservoir to the needle tip (with an end radius of about 10 mm), where it is extracted by field emission. A large negative potential between the needle and an extraction electrode generates an electric field of magnitude 1010 V/m at the needle tip. The balance between the electrostatic forces and the Ga surface tension wetting the tapered W needle geometry results in the formation of a single Taylor cone at the needle tip. For typical emission currents used in FIB microscopes ($\sim$ 2 mA), a cusp forms at the tip of the Taylor cone with a tip radius of approximately 5 mm. The simplest and most widely used ion beam columns consist of two lenses (a condenser and objective lens) to define the beam and then focus it on the sample, beam-defining apertures to select the beam diameter and current, deflection plates to raster the beam over the sample surface, stigmation poles to ensure a spherical beam profile, and a high-speed beam blanker to quickly deflect the beam off the sample and onto a beam stop such as a Faraday cup. Because the focusing strength of an electromagnetic lens is directly related to the charge/mass ratio of a particle, it is impractical to build electromagnetic lenses for ions (which would weight thousands of kilograms); thus, focusing and steering are performed using electrostatic components rather than the electromagnetic components used for electrons. The size and shape of the beam intensity profile on the sample determines the basic imaging resolution and micromachining precision. Generally, the smaller the beam diameter, the better the achievable resolution and milling precision, although the requirements for the two applications are not exactly the same. For the energies, currents, and acceptance angles used in typical FIB systems, the beam spot size is limited mostly by the chromatic aberration that results primarily from the energy spread of the beam due to space charge effects at the ion source and secondarily from the spherical aberration of the lenses. However, the ultimate spatial resolution for FIB imaging is, in fact, limited by sputtering and is thus sample-dependent. In modern FIB systems, the imaging resolution determined by the sputter-limited signal/noise usually is about 10 nm. The sample is mounted on a grounded stage with three-axis translation, rotation, and tilt capabilities. The stage is designed to have a eucentric point (i.e., a well- centered point such that the field of view is maintained when tilting the specimen) at the location where the two beams cross (or at the working distance of the ion beam, in the case of a single-beam FIB). The region of interest on the sample is moved to the eucentric point using translation and rotation and then tilted for the desired angle of beam incidence. The total current on the sample (sum of the incoming ion or electron beam and all emitted charged particles) is measured at the stage. Depending on the application, the various emitted particles or radiation can be detected with appropriate detectors in the sample chamber. Traditional detectors such as those in an SEM can be used to detect the electrons or x-rays created by the

interaction of the ion beam with the sample. The ions sputtered from the sample can also be detected using a variety of detectors such as charge electron multipliers, and mass selection of the sputtered charged particles is also possible (secondary ion mass spectrometry). FIBs derive an important additional functionality through the use of gas-injection sources to deliver gas locally to either enhance the etching rate or result in site-specific CVD. Secondary electrons generated by the incident ion beam (or, alternatively, the incident electron beam in dual-beam systems) can crack hydrocarbon precursor gases, leading to local deposition of the conducting material (W, Pt, or C) or insulating material (SiO_2). The local deposition of material also enables sophisticated micromanipulation within the FIB chamber, made possible through micromanipulation accessories and the ability of the FIB to cut (sputter), paste (deposit), and watch (image) during a manipulation process within the chamber. The result is a system that can image, analyze, sputter, and deposit material all with very high spatial resolution and controlled through one software program. In a large part, it is this multi-functional versatility that has made FIB instruments popular among materials researchers.

8.2.2 High energy Ga^+ ions interaction with matter

Because of the sputtering action of the ion beam, the FIB can be used to locally remove or mill away material. For direct milling, the limiting feature size is typically about 10 nm. Quantitative aspects of sputtering are complicated and depend on the material, crystal orientation, ion beam incidence angle, and the extent of redeposition. As the incidence angle of the ion beam is increased, the intersection of the collision cascade with the sample surface increases, and the number of sputtered atoms per collision cascade increases. However, at the same time, the fraction of reflected or backscattered Ga^+ ions increases. The combination of these two effects leads to a maximum in sputtering yield at an incidence angle of approximately 75° - 80°. Silicon or amorphous solids are ideal for such a study because the effects of crystal channeling are avoided (the surface region of Si amorphizes under the Ga^+ beam). The behavior is more complicated in crystalline material where both incident angle and channeling effects are present. The sputtering yield at a given incidence angle can vary by as much as a factor of 10 for strongly channeling crystal orientations in materials such as Cu. This is because for easy channeling orientations, the ion experiences only inelastic glancing-angle collisions with the atoms lying in a crystal plane and travels deeper into the crystal before causing elastic collisions, so that fewer atoms are sputtered from the surface. The sputter profiles also depend on the exact sequence in which the ion beam is rastered over the surface.

Redeposition decreases the effective sputter yield and changes sputter profiles. The decreased yield comes about because redeposited material lands in the area being sputtered and must be sputtered a second time. Redeposition is also given

as a reason why completely vertical side walls cannot be cut with the FIB without over-tilting the sample, but it is certainly also partly because of the intensity tails of the ion beam profile and of the decrease in sputter yield at high incidence angles. Many details of redeposition effects remain open, such as the development of crystal orientation and channeling effects seen in the redeposited material. In addition to redeposition, surface roughening and shadowing effects are prevalent during sputtering. Surface roughening, specifically ripple formation, is widespread during ion bombardment and is attributed to competition between smoothing by surface diffusion or viscous flow and roughening because of surface curvature-dependent sputter yields (the sputter yield depends on local curvature for the same reasons it depends on angle of incidence). Even during normal-incidence sputtering, surface roughening can occur and is dependent on the crystal orientation. Such crystal-orientation-dependent rippling is attributed to anisotropic surface diffusion.

8.3 The nanoSNIS fabrication process

The fabrication process implemented to further reduce the Nb/Al-AlO_x/Nb SNIS dimensions towards the mesoscopic scale based on FIB technique can be summarized in the following steps :

- Deposition and patterning of the multilayer structure
- Definition of the junction area by the 3 D FIB sculpting method
- Anodisation of the junction's sidewalls

and can be schematized as in Figure 8.2.

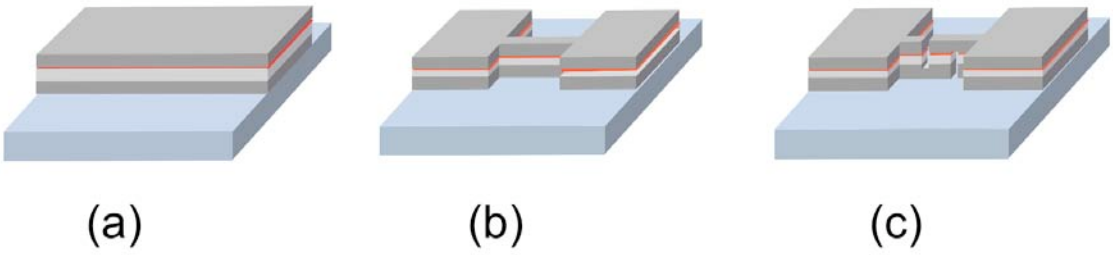

Figure 8.2. The main steps for nanoSNIS JJs fabrication by FIB etching method. (a) Deposition and patterning of the multilater structure; (b) and (c) FIB steps detailed later (Figure 8.4).

8.3.1 The deposition and patterning of the multilayer structure

The first patterning step in the 3D SNIS device fabrication was performed by optical lithography and lift-off techniques to define the Nb/Al-AlO_x/Nb multilayer structure, previously deposited on a 1 x 1 $inch^2$ Corning glass substrate (Figure 8.2 (a)).

The choice of substrate has to take in account his good planarity and insulating properties for both the electrical measurement and the anodization process.

The optical mask used to pattern the nanoSNIS trilayer was made in collaboration with NanoFacility Piemonte using a Low Vacuum EBL process (see the Appendix B.7) using the Quanta^{TM} 3D e-column. The mask is represented in Figure 8.3, with its relative CAD layout. This first lithographic step does not present criticism because dimensions of all patterned components (both electrical contact pads, and microstrip lines) are sufficiently large for the definition by the lift-off technique.

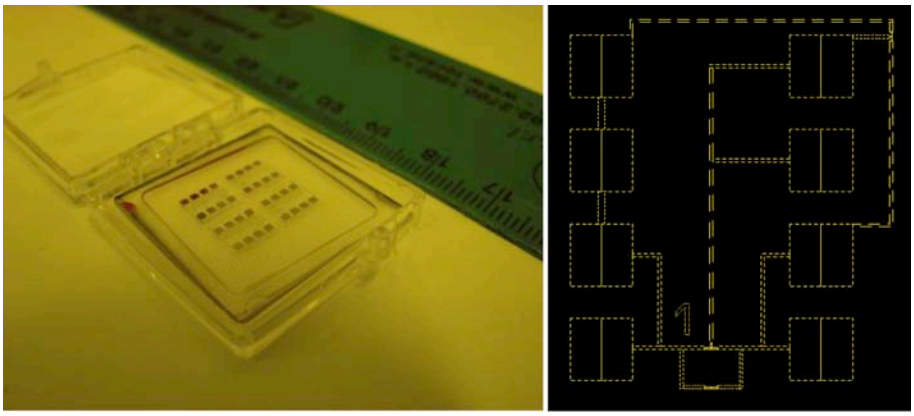

Figure 8.3. Image of the optical mask used for the FIB technique (left side), and its CAD layout (right side).

Same as in the previous processes, the thin film deposition of the Nb/Al-AlO_x/Nb multilayer was carried out by the RF magnetron sputtering, Appendix C.1), in a high vacuum ambient at some units in 10^{-7} mbar. In this way, high reproducibility and quality are guaranteed because of the highly pure metal electrodes and the very low defects in the barrier.

The thickness of both niobium electrodes was, in this case, 400 nm, much thicker compared to the previous SNIS trilayers. This thickness is imposed by the FIB technique, thereafter employed to define the effective area of the junction, as described later. The metallic aluminum barrier was 80 nm thick, and the AlO_x grown *in-situ* without breaking the vacuum by oxidation, in pure oxygen pressure and with a gas

exposure, E (E = oxygen pressure x exposure time) of about 200 Pa $\cdot$ s. For more details, see the Appendix B.5.

8.3.2 The 3D FIB Sculpting method

The focused ion beam process was entirely exploited by means of a FEI Company Quanta 3D dual-beam system, which has the two functions of milling and observation. The secondary electron imaging induced by the gallium ion (Ga^+) beam scanning allows accurate alignment to be obtained over nanometer-size existing structures, and a fine tuning of the device parameters was obtained through real time monitoring of the milling process. A compensation of small sample drifts by using a beam-shift tool was also achieved.

The smallest ion beam spot size is approximately 7 - 10 nm, which enables correspondingly small features to be patterned. The shape of an FIB cut is dependent on many factors, such as its geometry, milled depth, ion beam profile, and the redeposition of sputtered material. The combination of ion beam profile effects and sputter yield changes with the FIB angle of incidence causes rounding of the top edges of an FIB cut and the side-walls to be inclined a few degrees from the perpendicular (the exact angles depend on the ion beam profile and milled depth). Redeposition may also cause the sidewalls to incline. As the milling depth increases, the probability of the sputtered material re-depositing onto the sidewalls increases. If a line or hole is milled 10 to 15 times deeper than its width, redeposition results in V-shaped cross sections. The aspect ratio (depth to width) can be improved by using gas-enhanced etching. Because the shape of a cut is dependent on the milled depth, the milling is referred to as 2D patterning if the sputtered depth is < 100 nm, and 3D micromachining if the sputtered depth is > 100 nm.

The ion beam lithography step was performed using a custom sample holder able to locate the specimen surface both perpendicular and parallel to the ion beam.

First, tilting the custom stub at 22° with respect to the electron beam and the sample perpendicular to the ion beam trajectory (Figure 8.4, left), a multilayered lamella was roughly narrowed up to 500 nm by a multi-step etching, with a series of decreasing beam currents, down to 100 pA. This not only for efficiency but also to minimize the amount of material redeposited on the sides of the narrow track. In particular, the Figure 8.5 exhibits the SEM photograph of the lamella milled by FIB according to the previous procedure.

The impinging ions either implanted themselves or milled material from the surface of the sample, thus producing an amorphous layer and a buried implanted region within the surface. Consequently, to reduce these unwanted redeposition effects, the width of the lamella was further narrowed down to 390 nm, and hence the junction width (w, in Figure 8.6) was defined.

Furthermore, the custom stub was tilted at -8° with respect to the electron beam

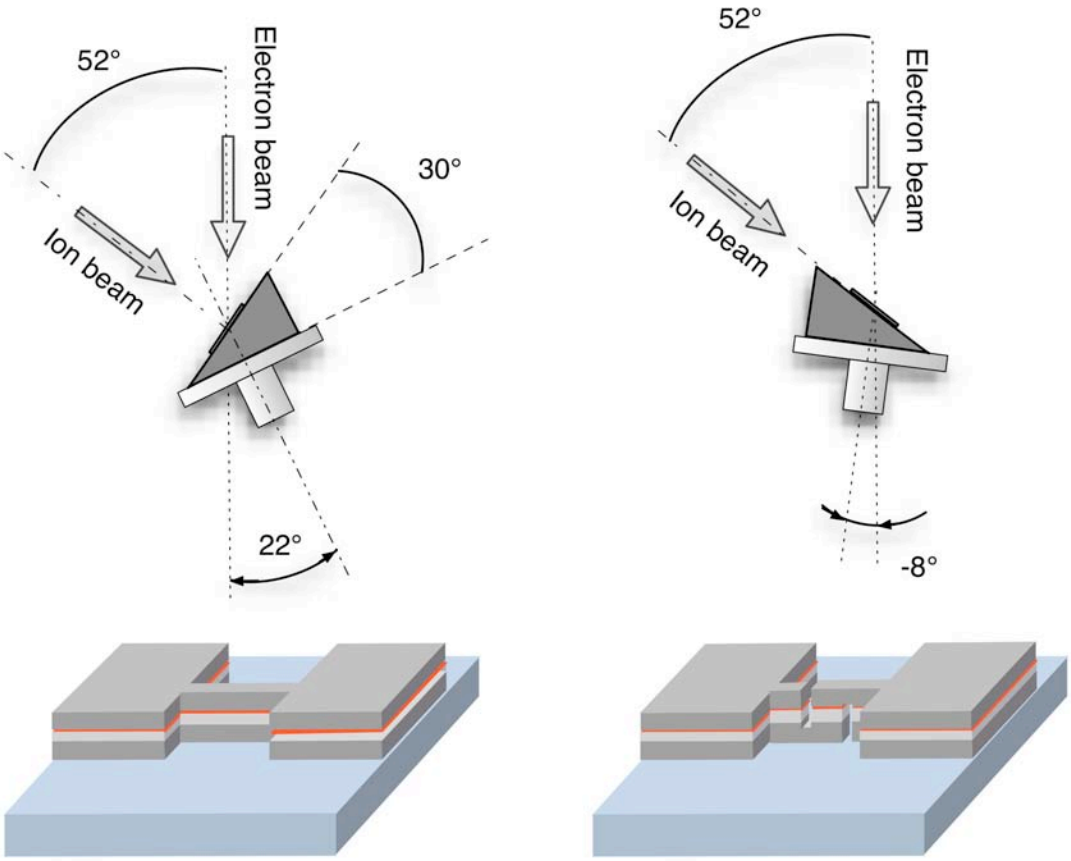

Figure 8.4. The representation of the two fabrication steps based on FIB technique: milling at 22° (left), and at -8° (right) with respect to the electron beam axis.

and the sample surface placed parallel to the ion beam trajectory (Figure 8.4, right). In this way, two side cuts in the lamella were performed, and the distance (390 nm) between them determines the junction length (l, in Figure 8.6).

A SEM image of an angular view of a 3D SNIS junction fabricated by FIB is shown in Figure 8.7. The different layers of the Nb/Al-AlO_x/Nb structure in the lamella may be easily recognized. In the inset of Figure 8.7, the scheme of the multilayered junction is represented with the flowing current through the tunneling barrier, labeled I.

It has to be taken in account that one of the major drawbacks of FIB imaging and machining, particularly for nanoelectronic devices and Transmission Electron Microscope (TEM) samples, is the damage generated by the ion beam [92]. In fact, as the ion dose increases, the individual disordered cascade regions overlap and a

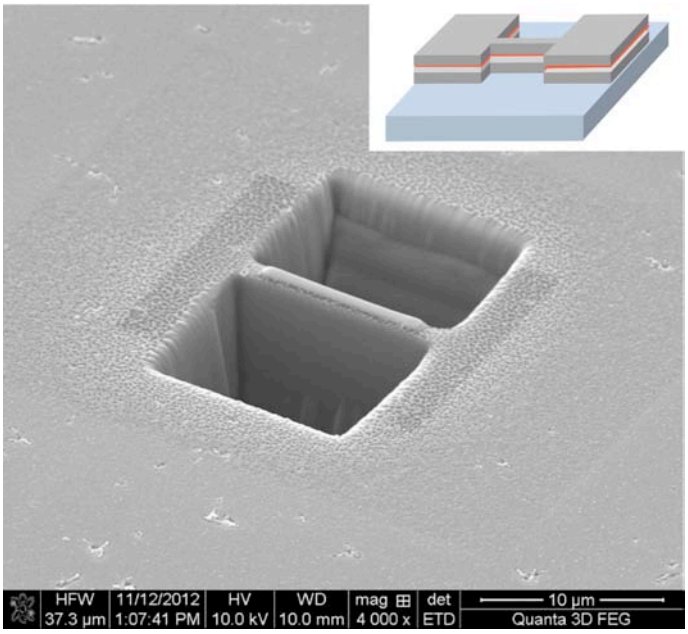

Figure 8.5. A SEM photograph of a lamella of the SNIS trilayer, milled by FIB according to the scheme represented in the inset.

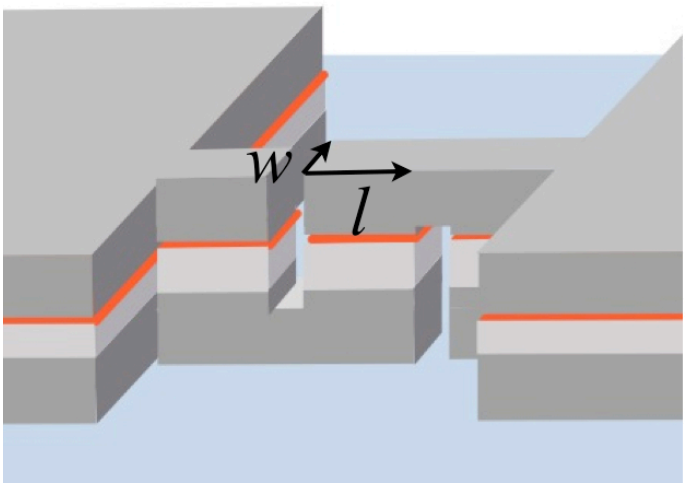

Figure 8.6. A scheme of the final nanoSNIS Josephson device after the last FIB step. The junction dimensions are represented: w, the width, and l the length.

damaged surface layer is formed. Depending in particular on the sample material and temperature, the ion beam damage can take the form of sample surface amorphization, point defect creation, dislocation formation, phase formation, grain

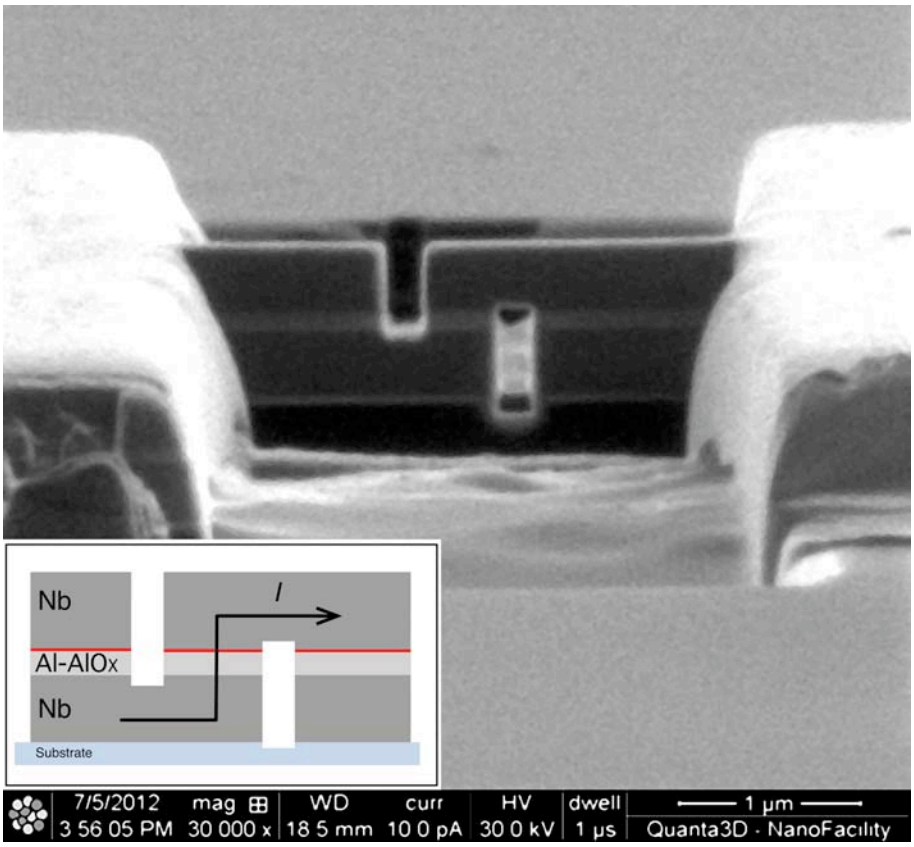

Figure 8.7. A SEM photograph of a nanoSNIS junction fabricated by FIB. A scheme of the junction is represented in the inset, wherein the flowing tunnel current through the nano junction is labeled *I*.

modification, or other unusual effects. With the exception of Si amorphization, systematic investigations of FIB damage are just beginning. Nonetheless, several trends can be identified based on literature results for broad beam ions and on anecdotal FIB observations. Since pure metals (like Nb and Al in these devices) have non-directional bonding they do not amorphize. Thus, thin amorphous layers sometimes observed at the edge of pure metal TEM samples made by FIB presumably contain impurities such as Ga, C, or O. Some oxygen gets in because of the relatively poor quality of the vacuum. Point defects and dislocation loops can also be created during FIB imaging and machining. Systematic studies of FIB-induced defects have not been undertaken, although there are many isolated observations, both published and unpublished. For example, Cu is prone to extensive FIB damage [93], but Al is not and even provides reasonable-quality high-resolution TEM samples [94].

Several additional and unusual types of damage have been observed in FIB-milled samples. These include the formation of Ga-containing surface phases [92] as well

as ion-beam-induced grain growth in fine-grained Ni and Ni alloys [95]. Preferential sputtering, which is prevalent during FIB milling of materials that decompose at low temperatures, can lead to chemical changes in the surface region and influence the ease of damage formation and amorphization.

8.3.3 The anodization of the junction's sidewalls

As previously mentioned, this highly energetic etching leads to spurious inclusions of implanted Ga^+ ions and this event may influence the final electrical behavior of the junction. Therefore, a standard anodization was performed as final step to eliminate the unstructured layer and short circuits of the junction due to conducting materials (mostly Nb) redeposited during FIB etching, by changing the conducting materials into insulating oxides. The second is to suppress the contribution of the sample surface, which might have been damaged by Ga^+, to electrical conduction.

A typical electrochemical solution based on ammonium pentaborate was employed, with a constant current density of about 1 mA/cm^2 flowing through the cell, up to a voltage value of 60 V. This step exploits the experimental setup already mentioned in the Section 5.6 (refer to Appendix B.2 for a detailed description of this process).

In this condition, about 54 nm of Nb [96] were converted in NbO_x, further reducing the effective junction's area down to about 280 x 280 nm^2. According to D. Yuvaraj et al. [97], this value is sufficient to entirely remove the damaged region. It is important to stress also that niobium is a well-behaved metal in respect to anodisation not only because it works with many different electrolytes, but mostly because is insensitive to contaminations. For more technical details, see the Appendix B.9, and refer to Figure 8.8 for the results of the anodization process on a FIB milled device.

Furthermore, the anodised device was prepared and the lamella made thinner according to the TEM-lamella procedure in order to perform a scanning transmission electron microscopy (STEM) investigation to verify the trend of the anodisation process into the tunneling barrier. STEM combines the principles of transmission electron microscopy and scanning electron microscopy and can be performed on either type of instrument. Like TEM, STEM requires very thin samples and looks primarily at beam electrons transmitted by the sample. One of its principal advantages over TEM is in enabling the use of other of signals that cannot be spatially correlated in TEM, including secondary electrons, scattered beam electrons, characteristic X-rays, and electron energy loss. Like SEM, the STEM technique scans a very finely focused beam of electrons across the sample in a raster pattern. Interactions between the beam electrons and sample atoms generate a serial signal stream, which is correlated with beam position to build a virtual image in which the signal level at any location in the sample is represented by the gray level at the

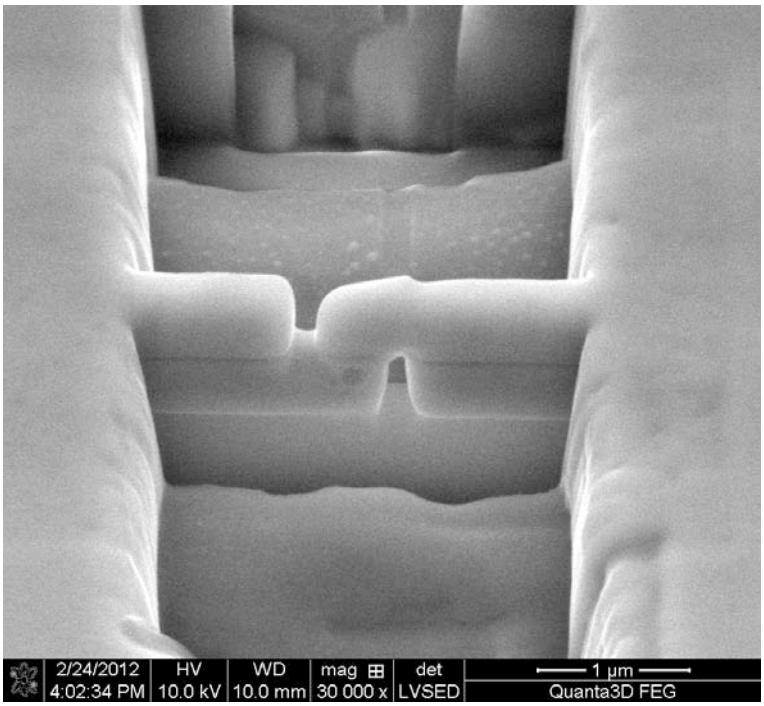

Figure 8.8. A SEM picture of a nano SNIS after anodisation. The anodic oxide growth is appreciable as a volumetric expansion.

corresponding location in the image. Its primary advantage over conventional SEM imaging is the improvement in spatial resolution. STEM analysis has been carried out by using the STEM detector included into the Quanta^{TM} 3D system, and Figure 8.9 shows the STEM image concerning the lamella related to the nanoSNIS junction after anodisation.

Through this analysis has been possible to appreciate that the anodic oxide grows for half inside and half outside the sidewalls of the junction, including the amorphisation layer in its matrix. The Ga^{+} ions implantation is visible with a thickness of 30 nm and embedded into the oxide layer, about 100 nm thick. The thickness of the oxide is directly linked to the voltage limit reached during the process. In this case the operating voltage was around 60 V.

At the end of the anodization process the device can be mounted on a sample holder and micro-bonded (Appendix C.7) to macroscopic contacts, following a particular procedure in order not to expose the nanoSNIS junction to unwanted electrostatic discharge.

In contrast to the previous SNIS fabrication processes (Chapters 5 and 7) wherein the junctions dimensions are defined by optical lithography or Electron Beam Lithography through the "window" process, the FIB processing requires neither resist

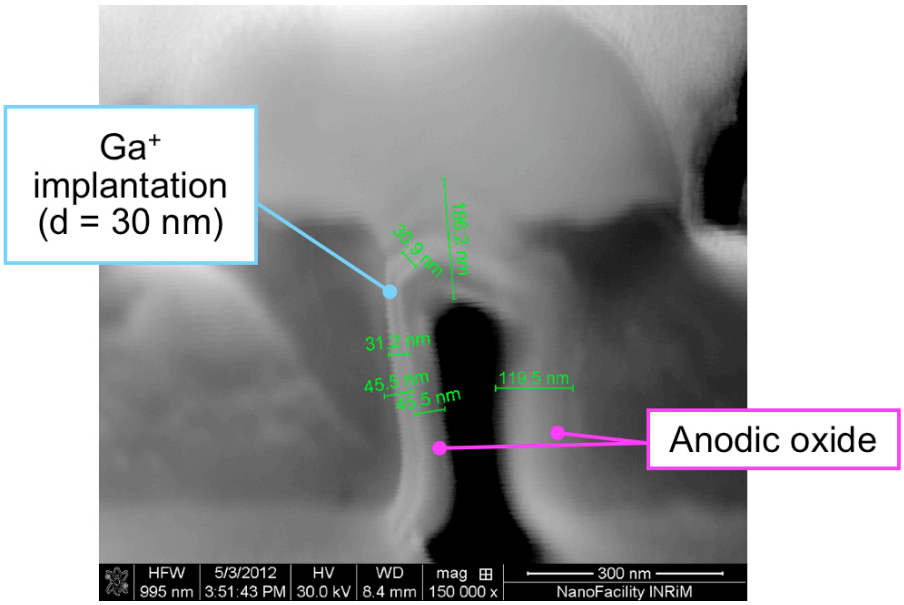

Figure 8.9. A STEM picture of the nanoSNS device after the anodization process. The Ga^+ ions implantation is visible (clearer layer) with a thickness of 30 nm, embedded into the anodic oxide.

masking, post-FIB wet or dry etching, nor resist removal. Accordingly, the entire device fabrication becomes more appealing due to the drastic reduction of the fabrication steps compared to the others.

8.4 The electrical characterization of the nanoSNIS device

The 3D SNIS device is extremely sensitive to electrostatic discharge due to small capacitance value (few fF), and a three-level shorting protection was adopted during its electrical characterization, at the liquid helium temperature. In particular, a proper wiring was included at the device level, in the packaging through a shorting Printed Circuit Board (PCB) and at the measurement set-up level (Appendix A.1) thanks to shorting plugs on coaxial connections.

The I-V response concerning a 3D SNIS junction typical of a batch of several devices, with an effective area of about 280 x 280 nm^2 and I_c of about 200 μA is shown in Figure 8.10, and the overdamping behavior is clearly maintained. This junction is characterized by J_c of 250 kA/cm^2 , with R_n of 1.6 Ω and V_c of 320 μV ($V_c = I_c \cdot R_n$, being I_c the critical current and R_n the normal state resistance of the junction). The I-V curve does not present any thermal film transition, and the normal resistance is obtained from the tangent to the curve at a current about two

times the I_c. This choice is to be sure to be out of superconducting conditions and to calculate the resistance due only to the tunneling of normal electron without any other contribution.

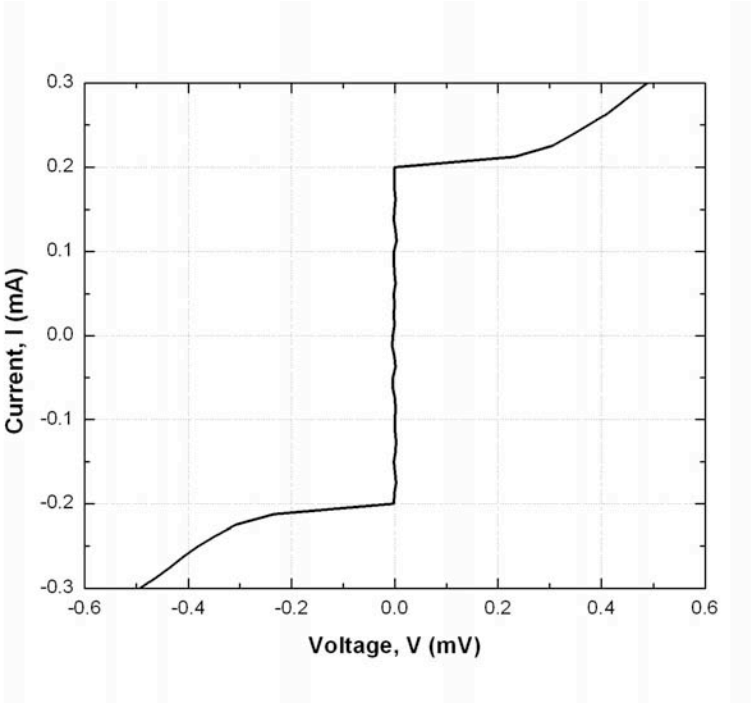

Figure 8.10. Current–voltage characteristic referred to a 3D FIB SNIS junction with a V_c of 320 μV and I_c of 0.2 mA.

In Figure 8.11 (i.e. squares) the 3D SNIS current density is compared to J_c values of SNIS junctions with larger areas [98, 99], and fabricated with a classical "window" method merging optical and electron-beam lithography with the RIE technique. The increase of J_c by reducing the junction dimensions is presently not completely understood. Indeed, although the oxide layer of the barrier is very thin (about 1 nm), showing a transparency distribution of the Schep-Bauer type [28, 100] any effect related to the presence of pinholes was not observed [101].

This effect could be related to the occurrence of oxygen diffusion from the barrier to the outside through the edges of the junctions during FIB self-annealing or RIE. Both these processing steps are highly energetic and in vacuum, and the oxygen effusion could occur. However, it is not possible to exclude the formation of defects in the barrier due to FIB redeposition, but the successive anodization process converts the amorphized layers into oxide, eliminating possible leakage currents through the defective sites. In order to ascertain this phenomenon, a deeper study is in progress by Transmission Electron Microscopy (TEM) and Electron Energy

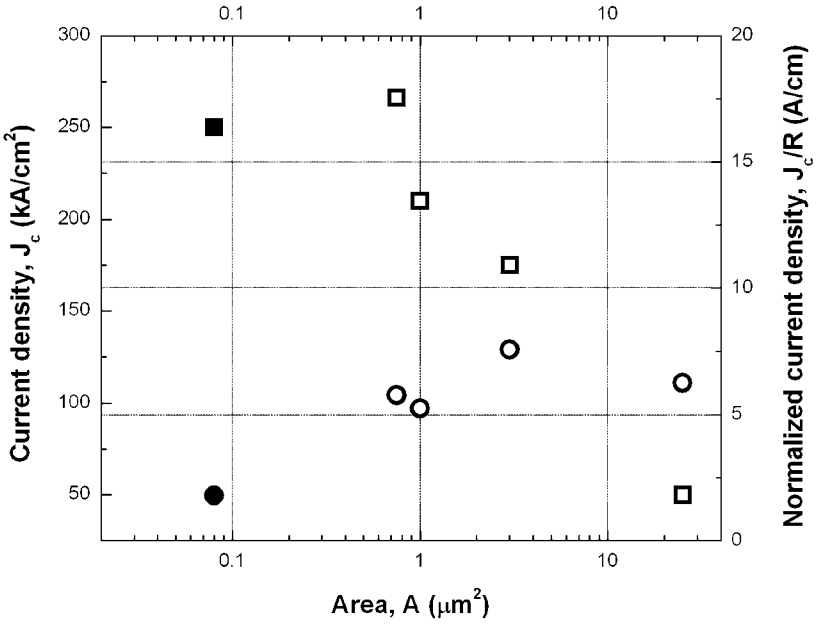

Figure 8.11. Current density (J_c, squares) and normalized current density (J_c/R, circles) versus SNIS junctions' areas, where R is the P/A (Perimeter/Area) ratio for FIB precess (solid marks) and classical "window" technique (open marks).

Loss Spectroscopy (EELS). The oxygen leakage from the aluminum oxide or from the defects is probably located at the AlO_x/vacuum interface, on the sidewalls of the junctions. Consequently, the barrier transparency depends on the ratio P/A (Perimeter/Area and named R in this context), hence J_c increases for increasing values of R (i.e. smaller junction sizes). Plotting the normalized J_c/R versus SNIS junctions' areas (Figure 8.11, i.e. circles), a reasonably consistent value of J_c/R (around 6 A/cm) can be observed for devices fabricated by EBL and optical lithography (A $\geq$ 0.7 μm^2, Figure 8.11, i.e. open circles). This result seems to confirm the influence of R on J_c. Regarding the junction fabricated by FIB sculpting (A = 0.08 μm^2, Figure 8.11, i.e. solid circle), the anodization of the barrier edges partially compensates the oxygen leakage, entailing a smaller J_c/R ratio.

A measurement of the RF response of the junction to a microwave radiation at 70 GHz (Figure 8.12) clearly shows quantized steps up to $n = 3$. The $n = 2$ step, due to the high characteristic voltage of the SNIS junction, is enhanced compared to the $n = 1$ step [34]. The inset in Figure 8.12 represents the $n = 1$ step ($\Delta I = 90$ μA) optimized by varying the RF power in agreement with the Shapiro relationship [14, 102].

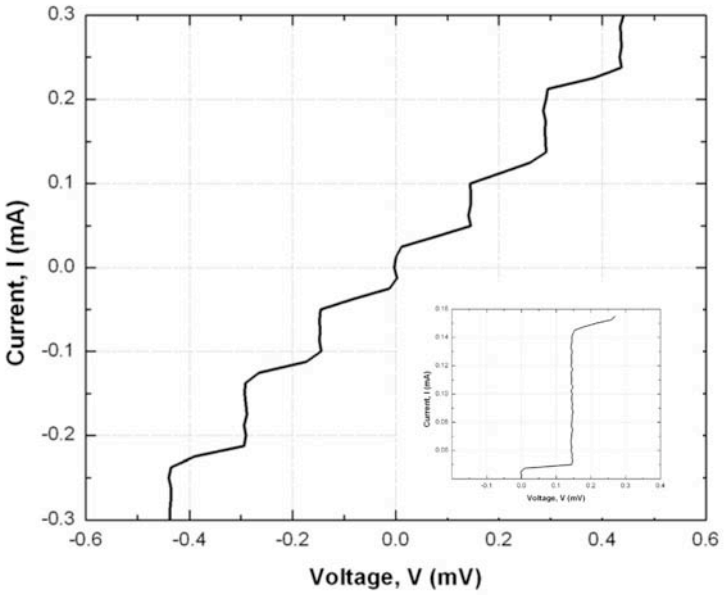

Figure 8.12. Quantized voltage steps of a 3D FIB SNIS junction, measured at about 70 GHz, at 4.2 K. The $n = 2$ step is enhanced compared to the $n = 1$. The inset represents the optimized $n = 1$, with ΔI of about 90 μA.

8.5 Conclusions

Overdamped Nb/Al-AlO_x/Nb SNIS junctions were fabricated on a deep submicrometer scale by a 3D FIB etching technique, where the combination of SEM and FIB revealed a powerful tool to create complex 3D nanostructures featuring good dimension control.

Exploiting this method, the junction area is easily controlled, still maintaining the fundamental properties of the junctions fabricated by the other "window" resist-based approaches. The overdamping is easily reproduced, and the presence of Shapiro steps measured at 4.2 K validates the innovative and alternative fabrication process for SNIS nanostructuring. Moreover, the number of fabrication steps has been drastically reduced compared to the previous processes.

Finally, the 3D FIB etching method reported represents a promising technique for the fabrication of devices requiring mesoscopic tunneling junctions, nanoSQUID and when single Josephson junctions should be embedded into more complex circuits previously defined by standard optical lithography.

Conclusions

This thesis was focused on the study and the realization of superconducting devices based on Nb/Al-AlO_x/Nb SNIS (Superconductor - Normal metal - Insulator - Superconductor) Josephson junctions, by investigating and optimizing several fabrication processes exploiting different lithographic techniques in order to gradually downscale the junctions dimensions.

In particular, a reliable and reproducible fabrication process to realize multilayered SNIS-based devices at the micrometer level has been implemented exploiting the thin film technology as a combination of different technique: RF sputtering for thin film deposition, optical lithography for pattering, dry etching for material removal, etc). A good control on electrical features of Josephson junctions has been obtained by trimming of fabrication parameters (oxidation exposure and normal metal thickness).

A binary-divided Programmable Josephson Voltage Standard (PJVS) based on 8192 SNIS Josephson junctions (5 x 12 μm^2) connected in series has been realized to reproduce 1 Volt as output voltage. By the RF electrical characterization stable quantized voltage steps of different order have been measured. Their large amplitude in current makes this technology appealing for the development of a new generation of JVS. Quantized steps were observed also at operating temperatures above liquid helium (4.2 K), making these junctions promising for voltage metrology application. This open the possibility to use SNIS junctions in cryocooling systems.

Successively, an Electron Beam Lithography (EBL) process has been optimized to reduce the junction dimension at the submicrometer scale. Thereby, the optical lithography has been replaced, and the "micro" fabrication process has been adapted by properly evaluating fabrication and electrical parameters considering the downscaling of the areas. Meanwhile, the Reactive Ion Etching (RIE) and the anodization steps have been adapted and calibrated as a function of patterned dimensions by EBL, in order to preserve the resist and avoid uncontrolled reductions of sizes.

SNISs in single-junction configuration have been realized by EBL, scaling the typical size (5 x 5 μm^2) reached by optical lithography down to 800 x 800 nm^2. The intrinsic overdamping behaviour is maintained also at subμm level. A proper scaling of electrical parameters was observed and quantized voltage steps were also

measured, validating the new fabrication process.

An innovative fabrication method exploiting the three-dimensional 3D FIB sculpting has been implemented on the SNIS multilayer structure to further downscale the junction dimensions at the nanometer level. This approach represents an alternative solution to the classical EBL and allows for an accurate control of the junction dimensions.

Exploiting this method, SNIS-structured junctions were fabricated drastically reducing their dimensions down to about 300 x 300 nm^2 by using a 3D FIB nanosculpting method. A good control on dimensions has been reached and the "multi-step" standard fabrication process has been considerably simplified. Furthermore, the DC and RF characterization demonstrated the good quality of the nanoSNIS junctions.

Finally, this work has thereby led to the definition and validation of a new generation of devices and processes down to the nanometer scale, and these approaches represent precious experiences of nanofabrication valuable for new research activities and projects.

Appendix A

The cryogenic measurement set up

A.1 The electrical measurement set up

All the electrical measurements of Nb/Al-AlO$_x$/Nb SNIS prototypes realized in this thesis, were carried out in a cryogenic ambient, at liquid helium temperature of 4.2 K, in a transportable and magnetically shielded Dewar (Figure A.1).

The Josephson junction device is mounted inside a high-permeability magnetic shield at the end of a cryoprobe that drives the transition between a liquid-helium Dewar and the room-temperature environment (Figure A.2). The shield is able to protect the Josephson device from electromagnetic interference that could cause step transitions and magnetic flux trapping.

The current-voltage I-V characteristics are measured with the standard four terminal technique to avoid contribution of the leads. A personal computer is connected to the instrumentation and controls a current source (Keithley 220) and a multimeter (HP 34401A), a Visual Basic program plots the I-V curve in real time and store the data in .dat files. A view of the measurement set up is reported in Figure A.3.

During RF measurements a gunn oscillator is located at the top of the cryoprobe, and were used 70 GHz, 75 GHz and 94 GHz gunns for different samples to study the junctions' behaviour at different frequencies. Gunns are supplied with an Agilent E3631A DC power supply. To maximize microwave power with large arrays, an amplifier is series connected to the gunn in order to obtain power up to 100 mW. For precision measurements, the gunn frequency is monitored and locked with an EIP 578 Source Locking Microwave Counter.

Temperature measurements are performed moving the cryoprobe above liquid helium level, and at the end of the sample holder, at the same height of the device, is fixed a cryogenic silicon diode thermometer (Lakeshore DT 470) connected to a Lakeshore 332 temperature controller. A heater is connected to the same controller

to obtain a good temperature stability.

Figure A.1. The magnetically shielded Dewar for the electrical characterization of Josephson junctions, in INRIM.

Figure A.2. A Josephson junction device (left) mounted at the end of a cryoprobe (right), inside a high-permeability magnetic shield (right, inset).

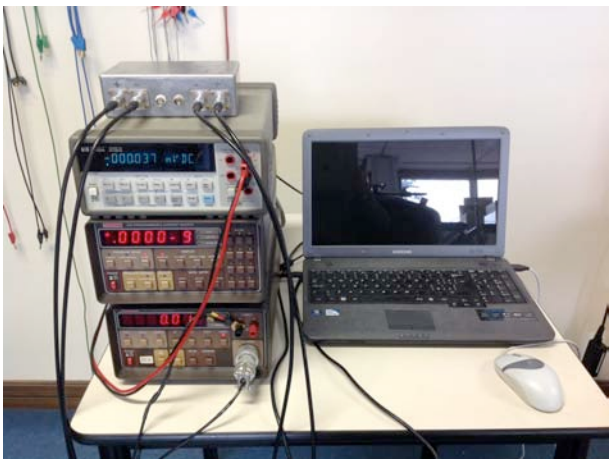

Figure A.3. The measurement setup for Josephson's junctions electrical characterization.

Appendix B

Recipes

B.1 Standard positive optical lithography

1. Substrate cleaning with acetone and isopropanol in ultrasonic bath (5 minutes each)
2. AZ 5214E resist spinning at 3500 rpm for 30 s (thickness: ∼1.5 µm)
3. pre-bake on hotplate at 110°C for 3 min
4. UV masked exposure for 9 s
5. Development: AZ developer:deionized water (DI) 1:1 for 20 s
6. Rinse: deionized water (DI) for 20 s

B.2 Standard negative optical lithography

1. Substrate cleaning with acetone and isopropanol in ultrasonic bath (5 minutes each)
2. AZ 5214E resist spinning at 4000 rpm for 30 s (thickness: ∼1.2 µm)
3. pre-bake on hotplate at 95°C for 1 min
4. UV masked exposure for 9 s
5. post-bake on hotplate at 95°C for 1 min
6. UV flood exposure for 28 s
7. Development: AZ 351B:deionized water (DI) 1:4 for 10 s

8. Rinse: deionized water (DI) for 20 s

B.3 Nb/Al-AlO$_x$/Nb Trilayer deposition for micrometer SNIS JJs

1. Base pressure: $2 \cdot 10^{-7}$ mbar
2. Substrate cleaning sputter etching: 500 V-DC bias for 5 min
3. Nb target cleaning pre-sputtering: 1000 V-RF for 10 min
4. Nb deposition: 120 nm with rate 0.7 nm/s
5. Al target cleaning pre-sputtering: 1000 V-RF for 10 min
6. Al deposition: 30 -100 nm with rate 1.3 nm/s
7. Oxidation $\sim$ from 160 to 400 Pa $\cdot$ s
8. Nb target cleaning pre-sputtering: 1000 V-RF for 10 min
9. Nb deposition: 120 nm with rate 0.7 nm/s
10. Lift-off: acetone for 1 night

B.4 Nb/Al-AlO$_x$/Nb Trilayer deposition for subμm SNIS JJs

1. Base pressure: $2 \cdot 10^{-7}$ mbar
2. Substrate cleaning sputter etching: 500 V-DC bias for 5 min
3. Nb target cleaning pre-sputtering: 1000 V-RF for 10 min
4. Nb deposition: 120 nm with rate 0.7 nm/s
5. Al target cleaning pre-sputtering: 1000 V-RF for 10 min
6. Al deposition: 50 nm with rate 1.3 nm/s
7. Oxidation $\sim$ from 160 to 200 Pa $\cdot$ s
8. Nb target cleaning pre-sputtering: 1000V-RF for 10 min

9. Nb deposition: 50 nm with rate 0.7 nm/s
10. Lift-off: acetone for 1 night

B.5 Nb/Al-AlO$_x$/Nb Trilayer deposition for 3D FIB nanoSNIS

1. Base pressure: $2 \cdot 10^{-7}$ mbar
2. Substrate cleaning sputter etching: 500 V-DC bias for 5 min
3. Nb target cleaning pre-sputtering: 1000 V-RF for 10 min
4. Nb deposition: 400 nm with rate 0.7 nm/s
5. Al target cleaning pre-sputtering: 1000V-RF for 10 min
6. Al deposition: 80 nm with rate 1.3 nm/s
7. Oxidation $\sim$ 300 Pa $\cdot$ s
8. Nb target cleaning pre-sputtering: 1000V-RF for 10 min
9. Nb deposition: 400 nm with rate 0.7 nm/s
10. Lift-off: acetone for 1 night

B.6 EBL process for patterning of subμm SNIS JJs area

1. Substrate (trilayer on Si/SiO$_2$ substrate) cleaning with acetone and isopropanol in ultrasonic bath (5 minutes each)
2. ma-N-2405 resist (by *Microresist Technology*) spinning at 3000 rpm for 30 s + bake on hotplate at 90°C for 1 min - (total thickness: $\sim$ 500 nm)
3. EBL exposure in FEI Quanta3D^{TM} FEG system
   (a) Acceleration voltage: 30 kV
   (b) Working distance: 5 mm
   (c) Beam current: $\sim$ 10 pA
   (d) Exposure dose: 60 μC/cm^2

4. Development: ma-D-532 for 10 s
5. Rinse: deionized water (DI) for 5 min

B.7 Low Vacuum EBL process for optical mask fabrication

1. Substrate (Corning glass) cleaning with acetone and isopropanol in ultrasonic bath (5 minutes each)
2. RF 50 W sputtering of $Fe_{20}Ni_{80}$80 nm at argon pressure of $1 \cdot 10^{-1}$ mbar (rate $\sim$ 0.8 Å/s)
3. (2x) MRT MA-N-2401 resist spinning at 3000 rpm for 30 s + bake on hotplate at 90°C for 1 min - (total thickness: $\sim$ 200 nm)
4. EBL exposure in FEI Quanta3D^{TM} FEG system (Low Vacuum mode)
   (a) Acceleration voltage: 30 kV
   (b) Chamber H_2O vapor pressure: 40 Pa
   (c) Working distance: 5 mm
   (d) Beam current: $\sim$ 1 nA
   (e) Exposure dose: 60 µC/cm^2
5. Development: MA-D 532 for 10 s
6. Rinse: deionized water (DI) for 5 min
7. Sputter-etch 100 W with chamber argon pressure $1 \cdot 10^{-1}$ mbar for 12 min

B.8 3D Focused Ion Beam trilayer milling for nanoS-NIS junction fabrication

1. FIB perpendicular milling in FEI Quanta3D^{TM}FEG dual/beam system
   (a) Acceleration voltage: 30 kV
   (b) Beam current: big areas @ 1 nA (lamella: 1 µm), small areas @ 50 pA (lamella: 0.5 µm) - cleaning - 10 pA (lamella: 0.4 µm)
2. FIB parallel milling

(a) Acceleration voltage: 30 kV

(b) Beam current: 10 pA

(c) Milling area: 200 x 600 nm^2

B.9 Fixed current-limited voltage anodization process

1. Electrolyte:

   (a) 8.3 g ammonium pentaborate

   (b) 60 ml ethylene glycol

   (c) 40 ml distilled water

   (d) Stirred and heated to about 100°C

2. Fixed current (10 μA) gives, on the resist window area, an anodization rate of $\sim$ 60 mV/s

3. Voltage limit: 60 V ($\sim$ 60 nm anodic oxide)

Appendix C

Instrumentation

C.1 High Vacuum RF Sputtering system

Figure C.1. Picture of the Leybold high vacuum RF Sputtering system, at INRIM. This system is equipped with Nb, Al, and SiO_2 targets.

C.2 Reactive Ion Etching system

Figure C.2. Picture of the Reactive Ion Etching system, at INRIM. This system is equipped with CF_4, CHF_3, O_2, and Ar gases.

C.3 ISO5 Clean room and optical lithography facilities

Figure C.3. Picture of the "Thin Film" ISO5 clean room Laboratory at INRIM. From left to right: two mask aligners for the optical lithography, the spinner for the resist deposition and a hood for chemical processes (substrate cleaning and resist development).

C.4 FEI Quanta 3D^{TM} dual-beam system

Figure C.4. Picture of the FEI Quanta 3D^{TM} dual-beam system, at NanoFacility Piemonte (http://www.nanofacility.it). The electron (vertical) and the ion (52° on the left) columns collide beams in the eucentric point at a working distance of 10 mm from the electronic final lens. This powerful setup can operate under different chamber pressure from the high vacuum range up to 500 Pa of water vapor. The NPGS lithography tool control both colums via a CAD pattern and relative exposure recipe opening a wide range of applications in the nanotechnology field.

C.5 Mask aligner

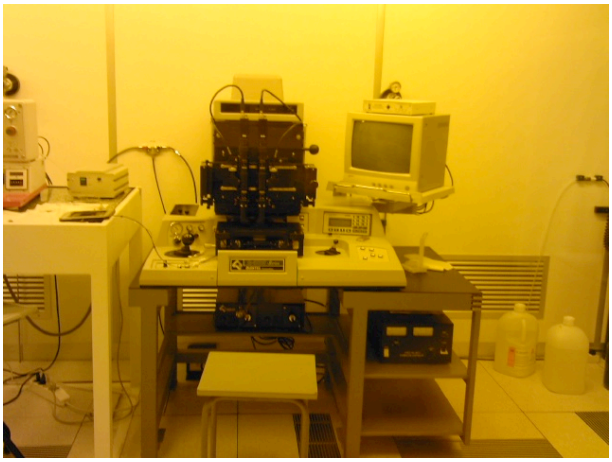

Figure C.5. Picture of the Quintel-Neutronix mask aligner for optical lithography, in the "Thin Film" ISO5 clean room Laboratory.

C.6 Anodization setup

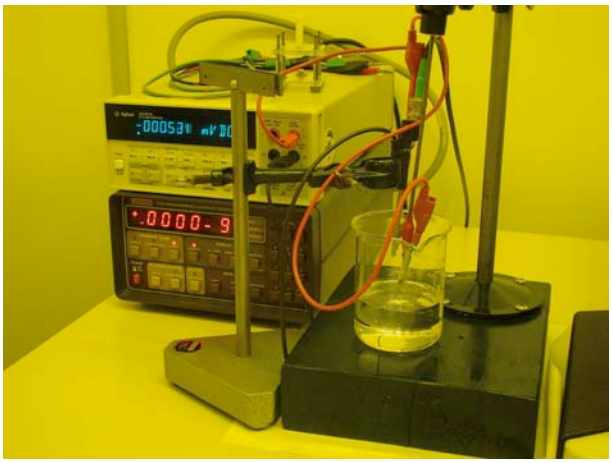

Figure C.6. Picture of the anodization setup. The current is imposed by the Keithely 220 (bottom) current source and the voltage is monitored by means of the Agilent digital multimeter 34401A (top).

C.7 Wedge bonder

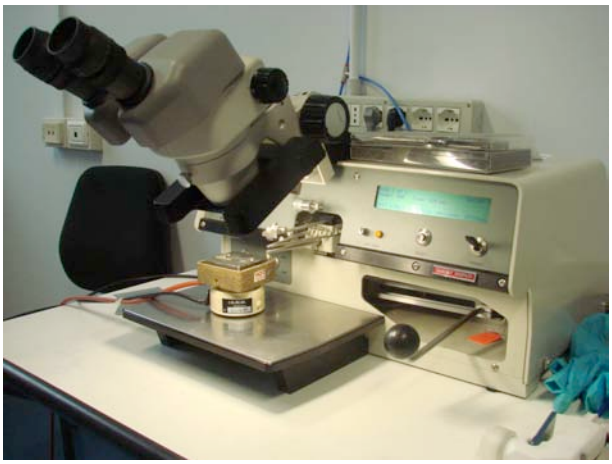

Figure C.7. Picture of the wedge bonder used to realize the micro-contacts from lithographic pads and macroscopical stripes.

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