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Original
Design issues of a standard cell BiCMOS carrier transceiver on low voltage power lines / Lazarescu, M.T., Sartori, M., Civera, P.. - ELETTRONICO. - (1995), pp. 375-380. (Semiconductor Conference 1995 (CAS '95) Sinaia, Romania October 1995) [10.1109/SMICND.1995.495040].

Availability:
This version is available at: 11583/2507493 since:

Publisher:
IEEE / Institute of Electrical and Electronics Engineers Incorporated:445 Hoes Lane:Piscataway, NJ 08854:

Published
DOI:10.1109/SMICND.1995.495040

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06 October 2026

Design Issues of a Standard Cell BiCMOS Carrier Transceiver on Low Voltage Power Lines

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ABSTRACT

In this paper are described some of the issues of the mixed signal standard cell VLSI design with emphasis on the practical experience resulted from designing a carrier transceiver in SGS-THOMSON 2μm BiCMOS technology. Are presented the circuit block structure, some advantages and disadvantages of the standard cell design approach, the testing strategy we implemented, and finally some practical conclusions as resulted from our experience.

1 Introduction

In the middle of the informational explosion of our days, the communications are essential. We assist at a boom of the communication equipment offer, the products on the market featuring a huge diversity in performances. In this conditions the product time-to-market is of crucial importance and the design approach should be chosen taking this aspect into account. Moreover, for ASIC circuits it is very important to reduce the NRE (Non Recurrent Expenses), that is to have a bug-free and specifications compliant design at the first or after very few runs. To achieve this goal the design process should be as much as possible supervised by automatic CAD tools such as simulators, electric and layout rules checkers, synthesis tools for the digital parts and for switched capacitor circuits, etc.

For mixed ASIC design, the standard cell (SC) approach is the most complying to this requirements. The foundries offer of mixed mode signal SC is widening and diversifying giving a better choice of performance in order to match tighter design requirements. Fast analog models are also provided that, together with efficient mixed mode simulators and powerful

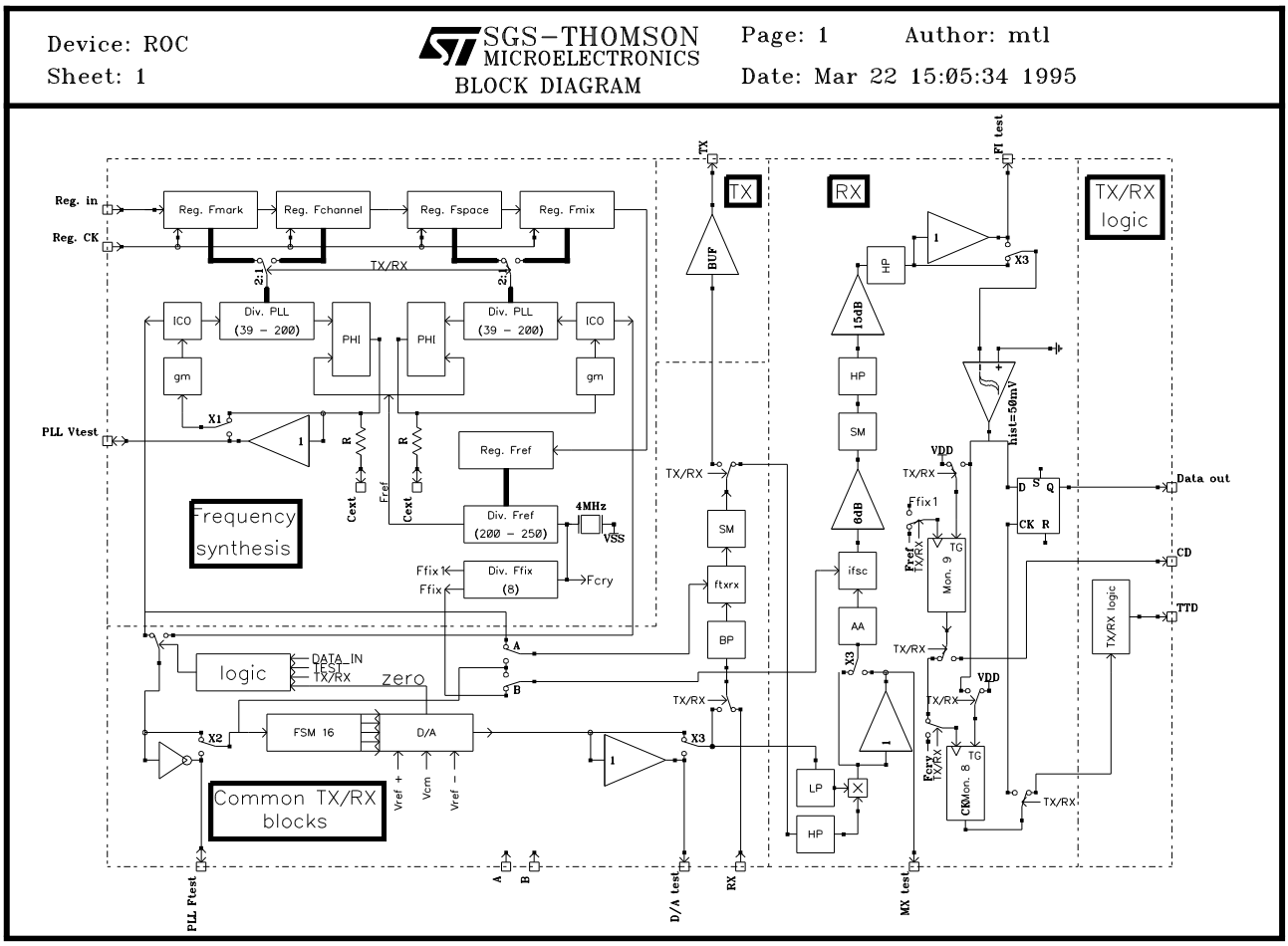

Figure 1: Carrier transceiver block schematic

computers make possible the simulation of large parts of the circuit as a whole allowing a better check of the functionality and specifications compliance of the design.

The SC libraries hidden the most of the boring and very time consuming layout related issues to the designer allowing a larger part of the design time to be allocated to system and functional issues. This way the design time and NRE are considerably reduced with better specification compliance.

In this paper will be presented the main characteristics of a mixed signal design. The particularities of the SC approach will be emphasized. The practical experience of a carrier transceiver design using the standard cell approach in the 2μm BiCMOS technology of SGS-THOMSON will be used to annotate the presentation.

2 System block schematic

The block schematic of the carrier transceiver as represented in the ADS design environment of SGS-THOMSON is reported in figure 1. It is composed of the following main subsystems:

`Frequency synthesis` block which generates all the square wave frequencies used by other blocks in the circuit both in RX and in TX operation modes. This block in turn is composed of:

- a crystal chain which generates several fixed frequencies;

- two programmable PLL frequency synthesisers, one of which with testing facilities embedded;
- preset registers storing values of the constants corresponding to the various frequencies PLLs have to generate.

`Common TX/RX blocks` part that contains most of the transmission blocks which can be reused in RX mode. It is composed of:

- a sine wave synthesizer composed of a 16-states Finite State Machine (FSM) driving a dedicated D/A converter;
- a logic block synchronized with sine wave zero crossing with positive derivate to switch the input of the FSM from one PLL to the other according to the value of the input data;
- a radio frequency switched capacitor filter with antialiasing and smoothing continuous time filters;
- bidirectional test points placed before and after the sine wave generator.

`TX` that contains only the transmission output buffer, which is the only TX dedicated block;

`RX` that contains almost all the receiver chain (excepting the input switched capacitor filter shared with the transmission part):

- an analog multiplier acting as frequency mixer to scale down the received signal frequency;
- an Intermediate Frequency (IF) switched capacitor filter with smoothing and antialiasing continuous time filters;
- two signal amplifiers rising the receiver gain to 21dB;
- several high-pass filters to reject the DC offset along the chain;
- an externally programmable hysteresis comparator;
- a digital demodulator and carrier detect circuit;
- test points after the analog multiplier and before entering the hysteresis comparator.

`TX/RX logic` containing operation mode switching logic, power-on reset, transmission timeout, etc.

The block functional description above was given to make an idea of the complexity and the dimensions of the project. Despite that, due to standard cell approach of the design, the use of a high level synthesiser and silicon compiler for the switched capacitor filters design, and of the logic, electric, and mixed mode simulation facilities available under the SGS-THOMSON ADS design environment, the chip design was completed in one year time with the continuous work of approximately one full-time person. The chip size is 28mm^2.

3 Mixed signal standard cell approach main issues

There is a great deal of particularities of the standard cell design of mixed mode circuits. Next we will try to summarize some of the most important we have met during this project.

First of all it is to be noted that the library cells available are pushing the designer towards a design style and solutions that are very close to the usual discrete components ones. The main advantages of this design style are:

- the use of the high level cells available in the library leads to a safer design. Unlike the design at transistor level when the designer has the whole responsibility for the design relying only on the previous experience and on the simulations result, each of the library cells is well tested and characterized by the foundry that guaranties its performances and the accuracy of the simulations results based on extensive test runs;

- for the analog standard cells fast simulation macromodels are provided that can be used to run electrical simulations on large subsystems in order to check the proper operation of the individual blocks once interconnected. If on the contrary, the design is made at transistor level, only small size circuits can be simulated and load effects or large loops with long transients (such as a PLL) pose serious simulation constraints;

- when operating with high level functional blocks to design the circuit, the designer does not have to cope anymore with circuit and layout details such as transistor sizes and matching, etc., but can pay more attention instead to system issues, block implementation, design for testability, etc.;

- the ease of building blocks with standard cells offers the designer the possibility to realize, simulate, and compare different implementations of the same circuit block and to choose the most suited structure for each particular case. Circuit modifications can be made easily and safely in case of changes in specifications or added features;

- the enormous amount of time saved designing with standard cells can be used to extensively simulate large parts of the circuit in full temperature range and technological process spread, increasing this way the probability of a first time working and reliable circuit.

The most important drawback of the standard cell design approach is that it is not possible to exploit the whole resources of a given technology. This is why blocks may need a transistor level design using either single transistors (with a few choice of dimensions), current mirrors, etc. provided as standard cells in the library or taking the whole freedom in defining a full custom layout for some blocks. It is better to avoid the last solution, but the choice depends on how many "elementary" cells (like single parametrized transistors, current mirrors, differential stages, etc.) are available on the library.

All the standard cells of the same type have the same height. Usually the analog cells are higher than the digital cells what causes analog and digital cells to be placed in different rows in the layout. Since there is always some small amount of logic to be placed near the analog cells (such as inverters used as output buffers for analog comparators, buffers for the power down signal for the analog cells, etc.), the ADS environment library offers digital cells with analog height, that can be abutted in analog rows. The designer has to take care to place this special type of cells whenever required and to specify the same supply as for the analog cells they have to stay with on the layout to avoid a long routing from the digital part of the layout.

The switched capacitor filter synthesiser and compiler proved to be of great help in the design. Using these tools it is possible starting from a high level description of the filter mask, zeros and poles position, etc. or any valid SWITCAP[1] netlist to semi-automatically generate the whole layout of the switched capacitor circuit providing the designer with a SWITCAP netlist (if synthesis was started from a high level filter description) and with the schematic capture of the circuit ready to be simulated with an electrical simulator.

[1]SWITCAP is a simulator dedicated to switched capacitor circuits simulation developed at Columbia University, New York, U.S.A.

4 Testing

Even designing with standard cells we cannot be sure to avoid all the design errors therefore we placed in the circuit several test points creating an efficient test structure. The observability and testing features are very important for a new design because they ease the chip debugging and redesign.

Besides the normal inputs and outputs of the circuit we placed several analog and digital IO test pads activated with special external test signals in the key points of the circuit after a long observability analysis. The test point capabilities are to monitor the signal that passes across them or to cut it and supply a signal from outside as input for the following block.

The test point disposition in the circuit was carefully chosen also with the target of allowing for the important subsystems the injection of an externally synthesized signal that emulate the output of the preceding block so that the rest of the circuit can be tested in normal operation even if one or several block failure occurs.

A first analog IO test point is placed in the loop of one of the PLLs (see figure 1). It allows monitoring the command voltage of the VCO and to impose externally the command voltage in order to extract the VCO voltage-frequency characteristic or in case of PLL failure.

A digital IO test point is placed before the sine wave shaper. This point can monitor the output frequencies of the two PLLs and can also force an external input frequency for the sine wave shaper in case of general failure of both PLLs. If one of the external A or B signals are becoming active, this test point can be used also to provide from outside the sampling frequency for the switched capacitor filters.

The output of the sine wave shaper is monitored by an analog IO test point so that in conjunction with the preceding test point the sine wave shaper can be isolated and tested independently from the rest of the circuit. This test point is used in transmission mode to force the input of the common TX/RX switched capacitor filter while monitoring the output of the same filter at the TX output pad. In RX mode it can be used to feed the locally generated frequency into the multiplier while the other mixer input is injected from the normal RX input pad.

Another analog IO test point is placed at the output of the analog multiplier. This can be used to monitor the output of the multiplier for test purpose and also to inject an external signal into the input of the IF chain.

At the end of the IF chain is placed the last test point, an analog IO. This is designed to check the whole IF chain in pair with the test point at the output of the multiplier. It can also supply an external signal to the hysteresis comparator to check its functionality, the hysteresis value, and the hysteresis external regulation. Moreover, it is used to provide test signal for the digital demodulator and carrier detect circuits via the hysteresis comparator. The normal operation of the digital blocks can be inspected at the outputs of the receiver and of the carrier detect circuit.

5 Conclusions

The practical experience of designing a complex mixed signal circuit using a standard cell approach showed us that the SC design style is very efficient. Of course, this efficiency is paid in larger designs and in constraints regarding the choice of the circuit solution.

We encountered however different kinds of problems during the design and some of them could be avoided by a careful initial check of the design environment and through a selection of the foundry with respect not only to technology performance but also to completeness of the

libraries and cells electrical specifications:

- we need for the PLL VCO high performances so we had to design part of them at transistor level, that is using standard cell transistors and current mirrors. This increased the risk of non functioning for this block because of process and temperature spread so we had to provide external adjustments to compensate this influences;
- the ADS environment did not provide a logic circuit synthesiser so we had to design all the logic parts by hand. As the digital part of this circuit is quite complicated, this process took us a lot of time and can become easily a source of errors;
- the switched capacitor silicon compiler did not check all the user input creating the possibility of human-introduced errors;
- fast simulation models for some analog cells proved to be erroneous or to have a bad convergence in mixed mode simulations;
- the ADS library documentation was faulty or confuse sometimes;
- some of the simulators provided with the design environment had bugs and could not be upgraded because of version incompatibility.

Despite these drawbacks we do believe we have chosen the best technology–design environment trade-off taking into account the complexity and the narrow specifications of the chip.

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