Latch-up test measurement for long duration space missions

# Latch-Up Test Measurement for Long Duration Space Missions

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*Abstract*— **Long duration space missions require extremely high reliable components that must guarantee components functionality without incurring in damaging effects. When Integrated Circuits (ICs) are considered, radiation hardened technology should be mandatorily adopted, since it allows to adequately protect against Single Event Latchup (SEL). In this paper we present a complete test measurement experimental setup in order to measure the SEL occurrences at high temperature conditions. The SEL test setup and the executed experiments are described. The experimental environment has been used to test SEL effects in Gate Arrays MG2 Radiation Hardened technology with respect to strike of heavy ions. We performed a complete radiation test at GANIL radiation facility, executed at high temperature by monitoring current absorption and analyzing the functionality of the MSDRX ASIC core. Experimental results show that a drastic improvement of the device SEL sensitivity is observed for high power supply voltages.**

***Keywords: Single Event Latch-Up, Current and Voltages Measurements, Radiation Hardened Technology***

## I. INTRODUCTION

Single Event Effects (SEEs) is a widely know phenomena that lead permanent or temporary damage due to heavy ion exposure. With the progressive scaling to smaller technologies, there is an increasing concern that circuits may be more susceptible to various mechanisms including Single Event Latchup (SEL), Single Event Burnout (SEB) or Single Event Gate Rupture (SEGR). In particular, the occurrence of SEL event happens when a parasitic NPNP feedback latch structure becomes biased into the on state due to a very dense track of electron-hole pairs which are created along the heavy ion track through the silicon. This latch-up is self-maintained since there is a positive feedback path which sustains it and that requires an external power cycle in order to be deactivated. SELs can be potentially destructive depending on the kind of involved parasitic circuit elements forming the silicon controller rectifier (SCR) [1][2][3]. Generally, a destructive SEL occurs when the device current is not limited and is not removed before the rupture of the affected junction, vice versa a non-destructive SEL occurs in case the latch-up event is self-limited thus preventing that the current draw damages the gate junctions or the bond wires. Eventually, a micro-latch effect may happen in case the device current remains below the maximum specified value. A removal of the power supply is required in all non-catastrophic SEL conditions in order to recover the correct device operations.

Several documented heavy-ions SEL test [4] demonstrated that physical damages may become worse and in some case evident with the increasing of LET and fluence. SEL test procedures are included in different official standard widely adopted to manage such kind of tests. An example of these standards are the ASTMF1192 or the EIA/JESD57. The common rules provided by the standards is that SEL test must be performed at the maximum Device Under Test (DUT) datasheet voltage and temperature and applying a fluence greater than 1E7 ions/cm$^2$.

Although recent investigations have been concentrated on nanometer technologies showing effects of temperature and angle of incidence for heavy ions on latch-up effects [5][6] and they demonstrated that latch-up cross-sections increase with both increases of temperature and incident angle, the usage of micrometer technologies such as 0.5 µm is still largely used in space avionic systems and nowadays, a wide set of communication and other satellite systems are currently adopting it. The results provided by tests of this technology under severe conditions evaluating its behavior, enable the adoption of 0.5 µm technology in a wider set of application fields including satellite systems working in extreme temperature and harsh environments [7] [8].

The main scientific contribution of the present paper is to provide the first high temperature radiation test analysis of the SEL sensitiveness of 0.5 µm radiation hardened technology. The SEL analysis has been performed on an ASIC developed by Thales Alenia Space Italy (TASI) and manufactured on the Atmel MG2RT 0.5 µm radiation hardened technology. The tests have been performed with heavy ion having in-depth penetration range at a working frequency of 75°C. A total of two devices were tested at an LET ranging from 66.34 MeV·cm$^2$/mg to 86 MeV·cm$^2$/mg at the temperature of 75°C and at the power supply voltages of 3.3 and 5.25 V. The two devices have been initially irradiated to a maximum fluence of 3E7 ions / cm$^2$ and they have been stimulated with a clock signal of 10 MHz applying static input signals. The devices have been monitored observing the current absorption and two output signals consisting in the clock spy and divider were observed in order to detect both permanent and temporary malfunctions. Based on the results, devices were found to have strong SEL threshold at high power supply voltage. Since we found that devices have a SEL sensitivity LET threshold of

72.1 MeV·cm$^2$/mg at 3.3 V while an LET threshold of 86.19 MeV·cm$^2$/mg at 5.25 V. Temporary effects have been also recorded during the runs and probably due to the influences of SEU effects. The paper is organized as follows: Section II provides background information about the MG2RT Atmel technology and the implemented ASIC design. Section III provides an overview on the Single Event Latch-Up effects causalities, while Section IV describes the test environment developed and the experimental setup executed. Section V presents the test measurement results. Finally, conclusions and future works are drawn in Section VI.

## II. Background on MG2 technology

The MG2RT technology is a 0.5 µm, array based, CMOS product family. MG2RT is manufactured using a 0.5 µm drawn, 3 metal layers CMOS radiation tolerant process. The base MG2RT series provide a cell architecture characterized by high routability of logic with dense compiled memories such as RAM, DRAM or FIFO. Clock distribution is controlled by PLL hardware and Clock Tree Synthesis (CTS) automatic software, besides, noise prevention techniques have been adopted both into the device array and in the periphery since three independent power supplies, internal decoupling, dependent supply routing and noise filtering improve the noise immunity of the functionality implemented on the device.

The I/O interfacing is guarantee by a flexible buffer interface that allows to configure as input, output, bi-directional, oscillator or supply each single DUT pin. In details, input buffers have CMOS or TTL non-inverting threshold and feature with and without hysteresis. The MG2RT technology support high frequency and design density which provoke large switching current spikes that can cause parasitic elements that can affect the behavior of the circuit functionality itself or erroneously influencing the external connected devices with ground bounce effects. In order to improve the noise immunity, the MG2RT technology includes two kinds of protection mechanisms: limitation of the I/O buffer switching noise and the protection of the I/O buffers against switching noise coming from the internal locations of the MG2RT internal array.

Particular cares are taken in account concerning the power supplier which has been investigated during the radiation tests performed in this work. The functionality of the circuits is protected versus noise glitches generated by the internal gates simultaneous switching or on the power supply buffers by including three features. The former is the integration of the decouple capacitors directly on the silicon in order to reduce the power supply drop; secondly the power supply network has been implemented into the technology matrix to reduce the number of parasitic elements such as inductance and resistance between cells and creating a virtual VDD and GND plane; the latter consists on a pass filter added between the cell matrix and the input and output buffers in order to limit the transmission of noise coming from the ground or VDD power supply of the matrix to the external device connection [9].

The circuit implemented on the MG2RT technology consists on the MSDRX ASIC that realizes the core of a TAS-I project transponder which includes in a single chip an Embedded Mini-Controller internally developed by TAS-I, the DSP function for up-link signal acquisition, tracking and demodulation. The ASIC also includes ancillary functions for interconnections with other device such as TC/TM interface, general purpose serial interfaces.

## III. The Single Event Latch-up Phenomena

The sources of radiations can be classified in different ways, depending on where the system is deployed. We can consider three so-called radiation environments: space, atmospheric, and ground radiation environments. In general, the space radiation environment is composed of particles trapped by planetary magnetospheres (protons, electrons, and heavier ions), galactic cosmic ray particles (heavy ions and protons) and particles from solar events, such as coronal mass ejection and flares, which produce energetic protons, alpha particles, heavy ions, and electrons. The maximum energy the particles have ranges from 10 MeV for trapped electrons up to 1 TeV for galactic cosmic rays (1 eV being equivalent to 16x10-21 Joules). Due to the very high energies involved, shielding may not be effective in protecting circuits, and therefore the impact of ionizing radiation on electronic devices should be investigated deeply, to devise effective fault compensation techniques. Atmospheric and ground radiation environments are quite different with respect to the space environment. Indeed, when cosmic ray and solar particles enter the Earth's atmosphere, they interact with atoms of nitrogen and oxygen, and are they are attenuated. The product of the attenuation process is a shower of protons, electrons, neutrons, heavy ions, muons, and pions. Among these particles, the most important ones are neutrons, which start to appear from 330 Km of altitude. Neutron density increases up to the peak density found at about 20 Km of altitude, and then it decreases until the ground level, where the neutron density is about 1/500 of the peak one. The maximum energy observed for the particles in the atmospheric radiation environment is about some hundreds of MeV.

At the ground level, beside neutrons resulting from the interaction of galactic cosmic ray and sun particles with the atmosphere, second most important radiation source is the man-produce radiation (nuclear facilities). No matter the radiation environment where the system is deployed, we have that when radiations interact with semiconductor devices two types of interactions can be observed: atomic displacement or ionization. Atomic displacement corresponds to modifications to the structure of silicon device, which may show for example displaced atoms, and it is out of the scope of this chapter. Conversely, the latter corresponds to the deposition of energy in the semiconductor, and it is focused in this chapter.

Radiations may inject charge (i.e., ionize) a semiconductor device in two different ways: direct ionization by the particle that strikes the silicon, or ionization by secondary particles created by nuclear reactions between the incident particle and the silicon. Both methods are critical, since both of them may produce malfunctions. When an energetic particle passes through a semiconductor material it frees electron-hole pairs along its path, and it loses energy. When all its energy is lost, the particle rests in the semiconductor, after having travelled a path length called particle range. The energy loss per unit path length of a particle travelling in a material is known as linear energy transfer (LET), measured in MeVcm2/mg: the energy loss per unit path length (MeV/cm) divided by the material

density (mg/cm3). As an example, a particle having an LET of 97 MeVcm2/mg deposits a charge of 1 pC/mm in Silicon.

Heavy ions inject charges in a semiconductor device by means of the mechanism called direct ionization. Protons and neutrons do not produce enough charge by direct ionization to cause single-event effects, although recent studies showed that single-event effects due to direct ionization by means of protons are possible in highly scaled devices. Indirect ionization is the mechanism through which protons and neutrons produce single-event effects. Proton, or neutron, entering a semiconductor device produces atomic reactions with silicon atoms, originating by-products like alpha or gamma particles. These by-products can deposit energy along their paths by direct ionization, causing single-event effects.

Semiconductor devices like pMOS or nMOS transistor contains several parasitic structures. These structures are composed of two bipolar transistors forming a silicon-controlled rectifier, as depicted in Figure 1. If the current resulting from ionization triggers the parasitic structure, a short circuit between power and ground lines is activated, resulting in a high current flowing in the device. In case such a current is not stopped promptly, permanent damage of the device is likely to happen.

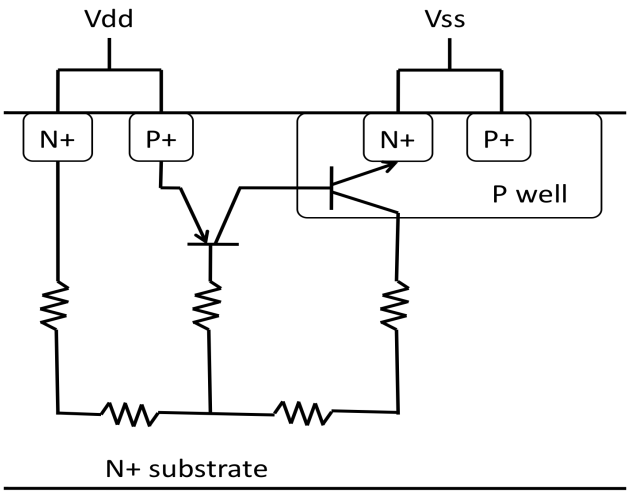


Fig. 1. The parasitic silicon-controller rectifies in a nMOS device.

SEL can be solved using two alternative approaches, one working at system level, and a second one working at layout level.

The first one uses current sensors at the system level to detect the excessive current flowing when the SEL is triggered to promptly shutdown the power supply. As the device is powered off, the SEL is stopped, and after a rest period sufficient for the injected charge to annihilate, the device can be power on again. The main drawback of this approach is that the circuit state is lost at power off and therefore a suitable synchronization phase is needed when the device is power on again. The second approach uses SEL-aware design guidelines during the layout of transistors. By exploiting guard rings, the parasitic silicon controller rectifier is broken, so that SEL are likely not to take place. To further improve such layout-based techniques, special manufacturing process can be exploited. To further reduce the SEL occurrence probability silicon grown on epitaxial layer, or silicon on insulator, is preferable over bulk silicon.

## IV. The Developed Test Environment

The developed test environment, illustrated in Figure 2, consists of a control board implemented using an Actel Flash-based FPGAs which controls and stimulates the Design Under Test (DUT) devices. The input signals are delivered and monitored by the control board which applies static input stimuli and the clock signal. The power and ground pins are connected to a separate board which is connected to power suppliers and oscilloscopes in order to monitor and store the read voltage and current values as well as the output patterns generated by the devices during the execution of the test. A separate power supplier is used to supply the thermal-resistors heating the device at the defined temperature conditions. During the execution of each run, data related to the voltage and current absorbed by the DUT are monitored and stored. Biased connections provide the link between the DUT power supplier and the scope monitors in the control rooms, while a scope interface provides the data coming from the DUT outputs and the status signals suitably generated by the control board. The scope-monitors read the $I_d$ value and the spy DUT signals. The temperature of the device has been monitored by a laser sensor suitably placed close to the DUT and pointed directly on the die.

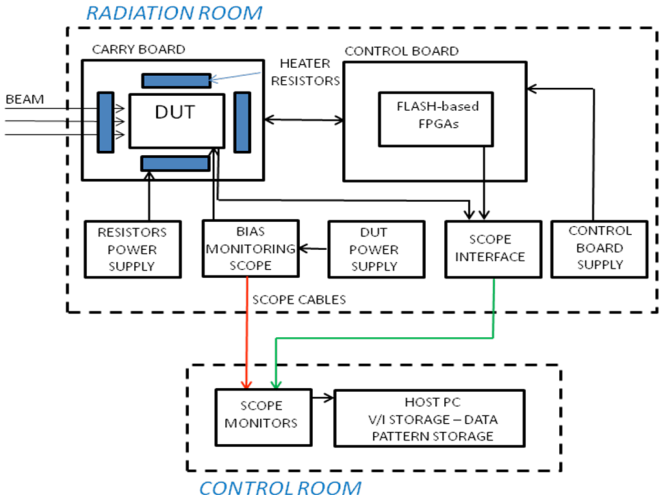


Fig. 2. The developed Test Measurement Environment.

The tests were performed at the GANIL radiation facility using a beam with $^{129}Xe$ at 49.99 MeV/u with a $46^{+}$ charge, with an energy, measured at the exit of the accelerator, of 49.86 MeV/u. In details, the energy of the beam, the linear energy transfer and the ranges for the silicon with a position of the components of 0 degrees is reported in Table I. The flux may vary during the experiment from 2,000 to 9,000 particles/s/cm$^2$.

TABLE I
Characteristics of The Beam

| Air [mm] | Degrader Al [µm] | Input Energy [MeV/u] | LET [MeV·cm$^2$/mg] | Ion Range [µm] |
|---|---|---|---|---|
| 220 | 350 | 17.87 | 45.43 | 184.93 |

In order to read the DUT $I_d$ value, a 3.4 ohm resistor was chosen to measure the current going into the device $V_{dd}$. The resistor has a low value that does not influence the electrical behavior of the DUT. The 3.4 ohm values has been selected in order to obtain a reasonable $V_{dd}/I_{dd}$ observation while accounting the resistance drop of the long cables between the test device and the scope (which length was approximately of 4 meters).

The Flash-based FPGA board, which is physically placed vertically with respect to the DUT board, provides the static and dynamic input stimuli to the DUT device. For the purpose of this test, we applied a logic start-up configuration of the DUT, which consist of a static pattern enabling the basic clock divider functionalities. Besides, an input clock frequency of 10 MHz has been generated by the control board and applied to the DUT.

## V. Experimental Results

The performed radiation test experiments have two main goals: the former is the verification of the MG2RT technology SEL robustness at the temperature of 75°C with high fluence condition of 3E7, the latter is the identification of the maximum LET SEL threshold of such technology devices.

For such purpose, according to the system requirements where the addressed MG2RT device will be employed, the SEL threshold current value has been settled around the 25% overhead with respect to the nominal device current at the temperature of 75°C which correspond to a threshold of 0.16 A and 0.247 A for the test at 3.3 V and 5.25 V respectively. This conditions has been directly monitored by a multimeter before activating the beam and with the DUT at the temperature of 75°C. The set of beam runs performed are depicted in Table II where for each addressed run we indicated the device sample used, the maximal fluence, the device voltage power supply, the LET, the identification of the SEL effect and finally the number of SEU effects observed. Please note that the LET values have been obtained by suitably tilting the device and by using a degrader.

TABLE II
Radiation Experiment Results

| Run [#] | Device Sample | Maximal Fluence | Device Voltage [V] | LET [MeV·cm$^2$/mg] | SEL effect | SEU Effects [#] |
|---|---|---|---|---|---|---|
| 1 | A | 2.44E7 | 3.3 | 75.52 | Yes | 16 |
| 2 | A | 1.09E6 | 3.3 | 66.34 | No | 0 |
| 3 | A | 1E6 | 3.3 | 70.54 | No | 0 |
| 4 | A | 1.71E6 | 3.3 | 73.76 | Yes | 3 |
| 5 | A | 2E6 | 3.3 | 72.1 | No | 0 |
| 1 | B | 3E7 | 5.25 | 75.52 | No | 0 |
| 2 | B | 1E6 | 5.25 | 77.39 | No | 1 |
| 3 | B | 1E6 | 5.25 | 79.38 | No | 2 |
| 4 | B | 0.98E6 | 5.25 | 86.19 | Yes | 2 |

Two device samples (A and B) have been tested at the two specified power supply voltages. The thermal resistors placed around it, heat the device sample. In details, before the activation of the beam the temperature of the DUT die is monitored by a laser thermometer which verifies that the average temperature of the devices is reasonably stable at 75°C than the beam is turned on. As illustrated in Table II, the sample A incurs in a latch-up prior to the completion of the total maximum fluence, besides 16 device behavior anomalies have been detected. These anomalies are correlated to the occurrence of SEUs within the device resources. The progressive current value observed during the run 1A is illustrated in Figure 3, where we represented the average current value absorbed by the DUT for each minute as computed by the monitoring scope. As the reader can notice, the trend of the current is not linear and undergoes to various spurious oscillations; the SEL effect is detected after around sixty minutes from the starting of the run. Once the SEL effect is triggered, the DUT peak of current absorption is of 0.176 A, then subsequently the DUT reduces the current absorption to 0.04 A and remains stable at this value until the power off.

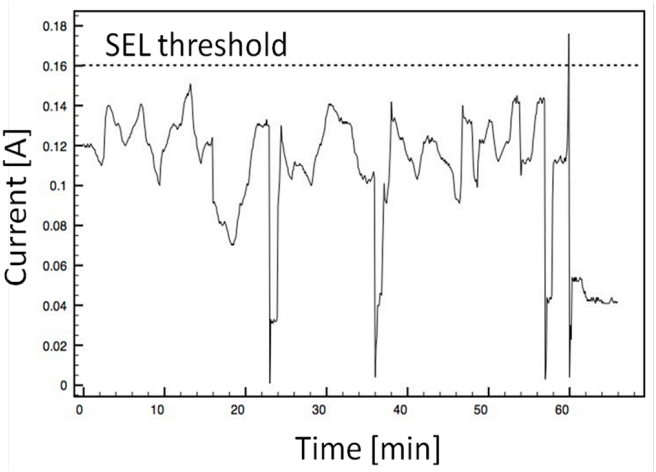


Fig. 3. Current measured during the execution of the run 1A, SEL test at 3.3 V at the LET of 75.52 MeVcm$^2$/mg.

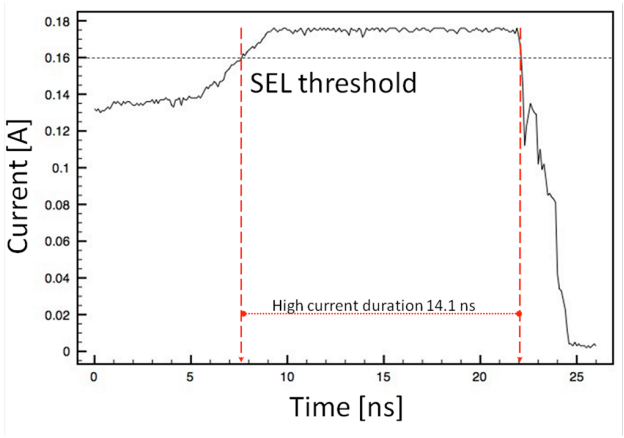


Fig. 4. High current measured before SEL event during the execution of the run 1.

The behavior of the SEL effect has been depicted in Figure 4, where it is possible to notice that the current drastically increase from the nominal value of 0.135 A to the maximum value of 0.176 A. The current remains over the SEL threshold for 14.1 ns, while the duration of maximum current peak is of 12 ns; after the peak, the current rapidly decreases up to 0.01 A, condition in which the device functionalities are interrupted, after the detection of the SEL effect, the DUT has been powered off. The test does not reveal any disruptive latch-up, since none devices has been permanently broken. This condition has been determined since after the device

power-off, the DUT power supply was turned on again and we observed that the device samples are still correctly working.

The observed SEU could be related to two detected anomalies: the original clock output, read from the clock-spy pin of the DUT and illustrated in Figure 5.a, undergoes to the modification of the duty cycle, effect in Figure 5.b, and to the modification of the frequency as illustrated in Figure 5.c. The impact of such effects on the full application is currently under evaluation. We observe 3 effects related to the different working frequency, which events correspond to the low current, point depicted in Figure 3; and 13 effects related to a different duty cycle.

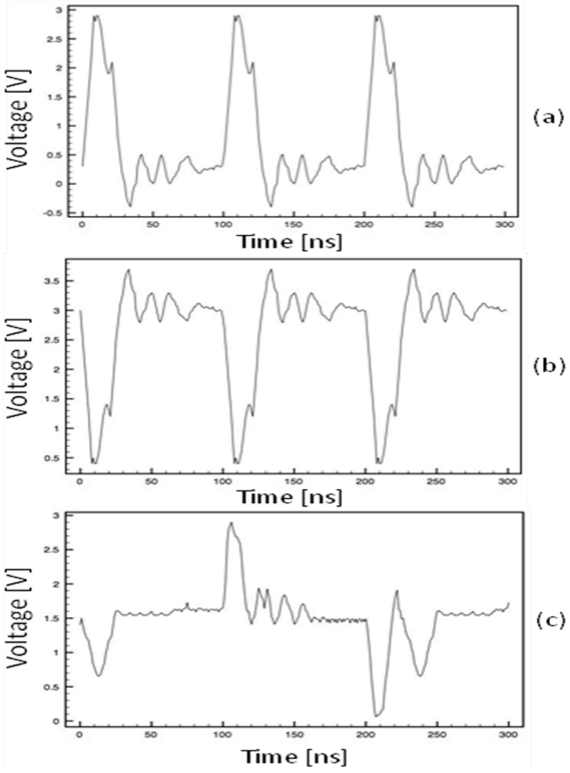


Fig. 5. Diagram of the first DUT anomalous behavior due to SEU effect. The erroneous behavior corresponds to a modification of the original clock output (a) into a waveform with different duty cycle (b) or different working frequency (c).

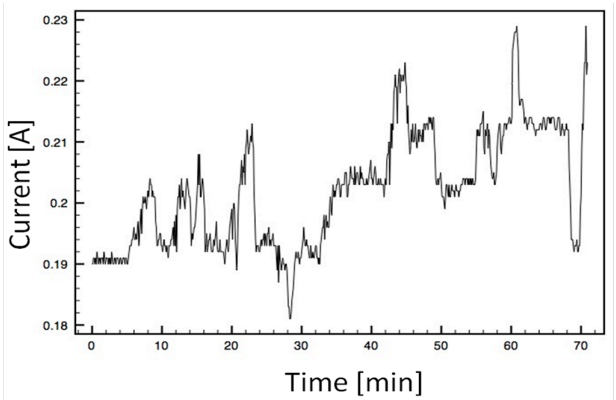


Fig. 6. Current measurement during the execution of the run 1B, SEL test at 5.25 V at the LET of 75.52 MeVcm$^2$/mg.

Vice versa, the progressive current value observed during the run 1B executed at 5.25 V, is illustrated in Figure 6. This run does not trigger any latch-up, besides none SEU has been observed. However, it is possible to observe a progressive current increase due to TID effects on the device.

In order to identify the LET SEL threshold, we performed the other test runs, as illustrated in Table II we found that MG2RT devices have a SEL sensitivity LET threshold of 72.1 MeV·cm$^2$/mg at 3.3 V while an LET threshold of 86.19 MeV·cm$^2$/mg at 5.25 V. The total accumulated dose has been of 38.49 Krad and 40.18 Krad for the device sample A and B respectively.

## VI. CONCLUSIONS AND FUTURE WORKS

In this paper we present a test environment in order to measure the SEL sensitivity of 0.5 MG2RT Atmel radiation hardened technology. The experimental results have been achieved with real radiation test executed at the GANIL (Caen, France) facility. The measurement environment includes suitable monitoring and control platforms able to apply static and dynamic input stimuli to observe the DUT behavior detecting permanent or temporary erroneous functionality. The results we achieved allow to identify the LET threshold that activate the SEL phenomena. SEU effects have been also observed and classified. Currently, according to the whole systems were the DUT will be used, we are evaluating the impact of the SEL and SEU effects on the whole application. As future activity, we plan to perform further analysis able to identify the source of the SEL effects and to evaluate the impact of a dynamic workload applied to the DUT under high temperature and heavy ion irradiations.

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