POLITECNICO DI TORINO

Corso di Dottorato in Ingegneria Elettronica
e delle Comunicazioni

Tesi di Dottorato

Behavioral modeling of nonlinear circuit elements

Application to signal integrity and electromagnetic compatibility

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XIII Ciclo di Dottorato

Summary

Nowadays the availability of computational models of nonlinear dynamic components is becoming a key requirement for the analysis and design of complex systems. The complexity of many components, however, as well as the lack of information on their internal structure often prevent from the development of traditional physical models. This scenario raise the interest for behavioral models, which are models obtained from the observation of the external behavior of components.

In this thesis we focus on the development of behavioral models for the assessment of Signal Integrity (SI) and ElecroMagnetic Compatibility (EMC) effects on fast digital circuits. Such an assessment, that is mainly achieved by simulating the evolution of signals sent on interconnects by digital integrated circuits (ICs), requires efficient and accurate models of IC ports driving and loading the interconnects themselves. The required models must allow the simulation of large realistic problems and must performs at an accuracy level useful to the prediction of sensitive effects, like crosstalk and radiation. Behavioral models meet such requirements and are establishing as the best tools for the description of IC ports.

We analyze possible behavioral modeling methods for IC ports and concentrate on behavioral modeling via black-box identification. It amounts to the selection of a suitable parametric model and to the estimation of its parameters from measured transient responses. The selection of a suitable class of parametric models leads to Radial Basis Function (RBF) representations, that offer many advantages in the modeling of systems with strong nonlinear nature and multiple inputs. We developed a simplified RBF model that can be obtained from measured port voltage and current. The estimation of such model is simple and relies on a robust algorithm.

In order to test the effectiveness of the proposed approach and its feasibility, we apply it to the modeling of several virtual devices and to an actual device of interest. The obtained models perform at a fairly good accuracy and efficiency levels and turn out to be weakly sensitive to driven loads and measurement setup. Besides, since the model structure is selected by the estimation process itself, all the relevant physical effects relating input and output signals (*e.g.,* substrate or packaging effects) are automatically taken into account.

Acknowledgements

Turin, January 2001

I wish to thank my Ph.D. thesis advisor, Prof. F.Canavero for his advises and comments throughout the whole research activity and the preparation of this Thesis. I also wish to thanks Prof. I.Maio for supporting my work with continuos helpful suggestions and fruitful discussions. Their enthusiasm and scientific methodology have been a reference for me and their contributions improve the quality of the results.

A final thought goes to my parents. Thank you for your encouragement and constant support during all my studies. I have learnt from you more than anyone else. To you, I dedicate this thesis.

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Chapter 1

Introduction

Nowadays the availability of computational models of nonlinear dynamic systems is becoming very important. The complexity of actual systems and the lack of detailed physical models require a modeling approach based on the observation of system behavior.

In this scenario, the development of **behavioral models** plays a crucial role. The behavioral modeling of a system means to look for a relation among all the relevant system variables on the basis of the external observation of the system response to suitable stimuli. Application examples can be easily found in almost any areas of interest. The control of industrial plants or complex mechanical systems as well as the prediction of economic phenomena and the numerical simulation of electrical and electronic circuits demand the availability of such models. In fact, these applications require simple but effective models of actual systems, that can be hardly obtained from their detailed physical descriptions, even if they were available. This is maily due to the huge number of variables and unknown nonlinear effects influencing the behavior of actual systems.

Even if the methodology addressed in this Thesis is quite general, we concentrate on the numerical simulation of fast digital circuits for the assessment of Signal Integrity (SI) and ElecroMagnetic Compatibility (EMC).

Such an assessment is of paramount importance in the design of fast circuits. It is devised to predict sensitive effects, like waveform distotsion, crosstalk, overshoots and radiation [6.1]. This prediction is mainly achieved by simulating the evolution of signals sent on interconnects (cable wires, PCB and MCM lands) by digital ICs. The accuracy of SI/EMC simulations

heavily depends on the available models of circuit elements. Whereas the modeling of inteconnects is rather established, the modeling of digital ICs is in the beginning.

Since digital ICs are complex nonlinear dynamic systems, containing a very complex functional part and a high number of pins (several hundreds for modern microprocessors), there is no hope to effectively model both the functional part (the IC internal logic) and the input/output ports. For this reason and for the prediction of waveforms on interconnects, we require effective and accurate models of digital IC ports driving and loading the interconnects themselves. The main objective of this work is to look for effective behavioral methods for such a modeling task. This is due to the lack of detailed physical models of digital IC ports (*e.g.,* SPICE transistor level), mostly classified by IC manufacturers, as well as their complexity.

The structure of this thesis is as follows.

Section 2 deals with the general problem of IC ports behavioral modeling and possible modeling approaches.

Section 3 deals with the approach we mainly discuss in this Thesis: the behavioral modeling via black-box identification. Here we investigate possible methods for the black-box identification of models of nonlinear dynamic circuit elements.

Section 4 discusses the application of the black-box identification approach based on Radial Basis Function (RBF) models to the modeling of digital IC ports. In this Section we address the development of simplified RBF models for the output ports of digital ICs, that can be easily obtained from port measurements.

Finally, **Section 5** and **Section 6** collect the comment on our contributions on this subject and conclusions, respectively.

Chapter 2

IC port modeling

This Section defines the problem of modeling fast digital IC ports and outlines possible modeling approaches. IC ports can be classified into input, output and power supply ports. The modeling of input ports is rather straightforward because their operation is scarcely correlated to the IC internal operation. For this reason they can be assumed as simple dynamic one-ports, that can be easily characterized by the observation of their external behavior only, *i.e.,* from port current and voltage waveforms. Conversely, the modeling of output and power supply ports is not trivial, because their operation is strongly influenced by IC internal signals. As an example, the evolution of output port signals is decided by the load and port characteristics, the latter depending on the internal signals controlling the port logic state.

In order to address the modeling of IC ports, we focus on output ports and discuss their structure through the following example. Figure 2.1 shows the circuit of a typical CMOS output buffer behind an output port (terminal (a) and (b) are the port output pin and the V_{ss} pin, respectively) [6.2]. Output buffers of digital integrated circuits, for any kind of technology/architecture, are composed of cascaded stages with growing driving capabilities. Such circuits provide the interface between the fast low-energy internal parts of ICs and the off-chip interconnects, that require higher energy signals. Output buffers, therefore, must increase the power of transmitted signals limiting as much as possible the added delay and the increase of the rise/fall times.

With reference to the previous example, the structure of a generic output buffer is shown in Fig. 2.2, where v_i denotes the buffer input voltage (*i.e.,* the output of the functional part of the integrated fast digital circuit), v and

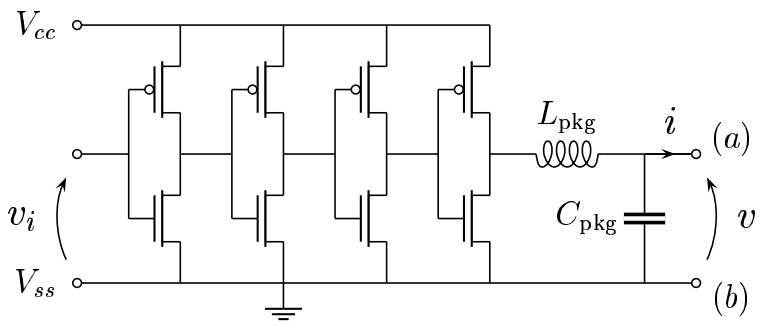

Figure 2.1. 4-stages 1.2 μm CMOS output buffer.

i the buffer voltage and current at the output pin, respectively, v_ℓ the input voltage of the last stage and V_{cc} and V_{ss} the power supplier voltages.

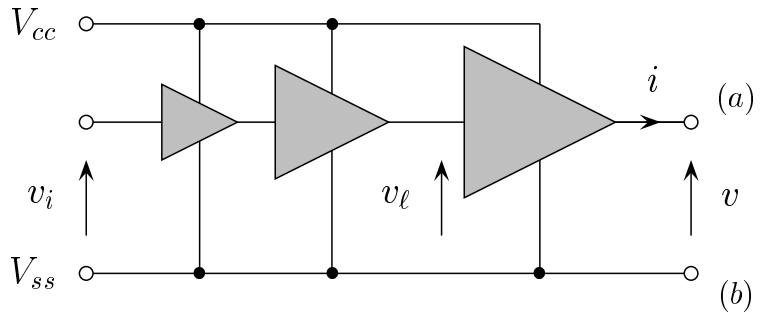

Figure 2.2. Generic multistage output buffer and its relevant electric variables.

The best modeling approach is the development of behavioral models, that are establishing as the most effective description of digital IC ports for SI/EMC simulations. A behavioral model of a device is a set of port characteristic equations (or the equivalent circuit of such equations) obtained from external (possibly virtual) measurements. Behavioral models have the required numerical efficiency and, when properly used, yield responses close to the response of the detailed transistor-level models of the ICs. Behavioral models of IC output ports for SI/EMC simulations must relate the port voltage v and current i, taking into account the port logic state and state transitions.

The most common approach to behavioral modeling is via **simplified**

equivalent circuits. A port model is defined by a suitable equivalent circuit, whose parameters can be estimated from input/output data; the information on the IC technology is used to devise the equivalent circuit, i.e. the model structure. An important example of the equivalent circuit approach to behavioral modeling is the widely adopted Input/output Buffer Information Specification (IBIS). IBIS is a set of rules defining and formatting data, from which IC port models based on simplified equivalent circuits can be developed [6.3, 6.4, 6.5]. IBIS offers high numerical efficiency, large data library and commercial software tools handling models and complex modeling problems. However, the equivalent circuit approach to behavioral modeling has also inherent limitations. Mainly the estimation of model parameters is easy only by virtual measurements, *i.e.,* from transistor-level models of the devices, and the physical effects taken into account by the model are decided a priori, when the equivalent circuit defining the model is selected. As an example, Fig. 2.3 shows the simplified equivalent circuit assumed by IBIS for the output port of a generic digital IC. In this simplified circuit, the electric

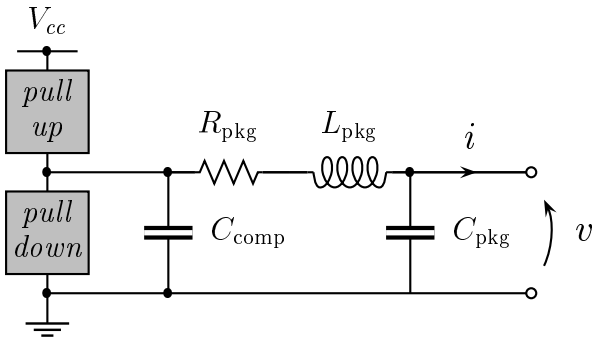

Figure 2.3. IC output port equivalent circuit assumed by IBIS.

equivalent of the package is composed of the $R_{\rm pkg}$, $L_{\rm pkg}$, $C_{\rm pkg}$ elements and the silicon output port capacitance is assumed linear and modeled by $C_{\rm comp}$. Finally, the *pull-up* [*pull-down*] block collects the information on both the static characteristics when the port is driven in LOW [HIGH] output state and the dynamics during state switchings. Data provided by IBIS, in accordance to the assumed equivalent circuit, must be translated into a executable model (IBIS model) in order to be used in circuit simulation environments. In the contributions **IV**, **V**, **VI** we provide guidelines to build models from

IBIS data sets and we propose an effective model based on IBIS Ver. 1.1-2.1 for the output ports of CMOS ICs.

A second possible approach to behavioral modeling, the one we mainly address in this Thesis, is via **Black-Box (BB) identification**. Such an approach amounts to the selection and estimation of a suitable discrete-time nonlinear dynamic parametric model from the waveforms that can be measured at buffer output. Parametric models offer high accuracy and an acceptable numerical efficiency. They are easier to obtained from actual measurements, as they require only the knowledge of transient input and output data. Furthermore, since the model structure is selected by the estimation process itself, parametric models automatically take into account all the physical effects relating input and output data. They would enable any user to easily model sample devices and to simulate critical interconnect structure to assess sensitive SI/EMC effects.

Chapter 3

Behavioral modeling via black-box identification

3.1 Generalities

In this Section we investigate possible methods for the behavioral modeling of nonlinear dynamic circuit elements via black-box identification. This is the novel approach to behavioral modeling we discuss in this Thesis. The aim of this investigation is to provide guidelines for the selection of a suitable black-box identification method to solve the modeling problem of Sec. 1, *i.e.,* the behavioral modeling of digital IC ports from external measurements.

A black-box identification approach amounts to the selection and estimation of a suitable nonlinear dynamic input/output parametric model (*parametric model hereafter*) accurately describing the behavior of a Device Under Modeling (DUM). This is done on the basis of the observation of the DUM responses to suitable stimuli, *i.e.,* from input/output data.

Estimation means to look for the unknown parameters defining the parametric model from the available input/output data (*identification signals*) [6.6], in order to get the best fitting between the model and the DUM responses. Since we are interested in the behavioral modeling, which means modeling from external observations, we could ignore the internal structure of the DUM.

In such a way, our key idea is to investigate the class of parametric models

developed and widely used in the area of automatic controls and system theory to model nonlinear dynamic systems from input/output data. A generic parametric model of such a class is of discrete-time type and is defined by the following general relation

$$\begin{cases} y(k) &= F(\boldsymbol{\Theta},[y(k-1),\ldots,y(k-r),\mathbf{u}^T(k),\ldots,\mathbf{u}^T(k-r)]^T) \\ &= F(\boldsymbol{\Theta};\mathbf{u}) \end{cases} \tag{3.1}$$

where $y(k)$ is the output sequence of the model, $\mathbf{u}$ is the vector of input sequences (each component is the sequence of an input variable), $[y(k-1),\ldots,y(k-r),\mathbf{u}^T(k),\ldots,\mathbf{u}^T(k-r)]^T$ is the vector of regressors, $\boldsymbol{\Theta}$ is the unknown vector of parameters, r is the dynamic order of the system and F is a generic nonlinear scalar function. Parametric models can be used to model the relation between the inputs and one output of most nonlinear dynamic systems with *fading memory* (*e.g.,* see [6.7]).

As an example, if we consider the nonlinear dynamic two-port circuit element shown in Fig. 3.1 and controlled by its port voltages $v_1(k)$ and $v_2(k)$, we could model its output current by setting $y(k) = i_2(k)$ and $\mathbf{u}^T(k) = [v_1(k),v_2(k)]$ into (3.1).

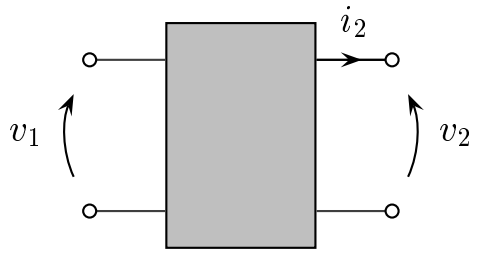

Figure 3.1. Generic two-port circuit element.

In order to build model (3.1), we have to estimate the values of the parameters in $\boldsymbol{\Theta}$ that best relate the available input samples to the output ones. The simplest way to accomplish such a task is to look for $\boldsymbol{\Theta}$ that minimizes the sum of the square of the error between the model and the DUM responses. This means to find

$$\boldsymbol{\Theta} \mid \min\{\frac{1}{n}\sum_{k=1}^{n}[\bar{y}(k)-y(k)]^2\} \tag{3.2}$$

where $\bar{y}(k)$ is the sampled response of the DUM, $y(k)$ is the output sequence of the model and n is the number of available samples.

Section 3.2 deals with the subspace approaches, which are an effective solution for the estimation of MIMO (Multi Inputs Multi Outputs) state-space models. Even if they are for modeling linear systems, here we overview their features and explore possible extensions to the nonlinear case. Sections 3.3 and 3.4 deal with the estimation of NARX (Nonlinear Auto Regression with eXtra input) and RBF parametric models, respectively. NARX models were the first we tried for the modeling problem of Sec. 1, however they showed limitations. In order to overcome such limitations we turned to RBF models. Such models turned out to be quite effective for the problem at hand. We thoroughly discuss them in Sec. 4.

3.2 State-space models

In the last years many contributions on the estimation of time invariant, linear dynamic state-space models have been published, leading to a well established theoretical framework.

Such estimation techniques, usually named *subspace approaches*, are limited to linear models and their extension to the nonlinear case is not trivial. However they can be useful for nonlinear modeling problems, too, when piecewise linear state-space models [6.8] or Wiener/Hammerstein cascade models [6.9] are exploited.

A discrete-time linear state-space model is defined by

$$\begin{cases} \mathbf{z}(k+1) &= \mathbf{A}\mathbf{z}(k) + \mathbf{B}\mathbf{u}(k) \\ y(k) &= \mathbf{C}\mathbf{z}(k) + \mathbf{D}\mathbf{u}(k) \end{cases} \tag{3.3}$$

where $\mathbf{z} \in \Re^r$ is the state vector and matrices $\mathbf{A}$, $\mathbf{B}$, $\mathbf{C}$, $\mathbf{D}$ are the unknowns (parameters) of the model.

A state-space model is the most natural representation of a dynamic system and has been widely used in the area of automatic controls and system theory to model actual systems such as industrial plants or power electric machines.

With the aid of subspace approaches, the estimation of state-space models for circuit elements with multiple inputs is practicable and the numerical

complexity is not critical. The key step of subspace methods to approximate systems with model (3.3) is the estimation of the column space of the extended observability matrix from suitable matrices containing the input/output perturbed data. The estimation is performed by the span of the column or row space of the matrices of input/output data. Then, the model unknowns, *i.e.,* the **A**, **B**, **C**, **D** matrices, are directly obtained from the estimation of the extended observability matrix. Details on the subspace identification theory and techniques can be found in the literature [6.10, 6.11, 6.12, 6.13, 6.14, 6.15].

Some of the features of subspace approaches can be appreciated in the following example. We apply the algorithm of [6.17] to the example circuit shown in Fig. 3.2.

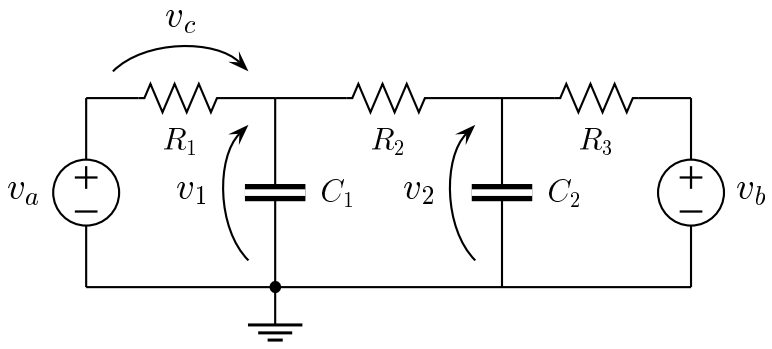

Figure 3.2. Example circuit ($R_{1,2,3} = 200\,k\Omega$; $C_1 = 10\,nF$; $C_2 = 1\,nF$).

The continuos-time state-space equations for such a circuit are

$$\begin{cases} \frac{d}{dt}\mathbf{z}(t) &= \mathbf{A}_c\mathbf{z}(t) + \mathbf{B}_c\mathbf{u}(t) \\ y(t) &= \mathbf{C}_c\mathbf{z}(t) + \mathbf{D}_c\mathbf{u}(t) \end{cases} \tag{3.4}$$

where $\mathbf{u} = [v_a, v_b]^T$, $y = v_c$ and $\mathbf{z} = [v_1, v_2]^T$. With such definitions, the matrices of (3.4) write

$$\mathbf{A}_c = \begin{bmatrix} -1000 & 500 \\ 5000 & -10000 \end{bmatrix} \quad \mathbf{B}_c = \begin{bmatrix} 500 & 0 \\ 0 & 5000 \end{bmatrix} \tag{3.5}$$
$$\mathbf{C}_c = [1 \;\; 0] \qquad \mathbf{D}_c = [-1 \;\; 0]$$

In order to apply subspace methods we need a discrete-time representation like (3.3). This is done by applying standard conversion routines such

as the Matlab function `c2d` [6.16] to (3.4) and (3.5). The key step in this conversion follows. Under the hypotesis that the input vector $\mathbf{u}(t)$ is costant in the time interval $[t = kT,\ t = kT + T]$ (where T is the sampling time), the exact solution of (3.4) is

$$\begin{aligned} \mathbf{z}(kT+T) &= \mathbf{z}(k+1) \\ &= e^{\mathbf{A}_c T}\mathbf{z}(kT) + \{\int_{kT}^{kT+T} e^{\mathbf{A}_c(kT+T-\lambda)}\mathbf{B}_c d\lambda\}\mathbf{u}(kT) \\ &= \mathbf{A}\mathbf{z}(k) + \mathbf{B}\mathbf{u}(k) \\ y(kT) &= y(k) \\ &= \mathbf{C}_c\mathbf{z}(kT) + \mathbf{D}_c\mathbf{u}(kT) \\ &= \mathbf{C}\mathbf{z}(k) + \mathbf{D}\mathbf{u}(k) \end{aligned} \tag{3.6}$$

In such a way, with a sampling time $T = 30\,\mu s$, the discrete-time state-space representation (3.3) for this specific example turns out to be defined by the following $\mathbf{A}$, $\mathbf{B}$, $\mathbf{C}$, $\mathbf{D}$ matrices

$$\mathbf{A} = \begin{bmatrix} 0.97144550 & 0.01276185 \\ 0.12761851 & 0.74173217 \end{bmatrix} \quad \mathbf{B} = \begin{bmatrix} 0.01478238 & 0.00101027 \\ 0.00101027 & 0.12963905 \end{bmatrix}$$
$$\mathbf{C} = \mathbf{C}_c,\ \mathbf{D} = \mathbf{D}_c \tag{3.7}$$

Such state-space equations are then used to compute the example circuit response $y(k)$ (output identification sequence) to suitable input identification sequences $\mathbf{u}(k)$. Input and output identification sequences are processed by the subspace algorithm to estimate the unknown parameters of a state-space model. The algorithm [6.17] is applied to estimate matrices $\mathbf{A}$ and $\mathbf{C}$. This is done on the basis of the output identification sequence obtained by driving the element under modeling with white gaussian inputs $\mathbf{u}(k)$. Then, in order to get the best model, matrices $\mathbf{B}$ and $\mathbf{D}$ are obtained by minimizing the error between the model and the reference responses to a different input identification sequence (*e.g.,* a multilevel waveform). It can be shown that, once $\mathbf{A}$ and $\mathbf{C}$ are estimated, the response of a model defined by (3.3) can be turned into a linear combination of the elements of $\mathbf{B}$ and $\mathbf{D}$. In such a way, $\mathbf{B}$ and $\mathbf{D}$ can be obtained by solving a standard linear least square problem.

We checked the ability of the estimation algorithm to retrieve the parameters of the original system (*i.e.,* matrices (3.7)) when the identification signals are noise free or corrupted with a superimposed gaussian noise (SNR=20 dB).

In the first case (noise free identification), the algorithm exactly estimates the matrices of the original system. In the second case (noisy identification), the estimated model approximates very well the original system, as shown by the validation response of Fig. 3.3.

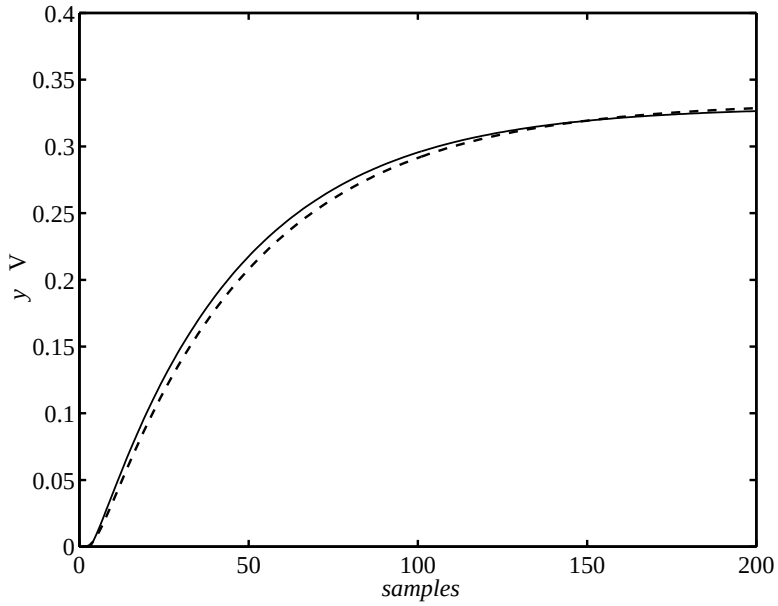

Figure 3.3. Discrete-time response $y(k)$ of the original system and of the estimated model to the input sequence $\mathbf{u}(k) = [0,0]^T$, $k < 0$; $\mathbf{u}(k) = [0,1]^T$, $k > 0$. Dashed line: reference response; solid line: estimated model response.

The accuracy of the obtained model can be also appreciated by comparing the eigenvalues of the estimated matrix $\hat{\mathbf{A}}$ to those of the original matrix A, as shown below.

$$\begin{aligned} \text{eig}(\mathbf{A}) &= \{0.97832914, 0.73484853\} \\ \text{eig}(\hat{\mathbf{A}}) &= \{0.97777425, 0.73098978\} \end{aligned} \tag{3.8}$$

Recently, possible direct extensions of subspace approaches to the nonlinear system identification started to appear but they are limited to bilinear state-space models [6.18, 6.19].

3.3 NARX models

NARX models are parametric models of the form (3.1), where the nonlinear function F is a polynomial function.

As an example, Eq. (3.9) shows a single input ($\mathbf{u} = u$) NARX model with dynamic order $r = 1$ and quadratic nonlinear degree ($q = 2$).

$$y(k) \;=\; a + bu(k) + cy(k-1)u(k-1) + dy^2(k-1) = F(\mathbf{\Theta}; \mathbf{u}) \qquad (3.9)$$

In this example, the vector of parameters $\mathbf{\Theta} = [a,b,c,d]^T$ and the components defining the model structure are $\{u(k),y(k-1)u(k-1),y^2(k-1)\}$.

NARX models have been widely studied in the area of control systems, where suitable estimation algorithms have been developed and successfully applied to moderately nonlinear dynamic systems [6.9]. Also, the direct derivation of NARX models from nonlinear differential models and a discussion of their effectiveness in the modeling of physical systems have been addressed [6.20].

In a practical NARX estimation algorithm (*e.g.,* [6.9]), the components defining the model structure (*e.g.,* $\{u(k),y(k-1)u(k-1),y^2(k-1)\}$ for (3.9)), are selected in the whole space of potential components, obtained by multiplying possible regressors up to the nonlinear degree q. This is done in accordance to the minimization criterion (3.2). Since the number of potential components grows rapidly with the dynamic order r of the model, its nonlinear degree q and the number of possible inputs, the critical point in any NARX estimation algorithm is the selection of the components. Owing to the previous reason, NARX estimation cannot be effectively exploited to model systems with multiple inputs and strong nonlinearities. This means that as the nonlinear degree as well as the number of inputs increase, the estimated NARX model fails to converge to the original system. Finally, once the structure of the model has been selected, the vector of unknown parameters $\mathbf{\Theta}$ can be easily estimated by using standard linear least square methods.

In the contributions **I**, **II**, **III** we try to assess the performances of NARX models and of their estimation in the modeling of highly nonlinear fast dynamic circuit elements such as digital gates. We carry out the study by applying the NARX identification algorithm proposed in [6.21] to a simple

device: the CMOS inverter gate. In spite of the limitations of the NARX estimation algorithm in the modeling dynamical systems with multiple inputs and strong nonlinearities, we obtained simple and accurate NARX models of the CMOS inverter gate. However, this approach can be hardly extended to IC ports. The problem of modeling IC ports has been effectively solved by using RBF models, as described in the following Sections.

3.4 RBF models

RBF parametric models are defined by the following representation

$$\begin{cases} y(k) &= \sum_{j=1}^{p} \theta_j \Phi(|\hat{\mathbf{x}} - \hat{\mathbf{c}}_j|,\beta) \\ \hat{\mathbf{x}}^T &= [y(k-1),\ldots,y(k-r),\mathbf{u}^T(k),\ldots,\mathbf{u}^T(k-r)] \\ \boldsymbol{\Theta}^T &= [\theta_1,\ldots,\hat{\mathbf{c}}_1,\ldots,\beta] \end{cases} \tag{3.10}$$

where the present output of the model $y(k)$ is a linear combination of the p basis functions $\Phi(|\tilde{\mathbf{x}} - \tilde{\mathbf{c}}_j|,\beta)$, Φ is a scalar asymptotically vanishing function generating all the basis functions and $|\cdot|$ denotes the Euclidean norm. Each basis function is defined by its position in the space of regressors (center $\hat{\mathbf{c}}_j$) and a spreading (scale parameter β, common to all Φ's) [6.22]. Possible mother basis function are

$$\Phi(\xi,\beta) = \begin{cases} \exp(-\xi^2/\beta^2) & \text{(Gaussian)} \\ 1/(\xi^2+\beta^2)^{\alpha} & \alpha > 0 \\ (\xi^2+\beta^2)^{\gamma} & 0 < \gamma < 1 \end{cases} \tag{3.11}$$

However, such a choice is not crucial for the performances of RBF models, that critically depends upon the chosen centers $\hat{\mathbf{c}}_j$ [6.23, 6.24]. RBF models can be estimated by very effective algorithms, that work well even for problems with many input variables and strongly nonlinear nature (*e.g.,* [6.24]). This is a consequence of the ability of asymptotically vanishing functions to fit complex surfaces. The previous features overcome the main limitations of NARX models and make RBF models the best candidates to solve the modeling problem at hand.

In the following Section, an effective IC ports modeling approach based on RBFs is proposed. The powerfulness of the proposed approach has tested on several numerical examples and its feasibility demonstrated via an experimental validation.

Chapter 4

RBF models of IC ports

4.1 Introduction

For the modeling problem at hand we could look for a suitable parametric model (3.1) for the output port of the circuit of Fig. 2.2. The convenient variables for such a model would be $y = i$ (output) and $\mathbf{u}^T = [v,v_\ell]$ (inputs). In order to simplify the problem, constant supply voltages are assumed. The generic parametric model for such a port writes

$$\begin{cases} i(k) &= F(\mathbf{\Theta};\mathbf{u}) \\ \mathbf{u}^T &= [v,v_\ell] \end{cases} \tag{4.1}$$

Such a model, however, could not be directly estimated from measured transient waveforms, because neither v_ℓ nor other possible buffer inputs are accessible.

4.2 Derivation of the model

In order to overcome this difficulty, we developed a simplified 2-piece RBF model, that can be estimated just from port voltage v and current i waveforms. As shown below, it stems from the properties of cascaded inverter stages and of RBF models generated by the exponential function

$$\Phi(\xi,\beta) = \exp(-\xi^2/\beta^2) \tag{4.2}$$

With the previous choice, the RBF model (3.10) for the generic output

port of the circuit of Fig. 2.2 writes

$$\begin{cases} i(k) &= \sum_{j=1}^{p} \theta_j \exp(-|\hat{\mathbf{x}} - \hat{\mathbf{c}}_j|^2/\beta^2) \\ \hat{\mathbf{x}}^T &= [i(k-1),\ldots,i(k-r),v(k),\ldots,v(k-r), \\ & \quad v_\ell(k),\ldots,v_\ell(k-r)] \end{cases} \tag{4.3}$$

The $j-th$ exponential term of the above sum can be expanded as shown below

$$\begin{aligned} \exp\left(-|\hat{\mathbf{x}} - \hat{\mathbf{c}}_j|^2/\beta^2\right) &= \exp\left(-[(i(k-1) - \hat{c}_{j1})^2 + \ldots \right. \\ &\quad \left. +(i(k-r) - \hat{c}_{jr})^2 + \ldots]/\beta^2\right) \\ &= \exp(-(i(k-1) - \hat{c}_{j1})^2/\beta^2)\ldots \\ &\quad \exp(-(i(k-r) - \hat{c}_{jr})^2/\beta^2)\ldots \end{aligned} \tag{4.4}$$

Then, by assuming

$$\begin{cases} \hat{\mathbf{x}}^T &= [\bar{\mathbf{x}}^T,\mathbf{x}^T] \\ \hat{\mathbf{c}}_j^T &= [\bar{\mathbf{c}}_j^T,\mathbf{c}_j^T] \\ \bar{\mathbf{x}}(k) &= [i(k-1),\ldots,i(k-r),v(k),v(k-1),\ldots,v(k-r)]^T \\ \mathbf{x}(k) &= [v_\ell(k),\ldots,v_\ell(k-r)]^T \end{cases} \tag{4.5}$$

we can split (4.4) into the product

$$\exp\left(-|\hat{\mathbf{x}} - \hat{\mathbf{c}}_j|^2/\beta^2\right) = \exp(-|\bar{\mathbf{x}} - \bar{\mathbf{c}}_j|^2/\beta^2)\exp(-|\mathbf{x} - \mathbf{c}_j|^2/\beta^2) \tag{4.6}$$

With the above definitions, (4.3) writes

$$i(k) \;= \sum_{j=1}^{p} \theta_j \exp(-|\bar{\mathbf{x}} - \bar{\mathbf{c}}_j|^2/\beta^2)\exp(-|\mathbf{x} - \mathbf{c}_j|^2/\beta^2) \tag{4.7}$$

For typical output buffers, the components of $\{\mathbf{c}_j\}$, *i.e.,* the position of the basis functions in the subspace of regressors generated by v_ℓ, turn out to be clustered around either V_{ss} or V_{cc}. The rationale for such a property is that the typical surface $i = i(\mathbf{x})$ is flat around V_{ss} and V_{cc}, and the centers of the approximating basis functions accumulate in such regions. We verify this property by extensive estimation experiments carried out on virtual devices defined by transistor level models of output buffers.

As an example, we consider a virtual device consisting of a detailed SPICE transistor level model of the last stage of the output buffer circuit of Fig. 2.1 only (See Fig. 4.1). In such a way, the input variable v_ℓ is accessible and the

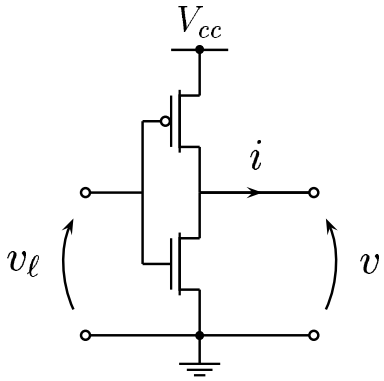

Figure 4.1. Last stage of the example buffer circuit of Fig. 2.1

RBF model (4.3) for such a system can be directly estimated from $i(t)$, $v(t)$, $v_\ell(t)$ waveforms. This is done by using the estimation algorithm [6.24].

Since v and v_ℓ act as inputs and i as output of the RBF model, the identification sequences used by the estimated algorithm are obtained by sampling suitable driving voltage waveforms $v(t)$, $v_\ell(t)$ (input identification signals) applied to the system and the corresponding current waveform response $i(t)$ (output identification signal). In this example, the sampling pitch is $T = 100\,\text{ps}$. The design of such stimuli, however, is a critical point for every nonlinear estimation problem, because only qualitative guidelines are available [6.6]. Typical driving waveforms are multilevel signals spanning the whole range of allowed input values with suitable duration and added noise.

Figures 4.2 and 4.3 show the identification signals devised for the estimation of the RBF model (4.3) for the circuit of Fig. 4.1. With reference to Figure 4.2, the shape of $v_\ell(t)$ is chosen of trapezoidal type. This is due to the fact that, for such a system, *i.e.,* the last stage of a buffer circuit, the trapezoidal waveform is quite close to the input waveform driving the system in an actual operating situation.

The estimated RBF model has a dynamic order $r = 1$ and turns out to be composed of $p = 20$ basis functions. The accuracy of the obtained model is verified by taking into account several validation experiments, in which we test the ability of the model to retrieve the original system behavior.

Figure 4.4 shows the position of the first 10 centers $\{\mathbf{c}_j\}$ of the estimated model and Fig. 4.5 shows the position of all the $p = 20$ centers $\{\mathbf{c}_j\}$. The

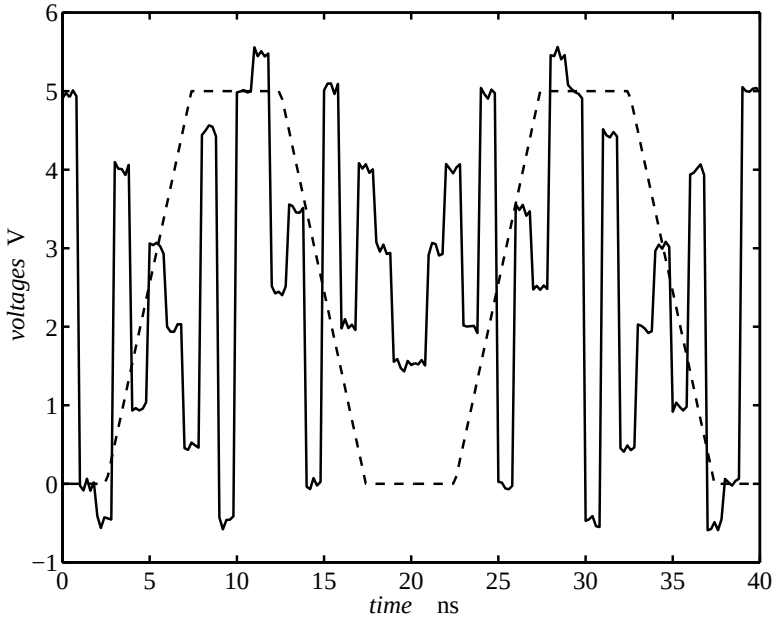

Figure 4.2. Input identification signals $v(t)$ (solid line) and $v_\ell(t)$ (dashed line).

$\{\mathbf{c}_j\}$ clustering around $V_{cc} = 5\,\mathrm{V}$ and $V_{ss} = 0\,\mathrm{V}$ is confirmed.

Now, in order to define the simplified RBF model for the output ports of digital ICs, we assume $\{\mathbf{c}_j\}$, the centers of the basis function in the subspace of $\mathbf{x}$, either exactly at $V_{cc}\mathbf{I}$ or at $V_{ss}\mathbf{I}$, where $\mathbf{I} = [1, \ldots, 1]^T \in \Re^{r+1}$. Also, for a given input waveform $v_\ell(t)$, factors $\exp(|\mathbf{x}-V_{cc}\mathbf{I}|^2/\beta^2)$ and $\exp(|\mathbf{x}-V_{ss}\mathbf{I}|^2/\beta^2)$ are given functions of time. In such a way, the equation defining the simplified 2-piece RBF model writes

$$\boxed{i(k) = w_1(k) f_1(\boldsymbol{\Theta}_1, \bar{\mathbf{x}}) + w_2(k) f_2(\boldsymbol{\Theta}_2, \bar{\mathbf{x}})} \tag{4.8}$$

where f_1 and f_2 are RBF submodels that describe the output port for constant inputs forcing its logic state to the LOW and HIGH values, respectively, (v_ℓ is not an input variable of these submodels), and $w_1(k)$ and $w_2(k)$ are time varying weight coefficients that take into account the evolution of the port logic state and act as switches between submodels f_1 and f_2. Each weight coefficient w_n is formed by concatenating two basic sequences $w_n^u(k)$ and $w_n^d(k)$, that describe the "up" and the "down" transition, respectively. The sequences of the two transitions occur in alternate order and are issued

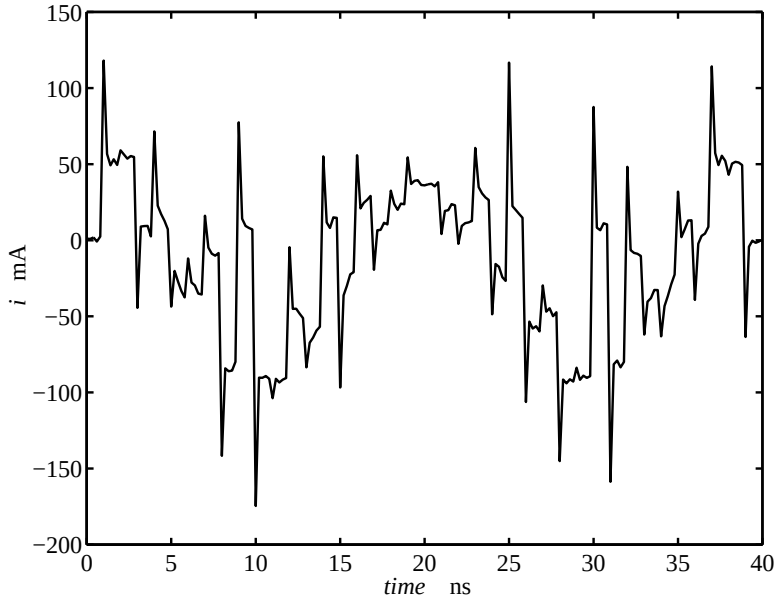

Figure 4.3. Output identification signal $i(t)$.

synchronously with the changes of the input controlling the modeled port. Of course, such a simplified model holds only for logic state transitions spaced enough in time, so that every new transition starts after the previous one has been completed. However, since the above validity condition is satisfied in properly working digital circuits, it does not limit the use of the model in EMC simulation problems.

Besides, since the 2-piece RBF model (4.8) approximates (4.3), it inherits most of the strengths of complete RBF models. Its estimation is easy and, even with a few basis functions (*e.g.,* $p \in [5,20]$), the obtained models track accurately the behavior of most output buffer circuits. Furthermore, since the complete RBF model (4.3) holds for arbitrary loads, the accuracy of the simplified model turns out to be fairly insensitive to the loads it drives.

4.3 Modeling process

The modeling of an IC output port via the proposed approach can be divided into three parts:

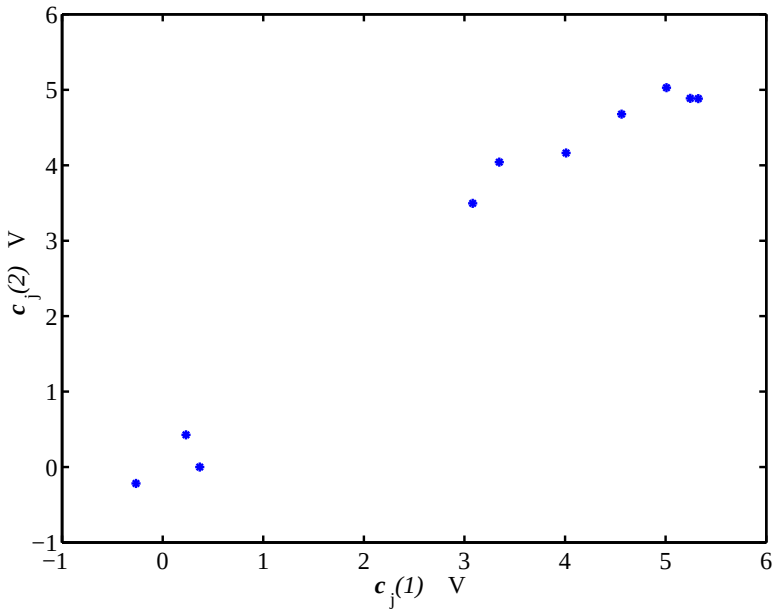

Figure 4.4. Components of the centers $\{\mathbf{c}_j\}$, $j = 1...10$ for the ($r = 1$, $p = 20$) RBF model (4.3) of the circuit of Fig. 4.1.

(1) The excitation and recording of transient responses of the port under modeling;

(2) The estimation of the model parameters $\boldsymbol{\Theta}_n$ and w_n, $n = 1,2$, from the recorded transient responses;

(3) The implementation of the obtained model in a standard circuit simulation environment (*e.g.,* SPICE).

Part (1) amounts to drive the buffer under modeling to obtain transient output signals carrying the information on the buffer behavior. The excitation and response signals involved in this step are the identification signals (see Sec. 3.1). In our problem, we need two sets of identification signals: the **HIGH/LOW state identification signals**, for submodels f_1 and f_2, and the **switching identification signals**, for the weight coefficients w_1 and w_2. Submodels f_1 and f_2 yield the current response $i(t)$ caused by $v(t)$ at fixed logic state. The HIGH/LOW state identification signals, therefore, are composed of a driving voltage waveform applied to the port (submodel input variable) and of its corresponding current response (submodel output

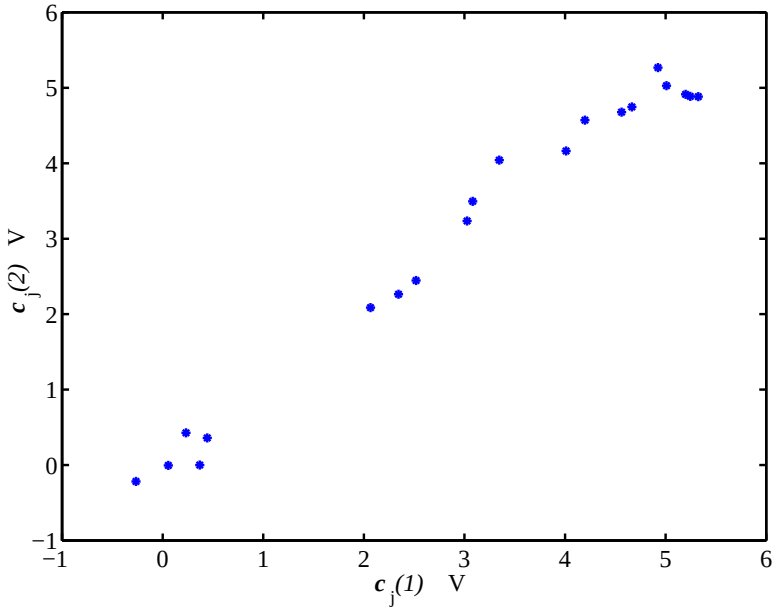

Figure 4.5. Components of the centers $\{\mathbf{c}_j\}$, $j = 1...p$ for the ($r = 1$, $p = 20$) RBF model (4.3) of the circuit of Fig. 4.1.

variable). The driving waveform must be carefully designed, in order to excite every possible dynamic behavior of the system under modeling. As we have already seen in the previous Section, typical driving waveforms are multilevel signals with suitable duration and added noise, spanning the whole range of allowed port voltage values. The selection of the driving waveform is a matter of repeated estimation experiments, where the ability of different identification signals to yield good quality models is verified over a set of sample systems. In order to obtain driving waveform that can be synthesized by standard waveform generators, we look for the simplest driving waveform ensuring successful identification. Our optimum choice is a multilevel voltage waveform, which has flat parts allowing the output port to reach steady state operation and edges with rise/fall times comparable to the switching times of the port. Extensive numerical experiments show that noiseless waveforms of this kind are sufficient for the modeling of typical output buffers. Once f_1 and f_2 are estimated, the weight coefficients w_1 and w_2 are obtained from a

set of switching identification signals by linear inversion of (4.8), *i.e.,*

$$\begin{bmatrix} w_1(k) \\ w_2(k) \end{bmatrix} = \begin{bmatrix} f_1(\boldsymbol{\Theta}_1,\bar{\mathbf{x}}_a) & f_2(\boldsymbol{\Theta}_2,\bar{\mathbf{x}}_a) \\ f_1(\boldsymbol{\Theta}_1,\bar{\mathbf{x}}_b) & f_2(\boldsymbol{\Theta}_2,\bar{\mathbf{x}}_b) \end{bmatrix}^{-1} \begin{bmatrix} i_a(k) \\ i_b(k) \end{bmatrix} \tag{4.9}$$

In the above equation, waveforms $\{i_a,v_a\}$ and $\{i_b,v_b\}$ are the switching identification signals, which are recorded when the output port drives two different loads (load (a) and load (b)) and complete state switchings are caused by variations of the logic inputs. To be more precise, the basic sequences (see Sec. 4.2) w_1^u and w_2^u [w_1^d and w_2^d] are computed from $\{i_a^u,v_a^u\}$ and $\{i_b^u,v_b^u\}$ [$\{i_a^d,v_a^d\}$ and $\{i_b^d,v_b^d\}$] recorded during a LOW to HIGH [HIGH to LOW] transition. There are no restrictions on load (a) and load (b), which can be also real sources stimulating the output port. The best loads would be those allowing $\{i_a,v_a\}$ and $\{i_b,v_b\}$ to explore the widest possible region of the regressor space. We do not yet address the optimization of such loads. Presently we use the same loads recommended by IBIS to characterize port switchings, *i.e.,* load (a) is a resistor and load (b) is a series connection of a resistor and a battery.

In part (2) we compute the model parameters from the identification signal obtained in part (1) of the modeling process. As described above, the evaluation of the weight coefficients $w_n(k)$ is a straightforward operation, that follows the estimation of submodels f_n and is carried out via the closed form equation (4.9). Submodels f_1 and f_2, instead, must be obtained from the HIGH/LOW state identification signals via an actual estimation algorithm. We use the algorithm of [6.24] organized as follows. The HIGH/LOW state identification data define a set of points $\bar{\mathbf{x}}(k)$ in the regressor space. Each of such point is a candidate center for a radial basis function and the scale parameter β is preset to a value ensuring a good overlapping of every possible basis function. Then, for $p = 1,2,3,...$ steps *(i)* and *(ii)* below are repeated

(i) A new model is built by adding a basis function to the $p-1$ model; the center of the function is the point $\bar{\mathbf{x}}(k)$ minimizing the mean square error of the new model.

(ii) The statistical significance of the new model is assessed by suitable indexes.

The selection of the centers is facilitated by the orthogonalization of the time sequences and the process is terminated when the most significant model is reached.

Finally, in part (3) of the modeling process, the obtained input-output discrete-time model is replaced by a continuous-time state-space model, in order to be easily coded as a macromodel of circuit simulators like SPICE. Such a conversion is obtained as described below. In order to simplify the mathematical formulation we assume a dynamical order $r = 1$. Equation (4.8) becomes

$$\begin{array}{rcl} i(k) & = & \sum_{n=1}^{2} w_n(k) f_n(\mathbf{\Theta}_n; [i(k-1), v(k), v(k-1)]^T) \\ & = & F(\mathbf{\Theta}; [i(k-1), v(k), v(k-1)]^T) \end{array} \tag{4.10}$$

Then, by introducing the extra variables $x_1(k) = i(k-1)$ and $x_2(k) = v(k-1)$, Eq. (4.10) writes

$$\left\{ \begin{array}{rcl} x_1(k) & = & i(k-1) = F(\mathbf{\Theta}; [x_1(k-1), v(k-1), x_2(k-1)]^T) \\ x_2(k) & = & v(k-1) \\ i(k) & = & F(\mathbf{\Theta}; [x_1(k), v(k), x_2(k)]^T) \end{array} \right. \tag{4.11}$$

When first order finite differences are introduced, the following discrete-time state space representation arises

$$\left\{ \begin{array}{rcl} \frac{1}{T}[x_1(k) - x_1(k-1)] & = & \frac{1}{T}[F(\mathbf{\Theta}; [x_1(k-1), v(k-1), x_2(k-1)]^T) + \\ & & -x_1(k-1)] \\ \frac{1}{T}[x_2(k) - x_2(k-1)] & = & \frac{1}{T}[v(k-1) - x_2(k-1)] \\ i(k) & = & F(\mathbf{\Theta}; [x_1(k), v(k), x_2(k)]^T) \end{array} \right. \tag{4.12}$$

Finally, by replacing back the time variable and the difference operator with a differential one in (4.12) (*e.g.*, $\frac{d}{dt} z(t) \simeq \frac{1}{T}[z(kT) - z(kT - T)]$, where T is the sampling time used to sample the input and output waveforms), we obtain the following equivalent continuos-time state-space representation

$$\left\{ \begin{array}{l} \frac{d}{dt} \left[\begin{array}{c} x_1(t) \\ x_2(t) \end{array} \right] = \frac{1}{T} \left[\begin{array}{c} F(\mathbf{\Theta}; [x_1(t), v(t), x_2(t)]^T) - x_1(t) \\ v(t) - x_2(t) \end{array} \right] \\ i(t) = F(\mathbf{\Theta}; [x_1(t), v(t), x_2(t)^T]) \end{array} \right. \tag{4.13}$$

The previous state-space equation can be effectively implemented in any circuit simulation environment by its equivalent circuit representation. To

do this, the first two rows of (4.13) can be implemented by simple equivalent circuits with voltage controlled sources and the third by a current controlled source only. As an example, Fig. 4.6 show the circuit synthesis of the second equation of (4.13). The circuit systesis of the first equation is obtained by properly replacing the controlled source.

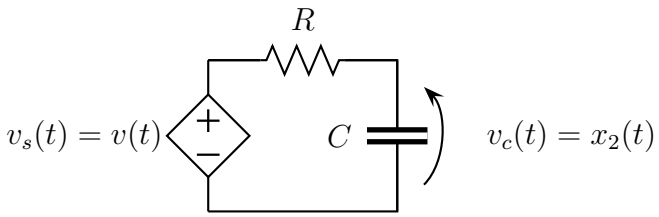

Figure 4.6. RC equivalent circuit for $\frac{d}{dt}x_2(t) = \frac{1}{T}[v(t) - x_2(t)]$, $(T = RC)$.

The complete equivalent circuit of (4.13) can be easily coded as a SPICE subcircuit, as shown in Fig. 4.7.

4.4 Numerical Example

This Section shows the application of the proposed modeling procedure to a virtual device, which is a SPICE transistor-level model of the buffer circuit shown in Fig. 2.1. The parameter values used for this example are those reported at pag. 293 of [6.2], that are representative of output buffers composed of 1.2 μm CMOS inverter stages. The measurement of v and i of such a virtual device (the DUM hereafter) is simulated by driving and loading it with the same circuit that would be used in an actual experiment and by computing the response of the complete circuit in SPICE. The sampled data needed for the estimation are obtained by sampling the computed waveforms with a $T = 100$ ps pitch. This example is one of the many estimation experiment carried out to tune the proposed modeling approach.

The HIGH/LOW state identification signals are obtained by setting v_i either to HIGH or LOW state and by driving the output port as described in Sec. 4.3. Figures 4.8 and 4.9 show the HIGH/LOW state identification signals when the DUM is driven in LOW and HIGH output state, respectively.

```
.subckt RBF2piecemodel w1 w2 v
**************************************************
 + PARAMS:
 * sampling time T=Rx*C (Rx=1, C=T)
 + Rx = 1
 + T = ...
 *
 * dx1/dt={F-x1}/T
   Cx1  x1 0  {T}
   R1   x1 z1 {Rx}
   Ex1  z1 0   value={V(w1)*V(f1)+V(w2)*V(f2)}
 *
 * dx2/dt={v-x2}/T
   Cx2  x2 0  {T}
   R2   x2 z2 {Rx}
   Ex2  z2 0  value={V(v)}
 *
 * output controlled current source
 * i=(w1*f1+w2*f2)
   Gy  0 v    value={V(w1)*V(f1)+V(w2)*V(f2)}
 *
 * RBF Submodel 1:
 * Ef1 = f1(x1,v,x2) = f1(V(x1),V(v),V(x2))
   Ef1 f1 0 value={
   * sum of exponential RBFs
   ...
   +}
 * RBF Submodel 2:
 * Ef1 = f2(x1,v,x2) = f2(V(x1),V(v),V(x2))
   Ef2 f2 0 value={
   * sum of exponential RBFs
   ...
   + }
**************************************************
.ends
```

Figure 4.7. SPICE implementation of the 2-piece RBF model (4.8).

The switching identification data are obtained by applying a pulse v_i waveform containing a LOW to HIGH transition and, after a sufficient time lag, a HIGH to LOW transition, when the DUM drives either a 100 Ω resistor

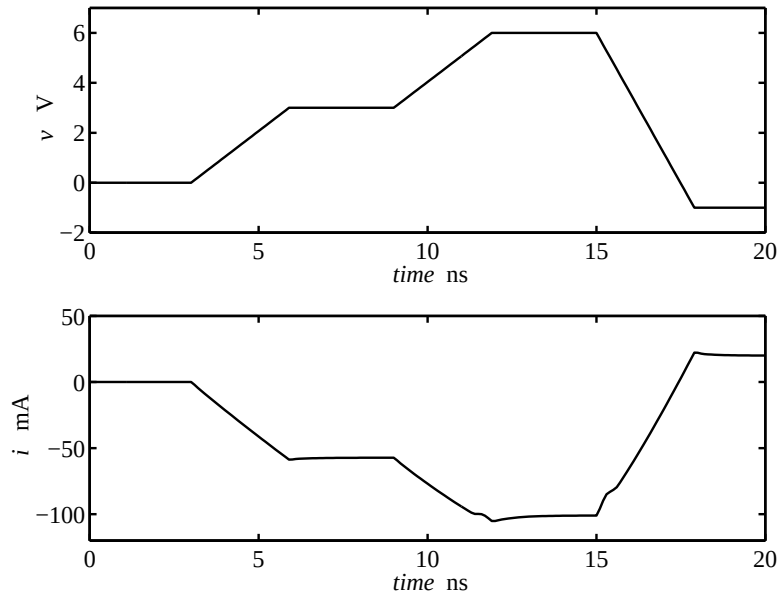

Figure 4.8. HIGH/LOW state identification signals $v(t)$ and $i(t)$ for submodel f_1.

(load (a)) or the series connection of a $100\,\Omega$ resistor and a 5 V battery (load (b)). Figures 4.10 and 4.11 show the switching identification signals $\{i_a,v_a\}$ and $\{v_b,i_b\}$, respectively.

Once the HIGH/LOW state and the switching identification signals are recorded, the 2-piece RBF model is estimated as described in Sec. 4.3. It turns out to be composed of two submodels with dynamic order $r = 1$ and number of basis functions $p = 12$. Figure 4.12 shows the computed weight sequencies $w_1(k)$ and $w_2(k)$.

In order to check the quality of the obtained model, we compare its responses with the responses of the DUM for various test loads, different from those used in the computation of the switching identification signals. Figure 4.13 shows the setup of a first validation test in which the DUM is driven by a HIGH pulse and loaded by the connection of a resistor R and a shunt capacitor C. Figure 4.14 shows the responses of the model and of the DUM for the validation test of Fig.4.13 when some mainly resistive loads and a highly capacitive load are considered. The accuracy of the model and its insensitivity to the driven load can be clearly appreciated.

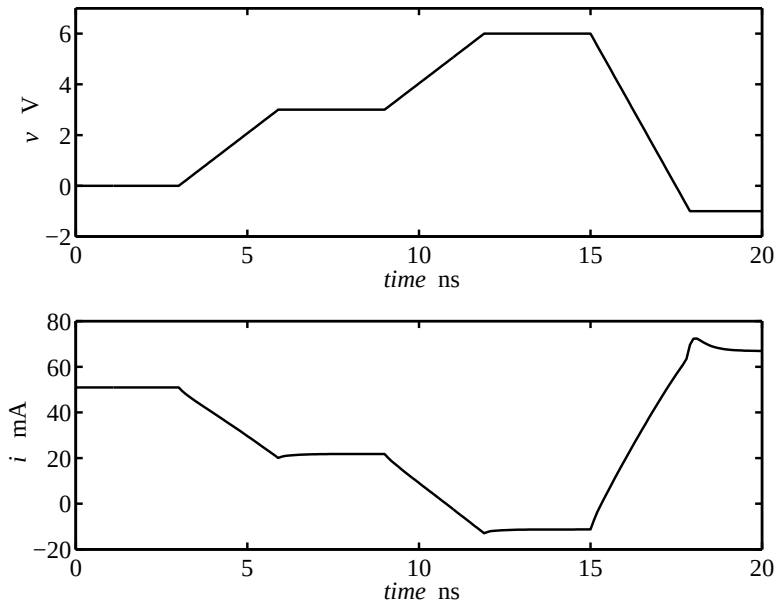

Figure 4.9. HIGH/LOW state identification signals $v(t)$ and $i(t)$ for submodel f_2.

Similarly, Figure 4.15 shows the setup of a second validation test in which the DUM is driven by a HIGH pulse and loaded by a ideal open ended transmission line with $Z_0 = 200\,\Omega$ and $T_d = 2\,\text{ns}$. Fig. 4.16 shows the responses of the model and of the DUM for the validation test of Fig.4.15. Again, the estimated model turns out to be quite accurate.

4.5 Experimental results

In order to demonstrate the feasibility of the proposed approach, *i.e.,* that measurement errors and noise do not prevent its application, we test it on a real device. In this Section, the DUM is a NAND gate of an HC7400 IC, that is connected as an inverter. Such a DUM is both sufficiently simple and representative to be an easy and significant test case.

For a real device, a text fixture suitable to apply and measure signals is needed. The main point is that, in a real setup, ideal voltage sources are not available and, therefore, the identification voltage waveform cannot be directly imposed. The remedy is to stimulate the DUM by a common

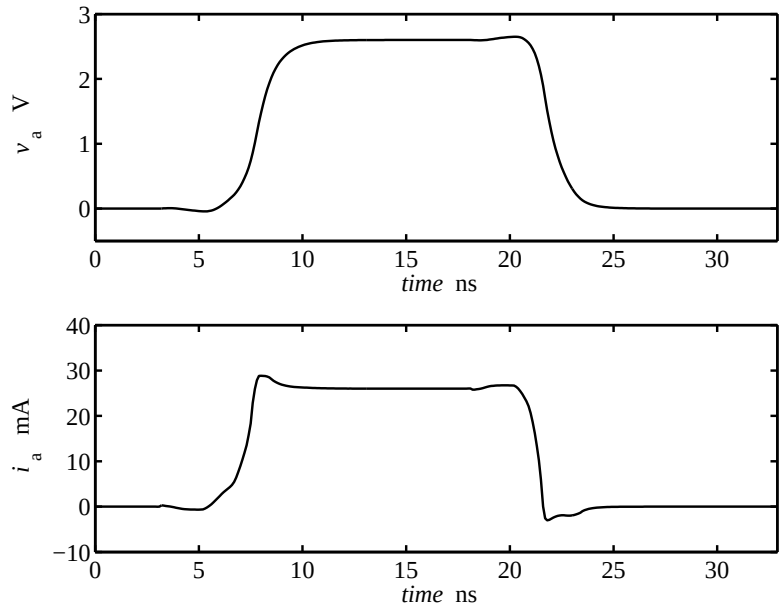

Figure 4.10. Switching identification signals $\{i_a, v_a\}$.

waveform generator and to measure both i and v of the output port. The parameter of the waveform generator are then tuned till the observed voltage waveform has the requested behavior (see Sec. 4.3). The measurement of the output current i can be performed by either a wideband current probe or, indirectly, by a series resistor. We choose the series resistor arrangement and assembled the test fixture shown in Fig. 4.17.

An SMD 100 Ω resistor is series connected to the output pin of one of the four NAND gates of the HC7400, whereas SMA connectors are placed on the back of the board to inject and probe signals. The voltages at the terminals of the series resistor are simultaneously recorded by an oscilloscope Tektronix TDS380 (sampling pitch $T = 200\,\text{ps}$) and passive voltage probes P6114B. The current waveform is extracted from the two recorded voltage waveforms via the equivalent circuit shown in Fig. 4.18 as $i = C_p dv/dt + (v - v')/R_s$. In such a circuit the shunt capacitors at the terminals of the series resistor represent the parasitics of probes.

The HIGH/LOW state identification signals are generated by using a Rhode & Schwarz AFS multifunction waveform synthesizer connected as S_2 while the DUM input is set, via the source S_1, to either the HIGH or the LOW

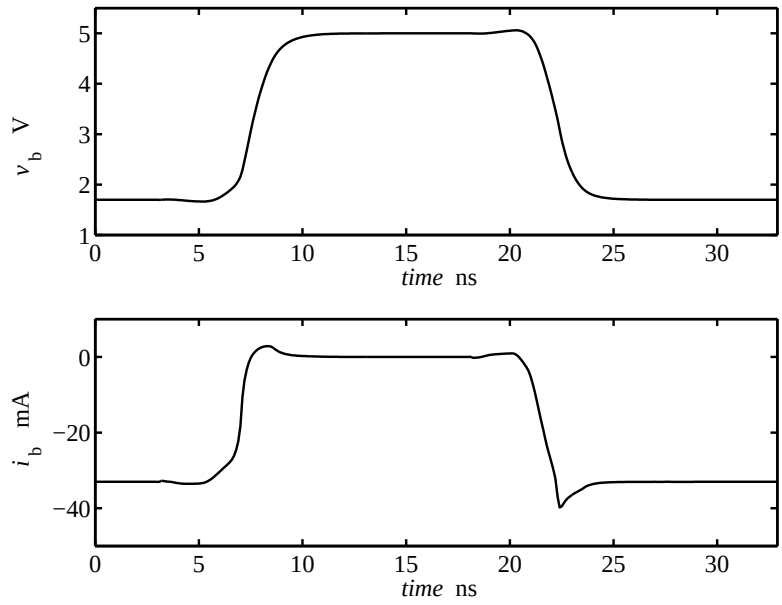

Figure 4.11. Switching identification signals $\{i_b,v_b\}$.

logic output state. The HIGH/LOW state identification signals obtained in this way for submodels f_1 and f_2 are shown in Fig. 4.19 and Fig. 4.20, respectively. The waveform generator to excite such signals is not a critical element. In this setup, the shaping of the identification signal is obtained by a stub element connected between S_2 and the test fixture. In a setup for routine measurements, the waveform generator could be provided by a dedicated circuit composed of discrete logic gates.

The switching identification signal, finally, are obtained by replacing S_2 with a $50\,\Omega$ coax resistor and with a $60\,\Omega$ carbon resistor connected to V_{cc} as load (a) and load (b), respectively, and by driving (via S_1) the DUM to produce a HIGH pulse.

Figures 4.21 and 4.22 show the switching identification signals $\{i_a,v_a\}$ and $\{v_b,i_b\}$, respectively.

The obtained model turns out to be composed of two submodels with dynamic order $r = 1$ and number of basis functions $p = 5$.

Figure 4.23 shows the equivalent circuit of the validation setup devised to test the accuracy of the obtained model. It consists of the DUM driven by a pulse and loaded by a series connection of R_s and an open ended 1.5 m

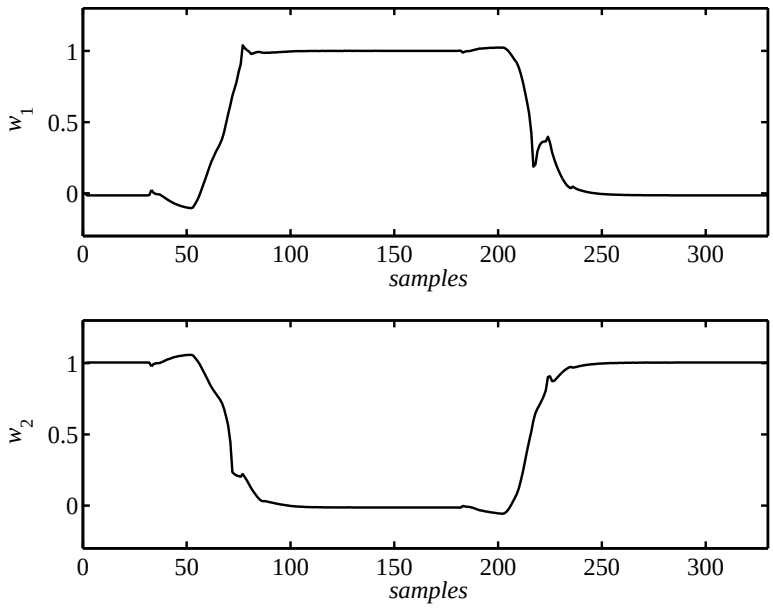

Figure 4.12. Weight sequencies $w_1(k)$ and $w_2(k)$ (sampling time $T_s = 100\,\text{ps}$).

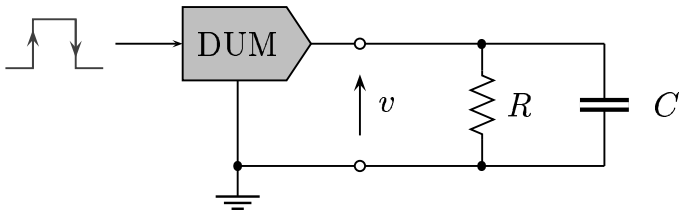

Figure 4.13. Setup for the first validation test.

long RG58 coaxial cable. Figure 4.24 shows the simulation results for the validation test described above. The two curves are the measured response of the DUM (dashed line) and the computed response of the estimated model (solid line). Such a comparison shows that the estimated model performs at a fairly good accuracy level. Besides, it is ought to remark that, in this example, modeling and validation are based on a rather idealized equivalent circuit of the test fixture.

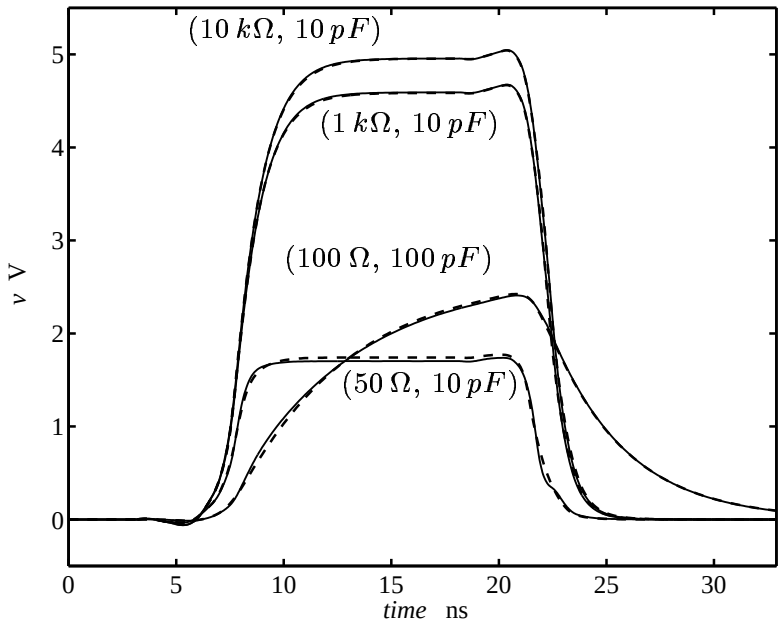

Figure 4.14. Computed output voltage waveforms for the validation test of Fig. 4.13. Dashed line: reference response; solid line: response of the 2-piece RBF model.

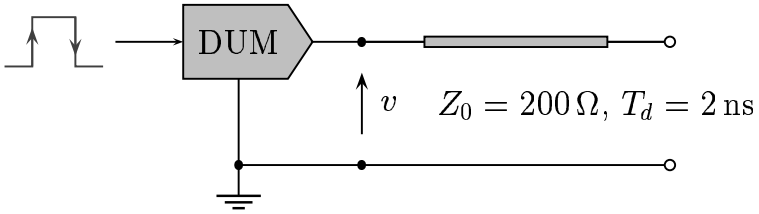

Figure 4.15. Setup for the second validation test.

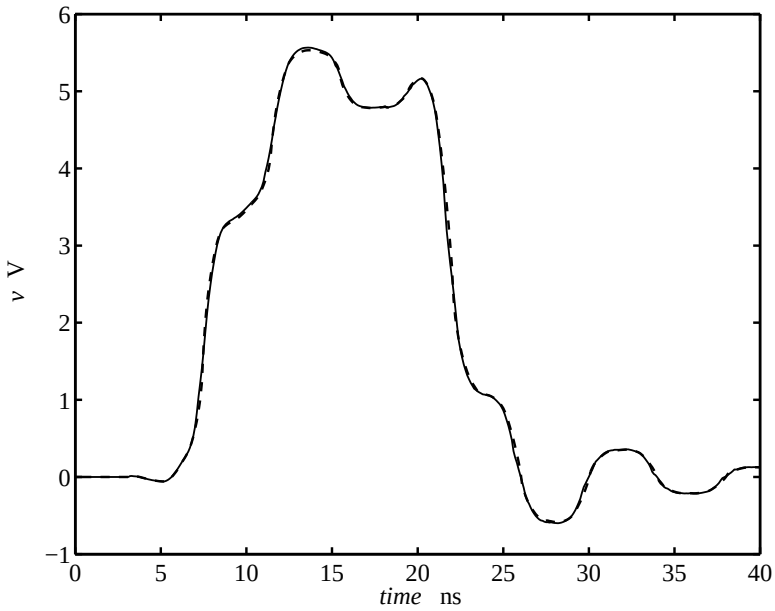

Figure 4.16. Computed output voltage waveforms for the validation test of Fig. 4.15. Dashed lines: reference curves; solid lines: responses of the 2-piece RBF model.

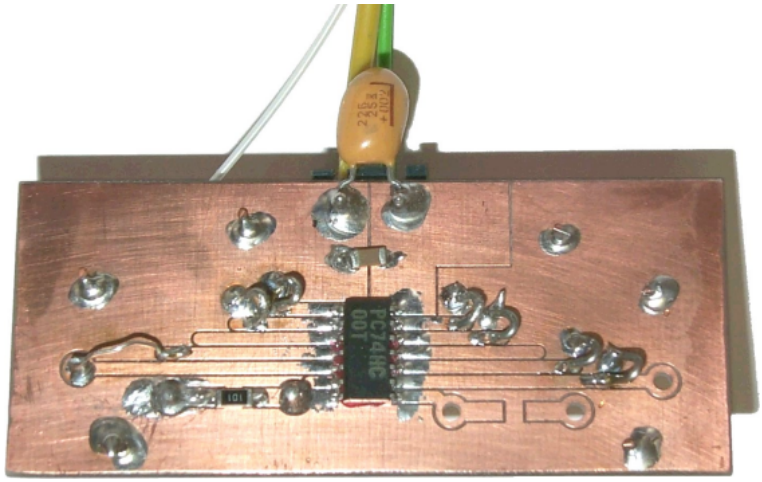

Figure 4.17. Test fixture.

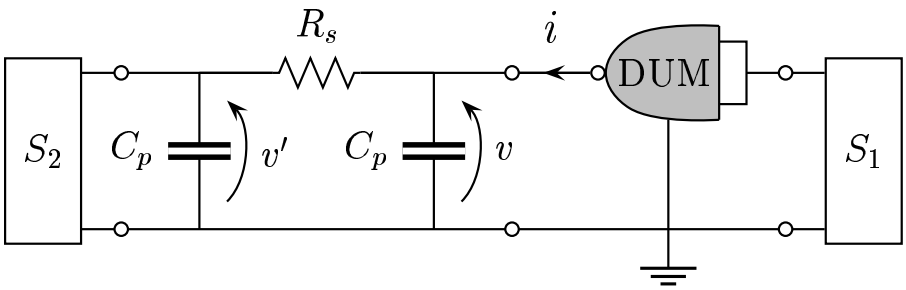

Figure 4.18. Equivalent circuit of the test fixture ($R_s = 100\,\Omega$,$C_p = 14.1\,\mathrm{pF}$). S_1 and S_2 are the sources of the identification signals.

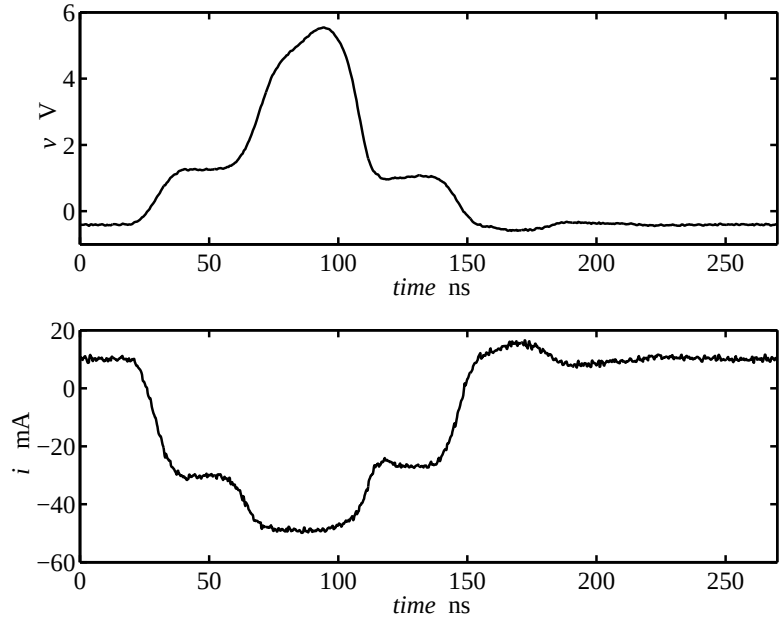

Figure 4.19. Measured HIGH/LOW state identification signals $v(t)$ and $i(t)$ for submodel f_1.

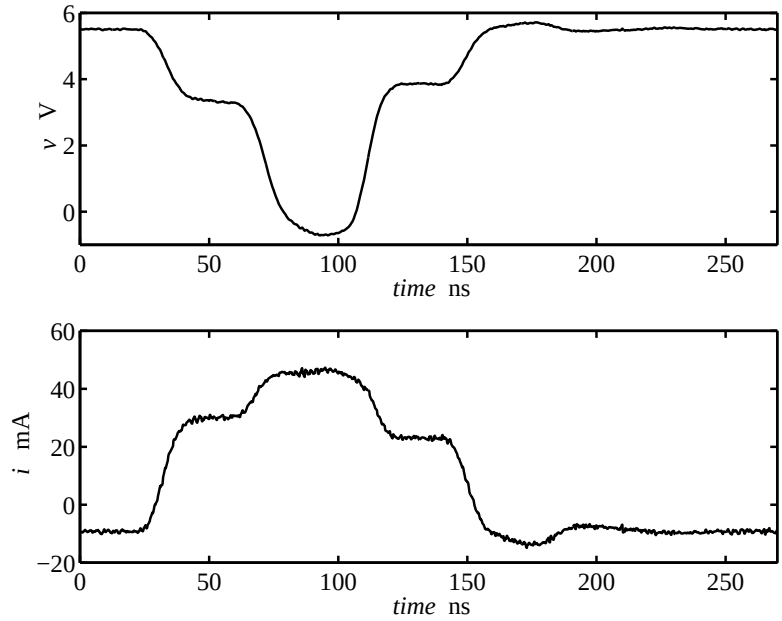

Figure 4.20. Measured HIGH/LOW state identification signals $v(t)$ and $i(t)$ for submodel f_2.

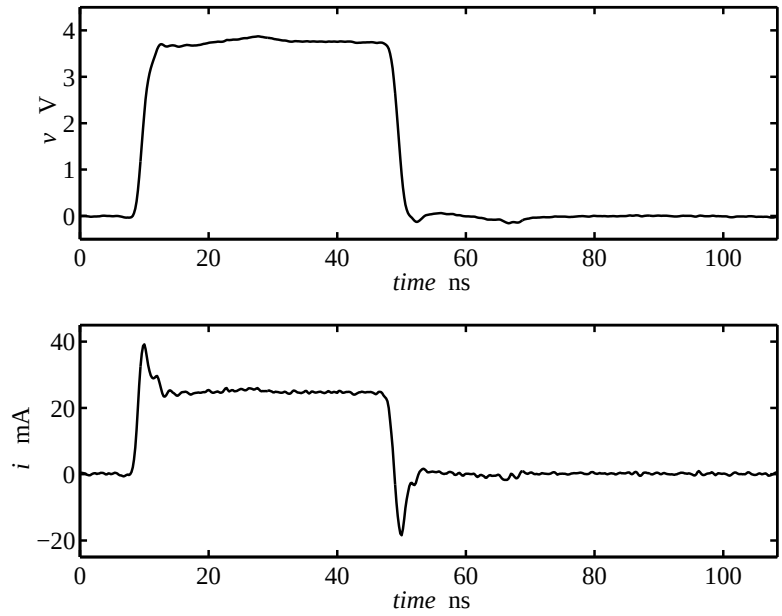

Figure 4.21. Switching identification signals $\{i_a,v_a\}$.

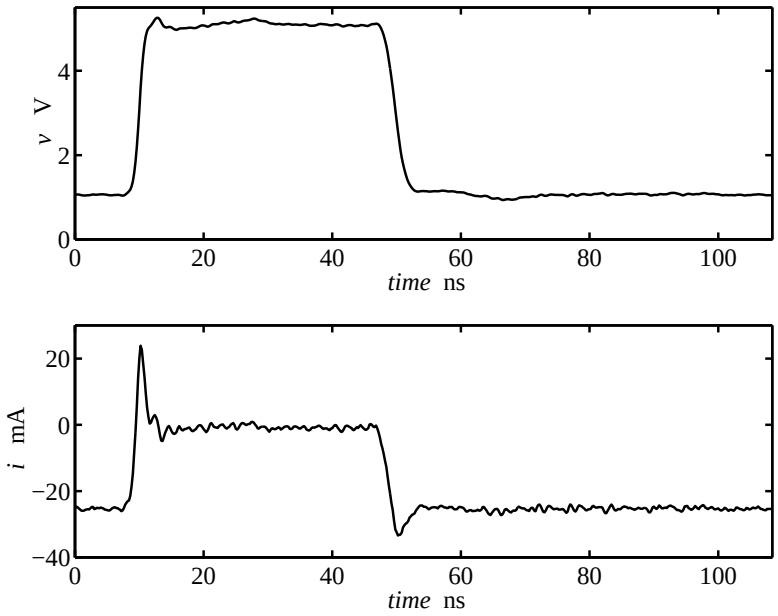

Figure 4.22. Switching identification signals $\{i_b,v_b\}$.

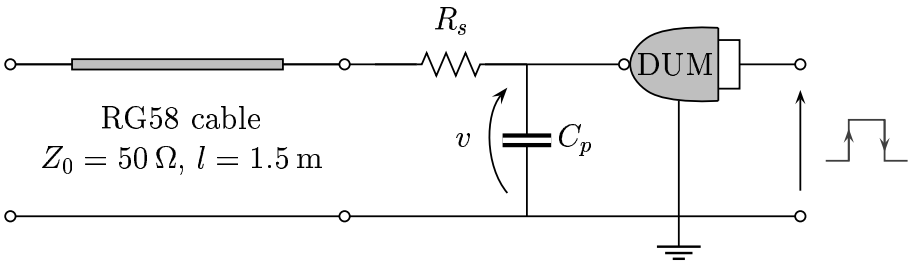

Figure 4.23. Equivalent circuit of the validation setup (see text).

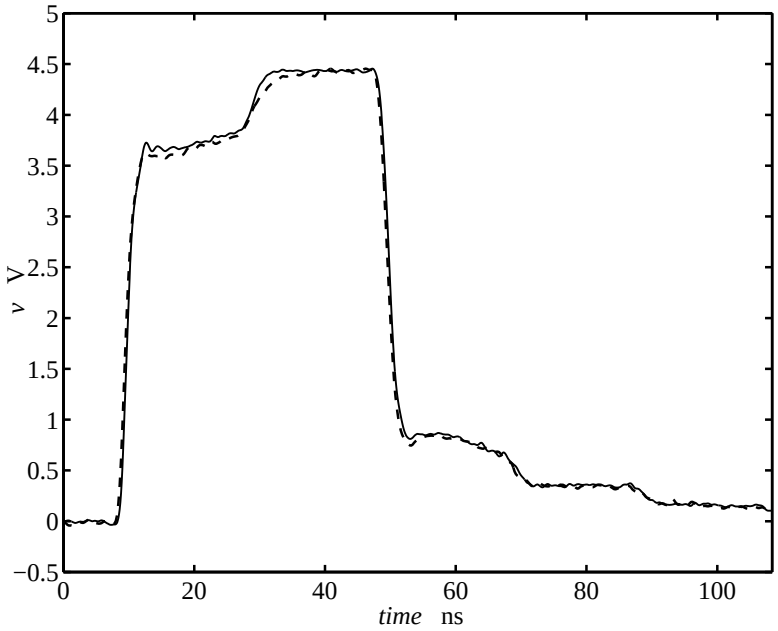

Figure 4.24. Output voltage waveform of the DUM connected as shown in Fig. 4.23. Dashed line: measured reference response; solid line: response of the 2-piece RBF model.

Chapter 5

Discussion of the original research work

In this Section, we shortly comment our contributions to the behavioral modeling of fast digital ICs. For each of the 10 contributions included in the Appendix, we list the original parts within the framework of the previous Sections.

Paper I

I. A.Maio, I. S.Stievano, F. G. Canavero, "NARX Approach to Black-Box Modeling of Circuit Elements," in *ISCAS'98, IEEE International Symposium on Circuits and Systems*, Monterey, CA, May 31 – June 3, 1998.

In this contribution we try to asses the performance of NARX models and of their estimation in the black-box modeling of highly nonlinear dynamic elements (see Sec. 3.3). We apply the proposed approach to a CMOS inverter gate and experiment with the main elements controlling the estimation process.

Paper II

F. G. Canavero, I. S.Stievano, I.A.Maio, "Modeling of Digital Circuits via NARX Identification," in *2^{nd} IEEE Workshop on Signal Propagation on Interconnects*, Travemünde, D, May 1998.

This paper deals with the application of nonlinear system identification methods to digital circuit elements, presenting fast dynamics and

highly nonlinear behaviors. In this contribution, we concentrate on NARX models of CMOS digital gates, as in the previous one, and we investigate the possibilities of nonlinear identification methods for both the black-box modeling and the indirect order-reduction.

Paper III

I. S. Stievano, I. A. Maio, F. G. Canavero, "Black-Box Modeling of Digital Devices," Interconnects in VLSI Design, H. Grabinski (Ed.), Kluwer Academic Publishers, Boston, 2000, ISBN 0-7923-7997-7, 12pp.

This is the last contribution on the NARX modeling approach. We summarize the results obtained for the behavioral modeling of digital ICs for SI/EMC simulations and we provide a SPICE implementation of NARX models. Such an implementation allows us to test the efficiency of NARX models of a CMOS inverter gate, that remains significantly higher than the efficiency of the SPICE reference transistor level model.

Paper IV

I. A. Maio, I. S. Stievano, F. G. Canavero, "Signal Integrity and Behavioral Models of Digital Devices," in *13^{th} International Zurich Symposium on Electromagnetic Compatibility*, Zurich, CH, pp. 149–154, Feb. 13–15, 1999.

In this paper, we address the behavioral modeling of CMOS integrated circuit on the basis of the Input/output Buffer Information Specification (IBIS) Ver. 1.1-2.1 (See Sec. 2). The aim of this work is to provide guidelines to build executable models from IBIS data, which is not provided by the IBIS specification itself. Such an ability is of paramount importance for the validation of IBIS data sets through the comparison of measured transient responses of digital devices and the corresponding responses obtained by IBIS models. Besides discussing basic elements of IBIS models and their critical points, we propose an effective IBIS model, which offers improved accuracy and efficiency, and can be effectively exploited for experimental validations.

Paper V

I. S.Stievano, I.A.Maio, F. G. Canavero, "Behavioral Models of Digital Devices," in *3rd IEEE Workshop on Signal Propagation on Interconnects*, Titisee-Neustadt, D, May 19–21, 1999.

Here we propose an effective IBIS Ver. 1.1-2.1 model of CMOS ICs and we compare its response to the responses of an accurate SPICE transistor level model of such a circuit and of a commercial IBIS model. This study highlight some limitations of IBIS models, yet confirming that a properly designed IBIS models have accuracy and efficiency adequate to SI simulations.

Paper VI

F. G. Canavero, I. A. Maio, I. S. Stievano, "Behavioral Models of Digital Devices and their Impact on Signal Integrity," in *URSI GA99, XXVI General Assemmbly of the International Union of Radio Science*, Toronto, CA, Aug. 13–21, 1999.

In this contribution we summarize the results obtained with the IBIS modeling approach and discuss its inherent limitations. Besides, in order to overcome such limitations, we address the potential of a black-box approach to behavioral modeling. This work drives our interest to the behavioral modeling via black-box identification.

Paper VII

F. G. Canavero, I. A. Maio, I. S. Stievano, "Behavioral Modeling of Digital Devices via Black-Box Identification," in *4th IEEE Workshop on Signal Propagation on Interconnects*, Magdeburg, D, May 17–19, 2000.

In this paper we address the behavioral modeling of digital ICs on the basis of the simplified RBF model introduced in Sec. 4. We perform numerical experiments within the framework of an idealized identification setup and obtain simple models performing at a good accuracy level for remarkably different loads (see Sec. 4.4).

Paper VIII

F. G. Canavero, I. A. Maio, I. S. Stievano, "Modélisation des Circuits Intégrés Digitaux pour la Simulation CEM," in *CEM COMPO 2000: La Compatibilité Electromagnétique des Circuits Intégrés,* Toulouse, F, pp. 67–71, 27–28 juin 2000.

The aim of this work is the characterization of the ports of (poorly documented) digital integrated circuits from standard input/output transient measurements. We follow the same modeling approach discussed in the previous paper. Finally, since the port models must operate effectively in circuit simulation environments, we provide an effective SPICE implementation of the obtained models (see Sec. 4.3).

Paper IX

F. G. Canavero, I. A. Maio, I. S. Stievano, "Black-Box Identification of Digital Devices for Radiation Prediction," in *4th European Symposium on Electromagnetic Compatibility,* Brugge, B, Sep. 11–15, 2000.

In this paper we summarize the results obtained in the behavioral modeling of digital IC ports for the assessment of SI/EMC effects in fast digital circuits. In order to demonstrate the feasibility of the proposed approach, we apply it to the modeling of an actual device: a HC7400 IC, and we verify that measurement errors and noise do not prevent the application of the approach (see Sec. 4.5).

Paper X

I. S. Stievano, I. A. Maio, "Behavioral models of digital IC ports from measured transient waveforms," in *9th IEEE Topical Meeting on Electrical Performance of Electronic Packaging (EPEP2000),* Scottsdale, AZ, pp. 211–214, Oct. 23–25, 2000.

This paper is a short presentation of results contained in **IX**. It aims to provide final users with the key elements of the proposed modeling approach.

Chapter 6

Conclusions

In this Thesis we propose a systematic analysis of possible approaches to the behavioral modeling of digital IC ports for the assessment of SI/EMC effects on fast digital circuits.

We concentrate on the new behavioral modeling via black-box identification, that amounts to the selection and estimation of a suitable parametric model from measured external signals. The selection of a suitable class of parametric models leads to RBF representations, that offer many advantages in the modeling of systems with strong nonlinear nature and multiple inputs. Furthermore, since the model structure is selected by the estimation process itself, all the physical effects relating input and output signals are automatically taken into account. We propose a simplified RBF model that can be obtained from measured port voltage and current. The estimation of such model is simple and relies on a robust algorithm.

In order to test the effectiveness of the proposed approach and its feasibility, we apply it to the modeling of several virtual devices and an actual device of interest. The obtained models perform at a fairly good accuracy and efficiency levels and turn out to be weakly sensitive to driven loads and measurement setup.

We are currently working to extend the approach to the modeling of power supply ports and to include other effects such as the simultaneous switching noise. This would provide a complete tool for the modeling of poorly documented digital ICs for SI/EMC simulations.

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Appendix A

Enclosed papers

Paper I

NARX APPROACH TO BLACK-BOX MODELING OF CIRCUIT ELEMENTS

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ABSTRACT

This paper deals with the identification of NARX (Nonlinear AutoRegression with eXtra input) models for the numerical simulation of circuit containing nonlinear dynamic elements. NARX identification, based on a sequence of input/output samples, is useful for black-box modeling and for the refinement of models of nonlinear circuit elements. In order to assess the suitability of such an approach, we apply it to a CMOS inverter gate and experiment with the main elements controlling the identification process. We obtain accurate models with relatively simple structure and observe reliable operation of the identification process, as well as a good insensitivity to the noise content of the output samples. Such results confirm that NARX identification could be a useful tool for circuit simulations.

1. INTRODUCTION

The development of efficient and accurate numerical models to describe the behavior of circuit elements is of paramount importance in the area of circuit simulation. In particular, the availability of techniques for the black-box modeling of nonlinear dynamic circuit elements and for the simplification (*i.e.*, order reduction) of existing models would be very useful. Black-box modeling is the most general approach to the description of poorly known devices, whereas model simplification allows the balancing of model accuracy and efficiency.

The latter point is going to be a dominant issue of future simulation problems. In fact, as circuit applications become more complex and their operation more critical, conventional circuit simulation and functional simulation become ineffective, since they are, respectively, too expensive and/or too idealized. Fast digital circuits are important examples of this evolution. Their short switching times activate many parasitic effects and require the use of non ideal models, whereas their size limits the complexity of models that can be used. However, for logic gates, the trade-off between model accuracy and complexity is not trivial. The transistor level description of gates leads to complex models, not affordable in the simulation of realistic problems, whereas simpler nonideal models are hardly devised.

In this scenario, the NARX models could provide a useful modeling approach. Such models are the extension of the widely used ARX models to nonlinear systems and are general enough to describe a wide class of them (*e.g.*, see [1]), possibly including many nonlinear electric and electronic components. The identification of NARX models from input/output signals could be exploited for both the black-box modeling and the refinement of models of nonlinear circuit elements. Besides, NARX identification could be applied to the input/output signals of existing accurate models as a method for their simplification. Although such a method has a brute-force nature, its use is justified by lack of systematic methods for the direct simplification of nonlinear models [2].

NARX models have been widely studied in the area of *control systems*, where suitable identification algorithms have been developed and successfully applied to moderately nonlinear dynamic systems [3]. Also, the direct derivation of NARX models from nonlinear differential models and a discussion of their effectiveness in the modeling of physical systems have been carried out [4].

In this paper, we try to assess the performances of NARX models and of their identification in the modeling of highly nonlinear fast dynamic circuit elements. We carry out the study by applying the NARX identification algorithm proposed in [5] to a CMOS inverter and by experimenting with the relevant identification parameters. Since the inverter is the basic element of logic gates, the results obtained in this study should give a first indication of the possibilities of the considered approach in the modeling of digital devices.

2. IDENTIFICATION ALGORITHM

NARX models are discrete-time linear-in-parameter models defined by Kolmogorov-Gabor polynomials [5]

$$y(k) = \bar{y} + \sum_{i=1}^{\gamma} a_i x_i + \sum_{i=1}^{\gamma}\sum_{j=1}^{\gamma} a_{ij} x_i x_j + \ldots + \underbrace{\sum_{i=1}^{\gamma}\sum_{j=1}^{\gamma}\cdots\sum_{p=1}^{\gamma} a_{ij\ldots p} x_i x_j \ldots x_p}_{q \text{ terms}} + e(k) \quad (1)$$

$$X = \{u(k), u(k-1), \ldots, u(k-r), y(k-1), \ldots, y(k-r)\} \quad (2)$$

where $u(k)$, $e(k)$ and $y(k)$ are the samples at the k-th time point of the input, disturbance and output signals, respectively, x_p is the generic element of X, *i.e.*, the present sample of u or the past samples of u and y up to the time $k-r$, and $\gamma = 2r+1$. The integer variables r and q are the *dynamic order* and the *nonlinear degree* of the model, respectively. Every possible product of up to q elements of X is a *potential component* of the model and appears in (1). The potential components with nonzero coefficients are the model *actual components* (or *components* in short) and their coefficients are the *model parameters*.

In order to identify a NARX model from a sequence of input/output samples (*i.e.*, to select the components of the model and compute their parameters), we implement and use the algorithm of Pottman et Al. [5]. Since the number of potential components that can compose a NARX model grows rapidly with r and q, making the identification computationally expensive, we base our implementation on a step forward approach. In such an approach, the model is built by starting from a minimal *guess model* (possibly with no components) and by adding at each step the potential component that mostly reduces the model mean-square error.

In detail, the implemented identification algorithm is organized as follows. A model dynamic order r and a nonlinear degree q are chosen. The model dynamic order is estimated a priori from the input/output sequence by the algorithm of [6], whereas the nonlinear degree is estimated empirically. Such a choice defines the set of potential components. Then a guess model is decided and the following three steps are repeated.

1. The reduction of the model mean-square error produced by each potential component not in the *current model* is estimated off-line by orthogonalization of the time sequences [5]. A *new model* is generated by adding to the current one the potential component that minimizes the mean-square error.
2. The stability of the new model is verified and, if necessary, the added component is discarded.
3. For the new model, the values of suitable statistical indexes are computed [5].

Each execution of the above steps generates a new model, whose statistical significance is assessed by the index values computed in step (3). When a new model has values of the statistical indexes not better than the previous one, the process is terminated and the model with the best values of the statistical indexes is retained as the final one. Eventually, the final model is validated by checking its ability to reproduce the system output for input signals different from those used in the identification process.

As an example, we apply the above procedure to the input/-output sequences of a NARX test system and verify its ability to correctly retrieve such system. The test system is defined by the following particular Kolmogorov-Gabor polynomial with $r = 1$ and $q = 4$

$$\begin{aligned} y(k) &= 0.2025 + 0.405y(k-1) + 0.09u(k-1) \\ &+ 0.0008y^4(k-1) - 0.0056u(k-1)y^2(k-1) \\ &+ 0.177y^2(k-1) + 0.09u(k-1)y(k-1) \\ &- 0.0253y^3(k-1) + 0.01u^2(k-1) \end{aligned} \tag{3}$$

The input *identification sequence* used is obtained by sampling a random multilevel signal with a small white noise superimposed. The identification sequence has 3600 samples, and its level variations are wide enough to highlight the nonlinear nature of (3). Table 1 shows the main figures of some of the models generated by the identification procedure for this example. Each row of such a Table describes a different model and lists, from left to right, the number of components of the model (n), the maximum value ($e_{\max}$) and the variance (σ_e^2) of the error between the model and the reference outputs, and the value of the OVF index [5]. The OVF index is a decreasing function of σ_e^2 and of n, so that its maximum should indicate the most significant model of the sequence. For this example, the OVF index is maximum for the model with $n = 9$ (see the bold row of Tab. 1), which indeed coincides with the original system. The detailed structure of models with $n = 8, 9, 10$ is reported in Tab. 2. Models with $n < 9$ are composed of a subset of the component of the original system and their parameters approximate the corresponding parameters of the original system. On the other hand, models with $n > 9$ have the same components and parameters of the original systems plus spurious components with negligibly small coefficients.

n	e_{max}	σ_e^2	OVF
6	0.2386	2.014×10^{-3}	7.477×10^{5}
7	0.1703	2.014×10^{-3}	8.916×10^{5}
8	0.0712	1.312×10^{-13}	1.381×10^{7}
9	$\mathbf{1.249\times10^{-6}}$	$\mathbf{1.314\times10^{-13}}$	$\mathbf{7.249\times10^{15}}$
10	1.229×10^{-6}	1.306×10^{-13}	6.43×10^{15}
11	1.256×10^{-6}	1.3×10^{-13}	5.8×10^{15}

Table 1: *Main figures for models of the example of Sec. 2 .*

n	8	9	10
$\bar{y}$	0.1809	0.2025	0.2025
$y(k-1)$	0.3938	0.405	0.405
$u(k-1)$	0.1245	0.09	0.09
$y^4(k-1)$	0.0009	0.0008	0.0008
$u(k-1)y^2(k-1)$	-0.0052	-0.0056	-0.0056
$y^2(k-1)$	0.1824	0.177	0.177
$u(k-1)y(k-1)$	0.0901	0.09	0.09
$y^3(k-1)$	-0.0267	-0.0253	-0.0253
$u^2(k-1)$	—	0.01	0.01
$u^2(k)y^2(k-1)$	—	—	0.0

Table 2: *Structure of models of the example of Sec. 2 .*

3. NARX INVERTER MODELS

In this Section, we address the NARX modeling of logic gates by applying the identification algorithm of Sec. 2 to an inverter gate of CMOS technology. We generate the output sequences for the identification process via Spice simulations based on the CMOS *level 2 model*, which is a detailed transistor model including several parasitics. The simulated output sequences are used either directly, to identify NARX models as simple as possible (model simplification), or corrupted by noise, to reproduce identification from measured data (black-box modeling).

We start by considering a Single Input Single Output (SISO) configuration of the inverter system, obtained by loading the inverter with an identical one and by using the voltages at its input and output ports as the input ($u(t)$) and the output ($y(t)$) signals, respectively. For this system, the estimated order is $r = 1$ and we start with $q = 3$ and a guess model with no components. The identification process yields the sequence of models described in Tab. 3. Since the modeled system is not of NARX type, the figures of Tab. 3 do not show the net threshold phenomenon shown in Tab. 1. However, among the identified models, the one with the maximum value of the OVF index ($n = 8$) still reveals the most faithful static and dynamic behavior and can be considered the final model. Furthermore, as in the example of Sec. 2, the parameters of the models with $n = 6$ and 7 still approximate the corresponding parameters of the model with $n = 8$. The accuracy of the model with $n = 8$ is good and can be appreciated in Fig. 1, where its response to a *validation input* (*i.e.*, a signal different from the identification input) and the reference response of the original system are compared. Finally, the complete identification process

n	e_{max}	σ_e^2	OVF
4	2.427	0.7444	1223
5	2.902	0.8784	916.6
6	1.572	0.1919	2969
7	0.7939	0.01882	27230
8	**0.3862**	**0.01266**	**34640**
9	0.3506	0.01253	30420
10	0.3346	0.01048	32140
11	0.3574	0.0108	28000
12	0.3651	0.01122	24450
13	0.3497	0.01139	22190

Table 3: *Main figures of NARX models obtained for a CMOS inverter in SISO configuration by using $r = 1$, $q = 3$ and a guess model with no components*

to obtain this model requires about 20 s on a 60 MHz Pentium PC.

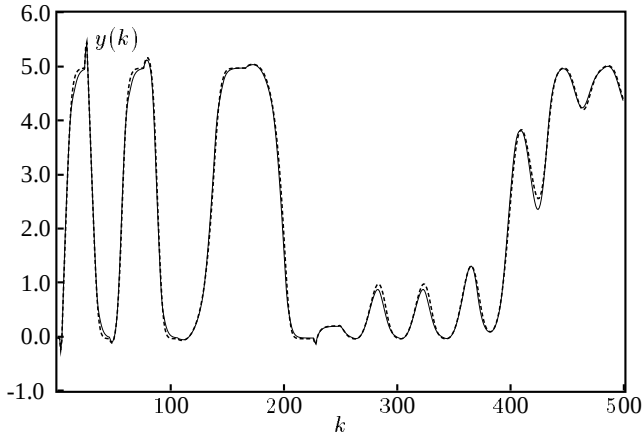

Figure 1: *Reference response to a validation signal (solid line) compared with the response of the $n = 8$ model of Tab. 3 (dashed line)*

In order to further assess the performance of NARX identification on the inverter device, we carry out a complete set of identification experiments for the simple SISO configuration.

The first point considered in such experiments is the influence of the guess model. In fact, the sensitivity of the NARX identification to the order in which the model components are selected is a known weakness [4], and the guess model affects such order. We verify that guess models defined by a subset of the components of the $n = 8$ model of Tab. 3 lead to the same final model. In contrast, guess models with components not in the $n = 8$ model may lead to different final models and show that the pure forward approach does not ensure the neutralization of inappropriate components.

The next element considered is the identification signal. The selection of suitable identification signals is a critical point in the identification of nonlinear system, because of the lack of theoretical guidelines. We try different types of identification signals and different lengths of the identification sequences. The best results are obtained with the random multilevel signals defined in Sec. 2 when the constant levels last enough in comparison with the system "local time constants". In this case we observe good identification properties and a weak sensitivity of the variance error to the length of the identification sequence.

Then we consider the ability of the identification process to obtain models from corrupted output sequences, which is the key property required to use NARX identification for black-box modeling. To check such an ability, we add white noise signals of different variance to the simulated output signal and use the resulting signal for the identification. In this way, we observe remarkably good insensitivity to the added noise. In fact, the identification process works also for the noisy output sequences and the final model is hardly affected (*i.e.,* has the same components and parameter values) for SNR values as low as 25 dB. Moreover, though lower values of the SNR of the output sequence lead to different final models, such models remain able to reproduce the qualitative behavior of the original system. As an example, Fig. 2 and Fig. 3 show, respectively, a part of a noisy output identification sequence and a response of the model identified from such a noisy sequence. In this example, the output identification sequence has SNR$= 20$ dB, and the response of the identified model to a validation signal, shown in Fig. 3, still tracks the reference output.

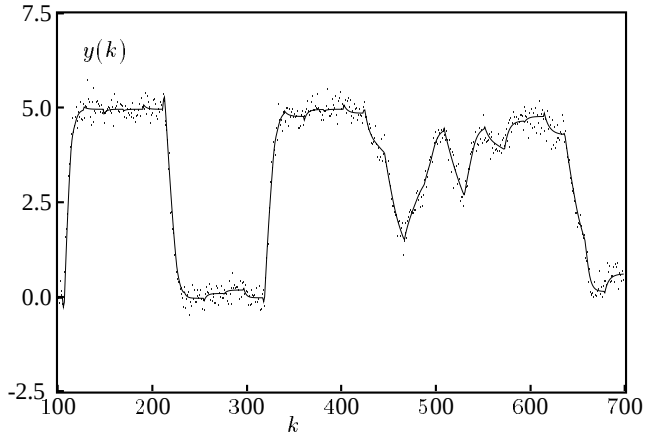

Figure 2: *Samples of an output identification sequence. Solid line: exact values; dots: values after the addition of a noise signal with SNR$= 20$ dB*

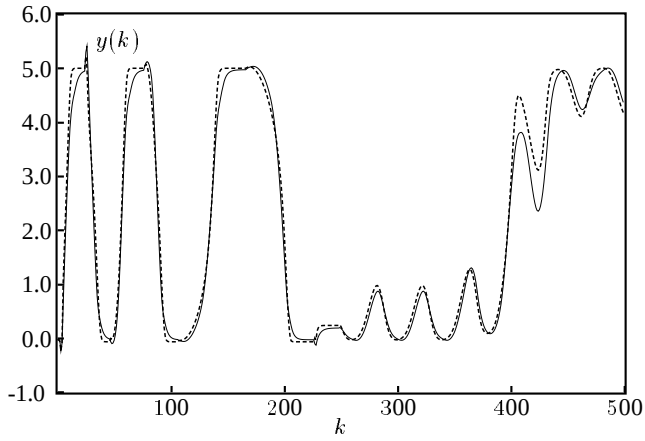

Figure 3: *Reference response to a validation signal (solid line) compared with the response of a model identified from the noisy sequence of Fig. 2 (dashed line)*

Finally, we check the sensitivity of the models to the non linear degree q by identifying NARX inverter models with different q

values. Such experiments highlight the ability of the NARX models to represent highly nonlinear systems even for moderate q values. In these comparisons, the static characteristic of the model is used as an additional index of its ability to reproduce the nonlinear behavior of the original system. For $q = 2$, the shape of the static characteristic cannot be obtained and the identification fails. For $q = 3$, instead, the characteristic is correctly reproduced and the accurate model with $n = 8$ of Tab. 3 is obtained. Moreover, the value $q = 3$ turns out to be an optimum choice for the problem at hand, as higher q values yield only minor improvements. This can be appreciated in Fig. 4, where the reference characteristic and the characteristics of two models with $q = 3$ and $q = 4$ are shown. An interesting method to improve the accuracy of NARX models without increasing q (and hence n) is the use of piecewise models [5]. We identify a piecewise model composed of two submodels with $r = 1$, $q = 3$ and $n = 7$, which works safely and is more accurate than the model with $n = 8$ of Tab. 3. The variance of its error, σ_e^2, is one order of magnitude smaller than the one reported in Tab. 3 and its response to the validation signal is better than the one shown in Fig. 1 (results are not presented for lack of space). In such a 2-piece model, the submodel domains are the two half planes $y < 2.5$ and $y > 2.5$, whereas the switching rule is hysteretic and takes into account the last two y samples.

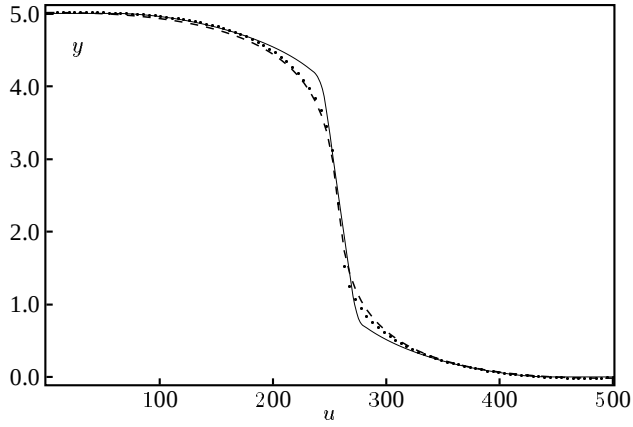

Figure 4: *Static characteristics of the CMOS inverter (solid line), of the model with $q = 3$ and $n = 8$ of Tab.3 (dashed line) and of a model with $q = 4$ and $n = 12$ (dotted line)*

SISO models are useful to assess the possibilities of the NARX approach, but the representation of multiport circuit elements requires Multiple Input Multiple Output (MIMO) models. In the inverter example, we deal with a 2-port element, where, in principle, two of its port variables are controlled by the other two variables. Since CMOS gates operate by forcing the voltages of their output ports, the natural input and output variables of the inverter circuit are v_1, i_2 and v_2, i_1, respectively, defined in the insert of Fig. 5. We identify a NARX MIMO inverter model by exciting the circuit through the input variables v_1 and i_2 and by using $r = 1$ and $q = 4$. The algorithm is applied to a set x defined as $X = \{v_1(k), v_1(k-1), i_2(k), i_2(k-1), v_2(k-1)\}$ and, in spite of the increase of the number of potential components, the identification remains affordable and produces accurate models. The best MIMO model obtained in this way has 16 components and its accuracy can be appreciated in Fig. 5. Such a Figure shows the waveform $v_2(k)$ produced by the MIMO model when it is loaded by a capacitor and is driven by a validation sequence $v_{in}(k)$. The waveform $v_2(k)$ obtained by the MIMO model tracks well the reference response of the simple test circuit.

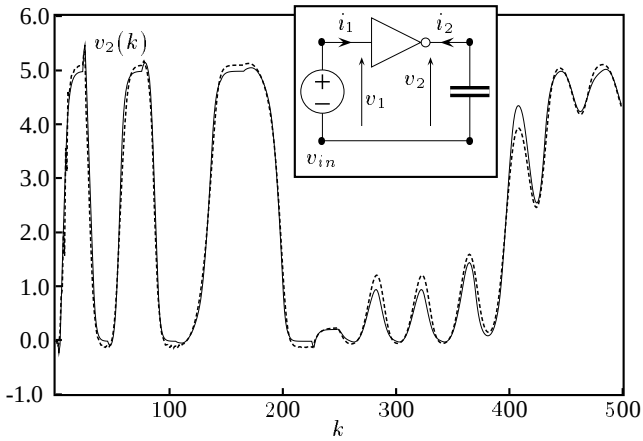

Figure 5: *Waveform $v_2(k)$ of the circuit of the insert for a validation input v_{in}. Solid curve: reference response; dashed curve: response produced by the NARX MIMO inverter model described in the text*

4. CONCLUSION

In this work, we investigate the performances of NARX identification applied to a dynamic highly nonlinear two-port element: the CMOS inverter. The numerical test carried out shows that such an approach has the potential to handle this type of nonlinear systems. The identification process yields accurate models with a moderate number of components, is robust and is practicable also for multiple inputs. Although many aspects should be further investigated before practical applications, the results obtained suggest that NARX identification could be a useful tool for circuit simulations.

5. REFERENCES

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Paper II

Modeling of digital circuits via NARX identification

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1 Introduction

The development of efficient and accurate numerical models to describe the behavior of circuit elements is of paramount importance in the area of circuit simulation. In particular, the availability of techniques for black-box modeling and order reduction of nonlinear dynamic circuit elements would be very useful. Black-box modeling provides the most general approach to the description of poorly known devices, whereas order reduction procedures allow the balancing of model accuracy and efficiency.

The latter point is going to be a dominant issue of future simulation problems. In fact, as circuit applications become more complex and their operations more critical, conventional circuit simulation (too heavy) and functional simulation (too idealized) become ineffective. Fast digital circuits are important examples of this evolution. Many of them are capable of switching times short enough to cause the appearance of propagation effects on internal interconnects. The simulation of these circuits requires nonideal models for both interconnects and gates, whereas the sizes of such problems limit the complexity of models that can be used. However, for logic gates, the right trade-off between model accuracy and complexity is particularly difficult to obtain. In fact, a transistor level description of gates leads to complex models, not affordable in the simulation of realistic problems, whereas simpler nonideal models are hardly devised.

Such a modeling problem would be solved if order reduction methods for nonlinear dynamic system were available. However, while order reduction method are well established for linear systems, their extension to nonlinear ones is difficult [1]. On the other hand, several identification methods for nonlinear systems have been developed and applied in the area of *control systems* [2]. In this situation, nonlinear identification methods become interesting for both black-box modeling and *indirect order reduction*, which follows when the response of a detailed model is used to identify a simpler model.

Owing to the above considerations, this work concerns the application of nonlinear system identification methods to digital circuit elements, which are fast strongly nonlinear systems, possibly with a high dynamic order. We concentrate on NARX models, which are the extension of the widely used ARX models to nonlinear systems. These parametric models are oriented to a full black-box approach, are general enough to accommodate a wide class of systems (*e.g.,* see [3]), and are likely to handle appreciable nonlinear behaviors.

In this work, we try to asses the performances of NARX models and of their identification in the modeling of digital circuits. We carry out the study by applying the NARX identification algorithm proposed in [4] to a CMOS inverter and experimenting with the relevant identification parameters.

2 NARX identification

NARX (Nonlinear AutoRegression with eXtra input) models are discrete-time linear-in-parameter models defined by Kolmogorov-Gabor polynomials [4]

$$y(k) = \bar{y} + \sum_{i=1} a_i x_i + \sum_{i=1}\sum_{j=1} a_{ij} x_i x_j + \ldots + \sum_{i=1}\sum_{j=1}\cdots\sum_{q=1} a_{ij\ldots q} x_i x_j \ldots x_q + e(k) \tag{1}$$

$$X = \{u(k), u(k-1), \ldots, u(k-r), y(k-1), \ldots, y(k-r)\} \tag{2}$$

where $u(k)$, $e(k)$ and $y(k)$ are the samples at the k-th time point of the input, disturbance and output signals, respectively, and x_p is the generic element of X, *i.e.,* the present sample of u or the past samples

of u and y up to the time $k - r$. In (1), every possible product of up to q elements of X contributes to $y(k)$ through the weight coefficients $\{\bar{y},\ a_i,\ a_{ij},\ \ldots\}$, which are the *model parameters*. Every product of elements of X appearing in the linear combination is a *model component*, whereas r and q are the *dynamical order* and the *nonlinear degree* of the model, respectively.

In order to identify the model parameters from the sequence of the input and output samples, we implement and use the algorithm of Pottman et Al. [4]. Since the number of potential components of NARX models grows rapidly with r and q, and makes model identification computationally expensive, we base our implementation on a step forward approach. In such an approach, the model is built by starting from zero components and by adding at each step the component that minimizes the model mean-square error. Such a procedure gives rise to a sequence of models with decreasing mean-square error and increasing number of components. The final model is selected in this sequence by assessing the statistical significance of each model through suitable statistical indexes [4]. Eventually, the obtained model is validated by checking its ability to reproduce the system output for input signals different from those used in the identification process.

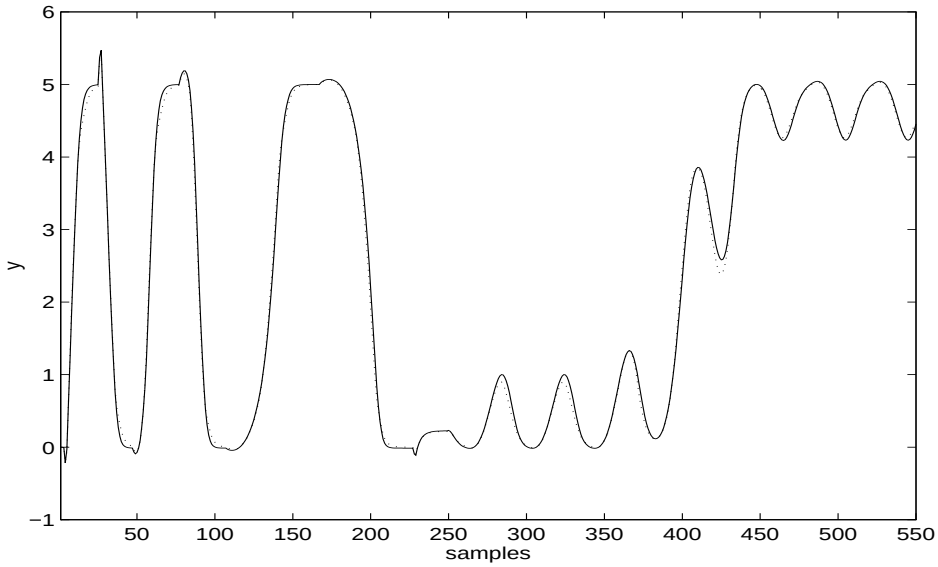

Figure 1: *Model (solid line) and system (dotted line) responses to a input validation signal.*

3 Results

In order to test the performances of NARX models on logical devices, we apply the identification algorithm to an inverter gate of CMOS technology.

The output sequences for the identification are generated by simulating the response of the device to a suitable *identification input signal*. The simulations are performed by PSpice and are based on the CMOS *level 2 model*, which is a detailed transistor model including several parasitics. The simulated output sequences are used either directly, to identify NARX models as simple as possible (order reduction), or corrupted by noise, to reproduce identification from measured data (black-box modeling).

An example of accuracy of a model identified for the CMOS inverter is shown in Fig. 1. The model is built for the single input single output configuration obtained by loading the inverter with an identical one and by using the voltages at its input and output ports as the input ($u(t)$) and the output ($y(t)$) signals, respectively. It is defined by $r = 1$ and $q = 4$ and is composed of 12 components. Its response to an input signal different from the one used for the identification is shown in Fig. 1 and tracks the reference response.

We performed several identification experiments to asses the influence of the identification parameters on the obtained inverter models. In order to test the sensitivity of the models to the non linear degree q we identify inverter models with $q = 2, 3, 4, 5, 6$. Such experiments highlight the ability of the NARX models to represent highly nonlinear systems even for moderate q values. In fact, $q = 4$ turned out to be an optimum choice, as higher q values do not improve significantly the model accuracy.

The selection of suitable identification signals is a critical point in the identification of nonlinear system,

because of the lack of theoretical guidelines. We use identification sequences composed of a small random signal added to a multilevel signal with wide variations. We observe good identification properties and a weak sensitivity of the variance error to the length of the identification sequence.

The ability to identify models from corrupted output sequences is the key property required to use identification for black-box modeling. The identification process used shows high insensitivity to noise effects. Even for SNR of the output signal as low as 20 dB, the identified models remain able to reproduce the qualitative behavior of the original system.

Finally, extensive numerical experiments are devoted to the identification of MIMO (Multiple Input Multiple Output) inverter models. MIMO models are indispensable to represent multiport circuit elements, whose output variables depend, at least, on two input variables. We obtain NARX MIMO inverter models by using the voltage at input port and the current through the output port as input signals and the voltage at the output port as output signal. In spite of the increase of the number of potential components of the model, the identification process remains practicable and the identified models maintain a good level of accuracy. Figure 2 shows the behavior of a model of this kind. The two curves are the responses $v_o(t)$ of the circuit of Fig. 2 to a signal $v_i(t)$ computed by representing the inverter device by the detailed PSpice model and by a MIMO NARX model.

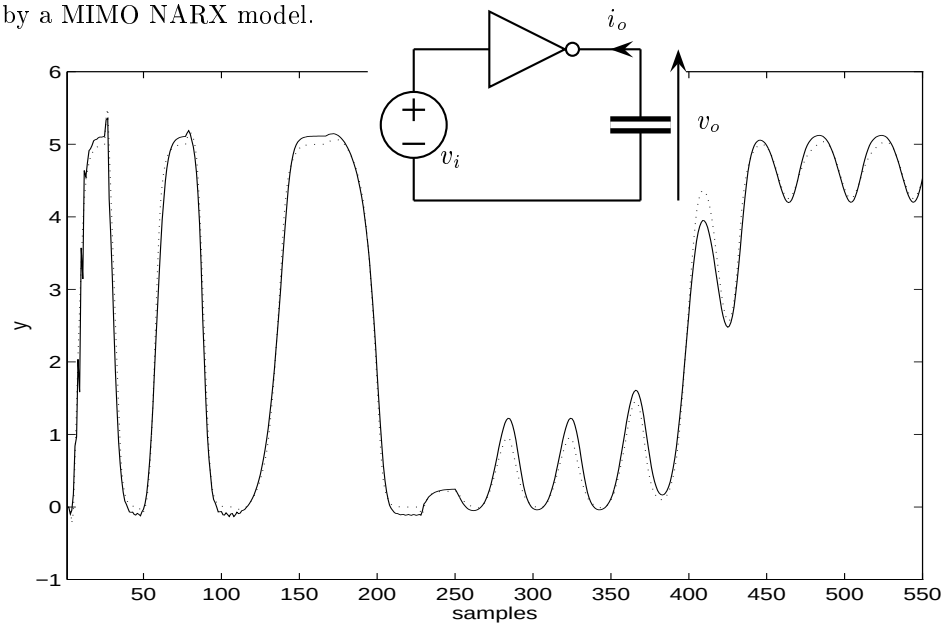

Figure 2: *Waveform $v_o(t)$ for a validation input signal $v_i(t)$ computed by a detailed circuit inverter model (dotted line) and by a MIMO NARX inverter model (solid line).*

In conclusion, we investigate the performances of NARX models applied to a dynamic highly nonlinear two-port element: the CMOS inverter. The numerical test carried out shows that NARX models have the potential to handle such kind of nonlinear systems. Although many aspects should be further investigated before approaching practical applications, results suggest that NARX models could be successfully used for circuit simulations.

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Paper III

BLACK-BOX MODELING OF DIGITAL DEVICES

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Abstract

The design for signal integrity and electromagnetic compatibility of modern fast electronic circuits heavily relies on numerical simulations and requires effective models of active devices. Black-box identification methods based on I/O data may offer a useful systematic approach to build such models. Black-box identification could be used for both the modeling of unknown components and for the refinement or the simplification of existing models. In this paper, we address the black-box identification of digital devices via NARX (Nonlinear AutoRegression with eXtra input) models. We apply a NARX identification algorithm to model a common highly nonlinear and fast electronic device, the CMOS inverter gate, and we perform different tests to assess the effectiveness of such an approach. We obtain accurate models with relatively simple structures and we also verify a low sensitivity of the identification process to the noise affecting the output data.

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1. Introduction

Circuit simulations to assess the signal integrity (SI) and electromagnetic compatibility (EMC) of electronic systems require models of active devices having both an accuracy compatible with the parasitic phenomena of interest and an efficiency compatible with large problems. Fast digital circuits are an important source of this need. In digital applications, functional models of logic components yield too idealized predictions, whereas detailed transistor level models of gates perform at high accuracy levels, but can be hardly afforded in the simulation of realistic problems.

The design of models of digital devices operating at the required level of accuracy and efficiency, however, is not an easy task. Presently, the behavioral description is the most used approach to build models of digital integrated circuits (ICs) for SI/EMC simulations [1, 2]. The behavioral description amounts to characterize ICs by suitable port constitutive relations, possibly obtained from actual or virtual measurements of voltages and currents at the device ports. The structures of behavioral models, however, stems from the physical structures of the device ports and they are mainly useful as one-port equivalents at the IC pins. Also their design is partially empirical and, when not available, the required behavioral data must be measured by specific setups.

The black-box modeling of active devices as nonlinear dynamic systems from their input and output signals may offer a complementary systematic approach to build models of digital devices for SI/EMC simulations. The black-box approach can handle poorly known devices and can help to improve known models from measured signals as well. Besides, black-box modeling could be applied to the I/O signals of existing accurate models as a method for their simplification. Although such a method has a brute-force nature, its use is justified by lack of systematic methods for the direct simplification of nonlinear models [3].

In this paper, we address the black-box modeling of digital devices by NARX (Nonlinear AutoRegression with eXtra input) models. Such models are the extension of the widely used ARX models to nonlinear systems and are general enough to describe a wide class of them (*e.g.*, see [4]), possibly including many nonlinear electric and electronic components. NARX models have been widely studied in the area of *control systems*, where suitable identification algorithms have been developed and successfully applied to moderately nonlinear dynamic systems [5]. Also, the direct derivation of NARX models from nonlinear differential models and a discussion of their effectiveness in the modeling of physical systems have been carried out [6]. We try to assess the performances of NARX models and of their identification in the modeling of highly nonlinear fast dynamic circuit elements. We carry out the study by applying the NARX identification algorithm proposed in [7] to a CMOS inverter and by experimenting with the relevant identification parameters. Since the inverter is the basic element of logic gates, the results obtained in this study should give a first indication of the possibilities of the considered approach in the modeling of digital devices.

2. Identification algorithm

NARX models are discrete-time linear-in-parameter models defined by Kolmogorov-Gabor polynomials [7]

$$\begin{aligned} y(k) = \bar{y} + \sum_{i=1}^{\gamma} a_i x_i + \sum_{i=1}^{\gamma}\sum_{j=1}^{\gamma} a_{ij} x_i x_j + \dots \\ + \underbrace{\sum_{i=1}^{\gamma}\sum_{j=1}^{\gamma}\dots\sum_{p=1}^{\gamma} a_{ij\dots p} x_i x_j \dots x_p}_{q \text{ terms}} + e(k) \end{aligned} \tag{1}$$

$$X = \{u(k), u(k-1), \dots, u(k-r), y(k-1), \dots, y(k-r)\} \tag{2}$$

where $u(k)$, $e(k)$ and $y(k)$ are the samples at the k-th time point of the input, disturbance and output signals, respectively, x_p is the generic element of X, *i.e.*, the present sample of u or the past samples of u and y up to the time $k-r$, and $\gamma = 2r+1$. The integer variables r and q are the *dynamic order* and the *nonlinear degree* of the model, respectively. Every possible product of up to q elements of X is a *potential component* of the model and appears in (1). The potential components with nonzero coefficients are the model *actual components* (or *components* in short) and their coefficients are the *model parameters*.

In order to identify a NARX model from a sequence of I/O samples (*i.e.*, to select the components of the model and compute their parameters), we implement and use the algorithm of Pottman [7]. Since the number of potential components that can compose a NARX model grows rapidly with r and q, making the identification computationally expensive, we base our implementation on a step forward approach. In such an approach, the model is built by starting from a minimal *guess model* (possibly with no components) and by adding at each step the potential component that mostly reduces the model mean-square error.

In detail, the implemented identification algorithm is organized as follows. A model dynamic order r and a nonlinear degree q are chosen. The model dynamic order is estimated a priori from the I/O sequence by the algorithm of [8], whereas the nonlinear degree is estimated empirically. Such a choice defines the set of potential components. Then a guess model is decided and the following three steps are repeated.

1. The reduction of the model mean-square error produced by each potential component not in the *current model* is estimated off-line by orthogonalization of the time sequences [7]. A *new model* is generated by adding to the current one the potential component that minimizes the mean-square error.

2. The stability of the new model is verified and, if necessary, the added component is discarded.

Table 1 Main figures for models of the example of Sec. 2 .

n	e_{max}	σ_e^2	OVF
6	0.2386	2.014×10^{-3}	7.477×10^{5}
7	0.1703	2.014×10^{-3}	8.916×10^{5}
8	0.0712	1.312×10^{-13}	1.381×10^{7}
9	$\mathbf{1.249\times10^{-6}}$	$\mathbf{1.314\times10^{-13}}$	$\mathbf{7.249\times10^{15}}$
10	1.229×10^{-6}	1.306×10^{-13}	6.43×10^{15}
11	1.256×10^{-6}	1.3×10^{-13}	5.8×10^{15}

3. For the new model, the values of suitable statistical indexes are computed [7].

Each execution of the above steps generates a new model, whose statistical significance is assessed by the index values computed in step (3). When a new model has values of the statistical indexes not better than the previous one, the process is terminated and the model with the best values of the statistical indexes is retained as the final one.

As an example, we apply the above procedure to the input/output sequences of a NARX test system and verify its ability to correctly retrieve such system. The test system is defined by the following particular Kolmogorov-Gabor polynomial with $r = 1$ and $q = 4$

$$\begin{aligned} y(k) &= 0.2025 + 0.405y(k-1) + 0.09u(k-1) \\ &\quad + 0.0008y^4(k-1) - 0.0056u(k-1)y^2(k-1) \\ &\quad + 0.177y^2(k-1) + 0.09u(k-1)y(k-1) \\ &\quad - 0.0253y^3(k-1) + 0.01u^2(k-1) \end{aligned} \tag{3}$$

The input *identification sequence* used is obtained by sampling a random multilevel signal with a small white noise superimposed. The identification sequence has 3600 samples, and its level variations are wide enough to highlight the nonlinear nature of (3). Tab. 1 shows the main figures of some of the models generated by the identification procedure for this example. Each row of such a Table describes a different model and lists, from left to right, the number of components of the model (n), the maximum value ($e_{\max}$) and the variance (σ_e^2) of the error between the model and the reference outputs, and the value of the OVF index [7]. The OVF index is a decreasing function of σ_e^2 and of n, so that its maximum should indicate the most significant model of the sequence. For this example, the OVF index is maximum for the model with $n = 9$ (see the bold row of Tab. 1), which indeed coincides with the original system. The detailed structure of models with $n = 8, 9, 10$ is reported in Tab. 2. Models with $n < 9$ are composed of a subset of the component of the original system and their parameters approximate the corresponding parameters of the original system. On the other hand, models with $n > 9$ have the same components and parameters of the original systems plus spurious components with negligibly small coefficients.

Table 2 Structure of models of the example of Sec. 2 .

n	8	9	10
$\bar{y}$	0.1809	0.2025	0.2025
$y(k-1)$	0.3938	0.405	0.405
$u(k-1)$	0.1245	0.09	0.09
$y^4(k-1)$	0.0009	0.0008	0.0008
$u(k-1)y^2(k-1)$	-0.0052	-0.0056	-0.0056
$y^2(k-1)$	0.1824	0.177	0.177
$u(k-1)y(k-1)$	0.0901	0.09	0.09
$y^3(k-1)$	-0.0267	-0.0253	-0.0253
$u^2(k-1)$	—	0.01	0.01
$u^2(k)y^2(k-1)$	—	—	1×10^{-7}

3. NARX inverter models

In this Section, we address the NARX modeling of logic gates by applying the identification algorithm of Sec. 2 to an inverter gate of CMOS technology. We generate the output signals for the identification process via Spice simulations based on the CMOS *level 2 model*, which is a detailed transistor model including several parasitics. The simulated output signals are used either directly, to identify NARX models as simple as possible (model simplification), or corrupted by noise, to reproduce identification from measured data (black-box modeling).

We start by considering a Single Input Single Output (SISO) configuration of the inverter system, obtained by loading the inverter with an identical one and by using the voltages at its input and output ports as the input ($u(t)$) and the output ($y(t)$) signals, respectively. For this system, the estimated order is $r = 1$ and we start with $q = 3$ and a guess model with no components.

As for the example of Sec. 2, we apply to the reference Spice model an input identification signal composed of random levels with superimposed small white noise fluctuations. Such a signal and the corresponding reference output, which is shown in Fig. 1, are then sampled at $T_s = 40$ ps to obtain the input and output sequences for the identification process. For such I/O sequences, the identification process yields the models described in Tab. 3. Since the original system is not of NARX type, the figures of Tab. 3 do not show the net threshold phenomenon shown in Tab. 1. However, among the identified models, the one with the maximum value of the OVF index ($n = 8$) still reveals the most faithful static and dynamic behavior and can be considered the final model. Furthermore, as in the example of Sec. 2, the parameters of the models with $n = 6$ and 7 still approximate the corresponding parameters of the model with $n = 8$.

As a final step, we validate the identified model by verifying its ability to reproduce

Table 3 Main figures of NARX models obtained for a CMOS inverter in SISO configuration by using $r = 1$, $q = 3$ and a guess model with no components

n	e_{max}	σ_e^2	OVF
4	2.427	0.7444	1223
5	2.902	0.8784	916.6
6	1.572	0.1919	2969
7	0.7939	0.01882	27230
8	**0.3862**	**0.01266**	**34640**
9	0.3506	0.01253	30420
10	0.3346	0.01048	32140
11	0.3574	0.0108	28000
12	0.3651	0.01122	24450
13	0.3497	0.01139	22190

the reference output for suitable *validation inputs, i.e.,* for input signals different from the identification input and relevant to the application. We use a validation input signal composed of digital transitions with different edge slopes followed by an analog oscillating waveform. Such a validation input allows to test the identified model for both the input signals occurring under ordinary operation and for possible anomalous inputs occurring in severe distortion regimes. Figure 2 compares the response of the model with $n = 8$ to the validation input against the corresponding reference response, and clearly shows the accuracy of the identified model. Finally it is worth noticing that the complete identification process to obtain the final model for this example requires about 20 s on a 60 MHz Pentium PC.

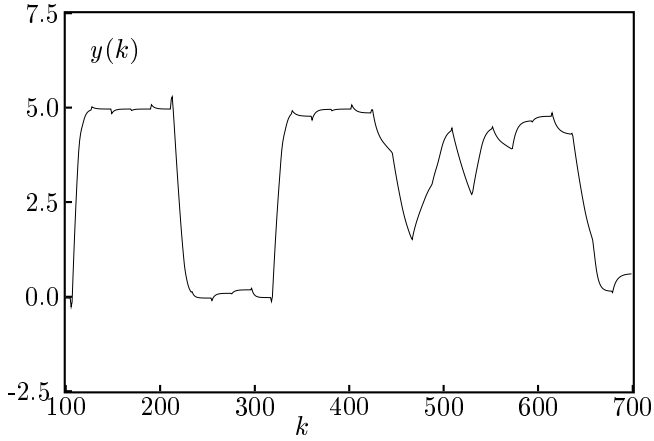

Figure 1 Reference response to the identification input

In order to further assess the performance of NARX identification on the inverter device, we carry out a complete set of identification experiments for the simple SISO

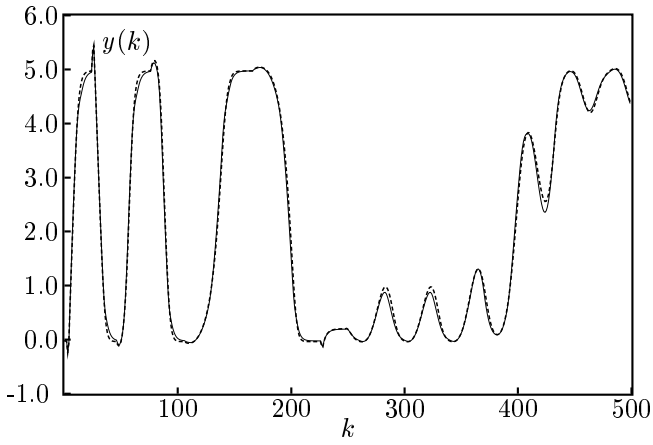

Figure 2 Reference response to a validation input (solid line) compared with the response of the $n = 8$ model of Tab. 3 (dashed line)

configuration.

The first point considered in such experiments is the influence of the guess model. In fact, the sensitivity of the NARX identification to the order in which the model components are selected is a known weakness [6], and the guess model affects such order. We verify that guess models defined by a subset of the components of the $n = 8$ model of Tab. 3 lead to the same final model. In contrast, guess models with components not in the $n = 8$ model may lead to different final models and show that the pure forward approach does not ensure the neutralization of inappropriate components. However those models still offer an excellent level of accuracy with a small number of components.

The next element considered is the identification signal. The selection of suitable identification signals is a critical point in the identification of nonlinear systems, because of the lack of theoretical guidelines. We experiment different types of identification signals and different lengths of the identification sequences. The best results are obtained by random multilevel signals with a small white noise superimposed, as proposed in [9], when the constant levels persist for enough time in comparison with the system "local time constants". In this case we observe good identification properties and a weak sensitivity of the variance error to the length of the identification sequence.

Then we consider the ability of the identification process to obtain models from corrupted output sequences, which is the key property required to use NARX identification for black-box modeling. To check such an ability, we add white noise disturbances of different variance to the simulated output signal and use the resulting signal for the identification. In this way, we observe remarkably good insensitivity to the added noise. In fact, the identification process works also for noisy output sequences, and it leads to the same final model provided the SNR value for the output

sequence is greater than 25 dB. Moreover, although lower values of the SNR of the output sequence lead to different final models, such models remain able to reproduce the qualitative behavior of the original system. As an example, Fig. 3 and Fig. 4 show, respectively, a part of a noisy output identification sequence and a response of the model identified from such a noisy sequence. In this example, the output identification sequence has SNR$=$ 20 dB, and the response of the identified model to a validation signal, shown in Fig. 4, still tracks the reference output.

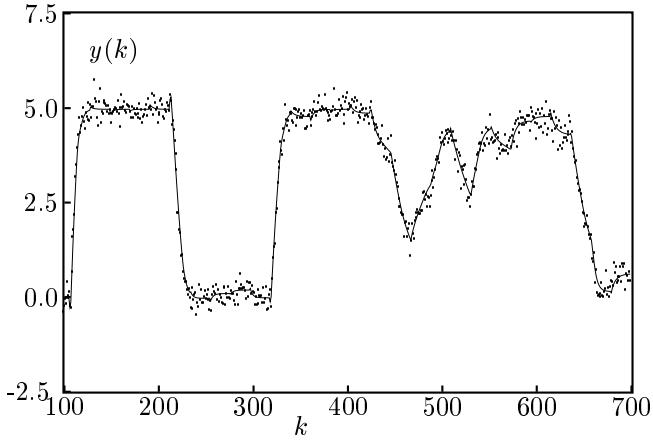

Figure 3 Disturbance added to the reference response for the identification input. Solid line: exact reference response (see Fig. 1); dots: reference response corrupted by added white noise with SNR$=$ 20 dB

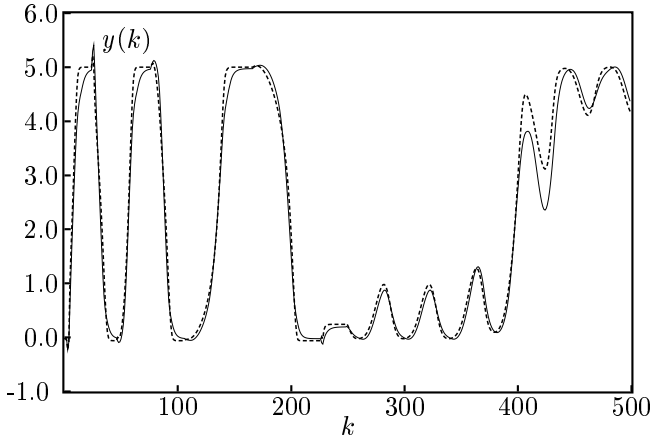

Figure 4 Reference response (solid line) to a validation input, compared with the response of a model identified from the noisy sequence of Fig. 3 (dashed line)

Finally, we check the sensitivity of the models to the non linear degree q by identifying NARX inverter models with different q values. Such experiments highlight the

ability of the NARX models to represent highly nonlinear systems even for moderate q values. In these comparisons, the static characteristic of the model is used as an additional index of its ability to reproduce the nonlinear behavior of the original system. For $q = 2$, the shape of the static characteristic cannot be obtained and the identification fails. For $q = 3$, instead, the characteristic is correctly reproduced and the accurate model with $n = 8$ of Tab. 3 is obtained. Moreover, the value $q = 3$ turns out to be an optimum choice for the problem at hand, as higher q values yield only minor improvements. This can be appreciated in Fig. 5, where the reference characteristic and the characteristics of two models with $q = 3$ and $q = 4$ are shown. An interesting method to improve the accuracy of NARX models without increasing q (and hence n) is the use of piecewise models [7]. We identify a piecewise model composed of two submodels with $r = 1$, $q = 3$ and $n = 7$, which works safely and is more accurate than the model with $n = 8$ of Tab. 3. The variance of its error, σ_e^2, is one order of magnitude smaller than the one reported in Tab. 3 and its response to the validation signal is better than the one shown in Fig. 2 (results are not presented for lack of space). In such a 2-piece model, the submodel domains are the two half planes $y < 2.5$ and $y > 2.5$, whereas the switching rule is hysteretic and takes into account the last two y samples.

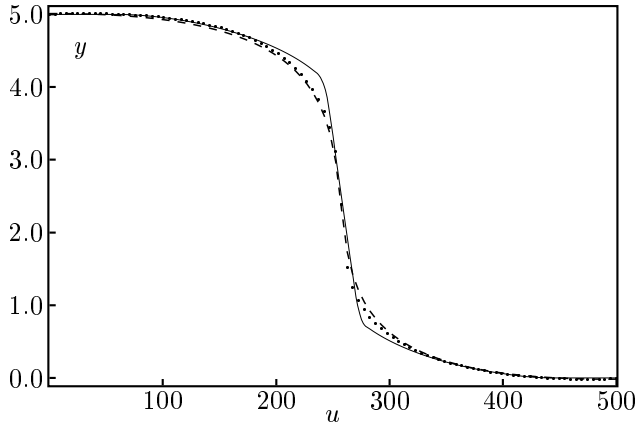

Figure 5 Static characteristics of the CMOS inverter (solid line), of the model with $q = 3$ and $n = 8$ of Tab.3 (dashed line) and of a model with $q = 4$ and $n = 12$ (dotted line)

SISO models are useful to assess the possibilities of the NARX approach, but the representation of multiport circuit elements requires Multiple Input Multiple Output (MIMO) models. In the inverter example, we deal with a 2-port element, where, in principle, two of its port variables are controlled by the other two variables. Since CMOS gates operate by forcing the voltages of their output ports, the natural input and output variables of the inverter circuit are v_1, i_2 and v_2, i_1, respectively, defined in the insert of Fig. 6. We identify a NARX MIMO inverter model by exciting the circuit through the input variables v_1 and i_2 and by using $r = 1$ and $q = 4$. The algorithm is applied to a set x defined as $X = \{v_1(k), v_1(k-1), i_2(k), i_2(k-1), v_2(k-1)\}$ and, in spite of the increase of the number of potential components, the identification

remains affordable and produces accurate models. The best MIMO model obtained in this way has 16 components and its accuracy can be appreciated in Fig. 6. Such a Figure shows the waveform $v_2(k)$ produced by the MIMO model when it is loaded by a capacitor and is driven by a validation sequence $v_{in}(k)$. The waveform $v_2(k)$ obtained by the MIMO model tracks well the reference response of the simple test circuit.

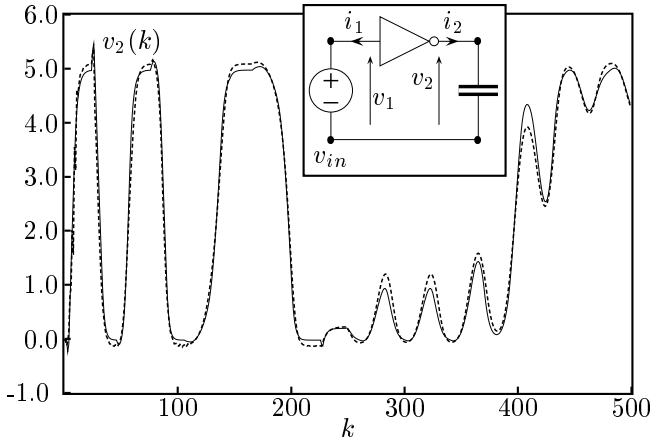

Figure 6 Waveform $v_2(k)$ of the circuit of the insert for a validation input v_{in}. Solid curve: reference response; dashed curve: response produced by the NARX MIMO inverter model described in the text

4. Spice comparison

Since device models must operate effectively in circuit simulation environments, in this Section, we check the performances of CMOS NARX models implemented in Spice. This is done by comparing the Spice implementation of the $n = 8$ NARX SISO model of Tab. 3 and the reference transistor level model generating such a NARX model.

For an effective Spice implementation, the discrete-time NARX model is approximated by a continuous-time state-space representation. As an example, for any NARX model of dynamic order $r = 1$ and arbitrary non linear degree q, which writes

$$y(k) = f(u(k), u(k-1), y(k-1)) \tag{4}$$

where f is a suitable polynomial function, a possible discrete-time state-space form is

$$\begin{cases} \bar{u}(k) &= u(k+1) \\ x_1(k) &= \bar{u}(k-1) \\ x_2(k) &= f(\bar{u}(k-1), x_1(k-1), x_2(k-1)) \\ y(k) &= x_2(k) \end{cases} \quad (5)$$

The above equation are converted into a continuous-time state-space representation by replacing back the time variable (the input and output signal samples are 40 ps spaced) and by replacing the difference operator with the differential one. The continuous time state-space model is then implemented in Spice by using standard components as capacitors, resistors and driven sources.

The error of the Spice continuous-time version of the $n = 8$ NARX SISO model of Tab. 3 with respect to the original discrete-time model turns out to be negligible. On the other hand, the Spice implementation of the NARX model remains significantly more efficient than the Spice reference transistor level model. Such an efficiency can be appreciated by Tab. 4, that shows the CPU times to compute a validation response for the Spice-NARX and for the Spice transistor level models.

Table 4 CMOS and NARX inverter simulation time

model	*transient analysis [s]*	*iterations*
CMOS	55	5897
NARX	26	4642

5. Conclusion

In this contribution, we have studied the black-box modeling of the CMOS inverter gate from its input and output signals via NARX identification, in order to evaluate the usefulness of such an approach. We have obtained simple NARX models (*i.e.*, models defined by a moderate number of components) performing at a fairly good accuracy level. We also have verified a low sensitivity of the identification process to the noise added to the output signal and the feasibility of the Spice implementation of the NARX models. Although this study is a preliminary one, results obtained clearly show the potential of the NARX black-box approach for the SI/EMC oriented modeling of digital devices.

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Paper IV

SIGNAL INTEGRITY AND BEHAVIORAL MODELS OF DIGITAL DEVICES

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Abstract The behavioral modeling of digital integrated circuits is becoming an important resource for the simulations of large and critical digital circuits. In this paper, we address the behavioral modeling of CMOS integrated circuit on the basis of the Input/output Buffer Information Specification (IBIS). The aim of this work is to provide guidelines to build executable models from IBIS data, which is not provided by the IBIS specification itself. Such an ability is of paramount importance for the validation of IBIS data sets through the comparison of measured transient responses of digital devices and the corresponding responses obtained by IBIS models. Besides discussing basic elements of IBIS models and their critical points, we propose an effective IBIS model, which offers improved accuracy and efficiency, and can be effectively exploited for experimental validations.

1. Introduction

Fast digital signals on Printed Circuit Boards (PCBs) are inherently analogic and, as clock rates become higher and higher, Signal Integrity (SI) simulations must be carried out to ensure proper design. SI simulations must be efficient and accurate enough to handle large circuits and to allow the assessment of the critical features of waveforms, such as *delays, threshold crossings, overshoots, dc levels* and *crosstalk noise* [1]. Such abilities heavily depend on the available models of circuit elements. Models of passive elements of PCBs (*e.g.,* interconnects, junctions, connectors, etc.) have been widely studied and are sufficiently established, whereas models of digital Integrated Circuits (IC) are in the beginning of their development.

In this paper, we address the development of a model for CMOS digital ICs based on the behavioral I/O Buffer Information Specification (IBIS). The use of behavioral models of digital ICs is establishing as an effective approach to the SI simulation of large and critical PCBs and the IBIS standard is going to be a key resource of such an approach. The IBIS description of a digital IC amounts to a software-parsable ascii-file collecting information on the electric behavior of the device ports. IBIS data files can easily describe complex ICs with thousands of pins and their use is strongly encouraged by IC manufacturers, who can distribute characteristics of their devices without disclosing proprietary information.

In order to be used for SI simulations, IBIS behavioral data must be translated into a suitable set of characteristic equations, *i.e.,* into an executable behavioral model. IBIS models can be obtained as built-in features in most Electronic Design Automation (EDA) software tools for SI simulations or they can be designed and built by the final user. EDA tools help users with ready to use IBIS models but hide what they do with IBIS data. On the contrary, self-made models allow a complete control on how IBIS data are processed, yet their design is not trivial because no explicit help is provided by IBIS documents. In fact, the way in which IBIS models are built from an IBIS file is beyond the scope of the IBIS standard, as it is clearly stated in the following sentence of [2]: *"Please note that the IBIS specification does NOT define an executable simulation model — it is a standard for the formatting and transfer of data. As such, the specification defines what the information included in an IBIS file represents and how it is to be gathered. It does not specify what an analog simulation application does with the data."*

In spite of such a difficulty, the design of self-made completely accessible IBIS models is worthwhile for the experimental validation of IBIS data. SI simulations, along with data and model used for them, should be continuously checked against measurements. Concerning IBIS data, however, their experimental validation via direct measurement is a difficult task for final users. Easier validations are possible by comparing measured device responses to test loads with the waveforms predicted by an IBIS model [3]. For this approach, a reliable IBIS model is required to describe the device behavior when it is connected to the test loads and to the measuring equipment. Besides, such an IBIS model should be also under the complete user control, in order to facilitate the debugging of possible inconsistencies between measured and computed waveforms.

For such reason, in this paper, we discuss the design of IBIS models from the user point of view. The study is centered on a formal analysis of IBIS models and their properties and leads to an effective IBIS model for CMOS ICs. Though the model is primarily intended for validation purposes, it turns out to be also highly efficient and therefore suitable to large scale SI simulations.

2. The IBIS standard

In this Section, we shortly review the key features of the IBIS standard. The idea underlying the standard has been proposed and studied by INTEL and other IC producers and EDA vendors in 1993. Since then, the "EIA IBIS Open Forum" has worked to establish and coordinate the development of the standard, that has rapidly grown by accommodating a large number of digital technologies [4].

An IBIS data file describes the electric behavior of the ports of a single digital integrated circuit (possibly including the variations due to production tolerances). The description is limited to the port layer, *i.e.,* no information on the device internal functions is included. The core of the standard is contained in the original version 1.1 of specifications and is best illustrated through the example IBIS data file of Tab. 1. Such a file is composed of three main parts: the *header*, the *pin-map* and the *silicon data* (see Tab. 1).

Table 1: Example of IBIS version 1.1 data file

Header

```
[IBIS Ver]    1.1
[File name]   example.ibs
[File Rev]    0.1
[Date]        09/12/98
[Source]      ...
[Notes]       ...
|
[Disclaimer] ...
|
[Component]   xyz
[Manufacturer]..
[Package]
|             typ        min        max
R_pkg         0.020      NA         NA
L_pkg         1.75nH     NA         NA
C_pkg         0.16pF     NA         NA
|
```

Pin-map

```
[Pin]  signal_name model_name  R_pin  ...
|
1      A1          buf1        ...
2      A2          buf2        ...
...    ...         ...
100    GND         Ground
|
```

Silicon data

```
[Model]       buf1
Model_type    Output
Polarity      Non-Inverting
Enable        Active-Low
|
Numeric data of buf1
...           ...
| [END]
```

The *header* part lists the key elements identifying the file and the associated device. The specification assumes that each device pin, which is the input of a device port, is connected to the actual port on the integrated circuit (the silicon port) by an electric equivalent of the package, which is composed of a shunt capacitor `C_pkg` and a series inductor `L_pkg` and resistor `R_pkg`. The default values of such package parameters are also listed in the header part, possibly distinguishing between typical, worst and best case values.

The *pin-map* part lists, for each pin of the device, the name of the applied signal, the name of the data set describing the silicon port to which the pin is connected (under column `model_name` in Tab. 1) and, possibly, the values of the package parameters to be used for that pin in place of default ones.

The *silicon data* part is the most important one, it contains the data sets describing the various types of silicon ports on the IC. For each silicon port, the data are collected and organized by assuming a specific physical structure of the port. To continue with the example, we specialize the following discussion to CMOS output ports (the CMOS input ports are a simpler subcase of this one). For such a silicon port the IBIS standard assumes the physical structure shown in Fig. 1 and classifies the following data (see Tab. 2).

(1) MOS transistors:

- 1.1 output capacitance (the `C_comp` parameter of Tab. 2)
- 1.2 MOS static characteristics $i_d(v_o)$ @ $v_i = 0$ and $i_u(V_{cc} - v_o)$ @ $v_i = V_{cc}$, where v_i is the IC internal voltage controlling the state of the output port (the `[pulldown]` and `[pulldup]` data of Tab. 2)
- 1.3 slopes of the rising and falling edges of $v_o(t)$ during state transitions (the `[Ramp]` data of Tab. 2)

(2) Protection diodes:

- 2.1 diode static characteristics $i_g(v_o)$ and $i_p(v_o - V_{cc})$ (the `[GND_clamp]` and `[Power_clamp]` data of Tab. 2)

The slopes of the output voltage during state transitions are measured when the port is loaded by a reference resistor (`[R_load]`) and complete turn on and

off processes are carried out. The slopes are defined as the ratio $\Delta v_o/\Delta t_r$ ($\Delta v_o/\Delta t_f$), where Δv_o is the voltage variation occurring between 20% and 80% (80% and 20%) of the total swing and Δt_r (Δt_f) is the time required for such a variation. Of course such a specification assumes nearly linear edge ramps.

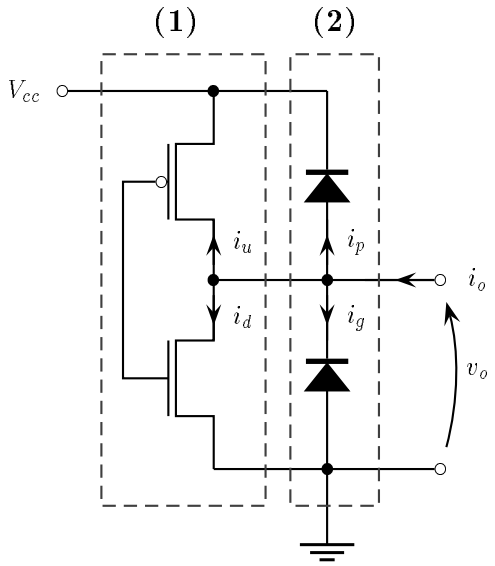

Figure 1: **Physical structure assumed by IBIS for the integrated part of a CMOS output port.**

Table 2: Numerical data of silicon port `buf1` of the file of Tab. 1

```
|              typ          min          max
C_comp         2.58pF       2.33pF       2.85pF
|
[Pulldown]
|Voltage       I(typ)       I(min)       I(max)
|
-5.0000        -180.8445mA  NA           NA
-4.5000        -159.5622mA  NA           NA
...            ...          ...
|
[Pullup]
|Voltage       I(typ)       I(min)       I(max)
|
10.0000        -241.9660mA  NA           NA
9.5000         -219.7553mA  NA           NA
...            ...
|
[Ramp]
|              typ          min          max
dV/dt_r        2.0/0.94n    NA           NA
dV/dt_f        2.4/0.99n    NA           NA
R_load         200
|
[POWER_Clamp]
|Voltage       I(typ)       I(min)       I(max)
|
-5             293e-3       NA           NA
-1             25e-3        NA           NA
...            ...
|
[GND_Clamp]
|Voltage       I(typ)       I(min)       I(max)
|
-5             293e-3       NA           NA
-1             25e-3        NA           NA
...            ...
|
```

3. IBIS models

An IBIS model is a set of computable port characteristic equations (possibly specified by an equivalent circuit composed of ideal elements) which are based on the data of an IBIS file. According to the physical structure assumed and to data supplied for a CMOS output port as well as to comments contained in official IBIS documentation, IBIS models of such a part must be described by the two-terminal element shown in Fig. 2. From the formal point of view, the characteristic of the variable nonlinear resistor $\bar{\imath}(v_o)$ contained in such models must satisfy the following two requirements.

(a) Behavior when the output is forced in LOW or HIGH state since long enough time:

$$\bar{\imath} = \begin{cases} i_d(v_o) & \text{for LOW} \\ @\ v_i = 0 & \text{output state} \\ & \\ i_u(V_{cc} - v_o) & \text{for HIGH} \\ @\ v_i = V_{cc} & \text{output state} \end{cases} \qquad (1)$$

(b) Behavior during state transitions:
when the voltage v_i controlling the state of the output port crosses the logic threshold the i_d and i_u characteristics must be replaced in a way that ensures a linear variation of $v_o(t)$ with either $\Delta v_o/\Delta t_r$ slope or $\Delta v_o/\Delta t_f$ slope

The above formal definition of IBIS models for CMOS output ports highlights two important points. Firstly, as in IBIS models state transition are merely decided by threshold crossings, no analogic information contained in the waveform of the internal voltage v_i can be transmitted to the output terminals. Secondly, the key element of CMOS IBIS models is the variable nonlinear resistor $\bar{\imath}(v_o)$ that must describe both the steady state and the switching behavior of the two MOS transistors. For such a resistor, the design of an effective switching mechanism satisfying condition (b) is not trivial, and IBIS models mainly differ in such a mechanism.

4. The proposed model

The IBIS models we propose for a CMOS silicon output port (described according to IBIS ver. 1.1 specifications) is defined by the equivalent circuit of Fig. 2 and by the following equations for the variable non-

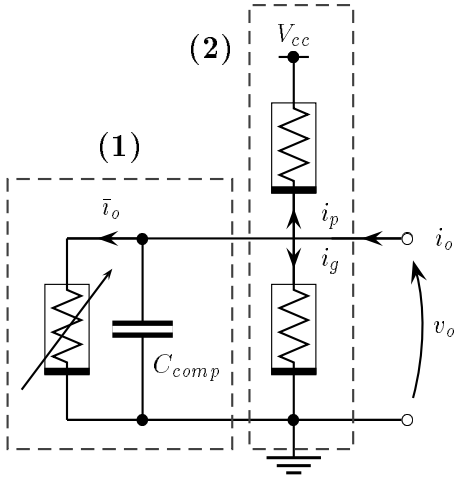

Figure 2: **Electrical equivalent of IBIS models for the silicon output port of a CMOS integrated circuit.**

linear resistor and its switching control mechanism

$$\bar{i} = i_d(v_o)f_d(x) + i_u(V_{cc}-v_o)f_u(x) \quad (2)$$

$$\frac{dx}{dt} = \frac{\Delta v_o}{\Delta t_r}u(v_i - v_{\rm th})u(V_{cc}-x) - \frac{-\Delta v_o}{\Delta t_r}u(v_{\rm th}-v_i)u(x) \quad (3)$$

In the above equations, $i_d(v_o)$ and $i_u(V_{cc}-v_o)$ indicate the pull-down and pull-up curve measured at $v_i = 0$ and $v_i = V_{cc}$, respectively (a non inverting relation v_i–v_o is assumed); $f_u(x) = [(|x|+x)/2V_{cc}]^2$, $f_d(x) = f_u(V_{cc}-x)$, $v_{\rm th}$ denotes the threshold for the controlling voltage v_i and $u(\cdot)$ is the ideal step function.

In eq. (2) x is a control parameter, playing the role of the gate voltage v_g of the two MOS transistors. Functions $i_d(v_o)f_d(v_g)$ and $i_u(V_{cc}-v_o)f_u(v_g)$ can be considered as rough approximations of the output static characteristic surfaces of the two MOS transistors $i_d(v_o, v_g)$ and $i_u(V_{cc}-v_o, v_g)$, respectively. In this way, the characteristic specified by eq. (2) (and shown in Fig. 3) is a rough approximation of the output static characteristic surface of the two complementary transistors. As the x parameter is varied, a continuous variation of $\bar{i}_o(v_o)$ between $i_d(v_o)$ and $i_u(V_{cc}-v_o)$ occurs, which mimics the actual variation of the output characteristic of the couple of complementary MOS transistors during a state transition. Owing to this property, we name the proposed IBIS model Gradual Switching (GS) model.

The state eq. (3) controls the velocity of state transitions. Such an equation has two equilibrium solutions $x = 0$ and $x = V_{cc}$. If $x = 0$, as v_i grows above $v_{\rm th}$, $x(t)$ grows linearly from 0 to V_{cc} in a time $t_r = (\Delta t_r/\Delta v_o)V_{cc}$. Whereas, if $x = V_{cc}$, as v_i decreases below $v_{\rm th}$, $x(t)$ decreases linearly from V_{cc} to 0 in a time $t_f = (\Delta t_f/\Delta v_o)V_{cc}$. Each ramp of $x(t)$ produces a rising or falling edge in the output voltage $v_o(t)$, whose total duration is either t_r or t_f and whose shape is decided by the x–v_o relation (2) and is of sigmoid type. Though such edges are not linear, as required by IBIS, owing to the nature of the model, which mimic transitions of actual devices, they are likely to be (or to be made by parameter tuning) more accurate than purely linear ones.

Finally, it is ought to remark that the model can be easily extended to include more than one threshold.

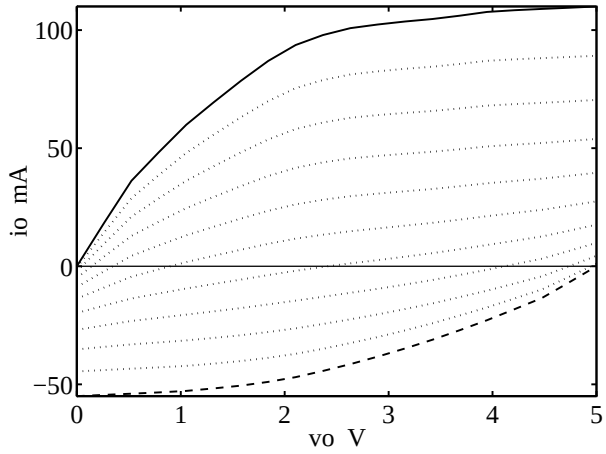

Figure 3: **Characteristic of the variable nonlinear resistor $\bar{i}_o$ as a function of v_o for different x values. The solid and the dashed curves hold for $x = 0$ and $x = V_{cc}$, respectively, and coincide with $i_d(v_o)$ and $i_u(V_{cc}-v_o)$, respectively. Dotted curves hold for x varying between 0 and V_{cc}.**

5. Model accuracy

In order to validate our IBIS model and to check its performances versus other IBIS models, we compare its response to the responses of an accurate Spice transistor level model and of a commercial IBIS model. The commercial IBIS model involved in the comparison is for Spice based simulators and it uses an abrupt switching of the pull-up and pull-down characteristics to describe logic state transitions. To satisfy IBIS specifications, the model uses a control mechanism producing linear variations of the output voltage during state transitions. Owing to its principle of operation, we indicate the commercial model as the Instantaneous Switching (IS) model.

The Device Under Test (DUT) for the comparison is a CMOS output buffer composed of four couples of 1.2 μm complementary MOS transistors with growing areas designed to minimize the circuit delay. The DUT is accurately modeled by a Spice transistor level model (the reference model of the comparisons)

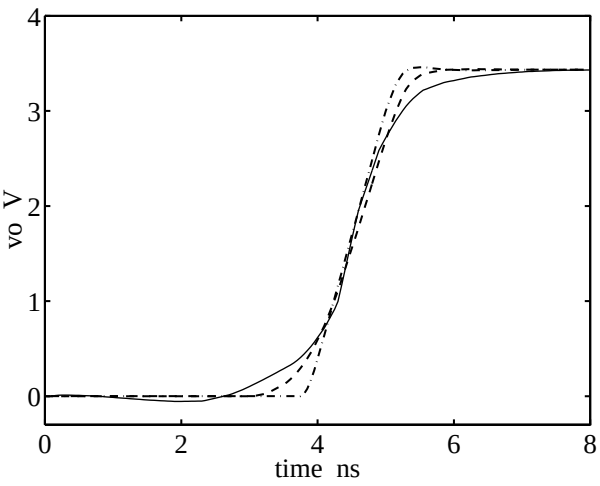

Figure 4: **Voltage waveforms $v_o(t)$ computed by the three models under comparison for the DUT loaded by the reference resistor used in the definition of `[Ramp]` parameters. Solid line: reference curve; dashed line: response of the GS model; dashed-dotted line: response of the IS model.**

based on Spice Level 2 models of MOS transistors. The reference model and the IBIS specification are then used to build an IBIS data set describing the DUT output port and such a data set is used to feed both the GS and the IS IBIS models.

We check the two IBIS models by using them to compute the responses of different test circuits obtained by connecting the DUT to test loads, and by comparing the computed responses with the responses of the reference model. In order to carry out computations by the same simulation engine, we implemented our GS model as a Spice subcircuit, likewise to the IS and the reference models.

The first test circuit considered is composed of the DUT loaded by the reference resistor used to measure the rise and fall times of the `[Ramp]` keyword (*i.e.,* a 200 Ω resistor). Figure 4 shows the rising edge of the output voltage waveforms computed for this circuit by the three models. Even for the simple DUT considered, the output voltage waveforms have edge shapes deviating from the linear shape and both IBIS models miss the corners of the reference response. However, according to its structure, the IS model produces almost linear edges, and, therefore, it yields the worst approximation. In contrast, the GS model produces edges shaped by the continuous output characteristics (2), and it yields the best approximation. It should be remarked that comparisons are carried out by using the same input IBIS data for both IBIS models. The GS model yields good edge approximations even without tuning of the [Ramp] parameters, as we would have supposed.

Efficiency and stability comments are also in order. The GS models turns out to be the most efficient of the two IBIS models. As an example, Spice requires about 35 s, 12.5 s and 6.5 s on a 486 PC to compute the reference, the IS and the GS curves of Fig. 4, respectively. Besides, the IS model, turns out to be also affected by convergence problems, and for some of the load conditions tested Spice was not able to compute the IS responses.

The second test circuit considered is composed of the DUT loaded by a 50 Ω resistor and a shunt 5 pF capacitor. This test load exceeds the driving capabilities of the DUT and is very different from the reference load used to obtain the rise and fall times; it is used to check the behavior of IBIS models outside their validity range. Figure 5 shows the output voltage waveforms computed for this circuit by the three models when a logic HIGH pulse lasting 8 ns is applied by the DUT. In this second test, the GS model still yields a good approximation of the edge slopes and of the first corners of edges, and a rough approximations of the second corners of edges. The IS model, instead, misses every corner and, even worse for SI applications, completely misses the slope of the falling edge and adds spurious ringings on its second corner. Ringing effects added by the IS models were observed in many other test cases and a relation of such ringings with the switching mechanism of the model is suspected.

The third test circuit considered is composed of the DUT loaded by an ideal TL terminated by a 5 pF capacitor at the far end. This circuit is one the test circuits recommended by [3] to crosscheck the whole set of IBIS data describing an output port. In fact, its response is influenced by both the reflection to the TL line caused by the characteristics of the output port (both parasitics and nonlinear static characteristics) and by the pulse waveforms feed to the TL. The TL of our test has 100 Ω characteristic impedance and 1 ns time delay. Figure 6 shows the voltage waveforms at the far end of the TL computed by the three models, when the DUT feeds the line with a logic HIGH pulse lasting 8 ns. For this test, the GS models reproduces qualitatively the reference waveform, whereas the IS model misses corners and falling edges, and adds ringings. Besides, the falling edges of the IS response are appreciably out of time. Unfortunately, timing problems are common to all IBIS models, as the timing of the output waveform is decided by the input waveform via a threshold. This problem is an inherent limitation of IBIS models that should be further studied.

The comparisons shown in this Section confirm that the switching between logic states is a critical point of IBIS models. A careful design of the switching mechanism is required to avoid significant loss of accuracy as well as low efficiency and stability problems. Our GS model improves the performances of the IS model offering better accuracy and efficiency.

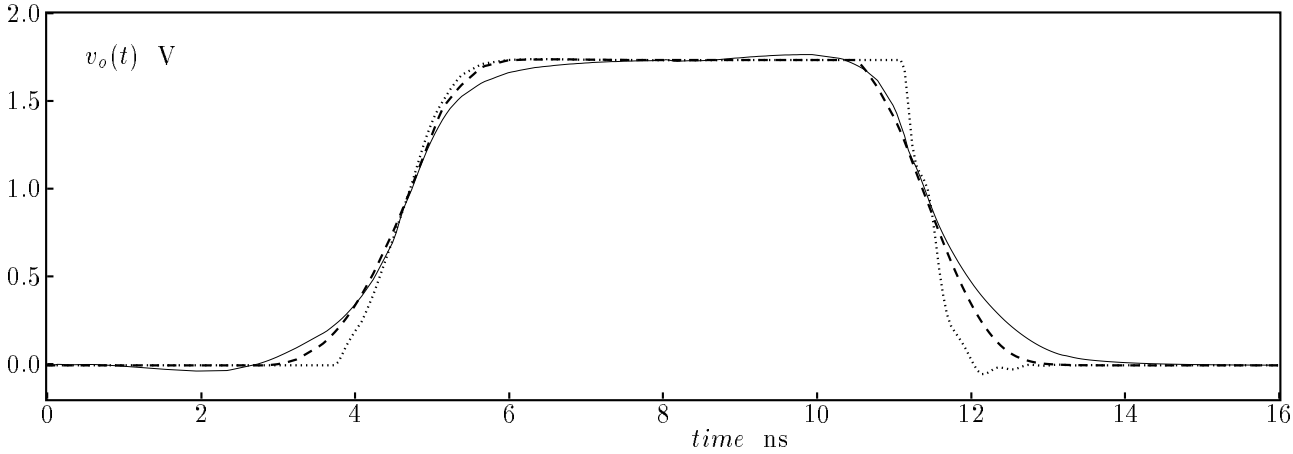

Figure 5: **Voltage waveforms $v_o(t)$ computed by the three models under comparison for the DUT loaded by a $50\,\Omega$ resistor and a 5 pF capacitor. Solid line: reference curve; dashed line: response of the GS model; dotted line: response of the IS model.**

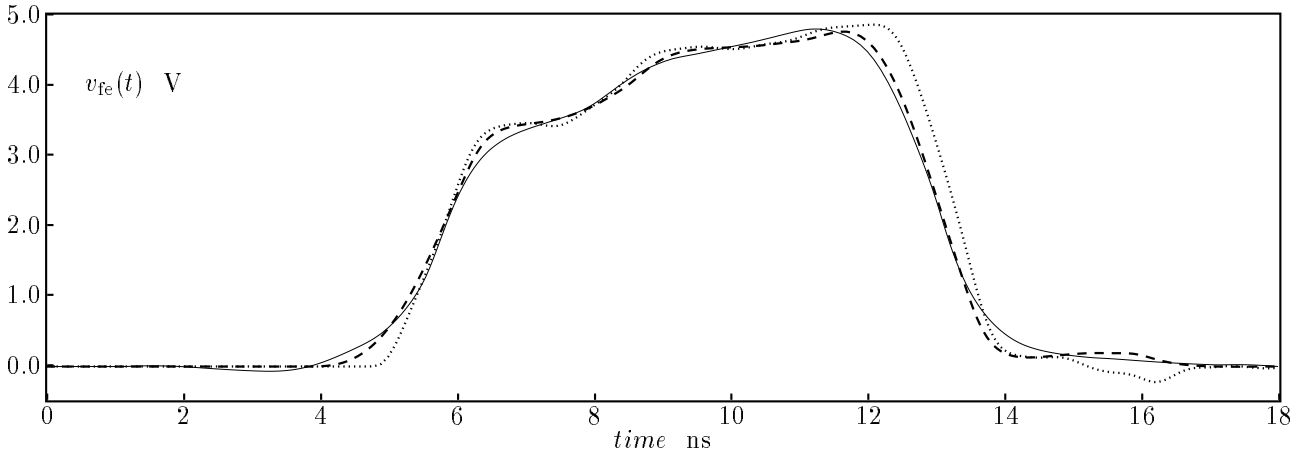

Figure 6: **Voltage waveforms at the far-end termination of an ideal TL loading the DUT (see Sec. 5) $v_{\mathrm{fe}}(t)$ computed by three models under comparison. Solid line: reference curve; dashed line: response of the GS model; dotted line: response of the IS model.**

It grasps the qualitative behavior of the waveforms and appears adequate for experimental validation purposes. On the other hand, this study shows also that even simple devices falling under 1.1 IBIS specification can lead to waveforms with scarcely linear edge shapes, which are hardly reproduced by IBIS 1.1 models. Furthermore the lack of transmission information in IBIS models creates considerable difficulties in reproducing the correct timing of waveforms. Further study of such weaknesses is in order.

6. Conclusions

In this paper, we propose an IBIS model for CMOS gates, which is intended for reference use in experimental validation of IBIS data sets. The study carried out shows that the description of the switching between logic states is a critical point of IBIS models. The proposed model describes the change of logic state by a gradual switching of the output characteristics and it offers improved accuracy and efficiency. Though the proposed model appears suitable for its original purpose, its performances highlight inherent limitations of IBIS models that should be further studied to exploit the entire potential of this standard in SI applications.

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Paper V

BEHAVIORAL MODELS OF DIGITAL DEVICES

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1. Introduction

The behavioral modeling of digital Integrated Circuits (ICs) is becoming an important resource for the Signal Integrity (SI) analysis of large and critical digital circuits. In fact, such a modeling approach seems both efficient and accurate enough to compute realistic waveforms in actual digital applications.

In this paper, we address the behavioral modeling of CMOS integrated circuit on the basis of the Input/output Buffer Information Specification (IBIS). The IBIS description of a digital IC amounts to a software-parsable ASCII-file collecting information on the electric behavior of the device ports. IBIS data files can easily describe complex ICs with thousands of pins and their use is strongly encouraged by IC manufacturers, who can distribute the relevant characteristics of their devices without disclosing proprietary information. The idea underlying the standard has been proposed and studied by several IC producers and Electronic Design Automation (EDA) vendors since 1993. Since then, the "EIA IBIS Open Forum" has worked to establish and coordinate the development of the standard, that has rapidly grown by accommodating a large number of digital technologies [1, 2].

In order to be used for SI simulations, IBIS behavioral data must be translated into a suitable set of characteristic equations, *i.e.,* into an executable behavioral model. IBIS models (*i.e.,* executable models based on IBIS data) can be obtained as built-in features in most EDA software tools for SI simulations or they can be designed and built by the final user. This latter task, however, is not trivial, because the design of executable models is beyond the scope of IBIS (*e.g.,* see [2]). The aim of this work is to provide guidelines to build IBIS models, which are not provided by IBIS itself. In the following, we discuss the basic elements and the critical points of IBIS models, leading to an effective IBIS model of CMOS ICs. Such a model offers improved accuracy and efficiency, and can be effectively exploited for SI simulations in the Spice environment.

2. IBIS data and models

The IBIS file of an IC component lists data describing the electric behavior of its ports. Data are collected and organized by assuming a specific physical structure of the ports (see [1] for a complete description). Here we focus on the description of CMOS output ports (input ports are a simpler subcase of this one) according to ver. 1.1 of IBIS, which is the core of the standard. For such ports, IBIS assumes a physical structure composed of an output pin connected via a bonding (modeled by an *RLC* equivalent) to the integrated output circuit (the *silicon port* thereafter) of Fig. 1a. The IBIS data provided for the silicon port are: (1.1) the output capacitance of the complementary MOS transistors ($C_{\rm comp}$); (1.2) the static characteristics $i_d(v_o)$ and $i_u(V_{cc}-v_o)$ holding when the port is driven to LOW and HIGH logic states, respectively (usually named pull-down and pull-up curve, respectively); (1.3) the slopes of the rising and falling edges of $v_o(t)$ during state transitions (which are assumed linear by the specification); (2.1) the static characteristics of the protection diodes $i_g(v_o)$ and $i_p(V_{cc}-v_o)$.

An IBIS model is a set of computable port characteristic equations (possibly specified by an equivalent circuit composed of ideal elements) which are based on the data of an IBIS file. According to the physical structure of Fig. 1a and to data supplied for a CMOS output port as well as to comments contained in official IBIS documentation, IBIS models of a silicon port must be described by the two-terminal element shown in Fig. 1b. From the formal point of view, the characteristic of the variable nonlinear resistor $\bar{i}(v_o)$ contained in such models must satisfy the following two requirements.

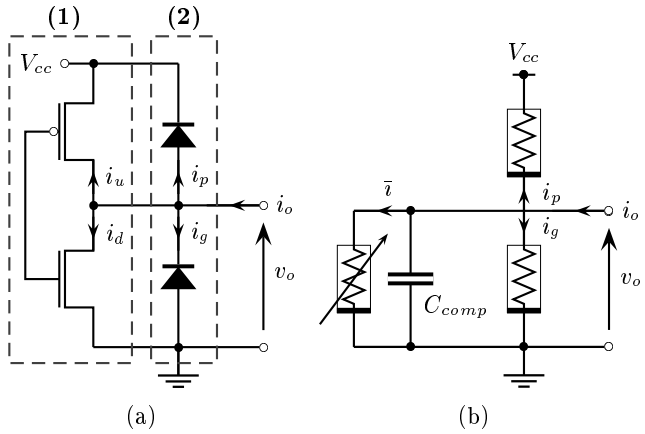

Figure 1: *(a) Physical structure assumed by IBIS for the integrated part of a CMOS output port. (b) Electrical equivalent of the CMOS output port IBIS model.*

(a) Behavior when the output is forced in LOW or HIGH state since long enough time:

$$\bar{i} = \begin{cases} i_d(v_o) & \text{for LOW output state} \\ i_u(V_{cc}-v_o) & \text{for HIGH output state} \end{cases} \quad (1)$$

(b) Behavior during state transitions:
when the voltage controlling the state of the output port (an internal voltage v_i) crosses its logic threshold, the i_d and i_u characteristics must be replaced in a way that ensures a linear variation of $v_o(t)$ with the slopes specified in (1.3), above.

The above formal definition of IBIS models for CMOS silicon ports highlights two important points. Firstly, as in IBIS models state transition are merely decided by threshold crossings, no analogic information contained in the waveform of the internal voltage v_i can be transmitted to the output terminals. Secondly, the key element of CMOS IBIS models is the variable nonlinear resistor $\bar{i}(v_o)$ that must describe both the steady state and the switching behavior of the two MOS transistors. For such a resistor, the design of an effective switching mechanism satisfying the second condition is not trivial, and IBIS models mainly differ in such a mechanism.

3. The proposed model

The IBIS models we propose for a CMOS silicon output port is defined by the equivalent circuit of Fig. 1(b) and by the following equations for the variable nonlinear resistor and its switching control mechanism

$$\bar{i} = i_d(v_o) f_d(x) + i_u(V_{cc}-v_o) f_u(x) \quad (2)$$

$$\frac{dx}{dt} = \frac{V_{cc}}{t_r} u(v_i - v_{\rm th}) u(V_{cc}-x) - \frac{-V_{cc}}{t_f} u(v_{\rm th}-v_i) u(x) \quad (3)$$

In the above equations, $f_u(x) = [(|x| + x)/2V_{cc}]^2$, $f_d(x) = f_u(V_{cc} - x)$, $v_{\rm th}$ is the threshold for the controlling voltage v_i, $u(\cdot)$ is the ideal step function and a non inverting relation v_i–v_o is assumed.

In eq. (2) x is a control parameter, playing the role of the gate voltage v_{gate} of the two MOS transistors. Functions $i_d(v_o)f_d(v_{gate})$ and $i_u(V_{cc} - v_o)f_u(v_{gate})$ can be considered as rough approximations of the output static characteristic surfaces of the two MOS transistors $i_d(v_o, v_{gate})$ and $i_u(V_{cc}-v_o, v_{gate})$, respectively. In this way, the characteristic specified by eq. (2) is a rough approximation of the output static characteristic surface of the two complementary transistors. As the x parameter is varied, a continuous variation of $\bar{i}(v_o)$ between $i_d(v_o)$ and $i_u(V_{cc}-v_o)$ occurs, which mimics the actual variation of the output characteristic of the couple of complementary MOS transistors during a state transition. Owing to this property, we name the proposed IBIS model Gradual Switching (GS) model.

The state eq. (3) controls the velocity of state transitions. Such an equation has two equilibrium solutions $x = 0$ and $x = V_{cc}$. If $x = 0$, when v_i grows above $v_{\rm th}$, $x(t)$ starts a linear ramp from 0 to V_{cc} completed in a time t_r. Whereas, if $x = V_{cc}$, when v_i decreases below $v_{\rm th}$, $x(t)$ starts a linear ramp from V_{cc} to 0 completed in a time t_f. The slopes of such ramps, V_{cc}/t_r and $-V_{cc}/t_f$, match IBIS data (1.3). Each ramp of $x(t)$ produces a rising or falling edge in the output voltage $v_o(t)$, whose total duration is either t_r or t_f and whose shape is decided by the x–v_o relation (2) and is of sigmoid type. Though such edges are not linear, as required by IBIS, owing to the nature of the model, which mimics transitions of actual devices, they are likely to be (or to be made by parameter tuning) more accurate than purely linear ones. Finally, it is ought to remark that the model can be easily extended to include more than one threshold.

4. Model accuracy

In order to validate and test our IBIS model we compare its response to the responses of an accurate Spice transistor level model and of a commercial IBIS model. The commercial IBIS model involved in the comparison is for Spice based simulators and uses an abrupt switching of the pull-up and pull-down characteristics to describe logic state transitions. To satisfy IBIS specifications, the model uses a control mechanism producing linear variations of the output voltage during state transitions. Owing to its principle of operation, we indicate the commercial model as the Instantaneous Switching (IS) model.

The Device Under Test (DUT) for the comparison is a CMOS output buffer composed of four couples of 1.2 μm complementary MOS transistors with growing areas designed to minimize the circuit delay. The DUT is accurately modeled by a Spice transistor level model (the reference model of the comparisons) based on Spice Level 2 models of MOS transistors. The reference model and the IBIS specification are then used to build an IBIS data set describing the DUT output port and such a data set is used to feed both the GS and the IS IBIS models.

We check the two IBIS models by using them to compute the responses of different test circuits obtained by connecting the DUT to test loads, and by comparing the computed responses with the responses of the reference model. Our GS model is implemented as a Spice subcircuit and all computations are carried out by Spice.

In such comparisons, the accuracy level of the two IBIS models is less than expected, because even the simple DUT chosen leads to waveforms with scarcely linear edge shapes. The GS model, however, is always significantly more accurate than the IS model, more efficient and, most important, free of integration problems. The IS model, instead, shows convergence problems and for some of the test circuits Spice was not able to compute its responses. Concerning efficiency, for the simple test circuits used, the GS and IS model run times are about 1/3 and 1/6 of the run time of the reference model, respectively.

As an example, we show the comparison for the test circuit formed by the DUT loaded by a 50 Ω resistor and a shunt 5 pF capacitor. Such a load exceeds the driving capabilities of the DUT and it is used to check the behavior of IBIS models outside their validity range. Figure 2 shows the output voltage waveforms computed for this circuit by the three models when a logic HIGH pulse lasting 8 ns is applied by the DUT. In this test, the GS model still yields an acceptable approximation of the edge slopes and of the first corners of edges, and a rough approximations of the second corners of edges. The IS model, instead, misses every corner and, even worse for SI applications, completely misses the slope of the falling edge and adds spurious ringings on its second corner. Ringing effects added by the IS models were observed in many other test cases and a relation of such ringings with the switching mechanism of the model is suspected.

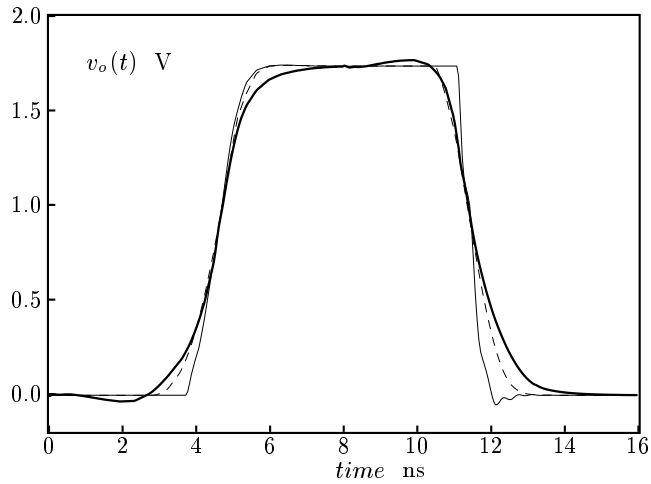

Figure 2: *Voltage waveforms $v_o(t)$ computed by the three models under comparison for the DUT loaded by a 50 Ω resistor and a 5 pF capacitor. Solid thick line: reference curve; dashed line: response of the GS model; solid thin line: response of the IS model.*

5. Conclusions

In this paper, we propose a behavioral model of CMOS digital gates based on IBIS data. The tests carried out remark that a careful design of the switching between logic states is required to avoid significant loss of accuracy as well as low efficiency and stability problems. Our model describes the change of logic state by a gradual switching of the output characteristics and it offers improved accuracy and efficiency, that could be effectively exploited in SI simulations. The study, however, highlights also some limitation of IBIS models, that should be further enquired.

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Paper VI

E8: Radiation from and coupling to PCBs

Behavioral Models of Digital Devices and their Impact on Signal Integrity

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Introduction

In this paper, we address the behavioral modeling of digital integrated circuits (ICs) on the basis of the Input/output Buffer Information Specification (IBIS). The use of behavioral models of digital ICs concerns an effective approach to the Signal Integrity (SI) simulations of large and critical circuits and the IBIS standard is becoming a key resource of such an approach.

IBIS data files can easily describe complex ICs with thousands of pins and their use is strongly encouraged by IC manufacturers, who can distribute the relevant characteristics of their devices without disclosing proprietary information. In order to be used for SI simulations, IBIS behavioral data must be translated into a suitable set of characteristic equations, *i.e.,* into an executable behavioral model. IBIS models (*i.e.,* executable models based on IBIS data) can be obtained as built-in features in most EDA software tools for SI simulations or they can be designed and built by the final user. The latter task, however, is not trivial, because the design of executable models is beyond the scope of IBIS (*e.g.,* see [1]). The aim of this work is to provide guidelines to build IBIS models, which are not provided by IBIS, and to propose an effective IBIS model for CMOS devices.

IBIS models of CMOS devices

Starting from the specification, we have developed a formal description of IBIS models for CMOS devices. Such a description highlights that the key element of CMOS IBIS models is the controlled nonlinear resistor providing both the output static characteristics for the two logic states and the proper output voltage waveforms during state transitions. In our model, such a resistor performs a gradual replacement of the pull-up and pull-down characteristics, in order to mimic the behavior of the actual device.

We validate the proposed IBIS model by comparing its response for different test loads to the responses of an accurate Spice transistor level model and of a commercial IBIS model for Spice simulators. The tests performed point out that the proposed model is always more efficient, stable and significantly more accurate than the commercial one and could be effectively exploited in SI simulations. Besides the comparisons highlights that the switching between logic states is a critical point of IBIS models and that it can cause loss of accuracy as well as reduced efficiency and stability problems.

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Paper VII

Behavioral modeling of digital devices via Black-Box identification

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1 Introduction

The numerical simulation of signals sent on interconnects (cable wires, PCB and MCM lands) requires effective models of the integrated circuit (IC) ports driving and loading the interconnects. Such models must allow the simulation of large realistic problems and must perform at an accuracy level useful for the prediction of Signal Integrity (SI) effects.

Presently, behavioral models are establishing as the most effective description of digital IC ports for SI simulations. A behavioral model of a device is a set of port characteristic equations (or the equivalent circuit of such equations) obtained from external (possibly virtual) measurements. Behavioral models have the required numerical efficiency and, when properly used, yield responses close to the response of the detailed transistor-level models of the ICs. The most common approach to behavioral modeling is via simplified equivalent circuits of the IC ports, because they facilitate the identification of the model parameters (by virtual measurements) and the implementation of the models. An important example of the equivalent circuit approach to behavioral modeling is the widely adopted Input/output Buffer Information Specification (IBIS). IBIS offers high numerical efficiency, large data library and commercial software tools handling models and complex modeling problems. However, the equivalent circuit approach to behavioral modeling has also inherent limitations. Mainly the identification of model parameters is easy only by virtual measurements, *i.e.,* from transistor-level models of the devices, and the physical effects taken into account by the model are decided a priori, when the equivalent circuit defining the model is selected. In order avoid such limitations, in this work we explore the modeling of digital IC via Black-Box (BB) identification. Such an approach amounts to the identification of a suitable nonlinear dynamic parametric model of the IC ports from measured transient waveforms. It should enable easier model identification from actual measurements, as it requires only the knowledge of input and output data. Furthermore, since the model structure is selected by the identification process itself, BB models automatically take into account all the physical effects relating input and output data.

2 Radial Basis Function models

We base our BB modeling approach on discrete-time Radial Basis Function (RBF) Input/Output (I/O) dynamic models defined by

$$\begin{aligned} &y(k) = \textstyle\sum_{i=1}^{p} \theta_i \Phi(\|\mathbf{x} - \mathbf{c}_i\|) \\ &\mathbf{x}^T = [\mathbf{u}^T(k), \ldots, \mathbf{u}^T(k-r), y(k-1), \ldots, y(k-r)] \\ &\Phi(v) = \exp(-v^2/\beta^2) \\ &\mathbf{\Theta}^T = [\theta_1, \ldots, c_1, \ldots, \beta] \end{aligned} \tag{1}$$

where $y(k)$ is the output sequence of the model, $\mathbf{u}(k)$ is the vector of input sequences (each component is the sequence of an input variable), $\mathbf{\Theta}$ is the vector of unknown parameters, r is the dynamic order of the model, $\|\cdot\|$ denotes the Euclidean norm, p is the number of basis functions Φ, $\mathbf{c}_i$ are the centers of the basis functions and β is a scalar constant value.

The above equation can be used to model the relation between the inputs and an output of most nonlinear dynamic systems with fading memory (*e.g.,* see [1]). As an example, if we consider a nonlinear dynamic two-port element controlled by its port voltages $v_1(k)$ and $v_2(k)$, we could model its output current by setting $y(k) = i_2(k)$ and $\mathbf{u}^T(k) = [v_1(k), v_2(k)]$ into (1). To build the model, we have to identify the values of the parameters in $\mathbf{\Theta}$ that best relate the available input samples to the output ones. RBF models can be identified by particularly effective algorithms, that work well even for problems with many input variables and strongly nonlinear nature. We use the algorithm of [2] organized as follows. In (1), $\mathbf{x}(k)$ and $\mathbf{c}_i$ are elements of $\Re^m$, with $m = n_i \times (r+1) + r$ and n_i the number of input variables. As k varies, the available I/O data define a set of vectors $\mathbf{x}(k)$ that is represented by a cloud of points in $\Re^m$. The first step is to set β to the maximum size of such a cloud of identification points. Then for $p = 1, 2, 3, \ldots$ steps *(i)* and *(ii)* are repeated
(i) a new model is built by adding a basis function to the $p-1$ *model; the center of the function is the identification point* $\mathbf{x}(k)$ *minimizing the mean square error of the new model*
(ii) the statistical significance of the new model is assessed by suitable indexes
The selection of the centers is facilitated by the orthogonalization of the time sequences and the process is terminated when the most significant model is reached. Eventually, the final model is approximated by a continuous-time state-space model, to ease its implementation in circuit simulators.

3 Models of IC output ports

The problem at hand amounts to the BB modeling of an output port of digital IC, the modeling of an input port being a simpler subcase.

Output ports of digital integrated circuits, for any kind of technology/architecture, are buffer circuits composed of cascaded stages with growing driving capabilities. Such circuits are needed to drive heavy offchip loads (as the offchip interconnects are) while limiting the increase of the delays and of the rise/fall times of the output signals. In order to study this problem, we focus on the four stage CMOS buffer shown in Fig. 1, where v_i denotes the input voltage (*i.e.,* the output of the integrated fast digital circuit), v_o, i_o the buffer output voltage and current, respectively, and $V_{\rm dd}$, $V_{\rm ss}$ the power supplier voltages.

We look for a behavioral model of the form (1) for the output port of the circuit of Fig. 1, assuming, without loss of generality, constant supply voltages. For this purpose, we could associate the output current i_o to the output variable y, and the input and output voltages v_i and v_o, respectively, to the input variables in $\mathbf{u}$. In this problem, however, since neither v_i nor other possible buffer inputs are measurable quantities, model (1) cannot be identified from measurements. In order to overcome this difficulty, we developed simplified RBF models that approximate (1) and can be identified just from v_o and i_o waveforms. Such models hold only for logic state transitions spaced enough in time, so that every transition starts

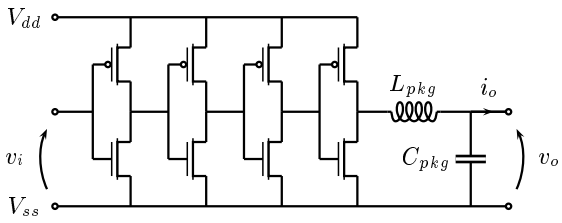

Figure 1: *Four stage CMOS output buffer.*

from steady state conditions, however they have interesting features. Their identification is easy and, even with a few basis function (*e.g.*, $p \in [5, 20]$), their accuracy is good and fairly independent of the load they drive. Such features stem from the properties of the cascaded invert stages and of the RBFs.

As an example, we briefly describe the modeling of the circuit of Fig. 1 via our simplified RBF models. The parameter values used for this example are those reported at pag. 293 of [3], that are representative of output buffers composed of 1.2 μm CMOS inverter stages. In order to simulate the measurement of v_o and i_o waveforms, we describe the circuit of Fig. 1 by a detailed Spice transistor-level model and compute its responses for suitable loads. The sampled data needed for the identification are obtained by sampling the computed waveforms at $T_s = 100$ ps rate.

The identification setup of this example is composed of the transistor-level model driving a series connection of a 100 Ω resistor and an ideal voltage source generating a suitable input identification waveform. Such a setup approximately describes the port under modeling connected to a real signal source with a 100 Ω internal impedance. In a practical measurement setup, a transmission line with known characteristics could be inserted between the port and the signal source, to facilitate the measurement of i_o.

The selection of input identification waveforms is a critical point of any nonlinear identification problem. We obtained effective identification by simple v_o waveforms, composed of a few steps spanning the range of output operating voltages with edges rising/falling at rate close to the port switching rate. An example of such (applied) voltage and (computed) current waveforms is shown in Fig. 2.

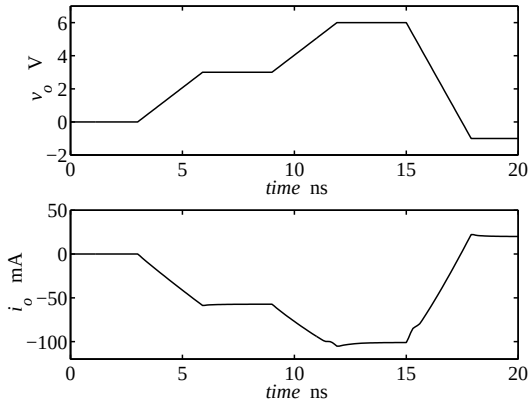

Figure 2: *Signals $v_o(t)$ and $i_o(t)$ used for model identification.*

Fig. 3 shows some responses of a simplified RBF model built as outlined above against the corresponding (reference) responses of the Spice transistor-level model. The responses are produced by a LOW to HIGH transition followed by a

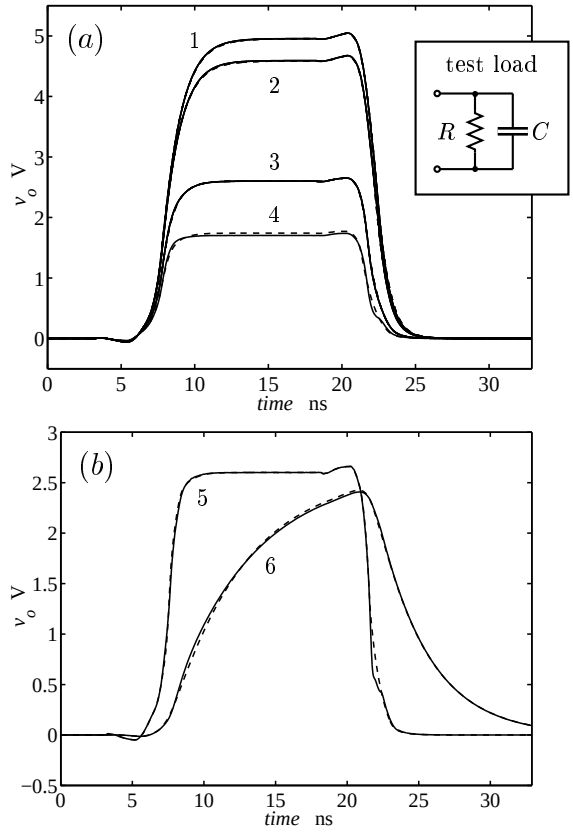

Figure 3: *Output voltage waveforms of the example buffer circuit for different test loads. Dashed lines: reference curves; solid lines: responses of a smiplified RBF model. Curves 1,2,3,4,5 and 6 hold for ($C = 10\,pF, R = 10^4\,\Omega$), ($C = 10\,pF, R = 10^3\,\Omega$), ($C = 10\,pF, R = 10^2\,\Omega$), ($C = 10\,pF, R = 50\,\Omega$), ($C = 0$, $R = 100\,\Omega$) and ($C = 100\,pF$, $R = 100\,\Omega$) respectively.*

HIGH to LOW transition when different test load are driven. Fig. 3a refers to mainly resistive loads, whereas Fig. 3b refers to a purely resistive and to a strongly capacitive loads. The accuracy of the model and its insensitivity to the driven load can be clearly appreciated.

In summary, we study a modeling approach for digital ICs, which is based on the identification of a simplified RBF model from measured transient waveforms at the device ports. We perform numerical experiments within the framework of an idealized identification setup and obtain simple models performing at a good accuracy level for remarkably different loads.

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Paper VIII

Modélisation des circuits intégrés digitaux pour la simulation CEM

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Résumé

On traite la modélisation des dispositifs logiques intégrés pour la simulation numérique des effets CEM dans les circuits digitaux rapides. Le but de ce travail, c'est la caractérisation des portes des circuits intégrés digitaux (peu documentés) à travers des mesures standards entrée/sortie de formes d'onde en transitoire. On suit une approche de modélisation basée sur l'identification de type boîte noire des modèles paramétriques dynamiques non-linéaires, à travers les données d'entrée/sortie.

1. Introduction

La simulation numérique de signaux transmis sur interconnexions (câbles, pistes de PCBs et de MCMs) exige des modèles efficaces des portes des circuits intégrés, qui pilotent ou qui chargent les interconnexions. Ces modèles doivent permettre la simulation de problèmes réalistes de grandes dimensions et doivent avoir une précision utile à la prédiction des effets d'intégrité des signaux (IS).

Une ressource largement utilisée pour une de ces tâches de modélisation est IBIS (Input/output Buffer Information Specification). Les modèles basés sur IBIS sont définis par des circuits équivalents et offrent une efficacité numérique élevée avec un bon niveau de précision. De plus, à cause de la diffusion de IBIS, de larges bases de données sont disponibles, ainsi que des logiciels commerciaux traitant ces modèles-là et les problèmes de modélisation complexes. Cependant, les modèles IBIS ont aussi des limites. En particulier, l'identification des données IBIS se fait simplement seulement à travers les mesures virtuelles, c'est-à-dire à partir des modèles des dispositifs à niveau de transistors, et les effets physiques considérés par le modèle sont décidés a priori, lorsque le circuit équivalent qui définit le modèle est sélectionné.

Dans cet article, on traite de la modélisation comportementale des buffers de sortie des circuits intégrés digitaux, effectuée à travers l'identification de type boîte noire. Une telle approche consiste en l'identification d'un modèle paramétrique dynamique non-linéaire à temps discret, à travers les formes d'onde qui peuvent être mesurées sur la sortie du buffer. Les modèles paramétriques offrent la même précision des modèles IBIS, mais ils sont plus faciles à identifier à partir de mesures réelles, car ils exigent seulement la connaissance des données d'entrée et de sortie. En outre, puisque la structure du modèle est sélectionnée par le même processus d'identification, les modèles paramétriques comprennent automatiquement tous les effets physiques reliés aux données d'entrée et de sortie. Ils permettent de modéliser facilement les échantillons de dispositifs pour lesquelles les données IBIS ne sont pas fournis et également de simuler des structures d'interconnexion critiques pour évaluer les effets CEM sensibles.

2. Modèles RBF

L'approche de modélisation de type boîte noire suivie est basée sur le modèle entrée/sortie dynamique RBF (Radial Basis Function) défini par

$$\begin{aligned} &y(k) = \textstyle\sum_{i=1}^{p} \theta_i \Phi(\|\mathbf{x} - \mathbf{c}_i\|) \\ &\mathbf{x}^T = [\mathbf{u}^T(k), \ldots, \mathbf{u}^T(k-r), y(k-1), \ldots, y(k-r)] \\ &\Phi(v) = \exp(-v^2/\beta^2) \\ &\mathbf{\Theta}^T = [\theta_1, \ldots, \mathbf{c}_1^T, \ldots, \beta] \end{aligned} \tag{1}$$

où $y(k)$ est la séquence de sortie du modèle, $\mathbf{u}(k)$ est le vecteur des séquences d'entrée (chaque composante est la séquence d'une variable d'entrée), $\mathbf{\Theta}$ est le vecteur des paramètres inconnus, r est l'ordre dynamique du modèle, $\|\cdot\|$ dénote la norme Euclidienne, p est le nombre des fonctions base Φ, $\mathbf{c}_i$ sont les centres des fonctions base et β une valeur scalaire constante.

L'équation ci-dessus peut être utilisée pour modéliser la relation entre les entrées et une sortie de la plus grande partie des systèmes dynamiques non-linéaires avec mémoire évanescente (voir [1]). Par exemple, si on considère un élément dynamique non-linéaire à deux portes contrôlé par ses tensions aux portes $v_1(k)$ et $v_2(k)$, on peut modéliser son courant de sortie en posant $y(k) = i_2(k)$ et $\mathbf{u}^T(k) = [v_1(k), v_2(k)]$ dans (1). Pour construire le modèle, on doit identifier les valeurs des paramètres dans $\mathbf{\Theta}$ qui mieux relient les échantillons disponibles d'entrée avec celles de sortie. Les modèles RBF peuvent être identifiés par algorithmes particulièrement efficaces, qui fonctionnent bien même sur des problèmes avec beaucoup de variables d'entrée et avec nature fort non-linéaire.

3. Modèles de portes de sortie des circuits intégrés

Le problème en question consiste en la modélisation de type boîte noire d'une porte de sortie d'un circuit intégré digital ; la modélisation d'une porte d'entrée est un cas particulier plus simple.

Les portes de sortie des circuits intégrés digitaux, pour n'importe quel type de technologie / architecture, sont des circuits buffers composés d'étages en cascade avec capacité de pilotage croissante. Ces circuits sont nécessaires pour piloter des charges de valeur élevée externes au circuit intégré (comme les interconnexions externes au circuit intégré) et, en même temps, pour limiter les retards et les temps de transition des signaux de sortie. Afin d'étudier ce problème, on considère le buffer CMOS à quatre étages représenté dans la Fig. 1, où v_i dénote la tension d'entrée (c'est-à-dire, la sortie du circuit intégré digital rapide), v_o, i_o, respectivement, la tension et le courant de sortie du buffer et $V_{\rm dd}$, $V_{\rm ss}$ les tensions d'alimentation.

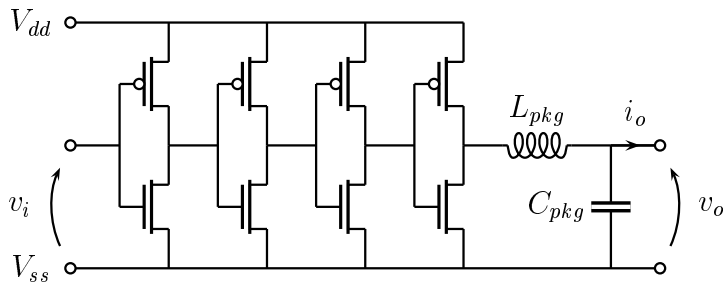

Figure 1 : *Buffer de sortie CMOS à quatre étages.*

On cherche un modèle comportemental de la forme (1) pour la porte de sortie du circuit de Fig. 1, en considérant les tensions d'alimentation constantes. A ce but, on peut associer le courant de sortie

i_o à la variable de sortie y, et respectivement les tensions d'entrée et de sortie v_i et v_o aux variables d'entrée en $\mathbf{u}$. Dans ce problème, toutefois, comme ni v_i ni d'autres entrées possibles du buffer sont quantités mesurables, le modèle (1) ne peut pas être identifié par des mesures. Cependant, en utilisant les propriétés des étages en cascade et des modèles RBF, on trouve qu'on peut utiliser le modèle simplifié à deux pièces qui suit.

$$\begin{aligned} y(k) &= w_1(k)y_1(k) + w_2(k)y_2(k) \\ y_1(k) &= \sum_n \theta_n \Phi(\|\mathbf{x}_2 - \mathbf{c}_{2n}\|) \\ y_2(k) &= \sum_m \theta_m \Phi(\|\mathbf{x}_2 - \mathbf{c}_{2m}\|) \\ \mathbf{x}_2^T(k) &= [u_2(k), \ldots, u_2(k-r), y(k-1), \ldots, y(k-r)] \end{aligned} \tag{2}$$

Dans l'équation ci-dessus, y_1 et y_2 sont des sous-modèles RBF qui decrivent la porte de sortie lorsqu'elle est posée respectivement à l'état logique dénommé "bas" (LOW) et "haut" (HIGH), le vecteur $\mathbf{x}_2$ contient les échantillons pour le temps précédent de la variable de sortie $i_o(t)$ et ceux des instants présents et précédents de la seule variable d'entrée $v_o(t)$ (en fait, $v_i(t)$ n'est pas une variable d'entrée des sous-modèles), $w_1(t)$ et $w_2(t)$ sont les coefficients de poids à temps variable qui tiennent en compte l'évolution de la variable d'entrée $v_i(t)$ et qui agissent comme interrupteurs entre les sous-modèles $y_1(t)$ et $y_2(t)$. Ce modèle est valide seulement pour des transitions d'état logique suffisamment distantes dans le temps, de façon que chaque transition débute d'une condition d'équilibre. Il a cependant des caractéristiques intéressantes : son identification est facile et, même avec peu de fonctions base ($p \in [5, 20]$), sa précision est bonne et presque indépendante de la charge qu'il pilote. Ces caractéristiques dérivent des propriétés des étages d'inverseurs en cascade et des modèles RBF.

Les tâches suivies pour identifier le modèle (2) à partir des données d'entrée/sortie mesurées sont :

1. identification des sous-modèles RBF y_1 et y_2;
2. évaluation des coefficients de poids $w_1(k)$ et $w_2(k)$.

La méthode utilisée pour identifier les sous-modèles RBF est l' *"orthogonal least squares learning algorithm"*, qui est une méthode efficace généralement citée dans la littérature [2]. Les coefficients de poids à temps variable $w_1(k)$ et $w_2(k)$ sont calculés à partir des formes d'onde connues v_o et i_o par inversion linéaire de (2).

Enfin, comme le modèle décrit par (2) doit opérer efficacement dans des logiciels de simulation des circuits, il est remplacé par un modèle approximé à équations d'état à temps continu et réalisé dans SPICE. Ceci s'obtient en réintroduisant la variable temps dans (2) ($t = kT$, où T est la période de découpage utilisé pour découper les formes d'onde d'entrée et de sortie) et en remplaçant l'opérateur différence avec l'opérateur différentiel (par exemple, $\dot{z}(t) \simeq \frac{1}{T}[z(kT) - z(kT - T)]$). Le modèle à équations d'état à temps continu obtenu est donc réalisé dans le logiciel SPICE, en utilisant des composants standards, tels que capacités, résistances et générateurs. La Fig. 2 illustre un exemple de réalisation dans SPICE du modèle RBF à deux pièces (2).

4. Exemple numérique

Dans cette section on décrit brièvement la modélisation du circuit de Fig. 1 à travers le modèle RBF à deux pièces développé. Les valeurs des paramètres utilisés dans cet exemple sont celles figurant à page 293 de [3] ; elles sont représentatives des buffers de sortie composés d'étages inverseurs CMOS de 1.2 μm. Afin de simuler la mesure des formes d'onde v_0 et i_0, on décrit le circuit de Fig. 1 par un modèle SPICE détaillé à niveau des transistors et on calcule ses réponses pour des charges appropriées. Les données découpées nécessaires pour l'identification sont obtenus en découpant les formes d'onde calculées avec une période $T = 100ps$.

```
.subckt bufRBF w1 w2 u
 Ef1 f1 0 value={
 + 1 + {theta1}*
 + EXP(-(PWR(V(u)-{c11},2) +
 + PWR(V(x1)-{c12},2)) / PWR({beta1},2) ) +
 ...
 * output controlled current source
 Gy 0 u value={V(y1)}
 ...
.ends
```

Figure 2 : *Exemple de réalisation dans SPICE du modèle RBF à deux pièces (2).*

La configuration pour l'identification est composée du buffer qui pilote une résistance de 150 Ω en série à un générateur idéal de tension, qui engendre une forme d'onde d'entrée appropriée à l'identification. Ce circuit décrit de façon approximative une source de signal réelle avec impédance interne de 50 Ω, liée à la porte à modéliser par une résistance série de 100 Ω, qui facilite la mesure de i_o.

La sélection des formes d'onde d'entrée pour l'identification est un point critique de tous les problèmes d'identification non-linéaires. On a obtenu une identification efficace à partir des simples formes d'onde v_o à différents niveaux, avec fronts de montée/descente comparables avec les transitions d'état de la porte. Un exemple de formes d'onde v_o (appliquée) et i_o (calculée) est représenté dans la Fig. 3.

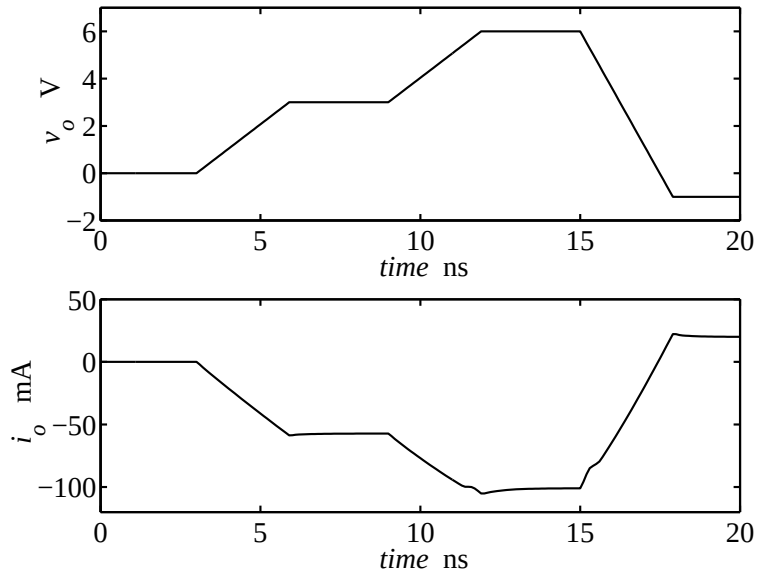

Figure 3 : *Signaux $v_o(t)$ et $i_o(t)$ utilisés pour l'identification du modèle.*

La Fig. 4 compare les réponses du modèle RBF dévelopé avec celles de référence du modèle SPICE à niveau transistor, pour le buffer de Fig. 1. Les réponses sont dues à deux transitions d'état du buffer, lorsqu'il pilote de différentes charges d'essai. Les courbes représentées montrent la précision du modèle développé et son indépendance de la charge pilotée.

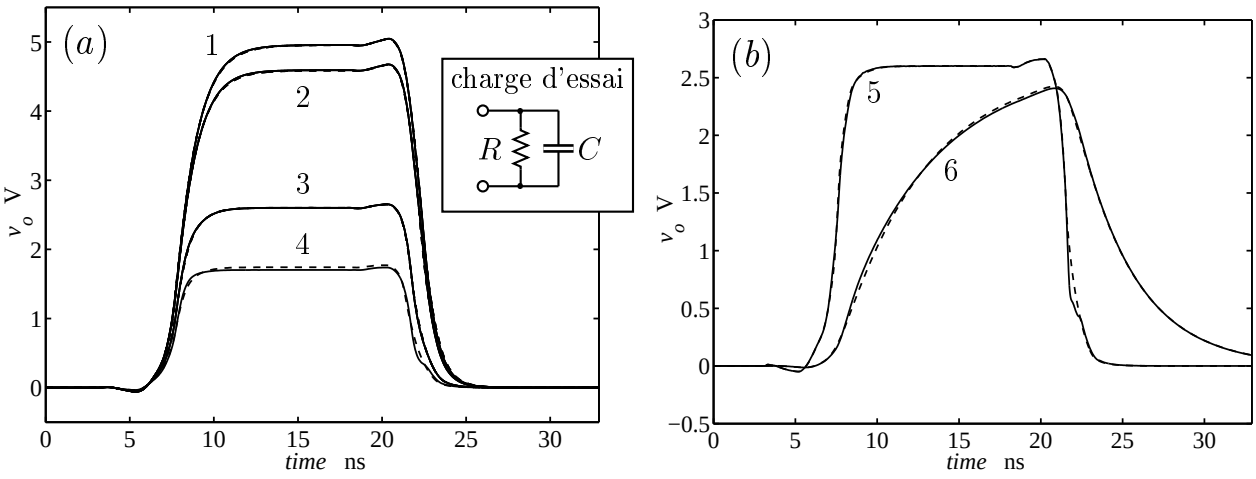

Figure 4 : *Formes d'onde de tension de sortie du buffer pour des différentes charges d'essaí. Lignes hachurées : courbes de référence ; lignes continues : réponses du modèle RBF simplifié. Les courbes 1 à 6 sont obtenues respectivement avec* ($C = 10\,pF, R = 10^4\,\Omega$), ($C = 10\,pF, R = 10^3\,\Omega$), ($C = 10\,pF, R = 10^2\,\Omega$), ($C = 10\,pF, R = 50\,\Omega$), ($C = 0$, $R = 100\,\Omega$) *et* ($C = 100\,pF$, $R = 100\,\Omega$).

5. Conclusion

Dans cet article on étudie une approche de modélisation pour des circuits intégrés digitaux, qui est basée sur l'identification de type boîte noire d'un modèle simplifié RBF. Cette approche se fonde sur les mesures de formes d'onde en transitoire aux portes du dispositif et automatiquement tient en compte tous les effets physiques significatifs relatifs aux signaux. On effectue des essais numériques dans le cadre d'une configuration idéalisée pour l'identification et, par la suite, on obtient de simples modèles performants à un bon niveau de précision pour des charges ayant une large gamme de valeurs.

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Paper IX

BLACK-BOX IDENTIFICATION OF DIGITAL DEVICES FOR RADIATION PREDICTIONS

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Abstract We address the modeling of logical integrated devices for the numerical simulation of EMC effects in fast digital circuits. The aim of this work is the characterization of the ports of (poorly documented) digital integrated circuits from standard input/output transient measurements. We follow a modeling approach based on the black-box identification of parametric nonlinear dynamic models from input/output data. Our models are defined by Radial Basis Functions, and their identification is simple and effective. The model structure is selected during the identification, which automatically takes into account all the significant physical effects relating the output signals to input ones. The proposed modeling process is described in detail and its feasibility is demonstrated on a real device.

I. INTRODUCTION

Nowadays the assessment of Signal Integrity (SI) and ElectroMagnetic Compatibility (EMC) effects in fast digital circuits at the design stage is of paramount importance. Such an assessment is mainly carried out by simulating the evolution of the signals sent on interconnects (cable wires, PCB and MCM lands) by digital Integrated Circuits (ICs). This requires efficient and accurate numerical models of the IC ports driving and loading the interconnects. The required models must allow the simulation of large realistic problems and must perform at an accuracy level useful to the prediction of sensitive effects, like the radiation from PCB lands.

A widely used resource for such a modeling task is the Input/output Buffer Information Specification (IBIS). Models based on IBIS are defined by equivalent circuits and offer high numerical efficiency at a good accuracy level. Besides, owing to the diffusion of IBIS, large data libraries as well as commercial software tools handling models and complex modeling problems are available. However IBIS models have also some limitations. Mainly, since they are based on equivalent circuits, the identification of IBIS data is easy only by virtual measurements (*i.e.,* from transistor-level models of the devices) and the physical effects taken into account by the model are decided a priori, when the equivalent circuit defining the model is selected.

In this contribution, we address the behavioral modeling of digital IC output buffers via Black-Box (BB) identification. Such an approach amounts to the identification of a suitable discrete-time nonlinear dynamic parametric model from the waveforms that can be measured at buffer output. Parametric models offer the same accuracy of IBIS models, yet they are easier to identify from actual measurements, as they require only the knowledge of input and output data. Furthermore, since the model structure is selected by the identification process itself, parametric models automatically take into account all the physical effects relating input and output data. They would enable any user to easily model sample devices for which IBIS data are not provided and to simulate critical interconnect structure to assess sensitive EMC effects.

II. RBF MODELS

We base our BB modeling approach on discrete-time Radial Basis Function (RBF) input/output nonlinear dynamic models defined by

$$\begin{aligned} & y(k) = \textstyle\sum_{j=1}^{p} \theta_j \Phi(|\mathbf{x} - \mathbf{c}_j|, \beta) \\ & \mathbf{x}^T = [y(k-1), \ldots, y(k-r), \\ & \qquad \mathbf{u}^T(k), \ldots, \mathbf{u}^T(k-r)] \\ & \Phi(\xi, \beta) = \exp(-\xi^2/\beta^2) \\ & \boldsymbol{\Theta}^T = [\theta_1, \ldots, \mathbf{c}_1, \ldots, \beta] \end{aligned} \qquad (1)$$

where $y(k)$ is the output sequence of the model and $\mathbf{u}(k)$ is the vector of input sequences (each component is the sequence of an input variable). The vector of regressors $\mathbf{x}$ collects the present samples of the inputs and previous r samples of the inputs and of the output, r being the dynamic order of the model, whereas vector $\boldsymbol{\Theta}$ collects the unknown parameters of the model. The present output of the model $y(k)$ is a linear combination of the p basis functions $\Phi(|\mathbf{x} - \mathbf{c}_j|, \beta)$, where Φ is a scalar asymptotically vanishing function generating all the basis functions. Each basis function is defined by its position in the space of regressors (center $\mathbf{c}_j$) and its spreading (scale parameter β) [1].

The above equation can be used to model the relation between the inputs and an output of most nonlinear dynamic systems with fading memory (*e.g.,* see [4]). As an example, if we consider a nonlinear dynamic two-port element controlled by its port voltages $v_1(k)$ and $v_2(k)$, we could model its output current by setting $y(k) = i_2(k)$ and $\mathbf{u}^T(k) = [v_1(k), v_2(k)]$ into (1).

To build the model, we have to identify the values of the parameters in $\mathbf{\Theta}$ that best relate the available input samples to the output ones. RBF models can be identified by particularly effective algorithms, that work well even for problems with many input variables and strongly nonlinear nature. Such a feature is a consequence of the ability of asymptotically vanishing functions to fit complex surfaces.

III. MODELS OF IC OUTPUT PORTS

The problem at hand amounts to the modeling of an output port of a digital IC via (1), the modeling of an input port being a simpler subcase. Output ports of digital integrated circuits, for any kind of technology/architecture, are buffer circuits composed of cascaded stages with growing driving capabilities. Such circuits provide the interface between the fast low-energy internal parts of ICs and the off-chip interconnects, that require higher energy signals. Output buffers, therefore, must increase the power of transmitted signals limiting as much as possible the added delay and the increase of the rise/fall times. The structure of a generic output buffer is shown in Fig. 1, where $\bar{v}$ denotes the buffer input voltage (*i.e.,* the output of the functional part of the integrated fast digital circuit), and v and i the buffer voltage and current at the output pin, respectively.

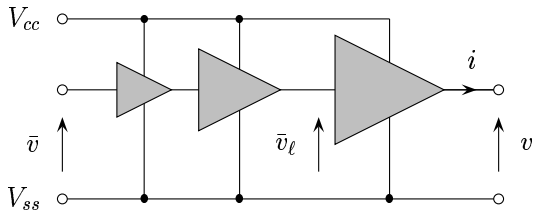

Figure 1: Generic multistage output buffer and its relevant electric variables.

We could look for a behavioral model of the form (1) for the output port of the circuit of Fig. 1 by using i as output variable (*i.e.,* $y = i$), and the input and output voltages $\bar{v}$ and v, respectively, as input variables (*i.e.,* $\mathbf{u}^T = [\bar{v}, v]$). Such a model, however, could not be identified from measured transient waveforms, because neither $\bar{v}$ nor other possible buffer inputs are accessible.

In order to overcome this difficulty, we develop a simplified 2-piece RBF model that approximates (1) and can be identified just from v and i waveforms. It stems from the properties of cascaded inverter stages and of the RBFs generated by the exponential function, as shown in Appendix, and inherits most of the strengths of the complete RBF model (1). Its identification is easy and, even with a few basis functions (*e.g.,* $p \in [5, 20]$), the identified models track accurately the behavior of most output buffer circuits. Furthermore, since the complete RBF model (1) holds for arbitrary loads, the accuracy of the simplified model turns out to be fairly insensitive to the loads it drives. The equation defining the simplified model writes

$$\begin{aligned} i(k) &= w_1(k) f_1(\mathbf{\Theta}_1, \mathbf{x}(k)) + w_2(k) f_2(\mathbf{\Theta}_2, \mathbf{x}(k)) \\ f_n(\mathbf{\Theta}_n, \mathbf{x}(k)) &= \sum_j \theta_{nj} \exp\{-|\mathbf{x} - \mathbf{c}_{nj}|^2/\beta^2\}, \\ & \qquad\qquad n = 1, 2 \\ \mathbf{x}^T(k) &= [i(k-1), \ldots, i(k-r), \\ & \quad v(k), v(k-1), \ldots, v(k-r)] \end{aligned} \tag{2}$$

where f_1 and f_2 are RBF submodels that describe the output port for constant inputs forcing its logic state to the LOW and HIGH values, respectively, ($\bar{v}$ is not an input variable of the submodels), and $w_1(k)$ and $w_2(k)$ are time varying weight coefficients that take into account the evolution of the input variable $\bar{v}$ and act as switches between submodels f_1 and f_2. Each weight coefficient w_n is formed by piping two basic sequences $w_n^u(k)$ and $w_n^d(k)$, that describe the "up" and the "down" transition, respectively. The sequences of the two transitions occur in alternate order and are issued synchronously with the changes of the input controlling the modeled port. Of course, such a simplified model holds only for logic state transitions spaced enough in time, so that every new transition starts after the previous one has been completed. However, since the above validity condition is satisfied in properly working digital circuits, it does not limit the use of the model in EMC simulation problems.

IV. MODELING PROCESS

The modeling of an IC port via the proposed approach can be divided into three parts: (1) the excitation and recording of transient responses of the buffer under modeling, (2) the identification of the model parameters $\mathbf{\Theta}_n$ and w_n, $n = 1, 2$, from the recorded transient responses, and (3) the implementation of the obtained model in a standard circuit simulation environment (*e.g.,* Spice).

Part (1) amounts to drive the buffer under modeling to obtain transient output signals carrying the information on the buffer behavior. The excitation and response signals involved in this step are named *iden-*

tification signals. In our problem, we need two sets of identification signals: the steady state identification signals, for submodels f_1 and f_2, and the switching identification signals, for the weight coefficients w_1 and w_2.

Submodels f_1 and f_2 yield the current response $i(t)$ caused by $v(t)$ at fixed logic state. The steady state identification signals, therefore, are composed of a driving voltage waveform applied to the port (submodel input variable) and of its corresponding current response (submodel output variable). The driving waveform must be carefully designed, in order to excite every possible dynamic behavior of the system under modeling. Such a design, however, is a critical point of every nonlinear identification problem, because only qualitative guidelines are available [3]. Typical driving waveforms are multilevel signals spanning the whole range of allowed input values with suitable duration and added noise. The selection of the driving waveform is a matter of repeated identification experiments, where the ability of different identification signals to yield good quality models is verified over a set of sample systems. In order to obtain driving waveform that can be synthesized by standard waveform generators, we look for the simplest driving waveform ensuring successful identification. Our optimum choice is the trapezoidal voltage waveform shown in Fig. 2, which has flat parts allowing the output port to reach steady state operation and edges with rise/fall times comparable to the switching times of the port. Extensive numerical experiments show that noiseless waveforms of this kind are sufficient for the modeling of typical output buffers.

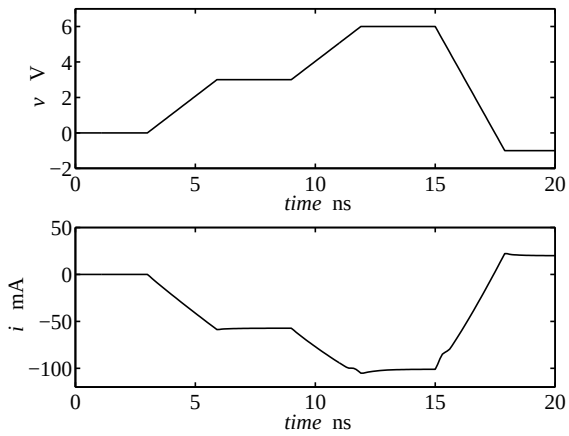

Figure 2: Typical driving voltage waveform $v(t)$ and the corresponding $i(t)$ response, forming the steady state identification signals for submodel f_1.

Once f_1 and f_2 are identified, the weight coefficients w_1 and w_2 are obtained from a set of switching identification signals by linear inversion of (2), *i.e.,*

$$\begin{bmatrix} w_1(k) \\ w_2(k) \end{bmatrix} = \begin{bmatrix} f_1(\boldsymbol{\Theta}_1, \mathbf{x}_a) & f_2(\boldsymbol{\Theta}_2, \mathbf{x}_a) \\ f_1(\boldsymbol{\Theta}_1, \mathbf{x}_b) & f_2(\boldsymbol{\Theta}_2, \mathbf{x}_b) \end{bmatrix}^{-1} \begin{bmatrix} i_a(k) \\ i_b(k) \end{bmatrix} \quad (3)$$

In the above equation, waveforms $\{i_a, v_a\}$ and $\{i_b, v_b\}$ are the switching identification signals, which are recorded when the output port drives two different loads (load (a) and load (b)) and complete state switchings are caused by variations of the logic inputs. To be more precise, the basic sequences (see Sec. IV) w_1^u and w_2^u (w_1^d and w_2^d) are computed from $\{i_a^u, v_a^u\}$ and $\{i_b^u, v_b^u\}$ ($\{i_a^d, v_a^d\}$ and $\{i_b^d, v_b^d\}$) recorded during a LOW to HIGH (HIGH to LOW) transition. There are no restrictions on load (a) and load (b), which can be also real sources stimulating the output port. The best loads would be those allowing $\{i_a, v_a\}$ and $\{i_b, v_b\}$ to explore the widest possible region of the regressor space. We do not yet address the optimization of such loads. Presently we use the same loads recommended by IBIS to characterize port switchings, *i.e.,* load (a) is a resistor and load (b) is a series connection of a resistor and a battery.

In part (2) we compute the model parameters from the identification signal obtained in part (1) of the modeling process. As described above, the evaluation of the weight coefficients $w_n(k)$ is a straightforward operation, that follows the identification of submodels f_n and is carried out via the closed form equation (3). Submodels f_1 and f_2, instead, must be obtained from the steady state identification signals via an actual identification algorithm. We use the algorithm of [2] organized as follows. The steady state identification data define a set of points $\mathbf{x}(k)$ in the regressor space. Each of such point is a candidate center for a radial basis function and the scale parameter β is preset to a value ensuring a good overlapping of every possible basis function. Then, for $p = 1, 2, 3, ...$ steps *(i)* and *(ii)* below are repeated
(i) a new model is built by adding a basis function to the $p-1$ model; the center of the function is the point $\mathbf{x}(k)$ minimizing the mean square error of the new model
(ii) the statistical significance of the new model is assessed by suitable indexes
The selection of the centers is facilitated by the orthogonalization of the time sequences and the process is terminated when the most significant model is reached.

Finally, in part (3) of the modeling process, the identified input-output discrete-time model is replaced by a continuous-time state-space model, in order to be easily coded as a macromodel of circuit simulators like Spice. Such a conversion is achieved by replacing back the time variable in (2) ($t = kT$, where T is the sampling time used to sample the

input and output waveforms) and by approximating the difference operator with the differential one (*e.g.*, $\dot{z}(t) \simeq \frac{1}{T}[z(kT) - z(kT-T)]$). The implementation of the continuous-time model is obtained by the equivalent circuits of its state-space equations, that are RC circuits with controlled sources. Fig. 3 shows an example netlist of the Spice implementation of the 2-piece RBF model (2).

```
.subckt bufRBF w1 w2 u
 Ef1 f1 0 value={
 + {theta11} * EXP(-(PWR(V(u)-{c11},2) +
 + PWR(V(x1)-{c12},2)) / PWR({beta1},2) ) +
 ...
 * output controlled current source
 Gy 0 u value={V(y1)}
 ...
.ends
```

Figure 3: Example of the Spice implementation of the 2-piece RBF model (2).

V. NUMERICAL EXAMPLE

This Section shows the application of the proposed modeling procedure to a virtual device, which is a Spice transistor-level model of the buffer circuit shown in Fig. 4. The parameter values used for this example are those reported at pag. 293 of [5], that are representative of output buffers composed of 1.2 μm CMOS inverter stages. The measurement of v and i of such a virtual device (the Device Under Modeling (DUM) hereafter) is simulated by driving and loading it with the same circuit that would be used in an actual experiment and by computing the response of the complete circuit for Spice. The sampled data needed for the identification are obtained by sampling the computed waveforms with a $T_s = 100$ ps pitch. This example is one of the many identification experiment carried out to tune the proposed modeling approach.

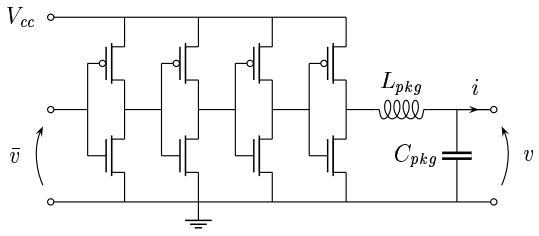

Figure 4: Four stage CMOS output buffer.

The steady state identification signals are obtained by setting $\bar{v}$ either to HIGH or LOW state and by driving the output port with the trapezoidal voltage waveform described in Section IV (see Fig. 2). The switching identification data are obtained by applying a pulse $\bar{v}$ waveform containing a LOW to HIGH transition and, after a sufficient time lag, a HIGH to LOW transition, when the DUM drives either a 100 Ω resistor (load (a)) or the series connection of a 100 Ω resistor and a 5 V battery (load (b)).

The identified model turns out to be composed of two submodels with dynamic order $r = 1$ and number of basis functions $p = 12$. In order to check the quality of the obtained model, we compare its responses with the responses of the DUM for various test loads, different from those used in the computation of the switching identification signals. Figure 5 shows the responses of the model and of the DUM when they apply a logic HIGH pulse to some mainly resistive test loads and to a highly capacitive test load. The accuracy of the model and its insensitivity to the driven load can be clearly appreciated.

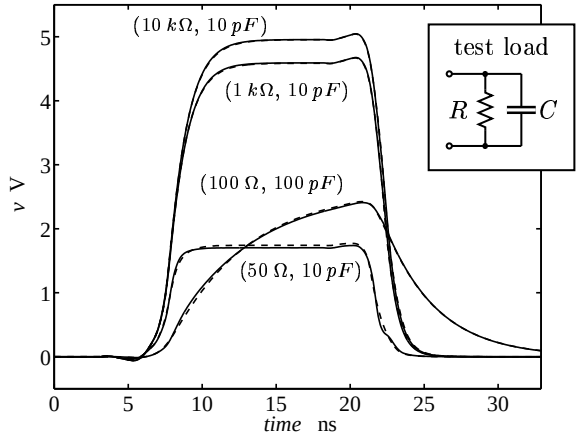

Figure 5: Output voltage waveforms of the example buffer circuit of Fig. 4 for different R and C values of the test load. Dashed lines: reference curves; solid lines: responses of our 2-piece RBF model.

Similarly, Fig. 6 shows the responses of model and of the DUM when they apply a logic HIGH pulse to a ideal open ended transmission line with $Z_0 = 200\,\Omega$ and $T_d = 2$ ns. Again, the identified model turns out to be quite accurate.

VI. EXPERIMENTAL RESULTS

In order to demonstrate the feasibility of the proposed approach, *i.e.*, that measurement errors and noise do not prevent its application, we test it on a real device. In this Section, the DUM is a NAND gate of an HC7400 IC, that is connected as an inverter. Such a DUM is both sufficiently simple and representative to be an easy and significant test case.

For a real device, a text fixture suitable to apply and

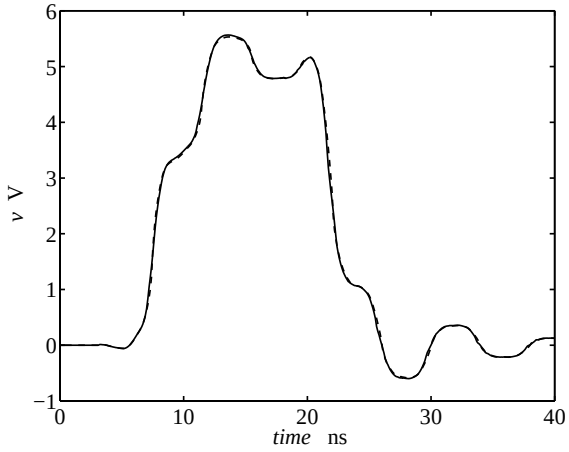

Figure 6: Output voltage waveform of the example buffer circuit of Fig. 4 driving an ideal transmission line (see text). Dashed line: reference response; solid line: response of our 2-piece RBF model.

measure signals is needed. The main point is that, in a real setup, ideal voltage sources are not available and, therefore, the identification voltage waveform cannot be directly imposed. The remedy is to stimulate the DUM by a common waveform generator and to measure both i and v of the output port. The parameter of the waveform generator are then tuned till the observed voltage waveform has the requested behavior (see Sec. IV). The measurement of the output current i can be performed by either a wideband current probe or, indirectly, by a series resistor. We choose the series resistor arrangement and assembled the test fixture shown in Fig. 7.

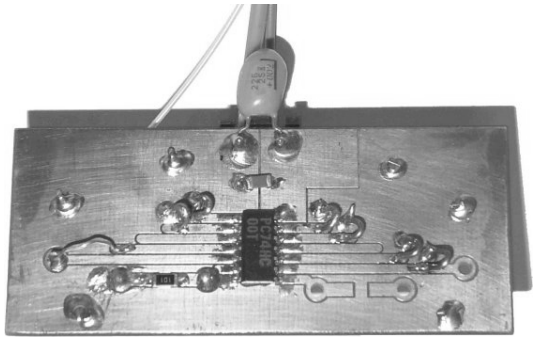

Figure 7: Test fixture.

An SMD $100\,\Omega$ resistor is series connected to the output pin of one of the four NAND gates of the HC7400, whereas SMA connectors are placed on the back of the board to inject and probe signals. The voltages at the terminals of the series resistor are simultaneously recorded by an oscilloscope Tektronix TDS380 (sampling pitch $T = 200\,\mathrm{ps}$) and passive voltage probes P6114B. The current waveform is extracted from the two recorded voltage waveforms via the equivalent circuit shown in Fig. 8 as $i = C_p dv/dt + (v - v')/R_s$. In such a circuit the shunt capacitors at the terminals of the series resistor represent the parasitics of probes.

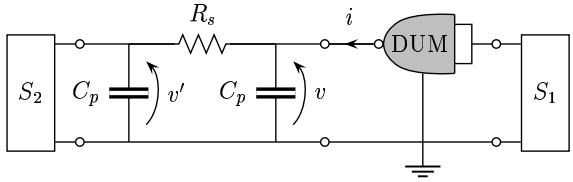

Figure 8: Equivalent circuit of the identification setup ($R_s = 100\,\Omega, C_p = 14.1\,\mathrm{pF}$). S_1 and S_2 are the sources of the identification signals.

The steady state identification signals are generated by using a Rhode&Schwarz AFS multifunction waveform synthesizer connected as S_2 while the DUM input is set, via the source S_1, to either the HIGH or the LOW logic output state. The steady state identification signals obtained in this way for the submodel f_1 are shown in Fig. 9. The waveform generator to excite such signals is not a critical element. In this setup, the shaping of the identification signal is obtained by a stub element connected between S_2 and the test fixture. In a setup for routine measurements, the waveform generator could be provided by a dedicated circuit composed of discrete logic gates. The switching identification signal, finally, are obtained by replacing S_2 with a $50\,\Omega$ coax resistor and with a $60\,\Omega$ carbon resistor connected to V_{cc} as load (a) and load (b), respectively, and by driving (via S_1) the DUM to produce a HIGH pulse.

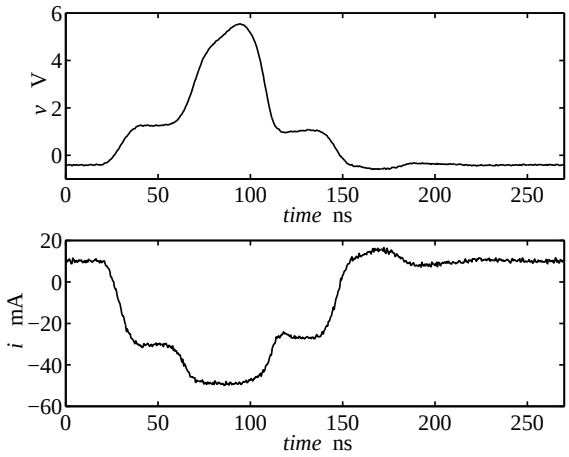

Figure 9: Measured steady state identification signals $v(t)$ and $i(t)$ for submodel f_1.

The identified model turns out to be composed of two submodels with dynamic order $r = 1$ and number of basis functions $p = 5$. Figure 10 shows the result of a validation test for such a model, the two curves are the measured response of the DUM and the computed response of the identified model when they send a pulse on the series connection of R_s and an open ended RG58 coaxial cable (see Fig. 8). Such a comparison shows that the identified model performs at fairly good accuracy level. Besides, it is ought to remark that, in this example, modeling and validation are based on a rather idealized equivalent circuit of the test fixture.

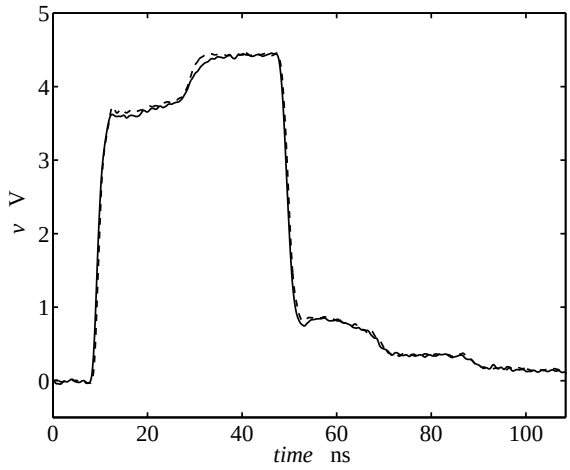

Figure 10: Output voltage waveform of the DUM driving a series connection of a $100\,\Omega$ resistor and an open ended 1.5 m long RG58 coaxial cable ($Z_0 = 50\,\Omega$). Dashed line: measured reference response; solid line: response of the 2-piece RBF model.

VII. CONCLUSION

This paper proposes a black-box approach to the modeling of digital devices for the simulation of EMC effects in fast digital circuits. This approach relies on measured transient waveforms at IC ports and automatically takes into account all the significant physical effects relating the signals. As an example, it takes into account the package parasitics and the nonlinear dynamics of the last stage when such elements indeed influence the observed output waveforms. Besides, the identified models hold for a wide range of driven loads and offer an accuracy level adequate to the simulation of critical EMC effects. The feasibility and the potential of the proposed approach are demonstrated by complete numerical and experimental examples.

VIII. APPENDIX

This Appendix justifies (2). With reference to Fig. 1, the convenient variable for an input/output model of an output buffer would be i (output), v and $\bar{v}_\ell$ (inputs). In fact, the input voltage of the last stage $\bar{v}_\ell$ is strongly related to i and is almost completely controlled by $\bar{v}$. Let $\mathbf{x}^T(k) = [i(k-1), \ldots, i(k-r), v(k), v(k-1), \ldots, v(k-r), \bar{v}_\ell(k-1), \ldots, \bar{v}_\ell(k-r)]$ then $|\mathbf{x} - \mathbf{c}_j|^2 = |\mathbf{x}' - \mathbf{c}'_j|^2 + |\mathbf{x}'' - \mathbf{c}''_j|^2$, where $\mathbf{x}'(k) = [i(k-1), \ldots, i(k-r), v(k), v(k-1), \ldots, v(k-r)]^T$ and $\mathbf{x}''(k) = [\bar{v}_\ell(k-1), \ldots, \bar{v}_\ell(k-r)]^T$. With the above definitions, (1) writes

$$\begin{aligned} i(k) &= \textstyle\sum_{j=1}^{p} \theta_j \exp(|\mathbf{x} - \mathbf{c}_j|^2/\beta^2) \\ &= \textstyle\sum_{j=1}^{p} \theta_j \exp(|\mathbf{x}' - \mathbf{c}'_j|^2/\beta^2) \\ &\qquad \exp(|\mathbf{x}'' - \mathbf{c}''_j|^2/\beta^2) \end{aligned} \tag{4}$$

For typical output buffers, the components of $\{\mathbf{c}''_j\}$, *i.e.,* the position of the basis functions in the subspace of regressor generated by $\bar{v}_\ell$, turn out to be clustered around either V_{ss} or V_{cc}. We verify this property by extensive numerical tests. The rationale for such a property is that the typical surface $i = i(\mathbf{x}'')$ is flat around V_{ss} and V_{cc}, and the centers of the approximating basis functions accumulate in such regions. We then assume $\{\mathbf{c}''_j\}$, the centers of the basis function in the subspace of $\mathbf{x}''$, either exactly at $V_{cc}\mathbf{I}$ or at $V_{ss}\mathbf{I}$, where $\mathbf{I} = [1, \ldots, 1]^T \in \Re^{r+1}$. With such an assumption, (4) splits into two sums collecting the two types of basis functions. Also, for a given input waveform $\bar{v}(t)$, factors $\exp(|\mathbf{x}'' - V_{cc}\mathbf{I}|^2/\beta^2)$ and $\exp(|\mathbf{x}'' - V_{ss}\mathbf{I}|^2/\beta^2)$ are given function of time, and (2) follows.

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Paper X

Behavioral models of digital IC ports from measured transient waveforms

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Abstract: This paper addresses the behavioral modeling of output ports of digital integrated circuits via the identification of nonlinear parametric models. The aim of the approach is to produce models for SI simulation directly from the measured transient responses of devices. The modeling process is thoroughly described and an experimental demonstration of its feasibility is given.

1 Introduction

The numerical simulation of off-chip transmissions of fast digital signals requires effective models of the transmitting and receiving integrated circuits (ICs). Such models must be efficient and accurate enough to allow both the simulation of complex circuits and the prediction of critical Signal Integrity (SI) effects. Behavioral models meet such requirements and are establishing as the main resource for the description of IC ports.

A behavioral model of a device is a set of port characteristic equations obtained from external (possibly virtual) measurements. The most common approach to behavioral modeling is via simplified equivalent circuits of IC ports, because equivalents allow physical insight and facilitate the implementation of models. An important example of the equivalent circuit approach to behavioral modeling is the widely adopted Input/output Buffer Information Specification (IBIS). IBIS offers high numerical efficiency, large data library and commercial software tools handling models and complex modeling problems. The equivalent circuit approach to behavioral modeling, however, has also inherent limitations. Mainly the identification of model parameters is easy only by virtual measurements, *i.e.,* from transistor-level models of the devices, and the physical effects taken into account by the model are decided a priori, when the equivalent circuit defining the model is selected. In order avoid such limitations, in this work we explore the modeling of digital IC ports via the identification of nonlinear dynamic parametric models. Such an approach amounts to seek approximate port characteristic equations of devices and has interesting advantages. Parametric models can be effectively generated from actual measurements, as their identification requires only input and output waveforms. They automatically take into account all the physical effects relating input and output data, for their structure is selected by the identification process itself. As an example, when package parasitics and the nonlinear dynamics of the output transistors contribute to the evolution of the output waveforms, they are automatically included in the model. Finally, parametric models have inherent low sensitivity to the load they drive, which means loads used to measure the output waveforms are not relevant and the obtained models can drive many different loads.

2 Parametric models of IC output ports

In order to discuss the proposed modeling approach, we focus on the modeling of an output port of a digital IC. In this case, the Device Under Modeling (DUM) is an output buffer of an IC. Such a DUM is a 2-port element, whose output port is the observed output port of the IC, and whose input port is on the chip. The parametric model, therefore, must relate voltage and current of the selected output pin (v and i, respectively, with outcoming current reference direction) and the voltage of the buffer input port, that cannot be measured. For this modeling problem, we develop the following 2-piece parametric model [1], that can be identified simply from the v and i waveforms

$$\begin{aligned} i(k) &= w_1(k) f_1(\boldsymbol{\Theta}_1, \mathbf{x}(k)) + w_2(k) f_2(\boldsymbol{\Theta}_2, \mathbf{x}(k)) \\ f_n(\boldsymbol{\Theta}_n, \mathbf{x}(k)) &= \sum_j \theta_{nj} \exp\{-|\mathbf{x} - \mathbf{c}_{nj}|^2/\beta^2\}, \qquad n = 1, 2 \\ \mathbf{x}^T(k) &= [i(k-1), \ldots, i(k-r), v(k), v(k-1), \ldots, v(k-r)] \end{aligned} \tag{1}$$

In the above equation, i is the output variable of the model, f_1 and f_2 are two radial basis function submodels predicting i for varying v and constant logic state, whereas vectors $w_1(k)$ and $w_2(k)$ are time varying weight coefficients that take into account the evolution of the port logic state and act as switches between submodels f_1 and f_2, and, finally, vectors $\mathbf{\Theta}_n$ collect the unknown parameters $\{\theta_{nj}, \mathbf{c}_{nj}, \beta\}$ that must be determined from a suitable set of measured waveforms [2]. Each weight coefficient w_n is obtained by means of a concatenation of two basic sequences $w_n^u(k)$ and $w_n^d(k)$, that describe the "up" and the "down" logic state transitions of the port, respectively. The sequences of the two transitions occur in alternate order and are issued synchronously with the changes of the logic inputs controlling the state of the DUM. Of course, such a simplified model holds only for logic state transitions spaced enough in time, so that every new transition starts after the previous one has been completed. However, since the above validity condition is satisfied in properly working digital circuits, it does not limit the use of the model in SI simulation problems. Indeed the parametric model (1) allows to exploit the advantages outlined in Sec. 1. It is easy to identify and, even with a few basis functions (*e.g.,* $p \in [5, 20]$), the identified models track accurately the behavior of most output buffer circuits for a large set of possible driven loads.

3 Modeling process

The modeling of an IC port via the proposed approach can be divided into three parts: (I) the excitation and recording of transient responses of the DUM, (II) the identification of the model parameters $\mathbf{\Theta}_n$ and w_n, $n = 1, 2$, from the recorded transient responses, and (III) the implementation of the obtained model in a standard circuit simulation environment (*e.g.,* Spice).

Part (I) amounts to drive the DUM to obtain transient output signals carrying information on its behavior. The excitation and response signals involved in this step are named *identification signals*. In our problem, we need two sets of identification signals: the steady state identification signals, for submodels f_1 and f_2, and the switching identification signals, for the weight coefficients w_1 and w_2.

Submodels f_1 and f_2 yield the current response $i(t)$ caused by $v(t)$ at fixed logic state. The steady state identification signals, therefore, are composed of a driving voltage waveform applied to the port (submodel input variable) and of its corresponding current response (submodel output variable). The driving waveform must be carefully designed, in order to excite every possible dynamic behavior of the system under modeling. Such a design, however, is a critical point of every nonlinear identification problem, because only qualitative guidelines are available [3]. Typical driving waveforms are multilevel signals spanning the whole range of allowed input values with suitable duration and added noise. The selection of the driving waveform is a matter of repeated identification experiments, where the ability of different identification signals to yield good quality models is verified over a set of sample systems. In order to obtain driving waveform that can be synthesized by standard waveform generators, we look for the simplest driving waveform ensuring successful identification. Our optimum choice are voltage waveforms composed of three to four level transitions over the range $[V_{ss} - \Delta, V_{cc} + \Delta]$, where Δ is the accepted overvoltage, and edges with rise/fall times comparable to the switching times of the port. The flat parts of the waveform last enough to allow the DUM to reach steady state operation and no noise signal are added (*e.g.,* see Fig. 3).

Once f_1 and f_2 are identified, the weight coefficients w_1 and w_2 are obtained from a set of switching identification signals by linear inversion of (1), *i.e.,*

$$\begin{bmatrix} w_1(k) \\ w_2(k) \end{bmatrix} = \begin{bmatrix} f_1(\mathbf{\Theta}_1, \mathbf{x}_a) & f_2(\mathbf{\Theta}_2, \mathbf{x}_a) \\ f_1(\mathbf{\Theta}_1, \mathbf{x}_b) & f_2(\mathbf{\Theta}_2, \mathbf{x}_b) \end{bmatrix}^{-1} \begin{bmatrix} i_a(k) \\ i_b(k) \end{bmatrix} \tag{2}$$

In the above equation, waveforms $\{i_a, v_a\}$ and $\{i_b, v_b\}$ are the switching identification signals, which are recorded when the output port drives two different loads (load (a) and load (b)) and complete state switchings are caused by variations of the logic inputs. To be more precise, the basic sequences (see Sec. 2) w_1^u and w_2^u (w_1^d and w_2^d) are computed from $\{i_a^u, v_a^u\}$ and $\{i_b^u, v_b^u\}$ ($\{i_a^d, v_a^d\}$ and $\{i_b^d, v_b^d\}$) recorded during a LOW to HIGH (HIGH to LOW) transition. There are no restrictions on load (a) and load (b), which can be also real sources stimulating the output port. The best loads would be those allowing $\{i_a, v_a\}$ and $\{i_b, v_b\}$ to explore the widest possible region of the v-i plane. We do not yet address the optimization of such loads. Presently we use the same loads recommended by IBIS to characterize port switchings, *i.e.,* load (a) is a resistor and load (b) is a series connection of a resistor and a battery.

In part (II) we compute the model parameters from the identification signal obtained in part (I) of the modeling process. As described above, the evaluation of the weight coefficients $w_n(k)$ is a straightforward operation, that follows the identification of submodels f_n and is carried out via the closed form equation (2). Submodels f_1 and f_2, instead, must be obtained from the steady state identification signals via an

actual identification algorithm. We use the algorithm of [4] that works by minimizing the mean square error between the identification output signals and the model output. Such an algorithm enables a Penthium PC to identify submodels with $10 \div 20$ radial basis functions in a few seconds.

Finally, in part (III) of the modeling process, the identified input-output discrete-time model is replaced by a continuous-time state-space model, in order to be easily coded as a macromodel of circuit simulators like Spice. Such a conversion is achieved by replacing back the time variable in (1) ($t = kT$, where T is the sampling time used to sample the input and output waveforms) and by approximating the difference operator with the differential one (*e.g.,* $\dot{z}(t) \simeq \frac{1}{T}[z(kT) - z(kT - T)]$). The implementation of the continuous-time model is obtained by the equivalent circuits of its state-space equations, that are RC circuits with controlled sources.

4 Experimental results

The proposed approach has been tuned by the identification of several virtual devices, that are transistor-level models of typical output buffers. In order to verify its practical feasibility, *i.e.,* that measurement errors and noise do not prevent its application, we verify it on a real device: a NAND gate of an HC7400 IC connected as inverter. Such a DUM is both sufficiently simple and representative to be an easy and significant test case.

For a real device, a text fixture suitable to apply and measure signals is needed. The main point is that, in a real setup, ideal voltage sources are not available and, therefore, the identification voltage waveform cannot be directly imposed. The remedy is to stimulate the DUM by a common waveform generator and to measure both i and v of the output port. The parameter of the waveform generator are then tuned till the observed voltage waveform has the requested behavior (see Sec. 3). The measurement of the output current i can be performed by either a wideband current probe or, indirectly, by a series resistor. We choose the series resistor arrangement and assembled the test fixture shown in Fig. 1.

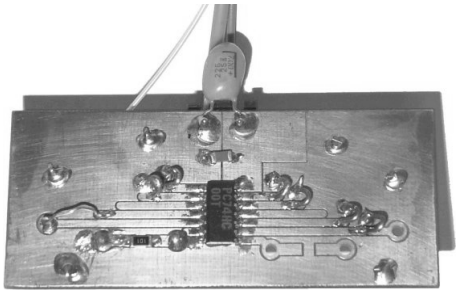

Figure 1: Test fixture.

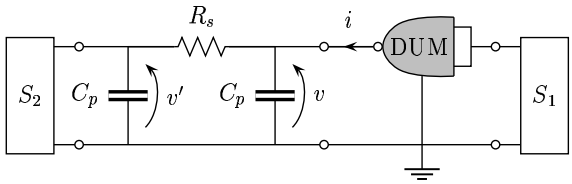

Figure 2: Equivalent circuit of the identification setup ($R_s = 100\,\Omega, C_p = 14.1\,\mathrm{pF}$). S_1 and S_2 are the sources of the identification signals.

An SMD $100\,\Omega$ resistor is connected in series to the output pin of one of the four NAND gates of the HC7400, whereas SMA connectors are placed on the back of the board to inject and probe signals. The voltages at the terminals of the series resistor are simultaneously recorded by an oscilloscope Tektronix TDS380 (sampling pitch $T = 200\,\mathrm{ps}$) and passive voltage probes P6114B. The current waveform is extracted from the two recorded voltage waveforms via the equivalent circuit shown in Fig. 2 as $i = C_p dv/dt + (v - v')/R_s$. In such a circuit the shunt capacitors at the terminals of the series resistor represent the parasitics of probes.

The steady state identification signals are generated by using a Rhode&Schwarz AFS multifunction waveform synthesizer connected as S_2 while the DUM input is set, via source S_1, to either the HIGH or the LOW logic output state. The steady state identification signals obtained in this way for the submodel f_1 are shown in Fig. 3. The waveform generator to excite such signals is not a critical element. In this setup, the shaping of the identification signal is obtained by a stub element connected between S_2 and the test fixture. In a setup for routine measurements, the waveform generator could be provided by a dedicated circuit composed of discrete logic gates. The switching identification signal, finally, are obtained by replacing S_2 with a $50\,\Omega$ coax resistor and with a $60\,\Omega$ carbon resistor connected to V_{cc} as load (a) and load (b), respectively, and by driving (via S_1) the DUM to produce a HIGH pulse.

The identified model turns out to be composed of two submodels with dynamic order $r = 1$ and number

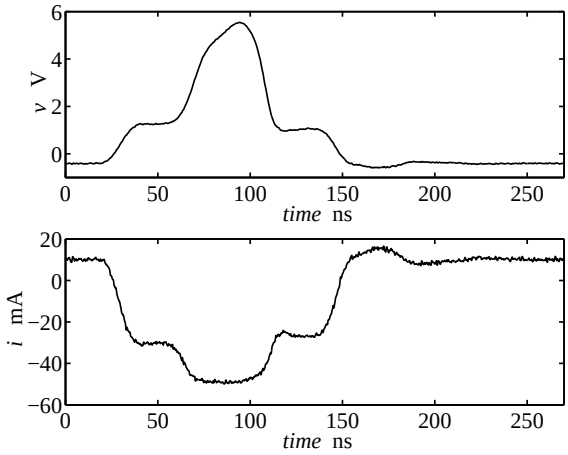

Figure 3: Measured steady state identification signals $v(t)$ and $i(t)$ for submodel f_1.

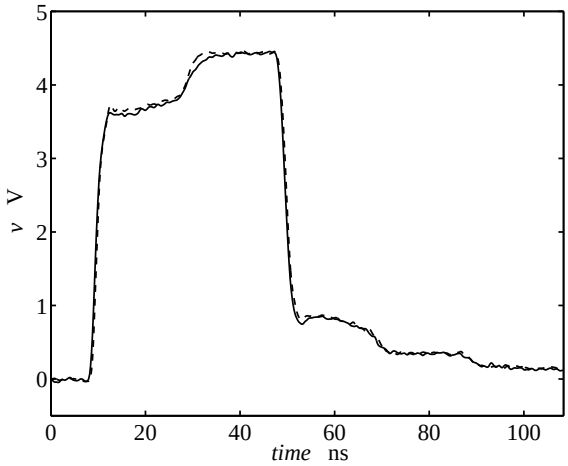

Figure 4: Output voltage waveform of the DUM driving a series connection of a 100 Ω resistor and an open ended 1.5 m long RG58 coaxial cable ($Z_0 = 50\,\Omega$). Dashed line: measured reference response; solid line: response of the 2-piece RBF model.

of basis functions $p = 5$. Figure 4 shows the result of a validation test for such a model, the two curves are the measured response of the DUM and the computed response of the identified model when they send a pulse on the series connection of R_s and an open ended RG58 coaxial cable (see Fig. 2). Such a comparison shows that the identified model performs at a very good accuracy level. Besides, it is ought to remark that, in this example, modeling and validation are based on a rather idealized equivalent circuit of the test fixture.

5 Conclusion

This paper addresses the behavioral modeling of digital IC ports via the identification of nonlinear parametric models. The aim of the proposed approach is to enable any user to easily model poorly documented devices just from measured transient responses and to use the obtained models to assess SI effects on critical nets by standard circuit simulators.

The loads involved in the measurement of the transient responses are not relevant to the identified models, which work accurately for different loads. Also, all the elements that may contribute to the responses of the IC port, as package parasitics and the nonlinear dynamics of the output transistors, are automatically included. Owing to such features, the parametric approach could be easily extended to include other effects, like the simultaneous switching of ports, or to model other ports like, the V_{cc}, V_{ss} port.

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