Foreword Special Section on Electrical Performance Analysis and Simulation of Interconnects, Packages and Devices Composing Electronic Systems for High-Performance

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Foreword
Special Section on Electrical Performance Analysis and Simulation of Interconnects, Packages and Devices Composing Electronic Systems for High-Performance Applications

THIS SPECIAL collection of 11 papers represents new results in electrical performance analysis and simulation of interconnects, packages, and devices composing electronic systems for high-performance applications. This special section includes expanded versions of several papers originally presented at the 11th Workshop on Signal Propagation on Interconnects (SPI), held at Portofino Kulm, Camogli, Italy in May 2007, and at the 16th Conference on Electrical Performance of Electronic Packaging (EPEP), held in Atlanta, GA, in October 2007.

The presentation order of papers proceeds from fundamental issues to applications. The first two papers deal with linear macromodeling. The paper entitled "Modal vector fitting: A tool For generating rational models of high accuracy with arbitrary terminal conditions" introduces a new approach for rational macromodeling of multiport devices by reformulating the vector fitting technique in terms of eigenvalues rather than matrix elements. The resulting modal vector fitting (MVF) method ensures high accuracy with arbitrary terminal conditions. The second paper is titled "A comparative study of passivity enforcement schemes for linear lumped macromodels" and presents a study where three classes of passivity enforcement schemes for linear lumped macromodels are applied to various kinds of high-speed interconnects and packages, with the aim of comparing their performance in terms of accuracy, efficiency, applicability, and robustness. A significant finding of this analysis is that carefully designed weighting schemes may dramatically improve performance for all considered algorithm classes.

The second set of papers concern interconnect modelling. The paper entitled "Frequency domain analysis of transmission zeroes on high-speed interconnects in the presence of an orthogonal metal grid underlayer" presents the propagation analysis of high-density-systems interconnects, and derives a simple equivalent circuit model and a set of expressions based on this model enabling to analytically determine the location of transmission zeroes in the frequency domain, for different orthogonal metal grids. The next paper, entitled "Performance comparison between metallic carbon nanotube and copper nano-interconnects" compares traditional copper interconnects with bundles of metallic carbon nanotubes. A new model fitting with the classical transmission line theory, is presented to describe the propagation of electrical signals along these carbon nanotube bundles.

The two subsequent contributions concern nonlinear macromodeling of digital devices. The paper titled "Locally-stable macromodels of integrated digital devices for multimedia applications" describes new techniques to macromodel device I/O for system level interconnect simulations. Such models are essential to enabling efficient system level simulation evaluations to be undertaken. Using SPICE level models is inordinately slow. The paper titled "Improving behavioral IO buffer modeling based on IBIS" demonstrates that the IBIS (input output buffer information specification) standard falls short of becoming a complete IO behavioral model when simulating for simultaneous switching noise, and presents a method for complementing the model with a black box that is simulator independent, without compromising with the speed that IBIS enjoys over the transistor models.

Then, three papers follow on system simulation. The paper entitled "Accurate system voltage and timing margin simulation in high-speed I/O systems designs" describes a statistical simulation technique to model random jitter in multi-Gbps serial links. Random jitter is an important source of eye closure, and if not included in the simulation, would lead to under prediction of bit error rate. However, including it as a random event in SPICE simulations would lead to slow simulations. A new technique is needed and is described in this paper. The next paper is entitled "Controlled inter-symbol interference design techniques of conventional interconnect systems for data rates beyond 20 Gbps" and reviews approaches to managing intersymbol interference and presents new passive methods for controlling it, and thus extending the data rate. The final paper under the heading of system simulation is entitled "Multiple edge responses for fast and accurate system simulations" and presents a fast technique for simulating high speed serial links, based on superimposing edge responses.

This special collection ends with two contributions related to applications. The paper entitled "Inductively coupled connec-

tors and sockets for multi-Gbps pulse signaling" presents the results of a set of experiments demonstrating multi-Gbps signalling data-rate capability and describes the principles behind the design of inductively coupled sockets and connectors. The final paper "Polymer-waveguide-based board-level optical interconnect technology for datacom applications" illustrates the capabilities of a polymer-waveguide-based board-level optical interconnect technology by means of a 12×10 Gbps card-to-card optical link demonstrator.

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Dr. Canavero is and Technical Editor of the EMC Newsletter. He has been the Editor-in-Chief of IEEE TRANSACTIONS ON ELECTROMAGNETIC COMPATIBILITY, and Chair of URSI Commission E (Noise and Interference). He received the IBM Faculty Award for the triennium 2003–2005, the Intel Research Grant for 2008, and several Best Paper recognitions. He has been the Organizer of the Workshop on Signal Propagation on Interconnects (SPI) (2001–2003, and 2007), and he is currently a member of the Scientific Steering Committees of several International Conferences in the field of EMC and electrical performance of interconnects and packages.

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