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***Abstract*—The design, implementation and characterization of a Doherty Power Amplifier (DPA) for 3.5 GHz WiMAX applications are discussed. The DPA has been implemented using a commercial GaN HEMT from Cree inc., following a class AB and C scheme for the main and peak module, respectively. The measured maximum power of the DPA is 22 W with a first peak efficiency of 57%, and maximum drain efficiency of 65% at the DPA saturation. Efficiency over the so-called Doherty region (where both the main and the peak amplifiers operate) does not drop below 55% from saturation to 6 dB input back-off. The gain at the onset of the Doherty region is 8 dB, with around 1 dB roll-off.**

***Index Terms*—GaN, power amplifier, wireless communications, Doherty**

## I. INTRODUCTION

The high signal Peak to Average Power Ratio (PAPR) typical of many modern wireless communication standards [1], [2] implies that transmitter amplifies operate on average with a significant power back-off with respect to the maximum output power. In fact, the high dynamics of the instantaneous signal power, conventionally described by the PAPR parameter, makes the PAs work on a large interval of power ranges, rather than at a fixed level, as in the case of constant or quasi-constant envelope modulations (e.g. GSM signal). In these conditions, the behavior of the efficiency as a function of the power level is definitely more important than the maximum efficiency in power saturation. Under this respect, a significant figure of merit will be the average efficiency, weighted according to the statistical distribution of the instantaneous power.

In the present paper we focus of the WiMAX standard, whose signal exhibits a PAPR of several dBs (up to 9 dB). To achieve high efficiency on a large output power range, the Doherty scheme, due to its relative simplicity, is one of the most exploited solutions, although its application to high frequencies (typically above a few GHz) exploiting conventional technologies (e.g. Si based LDMOS) poses significant challenges [3], [4]. In this framework, the GaN based HEMT technology appears to be the most valid candidate to replace LDMOS devices for higher frequency, even if only few results on DPA at frequency above the WiFi band, around 2.4 GHz, have been so far published.

The paper presents the design strategy, implementation details, and experimental results of a DPA fabricated with a commercial GaN process for WiMAX applications, i.e. 28 MHz bandwidth around 3.5 GHz. The realized DPA exhibits an output power higher than 22 W, with efficiency higher than 55% in a 6 dB input power back-off (IBO) range, therefore demonstrating very good efficiency performances when compared with recently published works adopting similar device technology, for the same kind of applications, e.g. [5].

The paper is organized as follows: section II describes the several steps of the design procedure, section III presents and discusses the carried out measurements, while in section IV some conclusions are finally drawn.

## II. DESIGN STRATEGY

The active device employed in the DPA is the CGH40010 from Cree inc., a GaN HEMT with typical output power of 10 W in C band, at the suggested drain bias of 28 V [6]. As a preliminary step, a cold-FET characterization campaign has been carried out to identify the extrinsic elements, needed to deembed the parasitic elements, and accurately transfer the external loads to the intrinsic drain current generator reference plane.

The DPA configuration is the well-known AB-C scheme (see Fig. 1), with a class AB and a class C amplifiers used as main and peak stage, respectively. To further increase the efficiency, the main amplifier has been designed exploiting a second harmonic tuning approach [3], rather than following a more conventional AB tuned load strategy.

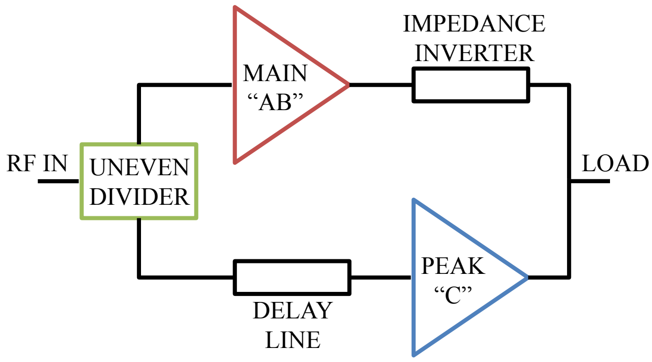


Fig. 1: Block scheme of the designed AB-C DPA.

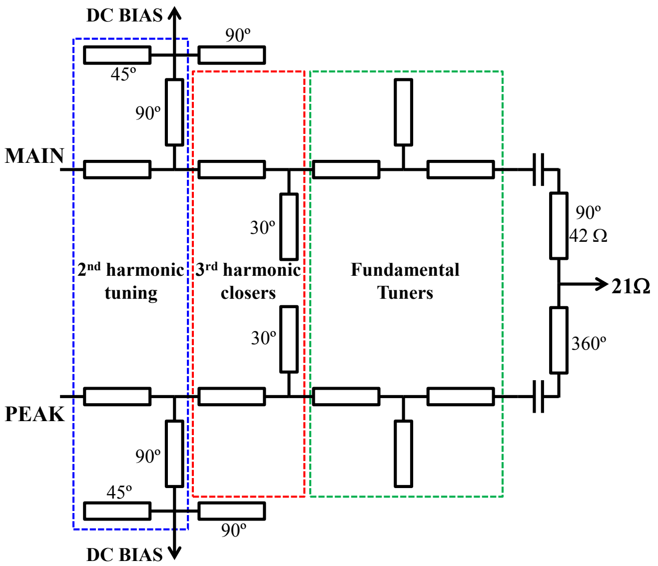


Fig. 2: Detailed scheme of the output matching network for the designed DPA.

The design of the output matching networks (OMNs) of the main and peak amplifiers, whose topologies are sketched in Fig. 2, has been carried out through careful exploitation of the active device foundry model (with parasitics deembedding), and Agilent Momentum EM simulations of the passive networks. The $R_{\text{opt}} = 30\,\Omega$ optimum load of the main amplifier at the fundamental frequency, found in tuned load conditions, must be increased by a factor of 1.41 [3] when using second harmonic tuning, thus leading to $R_{\text{opt,main}} = 42\,\Omega$. The OMN of the main stage has been therefore designed to produce a load of $84\,\Omega$, before the Doherty region, and of $42\,\Omega$ at its end. Finally, two $\lambda/4$ impedance transformers have been exploited to achieve the main load modulation, and for the output matching to the external $50\,\Omega$ load. From Fig. 3 it can be seen that the ratio between the fundamental and second harmonic components of the drain voltage is maintained almost constant for the 6 dB Doherty region of the DPA thus leading to a proper harmonic shaping of the drain voltage waveforms.

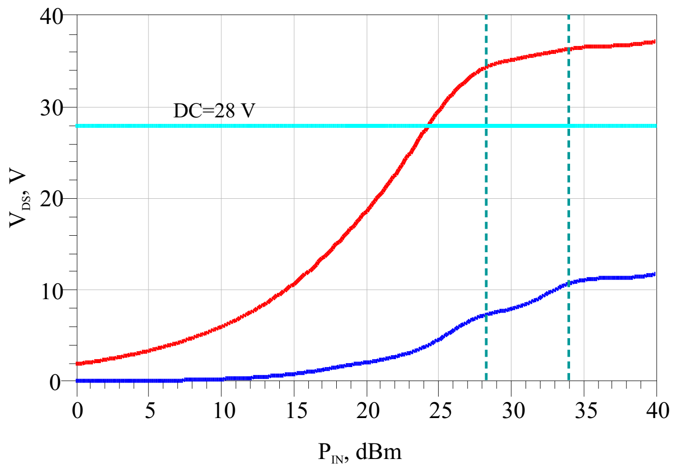


Fig. 3: Harmonic component simulation of the Main amplifier drain voltage: DC (light blue), fundamental (red) and II harmonic (blue).

According to the Doherty approach, the peak amplifier has been designed to ensure the correct load modulation of the main amplifier and, at the same time, the proper Class C loading termination for optimum power and efficiency.

The input power divider has been designed with uneven splitting to fed a larger input power to the peak, than to the main amplifier. This was made in order to combine the correct switch-on and gain of the peak amplifier. The optimized input divider ratio was found to be 42% for the main, and 58% for the peak. This splitting factor was obtained through a microstrip branch line optimized using electromagnetic simulations carried out with ADS Momentum; the final branch layout is shown in Fig. 4, while the EM simulation results of the designed branch line divider are shown in Fig. 5. Due to the high power level to be handled, an external $50\,\Omega$ load connected with a SMA connector at the branch line isolated port has been introduced instead of a SMD resistor. Finally, the input matching networks (IMNs), embedding the RC stabilization network, were designed to achieve a matching better than -10 dB over a 170 MHz bandwidth (see Fig. 6).

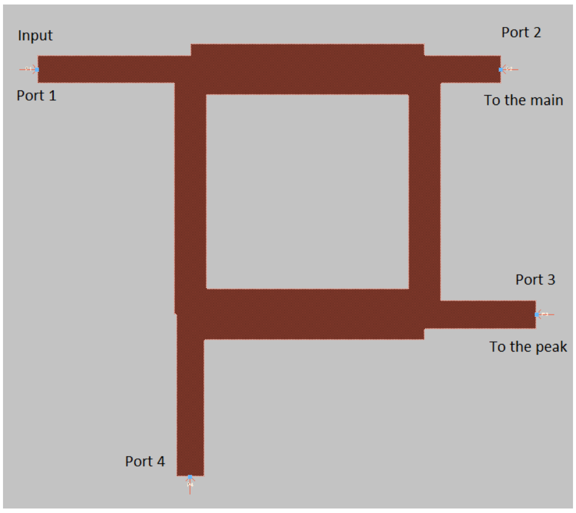


Fig. 4: Layout of the designed branch line divider.

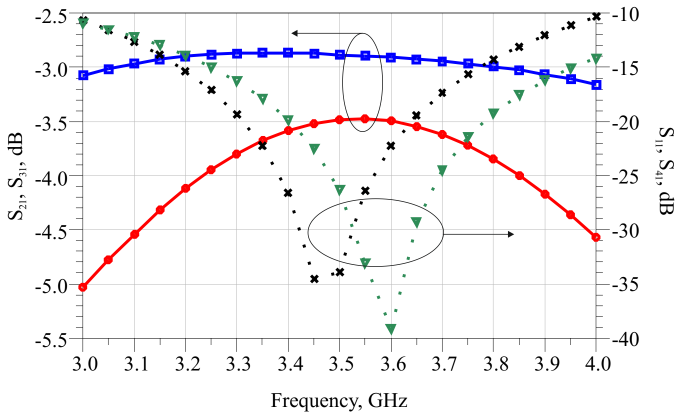


Fig. 5: EM simulations of the branch line uneven divider: $S_{11}$ (black + crosses), $S_{41}$ (green + triangles), $S_{21}$ (red + circles) and $S_{31}$ (blue + squares).

The microstrip circuit, fabricated exploiting a Taconic substrate with copper metalization (RF35 with $\epsilon_r = 3.5$, $H = 0.76$ mm and $t = 0.035$ mm) has been mounted on an aluminum carrier ensuring a properly dimensioned heat dissipator: a picture of the realized amplifier is presented in Fig. 7.

## III. RESULTS

The DPA has been characterized in small signal condition, and under single tone large signal excitation [8], [9], with nominal bias $V_{\text{DS,main}} = 28$ V, $V_{\text{GS,main}} = -2.73$ V (10% $I_{\text{DSS}}$), $V_{\text{DS,peak}} = 28$ V, and $V_{\text{GS,peak}} = -7$ V. Bias adjustments, to account for the expected loss of model

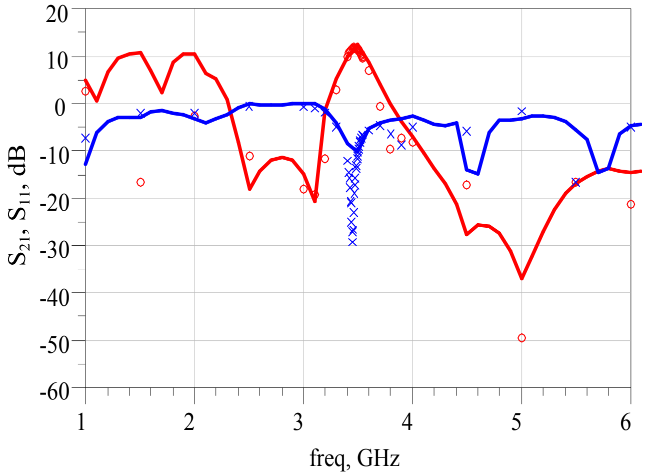


Fig. 6: Simulations (solid lines) and measurements (symbols) for $S_{11}$ (blue) and $S_{21}$ (red) of the DPA.

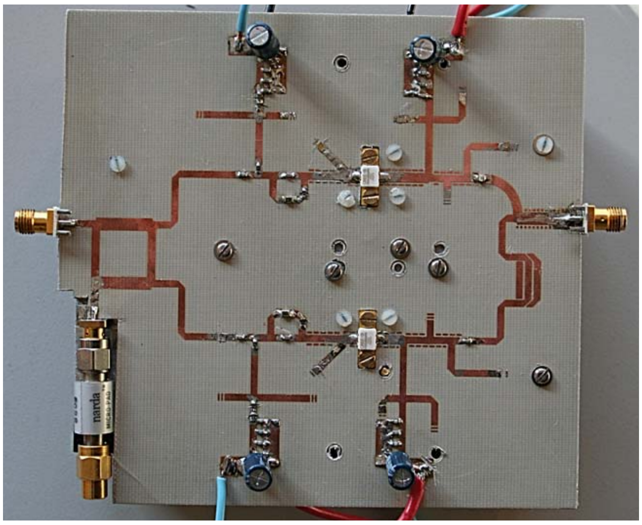

Fig. 7: Picture of the fabricated DPA.

accuracy for the deep class C active device of the peak, has been carried out (see [3], [10]), and the experimentally optimized values resulted unchanged for the main, while, $V_{\text{DS,peak}} = 26$ V and $V_{\text{GS,peak}} = -8.1$ V have been finally selected. As an example of the agreement found in small-signal conditions, between simulated (solid lines) and experimental data (symbols), concerning $S_{11}$ (blue) and $S_{21}$ (red) of the realized DPA are shown in Fig. 6. Fig. 8 summarizes instead the DPA power performances, showing output power, gain and efficiency. All values are in good agreement, although the measured efficiency is somewhat lower than the simulated one. The resulting saturated output power is around 43.5 dBm for an input power of 36 dBm. The first peak efficiency, according to the Doherty theory, appears at roughly 6 dB input back-off from the second one, for both measurements and simulations, and the measured drain efficiency, higher than 55% in a 6 dB IBO range with respect of the saturated power, exhibits a gain roll-off in the Doherty region lower than 1.4 dB.

The DPA main and peak measured DC current, relative to the maximum current of 700 mA, are reported in Fig. 9 stressing the correct peak amplifier turn on when the main stage reaches the first efficiency peak, and thus demonstrating the behavior expected from the Doherty theory.

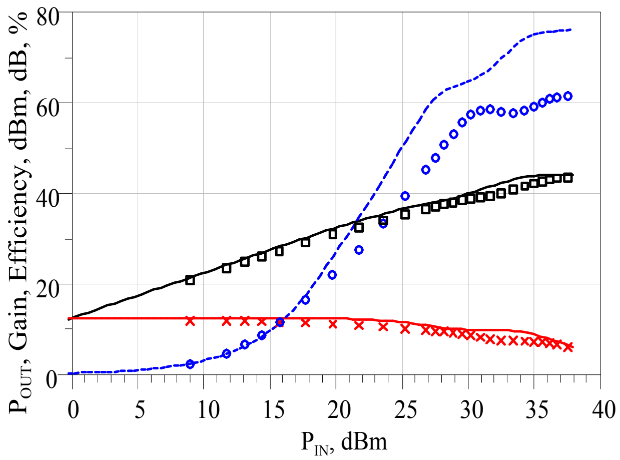


Fig. 8: Single Tone measurement of the 3.5 GHz DPA. Lines refer to simulations, while symbols to the measurements. Output power (black), Transducer gain (red) and Drain efficiency (blue).

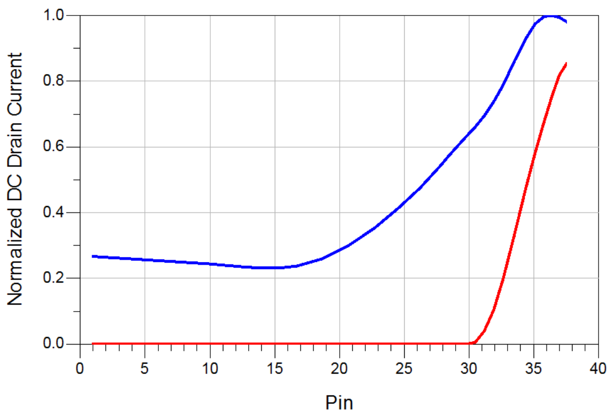


Fig. 9: Measured DC drain currents of Main (Blue) and Peak (Red) amplifiers.

## IV. CONCLUSIONS

Design strategy, implementation details, and results on the characterization of a Doherty Power Amplifier for 3.5 GHz WiMAX applications, based on a 10 W Cree GaN device has been presented and demonstrated. The final microstrip realization, fabricated on RF35 Taconic substrate, has shown a maximum output power of 22 W and efficiency higher than 55 % for 6 dB output power span, corresponding to the designed Doherty region. The monitoring of the main and peak amplifier DC currents as a function of the power level demonstrated the correct switch on of the peak amplifier relatively to the main stage, and therefore the proper Doherty operation of the presented power module. The measured performances show a significant improvement with respect to previous published results for the same frequency and application.

## V. ACKNOWLEDGMENTS


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