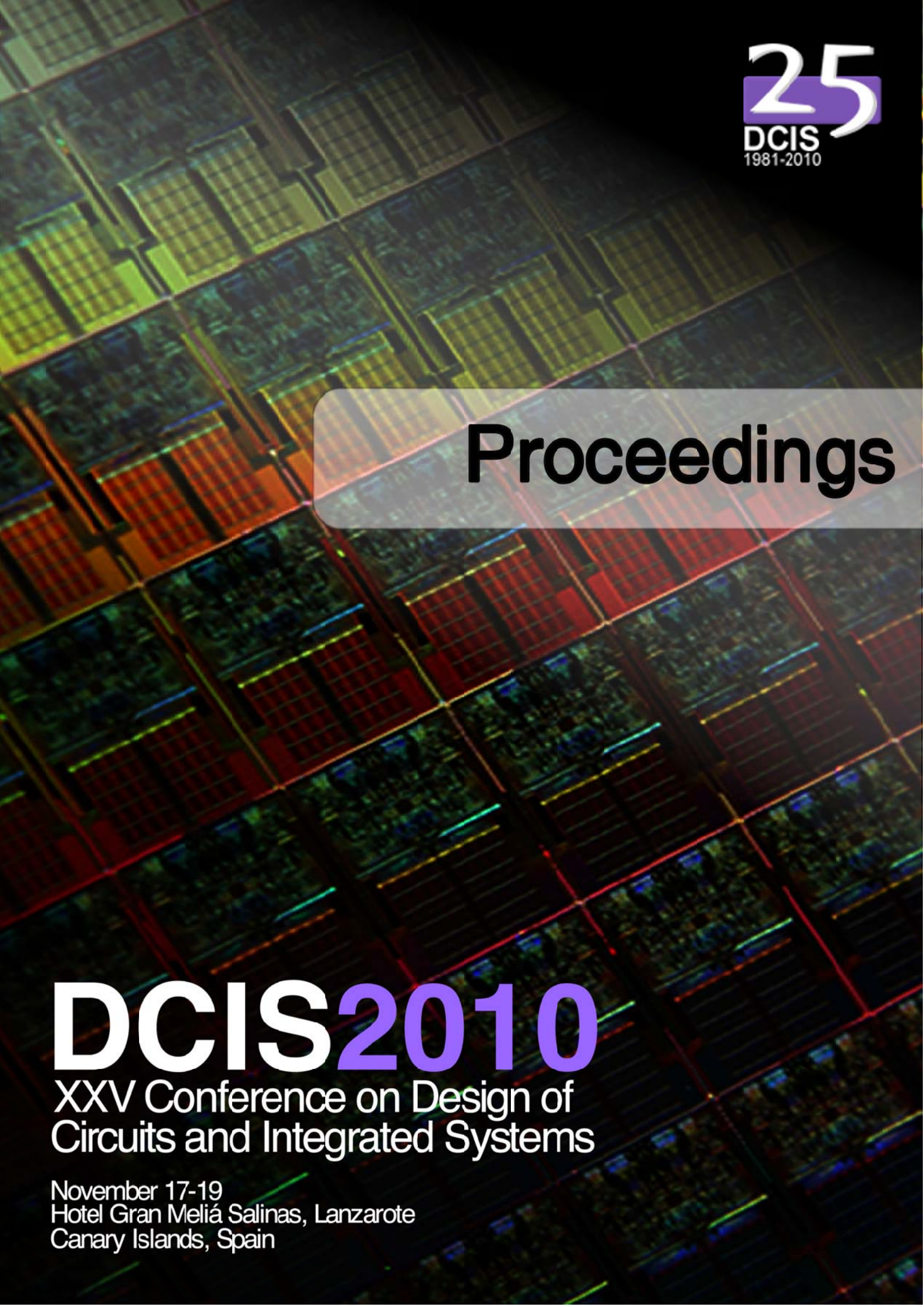
8T SRAM Defective Cell with Open Defects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***Abstract*—The defective behaviour of an 8T SRAM cell with open defects is analyzed. Full and resistive open defects have been considered in the electrical characterization of the defective cell. Due to the similarity between the classical 6T SRAM cell and the 8T cell, only defects affecting the read port transistors have been considered. In the work, it is shown how an open in a defective cell may influence the correct operation of a victim cell sharing the same read circuitry. Also, it is shown that the sequence of bits written on the defective cell prior to a read action can mask the presence of the defect. Different orders of critical resistance have been found depending on the location of the open defect. A 45nm technology has been used for the illustrative example presented in the work.**

Keywords: open defect, 8T SRAM cell, read error, delay fault, test, defect analysis.

I. INTRODUCTION

The extensive use of programmable processor cores in SOCs require a large amount of embedded SRAMs to implement on-chip data and instruction storage. The area occupied by SRAM is currently higher than the rest of the IC circuits and is increasing for each new technology node.

The aggressive scaling of SRAM cells decreases the reliability of operation of the memory cores due to an increasing impact of the variability of the process parameters, voltage and radiation noise and IC temperature gradients. The ITRS 2009 [1] reports an increase of three orders of magnitude (a factor of 10^3) in the variability-induced failure rate when scaling High Performance SRAM from 45 nm to 32 nm. The study assumes the traditional 6T cell design with the same circuits (pMOS and nMOS ratios, sizing and required read/write circuits, etc.) and the PTM [2] models with the expected process variability.

The vulnerability of the SRAM cores to catastrophic defects is also increasing due to the reduction of the minimum feature size and the higher complexity of the process steps. Open and bridge catastrophic defects are increasing in each new technology node and there is growing concern on its impact of the fabrication yield. Defect based testing (DBT) strategies require to analyse the impact of the defects in nano-scaled CMOS circuits [3]. The increasing number of contacts and vias, the reduced size of the connecting lines and the required process steps increase the probability of open defects. Some of these opens are *full* opens (the open defect causes a complete electrical disconnection) but other defects called *resistive* opens are modelled with a resistance added in the broken line [4].

Most of current defect based memory test algorithms are centred in the 6T (six transistors) cell circuit which is the dominant present architecture for commercial embedded SRAM cores. The 6T SRAM shares the bit lines for the READ and WRITE operations. To guarantee an acceptable SNM during the READ operation, the strength of the access nMOS transistor must be low compared to the strength of the pull-down nMOS. On the other hand, to assure an acceptable SNM during the WRITE operation, the strength of the access nMOS transistors must be high compared to the strength of the pull-down nMOS. These conflicting requirements are acceptable for cells with large SNM, but in the future with lower margins the cell becomes unreliable.

To overcome this problem in future technology nodes, for 32 nm and beyond, the 8T SRAM cell has been proposed [5] [14] as a possible substitute of the 6T cell SRAM. As can be observed, in the 8T cell of Figure 1 the READ and WRITE paths are independent thanks to adding a Read Word Line (RWL), a Read Bit Line (RBL) and two stacked transistors (RD and RDaux) [7] [8].

In this paper, we focus our attention to the open defects (full and resistive) located on the read port of the 8T SRAM cell. The defects on the 6 remaining transistors would behave similarly to the defects on the classic 6T cell which have been widely researched in recent years [9]-[12].

The rest of the paper is organized as follows: Section II reviews the 8T cell circuit functionality. The impact of the open defects is analyzed in Section III. A summary of the defective behaviour of the full and resistive opens is listed in Section IV. Finally, the conclusions of the work are presented.

II. 8T SRAM CELL

Figure 1 shows the electrical schema of the 8T SRAM cell considered in this work. The 8T SRAM is based on a cell schematically similar to cells commonly used in register files, by separating the Read Word Line (RWL) and Write Word Line (WWL) and adding two stacked NMOS transistors for single-ended read action.

Since the 8T memory cell has a separated read port comprised of two transistors (RD and RDaux in Figure 1), there is some area overhead compared with the 6T cell. However, some voltage control scheme proposals enable the

scalability of 8T SRAM cell crossing down the 6T cell area for technology nodes below 45nm [8].

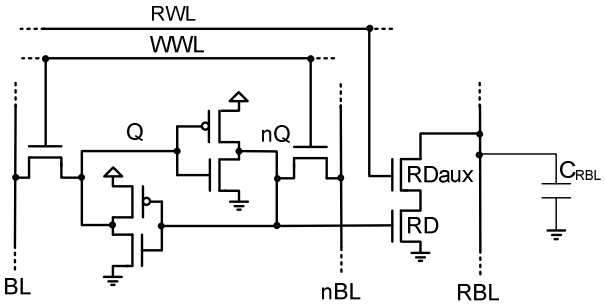

Figure 1 Electrical schema of the 8T SRAM cell considered.

During the normal operation of the 8T SRAM, the RDaux transistor is activated with signal RWL in order to perform a read action on the memorized bit, as illustrated in Figure 2. Assuming that the Read Bit Line (RBL) has been precharged to a high value before the reading operation, the RBL node will keep the high voltage if a memorized Q=1 (nQ=0) is in the cell (see Figure 2a). In the case of Q=0, the high voltage (nQ=1) feeding the RD transistor gate allows the discharge of C_{RBL} through the two stacked *on* transistors, as illustrated in Figure 2b.

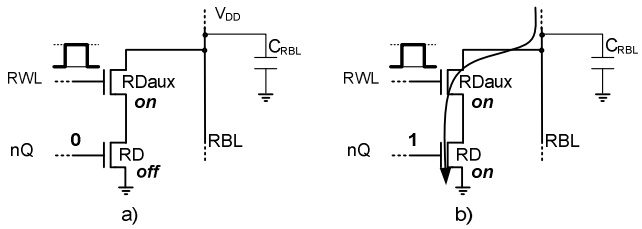

Figure 2 Read operation of the memory bit in the 8T SRAM cell of a previously a) Q=1 and b) Q=0 written state.

HSPICE simulations have been carried out in order to characterize the electrical behaviour of the SRAM cell. The Berkeley Predictive Technology Model 45nm has been used and standard sizing [7] [13] has been chosen to implement the cell included in this work as an illustrative example.

Figure 3 shows the timing response of the defect-free cell for a sequence of writing and reading actions assuming a working frequency of 1GHz. Figure 3c indicates the three W0-W1-W0 write operations (triggered by WWL) followed by the read action R0 (triggered by RWL). Figure 3b shows the response of Q and nQ to these write and read actions. Finally, Figure 3a illustrates the precharge of node RBL prior to the read operation, which results in a completed discharge of C_{RBL} as a consequence of nQ=1, i.e. Q=0.

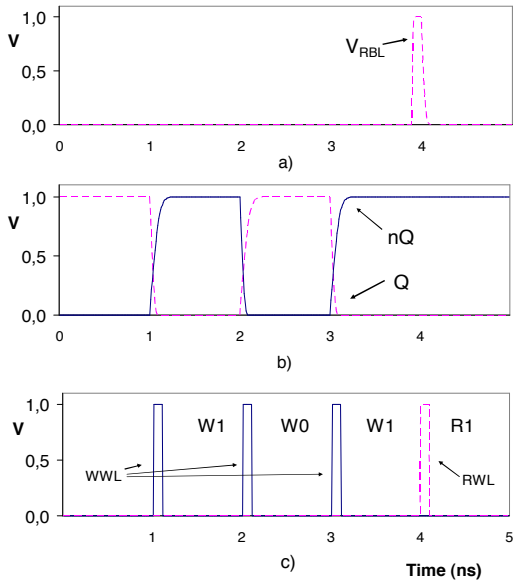

Figure 3 Timing behaviour of the defect-free 8T SRAM cell: c) indicates the write and read actions performed on the cell; b) shows the response of Q and nQ nodes; the precharge of node RBL is shown in a), together with its subsequent discharge as response to nQ=1 (triggered by RWL).

III. Defective 8T SRAM Cell

In this section, open defects affecting the terminal nodes of the read port transistors RD and RDaux are analyzed, (see Figure 4). The effects of full and resistive opens on each location are presented. During the electrical characterization, the written values on the cell are assumed to be correct since the defects only affect the read port.

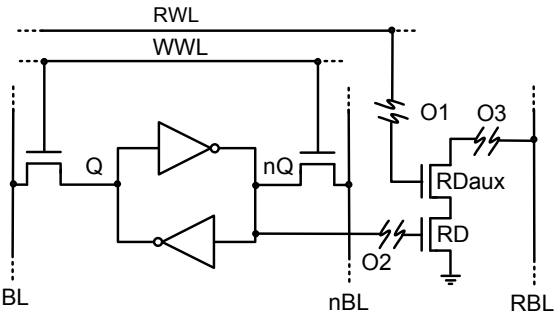

Figure 4 Open defects affecting the read port of an 8T SRAM cell.

A. Open defect at the gate of RDaux transistor (O1)

1) Full open defect O1

In the case of Q=1 (nQ=0), shown in Figure 5, the complete electrical discontinuity at the RDaux transistor gate does not affect the reading operation of the cell. In this case, the defect-free *off* transistor RD assures the precharged C_{RBL} capacitor to keep its charge and, thus, results in a correct reading R1 (Q=1).

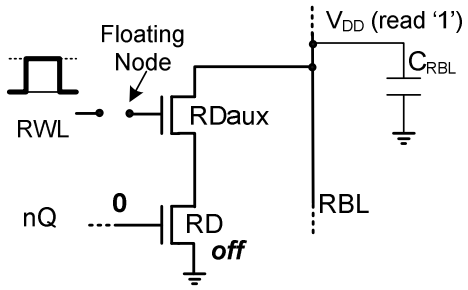

Figure 5 Full open defect O1 in the case of Q=1, nQ=0. The reading operation is correct since the precharged RBL line keeps the electrical charge.

Let us now consider that the memorized state is Q=0, i.e. nQ=1. Under this circumstance, the RD transistor is *on* as shown in Figure 6 and, in the case of a defect-free cell, the RBL should be discharged in order to correctly detect nQ=1 (R0). However, as illustrated in Figure 7, the floating node FN remains in an intermediate voltage that only allows the partial discharge of C_{RBL}. Indeed, during the RBL precharge, the coupling capacitance C_{par} (see Figure 6) pulls up the voltage of the floating node FN to an intermediate value V_{FN}. Note that this is possible because the positive RWL pulse is disconnected from the floating node due to the defect. The discharge of the RBL node is performed through the weakly *on* RDaux transistor (and RD), and is slower than expected.

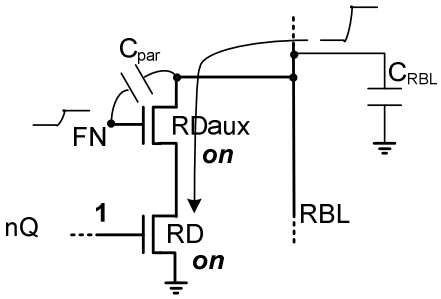

Figure 6 Effect of the precharge of RBL on the floating node in the case of a full open defect O1 with Q=0. The RBL precharge pulls up the floating node due to the coupling capacitance Cpar. The subsequent reading operation may be incorrect since the precharged RBL line is only partially discharged.

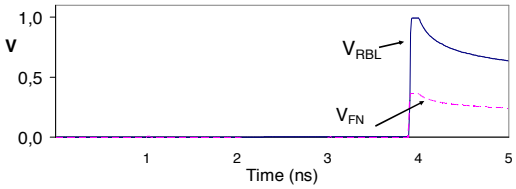

Figure 7 Partial discharge of RBL due to the intermediate voltage V_{FN} caused by the full open O1.

The behaviour illustrated in Figure 7 is due to the capacitive coupling between the floating node and the RBL line (the larger the capacitance, the higher the resulting voltage V_{FN} is). The effect of this intermediate voltage V_{FN} depends, among others, on the threshold voltage of the RDaux transistor, on the value of C_{RBL} (which depends on the number of cells sharing the same read bit line). As a result, the readout of the cell (with Q=0) depends on whether the final V_{RBL} falls below the threshold voltage of the read circuitry or not. The effect of the full open is a non assured correct reading R0.

2) Resistive open defect O1

The case where the open defect is a partial break of the electrical connection is shown in Figure 8 assuming the resistive model of the open [4]. Depending on Ropen, the gate of RDaux transistor may reach a sufficient voltage able to properly discharge C_{RBL}, as illustrated in Figure 9 for different resistance values. Figure 10 shows the defective node voltage (V_{FN}) and the discharged V_{RBL} at the end of the reading phase, for the 45nm SRAM cell considered in this work. In this example, Ropen<6.4MΩ result in V_{RBL} discharged below $V_{DD}/2$. Assuming a nominal threshold voltage of $V_{DD}/2$ for the read circuitry, although the electrical RBL response is degraded, the nQ bit is correctly interpreted as 1 (R0).

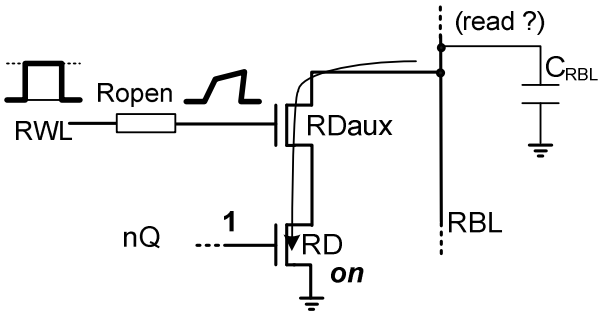

Figure 8 Partial open defect O1 modeled with resistance Ropen.

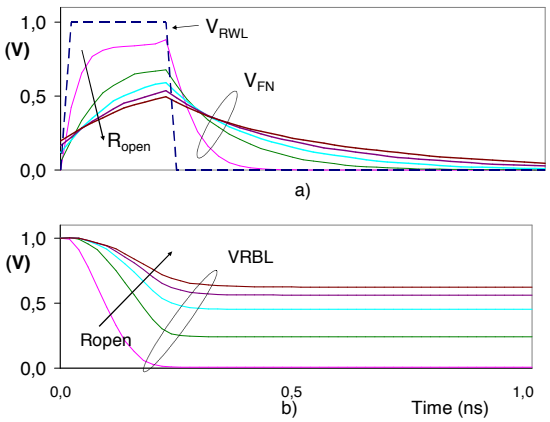

Figure 9 Response of the a) floating node voltage V_{FN} to a positive pulse V_{RWL} and b) resulting discharge of V_{RBL} depending on the resistance of the defect (Ropen).

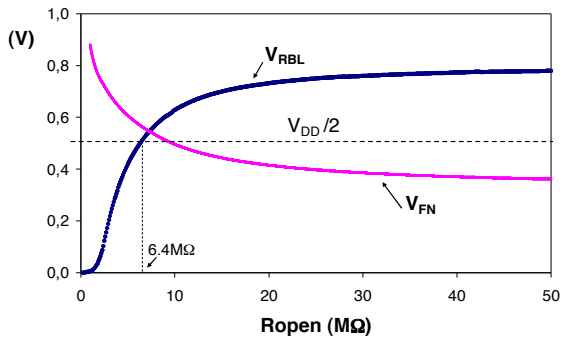

Figure 10 Read Bit Line voltage detected by the read circuity versus the resistance of the open O1.

3) Impact of O1 on victim cells

The presence of O1 in a defective cell may impact the read operation on other defect-free cells sharing the same RBL. In order to analyze this fact, let us assume a defect-free cell *i* and a defective cell *j*, as illustrated in Figure 11, which are connected to the same RBL.

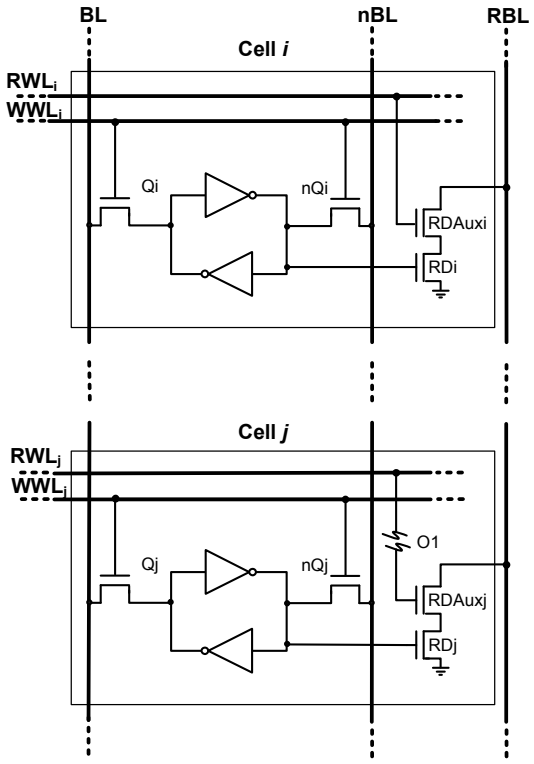

Figure 11 Defective cell *j* and defective-free cell *i* connected to the same Read Bit Line.

The electrical interaction between both cells is simplified to the circuit shown in Figure 12. In the case where the operation $R0_i$ is performed on the victim cell *i* (Qi=0, nQi=1), the influence of cell *j* has no effect and the RBL line is correctly discharged through the read port of cell *i*.

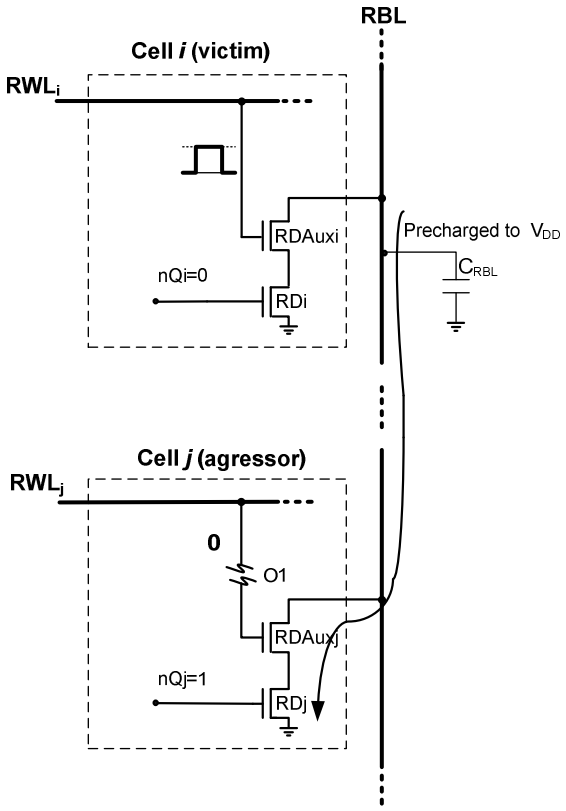

Figure 12 Read action on victim cell *i* affected by defect in agressor cell *j* due to full open O1.

However, the read operation $R1_i$ (Qi=1, nQi=0) can be disturbed by the connection to the read port of cell *j*. Let us assume the circuit in Figure 12 with Qi=1 and Qj=0, in this case, the read operation on Qi should keep C_{RBL} precharged to a high value, however the full open defect O1 allows the weak connection of $RDaux_j$ and, thus, the partial discharge of RBL (similar to Figure 7). Note that a resistive open O1 in cell *j* does not affect the reading of cell *i* since RWL*j* is not activated in this case.

B. Open defect at the gate of RD transistor (O2)

1) Full open defect O2

The resulting electrical circuit derived from the defective cell with full open O2 is illustrated in Figure 13. The effect of O2 during the read operation of the cell is expected to be similar to the effect of O1 since the floating gate node is also capacitively coupled (C) to the drain terminal of the defective transistor, as illustrated in Figure 13. The activation of RDaux with the positive pulse at RWL pulls up node x to V_{DD}-V_{TH} and node x, in turn, pulls up the floating node (due to C) to an intermediate voltage V_{FN} (see Figure 14a). However, voltage V_{FN} is not able to turn *on* RD transistor due to the voltage drop caused by RDaux. The value on nQ is always read as 1 since the RBL is not discharged (see Figure 14). The read action R0 is erroneous.

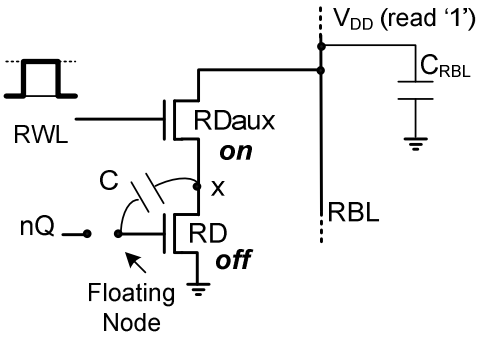

Figure 13 Full open defect O2 always resulting in a readout equal to "1" since the RD transistor remains *off*.

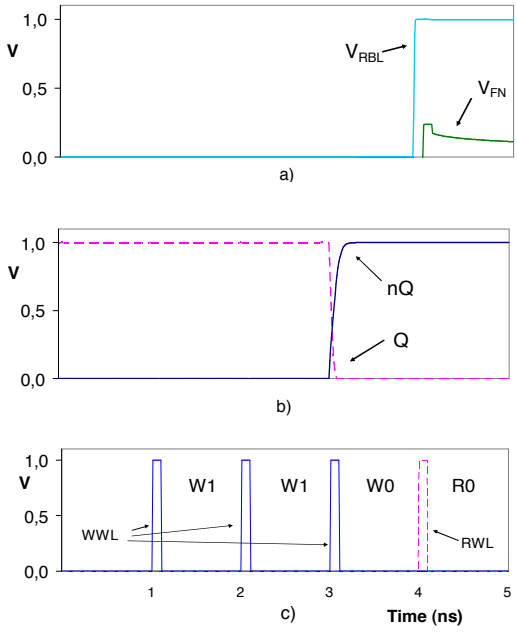

Figure 14 Read error R0 due to a full open defect O2 always resulting in a readout equal to "1" since the RD transistor remains *off*.

2) Resistive open defect O2

The effect of a resistive O2 is presented in this subsection. Figure 15 shows the circuit resulting from the inclusion of a resistance modeling for the open defect

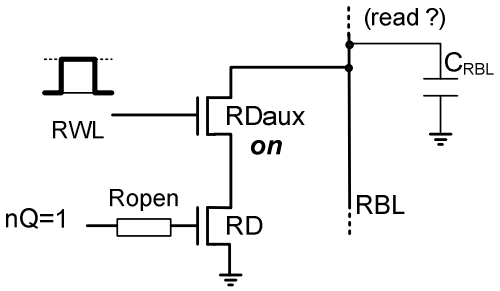

Figure 15 Resistive open defect O2 at the gate terminal of RD transistor.

Figure 16 shows the electrical behaviour of the cell with different resistive O2 defects higher than 300MΩ. As shown in the figure, the voltage at RBL node remains high and an (incorrect) nQ=0 is read. Resistances below this critical value (Rc) lead to a correct read operation R0 of the cell state.

Figure 16 Incorrect readout of Q=0 due to O2 with resistance higher than 300MΩ. The write and read actions are the same as in Figure 14.

However, the erroneous or correct effect of resistive open defect O2 on the read action of a cell depends not only on the resistance of the defect but may also depend on the previous write operations performed on the cell. In order to illustrate this fact, Figure 17 shows the defective circuit analyzed in Figure 16 but now with a particular Ropen=300MΩ. Figure 17a and Figure 17b illustrate the response of V_{FN} and V_{RBL} for different writing actions preceding R0. The same circuit may result in a correct or incorrect R0 depending on the time Q and nQ have been stable before the read action.

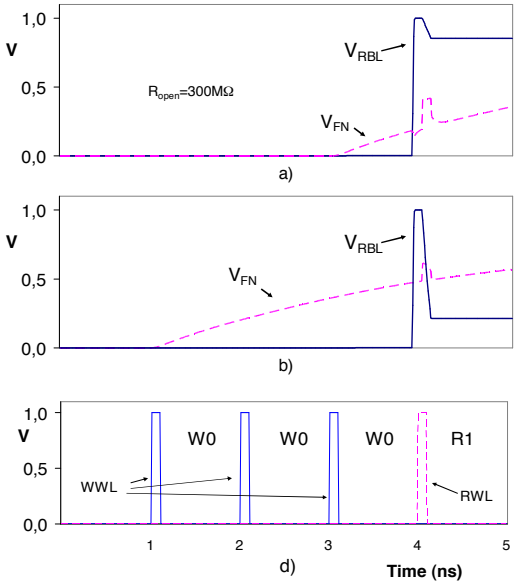

Figure 17 Circuit of Figure 15 with a particular Ropen=300MΩ and with different write sequences prior to R0: a) W1-W1-W0 (as in Figure 14) and b) W0-W0-W0 (as shown in d).

C. Open defect on the direct path of the read port O3

1) Full open defect on the direct path

Full open O3 and their equivalent opens (see Figure 18), cause the RBL to always remain precharged since the direct path to ground is completely broken. R1 is always correct.

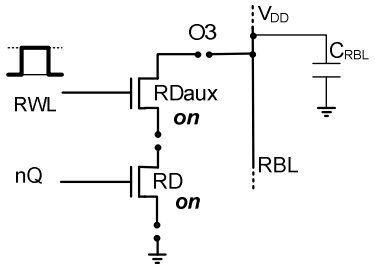

Figure 18 Full open defects on the direct path of the read port. The read operation result is Q=1 since the RBL can not be discharged.

2) Resistive open defect on the direct path

Resistive O3 and their equivalent opens (see Figure 18) may allow the discharge of C_{RBL} depending on the resistance of the defect Ropen as illustrated in Figure 19. In this example, resistances below critical Rc=25kΩ allow the discharge of RBL and result in a correct, but degraded, R0.

Figure 19 Resistive open defect O3 on the direct path of the read port with resistances between 1kΩ and 25kΩ.

IV. DEFECTIVE BEHAVIOUR CLASSIFICATION

According to the defective behaviour presented so far for an 8T SRAM cell with open defects at the read port, some detectability conditions can be derived. Note that the cell works properly as far as the writing operation is concerned. Only the read operation may result in an erroneous readout. TABLE I. summarizes the behaviour of the cell with the open defects presented in the previous section. The read action on Q=0 results in different behaviours as shown in column R0. R1 is always correct. The influence of an aggressor cell on a victim cell is listed in TABLE II.

TABLE I. READOUT OF AN 8T SRAM CELL WITH OPEN DEFECTS VS THE RESISTANCE OF THE OPEN (ROPEN) RELATED TO THE CRITICAL RESISTANCE OF THE DEFECT (RC). * INDICATES A TIMING CONDITION

		Q	R0	R1
O1,3	Ropen≤Rc	0	ok (degraded)	
	Ropen>Rc	0	incorrect	
O2	Ropen≤Rc	0	ok (degraded)	
	Ropen>Rc	0	ok (degraded) / incorrect *	
O1,2,3	-	1		ok

TABLE II. VICTIM CELL BEHAVIOUR DUE TO A FULL OPEN O1 IN THE AGGRESSOR CELL

Defective (aggressor) cell	Defect-free (victim) cell		
Q_{ag}	Q_{vic}	R0	R1
-	0	ok	
0	1		ok (degraded)

V. CONCLUCIONS

The defective electrical behaviour of an 8T SRAM cell with full and resistive open defect has been analyzed. Due to the similarity between the classical 6T SRAM cell and the 8T cell, only defects affecting the read port transistors have been considered. It has been shown how an open in a defective cell may influence the correct operation of a victim cell sharing the same read circuitry. Also, it has been shown that the sequence of bits written on the defective cell before the read action may mask the presence of the defect. Different orders of critical resistance have been found, namely, units of MΩ for O1, hundreds of MΩ for O2 and tens of kΩ for O3. The presented electrical characterization is a preliminary step to the identification of testability and diagnosability conditions of the defective cell. A 45nm technology has been used in this work.

ACKNOWLEDGMENT

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