A NCL-HDL Snake-Clock Based Magnetic QCA Architecture

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***Abstract*—The International Technology Roadmap of Semiconductors suggests that Quantum Dot Cellular Automata technology might be a possible CMOS substitute. In particular, Magnetic Quantum Dot Cellular Automata (MQCA) have recently drawn the attention of the researchers. Previous experimental works have demonstrated that MQCA are feasible, and can be fabricated with existing technological processes. They are also attractive due to their compactness and to an extremely small power dissipation. Unlike in previous contributions, where architectural blocks are often presented without or only slightly considering their relations with technology, here we conceived, implemented and described a complex MQCA computational block maintaining a clear link with technology.**

This link is achieved at different levels. At an architectural level we propose the use of delay insensitive Null Convention Logic^{TM} (NCL, [1]). It is implemented for magnetic QCA in order to solve the "layout=timing" problem in the specific case of Magnetic QCA. We thus describe an architectural block at system level using a Hardware Description Language (HDL). This NCL-HDL idea is adapted to a new structure, which we have called "snake-clock", proposed as a feasible solution for the problem of clock delivery, essential for MQCA operations. Furthermore we demonstrated by means of accurate micromagnetic and finite element method simulations that the three-phase "snake-clock" NCL structure works correctly.

***Index Terms*—Quantum Dot Cellular Automata, Magnetic circuits, Magnetic simulation, Null Convention Logic, GLobally synchronous Locally Asynchronous, VHDL model**

I. Introduction

Among emerging technologies, QCA are a credible alternative to CMOS [2]. They rely on logic states, rather than on conduction. Molecular and magnetic implementations are recognized as the two most promising ones in literature. Experimental evidence has proved the feasibility of magnetic implementations, while molecular implementations, though expected to outperform the magnetic, are far from any promising demonstration of feasibility in the near future. In general, QCA are defined as bistable cells coupled through electromagnetic forces. In the case of micro-magnetic implementation, single-domain nanometer pills-shaped magnets exhibit two stable magnetic states, "up" and "down", due to their aspect ratio (figure 1). These two configurations are associated with the binary information "1" and "0" respectively, and can be transferred from one nanomagnet to the next one by a "domino" effect, provided that specific geometrical and technological properties are present.

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Several works have been proposed in recent years on detailed physical nanomagnets behavior analysis [3] and on architectures and circuits [4]. Both types of approach are independently accomplished. Experiments are carried out by technologists to demonstrate the feasibility of the MQCA idea, while the work done by architects aims to demonstrate that, if the technology works, computation is feasible, and many of the traditional CMOS based digital implementations can be adopted. We believe that working separately with either of these approaches is not successful, especially if we have in mind the CMOS success story to date. Only by linking technology and architecture designers are able to survive in the complex Ultra Deep Submicron reality of today. Moreover, the current scientific MQCA scenario calls for connectedness between circuit design and technology in order to demonstrate the feasibility of the MQCA computation paradigm.

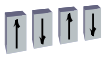

Fig. 1. Pill-shaped nanomagnets in a stable magnetization configuration.

The methodology we suggest uses both a mix of architecture and technological implementations, improving the way in which MQCA are currently studied. Our approach starts by assessing a practicable and non theoretical implementation for MQCA, and therefore constraining the circuit design on this idea. We try to solve problems arising from technological limitations, and at the same time to describe the architecture at circuit level including the information obtained from a real implementation. In this way, realistic circuit performance can be estimated and feedbacks to technologists can be suggested. The methodology is based on the simultaneous use of three simulators. They support circuit level HDL simulations (Modelsim [5]), magnetic pills interaction analysis based on Landau-Lifshitz-Gilbert (LLG) models (Magsimus [6]) and the relations among current, magnetic field and magnetization using the finite element analysis (Comsol multiphysics [7]). The result of this approach is a more efficient step down to physical implementation. Moreover the circuit description can be enriched using the obtained technological data. We are indeed setting up experiments to validate and refine our model with real data.

In this paper we show the preliminary results of this approach. A state of the art analysis and our methodology overview is reported in section II, while in section III the fundamental technological hypotheses are explained. In section

IV an example of circuit description is given with a specific architectural solution adopted and with the "low-level" details added to it. An example of NCL-HDL architecture is shown in section V together with comments on simulation results.

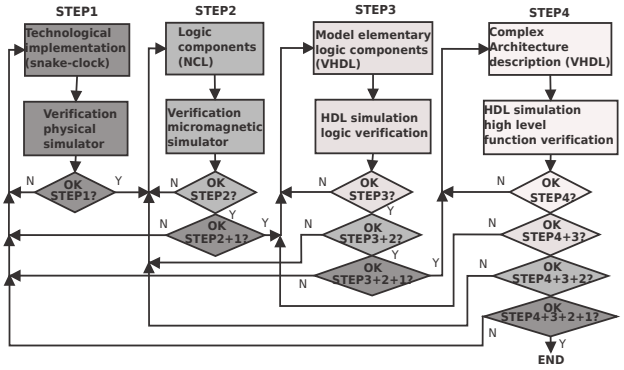

Fig. 2. Flow diagram of the proposed methodology organized in four steps: Technological implementation (1), logic components definition (2), HDL model of logic components (3), architectural HDL description (4). Each step requires a validation through a proper simulator. Progresses from one step to the next is subject to this validation and may require a feedback not only to decision on current step, but on previous ones as well.

II. MQCA BACKGROUND AND PROPOSED METHODOLOGY

Since the introduction of the QCA concept [8], specific attention has been focused on Magnetic QCA [9][10]. Several experiments have proven the feasibility of the idea using up to date technology [11]. Furthermore, manifold theoretical studies have analyzed MQCA power consumption [12]. The power consumption, under certain conditions, is expected to be very small even at room temperature. A design perspective is at the basis of numerous works (see for all [4][13] and [14]). Circuits and architectures are explored irrespective of the technology implementation, or in some cases, analyzed taking into account their reliability issues (see for all [15]). From the methodology point of view, the works [16] and [17] propose to adapt the standard CMOS top down design style to QCA circuits. The circuit behavior is described using Hardware Description Language (HDL). These descriptions are based on several abstraction degrees and include clocking methodologies and effects of fault injection. In our work we rely on this method. All these works approach QCA study and design from many perspectives. However, they do not link circuit and methodology with technology and real implementation. We believe that it is mandatory to solve this point to make a substantial step forward in the demonstration of QCA as a possible beyond CMOS technology.

One valid attempt has been proposed in a few works [18][19], where the "layout=timing" problem is addressed. Due to this problem the correct behavior depends on layout, i.e. on the number of magnets used to route a signal. The number of magnets, on its turn, is a function of the number of clock phases it goes through (see next section for further details on clock). In this technology, the placement of magnets aware of the "layout=timing" problem is in principle feasible, but it is unmanageable even for circuits with a few gates. The solution proposed in the cited works is based on the Null Convention Logic^{TM} (NCL) approach [20][1]. It was originally born for CMOS asynchronous design and consists in adopting a Locally Synchronous and Globally Asynchronous (GALS) philosophy. GALS solutions have been recently proposed in CMOS based architectures for solving the critical aspects related to the interconnects delay [21] or different synchronization systems [22]. In the NCL solution each logic gate is transformed into a more complex structure. Here the processing data relies on an acknowledge signal which assures data validity. This means that only when this signal is valid the information is transferred from one logic stage to another. Bearing this idea in mind we have built a library of NCL gates and described them using VHDL. The architecture can then be described and simulated at the high level. In the same time, it intrinsically solves a technological problem and represents thus a novelty in the state of the art.

Another important aspect related to MQCA is the impossibility to cascade a great number of magnets, since a long sequence of magnets will be subject to errors in the information propagation [23]. Moreover it has been demonstrated that one nanomagnet can influence a neighbor magnet only if this starts from an unstable magnetization state. This means that an horizontal magnetization state, different from the "up" or "down" stable magnetization state, must be reached. The solution consists in organizing magnets in groups, each related to an external magnetic field, i.e. a "phase". This field will be able to "reset" the magnet state to the unstable horizontal magnetization (see next section for a detailed explanation). This concept was proposed in [3] and four phases were shown as a possible solution to allow the propagation of information in all the directions of the circuit plane. In [24] similar analyses were performed and an alternative proposal for the external field distribution is reported. Though in theory the proposed system could work, in practice a specific external field independently controlled for each nanomagnet is not realistic, as it would imply to deliver one "phase" for each magnet. This would be unfeasible, especially if the information propagation is not monodirectional, as it is expected in real cases. Preliminary proposals on how to really generate this field, called "clock", are in [25][26][27]. Only in our work in [28] and [29], and later for some aspects in [30], a feasible structure is proposed, called "snake-clock", delivering three overlapped external phases. In this paper we show how the structure works and how we modeled, using VHDL [5], the NCL block including the "snake-clock" organization. We also validated our hypotheses [31] using both an accurate magnetic simulator [6] based on LLG model and a finite element method solver [7]. The model includes technological related aspects, and is thus a unique proposal in current literature scenario.

The proposed methodology can be summarized according to the flow in figure 2, which will be referred to in the following sections. It is organized in four steps, each requiring a validation phase. As a result, the design phase may require variations not only to the decisions related to the present step, but also to previous ones. In STEP1 the technology implementation scenario is identified: in our case the "snake-clock". STEP2 entails the study of the proper logic components that can be adapted to the STEP1 choices: in our case the

NCL gates combined with the 'snake-clock" organization. In STEP3 the elementary logic blocks are modeled using HDL, taking into account the results from previous steps. Finally, STEP4 consists in designing a complex architecture using the incremental validation results matured up to this point.

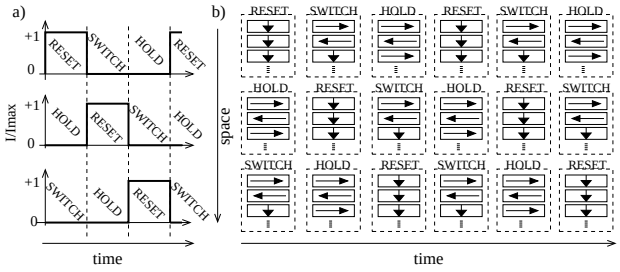

Fig. 3. Left: Clock signal on three phases delivered to three different zones in space and repeated in time following the Reset, Switch and Hold sequence. Right: logic organization of nanomagnets in time and space following the clock signal sequence (Reset, Switch and Hold).

III. THREE PHASES CLOCK (STEP1)

As previously mentioned, a few works in literature (see for all [12]) demonstrated that for Magnetic QCA, as well as for molecular QCA, an adiabatic switching could assure a correct information propagation. This means that the switching of a nanomagnet from the state "up" to the state "down" is favored if an intermediate state is reached first. An external field must be applied so that the pill "memory" (the previous magnetization "up" or "down" state) is erased (the magnetization becomes horizontal and thus perpendicular to "up" or "down" direction.) As soon as the external field is released, an input can force the new "up" or "down" magnetization to the pill more easily and with lower energy. This is particularly important when the input of nanomagnet-B is another nanomagnet-A, which can force on the coupled nanomagnet-B only a limited magnetic field due to its intrinsic characteristics (shape and material).

This external field acts as a clock, because it is iteratively switched on and off and because it enables the evaluation phase, even though it has not the "traditional" function of a clock signal. The multiphase clock organization in phases requires complex structures. In this work, starting from [25], [28] and [29], we propose a solution to the clock distribution problem, which we have called "snake-clock" (STEP1 of our methodology flow). It is more feasible with respect to other solutions previously proposed for the multiple-phases clock distribution. It should be noted that this multiple phase distribution is crucial to guarantee the information propagation without errors in complex nanomagnets arrays. Phases are three, differently from the four ones previously introduced. In figure 3.a the RESET, SWITCH and HOLD sequence is shown both in the time and the space axes. In figure 3.b the behavior of nanomagnets grouped in the correspondent clock zones is depicted. Each clock phase should serve a group of pills and not a single magnet. This is due to the unavoidable size difference between the pills and the metal line which generates the signal. When a cell group is in the HOLD phase the pills are in the stable "up" and "down" states which store the digital information. These magnets behave like an input for the neighbor group which is in the SWITCH state. This

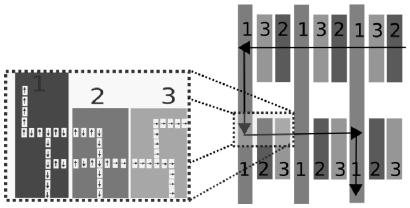

Fig. 5. Snake clock logic structure: information propagation through different clock zones following sequence 1-2-3. Magnets in phase 1 can deliver the information both vertically and horizontally, while magnets in phase 2 and 3 propagate the information horizontally only. In the inset an example of magnets layout is sketched. Magnets are not placed in the horizontal gap between phase 2 and 3: There wires are routed diagonally, and the magnets would be subjected to two phases in the same time.

means that the previous state of these switching pills has been already "cancelled" due to a reset, and now they are ready to be influenced again. The group in the following region is itself in the RESET state. In figures 4 and 5 the "snake-clock" structure is represented. The layout and physical views are in figure 4 both in the top (left) and 3D (right) perspectives. The nanomagnets arrays can be sandwiched between two thin oxide layers. Metal wires carrying the clock signal can be routed on the top and bottom of this structure. One stripe (phase 1) can be straight, while the others (phases 2 and 3) should be routed in a zig-zag style, twisted, but belonging to two different metal layers. In this case, for example, phase 2 is routed in the same plane with phase 1, while phase 3 belongs to the bottom plane. Active nanomagnet pills cannot be placed in zones where metal wires are oblique because there they would be subject to the fields generated by two crossing wires. In figure 5 the top "logic" view of the clock zones is sketched

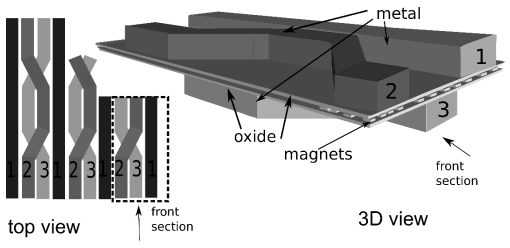

Fig. 4. Snake clock zones and phases layout. Left: top view. Right: 3D lateral view. The 3D view front section corresponds to the 2D detail evidenced by the dotted rectangle. Phase 1 is delivered through a straight line on upper plane. Phases 2 and 3 are twisted, but are routed on different planes: phase 2 is on the same plane of phase 1, phase 3 is below the lower plane. Nanomagnets are sandwiched between two oxide layers; they are visible in the section between the two planes. Magnets cannot be placed where wire 2 and 3 are diagonal.

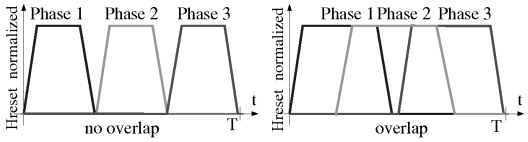

Fig. 6. Reset field showing a realistic slope. Left: non overlapping phases. Right: overlapping phases, preferred for a correct information propagation.

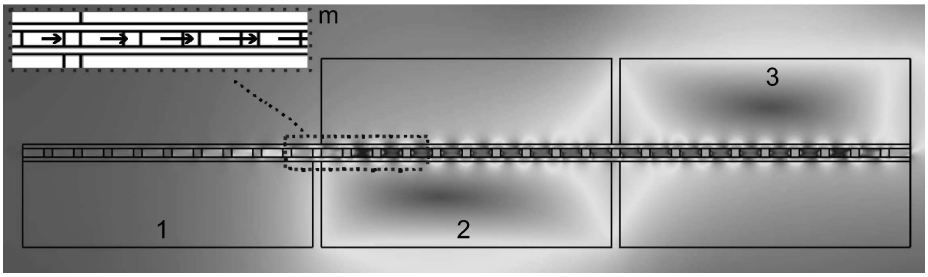

Fig. 8. Finite elements simulation (Comsol Multiphysics) of the snake clock structure in the case of overlapped phases 2 and 3. A section view of the structure shows a wire of consecutive nanomagnets between two oxide layers and the section of wires which deliver the clock. To each of these wires 10 nanomagnets are associated. A current is injected in metal wires correspondent to phases 2 and 3 (entering in the plane of the figure) and as a consequence a magnetic induction appears (different gray levels are related to the magnetic field intensity). The figure inset shows the correspondent magnetization (arrow length is proportional to the magnetization strength).

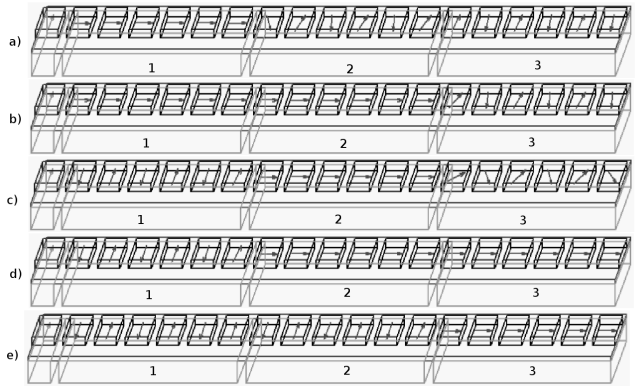

Fig. 7. Nanomagnet wire information propagation: three phases partially overlapped. a) Reset on first zone; b) reset on first and second zones; c) reset on second zone; d) reset on second and third zone; e) reset on third zone.

without the areas where phases 2 and 3 are crossed, as in those points magnets are not presents. The information flow is also depicted in the figure. As underlined by the arrows, this clock organization still allows the information flow in both the horizontal and vertical directions (as assured by the previously proposed four phases). However, the correct phase sequence (1,2,3 in figure) must be guaranteed, therefore, only a "snake" like propagation is possible. Even if this seems a limitation, this structure is feasible with technology processes currently available, differently from previously proposed solutions.

As mentioned before our aim is to maintain a clear link to technology and to a realistic implementation. For this reason we analyzed more in details the clock signal organization and behavior. The reset field is assured by a current flowing through each clock wire. A realistic current signal is more similar to the one in figure 6.left than the one previously shown in figure 3. Moreover, we have demonstrated [31] that the three phases should be overlapped as in figure 6.right in order to assure a correct information propagation.

Results are shown in figure 7, where a MQCA wire has been simulated using a LLG based magnetic simulator [6] which allows a 3D dynamic simulation (validation of STEP1). Nanomagnets sizes are $50X100X20nm$ (width, height, thickness), the distance between two of them is $20nm$ and they are made of Cobalt. The nanomagnet wire is organized in three parts corresponding to three clock zones (1,2,3) which generate the reset signal according to the overlapped phases (as in figure 6). In this simulation, for simplicity of representation, the clock wire is below the magnets layer in all the three phases. The behavior, in fact, does not change if the external field signal is above them and positioned at the same vertical distance as in figure 4 right. The reset signal is an external magnetic field which forces a magnetic induction of at least 4mT [26]. Figure 7 shows the information propagation through three phase zones in a sequence of five conditions (snapshots of a continuous time varying simulation). The reset is applied in sequence on zone 1, then 2 and later 3 with overlap according to figure 6.right. The initial magnetization state is random in each phase domain. Basically, to assure the correct information propagation, before cutting off the reset field from a zone (e.g. zone 1 in subfigure 7.a) it is necessary to apply it to the magnets of the neighbor zone (e.g. zone 2 in subfigure 7.b). In this way, once the magnets in the previous zone are free from reset (e.g. zone 1 in subfigure 7.c), they can be influenced by the input, as for example other magnets in a hold state on the left. This happens without the interference of dots in the following phase (e.g. zone 2 in subfigure 7.c). If this is not done and the reset field is shifted from zone 1 to zone 2 without overlapping, the magnets in zone 2 could still have a vertical magnetization. As a consequence they could influence backward the magnets in the switching state [31]. A sequence similar to the one just commented allows the information propagation from zone 2 to zone 3.

To verify the feasibility of this sequence we simulated the magnetic field effects using Comsol multiphysics [7] (validation of STEP1). The magnetic field was generated by the current flowing through clock metal wires. We analyzed the magnetic induction and the magnetization; however, Comsol does not include LLG model to analyze interaction among magnets, but easily allows to define time varying currents in a wire and to measure inductions and magnetization on nanomagnets. At the same time Magsimus does not allow to simulate a current in a wire, but permits to generate an external magnetic field on different zones. For these reasons we used both the simulators.

The Comsol simulation results are shown for a case of overlapping phases in figure 8. Wires are labelled with numbers 1, 2 and 3, and in this example phases 2 and 3 are subject to current. A sequence (wire) of nanomagnets (10 magnets

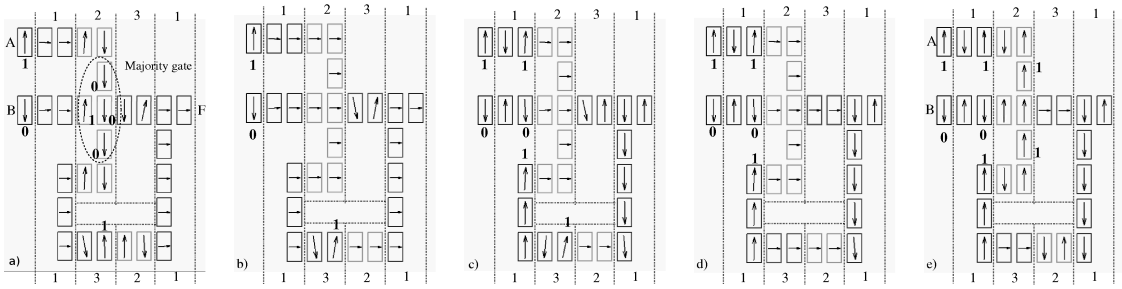

Fig. 9. NCL TH22 logic gate magnetic simulations using Magsimus [6] considering the proposed snake-clock organization. Phases zones are labelled with numbers 1,2 and 3. Inputs are A and B and output is F. a) Reset field applied to phase 1, while magnets on phases 2 and 3 are in a random state; b) Reset is applied to phases 1 and 2 (overlapping); c) reset is released from phase 1 and applied to phase 2 only; d) reset is applied to phase 2 and 3 (overlapping); e) reset is released from phase 2 and applied to phase 3.

TABLE I
DISTRIBUTION OF INDUCTION IN THE CLOCK WIRE OF PHASE 2 (ACCORDING TO FIGURE 8). MAGNETS ARE NUMBERED FROM LEFT TO RIGHT IN PHASE 2. MAGNETS FROM 1 TO 5 CORRESPOND TO THE INITIAL (LEFT) TO THE CENTER OF THE WIRE OF PHASE 2. MAGNET LABELLED AS -1 IS THE LAST IN THE PREVIOUS PHASE.

	Induction on nanomagnets [mT]					
Metal Thickness	Prev. phase	Current phase				
h	-1	1	2	3	4	5
100nm	1.8	2.8	3.4	3.7	3.8	3.9
200nm	3.6	5	6	6.5	6.8	7
300nm	5.2	6.8	8.2	8.9	9.3	9.6

for each phase) is separated from the metal wire by a thin oxide layer ($t_{ox} = 10nm$) on both sides. The current generates a magnetic field which magnetic induction is distributed in the surrounding space (visible by a gray gradient). The correspondent magnetization direction and amount (proportional to the arrows length) is clear from the detail shown in the figure top-left corner (m box). Table III shows the specific values of the magnetic induction in the magnets along the wire in zone 2. Magnets are numbered from 1 to 5 only (left to center of phase 2), as the others, from 6 to 10 (center to right of phase 2), have symmetrical behaviors. The values in this simulation are reported as a function of the clock metal thickness (h). The current density is constant and is equal to $J = 10^6 A/cm^2$. In [26] the authors demonstrate that an induction value of $B = 4mT$ is enough to force a reset in a nanomagnet of the same size. We want to reach this value for the magnets in the interested reset zone, but not in the neighbor zone (magnet number -1 in the table). Clearly the best thickness is the second one, i.e. 200nm. In fact a 100nm thickness does not assure enough current to generate a sufficient induction. On the contrary, the 300nm one would cause an induction bigger than the limit also in the neighbor zone (-1). As a consequence the clock structure and phase sequence can correctly work. Moreover, it is feasible with current technology [27], but, clearly, proper analyses should be performed to give feedbacks to technologists (feedback from STEP1 validation in the methodology flow).

IV. SNAKE-CLOCK NCL-HDL MQCA DESCRIPTION

The proposed clocking structure is the starting point for setting up a QCA architecture. However, the "layout=timing" problem must be tackled.

A. Layout=Timing and Null Convention Logic (STEP2)

Using a 3 phases clock to drive the propagation of information in the QCA circuit leads to a simple practical consequence. Each sequence of 3 clock zones, from 1 to 3, has the same behavior of a latch, as the output copy the input at every clock period. For this reason we say that a QCA circuit is intrinsically pipelined. As a result, the propagation delay of a QCA signal depends on the number of clock zones it traverses. Therefore it depends on the layout of the circuit. In the case of simple gates an accurate control of wire layout is feasible. On the contrary such a constraint cannot be met in complex structures. In other words, it is not possible to assure that two signals which are inputs of the same gate will traverse the same number of phases. They could in fact been routed starting from their own drivers, which might be placed at very different distances.

One possible solution is the use of a delay-insensitive logic, the Null Convention Logic^{TM} [19], proposed for QCA in [18]. In the NCL logic every bit is coded using 2 bits. The signal can be either in the DATA state (01 for a logic "0" or 10 for a logic "1") or in the NULL state (00), while the state 11 is not allowed. The delay-insensitivity is assured because, if the circuit is in the NULL state, it moves to the DATA state only when every signal steps from NULL to DATA. In the same way, when the circuit is in the DATA state, it moves to the NULL state only when every signal has changed from DATA to NULL. Even if the input signals change with different timing due to the circuit layout, the device still works, and the "delay=timing" problem is solved.

B. NCL magnetic implementation using snake clock (STEP2)

We adapted this solution to our snake-clock structure and designed the layout of every NCL gate on the basis of the snake-clock requirements. According to [20] there are 27 NCL basic gates with at most 4 inputs. One of the simplest is the TH22 cell with logic function reported in equation 1:

$$F = AB + F(A + B) \quad (1)$$

If the output of the gate is initially 0, it changes to 1 only if both the inputs A and B go to 1. On the contrary, if the output is initially 1, it goes to 0 only if both A and B change to 0. The NCL gates have a peculiar naming convention which is worth explaining. These gates have an intrinsic threshold suggested

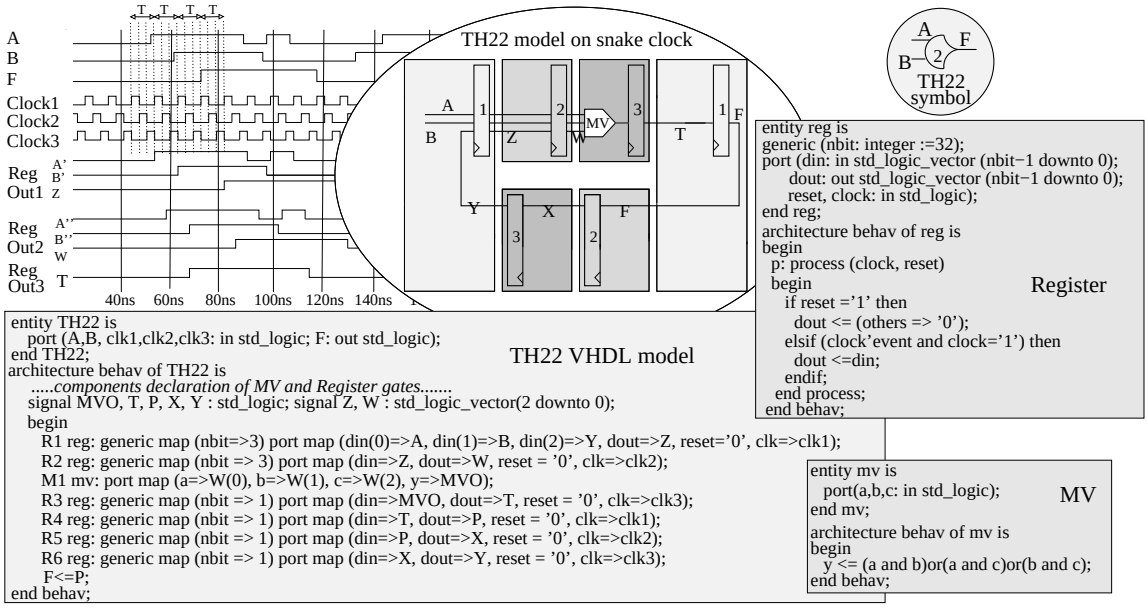

Fig. 10. TH22: symbol (top right), model based on the three snake-clock zones (center in the elliptical region) simulation (top left) and VHDL description in the boxes for a single register (reg), the majority voter (MV) and the whole gate (th22). T is the period spanning three clock "high pulses" T_H due to the three clock phases: $T = T_{HClock1} + T_{HClock2} + T_{HClock3}$. Here a case without overlapping is reported for simplicity.

by the TH in the gate name. This means that the gate switches from 0 to 1 only if a certain number of inputs change from 0 to 1. The second number in the NCL gate name represents the total number of inputs, while the first number represents the threshold, i.e. the number of inputs necessary to cause the switching of a gate. Therefore, in the TH22 cell two are the inputs and both must flip from 0 to 1 to assure an output switch. The TH22 gate function can be rewritten as in eq. 2

$$F = AB + FA + FB \tag{2}$$

The logic function above describes a majority gate Z=AB+AC+BC. This is also called majority voter (MV) and it is the elementary logic block of a QCA circuit [3]. For a TH22 cell the output of the MV is also connected to one of its inputs. We have designed the TH22 layout on the basis of a snake-clock structure as shown in figure 9 under the hypothesis that the width of every clock zone is equal to two nanomagnets (just for example). Inputs A and B acts in this simulation, which is the validation of STEP2 in our methodology, as permanent magnets placed externally and connected to the wires in clock zone 1. The majority voter (dotted box in figure 9.a) is in zone 2, and its output (central "down" arrow) is immediately connected to zone 3. The global output F in zone 1 is also fed back to the third input through zone 1, which allows vertical propagation, and then through zone 2 and zone 3 in the other clock island in the bottom of the figure. The simulation performed by Magsimus is dynamic. Noteworthy snapshots of the TH22 computation are here reported according to the overlapping phases. In the key-points we superpose "1" to up arrows and "0" to "down" arrows for an easier explanation.

At the beginning of the simulation (figure 9.a) all the magnets in zones 2 and 3 have a random magnetization state, while the magnets in phase 1 are in the reset state (horizontal arrow). The central majority voter has initially a zero output (the central magnet in the ellipsis). As there is a feedback, it is important to note that the initial (random) feedback value in phase 3 at the bottom is "1". After this initial step, the reset field is applied to phase 2 but still phase 1 is active (figure 9.b) due to the overlapping clock behavior. When the overlapping time ends and the reset field of phase 1 falls to 0 (figure 9.c), then the correspondent nanomagnets are free to switch. They change state according to inputs A and B and to the initial value of the feedback ("1"). The magnets switch in the correct order (1, 2, 3), from left to right in the upper part of the figure and from right to left in the bottom part. This happens because magnets in phase 3 and input cells are in the hold state, while the dots in phase 2 are in the metastable reset state. In this situation the three inputs to the majority voter in phase 1 are two "up" ("1") and one "0" (down), so the majority voter output is expected to go to "1". At this point the magnetic field is applied to the magnets in phase 3 (figure 9.d), while phase 2 is still under the influence of the reset field. When it goes to "0" (figure 9.e) the correspondent nanomagnets switch to a data state, as zone 1 magnets in previous sequence. The MV output is up ("1") as expected.

This simulation demonstrates that TH22 gate implemented with magnetic QCA and using the snake clock works properly, the reset sequence propagates correctly and logic values are as expected. The combination of NCL logic and snake clock can thus be successfully applied to QCA. The only constraint is that inputs must be stable at least for the time it takes the signal to propagate through the feedback. Though further analyses should be performed in order to determine whether this is a penalty, we can assess, on the basis of our simulations at higher level, that this is automatically guaranteed (feedback from STEP2 validation). In fact, the time necessary to pass through the whole circuit is always bigger than the time necessary to

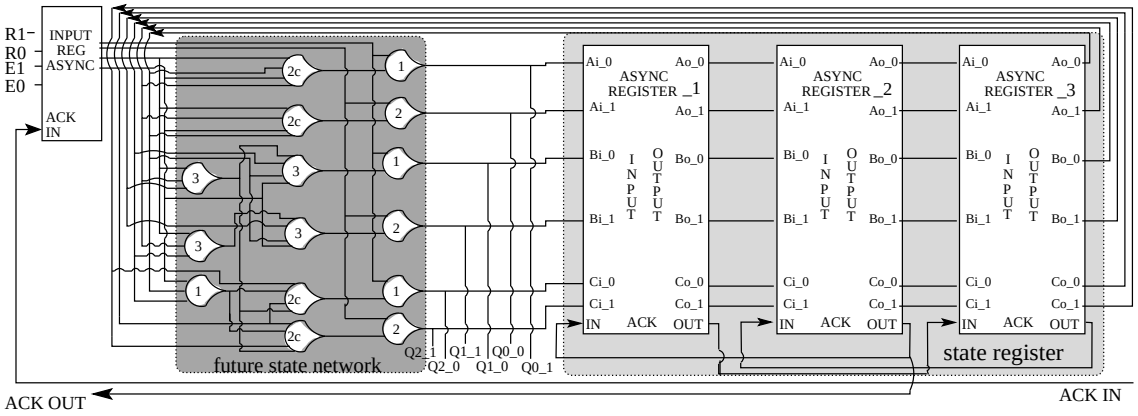

Fig. 11. NCL 3-bit counter architecture based on Magnetic QCA. Light gray box represents a 3 bits register given by three 3 bits asynchronous NCL registers [20]. Dark gray box includes the future state network. Numbers in NCL gates (e.g. "1", "2", etc.. state for various types of NCL gates performing different logic functions and based on different numbers of input net.)

pass through the local feedback. A further analysis should be performed to define the correct number of magnets in a phase that for this gate assure a correct behavior, giving a feedback to STEP1 (not done here as out of focus.)

C. Snake clock NCL-HDL logic gates modeling (step3)

Micromagnetic simulators cannot be used for complex Magnetic QCA NCL circuits, because they can efficiently simulate only a small number of nanomagnets (a few gates). As a consequence a different approach has been adopted. After the detailed analysis and characterization using magnetic simulators, we modeled the snake-clock NCL behavior using an high level description language (VHDL), approaching thus STEP3 in our methodology.

As explained before, the behavior of three consecutive clock zones is similar to the behavior of three consecutive registers. The clock of each register is a signal that has the same characteristics of the reset field. So it is possible to describe the QCA circuit using an equivalent RTL model. It consists of the necessary boolean logic functions (the Majority gate function in the TH22 gate case) added to a register for each clock zone. TH22 behavioral model is shown in figure 10 in its many views: The gate symbol (top right), the model (center), the output simulation (top left) based on Modelsim simulator [5] and the VHDL description of the single components (register and majority voter) and of the whole gate (th22). The majority voter is substituted with an equivalent logic circuit with zero delay (until detailed information are not derived from technology). The propagation delay due to the clock is simulated with one register for each clock zone, as evidenced by the *port map* statement in the VHDL model. The simulation results in figure 10 (left), reported in the case of non overlapping phases for sake of simplicity, confirm the expected behavior (validation of STEP3). Only when the inputs A and B goes both to 1, after a delay of 1 clock cycle the output F changes from 0 to 1. It is worth noticing that one clock cycle corresponds to the time necessary to pass through three clock zones, and thus to the sum of the three "high pulses" T_H of each clock phase $T = T_{HClock1} + T_{HClock2} + T_{HClock3}$. The output maintains its status until every inputs go to 0, and then the output changes from 1 to 0 after 1 clock cycle. Signals A', B', A", B", Z and W are A, B and Y replicas just shifted of $T_{HClock1}$ and $T_{HClock1} + T_{HClock2}$, respectively. Signal T is the result of majority voting among A", B" and W. Signals X and Y are the output F shifted on $T_{HClock1}$ and $T_{HClock1} + T_{HClock2}$, respectively (not shown in the simulation for sake of brevity).

V. Architecture: circuit and results (STEP4)

All the NCL gates have been modeled according to the snake-clock magnetic implementation and more complex NCL architectures have been designed (STEP4 of our methodology). Here we show a counter, which represents a good balance between circuit complexity and completeness, as both sequential and combinational gates are included.

A three bit implementation NCL-HDL counter is sketched in figure 11, while simulation results are shown in figure 12 (validation of STEP4). The counter is based on the generic structure of a NCL finite state machine. A memory register (light grey box) is used to store the present state, and a combinational circuit generates the future state (dark grey box). Many NCL gates are used to build this part of the counter. One example is the OR gate, as the TH12 gate (the three blocks with label "1" having two input signals) that has a logic function equal to $F = A + B + F(A + B)$. A similar block is TH13 (the gate with label "1" with three input signals) which implements $F = A + B + C + F(A + B + C)$. Gates performing an AND logic function are also used. One is the TH22 described in subsection IV-B (the gates with label "2" with two input signals). Another is the TH33 (the gates with label "3" with three input signals) that has a logic function equal to $F = ABC + F(A + B + C)$. The TH34 (the gate labelled with "3" with four inputs) has a more complicated equation: $F = ABC + ABD + ACD + BCD + F(A + B + C + D)$. A particular case is the TH24 comparator (the gates with label 2c) which logic function is $F = AC + BC + AD + BD + F(A + B + C + D)$.

NCL registers do not have a memory function. Their aim is to implement the asynchronous communication protocol to guarantee the delay insensitivity [20]. In order to implement

the memory registers needed for our counter we use a 3 bit asynchronous register connected as in figure 11. Each register uses "acknowledge" (ACK) signals to step from one state to another. In this configuration the ACK_OUT signal of every register is connected to the ACK_IN of the previous one. Using this connection the last register in the sequence is always in the opposite state with respect to the others two. It means that when the circuit is in the NULL state, in which every signal is zero, the last register is in the DATA state. Consequently it maintains the present state safely stored. On the contrary, when the last register is in the NULL phase, the new logic state is loaded in the first register. After the propagation of the acknowledge signal, this new state is loaded in the second asynchronous register according to a sort of "master slave like" dynamic. The input register (left top in figure) is used for communication purposes with other blocks. It allows the acceptance of a new input only when an ACK_IN signal is received from the block placed after the counter. Only when this following block is ready, new data are processed by the counter. This happens only when the next block has already received the current value from the counter, and can then step to another DATA phase. The combinational logic (dark grey box) generates the future state starting from the present state at every data cycle. In this case the value of the present state is simply incremented by one if the external "count enable" signals E0 and E1 are active.

Further inputs are the reset R0 and R1. Both of them are doubled to be adapted to the null convention logic encoding. The counter outputs are nodes $Q0\_0$, $Q0\_1$, $Q1\_0$, $Q1\_1$ and $Q2\_0$, $Q2\_1$. The output acknowledge signal of the whole counter, ACK_OUT, is connected to the output of the second asynchronous register. It is the only memory register, and can be used from other blocks preceding the counter. The ACK_OUT signal is generated only when the combinational logic has completed the future state generation.

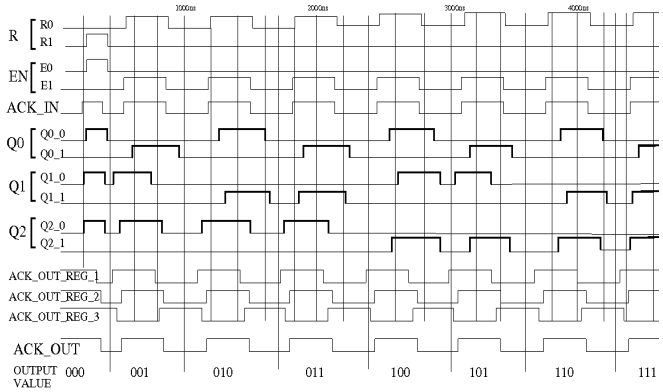

Fig. 12. NCL counter simulation results. Outputs are nodes $Q0\_0$, $Q0\_1$, $Q1\_0$, $Q1\_1$ and $Q2\_0$, $Q2\_1$. They switch from the NULL (00) to the DATA (01 or 10) state. Output values are also reported in the bottom line in digital un-encoded format. The ACK_OUT signal validates outputs.

The counting sequence is underlined in the bottom line of the simulation results in figure 12. As expected all the outputs switch from the DATA state to the NULL state (both the signals in a couple are 0) and viceversa. The bold lines in the figure show when one of the bits assumes a DATA configuration. The entire structure works using clock phases correspondent to the snake clock, not reported here for sake of simplicity. They would appear as in the TH22 simulation (figure 10) as each gate has a specific structure organized in a different number of phase zones. It is worth noticing that output signals are not synchronous, but are generated at different time slots. This is because each gate has a different layout, therefore they have different propagation delays in terms of snake clock phases latency. These delays further demonstrates how NCL logic can solve the layout=timing problem of the QCA circuits. If a problem arises at this point then solutions must be searched not only in the architecture design, but also in previous steps, e.g. refining the model (STEP3), improving the logic choice (STEP2), changing technology constraints due to the "snake-clock" (STEP1.)

VI. Conclusions and future works

To prove the validity of Magnetic QCA as possible substitute of CMOS technology both architectural and technological aspects must be inspected, and their mutual influence explored and exploited. A full magnetic and snake-clock NCL structure has been here demonstrated. It assures promising potentialities for further architectures developments. It solves a critical limitation of MQCA and is based on a practicable clock structure. We demonstrated how it is possible to solve a technological problem at architectural level, and how technology choices can be reflected on the architecture description by adopting proper models. We also proved, by means of detailed micromagnetic simulations, that the three overlapped phases technique, based on snake clock structure, not only is feasible from a practical point of view, but is also reliable in terms of logic functions evaluation. We are currently working to an enrichment of the model in order to include, in a parametric style, power dissipation, timing and fault tolerance due to switching, layout and technological parameters. We plan to further improve these descriptions on the basis of the physical implementation. We believe that on one hand the architecture is in this way more physically meaningful and that variations can be discussed on a technology basis. On the other hand feedbacks to technology solutions can be derived by the analysis of circuits which description is aware of technological constraints. This is the reason why we set up our own experiments, still at the preliminary phase, consisting in the fabrication of arrays of dots [32],[33]. We are now ready to characterize them and to include their real characteristics in our high level model.

VII. Acknowledgements

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