Validation by Measurements of a IC Modeling Approach for SiP Applications

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***Abstract*— The growing importance of signal integrity (SI) analysis in integrated circuits (ICs), revealed by modern system-in-package (SiP) methods, is demanding for new models for the IC sub-systems which are both accurate, efficient and extractable by simple measurement procedures. This paper presents the contribution for the establishment of an integrated IC modeling approach whose performance is assessed by direct comparison with the signals measured in laboratory of two distinct memory IC devices. Based on the identification of the main blocks of a typical IC device, the modeling approach consists of a network of system-level sub-models, some of which with already demonstrated accuracy, which simulated the IC interfacing behavior. Emphasis is given to the procedures that were developed to validate by means of laboratory measurements (and not by comparison with circuit-level simulations) the model performance, which is a novel and important aspect that should be considered in the design of IC models that are useful for SI analysis.**

***Index Terms*— System-in-Package, Modeling, Computer Aided Design, Integrated Circuits, Simulation.**

I. INTRODUCTION

THE highly competitive market of electronic devices imposes the current trend of device size shrinking with simultaneous increase of the number of functionalities such devices are offering. The mobile phones are a typical example of such trend, where the main selling slogans point exactly to their reduced size or weight, to the new functionalities included (for instance, digital camera, wireless communications, higher performance processing units) and also the extended battery autonomy. The latter aspect, i.e., device energetic efficiency, has also an impact in the shrinking trend of the device components [1].

To follow up with the market trends, new technologies are being used or investigated by the IC manufacturer industry, from which is highlighted the System-in-Package (SiP) approach, where different dies [which were previously implemented in distinct integrated circuits (ICs)] are mounted together within the same IC package (either in a vertical, horizontal or mixed arrangement) [2]-[5]. The proximity of distinct dies, sometimes provided by different manufacturers, increases significantly the electromagnetic interaction between the electrical signals propagating through the IC lines, causing interference problems that are very difficult to predict in the design phase of the SiP IC. Also unpredictable are non-ideal behavioral effects of the IC sub-systems, which are usually manifested as bouncing on the ground and power signals, and as perturbation of the analog signals generated by the output drivers of the IC [6]-[8]. Such unpredictability is very expensive for the IC manufacturer because such interference (which sometimes leads to device malfunctioning) is only detected after creating the prototype.

Signal Integrity (SI) analysis is a very important tool to a priori investigate the possibility, or probability, of the occurrence of significant signal interference, thus strongly increasing the success rate of early IC prototypes [9]-[11].

This paper presents the application of innovative SI techniques in modeling the behavior of the most significant components of a memory die, for incorporation in a software simulation package. This modeling approach results in a simulation model specification that allows IC manufacturers to test, through computer simulation, the inclusion of the modeled die within their new SiP devices. It is important to state that circuit-level simulation of the full die, such as SPICE-like simulation, does not provide an efficient solution to this problem. This is due to the complexity of the IC circuits, with a considerable overall number of transistors, which makes the circuit-level simulation highly time-consuming (if not impossible to simulate), and such time is very precious in the IC design and manufacturing line. Thus, the proposed approach is based firstly on the identification of the most significant basic blocks (in terms of impact on SI) of a typical logic IC device – these are the elements that interface the die with the outside world, namely the I/O buffers and the power rails of the I/O buffers and of the IC core. Secondly,

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each basic block is characterized by a behavioral model (or by other feasible modeling descriptors). The resulting models are incorporated into a simulation platform that will handle the joint simulation of the global IC model. Special focus is given to the characterization of the power rail interconnects whose model parameters were determined from laboratory measurements and not from simulation data or vendor information. For this purpose, specific test fixtures were developed which allow the device characterization through a simple laboratory setup, general enough to accommodate the characterization of most dies.

Instead of validating the proposed IC modeling approach against on circuit-level simulations, we have aimed to use real measurements from real IC devices to demonstrate the global model performance. This is an important issue that this strategy wishes to evidence since, although not very simple to implement (and, thus, hardly tried), it validates the model under conditions which are very close to those of real applications, This way, the predictive ability of the model is directly assessed. Recognizing the importance of the process to perform validation by measurements, a strong emphasis is given to the procedures required for such validation. For this analysis, two particular memory ICs were tested: (i) a 66MHz 512Mb NOR flash memory developed by Numonyx, Srl. in 90nm technology – here denominated the proprietary test-case – and (ii) a 133MHz 512Mb LPDDR memory manufactured by a third party company – here identified as the external test-case. For the proprietary test-case, detailed information of the memory IC contents was known an so the respective IC models could additionally be verified according to such information. However, for the third-party test-case, no information was known of the die inner circuits, and so the model validation was checked against the measured waveforms of the device (illustrating the natural SI analysis procedure for the case of incorporation of ICs from third-party vendors, in the design stage of new SiP devices).

The organization of this paper is described as follows. Section II presents the adopted modeling strategy for the IC sub-systems that have impact on the SI analysis. Afterwards, in Section III, a description of the methods developed for extracting the parameters of such models, by means of laboratory measurements, is provided. This includes the description of the developed test fixtures, especially devoted to the extraction of the IC behavioral models. Following, Section IV describes the hardware setup that was considered to test the two IC memory devices, with emphasis on the points that must be taken into account also in the simulation environment. The global simulation model implementation aspects are described in Section V, and the obtained validation results are shown in Section VI, accompanied by a thorough discussion. Finally, concluding remarks are provided in Section VII.

II. Modeling Approach of IC Sub-Systems

A general logic IC device, such as flash memory ICs, can be easily decomposed into the core sub-system (which holds the huge number of minimal-size transistors that perform the logic processing, conducting very small currents), and the set of I/O buffers which are responsible for the interface between the IC core with the outside world. Each sub-system has usually its own power supply network, one for the IC core circuitry – the VDD/VSS power rail - and another for the I/O buffers – the VDDQ/VSSQ power rail. Naturally, more sub-systems can be encountered in modern IC devices, such as IC analog blocks. However, the intention of this paper is to present the concept of the modeling approaches and the respective validation through measurements, and not to be fully extensive in covering all the diverse functionalities encountered in the huge set of logic IC devices.

Following is provided a description of the approach adopted for the modeling of each of the two identified IC sub-systems.

A. Modeling the IC Core Influence

Although the currents along the IC core transistors are amazingly small, the number of transistors that are simultaneously switching in the core (at the pace imposed by the clock signals) is so high that the total current being drained from the IC core power supply shows several spikes of high magnitude. As these spikes have high-frequency components, the IC core power rail (which is a system that was not developed to have a good transmittance for high frequencies) reacts also with voltage fluctuation, producing bouncing of the power and ground signals.

Moreover, the electromagnetic interference caused by such high current spikes propagates to other blocks of the IC such as the I/O buffer traces and I/O power supply lines.

In order to incorporate the effects of the core switching activity on the IC peripheral circuits, independent current sources were considered in the simulation model. As shown in Fig. 1, these are distributed through a passive path to each of the VDD/VSS supply pads of the die. This approach followed that proposed by the Integrated Circuits Electrical Model (ICEM) [12]. Briefly speaking, in this approach, the power delivery network of the IC is described by means of a Norton equivalent where the short-circuit current generator accounts for the internal switching activity of the device and the equivalent impedance accounts for the passive interconnect structure. The above equivalent can be possibly refined when some information on the internal structure of the IC is available and can be effectively used to assume a simplified equivalent circuit of the power network.

The independent current sources of the circuit equivalent are a priori determined either by (partial) simulations (when access to the internal circuitry of the IC core is available), by measurements or by the information provided by the IC manufacturer on the characteristics of core switching activity currents.

As an example, Fig. 1 shows the model structure that was considered to mimic the die internally generated switching activity currents (where the power rail interconnects are represented by lumped series resistors and shunt capacitors, for representation simplicity). This structure has been assumed on the basis of the information on the internal structure of the

IC on the position of the different blocks responsible to switching activity current. The current sources set in parallel were conceived to represent the current signals characteristics for each operation mode of the die – burst read, program and erase. Each operation mode is selected by turning on the virtual switches placed in series with the current generators.

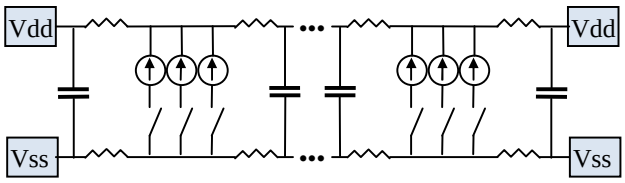

Fig. 1. General topology adopted to model the IC power rail switching currents generated inside the IC core (see text for details).

The power rail network of the IC core is very complex in terms of geometric distribution. As any dc power network, it was designed to supply dc current/voltage to the IC core elements and, thus, it is nearly transparent for very low frequencies. However, when the IC behavior is being analyzed for the purpose of SI assessment, where phenomena such as bouncing and switching activity are being accounted for, it is necessary to model the IC power rail interconnects in a wide frequency range, and not just for these low frequencies.

In the approach considered in this work, the IC power rail interconnects were assumed to be linear dynamic structures that could be mimicked by a cascade two-port networks of lumped elements. Each the ports of each two-port network corresponds to the VDD/VSS pads of the die, and different configurations can be used for these networks – from the traditional T or π impedance network to a black-box approach described by S-parameters. From the preliminary analysis that were performed by simulating the electromagnetic behavior of structures similar to those of the die distributed IC core power rail, it was observed that the dominant effects were that of a longitudinal resistance and a transversal capacitance, as is shown in Fig. 1.

In this work, the characterization of the lumped two-port networks of the IC core power rail will be based on S-parameter measurements at the IC pads, using a vector network analyzer (VNA), as described in Section III.

Figure 2 shows the model used for the IC power rail interconnects, where each port of the lumped blocks correspond to the accessible IC pads or to the inaccessible points of power application to the IC inner elements.

B. Modeling the IC Interface Circuitry

The circuitry that is dedicated to the interface between the inner digital signals and the devices that are external to the die are usually located at the periphery of the die – the I/O buffers. Typically, the power rail network that supplies the I/O buffers has a very simple geometry, which is roughly a set of straight lines passing through each of the individual I/O buffer circuits. Thus, the characteristics of the I/O buffer power rail network are significantly different from that of the core power rail. However, due to the dimensions of the rail and to the fact that its behavior is predominantly linear, the same interconnect modeling approach can be considered for the I/O buffer power network, by representing each segment between a pair of consecutive VDDQ/VSSQ pads through a lumped equivalent passive network. However, as the I/O buffer circuits must also be modeled, and these also impose a loading effect on the power rail interconnects, we propose the use of lumped three-port networks to model the I/O power rail, as it is shown in Fig. 2. In this representation, the power rail considered between two non-consecutive pairs of VDDQ/VSSQ pads (P1 and P2) is a cascade of three-port networks (each defined between consecutive pairs of VDDQ/VSSQ pads, or to any other reference plane of interest). The model adopted for each three-port block consists of a series impedance (*Zs*) between consecutive VDDQ pads, a VDDQ to VSSQ shunt impedance (*Zp*), a capacitance (C_B) mimicking the dominant capacitive effect that the I/O buffer circuit imposes on the power rail and, for generality, an extra impedance was considered for representing the interference between the power rail and the die substrate (it was observed from the measurements performed on the die, described in Section III, that the substrate influence was negligible, and so this extra impedance was not considered).

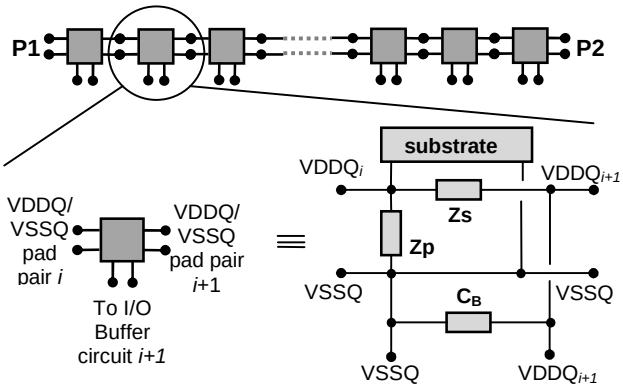

Fig. 2. Lumped structure used to model the IC power rail interconnects. Each lumped block has a longitudinal (Zs) and transverse (Zp) impedances.

Besides the power supply pads, the IC I/O buffers present a pad that is used either as an IC input signal, or as an output signal. In what respects SI analysis, it is far more significant the study of the I/O buffer as an output device than as an input one, because the signal it generates (as an output device) suffers from non-ideal behavior of the I/O buffer circuit and respective interconnects, which other ICs (for instance, in a SiP implementation) will interpret as logical level indicators. Moreover, the output circuit must supply higher currents than the input circuit (implying larger transistors) and the impact of the non-idealities of the input buffer are very reduced when compared to those of the output buffer. Thus, in this analysis the output operation mode of the I/O buffer is analyzed and simulated. Unfortunately, in a general die no access is given to the voltage signal sent by the IC core circuitry to the input of

the I/O buffer. This is why the characterization of the I/O buffer device is usually achieved by relating (by means of a nonlinear dynamic model) its output voltage and output current, in a single port configuration (naturally, subject to a particular logic state of transition at the I/O buffer input) [13]-[16], [21].

Even though any of the already published I/O buffer behavioral models could have been considered in the modeling approach here described (being directly applied into the simulation environment), the I/O buffer models that were used in this work were the SPICE netlists of the I/O buffer circuits which were available for the memory ICs under test. For the proprietary test-case, the back-annotated netlist was created from the knowledge of the circuit schematics of the I/O buffers, while for the external test-case the I/O buffer model consisted on an encrypted netlist with RC back-annotation provided by the IC manufacturer. Notice that the focus of this work is not on the time efficiency of the modeling solution but on the accuracy for SI analysis of a joint modeling approach of the IC main blocks, and since the netlists for both devices were available we decided to used them.

III. Sub-Model Extraction Procedures

For the implementation of the simulation sub-models presented in Section II it was necessary to determine the respective parameters so that they were able to correctly mimic the behavior of the IC devices being tested. Following is a description of the procedures that were considered for the determination of the parameters of such models.

A. Switching Activity Characterization

The simulation of the IC core power rail switching activity was based on the current generator information that each vendor of the tested ICs has provided. For each of the continuous read burst, program and erase operations of the memory ICs, a set of time-domain current source signals was estimated based on partial circuit simulations for the proprietary test-case, and based on the values provided by the vendor for the external test-case. Additionally, two innovative test-boards (one for each test-case) were developed to measure the current activity on the VDD/VSS power rail. The transient current is obtained via the indirect measurement of the voltage drop over a 1Ω resistor that is mounted in series with the ground pad of the power rail. This method, following the standard for the measurement of the conducted emission of ICs in the range from dc to 1GHz [22] has been selected among a limited number of possible alternative techniques, since it is simple to implement and has been proven to demonstrate accurate results in practical applications [21], [23][24]. As an example, Fig. 3 shows the current being supplied to the IC core through one VDD/VSS set of pads during a continuous read burst operation of the latter test-case.

It is relevant to note that the switching activity current like the one of Fig. 3, that is obtained via on board measurements, does not provide directly the current source of a Norton equivalent of the IC core power delivery network. The computation of the current source is a critical step of the modeling process and special care must be taken in collecting, interpreting and processing the measured current data. Readers are referred to work presented in [24]–which focuses on this particular problem, and provides an effective solution to it.

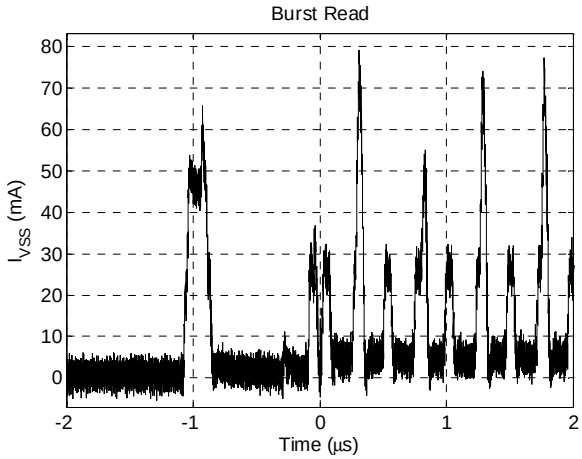

Fig. 3. Example of the measured current on a pair of VDD/VSS pads during a burst read operation of the proprietary test-case.

As each of the test-cases have a considerable number of VDD/VSS pads, distributed along the edges of the dice, the switching activity models adopted consisted of a net of current sources and impedances distributed in accordance with the geometrical placement of the respective die pads. The values of the impedances that are placed between each set of current sources were also estimated by circuit-level simulation for the proprietary test-case, and by the data given by the vendor for the external test-case.

With the above values estimated, the switching activity model was implemented in the simulation environment.

B. IC Power Rail Model Extraction

For the determination of the lumped elements that constitute the model of the IC power rail structures, as given in Section II.B, a series of full S-parameter measurements was performed with the VNA directly probing the die pads. For this case, a wafer with memory dies (one wafer for each test-case) was placed on the probing station and, by means of RF probes [Signal-Ground (SG) and Ground-Signal (GS) pairs], the VNA channels were connected to different pairs of VDDQ/VSSQ and VDD/VSS pads. In order to create a full network of lumped element structures, representing the power rail behavior between every couple of pairs, all combinations of power pads were probed. Additionally, to assess the difference on the dynamic behavior of the power rails, the set of S-parameter measurements was performed for the case of the die with no power applied (here referred as the unbiased case), and for the case where power is supplied to the die (the biased case). For supplying power to the die, either bias-Ts were used with the RF probes, or external dc probes were connected to

the die pads (chip enable and other configuration input pads were also set this way, when necessary).

Figure 4 shows an image of the on-wafer measurement setup and, in Fig. 5 it is a set of the obtained S-parameters for a pair of VDDQ/VSSQ pads, for the proprietary test-case (in both the unbiased and biased cases).

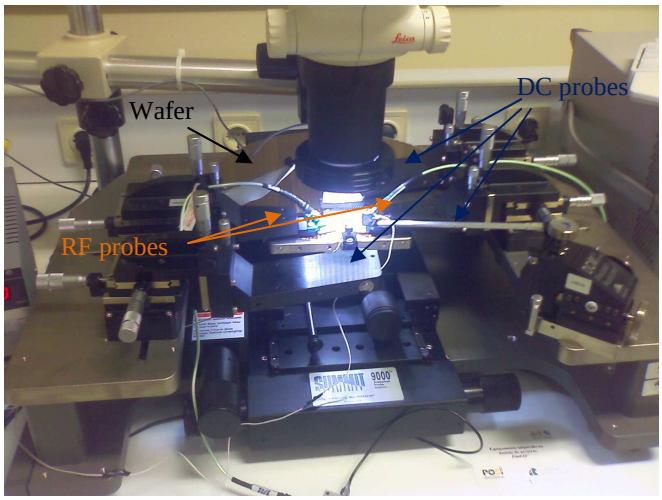

Fig. 4. On-wafer measurement setup used for IC power rails characterization (with be die being externally biased, in this case).

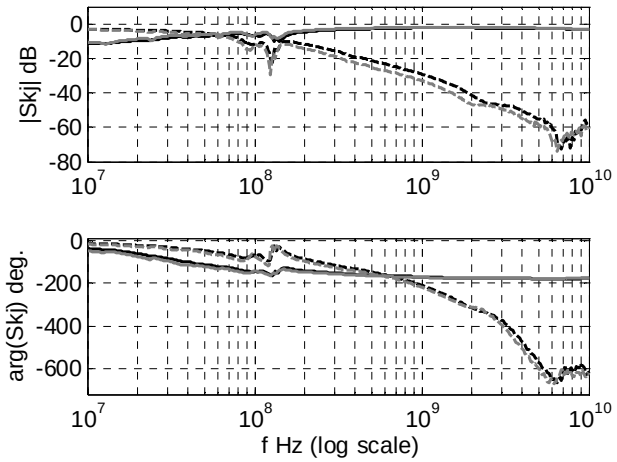

Fig. 5. A set of S-parameter measurements obtained between two pairs of VDDQ/VSSQ pads, for the proprietary test-case (in solid line is the S_{11} and in dashed line is the S_{12}; the gray curve corresponds to the unbiased case, and the black to the biased case).

From the observed results it was concluded that, for the two test-cases, the difference on the dynamic behavior of the power rail structures from the unbiased to the biased case was not significant. Also, from the S-parameter measurements performed between the VDD/VSS and the VDDQ/VSSQ power rails (using one bias-T in each of the VNA's channels) it was concluded that the cross coupling between IC core power rail and I/O buffer power rail was negligible, for the frequency range of interest (dc-3GHz), with the S_{12} magnitude being below -40 dB.

With the obtained S-parameter measurements, the parameters of the lumped models presented in Fig. 2 were then determined by least squares error minimization, being the error defined as the difference between the measured and modeled S-parameters. Fig. 6 presents an example of the fitting that was accomplished by the lumped elements model of Fig. 2, taking as fitting data the S-parameter measurements between two non-consecutive VDDQ/VSSQ ports of the die.

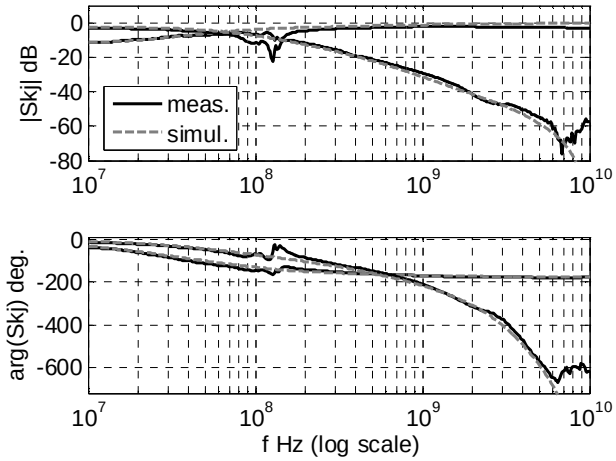

Fig. 6. Fitting the measured S-parameters with the lumped elements' model of Fig. 2, for two non-consecutive VDDQ/VSSQ ports.

For the case of the VDDQ/VSSQ power rail, the values that were considered for the lumped element parameters of the model of Fig. 2 verify that the impedance Z_S can be considered as purely resistive (for the frequency range of interest), having an estimated average value of 1.6 Ω for the proprietary test case, and 1.7 Ω for the external test-case (as the special distribution of the VDDQ/VSSQ pads is not uniform, this impedance value varies from basic cell to basic cell of the network). Note that each two-port structure of the network of Fig. 2 represents the connection between a pair of VDDQ/VSSQ pads (one port) and the point of power entry (the second port) of the I/O buffer circuit that is near the respective VDDQ/VSSQ pads. The impedance Z_P was neglected in this case since the parasitic capacitance of the I/O buffer power rail is much lower than the capacitance that the I/O buffer circuit presents to its power rail (C_B). In fact, from these measurements, C_B was estimated to be 6.3 pF for the proprietary test-case, and to 35 pF for the external test-case.

The measurements obtained for the VDD/VSS power rail reflected that this rail has a dominant capacitive behavior, and so it was represented only by a shunt capacitor whose total capacitance was estimated to 2 nF for the proprietary test-case, and to 6.5 nF for the external test-case. These apparently high values do, in fact, are coherent with the expected value when it is taken into account the high number of VDD/VSS pads spread along the die edges and with the area of the die (the VDD/VSS power rail supplies a huge number of transistors that are cover most of the area of the die). These are also within the range provided by the IC manufacturers.

C. I/O Buffer Model Characterization

As referred in Section II.B, since the SPICE netlists of the I/O buffer circuits were available for both test-cases, these were used to model the I/O buffer behavior. However, behavioral models could have been also considered, whose extraction procedure can also be based on laboratory measurements (see, for instance, [14], [21]).

IV. Measurement Setup Design

To test if the IC model platform would yield accurate results, two hardware boards were developed (one for each test-case) with the specific objective of model validation. The two boards share the same design approach that consists on a daughterboard holding the die under test, which is then attached to a motherboard – denominated Flash Fast Interface Board (FFIB) – with is based on a field programmable gate array (FPGA) that was programmed to control a memory chip. The memory chip die was assembled directly on the developed daughterboard PCB board – denominated Memory Module (MM). The die was glued to the MM and bonded, through gold bond-wires, to the MM bond-fingers. Figure 7 shows an image of the FFIB control board and in Fig. 8 it is shown one of the MM that was developed (in this case, for the proprietary test-case). The FFIB was designed with a standard interface connector which allowed different MM boards to be attached to it, and so with only one FFIB several memory chips can be tested (requiring only the design of the specific MM board).

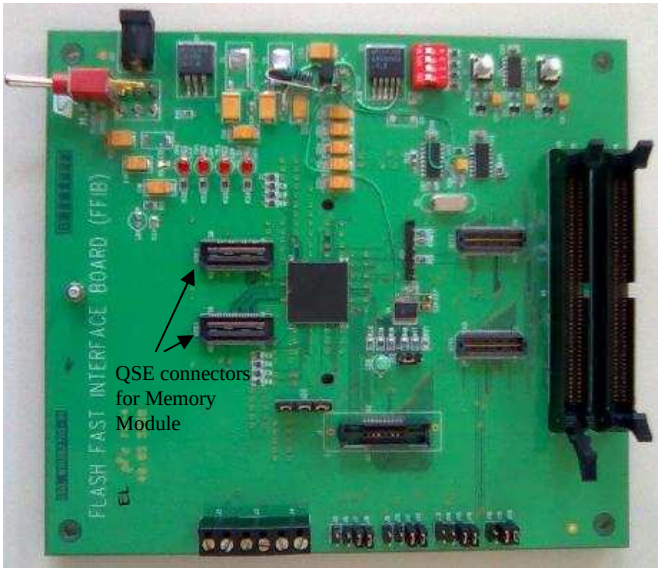

Fig. 7. Image of the FFIB control board.

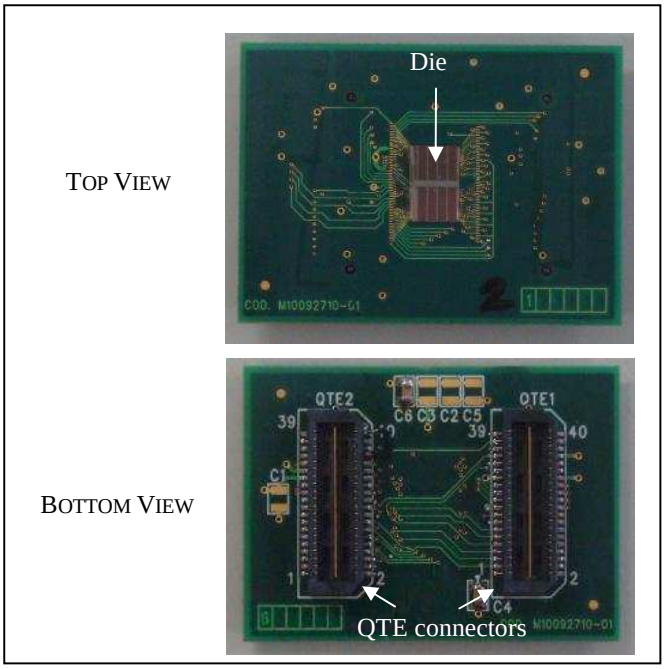

Fig. 8. Image of the MM of the proprietary device.

In order to measure the IC signals as close as possible to the IC pads, the developed MMs considered bond-fingers with an extended length for the signals to be probed (with a RF probe) directly at the bond-fingers. The distance between consecutive bond-fingers was set to 250 µm to allow the direct probing using 250 µm RF probes of the probing station. Additionally, extra paddles were also considered next to the extended bond-fingers whenever it was not possible to have in consecutive positions the two bond-fingers to be probed. Figure 9 presents an image of the extended bond-fingers and also of the additional paddles (in this case, for the external test-case MM).

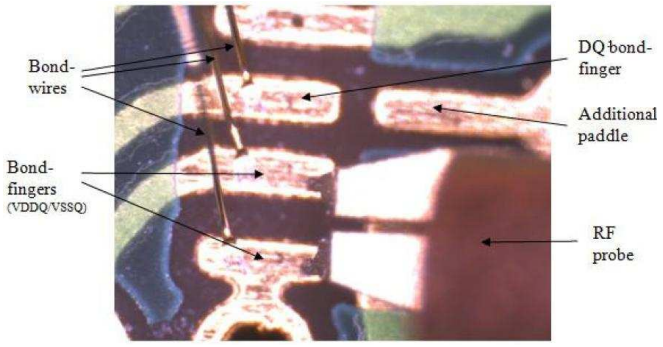

Fig. 9. Image of the extended bond-fingers and additional paddles for the external test-case MM.

To measure the voltage waveforms of the IC signals, a real time oscilloscope was used (Tektronix TDS3052B). The channels were set to the internal impedance value of 50 Ω as in this mode the channel impedance was kept almost constant for the whole frequency range considered (0 to 500 MHz). As this impedance is too low for loading the IC I/O buffer outputs, series elements were developed containing SMD resistors of 120, 270 and 330 Ω, as shown in Fig. 10. This way, the overall

impedance presented to the IC outputs was the value of the in-series resistor plus the internal 50 Ω (at the expense of signal attenuation). At the tip of each channel cable, immediately after the in-series resistor element, a on-wafer RF probe (with a pitch of 250 µm) was set. Figure 11 shows an image of the measurement workbench for the case of the external MM.

To estimate the real voltage signal that was sensed at the RF probe tips, a de-embedding procedure was employed which consisted of the inversion of the previously determined (by means of an AC sweep) transfer function from the RF probe tips to the values recorded by the oscilloscope channels (channel input impedance variation with frequency was also taken into account). This was performed by applying a fixed amplitude sine wave (using a high grade signal generator) and registering the amplitude measured by the oscilloscope for different frequencies of the sine wave. It was observed that only at high frequencies (near the limit of the oscilloscope's bandwidth) did the measured amplitude show variations. This effect was modeled by a linear transfer function which was then considered for removing such effect from the measurements. This way, the estimate of the voltage signals that were actually at the RF probe tip reference plane was determined.

Thus, the measurement set consisted of the acquisition of the I/O buffer output voltage of all buffers as the buffer inputs are switching in a controlled way by the firmware loaded into the FPGA. Figure 12 presents an example of the measured voltage on four I/O buffer output bond-fingers (after de-embedding the oscilloscope channel). Also, the measurement of the I/O buffer supply voltage (VDDQ/VSSQ) and of the IC core supply voltage (VDD/VSS) was measured in a synchronized way with the output voltage of one I/O buffer. This was to observe the influence on the supply voltages of the switching activity of the IC internal circuits. To analyze the worst case scenario, the I/O buffer outputs were programmed to switch all in a synchronous way.

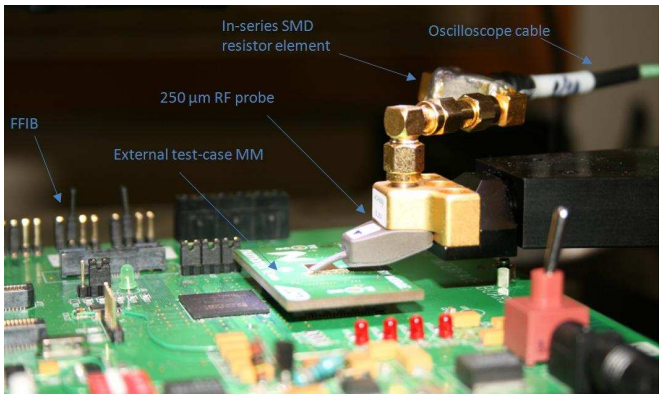

Fig. 10. Image of the developed oscilloscope probe, with an in-series SMD resistor mounted before the RF probe tip.

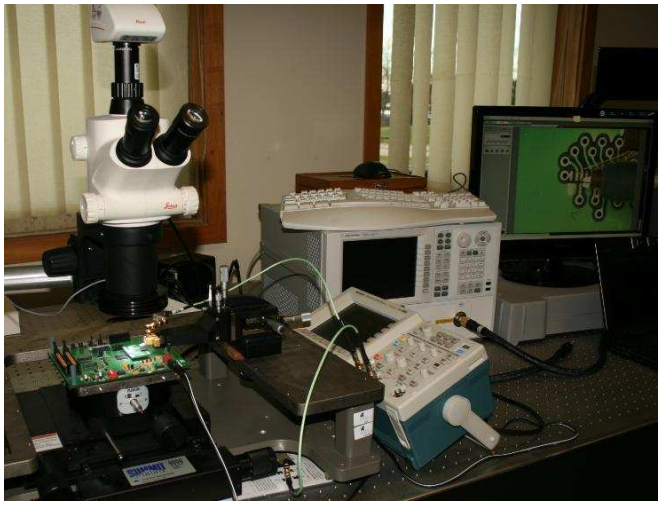

Fig. 11. Image of the measurement workbench, while probing an I/O buffer output of the external MM.

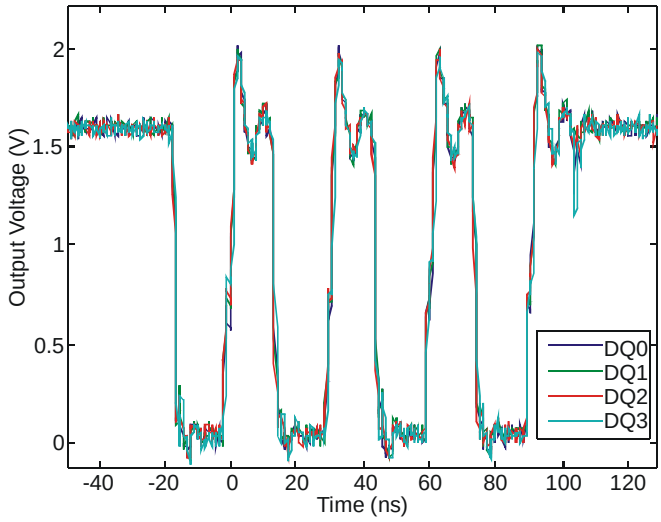

Fig. 12. Example of four measured I/O buffer output voltage signals for the proprietary test-case.

V. Global Simulation Model Implementation

To be able to cross-validate the voltage signals produced by the simulation model against the voltage signals that were measured with the setup of Fig. 11, the model must also take into account the transfer characteristics of the FFIB and MM traces (for the power supply network) and the loading effect that those traces, and also the oscilloscope probes, impose at the considered signal reference plane (the MM extended bond-fingers). For this purpose, the global simulation model was implemented in the Agilent's Advanced Design System (ADS) software.

At the starting point of this global model was the 1.8V dc power generator that supplied both the VDD/VSS and VDDQ/VSSQ power rails. This generator was modeled by a real voltage source whose internal resistance is 0.1Ω. As the dc power generator was connected to the dedicated power plane of the FFIB, such power plane was included in the model as an equivalent RLC network, from the power generator port up to

the location where the decoupling capacitors were installed (which is directly below the interfacing connector to the MM), for both the VDDQ/VSSQ and VDD/VSS power rails. To estimate the appropriate RLC values of the FFIB power networks, their S-parameters were determined between the respective two ports. For this purpose, a simplified version of the FFIB was imported into ADS (see Fig. 13) and with the Momentum tool from Agilent Technologies (which implements an electromagnetic simulation technique based on the method of moments) the S-parameters were generated.

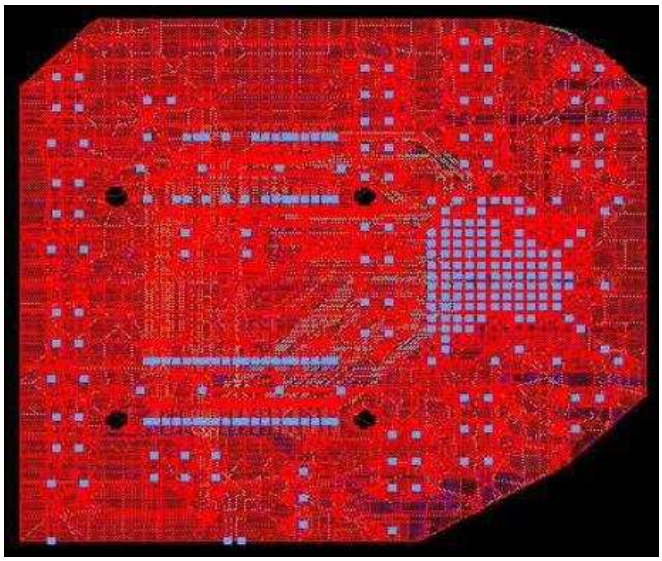

Fig. 13. Simplified version of the FFIB loaded into ADS for Momentum simulations.

A similar procedure was carried out for the characterization of the transfer function of the power rail traces on the MM boards. Through Momentum simulations, the S-parameters were determined from the MM interfacing connectors up to each pair of MM power bond-fingers. This way, a multiport equivalent SPICE circuit was determined to approximate the S-parameters determined by MoMemtum. The procedure that was used to estimate the parameters of this SPICE equivalent network was based on the Vector Fitting algorithm [17] which is a well-known state-of-the-art method for generation of reduced-order rational approximations. Passivity of the obtained rational approximations was guaranteed through the use of the technique described in [18]. In this analysis, the IDEM software of Idemworks [19] was used. Figure 14 shows an example of the fitting degree achieved. The maximum RMS error obtained was on the order of 0.006. To minimize the error introduced by the model of the MM traces, such model deliberately contained a considerable number of poles and zeros.

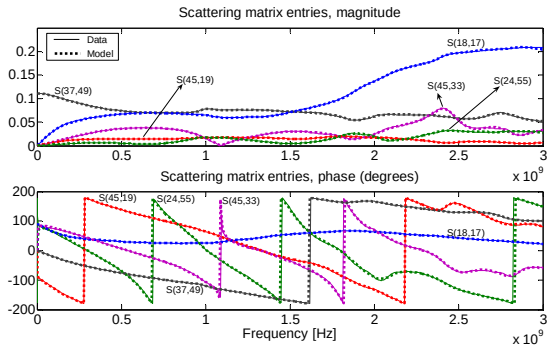

Fig. 14. Fitting the S-parameters of the proprietary test-case MM traces with IDEM [19].

Besides the bond-finger ports and the interfacing connector ports, the multiport network of the MM power traces also considered ports for the connection to the decoupling capacitors. These decoupling capacitors were also characterized through the S-parameter matching technique of IDEM, resulting on an ESR model for each capacitor, which was also included into ADS together with the multiport network.

As the MM bond-fingers are connected to the die pads through gold bond-wires, the series resistor-inductance model of each bond-wire was estimated through the use of the Momentum 3D electromagnetic simulator tool.

Finally, it was also necessary to take into account the loading effect that the data traces of the MM (which were extended through the FFIB) were imposing on the bond-fingers connected outputs of the I/O buffers. To determine the corresponding loading impedance, a MM without the die attached was connected to the FFIB and, using the on-wafer RF probes connected to the VNA, the S_{11} parameters seen from the respective bond-fingers were registered (from 10MHz to 10GHz). A reduced-order model for each output buffer port was calculated through IDEM, which was then integrated on the ADS model. Figure 15 shows an example of the measured and fitted S_{11} parameters, for the proprietary test-case. Additionally, the S_{11} parameters of the oscilloscope probes were also measured with the VNA in order to estimate the loading impedance that these were imposing on the output buffers while measuring the voltage signals. Following the approach used for the MM+FFIB data traces, the impedance of the oscilloscope probes was calculated and incorporated into the ADS model.

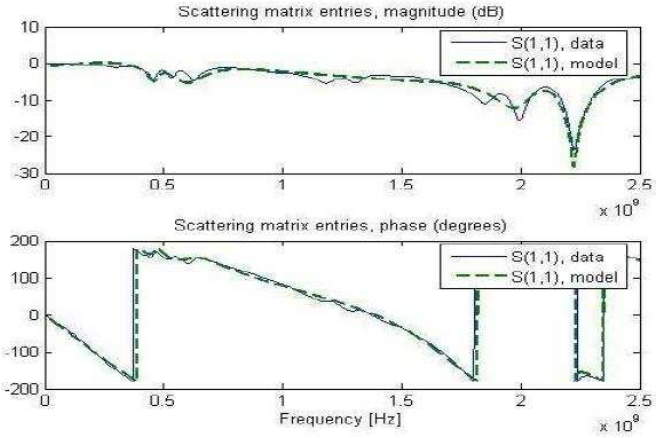

Fig. 15. Measured and fitted S_{11} parameter for the MM+FFIB loading effect on the data lines of the proprietary test-case.

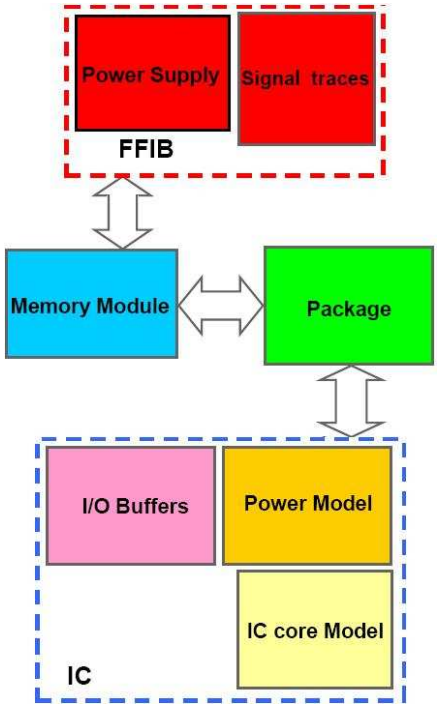

Fig. 16. Global model diagram for the simulation of IC memory chips.

At this point, all the elements were gathered into ADS forming the IC simulation model that was used in the validation tests. It includes the IC sub-system models described in Section II and extracted by the procedures of Section III, together with the power generator, transfer networks and loading impedances that were described above in this section. Figure 16 depicts the overall modeling diagram that was considered.

VI. IC Model Validation

With the complete virtual model implemented into ADS, the simulated I/O buffers output voltage signals were generated and compared with the signals measured with the real time oscilloscope at the corresponding die bond-fingers. In order to test the model under stressing conditions, all the data lines (DQ*n*, *n*=0,..,15 for both test-cases) were set to switch simultaneously. This is the situation that leads to maximum power bouncing.

It should be noticed that, since the circuit specification of the I/O buffers was available (for both test-cases), the overall signal integrity model contained the transistor-level models of the I/O buffer circuitry. As a consequence, simulation time was on the order of one hour per each clock cycle being simulated. However, system,-level models (such as those proposed in [13]-[16]) can be used for the I/O buffer blocks which would significantly improve the overall simulation efficiency (with insignificant loss of modeling accuracy, according to the results presented by such system-level models).

In the following sub-sections are presented the results that were obtained with both simulated and measured output buffer voltages, for each considered test-case.

A. Results for the Proprietary Test-case

For the I/O buffer output voltage simulation, two different sources for the switching activity current generator signals were considered: one obtained from the partial IC core simulation data (denominated SAs) and another that used the I_{SS} current signals measured through a 1 Ω resistor according to the strategy described in Section III.A (denominated SAm). For every DQn output, the simulated voltage signals were generated and plotted against the measured signal. The result for DQ0 is shown in Fig. 17. The obtained waveforms for the remaining DQ's were very similar to that of Fig. 17.

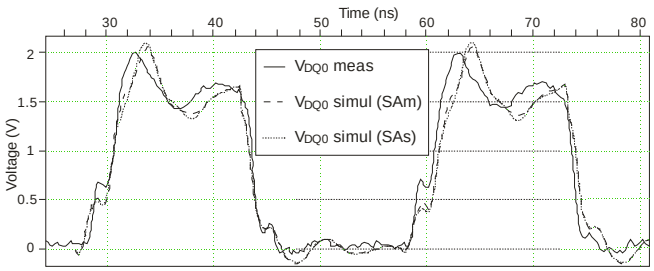

Fig. 17. Simulated versus measured voltage waveforms on DQ0 output bond-finger, for the proprietary test-case. V_{DQ0}meas is the measured waveform, VDQ0simul are the simulated voltages for both SAm and SAs switching activity generator models.

As it can be seen, the matching that was obtained with the simulation model is very good, predicting with high accuracy the bouncing of both low-high and high-low transitions of the DQ signals.

Also worth mentioning is the identical results obtained for both sources of switching activity current generators.

As the VDDQ/VSSQ power rail voltage was also simulated by the model, at the bond-fingers surrounding each I/O buffer terminals, the comparison to the measured voltage waveform was evaluated to analyze the ability that the model has to predict the bouncing of the I/O buffer power rail, at the bond-finger reference plane. Figure 18 shows these simulated waveforms confronted to the measured voltage at the

respective bond-fingers. For reference purposes, the synchronous output data voltage signal of the respective I/O buffer is also displayed.

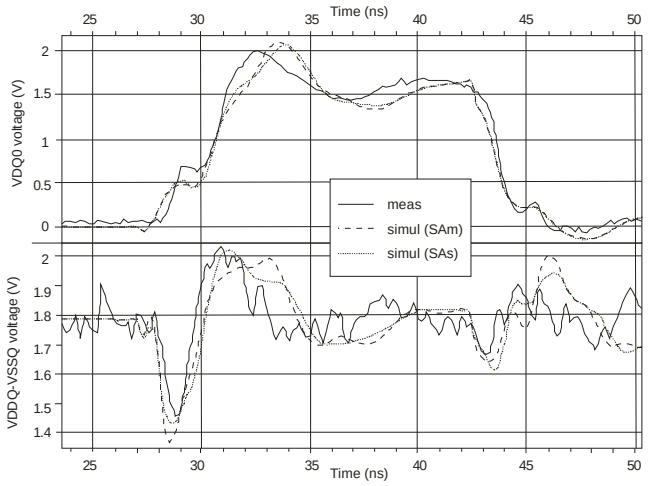

Fig. 18. Simulated versus measured voltage signals in a pair of VDDQ/VSSQ bond-fingers, for the proprietary test-case.

As illustrated on the results of Fig. 18, the developed model is able to predict the bouncing of the VDDQ/VSSQ rail with extremely good accuracy, demonstrating its usefulness for IC design processes.

A similar bouncing analysis was performed on the IC core power rail (VDD/VSS). It was observed, both by measurements and by simulations, that the variation of its voltage level was very small, on the order of some tens of mV, which falls inside the noise floor of the obtained measurements.

B. Results for the External Test-case

The validation test presented for the proprietary test-case was also performed on the external test-case. Figure 19 shows the obtained voltage waveforms, from both simulation and measurements, of one of the output buffers DQ line (on the reference plane of the bond-fingers), and also for its respective VDDQ/VSSQ power supply port.

Again, the model has demonstrated its capability of mimicking the IC (in its surrounding hardware) behavior, being able to predict with high accuracy the data line bouncing that was actually measured at the considered points. We also note that the DQ measurement presents low-level higher-frequency oscillations that the model was not able to predict in full extend, but the dominant bouncing effects, either in the up or down transitions of the signals were accurately predicted both in amplitude value and in timing, which reveals that the device dominant dynamics are being well characterized.

Furthermore, for the external test-case, a specific FPGA code for the FFIB was developed for the measurement of the eye-diagram of the output signal generated by an I/O buffer. This was also simulated by the proposed modeling approach and the results are shown in Fig. 20. Naturally, due to the jitter of the IC clock signal that was used to synchronize each signal acquisition with the real-time oscilloscope, the measured eye-diagram presents more deviation than the simulated one. However, they show a very similar pattern, and identical eye-overture.

For the VDDQ/VSSQ waveforms depicted in Fig. 19, it was noted that for the external test-case the voltage bouncing was not as severe as the one observed for the proprietary test-case. Thus, the measurement noise becomes more evident in the plot of Fig. 19. Nevertheless, the trend of the VDDQ/VSSQ signal is still clearly identified and, more important, that trend has a high correlation with the voltage signals generated by simulation model, demonstrating once more the good modeling results that were achieved.

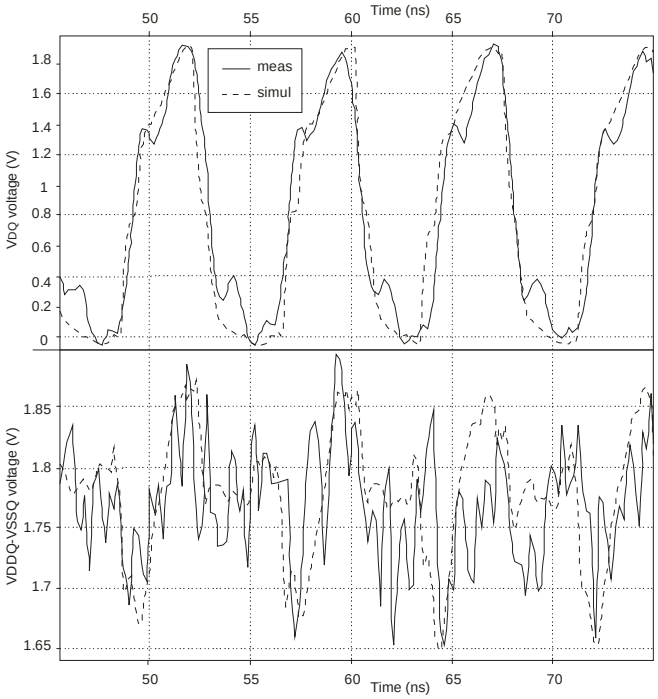

Fig. 19. Simulated versus measured voltage signals for the output of an I/O buffer and its respective VDDQ/VSSQ waveform, for the external test-case.

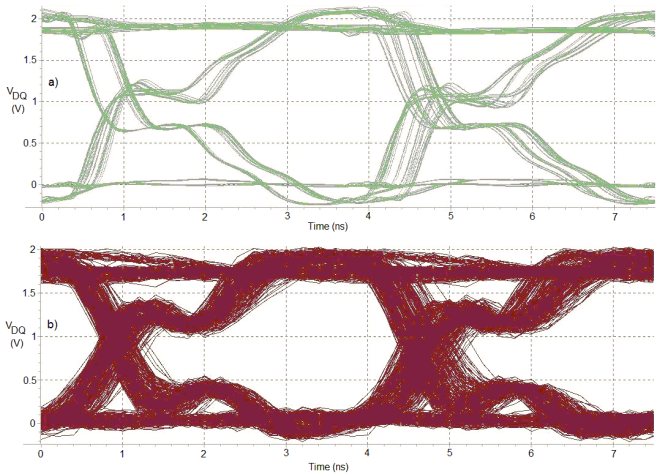

Fig. 20. Simulated (a) and measured (b) eye-diagrams of an output buffer

signal, for the external test-case.

Like in the proprietary test-case, the VDD/VSS voltage fluctuation was below the noise floor of the measurements. This was verified both by the measurements and by the simulation data.

VII. Conclusion

In this paper we have presented an IC modeling methodology dedicated to aid the design of new IC devices incorporating on or more (in a SiP architecture) dies. Identifying the IC sub-systems that are most significant for the IC behavioral characterization, the model definition considers specific sub-models for each sub-system, which can be all characterized through laboratory measurements.

The integrated IC model was validated by means of a dedicated hardware platform which was also characterized both by measurements and by electromagnetic simulations, creating in ADS a virtual environment that mimics the IC devices under test and the hardware to which they are connected (including the loading effect of the PCB boards that held the IC dies and also the loading of the measurement equipment). This virtual environment was described in detail in the text and the procedures to determine the impact of each of its components were also exposed.

From the comparison between the measured and simulated voltage waveforms, both at the I/O buffer data output lines and at the I/O buffer power supply ports (VDDQ/VSSQ), having as reference point the bond-fingers to which the die pads were bonded, it was demonstrated that the presented model approach produced extremely accurate results in both amplitude values but also on the timing characteristics of the waveforms. This means that the system dominant dynamics were correctly captured by the model.

Thus, an accurate prediction of the bouncing effects on the I/O buffer data lines, on the I/O buffer power supply ports, and also on the IC core power supply (VDD/VSS) was successfully achieved with the proposed model.

This demonstrates that the proposed strategy is suited for CAD applications involving IC development and SiP integration.

Acknowledgement

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